2^2	2^1	2^0	Command	Action
0	0	x	No Command	None
0	1	0	Read-modify-write	DRAM Read Cycle Followed by Write Cycle to Same Location (Exchange)
0	1	1	Refresh	DRAM Read Cycle with Address from Refresh Address Counter
1	0	0	Write	DRAM Write Cycle
1	0	1	Range Error Write	None
1	1	0	Read	DRAM Read Cycle
1	1	1	Range Error Read	None

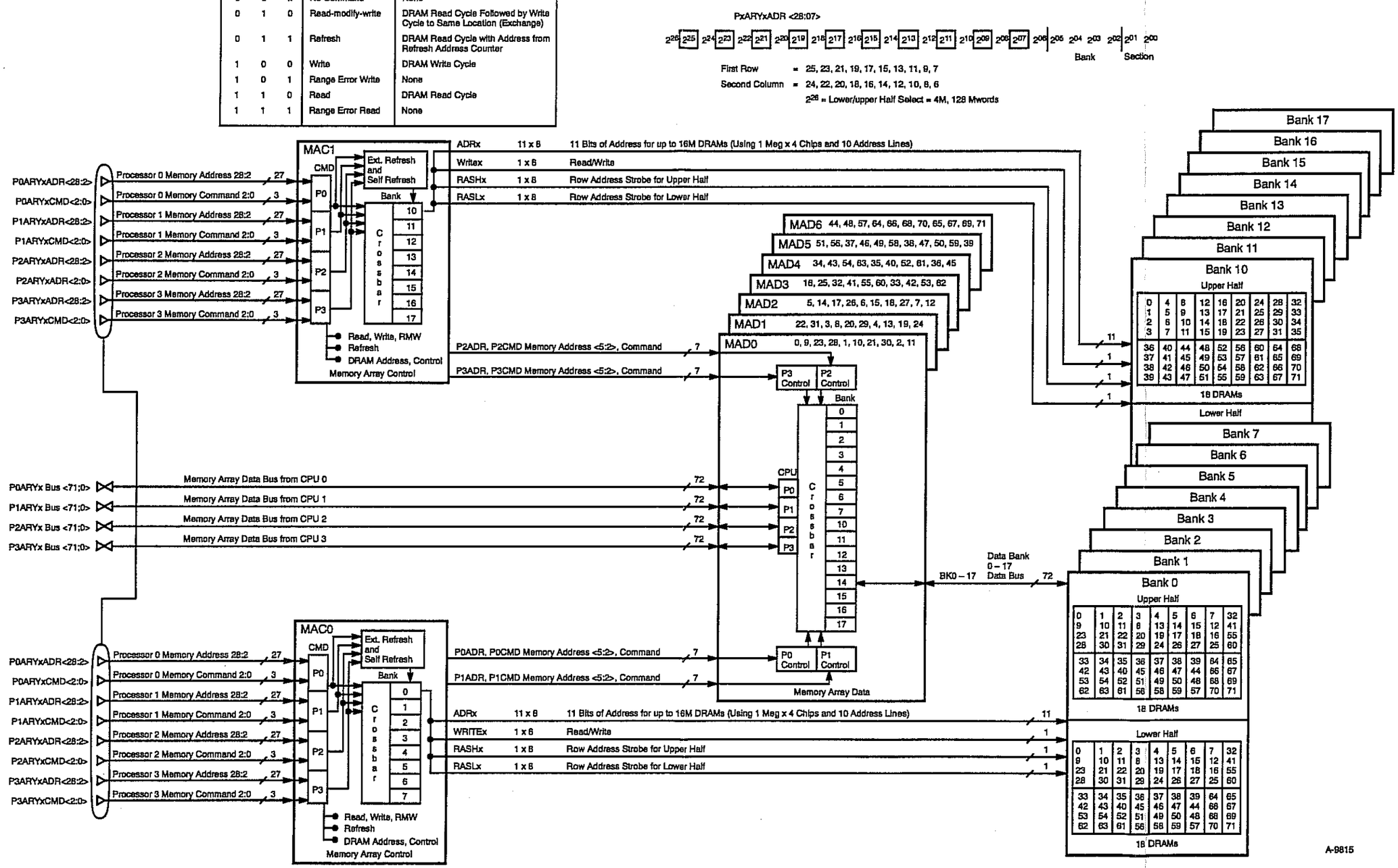

Figure 3-4. Memory Block Diagram