CZM-0934-000

MVME350/D2

MVME350
Streaming Tape Controller VMEmodule
User's Manual

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MVME350/D2

JUNE 1986

MVME350

STREAMING TAPE CONTROLLER VMEmodule

USER'S MANUAL

Second Edition

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MICROSYSTEMS

PREFACE

Unless otherwise specified, all address references are in hexadecimal throughout this user's manual.

An asterisk (*) following a signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following a signal name for signals which are edge significant denotes that the actions initiated by that signal occur on a high to low transition.

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CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, hardware preparation, installation instructions, operating instructions, functional description, and support information for the MVME350 Streaming Tape Controller (referred to as the VME350 in the remainder of this user's manual). Figure 1-1 illustrates a typical VME350 module.

1.2 FEATURES

The VME350 module features include the following:

- QIC-02 Streaming Tape Interface.
- Hardware supports up to four tape drives.
- Standard VMEbus interface.
- Intelligent Peripheral Controller (IPC) channel interface.
- 32-bit address and 16-bit data.
- Release-On-Request (ROR) VMEbus requester.
- Generates any one of the seven levels of VMEbus interrupts with programmable interrupt vector.
- 10 MHz MC68010 based processor control.
- MC68230 Parallel Interface/Timer (PI/T).
- Total of 16K bytes on-board static RAM with zero wait states on read and write (typical), and one wait state on write only (maximum).
- Confidence test and firmware supplied in 32K bytes of EPROM (supports up to 27512 devices for 128K bytes maximum EPROM).
- UNIX and VERSAdos supported firmware available.
- Diagnostic port.

1.3 SPECIFICATIONS

The VME350 module specifications are provided in Table 1-1.

Address modifiers are asserted under software control which allows the VME350 module to utilize address modes such as Short I/O, Privileged, Non-privileged, Program, and Data. Bus requests are monitored by a VMEbus requester which relinquishes the bus when another bus master requests the bus.

1.5 RELATED DOCUMENTATION

The following publications may provide additional helpful information. If not shipped with this product, they may be purchased from Motorola's Literature Distribution Center, 616 West 24th Street, Tempe, Arizona 85282; telephone (602) 994-6561.

DOCUMENT TITLE	MOTOROLA PUBLICATION NUMBER
VMEbus Specifications Manual	HB212/D
MC68010 Data Sheet	ADI-942
MC68681 Data Sheet	ADI-988
MC68230 Data Sheet	ADI-860

The QIC-02 Cartridge Tape Drive Intelligent Interface Standard (Revision D) may be obtained from Archive Corporation, 3540 Cadillac Avenue, Costa Mesa, California 92626; telephone (714) 641-0279.

CHAPTER 2

HARDWARE PREPARATION AND INSTALLATION INSTRUCTIONS

2.1 INTRODUCTION

This chapter provides the unpacking and hardware preparation instructions for the VME350 module.

2.2 UNPACKING INSTRUCTIONS

> **NOTE**
>
> If shipping carton is damaged upon receipt, request that the carrier's agent be present during unpacking/inspection of equipment.

Unpack and remove the module from its shipping carton. Refer to the packing list and verify that all items are present. Care should be taken during the unpacking of the module. Save the original shipping container and packing material for storing or reshipping of the module.

> **CAUTION**
>
> AVOID TOUCHING AREAS OF INTEGRATED CIRCUITS; STATIC DISCHARGE CAN DAMAGE THESE CIRCUITS.

Inspect for any shipping damage. If no damage exists, the module can then be prepared (jumper configurations) and readied for system installation.

2.3 HARDWARE PREPARATION

This section describes the hardware preparation of the VME350 prior to installation. Observance of this description will ensure the user that his VME350 components are properly configured for operation.

Jumpers are used to select various functions and options of the VME350 module. Before system installation, the user should verify the jumper configuration and alter the jumpers, as required, for the user's particular system operation. The VME350 has been factory tested for system operation and is shipped with factory-installed jumpers that are illustrated in Figure 2-1. The VME350 is operational with the factory-installed jumpers.

One eight-position DIP-type switch (S1) is located on the VME350 module. For additional information regarding the use of this switch, refer to Chapter 3.

Table 2-1 lists each VME350 jumper block by designation, function, and factory-installed configuration. A more detailed description of these jumper blocks is provided in the following sections.

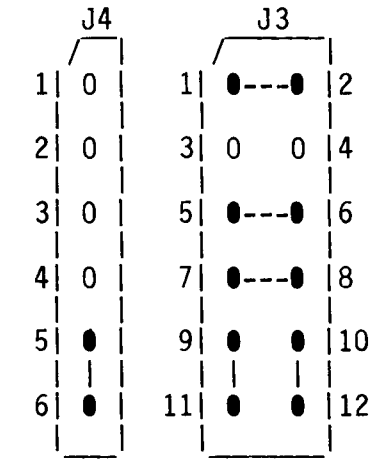
2.3.1 VME350 Jumper Settings

TABLE 2-1. VME350 JUMPERS

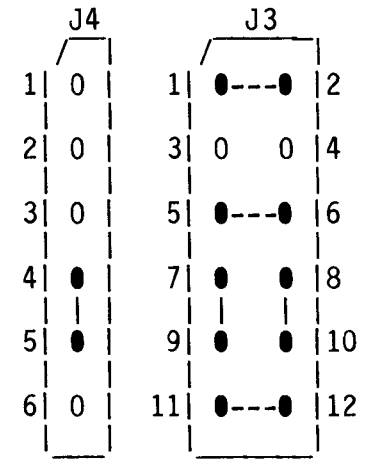
Jumper	Function	Factory Configuration	
J3	VMEbus Grant Level	(1-2), (5-6), (7-8), (9-11), (10-12)	[Bus Grant Level 3]
J4	VMEbus Request Level	(5-6)	[Bus Request Level 3]
J5	10 MHz Clock to PI/T Enable	(1-2)	Enabled
J6	RAM Size Selection	(2-3), (5-6)	[6264 Devices]
J7	DTACK Enable	(1-2)	Enabled
J8	ROM Size Selection	(2-3), (5-6), (7-8)	[2764 or 27128 Devices]

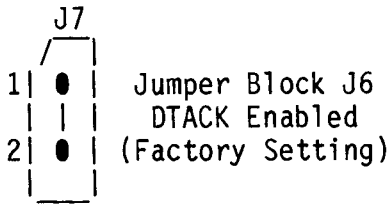
2.3.1.1 VMEbus Request/Grant Level (J3, J4). The VMEbus has four prioritized request lines (BR0* to BR3*) with each having an associated bus grant daisy-chain. Level 3 is the highest priority and level 0 the lowest. Jumper blocks J3 and J4 allow the user to select the desired priority level of the VME350 for VMEbus requests. The following configurations provide the proper jumpering for each bus arbitration level. Note: No other configurations will work properly.

VMEbus Request/Grant Level 3 (Factory Setting)



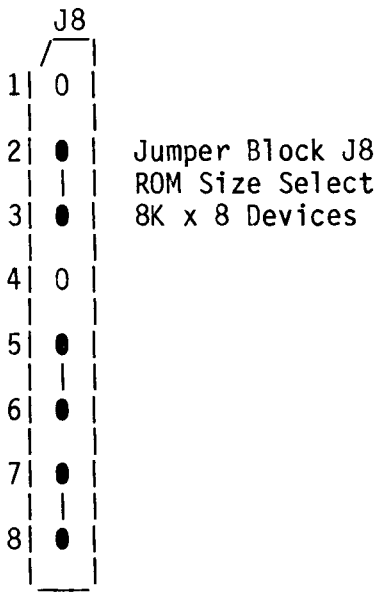
VMEbus Request/Grant Level 2

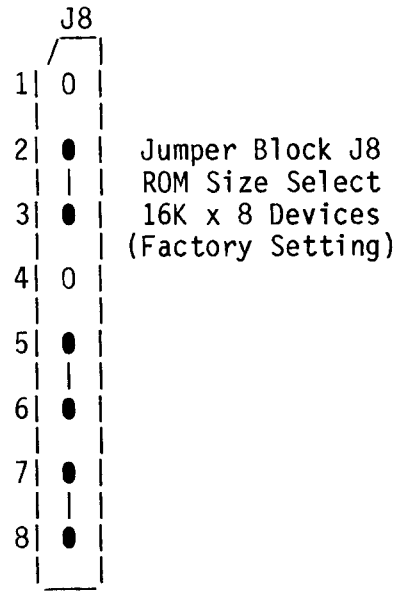


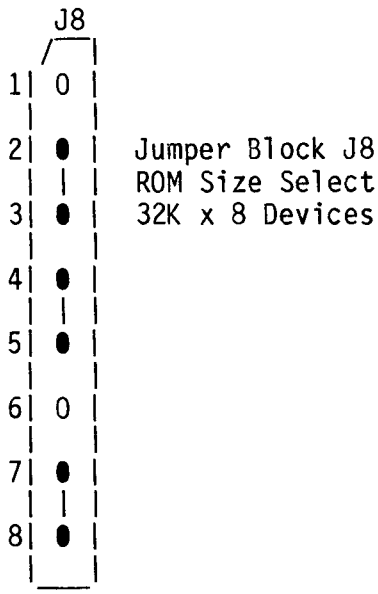


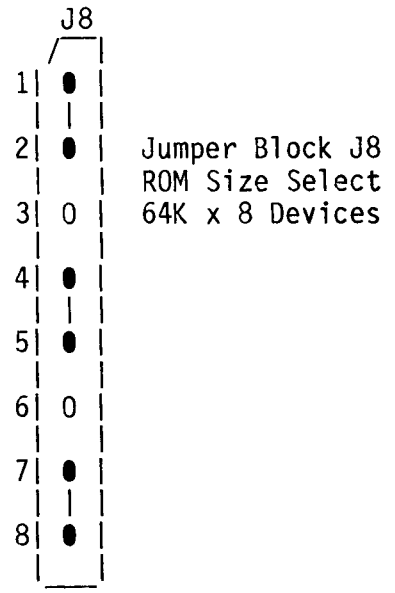
2

2.3.1.5 ROM Size Selection (J8). Jumper block J8 configures ROM sockets U40 and U47 for the desired ROM size. The VME350 module is capable of accepting ROMs ranging in size from 8K to 64K by 8.









2.4 INSTALLATION INSTRUCTIONS

When the VME350 module has been prepared (configured by the user) as desired, it is ready for system use and can then be installed in a VMEmodule chassis.

CHAPTER 3

OPERATING CONTROLS AND INDICATORS

3.1 INTRODUCTION

This section describes the controls and indicators found on the VME350 module.

3.2 FRONT PANEL

The VME350 front panel is illustrated in Figure 3-1. As shown, the HALT, FAIL, and RUN indicators are located on this panel.

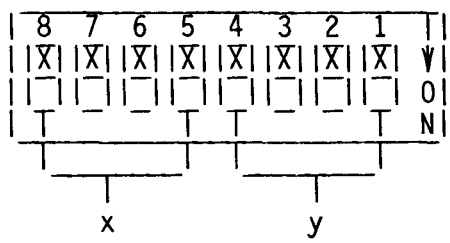
The HALT indicator is a discrete red LED which will be lit whenever the MC68010 processor is in reset or halted.

The FAIL indicator, also a discrete red LED, is controlled by a software register. The FAIL LED will normally indicate a problem on the VME350.

The RUN indicator, a discrete green LED, relates to the Q2 control/status control register, in the PI/T, and is used to indicate when the ONLINE* signal is asserted to the Q2 drive.

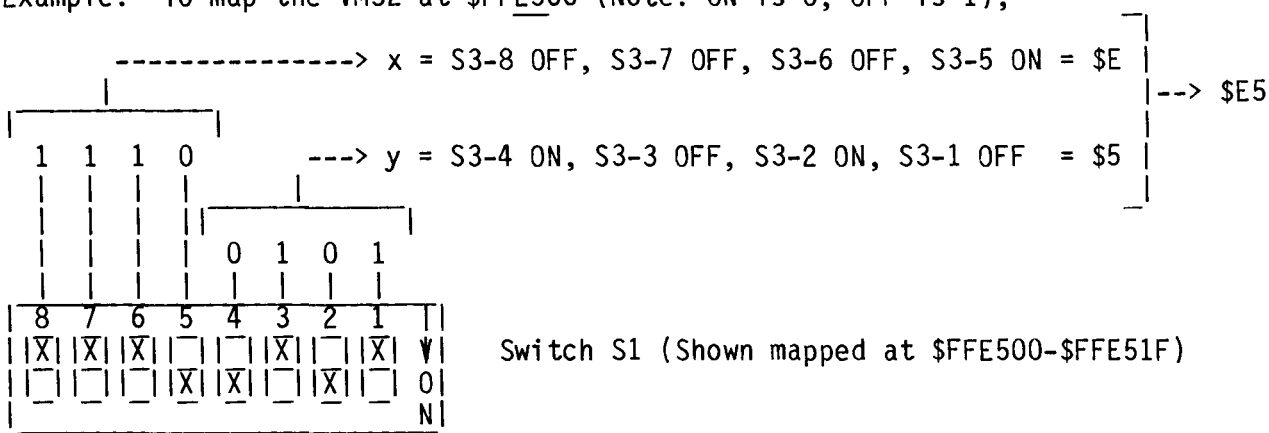
3.3 SWITCH S1 (VMEbus Mapping)

Switch S1 is an eight-position DIP switch that is used to select the VMEbus mapping boundary for the VME350 VMEbus CSR (VCSR). The VCSR is described in section 4.4.2. This switch will map the VME350 to any 256-byte boundary in the Short I/O space: $FFxy00, where x and y are determined as shown below. Note: ON is 0, OFF is 1. The VME350 will occupy the first 32 bytes: $FFxy00-$FFxy1F.



Switch S1 (Shown mapped at $FFFF00-$FFFF1F in the Short I/O space)

Example: To map the VM32 at $FFE500 (Note: ON is 0, OFF is 1),



Switch S1 (Shown mapped at $FFE500-$FFE51F)

CHAPTER 4

FUNCTIONAL DESCRIPTION

4.1 INTRODUCTION

This chapter provides a general description of the overall VME350. For further details, refer to the block diagram (Figure 4-1) and the schematic diagram in Chapter 5 (Figure 5-2).

4.2 GENERAL DESCRIPTION

The VME350 may be a 24-bit (standard) or 32-bit (extended) VMEbus master. All accesses to the VMEbus are made through an eight-megabyte window. This is accomplished using a nine-bit extended address register which allows access to the entire four gigabytes available in 32-bit systems. Bus error protection is provided for each end of the VMEbus window to reduce range checking for access to global memory. Address modifiers are asserted under software control which allows the VME350 to utilize any addressing mode such as Short I/O, Privileged, Non-privileged, Program, and Data.

An IPC VMEbus Control and Status Register (VCSR) space is provided for another VMEbus master to control the IPC initialization and operation. This shared area is 32 bytes deep and may be mapped on any 256-byte boundary in the 64K VMEbus Short I/O space via the eight-position switch S1. Functions that are provided include: registers for passing addresses and address modifiers, a Test and Set (TAS) bit for CSR control, a reset (RST) bit for holding the IPC in reset, and an attention (ATN) bit for causing an interrupt to the IPC microprocessor.

The VME350 uses a Release-On-Request (ROR) VMEbus requester. All bus request lines are monitored and the bus relinquished anytime another bus master requests the bus. Early Bus Busy (BBSY*) release is also used to hide the VMEbus arbitration time when the bus is requested during a VME350 VMEbus cycle.

There are 16K bytes of static RAM with the capability of 64K bytes.

The EPROMs provided contain confidence tests and firmware in 27128 devices. The 28-pin sockets will support up to 27512 devices with access times of 200 nanoseconds, giving 128K bytes of EPROM with one CPU wait cycle maximum (zero wait cycle typical) as the upper size limit. The EPROMs will image throughout the 128K-byte address space for sizes less than 27512s.

A diagnostic port is available at J1 (a 26-pin connector). This port is used for factory test engineering. The QIC-02 interface is made through a 50-pin ribbon connector at J2 (front) or at P2 (rear).

4.2.1 Central Processing Unit - MC68010

The Central Processing Unit (CPU) for the VME350 is a MC68010 Virtual Memory Microprocessor (U39). This is a Pin-Grid-Array (PGA) device with a clock speed of 10 MHz. The CPU controls the local address and data busses (LA BUS and LD BUS, respectively). The ROMs (U40 and U47), RAMs (U33 and U44), PI/T (U27), local control/status registers, and the serial diagnostic port are available to the CPU over these local busses.

4.2.2 Diagnostic Port

Included on the VME350 is a diagnostic port. The physical location of this port is the 26-pin J1 connector. This diagnostic port is used for factory test engineering. Under normal system operation there should be no connection made to the diagnostic port since the port is not supported by the firmware. See Table 5-3 for information about the signals which make up the diagnostic port.

4.2.3 Q2 Interface

QIC-02 is an intelligent interface for streaming tape drives. With the intelligence built into the interface, the host (in this case the VME350) is relieved of the overhead functions such as tape formatting, error processing, and tape positioning.

QIC-02 has an eight-bit wide bidirectional data bus for moving both commands/status and data. There are eight control lines, four from the tape drive to the host, and four from the host to the tape drive. These lines report exceptions from the drive, reset the drive, and perform the handshaking for the data. There are two pairs of handshaking lines, one pair for the movement of data, the other pair for the commands and status. Both handshakes are asynchronous, therefore, eliminating tight timing constraints.

There are three different sets of commands that are defined for QIC-02: standard commands, optional commands, and vendor unique commands. All of the standard commands are supported by the VME350 firmware (refer to the MVME350 Firmware User's Manual for more information). The following chart provides a list of the QIC-02 standard command set. A complete explanation of the commands can be found in the QIC-02 Interface Standard Specification (Rev D).

QIC-02 Standard Commands

Select Drive	Write Filemark
Beginning of Tape	Read Data
Erase Tape	Read Filemark
Retension Tape	Read Status
Write Data	

The implementation of the QIC-02 interface on the VME350 involves the local processor and the MC68230 PI/T (Parallel Interface/Timer). A state machine for the control of the handshaking lines for the interface has been implemented in a registered PAL, herein referred to as the Q2PAL.

4.3 ADDRESS DECODE

4.3.1 Local Mapping

Figure 4-2 illustrates the VME350 local memory map. Minimum address decoding is used to simplify the design. A "guardrail" mechanism is employed to give a bus error when an access to the VMEbus exceeds the window boundary. The addresses for the individual local registers can be found in register description. A more detailed address map is shown in Table 4-1.

TABLE 4-1. LOCAL ADDRESS MAP

Physical Address	Device/Register	Comments
000000-01FFFF	ROM	128K bytes; read only.
020000-03FFFF	RAM	64K bytes; read/write.
040000-05FFFF	Local CSR	Local Control/Status Registers
Details:		
040000	**	
040001	PCSR	Processor Control and Status Register
040002-040003	AER	Address Extension Register
040004	**	
040005	*	
040006	**	
040007	IVR	VMEbus Interrupt Vector Register
040008	**	
040009	DIAGSEL2	Diagnostic Port Select LED; write only
04000A-05FFFF	---	Multiply Mapped LCSR
060000-07FFFF	VCSR	VMEbus Control/Status Registers
Details:		
060000-060003	IAR	IPC Address Register
060004	IAMR	IPC Address Modifier Register
060005	---	Undefined
060006	ICR	IPC Control Register
060007	---	Reserved
060008-060009	ISR	IPC Status Register
06000A	IMDBR	IPC MDB/ID Register
06000B	---	Reserved
06000C	IAVR	IPC Abort Vector Register
06000D	---	Undefined
06000E-06000F	---	TAS Register
060010-06001F	---	Undefined
060020-07FFFF	---	Multiply Mapped VCSR
080000-08003F	PI/T	PI/T (Q2 Reg, Address Modifier Register, etc)
080040-09FFFF	---	Multiply Mapped PI/T
0A0000	**	
0A0001	Q2 COMMAND	QIC-02 Command Register
0A0002-0BFFFF	---	Multiply Mapped Q2 Command Register (at odd locations)
0C0000-0C0001	Q2 DATA	QIC-02 Data Register (Word Access Only)
0C0002-0DFFFF	---	Multiply Mapped Q2 Data Register
0E0000-0E001F	DIAGSEL2	Diagnostic Port Select (DUART)
0E0001-7FFFFF	---	Multiply Mapped Diagnostic Port
800000-FFFFFF	VMEbus	VMEbus Window

Notes: * Access to these addresses will return undefined data.
** Access to these addresses will result in a bus error unless a word access is made which includes a valid location.

Example: A byte access to $0A0000 will cause a bus error although a word access to $0A0000 will return undefined data in the upper byte and the value of the PCR in the lower byte.

4.4.1.1 Processor Control and Status Register (PCSR)

TABLE 4-2. PROCESSOR CONTROL AND STATUS REGISTER

Address: $040001 — Schematic: Sheet 7

Dx	Signal Name	La?	Re?	Access	Function/Description
0	PCSR1	Y	0	R/W	Generates a VMEbus interrupt at the level written into these bits.
1	PCSR2	Y	0	R/W	
2	PCSR3	Y	0	R/W	
3	IRQMSK	Y	0	R/W	Set; Masks all interrupts from CPU.
4	SYSFAIL	Y	0	R/W	Set; Disables SYSFAIL* signal to VMEbus.
5	TMOERR	Y	0	R/W	Set; Indicates a local timeout has occurred.
6	----	---	---	---	----
7	----	---	---	---	----

Note: Bits 0 through 2 should not be set to 1 unless a VMEbus interrupt is desired.

4.4.1.2 Address Extension Register (AER)

TABLE 4-3. ADDRESS EXTENSION REGISTER

Address: $040002-$040003 — Schematic: Sheet 8

Dx	Signal Name	La?	Re?	Access	Function/Description
0:6	---	N	-	--	Unconnected. Not defined when read, no effect when written to.
7	A23	Y	0	WO	This register contains the two upper address bytes that will be asserted onto the VMEbus if a bus cycle is run. This register may be written using byte, word, or longword (see note). Any read of this register will result in a bus error and must be written to as a word or longword.
8	A24	Y	0	WO	
9	A25	Y	0	WO	
10	A26	Y	0	WO	
11	A27	Y	0	WO	
12	A28	Y	0	WO	
13	A29	Y	0	WO	
14	A30	Y	0	WO	
15	A31	Y	0	WO	

Note: $040004 and $040005 are left unused to give longword write capability to this register.

4.4.1.5 Q2 Control/Status Register (Q2CSR) - Port A of PI/T

TABLE 4-6. Q2 CONTROL/STATUS REGISTER

Address: $080011 — Schematic: Sheet 7

Dx	Signal Name	La?	Re?	Access	Function/Description
0	ONLINE	Y	x	R/W	Asserts the ONLINE signal to the tape device.
1	RESET	Y	x	R/W	Asserts the RESET signal to the tape device.
2	REQHLD*	Y	x	R/W	Enables the REQUEST signal to the tape device during a Read Status Command.
3	-----	Y	x	R/W	Not Used.
4	RDY*	Y	x	R	Status of the READY signal from the tape device.
5	EXCP*	Y	x	R	Status of the EXCEPTION signal from the tape device.
6	-----	Y	x	R/W	Not Used.
7	ROMDIS*	Y	x	R/W	ROM Disable = Low addresses will bus error (i.e., 0000XX, where X = Don't Care).

x = Not affected by Reset; but all pins are defined as inputs after Reset.

4.4.1.6 Address Modifier Register (AMR) - Port B of PI/T

TABLE 4-7. ADDRESS MODIFIER REGISTER

Address: $080013 — Schematic: Sheet 13

Dx	Name	La?	Re?	Access	Function/Description
0	AM0	Y	0	R/W	Contains the Address Modifier code that will be asserted if a VMEbus cycle is run. The reset default is AM = 00 which is equivalent to a float on the VMEbus.
1	AM1	Y	0	R/W	
2	AM2	Y	0	R/W	
3	AM3	Y	0	R/W	
4	AM4	Y	0	R/W	
5	AM5	Y	0	R/W	
6	-----	Y	0	R/W	Not Used.
7	-----	Y	0	R/W	Not Used.

4.4.2 VMEbus CSRs

The following sections define the VMEbus Control/Status Registers (VCSRs) as they are implemented on the VME350 module. All locations are read/writable from the local processor and VMEbus. For a definition of VMEbus addressing, refer to section 3.3. Figure 4-3 illustrates the VMEbus CSR Address Mapping.

	31 ... 16		15 ... 0	
060000	IPC Address Register (MSW)	060001		
060002	IPC Address Register (LSW)	060003		
060004	IPC Address Modifier Register	060005	--------	
060006	IPC Control Register	060007	Reserved	
060008	IPC Status Register	060009	Reserved	
06000A	IPC MDB/ID Register	06000B	Reserved	
06000C	IPC Abort Vector Register	06000D	--------	
06000E	TAS Register	06000F		
060010	--------	060011	--------	
060012	--------	060013	--------	
060014	--------	060015	--------	
060016	--------	060017	--------	
060018	--------	060019	--------	
06001A	--------	06001B	--------	
06001C	--------	06001D	--------	
06001E	--------	06001F	--------	

The above addresses are relative. The physical address on the bus depends on where the VME350's VCSR is mapped (see section 3.3). The line (------) above indicates undefined R/W locations that may be used to pass data to and from the VME350.

FIGURE 4-3. VMEbus CONTROL/STATUS REGISTER ADDRESS MAPPING

4.4.2.1 IPC Address Register (IAR)

IAR: R/W both sides Local: 060000-060003 VMEbus: FFxy00-FFxy03

This is a general purpose register used to pass addresses to and from the IPC.

4.4.2.6 IPC Abort Vector Register (IAVR)

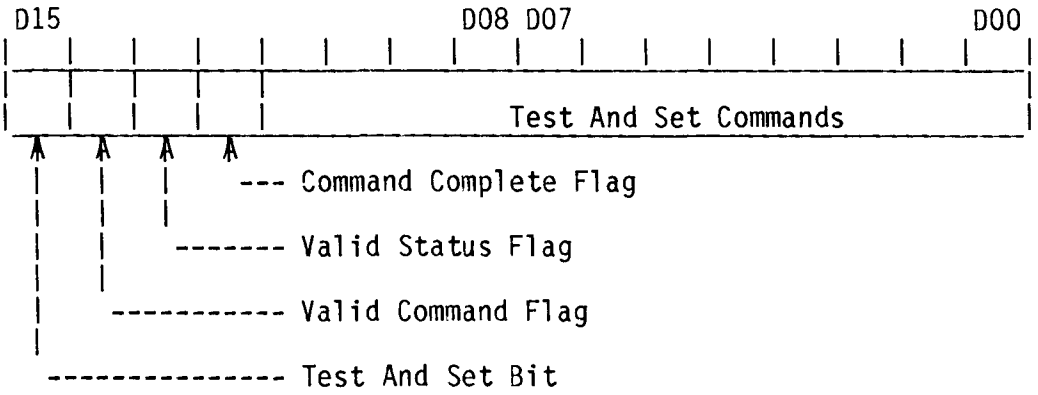
IAVR: R/W both sides Local: 06000C VMEbus: FFxy0C

This register is loaded by the host and should contain the vector that the IPC will supply during an emergency interrupt cycle. This would be used in the case where the IPC has faulted and cannot recover on its own.

4.4.2.7 IPC TAS Register (ITASR)

ITAS: R/W both sides Local: 06000E-06000F VMEbus: FFxy0E-FFxy0F

The IPC TAS Register is used when CSR commands are issued to the IPC. The bit definitions for the IPC TAS Register are shown below.



Bit 15 Test And Set (TAS). This bit is used to gain access to the CSR space of the IPC. Set by the host, this bit acts as an interlock to allow only one host at a time to issue CSR commands to the VME350.

Bit 14 Valid Command Flag. Set by the host to indicate to the VME350 that a CSR command has been loaded and the VME350 can execute it.

Bit 13 Valid Status Flag. This bit is set by the VME350 to indicate to the host that the CSR command has been completed and the command status has been loaded into the CSR status register.

Bit 12 Command Complete Flag. This bit is set by the host to indicate to the VME350 that it has read the status register and the VME350 can clear the CSR space including the TAS bit.

Bits 11-Bits 00 Test And Set Commands. These bits (zero through eleven) write the CSR command op-code into the IPC TAS register.

4.5 MEMORY

4.5.1 ROM

The VME350 is designed to accommodate two JEDEC standard 28-pin devices. Jumper selection (refer to section 2.3.4) permits the use of compatible 28-pin 8K, 16K, 32K, and 64K byte devices. The following 28-pin EPROMs with access times of 200 nanoseconds or less are supported:

4.7.1 Interrupt Generation

All seven levels of VMEbus interrupts are supported and any interrupt level can be selected under software control. All interrupts are disabled at power-up.

4.7.2 DTB Requester

The VMEbus requester is a Release-On-Request (ROR) device. All bus request lines (BR0* through BR3*) are monitored by the ROR requester.

4.7.3 VMEbus Options

The following options are supported in accordance with the VMEbus Specification.

D16 - Data path width of 16 bits.
A24 or A32 - 24 or 32 bits of address can be generated/decoded.

4.8 QIC-02 INTERFACE

The local processor is involved in all aspects of the QIC-02 interface. It is responsible for all data transfers, the issuing of commands, and the reading of status. It must transfer data between both the QIC-02 interface and the buffer RAM, and between the buffer RAM and the VMEbus, at a rate that will keep the tape device in a continuous streaming operation.

All data transfer done by the local processor will be 16 bits wide. This 16-bit word is transferred through the QIC-02 interface a byte at a time by the Q2PAL. The address location for the QIC-02 interface for data transfers is $C0000.

The address $A0001 should be used by the local processor to issue commands and read status. All transfers of this type will be eight bits wide. It is necessary to have two different address locations for commands/status and data to enable the Q2PAL to handshake with the interface on the correct set of lines.

The Q2PAL has been configured as a state machine to handle the handshaking signals necessary for the QIC-02 interface, and the control lines for the data latches. The signals required by the tape device are the command/status handshake line REQUEST and the data handshake line TRANSFER. The Q2PAL will also do the data byte swapping to split the 16-bit word which the processor uses to the 8-bit byte that the QIC-02 interface expects.

The following timing diagrams (Figures 4-4 through 4-7) illustrate the timing parameters involved for various Q2 commands and data transfers. Reference should be made to the VME350 schematic sheet 13 and to the appropriate figure for the following description on QIC-02 timing. Note: All time constraints shown are taken from the QIC-02 specification. Refer to that document for further information on the QIC-02 interface.

4.8.1 Command Issue

The format for a command issuance to the QIC-02 drive falls under two types. Figure 4-4 illustrates the timing associated with all commands with the ex-

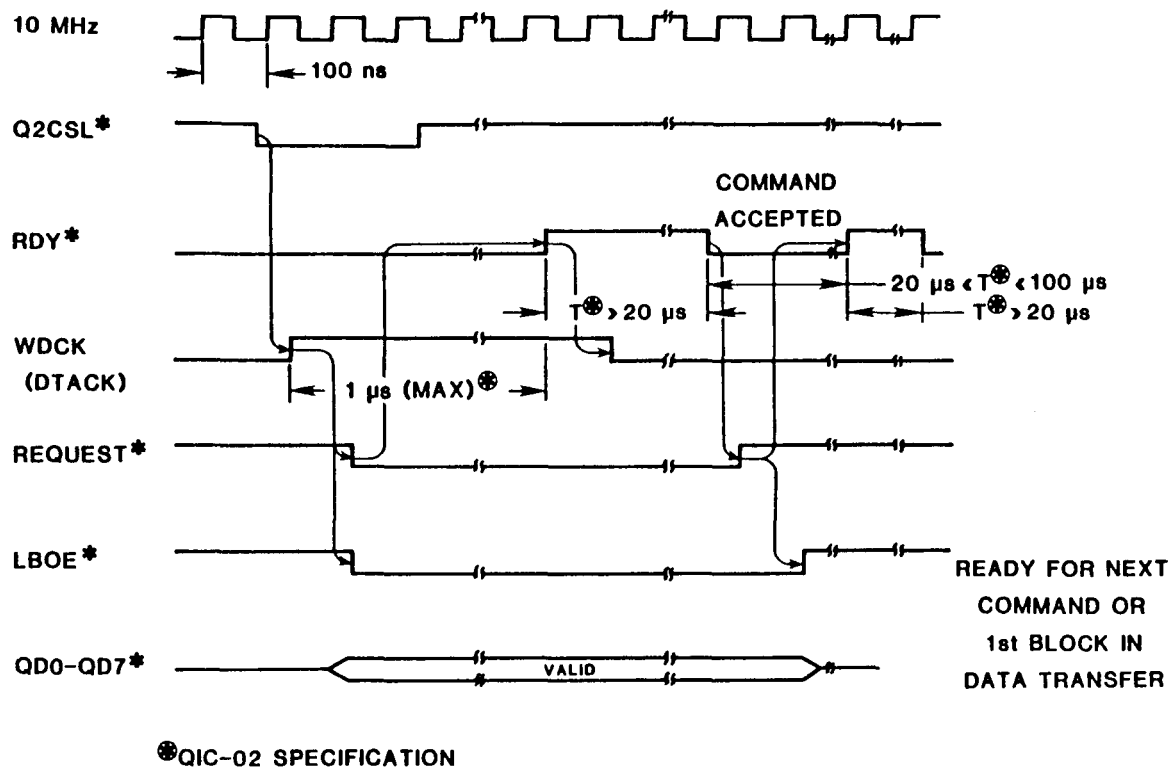


FIGURE 4-4. SELECT, BOT, INIT, ERASE, WRITE DATA, OR READ DATA COMMAND

serted next and this is initiated after the CPU polls for the RDY* (asserted) and then performing a write word cycle to address C0000. This generates a Q2DSL* (QIC-02 Data Select Line) which creates WDCK (Write Data Clock). This signal clocks 16 bits of data from the local data bus into latches U64 and U69. Since the QIC-02 interface is an 8-bit bus, the VME350 executes two QIC-02 cycles for every 16-bit CPU cycle. WDCK also generates LBOE* which output enables to the drive (the lower byte of the 16 bits written by the processor). LBOE* then generates XFER* to the drive. These signals all originate out of the Q2PAL (U58). The drive then removes RDY* and ultimately asserts LTCHACK* (Latched Acknowledge) indicating that it has accepted the first byte. The XFER* signal is then removed. Later the drive removes LTCHACK* which indicates it is read for the next byte. The Q2PAL then removes LBOE* and asserts HBOE* (High Byte Output Enable) which outputs the high byte of data that was stored in U64. XFER* is then asserted to the drive. The drive then asserts LTCHACK* with the Q2PAL removing HBOE* and XFER* and the drive removing LTCHACK* in response. This completes the first word that had been written by the processor. If the CPU had tried to write another word into the Q2 latches prior to this time, the Q2PAL would have held off the cycle until the second byte (or even byte) of the transfer had been completed (indicated by LTCHACK* going high). The next and subsequent Q2DSL* will initiate the transfers to the QIC-02 bus. Each word transfer will look like this figure (except for RDY* which will be re-asserted) up to and including 256 word (CPU) or 512 byte (QIC-02) transfers. After the 512th byte transfer, the CPU software will wait for RDY* to be asserted by the drive, indicating that it is ready for the next block of data. The entire sequence proceeds again as illustrated in Figure 4-6.

Read Data

A Read Data Transfer is initated if RDY* is asserted by the drive indicating that the command has been accepted. Figure 4-7 illustrates the associated timing during a Read Data Transfer. The CPU will poll for the command accepted RDY* signal. The drive will then assert the LTCHACK* indicating it has the first byte of data available on the QIC-02 bus. When Q2DSL* and LTCHACK* are valid, XFER* is asserted and then LBCK (Low Byte Clock) goes active and clocks the byte (D00 through D07) of information into latch U68. The drive responds to XFER* by removing RDY* and then LTCHACK*. RDY* will not re-assert until the next block of data is ready to be transferred. The removal of LTCHACK* will cause XFER* to de-assert. The drive then responds by re-asserting LTCHACK* when it has the next byte of data available. XFER* is asserted again and HBCK (High Byte Clock) goes active clocking this byte of data into the high byte (D08 through D15) latch U63. HBCK causes ROE* (Read Output Enable) which enables the previous byte (D00 through D07) and the current byte (D08 through D15) onto the local data bus. The CPU cycle has been held off until this second byte of data was ready and ROE* also generates a DTACK* to the processor releasing the CPU cycle thus Q2DSL* de-activates removing LBCK and ROE* in the process. The drive will remove LTCHACK* and the Q2PAL responds by removing XFER*. When the drive has another byte of data, the sequence will start over again, the CPU taking one word (16 bits) every 2 bytes retrieved from the QIC-02, until 512 bytes (256 words) have been transferred, then it starts over or is terminated if no more blocks are desired.

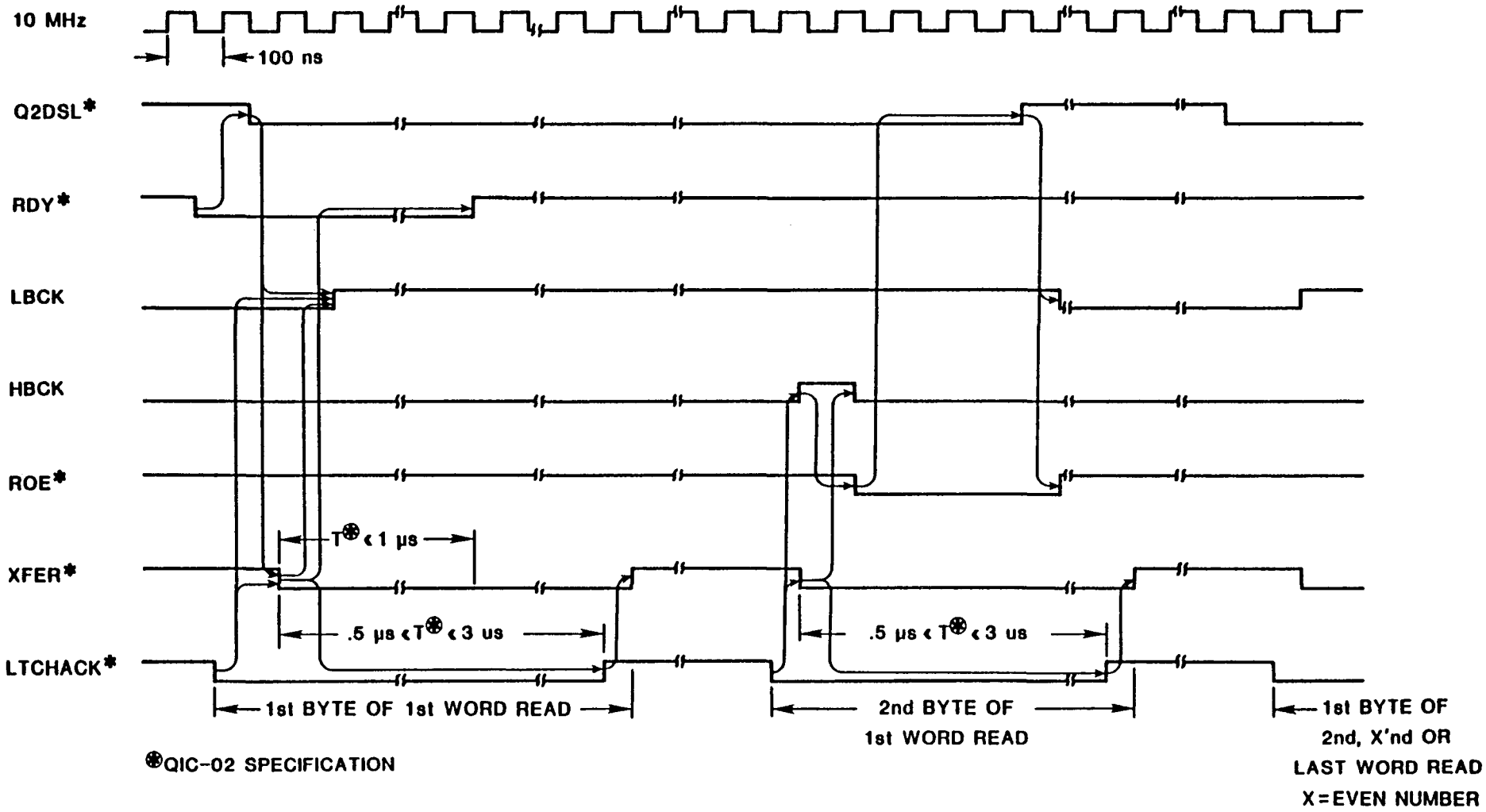


FIGURE 4-7. READ DATA TRANSFER

CHAPTER 5

SUPPORT INFORMATION

5.1 INTRODUCTION

This chapter provides the connector pin signal descriptions, parts list with associated parts location diagram, and schematic diagram for the VME350.

5.2 CONNECTOR PIN SIGNALS

Table 5-1 lists the connector pin signals on edge connector P1. Table 5-2 lists the connector pin signals on edge connector P2. Tables 5-3 and 5-4 list the connector pin signals for connectors J1 and J2.

TABLE 5-1. CONNECTOR P1 SIGNALS

Signal Mnemonic	Pin Number	Signal Name and Description
ACFAIL*	B:3	AC FAILURE - Open-collector driven signal which indicates that the AC input to the power supply is no longer being provided or that the required input voltage levels are not being met.
AM0-AM5	B:16-19, A:23, C:14	ADDRESS MODIFIER (Bits 0-5) - Three-state driven lines that provide additional information about the address bus, such as size, cycle type, and/or DTB master identification.
AS*	A:18	ADDRESS STROBE - Three-state driven signal that indicates a valid address is on the address bus.
A01-A07, A08-A23	A:30-24, C:30-15	ADDRESS BUS (Bits 1-23) - Three-state driven address lines that specify a memory address.
BBSY*	B:1	BUS BUSY - Open-collector driven signal generated by the current DTB master to indicate that it is using the bus.
BERR*	C:11	BUS ERROR - Open-collector driven signal generated by a slave. This signal indicates that an unrecoverable error has occurred and the bus cycle must be aborted.
BG0IN*-BG4IN*	B:4,6, B:8,10	BUS GRANT (0-3) IN - Totem-pole driven signals generated by the Arbiter or Requesters. Bus grant in and out signals form a daisy-chained bus grant. The bus grant out signal indicates to the next board that it may become the next bus master.
BG0OUT*-BG4OUT*	B:5,7, B:9,11	BUS GRANT (0-3) OUT - Totem-pole driven signals generated by Requesters. Bus grant in and out signals form a daisy-chained bus grant. The bus grant out signal indicates to the next board that it may become the next bus master.

TABLE 5-1. CONNECTOR P1 SIGNALS (cont'd)

Signal Mnemonic	Pin Number	Signal Name and Description
NC	A:10, B:2,21, B:22,31, C:13	NOT CONNECTED
SYSFAIL*	C:10	SYSTEM FAIL - Open-collector driven signal that indicates that a failure has occurred in the system. This signal may be generated by any module on the VMEbus.
SYSRESET*	C:12	SYSTEM RESET - Open-collector driven signal which, when low, will cause the system to be reset.
WRITE*	A:14	WRITE - Three-state driven signal that specifies the data transfer cycle in progress to be either read or write. A high level indicates a read operation and a low level indicates a write operation.
+5V	A:32, B:32, C:32	+5 Vdc POWER - Used by the VME350 circuits.
+12V	C:31	+12 Vdc POWER - Used by the Serial Port Diagnostic.
-12V	A:31	-12 Vdc POWER - Used by the Serial Port Diagnostic.

TABLE 5-2. CONNECTOR P2 SIGNALS

Signal Mnemonic	Pin Number	Signal Name and Description
ACK*	A:18	ACKNOWLEDGE - This input signal to the VME350 is used to transfer data between the VME350 and QIC-02 drive.
A24-A31	B:4-11	ADDRESS BUS (Bits 24-31) - Three-state driven bus expansion address lines.
DIRC*	A:21	DIRECTION - This input signal indicates which direction data is being driven on the bidirectional bus.
EXCP*	A:20	EXCEPTION - This input signal indicates that an error condition has been diagnosed by the tape drive.
GND	B:2,12, B:22,31, C:1-25	GROUND
NC	A:1-5, A:22-32, B:3,14-21,	NOT CONNECTED

TABLE 5-3. CONNECTOR J1 SIGNAL ASSIGNMENTS (cont'd)

Signal Mnemonic	Pin Number	Signal Name and Description
LA01-04	9-12	LOCAL ADDRESS (Bits 01-04) - The local address bits 1 1 through 4.
LD00-LD07	2-8,20	LOCAL DATA BUS (Bits 00-07) - The local data bits 1 through 7.
RST*	14	ON-BOARD RESET - The reset line.
R/W*	13	LOCAL READ/WRITE - The read/write line.
+5V	25,26	+5 Vdc POWER - Used by the SPB circuits.
+12V	24	+12 Vdc POWER - Used by the SPB circuits.
-12V	22	-12 Vdc POWER - Used by the SPB circuits.

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TABLE 5-4. CONNECTOR J2 SIGNAL ASSIGNMENTS

Signal Mnemonic	Pin Number	Signal Name and Description
ACK*	36	ACKNOWLEDGE - This input signal to the VME350 is used to transfer data between the VME350 and QIC-02 drive.
DIRC*	42	DIRECTION - This input signal indicates which direction data is being driven on the bidirectional bus.
EXCP*	40	EXCEPTION - This input signal indicates that an error condition has been diagnosed by the tape drive.
GND	1,3,5,7, 9,11,13, 15,17,19, 21,23,25, 27,29,31, 33,35,37, 39,41,43, 45,47,49	GROUND
NC	2,4,6,8, 10,44,46, 48,50	NOT CONNECTED
ONLINE*	28	ONLINE - Output signal to the tape drive.
QD0*-QD7*	26,24,22, 20,18,16, 14,12	QIC-02 DATA (Bits 0-7) - Bidirectional data bus between the VME350 and the QIC-02 tape drive.

TABLE 5-5. MVME350 PARTS LIST (cont'd)

Reference Designation	Motorola Part Number	Description
R1-R3,R13	06SW-124A37	Resistor, film, 1/4W, 5%, 330 ohm
R4,R8,R12	51NW9626A37	Resistor network, nine 10K ohm
R5,R7	51NW9626A22	Resistor network, five 10K ohm
R6	51NW9626A46	Resistor network, five 4.7K ohm
R9	51NW9626A67	Resistor network, nine 4.7K ohm
R10,R11	51NW9626A67	Resistor network, eight 220/330 ohm
S1	40NW9801A34	Switch, DIP, 8-position
U1,U6,U52, U59,U75	51NW9615J39	IC, 74F74PC
U2,U3,U7,U8	51NW9615R14	IC, 74F219PC
U4,U9	51NW9615E96	IC, SN74LS245
U5,U10	51NW9615R26	IC, SN74ALS645-1N
U11,U85	51NW9615C20	IC, SN74LS02N
U12,U51,U71	51NW9615C22	IC, SN74LS08N
U13,U32	51NW9615J13	IC, AM25LS2519PC
U14,U45	51NW9615F85	IC, SN74S38N
U15	51NW9615F05	IC, SN74LS20N
U16,U21,U62	51NW9615K71	IC, 74F04PC
U17,U88	51NW9615C24	IC, SN74LS32N
U18,U19,U63, U64,U68,U69	51NW9615E99	IC, SN74LS374N
U20,U23,U28, U34,U37,U49	51NW9615G07	IC, 74S244PC
U22	51NW9615G34	IC, SN74LS85N
U24,U65,U70	51NW9615F79	IC, SN74S240N
U25	51AW4591B48	IC, PROG PROM
U26	51NW9615C21	IC, SN74LS04N

TABLE 5-5. MVME350 PARTS LIST (cont'd)

Reference Designation	Motorola Part Number	Description
U78	51NW9615K72	IC, 74F02PC
U81	51NW9615K67	IC, 74F20PC
U82	51NW9615E67	IC, SN74S260N
U83	51NW9615C95	IC, SN74S74N
U86	51NW9615K69	IC, 74F10PC
Y1	48AW1068B03	Crystal, 20.0 MHz
	67NW9415A17	Kit, ejector handle (1 req'd)
	33-W4812B50	Nameplate (1 req'd)
	33-W4812B40	Nameplate, MVME (1 req'd)
	02SW990D007	Nut, hex M2 x 0.4 x 1.6 (4 req'd) [Use at P1 and P2]
	64-W4797B01	Panel, front (1 req'd)
	29NW9805C07	Pin, auto-insert [Use at J3(1-12), J4(1,2,3, 4,5,6), J5(1,2), J6(1,2,3,4,5,6), J7(1,2), J8(1-8)]
	29NW9805B17	Pin, shorting jumper [Use at J3(1-2,5-6,7-8, 9-11,10-12), J4(5-6), J5(1-2), J6(2-3,5-6), J7(1-2), J8(2-3,5-6,7-8)]
	42NW9401B14	Screw, captive collar (2 req'd)
	03NW9004B48	Screw, captive vero M2.5 (2 req'd)
	03SW993D110	Screw, phillips, M2 x 0.4 x 10 (4 req'd) [Use at P1 and P2]
	09NW9811A46	Socket, IC, 4-pin (Use at Y1)
	09NW9811A27	Socket, IC, 20-pin (Use at U25,U35,U54,U55, U58)
	09NW9811A21	Socket, IC, 28-pin (Use at U33,U40,U44,U47)
	09NW9811A26	Socket, IC, 48-pin (Use at U27)
	09NW9811A71	Socket, IC, 68-pin (Use at U39)

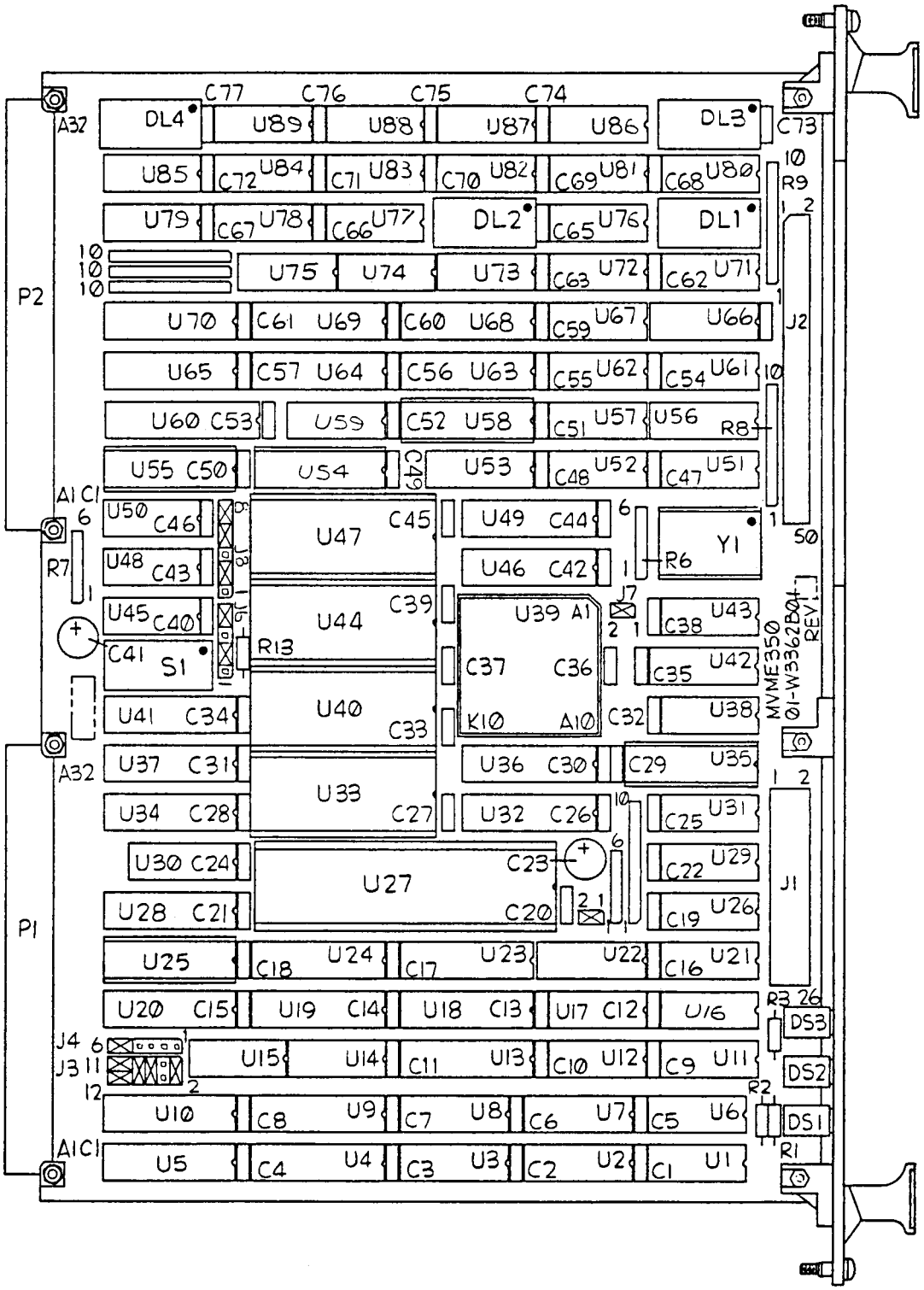

FIGURE 5-1. VME350 PART LOCATION DIAGRAM

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