CRAY SSD-T90: Clock and Boundary Scan

Record of Revision

February 1997

Original printing.

Introduction

This document describes the components of the clock module. Specifically, you will learn:

- How many clocks the CRAY SSD-T90 device uses
- The speeds of the clocks
- How the clock signals are fanned out

This document also describes the boundary scan feature and how it is implemented in the CRAY SSD-T90 device. Specifically, you will learn:

- The function of each boundary-scan component
- The path of the test data through the cabinet
- The functions of the boundary scan test
- How to initiate the boundary scan test
- How to interpret the error information

Terms

You will need to know how the following terms are used in this document to fully understand the material discussed in

this document:

Processing element (PE) - A PE contains a microprocessor, local memory, and support circuitry.

Control option (C option) - The C option is part of the support circuitry; it is the interface between the microprocessor, the interconnect network, and memory.

Network router option (R option) - The R option is the interface between the PE and the interconnect network.

I option - The I option performs I/O transfers between the nodes in the CRAY SSD-T90 device and the GigaRing option.

GigaRing option - The GigaRing option is the interface between the I option and the GigaRing channel.

Memory option (M option) - The support circuitry contains 4 M options; each M option controls the reads and writes for two banks of memory.

Clock

The CRAY SSD-T90 device uses three clocks: the system functional clock (NCLK), the boundary scan clock (TCLK), and the GigaRing clock (XCLK). The NCLK provides a 13.3-nanosecond (ns) clock to the options with the exception of the GigaRing options. The TCLK provides a variable clock (determined by a parameter of the boundary scan test) to the boundary scan logic that is located within the options. The XCLK provides a 8.0-ns clock to the GigaRing options.

The clock module consists of one printed circuit board (PCB) that contains master clock circuitry (refer to the circuitry above the dotted line in Figure 2) and slave circuity. The master clock circuitry consists of four oscillators (slow, normal, fast, and GigaRing) and fanout circuitry. The slave clock circuitry consists of fanout circuitry.

The master clock circuitry also performs a 1-to-8 fanout of the clock signals (refer to Figure 1). Using 1 of the 8 copies, the master clock circuitry sends the clock signal to itself (cabinet 0). The slave clock circuitry of cabinet 0 receives the clock signal from the master clock circuitry and performs a fanout of the clock signal to all of the PCBs within cabinets 0 and 1 (refer to Figure 3).

Figure 1. Clock Distribution

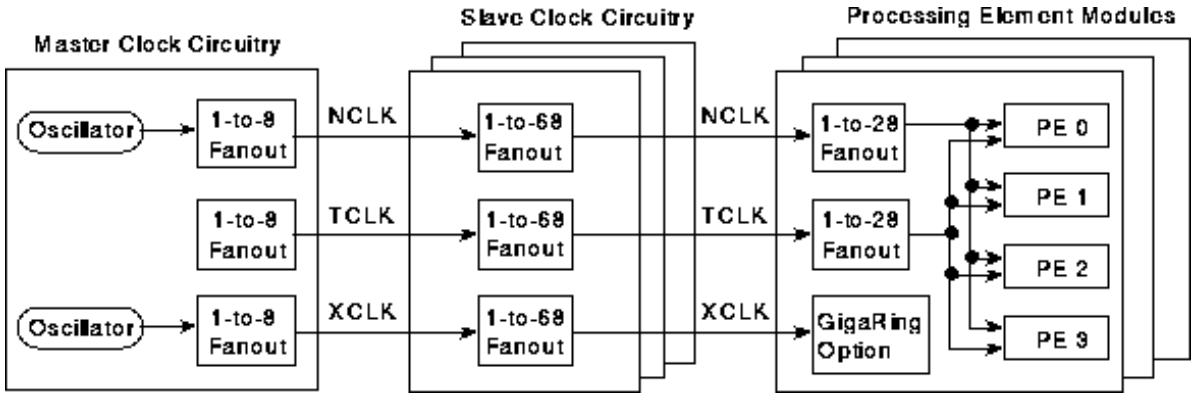
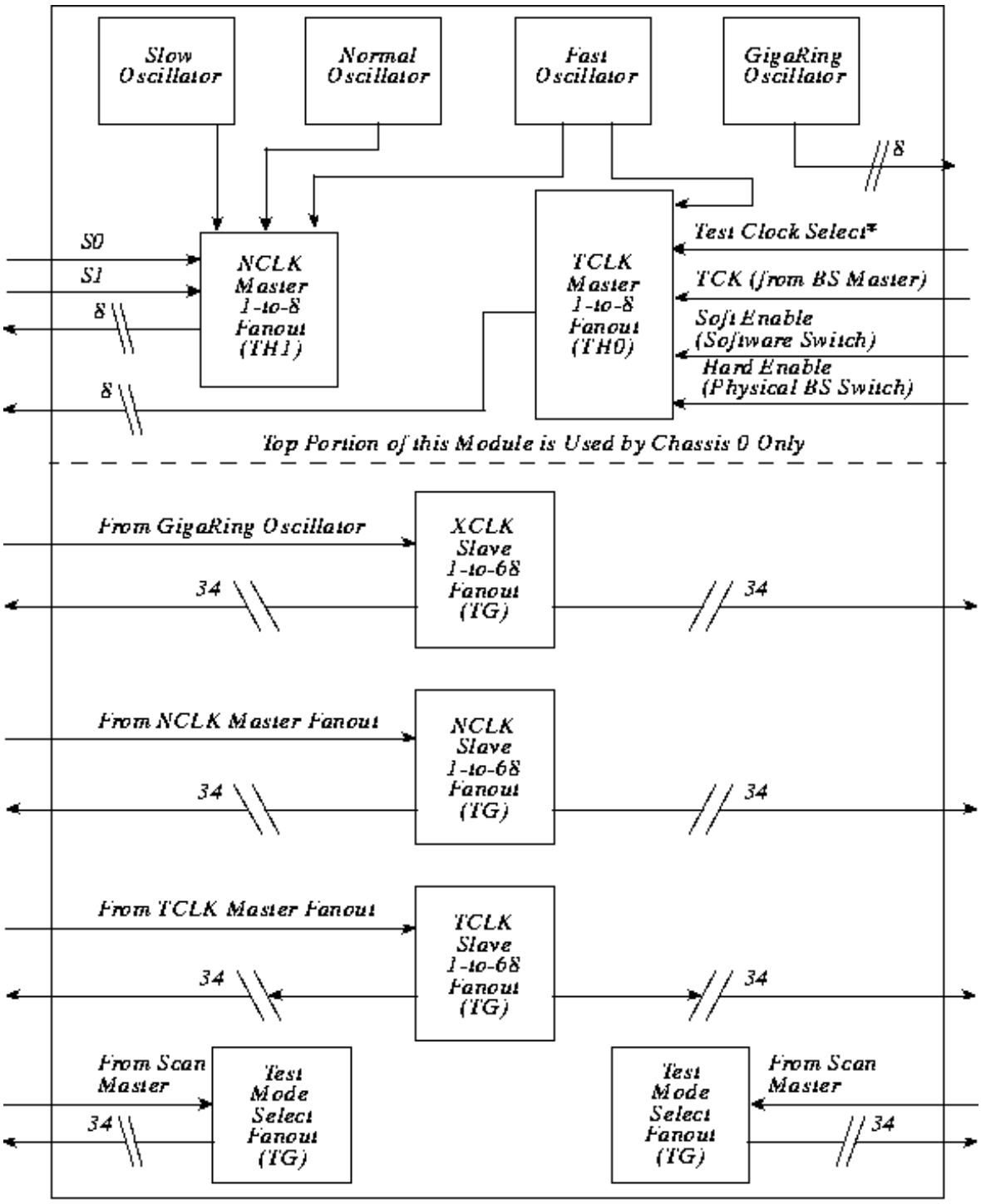
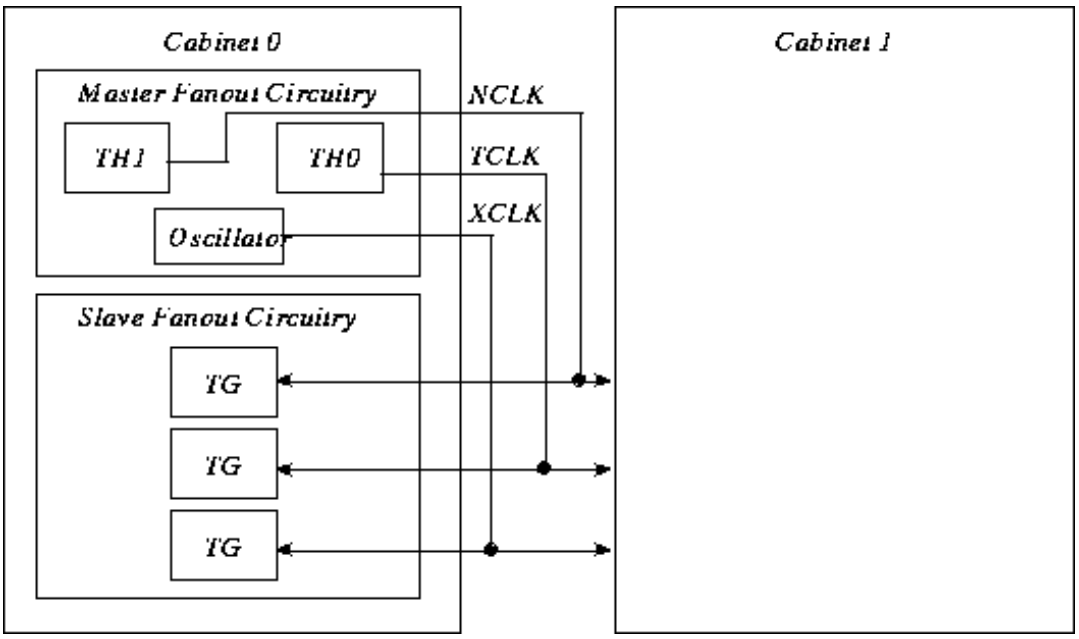


Figure 2. Clock Module



*The test clock select selects either the test clock from the boundary scan master or the fast oscillator.

Figure 3. Master and Slave Fanout Circuitry



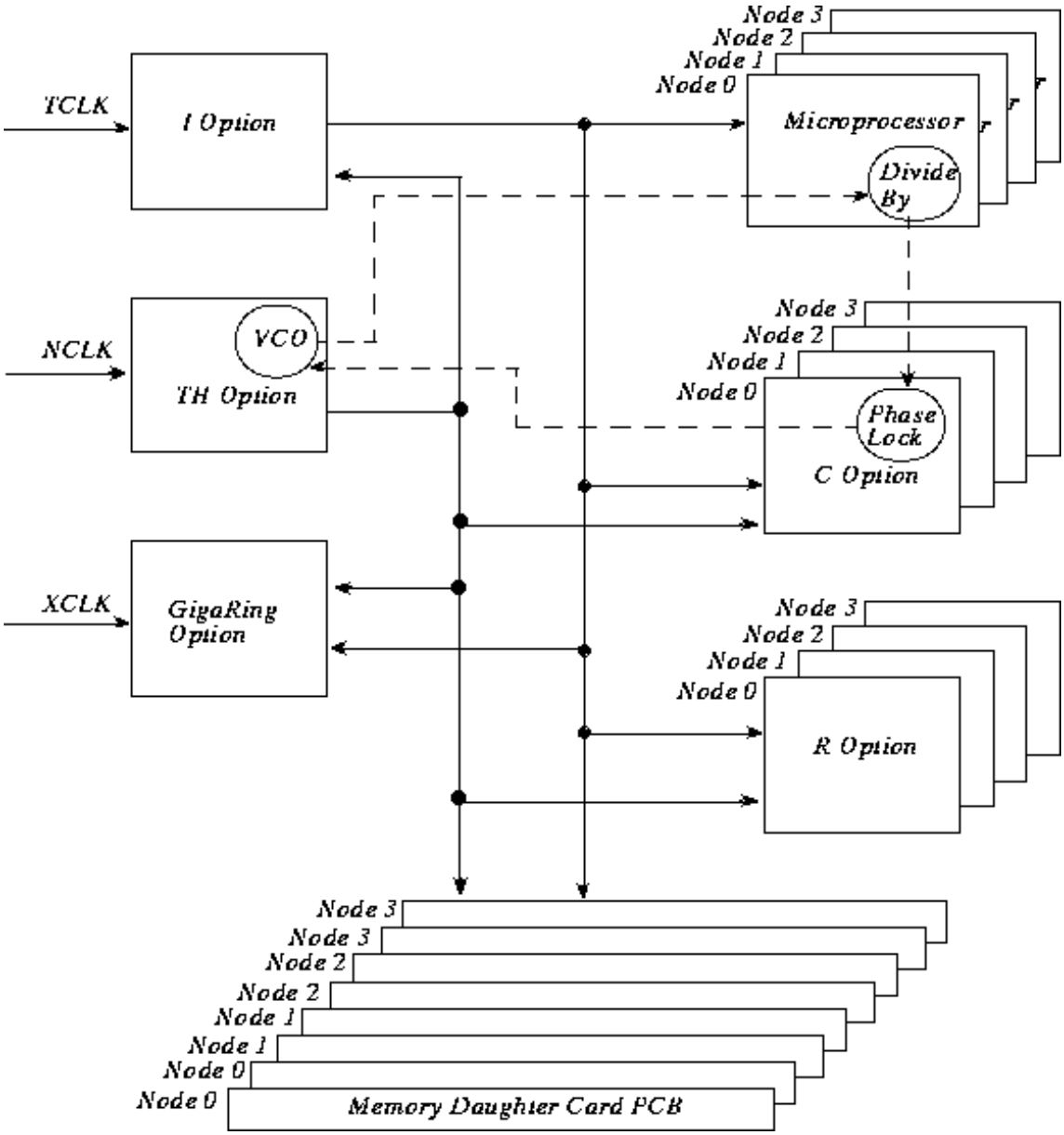
On the PCB, the I option fans out the TCLK (refer to Figure 4).

NOTE: The TCLK is only present when the CRAY SSD-T90 device is performing boundary scan operations.

The TH option fans out the NCLK to the C, R, I, and M options. The TH option also provides a clock signal (VCO) to the microprocessors. The microprocessors have a divide circuit (divide by1 or divide by 2) that produces a clock, which the microprocessor uses internally. Each microprocessor sends a copy of its internal clock signal to its local C option. The C options phase lock the clock signals and send the signals to the TH option.

The GigaRing option receives the XCLK signal.

Figure 4. Clock Distribution on a Printed Circuit Board



Boundary Scan

Boundary scan verifies the connections between cabinets, modules, and options in the CRAY SSD-T90 device. An external device (usually the system workstation) initiates the boundary scan test by sending a write scan request packet to the scan master I/O controller. There is only one scan master I/O controller per CRAY SSD-T90 device. The scan master is located in slot 1 of cabinet 0.

The write scan request packet contains a command and data. The command instructs the I/O controller to use the data from the packet as test vectors for the boundary scan test. The I/O controller sends the data from the packet to the boundary scan logic one bit at a time. The data bits are propagated through the boundary scan logic, where they test for continuity between the options and the modules. When the I/O controller sends the last bit to the boundary scan logic, the I/O controller sends a write-scan response packet to the external device.

The scan master I/O controller buffers the results of the boundary scan test. To view the results, the external device sends a read-scan request packet to the scan master I/O controller. After receiving the request, the scan master I/O

controller retrieves the test results from the buffer, places the results in a read-scan response packet, and sends the read-scan response packet to the external device.

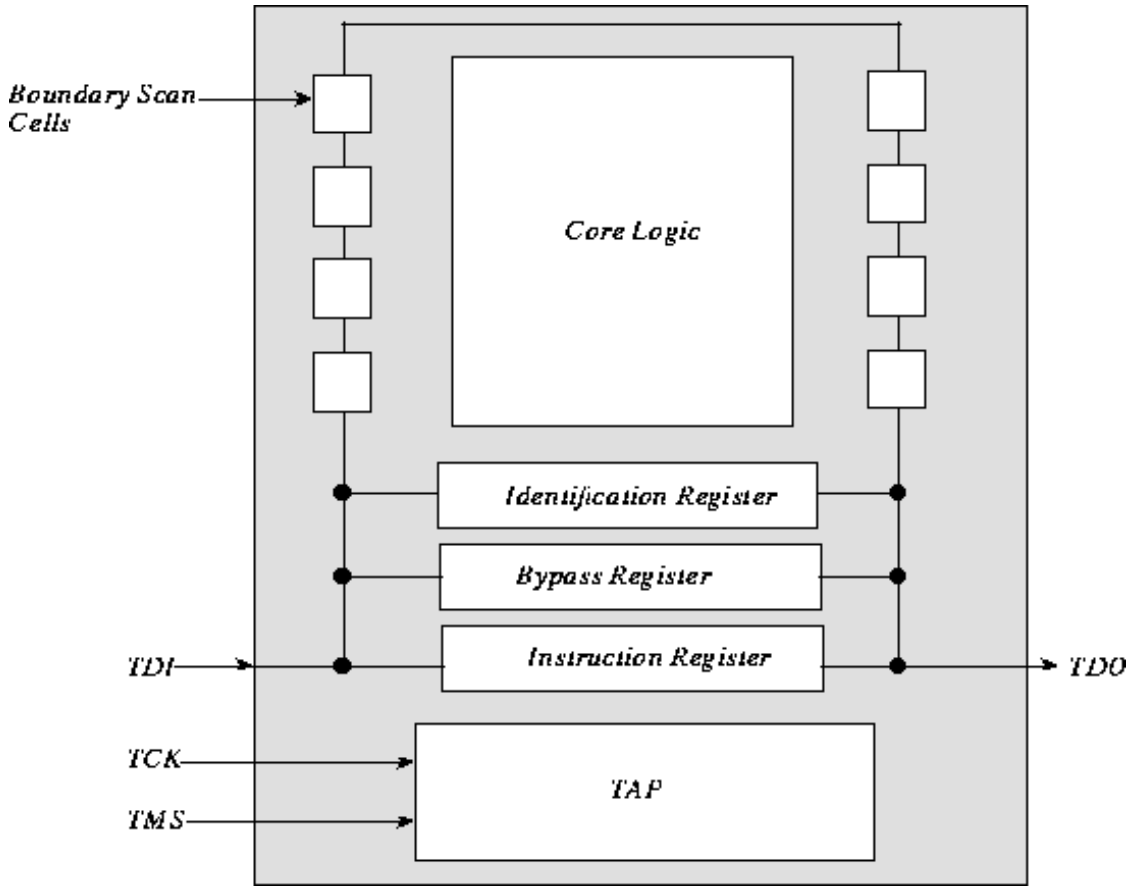
Run the boundary scan test to verify the integrity of the device after a failure occurs, or after you complete a repair procedure. You can initiate the boundary scan test by using command line syntax or `t3ems`. Boundary scan requires control of the system.

Components

Each option in the CRAY SSD-T90 device contains boundary scan logic. This logic consists of the test access port (TAP), an instruction register, a bypass register, an identification register, and boundary scan cells (refer to Figure 5).

The boundary scan logic requires four signal pins: test data input (TDI), test data output (TDO), test clock (TCK), and test mode select (TMS). The TDI pin inputs data serially. The TDO pin outputs data serially. The TCK pin inputs a clock signal that clocks the TAP and the internal scan chains during a scan operation. The TMS pin controls the state of the TAP controller.

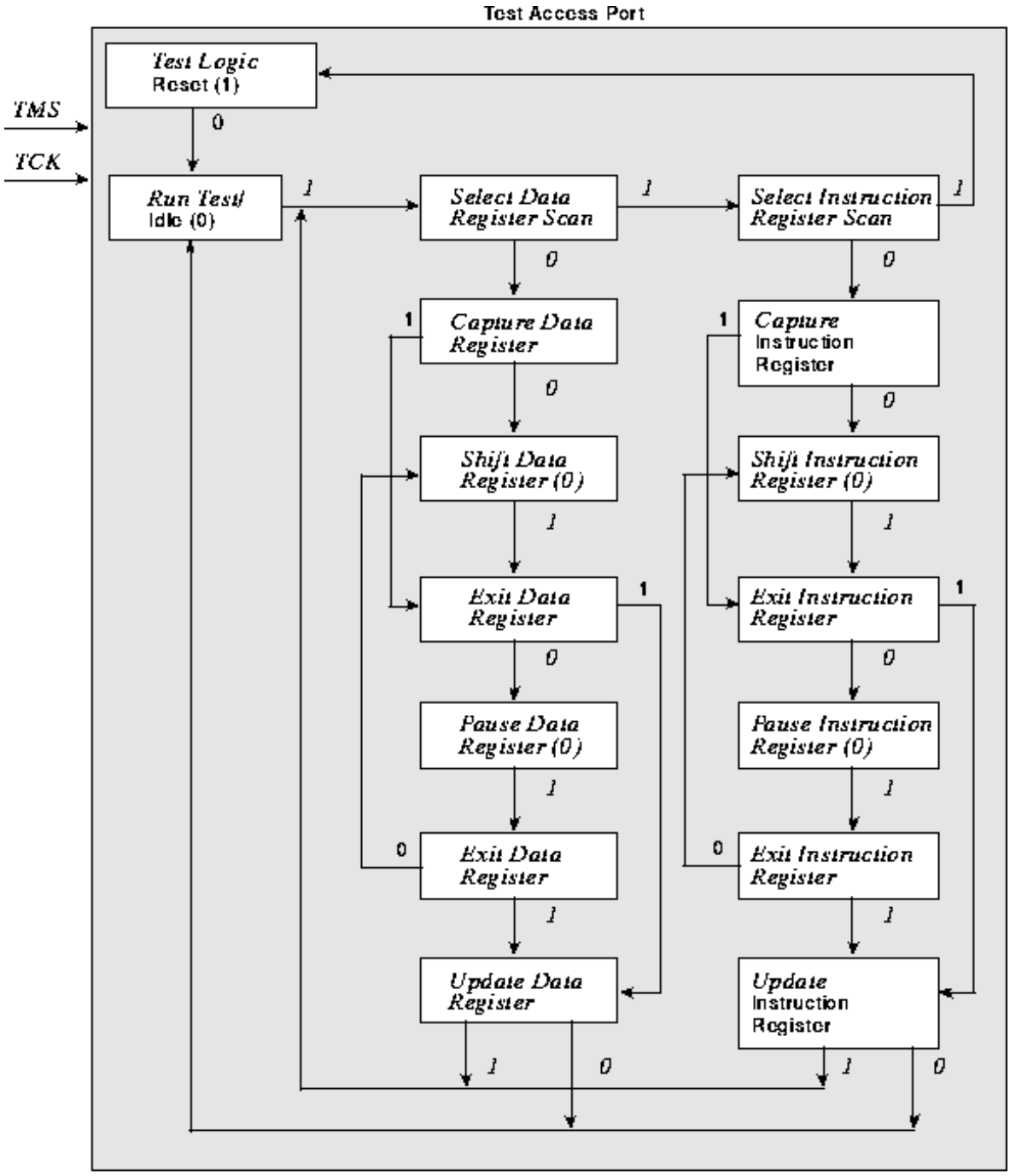
Figure 5. Boundary Scan Logic



Test Access Port (TAP)

The TAP controls the instruction register, the bypass register, the identification register, and the boundary scan cells. The TAP can be in 1 of 16 states (refer to Figure 6): idle, reset, data scan (requires 7 states), and instruction scan (requires 7 states). The boundary scan test changes the state of the TAP using the TMS and the TCK signals; the TAP changes state during the falling edge of the TCK signal.

Figure 6. States of the TAP

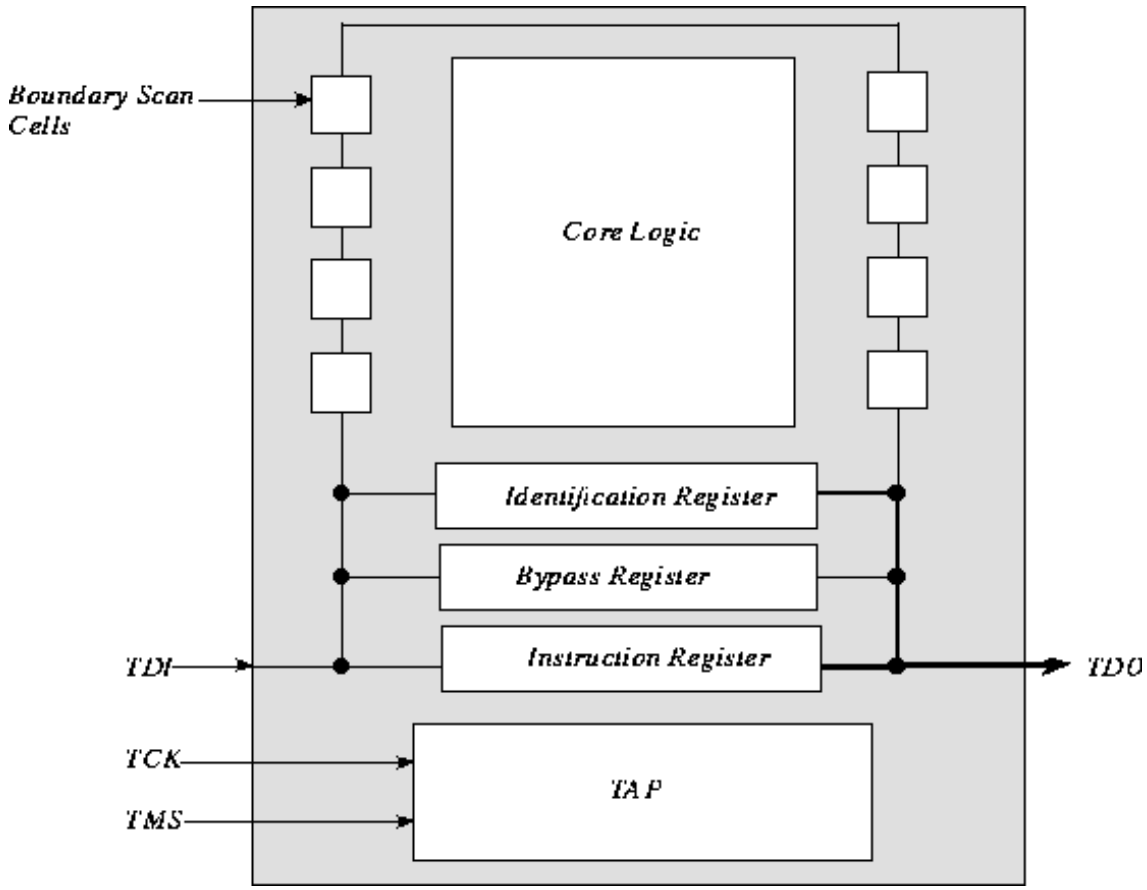


NOTE: The value(s) shown adjacent to each box represents the TMS signal level at the time of a falling edge of the TCK signal.

Instruction Register

The instruction register receives, holds, and decodes boundary scan instructions. The instructions indicate how the registers are connected to the TDI and TDO pins. For example, when the boundary scan test instructs the boundary scan logic to read the identification register, the TDO pin receives data from the identification register rather than from the boundary scan cells or the bypass register (refer to Figure 7).

Figure 7. Reading the Identification Register

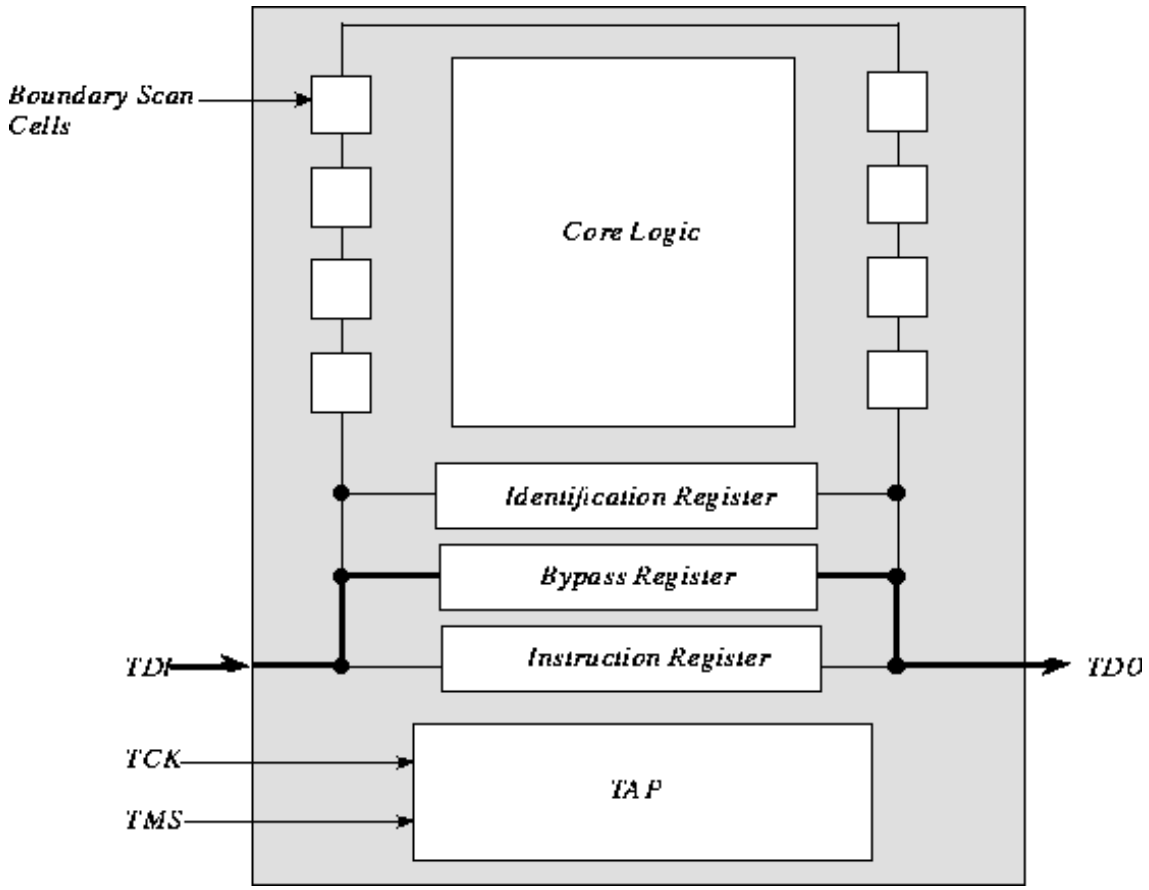


The options of the CRAY SSD-T90 device have a 5-bit instruction register; the GigaRing option has a 10-bit instruction register. When initiated, the boundary scan test first tests the scan chain by reading the pattern from the instruction register. For CRAY SSD-T90 options, this pattern is 10000. For the GigaRing option, the pattern is 1000000100.

Bypass Register

The bypass register routes signals from the TDI pin to the TDO pin; the signals do not flow through the boundary scan cells (refer to Figure 8).

Figure 8. Boundary Scan Path Using the Bypass Register

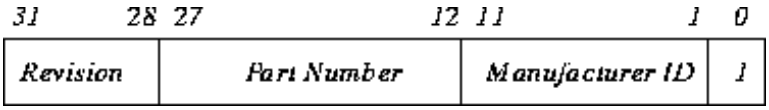


Identification Register

The identification register holds 32 bits of information that specifies the manufacturer of the option, the part number of the option, and the revision of the option (refer to Figure 9). The least significant bit must be a 1.

The identification register can also be used to shift in and shift out user-defined information.

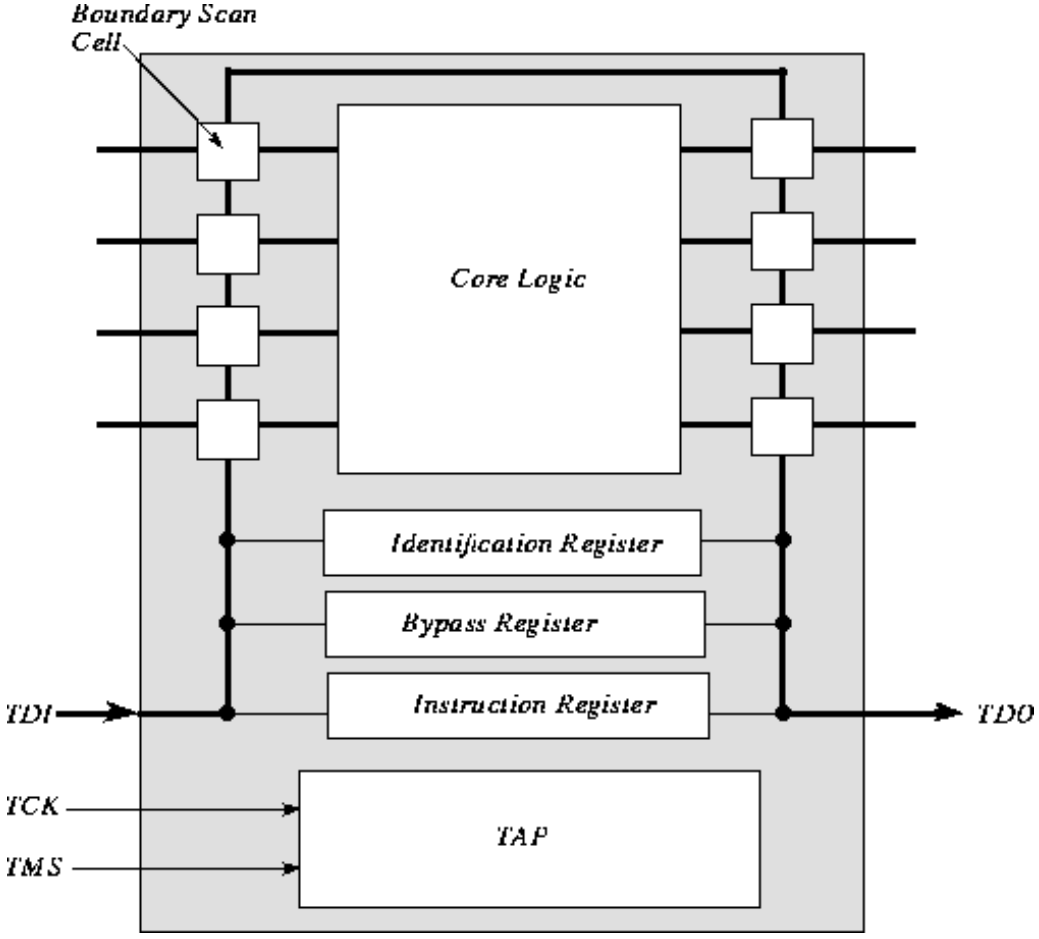
Figure 9. Identification Register



Boundary Scan Cells

The boundary scan cells capture data from the TDI pin, the option pins, and the core logic (refer to Figure 10). Likewise, the boundary scan cells transfer data to the TDO pin, the option pins, and the core logic. There is one boundary scan cell per input/output option pin.

Figure 10. Boundary Scan Cell Path

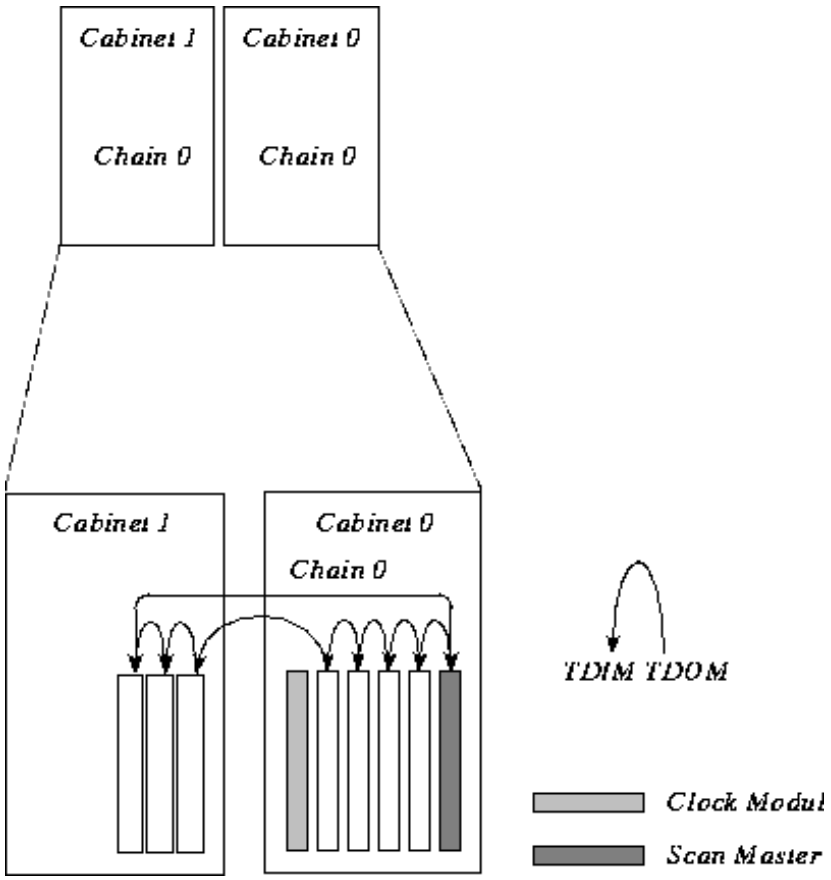


Scan Chain

A scan chain is the path that the test data takes through a cabinet. The CRAY SSD-T90 device contains one scan chain, which is referred to as
chain 0 (refer to Figure 11).

The boundary scan chain starts at the scan master, which is the PE module that resides in slot 1 of cabinet 0 The scan master starts the scan chain by using its TDIF pins to fan out the boundary scan signals; the TDIF0 pin fans out the signal to the module in slot 1 of cabinet 0. The boundary scan signal passes through the modules and leaves via their TDOM pins.The TDOM signal of a CRAY SSD-T90 module connects to the TDIM signal of the module that is next to it in the cabinet, with the exception of slot 5 of cabinet 0. For example, in a CRAY SSD-T90 device that contains two cabinets, slot 5 of cabinet 0 connects to slot 1 of cabinet 1 (refer again to Figure 11).

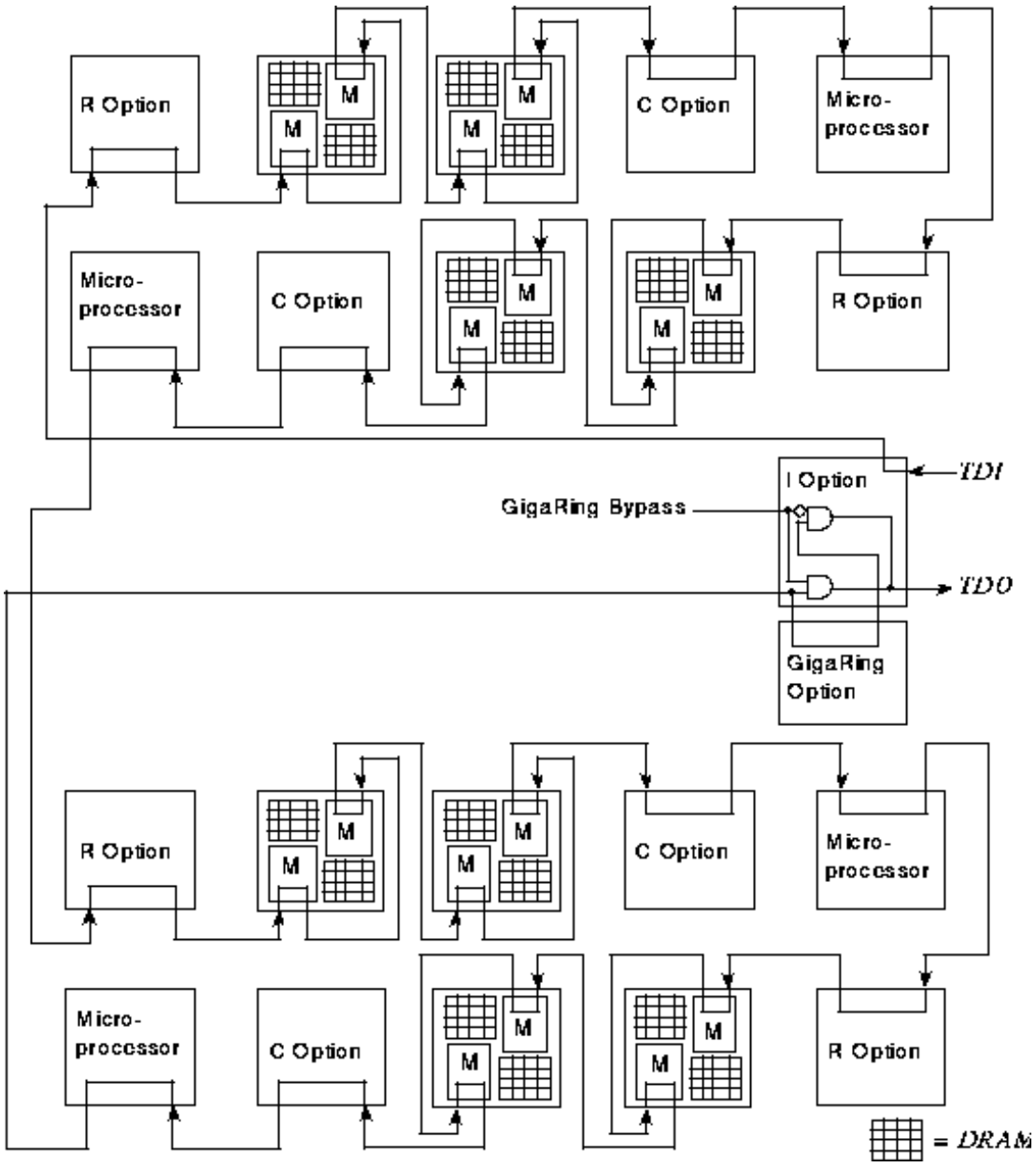
Figure 11. Scan Chain for a CRAY SSD-T90 Device



Within each PCB, the scan chain connects the boundary scan logic of the four PEs that reside on the PCB (refer to Figure 12).

NOTE: Normally, the boundary scan logic of the GigaRing option is not included in the scan chain. To bypass the GigaRing option, a GigaRing bypass jumper is inserted on the PCB.

Figure 12. Scan Chain Within a PCB



Boundary Scan Test Sequence

The CRAY SSD-T90 boundary scan test can perform the following functions:

1. Reads the configuration file to determine the number of cabinets in the system, the number of modules per cabinet, and wiring data (X, Y, and Z connections).

2. Verifies that the TAP circuitry on each board is operational. To do this, the boundary scan test reads the instruction registers and verifies that this information is correct.

3. Reads the printed circuit board revisions from the jumper on each PCB.

4. Generates test vectors and reference files. This setup is only necessary when you change the configuration (add a module, remove a module, add a module with a different revision, etc.) or when a reference file is missing or corrupted.

5. Verifies that the boundary scan registers are operational by scanning in and scanning out test patterns without updating the output pins.

   NOTE: At this point, the boundary scan cells are loaded with a test pattern.

6. Verifies that the interconnects (cables, wires, connectors, and foils) between the cabinets, modules, and options are operational.

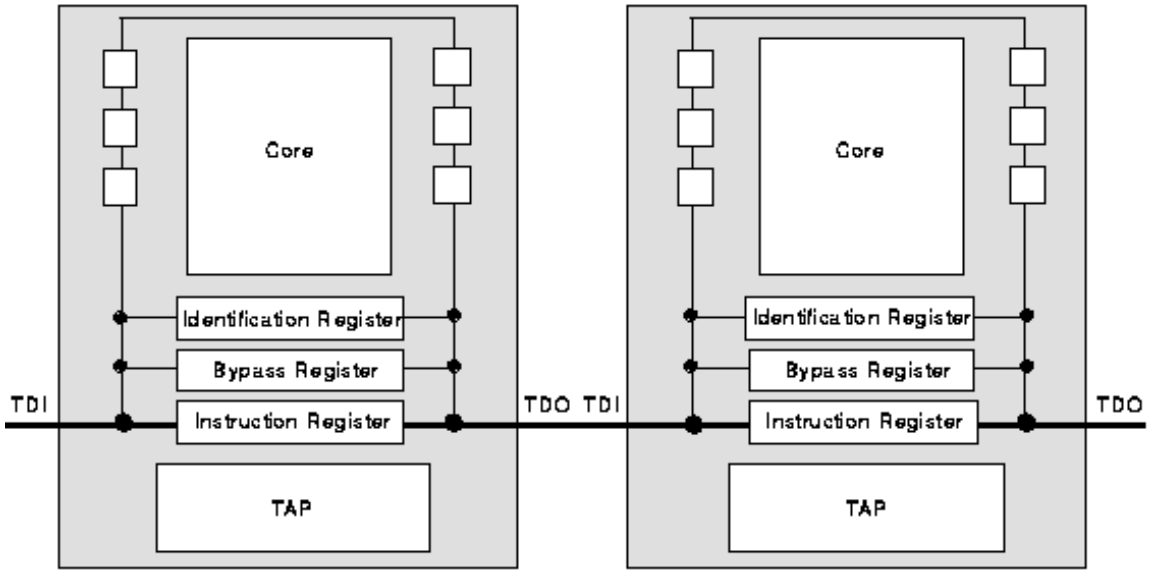
7. Verifies the results of the scan. When there is an error, the test displays the error information (failing net).

   NOTE: You select the functions that the boundary scan test performs when you initiate the boundary scan test (refer to the description of the -t command line option or the test select in the `Boundary Scan Options` window).

To verify that the interconnects between the cabinets, modules, and options are operational (Step 6), the boundary scan test uses the `extest` instruction that allows the boundary scan logic to scan in and scan out test patterns (refer to Figure 13 and Figure 14). The test patterns may include a 1's pattern, a 0's pattern, a bridging pattern, and a complemented bridging pattern.

Figure 13. extest Instruction

1. Load the extest instruction into the instruction register. This action places the boundary scan logic into test mode.
The extest instruction consists of three stages: capture, shift, and update.



2. The capture stage of the extest instruction causes all of the options within a scan chain to capture (latch) data from the input pins.

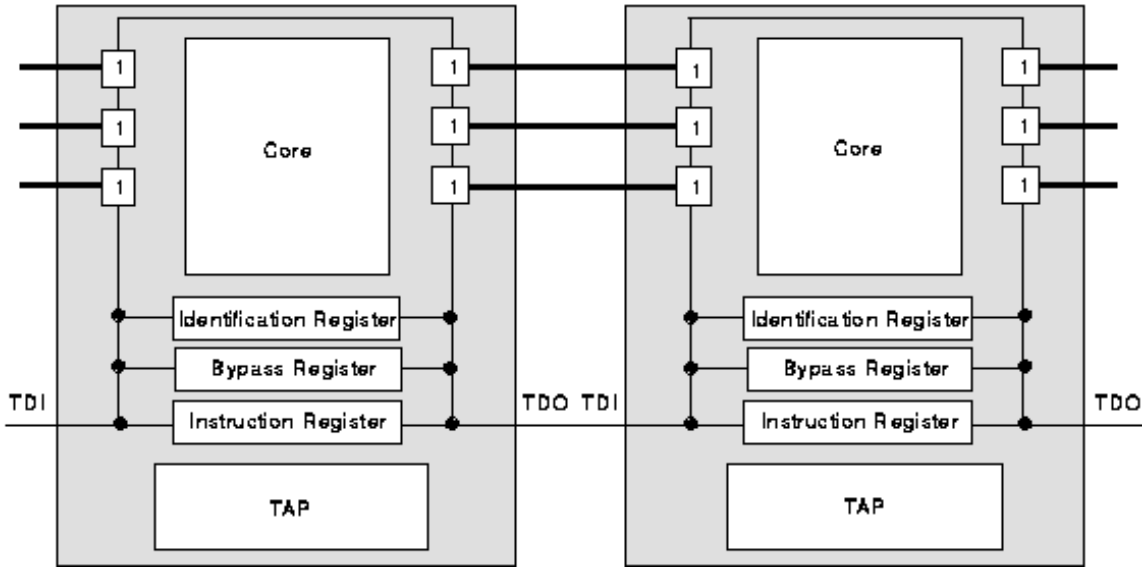
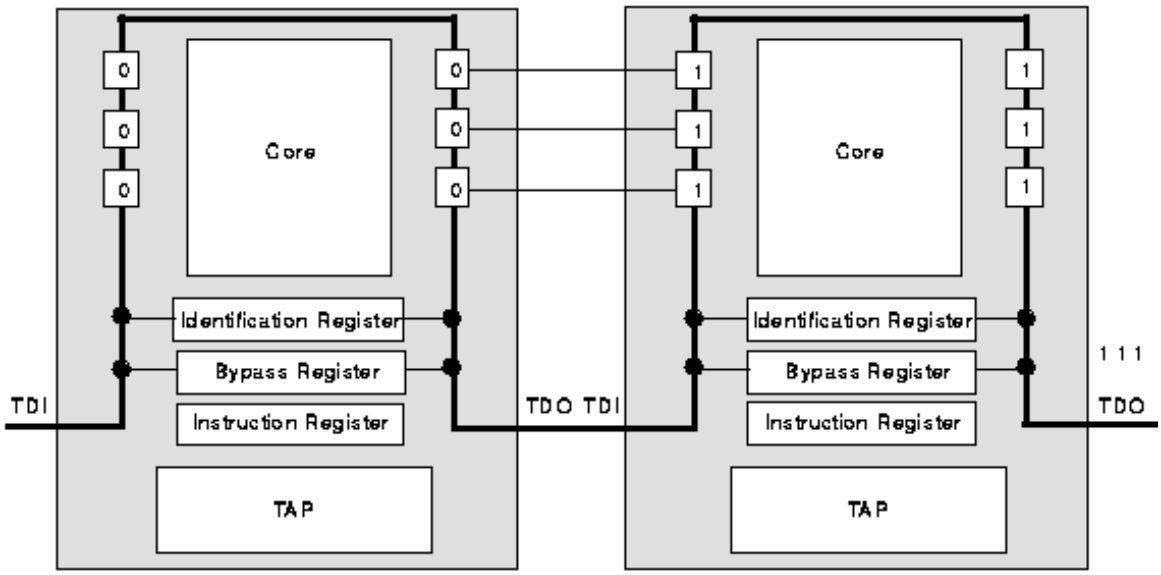


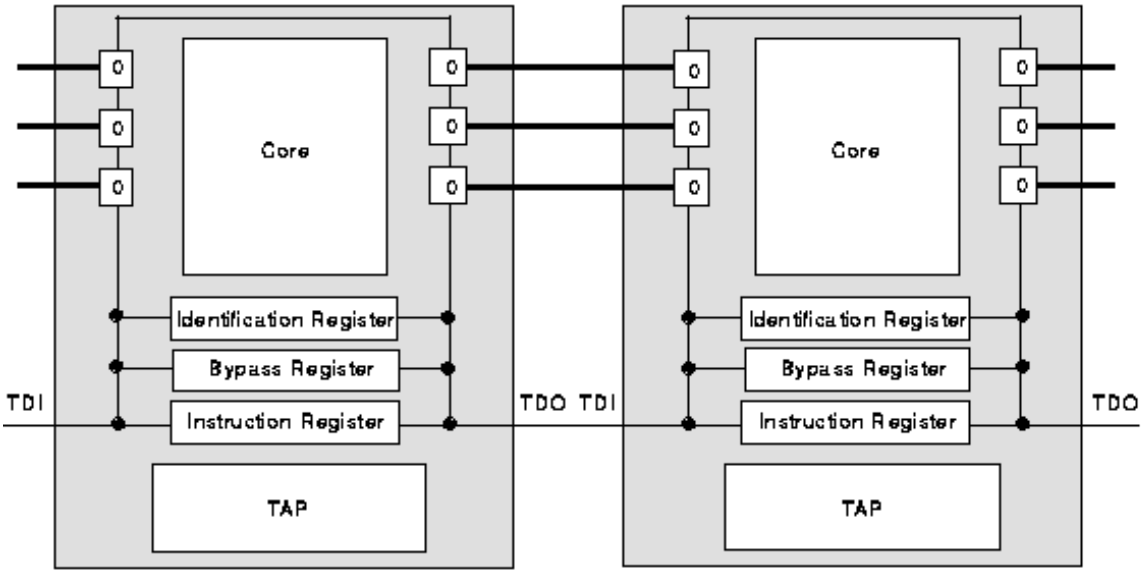
Figure 14. extest Instruction (continued)

3. The shift stage of the extest instruction causes the boundary scan logic to shift out the old test pattern through the entire scan chain and shift in a new test pattern.

   The scan master sends the old test pattern to the SWS. Software running on the SWS compares the test pattern to an expected test pattern to determine whether there are any errors.



4. Like the capture stage, the update stage of the extest instruction causes the options to latch in the new test pattern.



5. Repeat Steps 3 and 4 for all of the test patterns.

How to Initiate the Boundary Scan Test

You may run the boundary scan test to verify the integrity of the system after a failure that causes the operating system to fail, or after you complete a repair procedure.

Before you initiate the boundary scan test, perform the following steps:

1. Enable the boundary scan hardware switch.

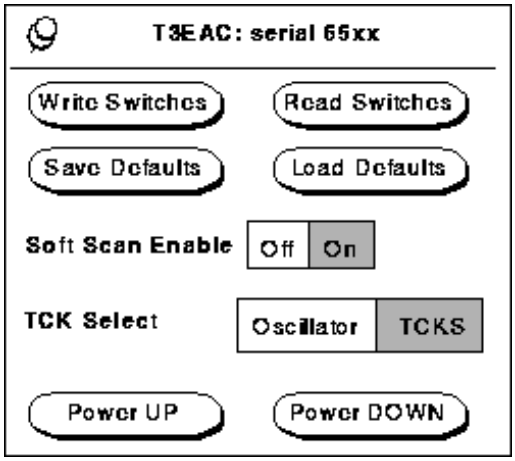
   For a CRAY SSD-T90 device, the boundary scan hardware switch is located on the rear side of chassis 0,

above the clock module (slot 6).

2. Enable the boundary scan software switch and test clock.

   To enable the software switch and the test clock, bring up the nwacs display, select `On` for the soft scan enable, select `TCKS` for the TCK select, and click on the `Write Switches` button (refer to Figure 15).

   Figure 15. Boundary Scan Software Switch (Soft Scan Enable)



   NOTE: The CRAY SSD-T90 device uses some of the same software as the CRAY T3E system; therefore, the titles of the CRAY SSD-T90 pop-up windows and diagnostic windows may contain `T3E`.

You can initiate the boundary scan test using `t3ems` or command line syntax.

Initiating the Boundary Scan Test by Using t3ems

NOTE: The CRAY SSD-T90 device uses the same offline diagnostic maintenance system as the CRAY T3E system; therefore, the offline diagnostic maintenance system windows are labeled CRAY T3E.

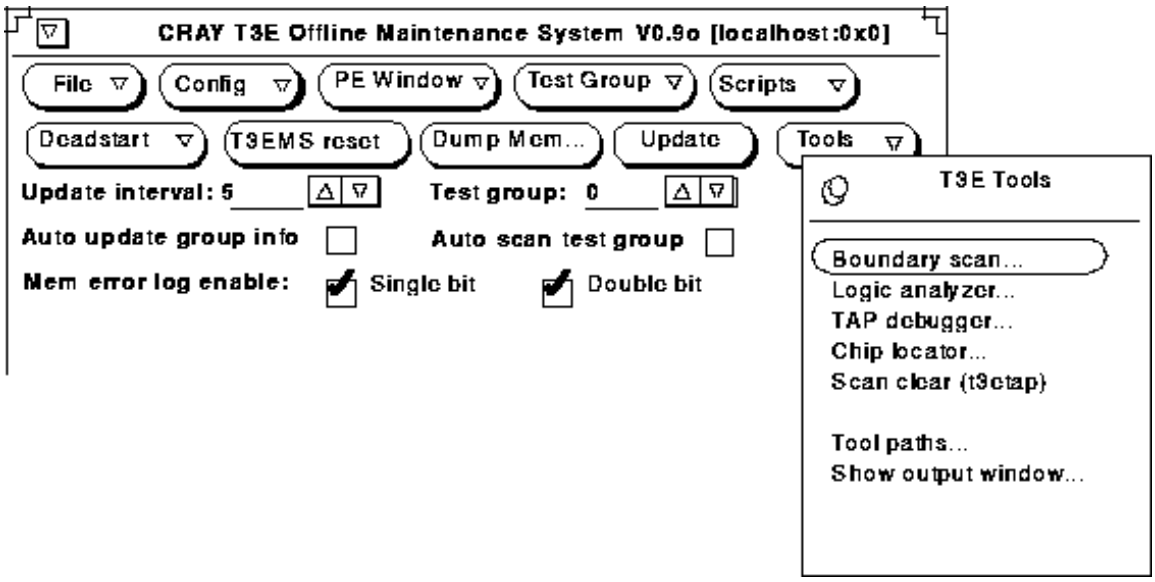
1. Bring up `t3ems`.

   At the prompt, type **`t3ems`**

   NOTE: `t3ems` is located in the /opt/CYRIdiag/t3e/bin directory.

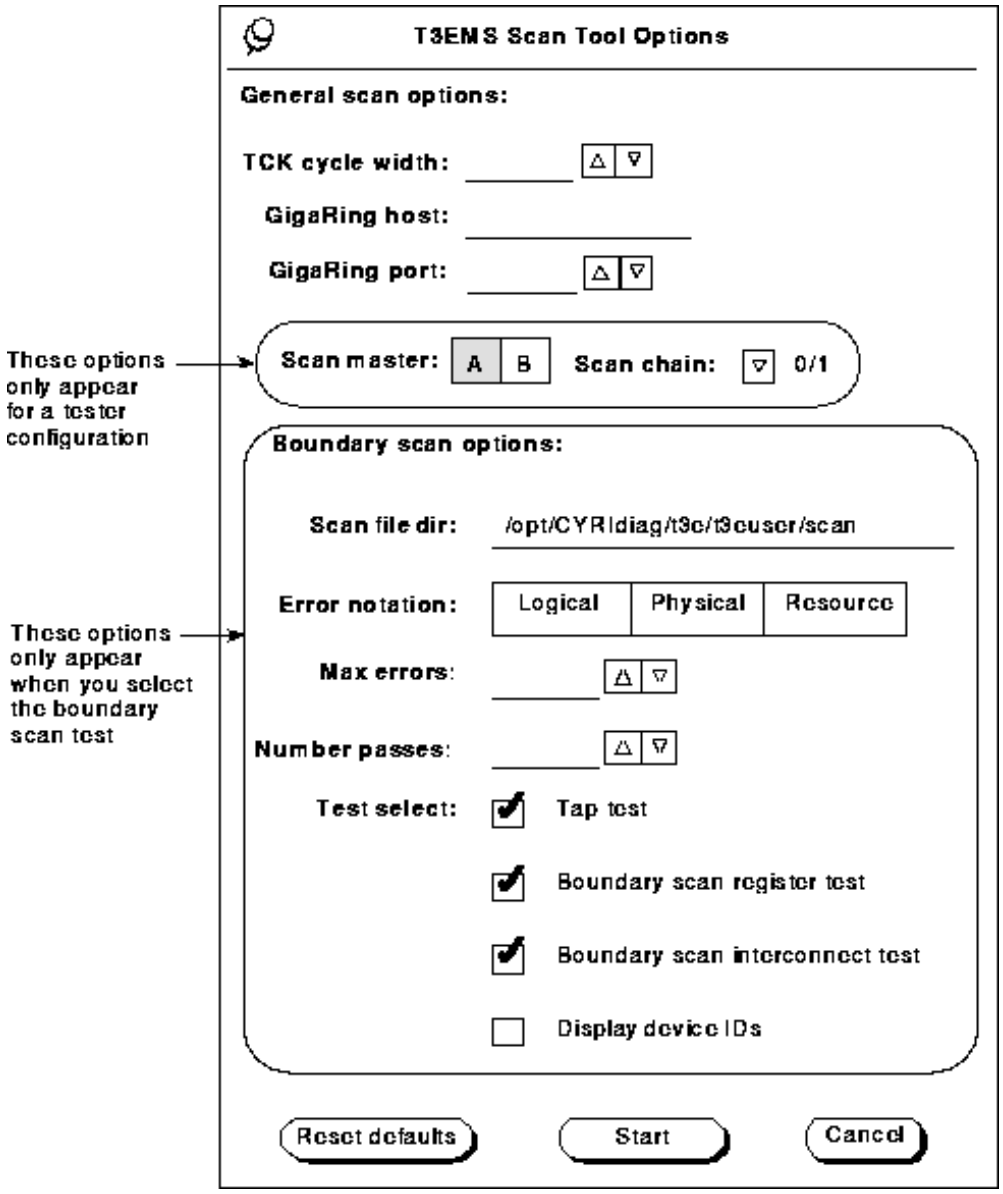
2. Select the boundary scan test from the `Tools` menu (refer to Figure 16).

   Figure 16. Tools Menu



The `T3EMS Scan Tool Options` window appears on the screen (refer to Figure 17).

Figure 17. T3EMS Scan Tool Options Window



3. Select an error notation option.

   This option specifies whether the boundary scan test should display the error information using logical or physical component designators (refer to Figure 22 and Figure 23), or display the failing resources (refer to Figure 24).

   The `T3EMS Scan Tools Options` window also lists the following user selectable options; however, the default selections of these options are based on the `t3ems` configuration information and do not need to be changed.

   `TCK cycle width`
   This option overrides the default TCK pulse width. This value can be any number between 3 and 60; the default value is 10.

   `GigaRing host`
   This option selects the host system.

   `GigaRing port`
   This option selects the I/O port.

   `Scan master`
   This option selects the scan master PCB and the scan chain for the A (top) PCB. This option is only available when you are running the boundary scan test on a module in a test vehicle.

   `Scan file dir`
   This option indicates the pathname of the scan files.

   `Max errors`
   This option specifies how many errors the boundary scan test displays to the user. This value can be any number between 1 and 100; the default value is 100.

   `Number passes`
   This option specifies how many passes the boundary scan test makes. This value can be any number between 1 and 100; the default value is 1.

   `Test select`
   This option specifies which tests the boundary scan test performs.

4. Click on 

to start the boundary scan test.

   Clicking on this button starts the selected boundary scan tests. `t3ems` directs the status and error information to the log window.

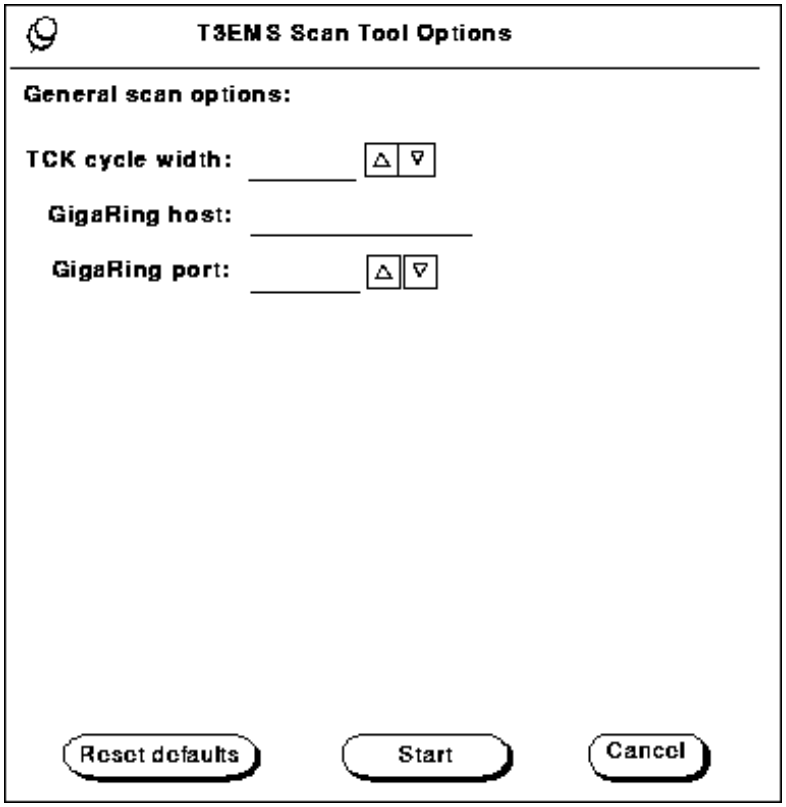
   NOTE: After the boundary scan test completes, you must run `Scan clear (t3etap)`. `Scan clear (t3etap)` resynchronizes the phase-locked loop between the microprocessor, the C option, and the TH option by adjusting the clock frequencies.

5. Select the `Scan clear (t3etap)` utility from the `Tools` menu (refer again to Figure 16).

The `T3EMS Scan Tool Options` window appears on the screen (refer to Figure 18).

6. Click on Start to start the `Scan clear (t3etap)` utility.

Figure 18. T3EMS Scan Tool Options Window for Scan Clear



`Scan clear (t3etap)` displays the following status information.

```
=== Begin scan clear ===

Hardware: A/C system with 8 PEs

Attempting connection to GRING node 0x0F via MPN
sn6503-mpn0:0470 done.

Performing TAP test:
    Chain 00...passed
        Detected from hardware: #chips=58 IR_len=290

Reading revisions from hardware and verifying configuration:
    Chain 00...done

Boundary-scan revisions from hardware (by scan chain):
    <GRC> = '+' if GigaRing chip in scan chain; ' ' if chip in bypass
    <BRD> = board on 'A' or 'B' side of coldplate
    <REV> = bits 2^3 - 2^0 of BSTREV (in hexidecimal)

          G B R
          R R E
    00    C D V
    ----  - - -
    002U    A 0
    001U    A 0

=== End scan clear =
```

Initiating the Boundary Scan Test by Using Command Line Syntax

1. Enter the `t3ebst` command with desired options.

   At the prompt, type:

   `t3ebst [-c <#>] [-d <path>] [-e <#>] [-g] [-h] [-p <#>] [-q] [-r <type>] [-s <def>] [-sim] [-t <test>] [-G <spec>]`

   `t3ebst` is located in the /opt/CYRIdiag/t3e/bin directory.

   The `t3ebst` command accepts the following options:

   `-c <#>`
   This option overrides the default TCK pulse width. This value can be any number between 3 and 60; the default value is 10.

   `-d <path>`
   This option specifies the test file directory for the system.

   `-e <#>`
   This option defines the maximum number of errors that the command will display to the user. This value can be any number between 1 and 10000; the default value is 100.

   `-g`
   This option generates boundary-scan test patterns and exits.

   `-h`
   This option displays the online option descriptions for this command.

`-p <#>`
This option specifies how many passes the boundary scan test makes. This value can be any number between 1 and 100; the default value is 1.

`-q`
This option specifies that `t3ebst` should run the short version of the boundary scan test.

`-r <type>`
This option defines the type of reference names that `t3ebst` uses to display errors. `t3ebst` can display errors using logical (log) reference names or physical (phy) reference names. The default type selection is logical reference names.

`-s <def>`
This option defines the scan master and the scan chains for a module that is being tested in a test vehicle.

`<def>` requires the following format:

```
<SM>+<top PCB chain#>
```

`<SM>` is the scan master board (A or B)

`<top PCB chain#>` is an even scan chain number (0, 2, ..., 14). The default format is `a+0`.

`-sim`
This option specifies that the boundary scan test should run in simulation mode. The program does communicate with real hardware.

`-t <test>`
This option specifies which tests the boundary scan test performs. The boundary scan test can perform any number of tests. When you select more than one test, use a plus sign (+) to separate the test names. For example, the following option selects the `tap`, `id`, and `bsr` tests:

```
-t tap+id+bsr
```

You can list the tests in any order; however, certain tests require that other tests are successful. Selection of one test may cause the automatic selection of other tests.

The following tests are valid tests:

`tap`
Tests all of the TAPs in the system.

`id`
Reads and displays the device ID registers. When you select the `id` test, the `t3ebst` command automatically selects the `tap` test.

`bsr`
Tests all of the boundary-scan registers. When you select the `bsr` test, the `t3ebst` command automatically selects the `tap` test.

`bst`

Performs the boundary scan interconnect test. When you select the `bst` test, the `t3ebst` command automatically selects the `tap` test and the `bsr` test.

The default test selection is `bst`, which is equivalent to `tap+bsr+bst`.

`-G <spec>`
This option defines the host system and the I/O port for the GigaRing communications. `<spec>` requires the following format:

`<host>:<port>`

Error Information

The following subsections contain examples of boundary scan failures.

NOTE: When the boundary scan test identifies a failure, run S`can clear (t3etap)` before removing power from the module.

Test Tap Failure

The boundary scan test displays the following error information when the boundary-scan hardware switch or the boundary-scan software switch is not enabled. This type of failure could also be caused by an open wire between the leftmost module in the scan chain and the scan master, failing scan master logic, or failing logic in the leftmost module in the scan chain.

```
=== Begin boundary scan test ===

T3E Boundary-Scan Test - t3ebst version 0.3

Hardware: A/C system with 8 PEs

Attempting connection to GRING node 0x0F via MPN sn6502-mpn0:0470 done.

Performing TAP test:

    Chain 00...failed
    All 1's coming out of instruction register chain.
    Verify power and communications to module(s) in system.

Unable to continue due to TAP test errors.

=== End boundary scan test ===
```

TAP Test Vector = IR_TEST TDO Failure

The boundary scan test displays the following error information when a boundary scan chain test fails.

```
=== Begin boundary scan test ===

T3E Boundary-Scan Test - t3ebst version 0.3

Hardware: A/C system with 8 PEs

Attempting connection to GRING node 0x0F via MPN sn6502-mpn0:0470 done.

Performing TAP test:
        Chain 00...
VECTOR=IR_TEST TDO

84210842  10842108  42108421  08421084  21087FFF FFFFFFFF FFFFFFFF FFFFFFFF
FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF
FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF
FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF
FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF
FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF
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FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF
FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF

=== End boundary scan test ===
```
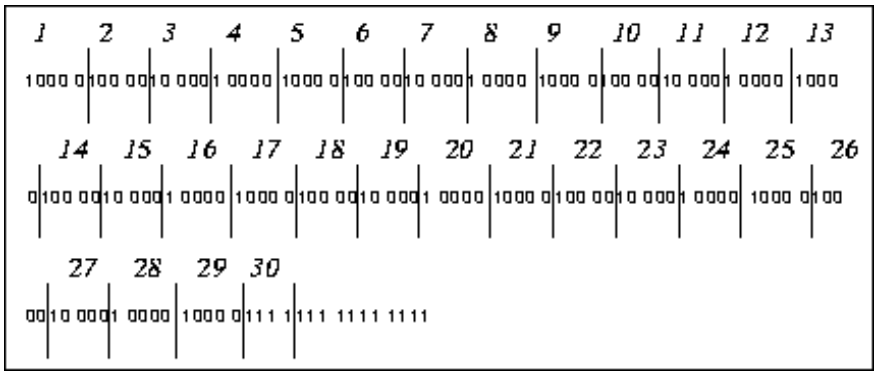

To interpret this failure information, you must convert the hex numbers to binary numbers. Figure 19 shows the 84210842 10842108 42108421 08421084 21087FFF pattern converted to binary numbers.

Figure 19. Hexadecimal to Binary Conversion

```
 8    4    2    1    0    8    4    2    1    0    8    4    2    1    0    8
1000 0100 0010 0001 0000 1000 0100 0010 0001 0000 1000 0100 0010 0001 0000 1000

 4    2    1    0    8    4    2    1    0    8    4    2    1    0    8    4
0100 0010 0001 0000 1000 0100 0010 0001 0000 1000 0100 0010 0001 0000 1000 0100

 2    1    0    8    7    F    F    F
0010 0001 0000 1000 0111 1111 1111 1111
```

The boundary scan IR_TEST TDO test reads a test pattern of 10000 (refer to Figure 20).

Figure 20. Test Pattern



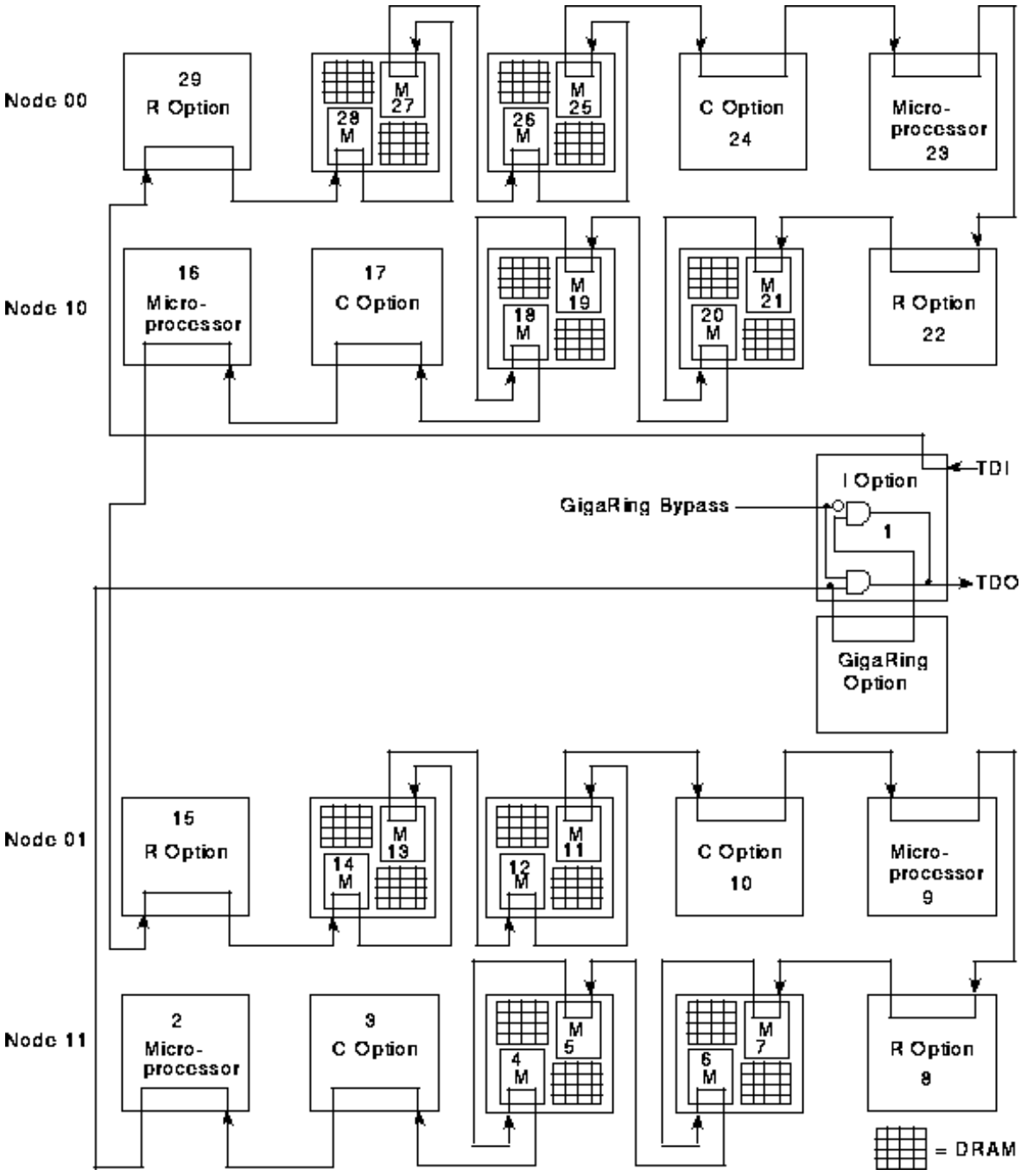
When the boundary scan test initiates the instruction register scan test, the boundary scan logic of each option automatically transmits the 10000 test pattern.

NOTE: The GigaRing option is not included in the chain (bypassed); therefore, each PCB contains 29 test locations (refer to Figure 21). When the Gigaring option is included in the chain, the test pattern is 1000000100.

The first pattern listed in Figure 20 is the output from the first test location (I option) of the leftmost module in the scan chain. For this example, the first pattern listed is the output from the module in slot 2 of Cabinet 0. The eighth pattern is the output from the R option in Node 11 (3). The thirtieth pattern is the output from the first test location of the module in slot 1 of Cabinet 0.

For this example, the failure occurred between module slots 1 and 2. Since the failure is between different modules, the cause of this failure could be a wire or connector.

Figure 21. Boundary Scan Test Locations within a PCB



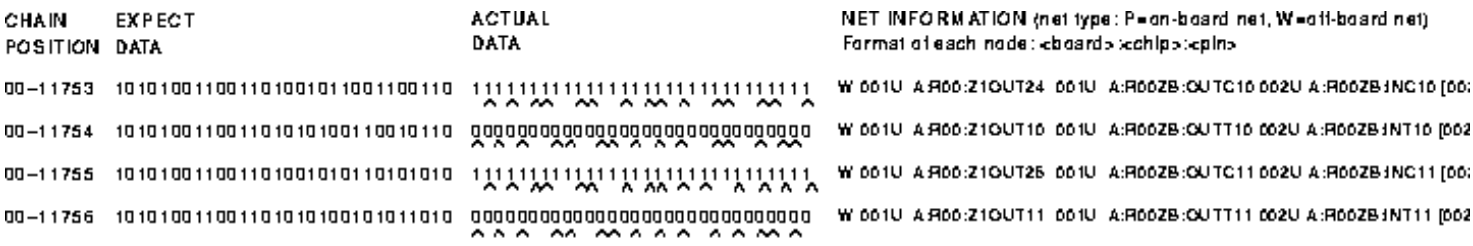
Interconnect Test Failure

The boundary scan test displays the following error information when it detects an interconnect failure.

```
=== Begin boundary scan test ===

T3E Boundary-Scan Test - t3ebst version 0.3

Hardware: A/C system with 8 PEs

Attempting connection to GRING node 0x0F via MPN sn6502-mpn0:0470 done.

Performing TAP test:
        Chain 00...passed
                Detected from hardware: #chips=58 IR_len=290

Reading revisions from hardware and verifying configuration:
        Chain 00...done

        Boundary-scan revisions from hardware (by scan chain):
        <GRC> = '+' if GigaRing chip in scan chain; ' ' if chip in bypass
        <BRD> = board on 'A' or 'B' side of coldplate
        <REV> = bits 2^3 - 2^0 of BSTREV (in hexidecimal)

             G B R
             R R E
        00   C D V
        ---- - - -
        002U   A 0
        001U   A 0

 Testing boundary-scan registers:
        Chain 00...passed

        Performing boundary scan interconnect test (pass 1 of 1):

                (30 patterns will be applied)

                Pattern 00...done
                Pattern 01...done
                Pattern 02...done
                Pattern 03...done
                Pattern 04...done
                Pattern 05...done
                Pattern 06...done
                Pattern 07...done
                Pattern 08...done
                Pattern 09...done
                Pattern 10...done
                Pattern 11...done
                Pattern 12...done
                Pattern 13...done
                Pattern 14...done
                Pattern 15...done
                Pattern 16...done
                Pattern 17...done
                Pattern 18...done
                Pattern 19...done
                Pattern 20...done
                Pattern 21...done
                Pattern 22...done
                Pattern 23...done
                Pattern 24...done
                Pattern 25...done
                Pattern 26...done
                Pattern 27...done
                Pattern 28...done
                Pattern 29...done
```

Following the pattern information, the boundary scan test lists the failure information. The boundary scan test logs the failing nets using logical names (refer to Figure 22), physical names (refer to Figure 23), or resource information (refer to Figure 24). You select how the boundary scan test logs the nets by clicking on the desired error notation in the `Boundary Scan Options` window.

Figure 22. Logical Boundary Scan Failure Information



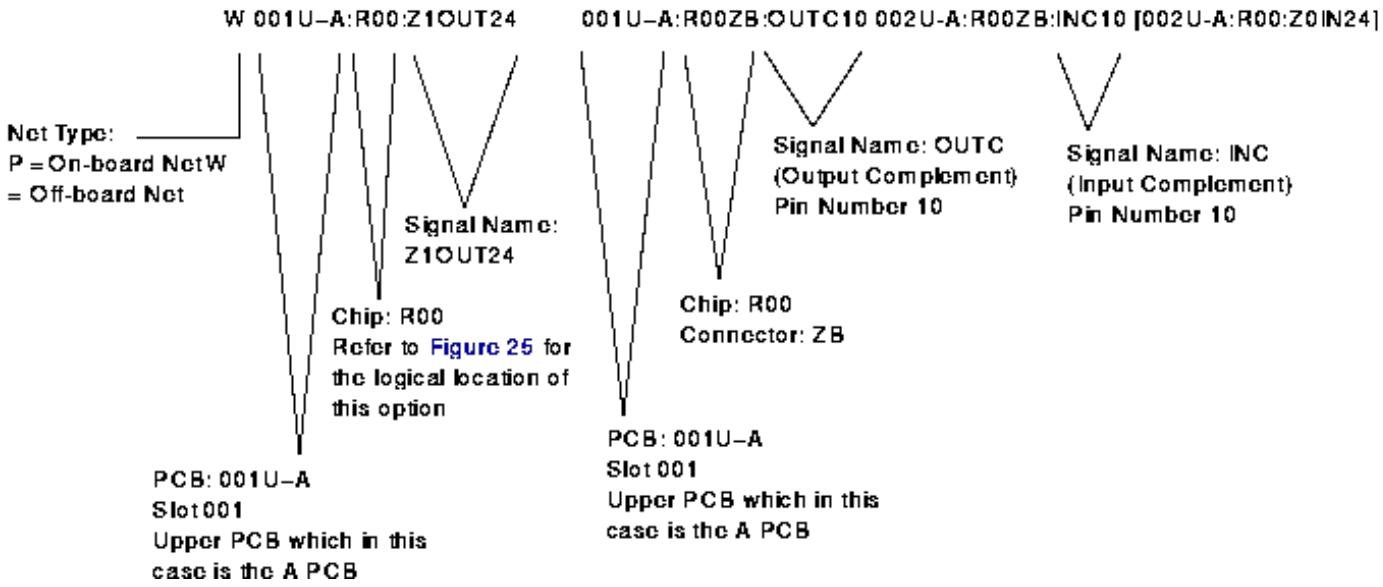


Figure 23. Physical Boundary Scan Failure Information

```
CHAIN     EXPECT                           ACTUAL                           NET INFORMATION (net type: P=on-board net, W=off-board net)
POSITION  DATA                             DATA                             Format of each node: <board>:<chip>:<pin>

00-11753  10101001100110100101100110 0110 11111111111111111111111111111111 W 001U-A:AC0:E9 001U-A:ACZ:35B 002U-A:ACZ:36B [002U-A:AC0:
00-11754  10101001100110101010011001011 0 00000000000000000000000000000000 W 001U-A:AC0:F10 001U-A:ACZ:35 002U-A:ACZ:36 [002U-A:AC0:C
00-11755  10101001100110100101011010101 0 11111111111111111111111111111111 W 001U-A:AC0:D8 001U-A:ACZ:37B 002U-A:ACZ:38B [002U-A:AC0:
00-11756  10101001100110101010010101101 0 00000000000000000000000000000000 W 001U-A:AC0:C7 001U-A:ACZ:37 002U-A:ACZ:38 [002U-A:AC0:B2
```

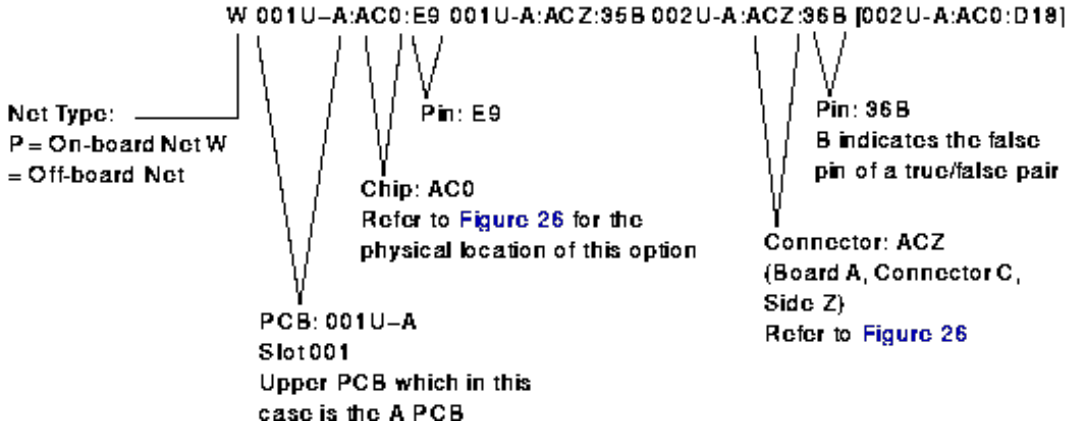
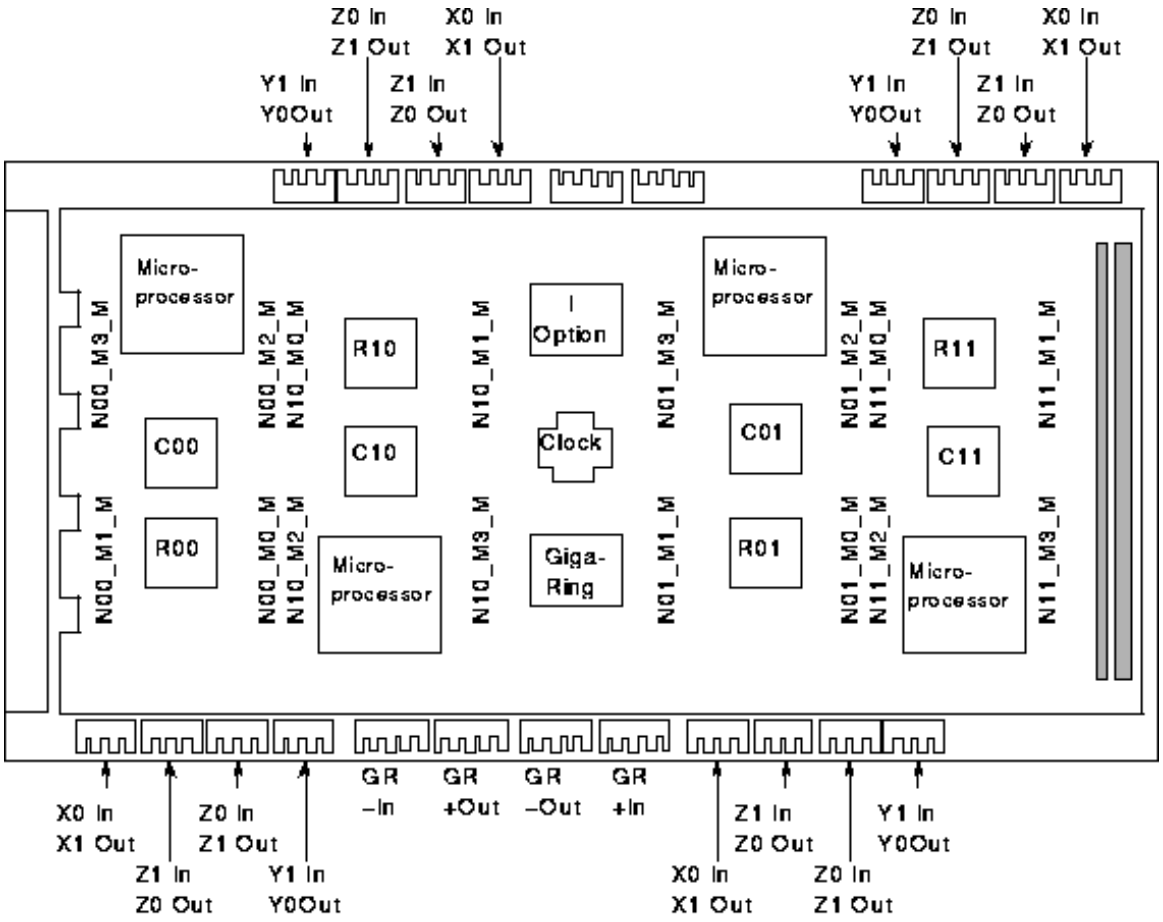


Figure 24. Resource Boundary Scan Failure Information

```
Boundary scan errors detected!!!

Raw pin number: 00-11753
Expected data: 10101001100110100101100110 0110
Actual data:   11111111111111111111111111111111
FAILING BOARD (source): CHASSIS = 0   SLOT = 1   BOARD = Upper(A)
FAILING BOARD (dest): CHASSIS = 0   SLOT = 2   BOARD = Upper(A)
FAILING NET NAME: CHIP = R00       PIN = Z1OUT24
RESILIENCY REQUIREMENT: Disable the -Z port on PWHO 000

Raw pin number: 00-11754
Expected data: 10101001100110101010011001011 0
Actual data:   00000000000000000000000000000000
FAILING BOARD (source): CHASSIS = 0   SLOT = 1   BOARD = Upper(A)
FAILING BOARD (dest): CHASSIS = 0   SLOT = 2   BOARD = Upper(A)
FAILING NET NAME: CHIP = R00       PIN = Z1OUT10
RESILIENCY REQUIREMENT: Disable the -Z port on PWHO 000

Raw pin number: 00-11755
Expected data: 10101001100110100101011010101 0
Actual data:   11111111111111111111111111111111
FAILING BOARD (source): CHASSIS = 0   SLOT = 1   BOARD = Upper(A)
FAILING BOARD (dest): CHASSIS = 0   SLOT = 2   BOARD = Upper(A)
FAILING NET NAME: CHIP = R00       PIN = Z1OUT25
RESILIENCY REQUIREMENT: Disable the -Z port on PWHO 000

Raw pin number: 00-11756
Expected data: 10101001100110101010010101101 0
Actual data:   00000000000000000000000000000000
FAILING BOARD (source): CHASSIS = 0   SLOT = 1   BOARD = Upper(A)
FAILING BOARD (dest): CHASSIS = 0   SLOT = 2   BOARD = Upper(A)
FAILING NET NAME: CHIP = R00       PIN = Z1OUT11
RESILIENCY REQUIREMENT: Disable the -Z port on PWHO 000
```

Figure 25. Logical Option and Connector Locations



NOTE: When the boundary scan test detects an error between the C option and the M option, the test indicates the failing M option using the following format:

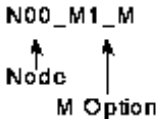
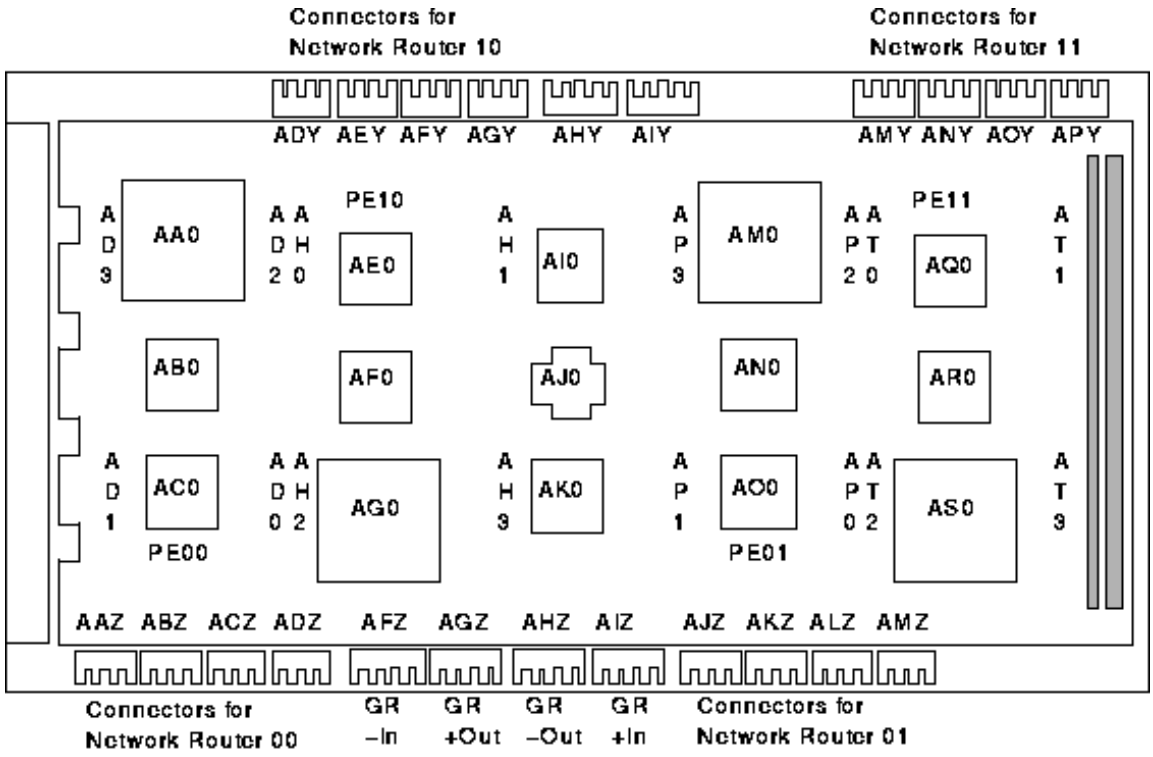


Figure 26. Physical Option and Connector Locations



NOTE: This diagram represents the top of the PCB before it is mounted to the coldplate.

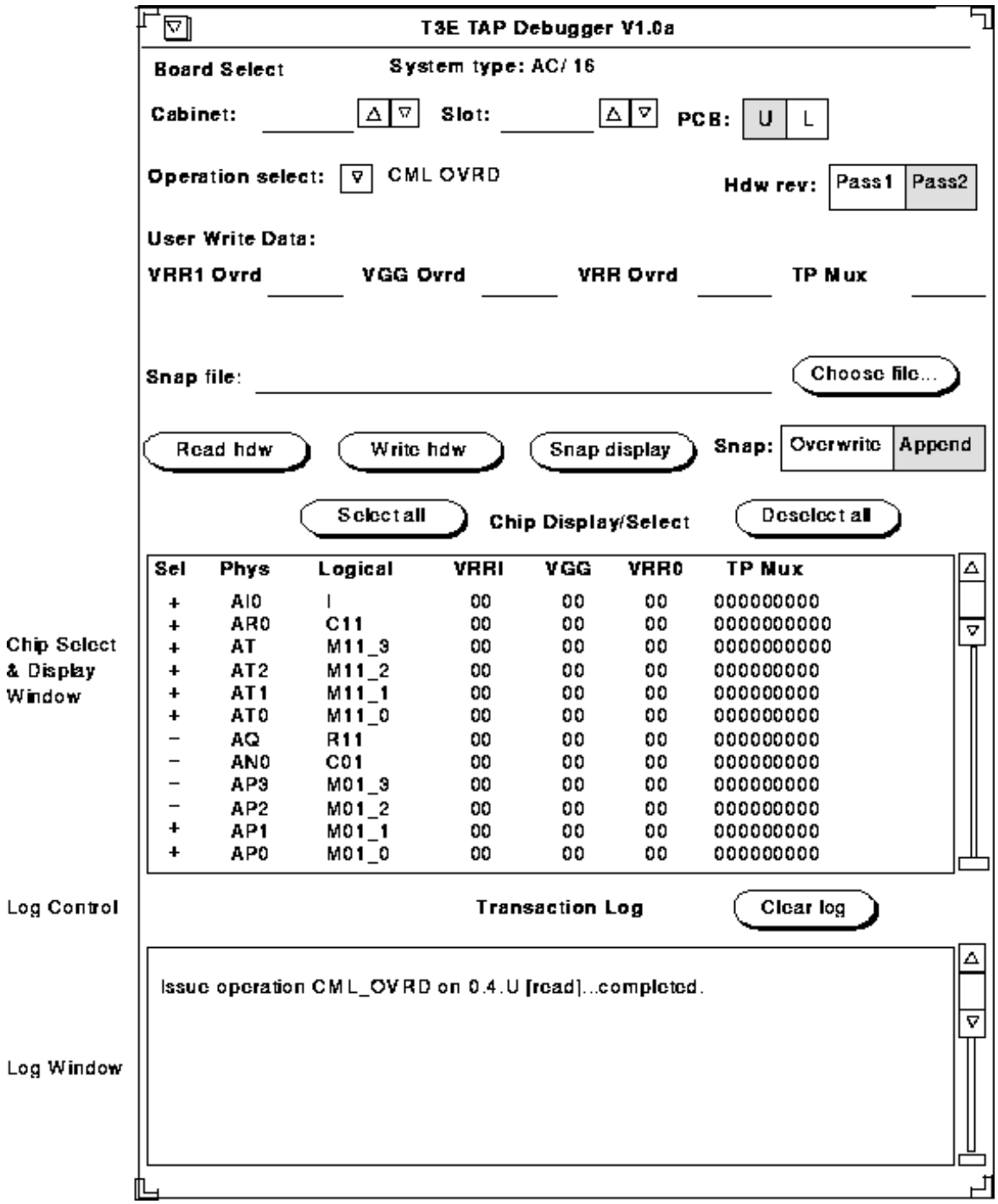
TAP Debugger Test (t3etap)

NOTE: This document applies to `t3etap` version 1.0 and above.

The SWS-based test access point (TAP) debugger program, `t3etap`, is a utility that allows you to exercise various functions of the TAP controller and boundary scan registers in the CRAY SSD-T90 device; you can select the TAP register and the group of options to operate on, enter test patterns, and issue scan operations. Depending on the register that you select, `t3etap` can read data from the register or scan data into the register. `t3etap` displays the results on the screen or writes the results to an output file.

The `t3etap Debugger` window controls all of the functions of the `t3etap` program. Figure 27 shows a snapshot of this window. It is divided into several subsections; the following text describes these subsections.

Figure 27. t3etap Window



Control Section

The control section, which is located in the top portion of the window, contains the main program controls.

Board Select and System Type

The board select identifies the module where you want `t3etap` to execute. Indicate this module by selecting the cabinet number, the slot number, the PCB letter, and the hardware revision of the options. The `t3etap Debugger` window provides choices that are limited to valid values for the configured system type.

NOTE: The cabinet and slot numbers are decimal values. Cabinet numbering begins with 0; slot numbering begins with 1.

The system type identifies the system as an air-cooled (AC) system and indicates the number of PEs. `t3etap` extracts this information from the system configuration information; you cannot alter this information from the `t3etap Debugger` window.

Operation Select

The operation select identifies the function that you want `t3etap` to execute. Table 1 lists the function choices and identifies the types of operation that are valid for each function. Table 1 also indicates whether the output appears on the screen of the SWS or in a file. Functions that are marked as "file output" always send their output to a file rather than to the screen. Functions marked "file input" require their input to be taken from a file rather than from information that the user inputs.

Table 1. Supported TAP Register Functions

Function	Read	Write	File Output	File Input
SDR	Not valid	Valid	Not valid	Not valid
DEVICE ID	Valid	Not valid	Not valid	Not valid
PLL_CLK_OK	Valid	Not valid	Not valid	Not valid
CML_OVRD	Valid	Valid	Not valid	Not valid
UART	Valid	Valid	Not valid	Not valid
RAMBIST	Not valid	Valid	Not valid	Not valid
RAMDUMP	Valid	Not valid	Valid	Not valid
INTERNAL SCAN	Valid	Valid	Valid	Valid
SYSTEM SCAN RESET	Not valid	Valid	Not valid	Not valid

Most operations are not supported by all of the option types. Only the options that support the current operation appear in the option list.

The `SYSTEM SCAN RESET` function is not a true TAP operation; it initiates the special built-in scan clear sequence. When this function executes, `t3etap` ignores the option selection.

User Input Area

The user input area, which is located directly below the operation select, allows you to input information when you select a writable register. Figure 27 shows inputs for the `CML_OVRD` function. After you enter the desired values, write the data to the system. When you select a non-writable function, the user input area is not visible. When you select a function that requires an output file, the user input area displays the message `<< OUTPUT FILE IS REQUIRED BY THIS FUNCTION >>`.

Input and Output Files

The control section provides two lines: one line for an input file name and one line for an output file name. You may enter either a file name or a path name. When you provide the file name, `t3etap` places the file in the current directory (the directory from which you started `t3etap`). To determine alternative file names, click on the `Choose file` button. A popup window appears that lists file names and directories. If you pick a file name from this window, insert the full path name on the line.

The functions listed in Table 1 that require an output file will not execute until you provide a file name. The output file name is also used by the window snap function.

When writing to the hardware, the internal scan operation is the only operation that requires an input data file. This input data file is an ASCII file that contains one or more sets of scan input data (TDI). The TDI entries are indexed by option; the options are numbered in the order in which they appear in the option display. Each entry uses the following format:

TD[n] = <data>

[<data>...]

The index n identifies the option. The data consists of a string of one or more hex digits with no spaces. `t3etap` places these hex digits in the TDI array. If the data provided is shorter than the actual TDI bit string, `t3etap` fills the remainder with zeros. For increased readability, you may break the data into multiple lines; `t3etap` ignores newline characters within the data string. `t3etap` terminates the data when the first character it encounters is not a newline or hex digit. The TD entries may be in any order and unused options do not need entries.

NOTE: `t3etap` uses this format when it reads the internal scan data from the hardware into a file. This allows `t3etap` to feed the output file directly back in as an input file. When `t3etap` writes an internal scan data file, it includes a TD entry for every option. For the options that do not support internal scan and for the options that are deselected, `t3etap` enters a single zero value into the TD entry.

Operation Controls

The `Read hdw` button and `Write hdw` button initiate the currently selected function. These buttons are only enabled when you select a valid function.

The `Snap display` button copies the current option window display to an output file. The snap setting determines whether the file is appended to the output file or the file overwrites the output file. The snap button is inactive for functions that write their output directly to a file.

The `Select all` button selects all of the options in the `Chip Display/Select` window. The `Deselect all`

button deselects all of the options in the `Chip Display/Select` window.

Chip Select/Display Window

This window lists all of the options that support the currently selected operation. `t3etap` uses the first column of the display to select the option(s) that it will operate on. The options preceded by a dash (-) are deselected; the options preceded by a plus sign (+) are selected.

You can select or deselect options by clicking on the `Select all` button or the `Deselect all` button; or by using the mouse buttons. The three mouse buttons operate as follows:

- The left (select) button toggles the selection
- The middle (adjust) button turns a selection on
- The right (menu) button turns a selection off

In order for the mouse to work, point the cursor at the + or - character. You can also hold the mouse button down and drag the mouse up or down to operate on more than one line. As the pointer approaches the top or bottom of the window, the view scrolls up or down automatically.

The `Chip Select/Display` window contains several other columns of information: the physical name of the options, the logical name of the options, VRRI, VGG, VRR0, and TP Mux.

NOTE: You can change the length of the `Chip Select/Display` window from the default of 16 lines. To change the length, add the following entry in your Xdefaults file (normally $HOME/.Xdefaults):

```
t3etap.chipWinLength: new_length
```

new_length is an integer value between 2 and 30. Any other values cause `t3etap` to print a warning and use the default setting. After adding the line to your Xdefaults file, execute the command **`xrdb -merge .Xdefaults`**. This command applies your change.

Transaction Log Window

This window records each operation you perform and the board on which the operation was performed. The window also lists whether the operation succeeded or failed. The `Clear` button clears the log contents. You can save the log to a file by using the standard menu of the window. (Access the standard menu by pressing the menu button with the pointer over the window).

How to Initiate t3etap

You can initiate `t3etap` by using command line syntax or `t3ems`.

Initiating t3etap by Using Command Line Syntax

1. Change to the /opt/CYRIdiag/t3e/bin directory.

At the prompt, type:

```
cd /opt/CYRIdiag/t3e/bin
```

2. Enter the `t3etap` command with desired options.

At the prompt, type:

```
t3etap [-r] [-c tck_width] [-i input_data_path] [-s tv_bd+chain] [-G host[:port]]
```

The `t3etap` command accepts the following options:

`-r`
This option causes `t3etap` to execute a scan reset sequence only; `t3etap` does not bring up the user interface.

`-c tck_width`
This option overrides the default TCK pulse width. This value can be any number between 3 and 60; the default value is 3.

`-i input_data_path`
This option allows you to bring up `t3etap` using a different scan directory than the default scan directory (/opt/CYRIdiag/t3e/t3esys/scan). Use this option only when you know how to generate customized data bases.

`-s tv_bd+chain`
This option defines the scan master and the scan chains for a module that is being tested in a test vehicle.

This option uses the following format:

`<SM>+<top PCB chain#>`

`<SM>` is the scan master board (u or a for upper, l or b for lower).

`<top PCB chain#>` is an even scan chain number (0, 2, ..., 14). The odd-numbered scan chain directly relates to the even-numbered chain. For example, when the `<def>` is `b+4`, the B PCB of slot 1 is scan master; the top PCBs use scan chain 4 and the bottom PCBs use scan chain 5.

The default format is `u+0`. (The A PCB of slot 1 is the scan master; the top PCBs use chain 0 and the bottom PCBs use chain 1.)

`-G host[:port]`
This option overrides the default host name and port number. `t3etap` uses the host name and port to connect to the GigaRing server process. The default host name is "localhost" (assuming that the server is running on the same host as `t3etap`) and the default port number is 5000. Normally, the port number should not have to be changed; therefore, the port number is optional.

Initiating t3etap by Using t3ems

NOTE: The CRAY SSD-T90 device uses the same offline diagnostic maintenance system as the CRAY T3E system; therefore, the offline diagnostic maintenance system windows are labeled CRAY T3E.

1. Bring up `t3ems`.

   At the prompt, type **`t3ems`**

   NOTE: `t3ems` is located in the /opt/CYRIdiag/t3e/bin directory.

2. Select the `t3etap` test from the `Tools` menu.

   The `Boundary scan options` window appears on the screen (refer to Figure 28).

3. Make the appropriate option selections.

   `TCK cycle width`
   This option overrides the default TCK pulse width. This value can be any number between 3 and 60.

   `GigaRing host`
   This option selects the host system.

   `GigaRing port`
   This option selects the I/O port.

   `Scan master`
   This option selects the scan master PCB and the scan chain for the A (top) PCB. This option is only available when you are running `t3etap` on a module in a test vehicle.

4. Click on 

to start the `t3etap` test.

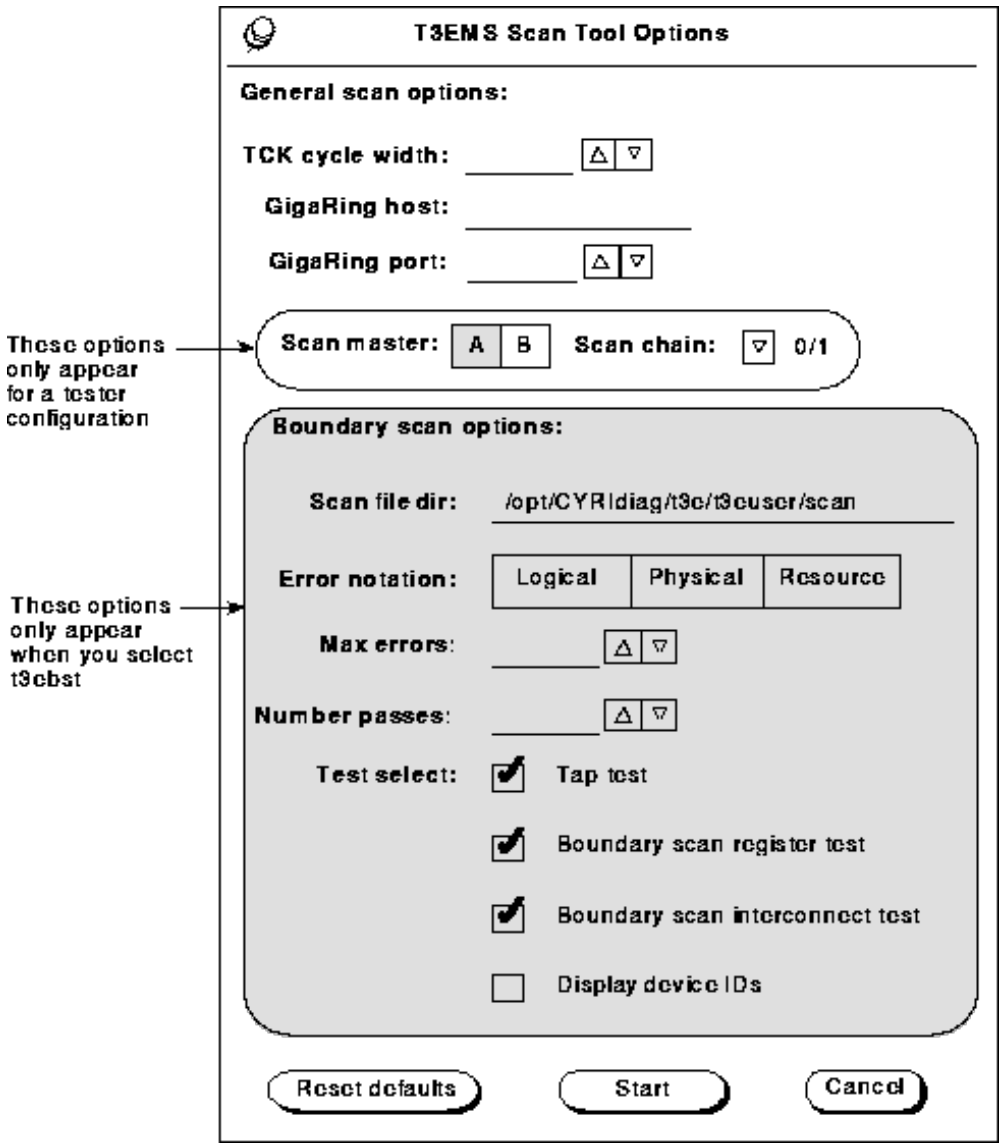
   Clicking on this button starts the `t3etap` test. `t3ems` directs the status and error information to the log window.

   After you start `t3etap`, `t3etap` calls a scan initialization routine that sets up data structures and reads the system configuration to determine whether the system is an air-cooled system, a system or a tester, and to determine the number of PEs in the system.

   `t3etap` also performs initial scan tests. When a failure occurs, `t3etap` prints the error information and terminates without displaying the main interface window. When the initial scan tests are successful, `t3etap` prints information about the test results and displays the main window shown in Figure 28.

   NOTE: The system configuration database server must be running and have the correct system setup for `t3etap` to function properly. When the system configuration server it is not set up correctly, use `t3ems` to correct the system type and the number of PEs. After you make the corrections, restart `t3etap`.

   Figure 28. T3EMS Scan Tool Options Window


T3EMS Scan Tool Options
General scan options:
TCK cycle width:
GigaRing host:
GigaRing port:
These options only appear for a tester configuration
Scan master: A B
Scan chain: 0/1
Boundary scan options:
Scan file dir: /opt/CYRIdiag/t3c/t3cuser/scan
These options only appear when you select t3cbst
Error notation: Logical Physical Resource
Max errors:
Number passes:
Test select:
Tap test
Boundary scan register test
Boundary scan interconnect test
Display device IDs
Reset defaults
Start
Cancel