SYSTEM CABLING

Figures

Sparc 5 Workstation-to-Support System Connections

Figure 4 shows the connections between a Sparc 5 workstation and the support system chassis. The fiber-optic cables plug into ports PHY A and PHY B on the support system chassis and connect to the FDDI port on the back of a Sparc 5 workstation. For more information on the support system and the Sparc 5 workstation connections, refer to the *CRAY T90 Series Support System* document, publication number HTM-xx-x.

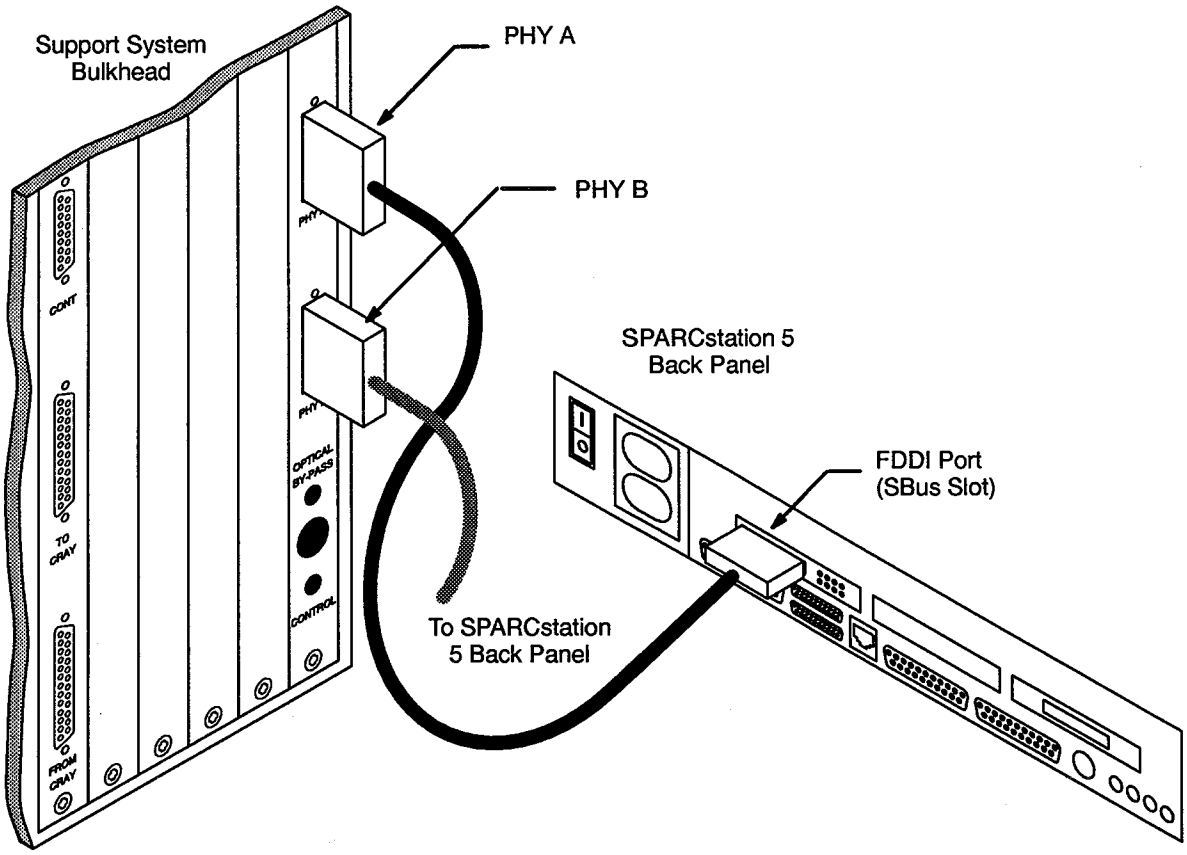

Figure 4. Support System-to-Sparc 5 Workstation Connections

Error Logger, Maintenance, Boundary Scan, and Support Channels

The error logger, maintenance, boundary scan and support channels transfer information between FEI-3 boards in the support system chassis and the mainframe. The user interfaces to these channels are the MWS and the OWS. The MWS and OWS access these channels through the FDDI network (refer to Figure 5).

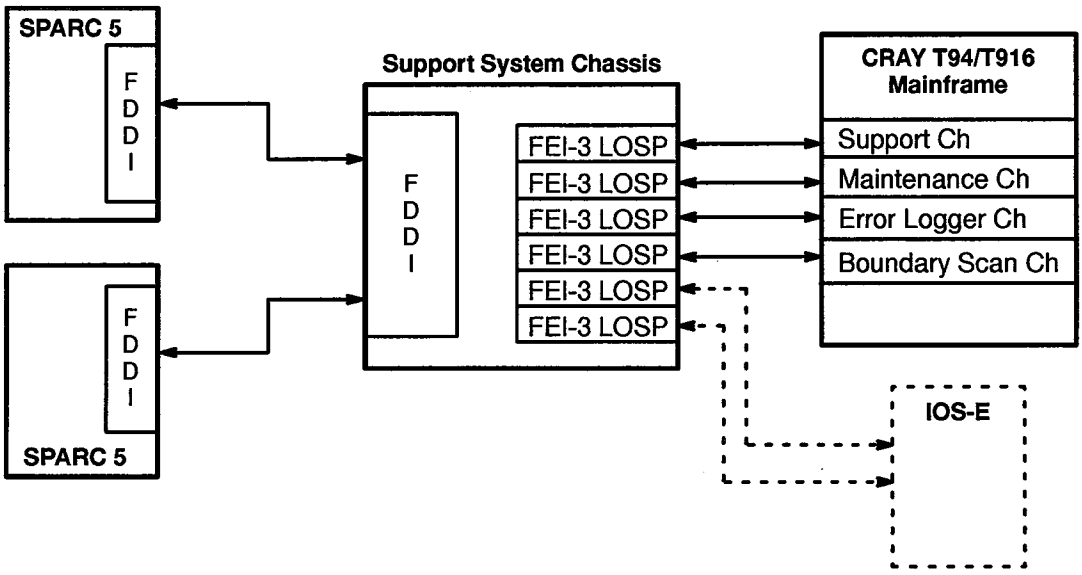

Figure 5. Error Logger, Maintenance, and Support Channel Configuration

The error logger channel, the maintenance channel and the support channel connect to the mainframe bulkhead and are routed inside the mainframe to the IO module. The error logger channel transfers error information. The maintenance channel enables you to perform maintenance functions such as configuring the system, sending and controlling sanity code, and performing the various master clears in the system. The support channel enables an OWS user to access the UNICOS operating system to perform specific software functions.

The boundary scan channel also connects to the mainframe bulkhead. From the bulkhead, this channel connects to the BS module. Harness assemblies from the BS module connect to the maintenance connector on each system module. The BS module sends and receives the continuity line sensing signals and contains all of the boundary scan logic.

Configuring the Error Logger, Maintenance, Boundary Scan, and Support Channels in SCE

The error logger, maintenance, boundary scan, and support channels must be configured in SCE. Figure 6 shows the base window for SCE. When you configure the Maintenance Port/Channel, Error Logger Channel, and Boundary Scan Channel, you are actually selecting the FEI-3 board in the support system chassis that the channel connects to.

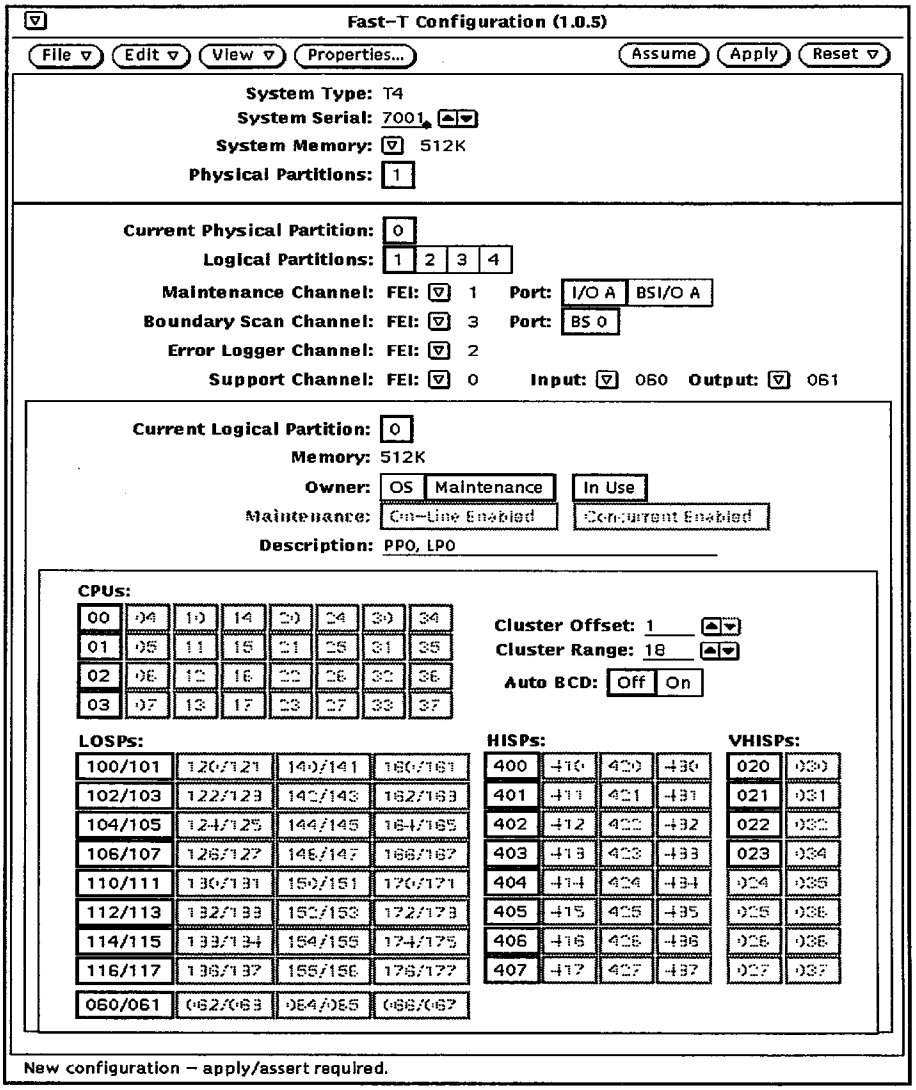

Figure 6. SCE Base Window

The Maintenance Port/Channel selection configures the maintenance channel in a normal system configuration. This channel should be assigned to channel 1. The I/O A or (I/O I) selection selects which IO

module the maintenance channel connects to. In a CRAY T94 system, I/O A is the only selection available because there can be only one IO module in the system. The BS I/O A selection applies only to a 4-processor tester when the maintenance channel is connected to a BS module plugged into the I/O module slot.

The Error Logger Channel selection configures the error logger channel. This channel should be assigned to channel 2.

The Boundary Scan Channel selection configures the boundary scan channel. In a CRAY T94 or CRAY T916 system, BS0 is the only selection available and should be assigned to channel 3. In a CRAY T932 system, BS0 and BS1 are the selections available. The two selections enable you to configure the two boundary scan channels required in a CRAY T932 system. In addition to configuring the boundary scan channel in SCE, you must also indicate the channel number in the command line of the `bscan` program. Refer to the *Boundary Scan System Test* document, publication number HDM-xxx-xx, for more information on how to run `bscan`.

The Support Channel selection configures the support channel. This channel should be assigned to channel 0. The Input and Output selections enable you to configure the support channel as any LOSP channel number.

WIN Channels

The IOS has two dedicated workstation interface channel pairs: WIN 0 and WIN 1. WIN 0 enables the OWS to communicate with the IOS and WIN 1 enables the MWS to communicate with the IOS. The workstations use these channels to read the IOS status, read or write data to memory in an I/O processor (IOP), and perform maintenance tasks such as deadstarting or master clearing an IOP. Figure 7 shows the configuration for the WIN channels.

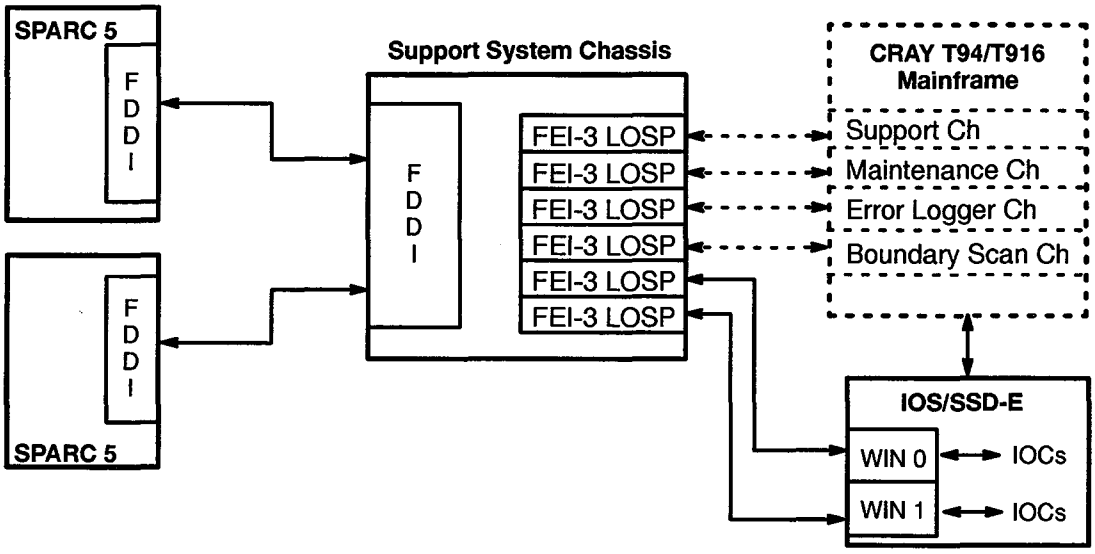

Figure 7. WIN Channel Configuration

SSD-E Maintenance Channel

An SSD-E system requires a maintenance channel for reporting errors back to the MWS. In a 600 or 800 series IOS/SSD-E chassis, the SSD-E shares this maintenance channel with the WIN channel paths of the IOS. In a 700 series chassis IOS/SSD-E, this maintenance channel may be shared with the WIN channel paths or it may be a dedicated maintenance channel. If this channel is a dedicated maintenance channel, an additional FEI-3 board is required in the support system, with a physical channel connection to the SSD-E. Figure 8 shows the configuration for the SSD maintenance channels.

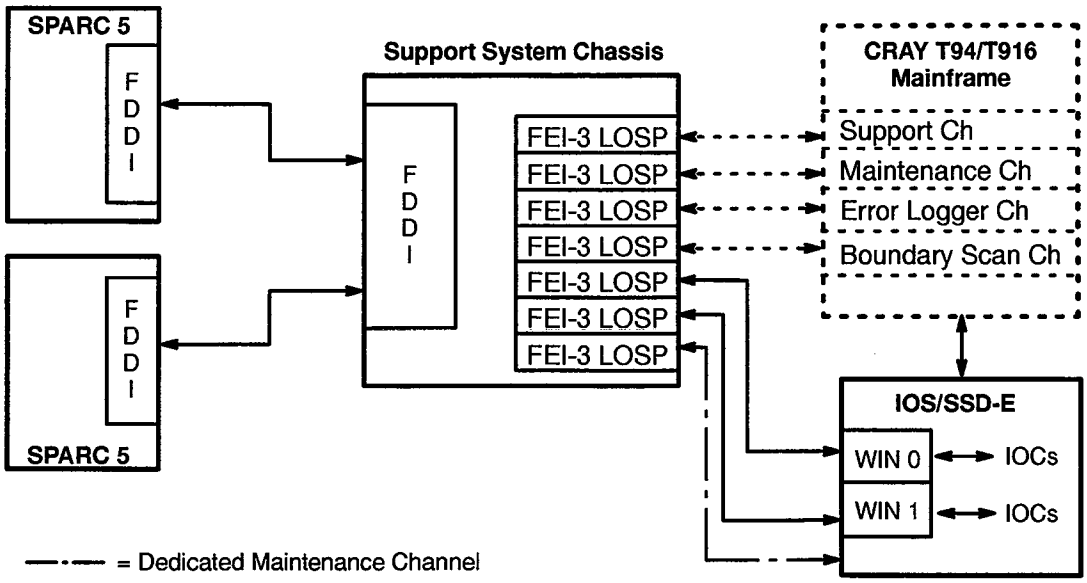

Figure 8. SSD Maintenance Channel Configuration

IOS/SSD-E-to-Mainframe Channel Connections

All connections between the mainframe bulkhead and the IOS/SSD bulkhead use Micro-D connectors. The VHISP channels use a 100-position connector (refer to Figure 9), and the LOSP and HISP channels use a 51-position connector (refer to Figure 10).

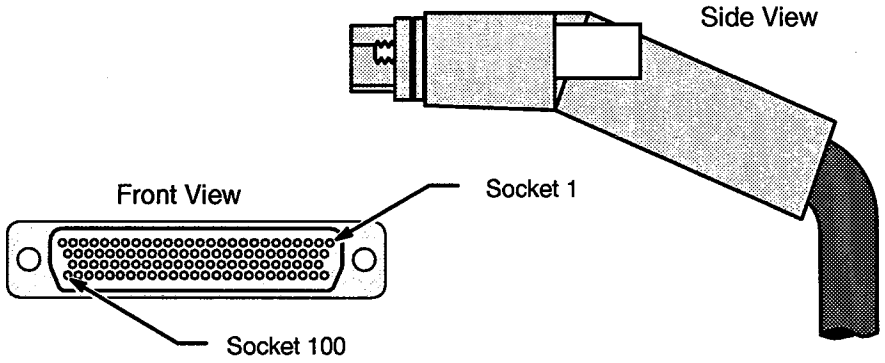

Figure 9. 100-position D-microminiature Connector

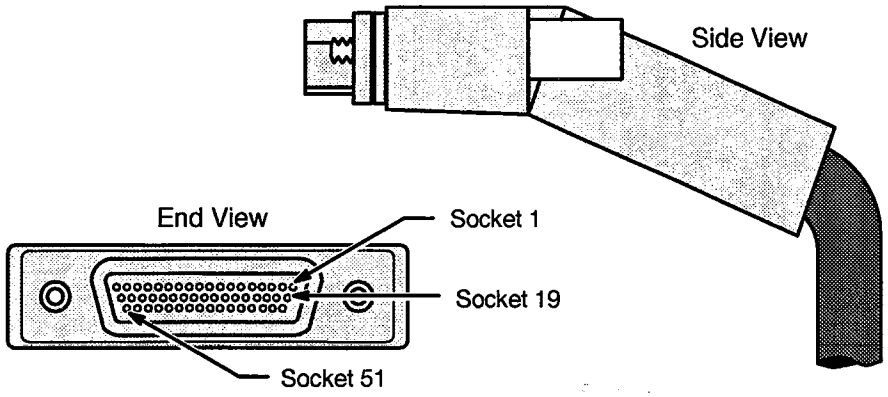

Figure 10. 51-position D-microminiature Connector

LOSP, HISP, and VHISP channels are directly connected from the mainframe to the IOS. Figure 11 shows an example of these cabling connections.

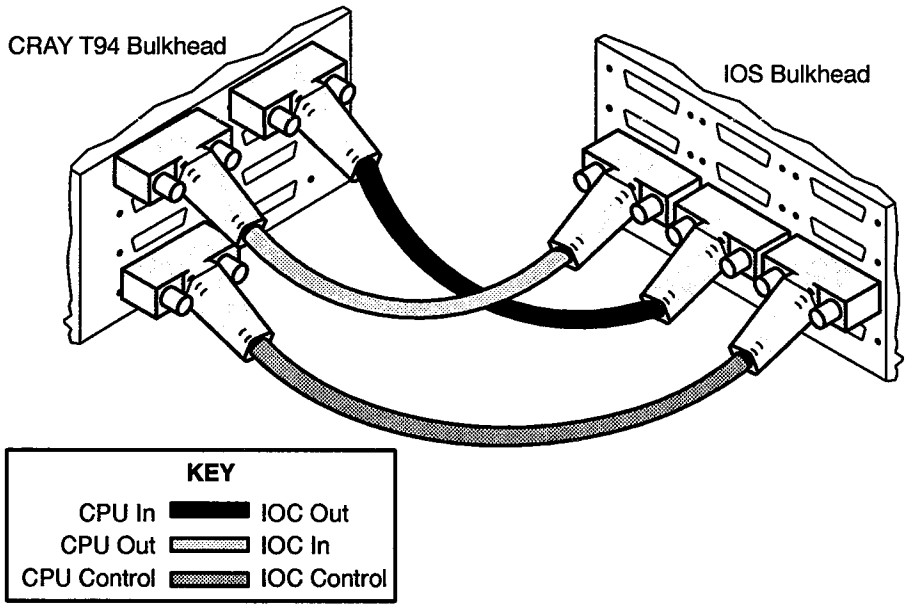

Figure 11. Mainframe-to-IOS/SSD-E Bulkhead Connections (Example)

LOSP, HISP, and VHISP Channels

Each LOSP, HISP, or VHISP channel is actually a pair of channels. Figure 12 shows a typical configuration for LOSP, HISP, and VHISP channels in a four-processor CRAY T90 series system. LOSP channels transfer control information between the mainframe and the IOS and between the mainframe and the support system. CPUs in the mainframe control the LOSP channels. The HISP channels transfer data between the IOS and the mainframe or between the IOS and the SSD. The I/O clusters (IOCs) in the IOS control the HISP channels. VHISP channels transfer data between the mainframe and the SSD. CPUs in the mainframe control the VHISP channels.

Channel configurations and numbering varies depending on the system configuration. Refer to the *CRAY T90 Series I/O Theory of Operations*, publication number HTM-xxx-x, for more information on LOSP, HISP, and VHISP channels. Refer to the *System Configuration Environment* document, publication number HDM-xxx-x, for more information on SCE and configuring the error logger channel and the maintenance channel.

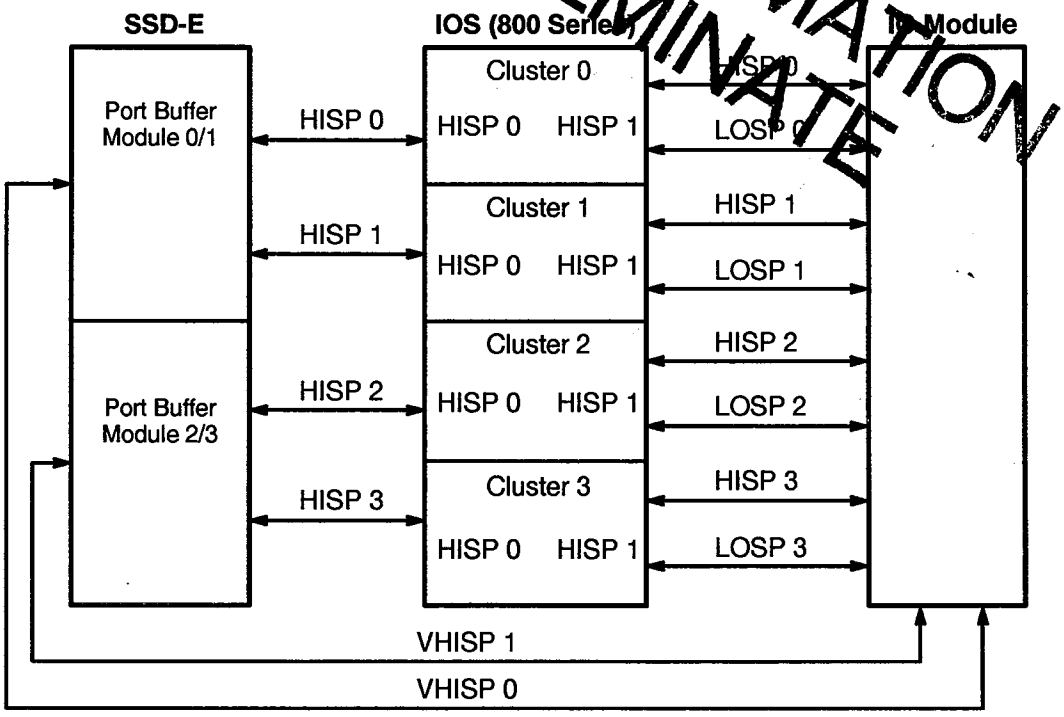

Figure 12. Typical LOSP, HISP, and VHISP Channel Configurations for a Four-processor System (with an 800 Series IOS/SSD-E)

MCU/PINT Channel

A programmable interrupt enables any IOC in the IOS-E to interrupt any logical CPU or group of CPUs. A programmable interrupt quarter board (PINT) in the IOS-E receives interrupt signals from each of the IOCs in the IOS-E. The PINT then sends the interrupt signals to the MCU/PINT fuzz-button connector on the IO module located inside the mainframe.

Figure 13 shows an example of a programmable interrupt configuration for a CRAY T90 series system. The MCU/PINT channel connects to the IOS-E bulkhead at the location labeled Programmable Interrupt and connects to the mainframe bulkhead at the location labeled MCU PINT.

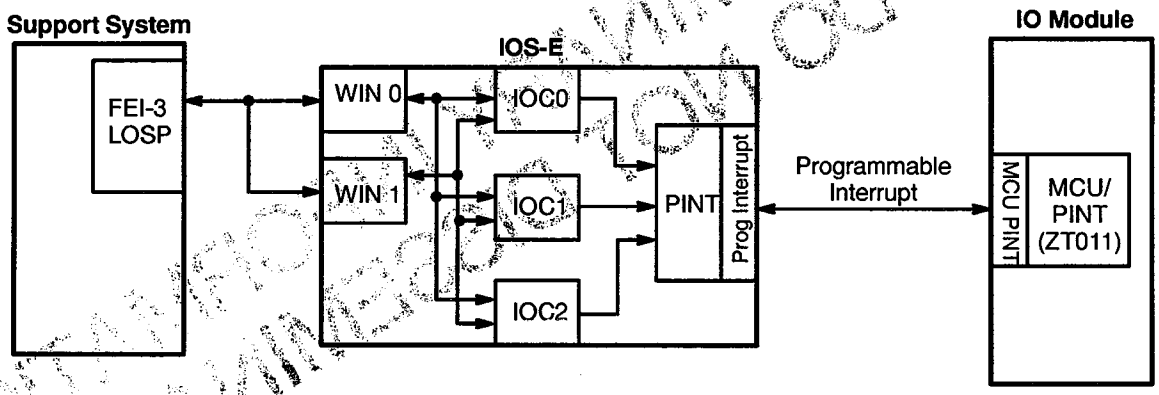

Figure 13. Programmable Interrupt Configuration

CRAY T90 Series Mainframe Bulkhead Connections

CRAY T90 series systems use one standard bulkhead. Figure 17 is the bulkhead map for a CRAY T94 mainframe. Figure 18 is the bulkhead map for CRAY T916 and CRAY T932 mainframes. The layouts of the two bulkheads differ; however, the bulkhead connector and the channel and function associated with it are the same in any CRAY T90 series system. Table 1 lists the bulkhead connector number, the type of channel, and the bits associated with the connector. The table also includes the number and location of the fuzz-button connector with which each bulkhead connector is associated with.

The BHTool program enables you to create and print a CRAY T90 series mainframe bulkhead map. For more information on BHTool, refer to the *BHTool User Guide*, publication number HGM-018-0.

Table 1. Mainframe Bulkhead Connections

Bulkhead Connector	Input/ Output	Channel	Functions	Connector		
				ZT__	Board	Loc.
00	Out	VHISP 0	Even word data bits 00 – 49	000	1	EA
01	Out	VHISP 0	Even word data bits 50 – 63 Even word check bits 00 – 07 Odd word data bits 00 – 27			
02	out	VHISP 0	Odd word data bits 28 – 63 Odd word check bits 00 – 07			
03	Out	VHISP 0	Block length bits 10 – 31 Control			
04	Out	Maintenance	Data/control	008	2	EA
05	Out	VHISP 1	Even word data bits 00 – 49	001	1	EB
06	Out	VHISP 1	Even word data bits 50 – 63 Even word check bits 00 – 07 Odd word data bits 00 – 27			
07	Out	VHISP 1	Odd word data bits 28 – 63 Odd word check bits 00 – 07			
08	Out	VHISP 1	Block length bits 10 – 31 Control			
09	Out	Support	Data/control	009	2	EB
10	Out	VHISP 2	Even word data bits 00 – 49	002	1	EC
11	Out	VHISP 2	Even word data bits 50 – 63 Even word check bits 00 – 07 Odd word data bits 00 – 27			
12	Out	VHISP 2	Odd word data bits 28 – 63 Odd word check bits 00 – 07			
13	Out	VHISP 2	Block length bits 10 – 31 Control			
14	Out	Error logger	Data/control	010	2	EC
15	Out	VHISP 3	Even word data bits 00 – 49	003	1	ED
16	Out	VHISP 3	Even word data bits 50 – 63 Even word check bits 00 – 07 Odd word data bits 00 – 27			
17	Out	VHISP 3	Odd word data bits 28 – 63 Odd word check bits 00 – 07			
18		VHISP 3	Block length bits 10 – 31 Control			
19	Out	MCU/Pint	Data/control	011	2	ED

Table 1. Mainframe Bulkhead Connections (continued)

Bulkhead Connector	Input/ Output	Channel	Functions	Connector		
				ZT__	Board	Loc.
20	In	VHISP 0	Even word data bits 00 – 49	008	2	EA
21	In	VHISP 0	Even word data bits 50 – 63 Even word check bits 00 – 07 Odd word data bits 00 – 27			
22	In	VHISP 0	Odd word data bits 28 – 63 Odd word check bits 00 – 07			
23	In	VHISP 0	Block length bits 00 – 09 Address bits 00 – 31			
24	In	Maintenance	Data/control	008	2	EA
25	In	VHISP 1	Even word data bits 00 – 49	009	2	EB
26	In	VHISP 1	Even word data bits 50 – 63 Even word check bits 00 – 07 Odd word data bits 00 – 27			
27	In	VHISP 1	Odd word data bits 28 – 63 Odd word check bits 00 – 07			
28	In	VHISP 1	Block length bits 0 – 9 Address bits 00 – 31			
29	In	Support	Data/control	009	2	EB
30	In	VHISP 2	Even word data bits 00 – 49	010	2	EC
31	In	VHISP 2	Even word data bits 50 – 63 Even word check bits 00 – 07 Odd word data bits 00 – 27			
32	In	VHISP 2	Odd word data bits 28 – 63 Odd word check bits 00 – 07			
33	In	VHISP 2	Block length bits 0 – 9 Address bits 00 – 31			
34	In	Error logger	Data/control	010	2	EC
35	In	VHISP 3	Even word data bits 00 – 49	011	2	ED
36	In	VHISP 3	Even word data bits 50 – 63 Even word check bits 00 – 07 Odd word data bits 00 – 27			
37	In	VHISP 3	Odd word data bits 28 – 63 Odd word check bits 00 – 07			
38		VHISP 3	Block length bits 0 – 9 Address bits 00 – 31			
39	In	MCU/Pint	Data/control	011	2	ED

Table 1. Mainframe Bulkhead Connections (continued)

Bulkhead Connector	Input/ Output	Channel	Functions	Connector		
				ZT__	Board	Loc.
40	Out	HISP 0	Data bits 00 – 23	012	2	FA
41	Out	HISP 0	Data bits 24 – 47			
42	Out	HISP 0	Data bits 48 – 63 Check bits 00 – 07			
43	Out	HISP 0	Address/control			
44	Out	LOSP 0	Data/control	012	2	FA
45	Out	HISP 2	Data bits 00 – 23	013	2	FB
46	Out	HISP 2	Data bits 24 – 47			
47	Out	HISP 2	Data bits 48 – 63 Check bits 00 – 07			
48	Out	HISP 2	Address/control			
49	Out	LOSP 2	Data/control	013	2	FB
50	Out	HISP 4	Data bits 00 – 23	014	2	FC
51	Out	HISP 4	Data bits 24 – 47			
52	Out	HISP 4	Data bits 48 – 63 Check bits 00 – 07			
53	Out	HISP 4	Address/control			
54	Out	LOSP 4	Data/control	014	2	FC
55	Out	HISP 6	Data bits 00 – 23	015	2	FD
56	Out	HISP 6	Data bits 24 – 47			
57	Out	HISP 6	Data bits 48 – 63 Check bits 00 – 07			
58	Out	HISP 6	Address/control			
59	Out	LOSP 6	Data/control	015	2	FD
60	In	HISP 0	Data bits 00 – 23	004	1	FA
61	In	HISP 0	Data bits 24 – 47			
62	In	HISP 0	Data bits 48 – 63 Check bits 00 – 07			
63	In	HISP 0	Address/control			
64	In	LOSP 0	Data/control	012	2	FA
65	In	HISP 2	Data bits 00 – 23	005	1	FB
66	In	HISP 2	Data bits 24 – 47			
67	In	HISP 2	Data bits 48 – 63 Check bits 00 – 07			
68	In	HISP 2	Address/control			
69	In	LOSP 2	Data/control	013	2	FB

Table 1. Mainframe Bulkhead Connections (continued)

Bulkhead Connector	Input/ Output	Channel	Functions	Connector		
				ZT__	Board	Loc.
70	In	HISP 4	Data bits 00 – 23	006	1	FC
71	In	HISP 4	Data bits 24 – 47			
72	In	HISP 4	Data bits 48 – 63 Check bits 00 – 07			
73	In	HISP 4	Address/control			
74	In	LOSP 4	Data/control	014	2	FC
75	In	HISP 6	Data bits 00 – 23	007	1	FD
76	In	HISP 6	Data bits 24 – 47			
77	In	HISP 6	Data bits 48 – 63 Check bits 00 – 07			
78	In	HISP 6	Address/control			
79	In	LOSP 6	Data/control	015	2	FD
80	Out	HISP 1	Data bits 00 – 23	012	2	FA
81	Out	HISP 1	Data bits 24 – 47			
82	Out	HISP 1	Data bits 48 – 63 Check bits 00 – 07			
83	Out	HISP 1	Address/control			
84	Out	LOSP 1	Data/control	004	1	FA
85	Out	HISP 3	Data bits 00 – 23	013	2	FB
86	Out	HISP 3	Data bits 24 – 47			
87	Out	HISP 3	Data bits 48 – 63 Check bits 00 – 07			
88	Out	HISP 3	Address/control			
89	Out	LOSP 3	Data/control	005	1	FB
90	Out	HISP 5	Data bits 00 – 23	014	2	FC
91	Out	HISP 5	Data bits 24 – 47			
92	Out	HISP 5	Data bits 48 – 63 Check bits 00 – 07			
93	Out	HISP 5	Address/control			
94	Out	LOSP 5	Data/control	006	1	FC
95	Out	HISP 7	Data bits 00 – 23	015	2	FD
96	Out	HISP 7	Data bits 24 – 47			
97	Out	HISP 7	Data bits 48 – 63 Check bits 00 – 07			
98	Out	HISP 7	Address/control			
99	Out	LOSP 7	Data/control	007	1	FD

Table 1. Mainframe Bulkhead Connections (continued)

Bulkhead Connector	Input/ Output	Channel	Functions	Connector		
				ZT__	Board	Loc.
100	In	HISP 1	Data bits 00 – 23	004	1	FA
101	In	HISP 1	Data bits 24 – 47			
102	In	HISP 1	Data bits 48 – 63 Check bits 00 – 07			
103	In	HISP 1	Address/control			
104	In	LOSP 1	Data/control	004	1	FA
105	In	HISP 3	Data bits 00 – 23	005	1	FB
106	In	HISP 3	Data bits 24 – 47			
107	In	HISP 3	Data bits 48 – 63 Check bits 00 – 07			
108	In	HISP 3	Address/control			
109	In	LOSP 3	Data/control	005	1	FB
110	In	HISP 5	Data bits 00 – 23	006	1	FC
111	In	HISP 5	Data bits 24 – 47			
112	In	HISP 5	Data bits 48 – 63 Check bits 00 – 07			
113	In	HISP 5	Address/control			
114	In	LOSP 5	Data/control	006	1	FC
115	In	HISP 7	Data bits 00 – 23	007	1	FD
116	In	HISP 7	Data bits 24 – 47			
117	In	HISP 7	Data bits 48 – 63 Check bits 00 – 07			
118	In	HISP 7	Address/control			
119	In	LOSP 7	Data/control	007	1	FD
120	– –	Controller	Main controller signals	J1 (on controller panel)		
121	– –	Controller	Standby controller signals	J2 (on controller panel)		
122	– –	Controller	Power supply margining Power supply current monitors	J3 (on controller panel)		
123	– –	Controller	Spare	– –		
124	In	LOSP	Boundary Scan	FA (on BS module)		
125	Out	LOSP	Boundary Scan	FA (on BS module)		
126	– –	Spare	– –	– –		

Bulkhead-to-IO Module Connections

All internal connections from the bulkhead are part of a harness assembly that goes to a fuzz-button connector. Sixteen harness assemblies (five different wiring configurations) are associated with the sixteen different ZT connectors on the IO module. Figure 14 illustrates an I/O harness assembly. Each assembly has either 4, 6, or 10 connections from the mainframe bulkhead with either 51-pin or 100-pin micro-D style connectors. The VHISP connections use 100-pin connectors. The HISP, LOSP, error logger, support, maintenance, and MCU/PINT channels use 51-pin connectors.

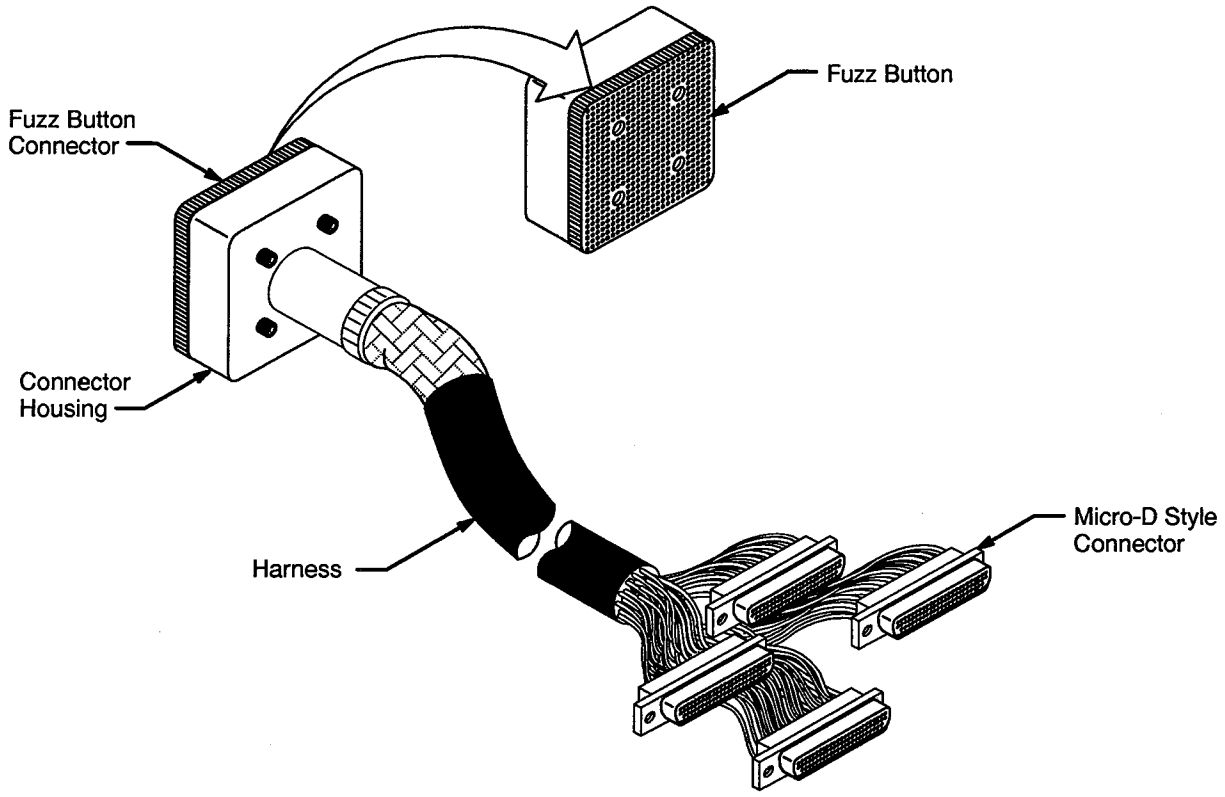

Figure 14. Fuzz-button Connector Assembly

Each fuzz button in a fuzz-button connector aligns with one pad in a ZT connector. Figure 15 shows a fuzz-button connector and the numbering scheme for each fuzz button.

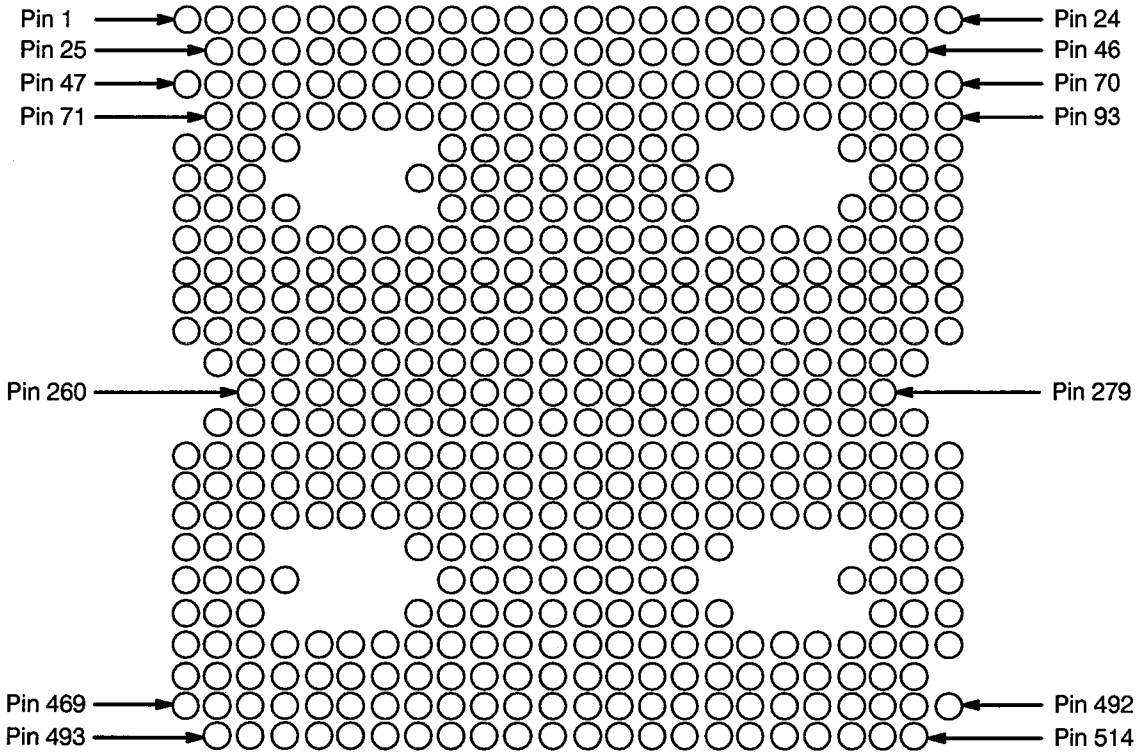

Figure 15. Fuzz-button Connector

Control System Cable Connections

Figure 16 shows the connectors on the control system bulkhead. Four connectors (J4 through J7) are the connections to the primary (J5 and J4) and back-up (J6 and J7) state logic processor and connect to the serial ports in the support system chassis. Three connectors (J1 through J3) are the interface to the controller used to monitor main controller signals, standby controller signals, and power-supply margining. These connectors connect to the mainframe bulkhead connectors 120, 121, and 122. Refer to Table 1 for specific information on the mainframe bulkhead connections.

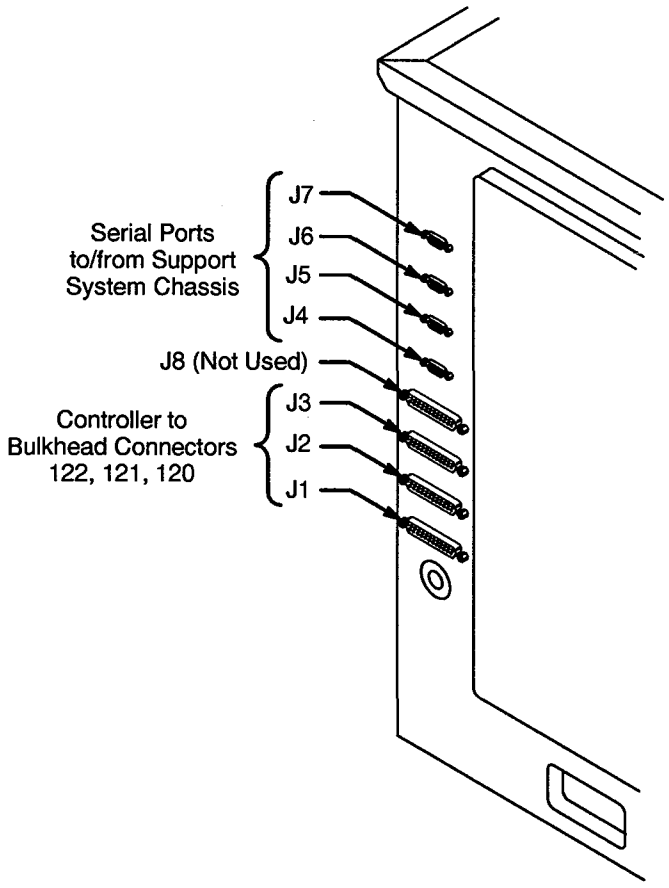

Figure 16. Control System Cable Connections

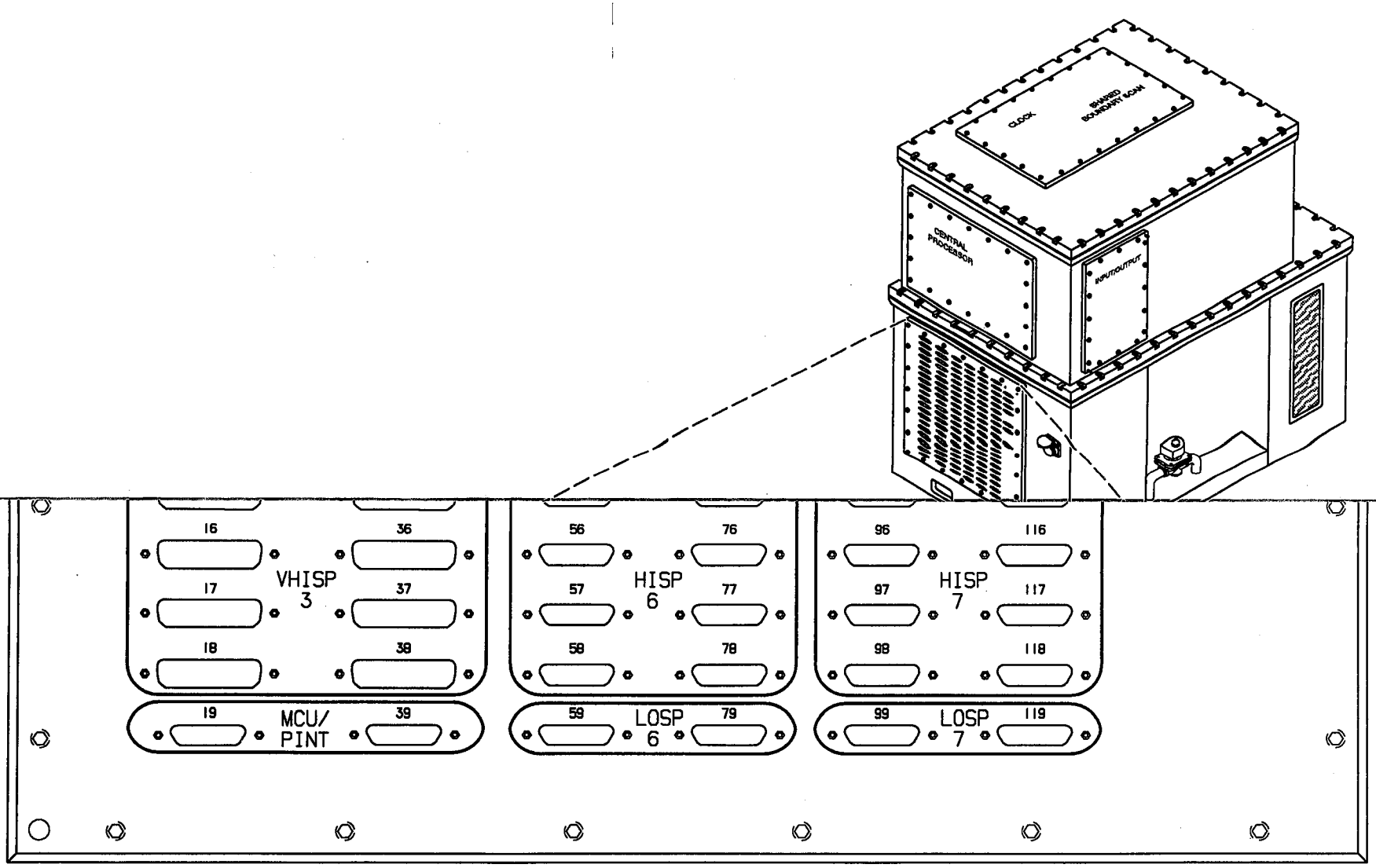

Figure 17. CRAY T94 Mainframe Bulkhead Map *(Panel Silkscreening may change)*

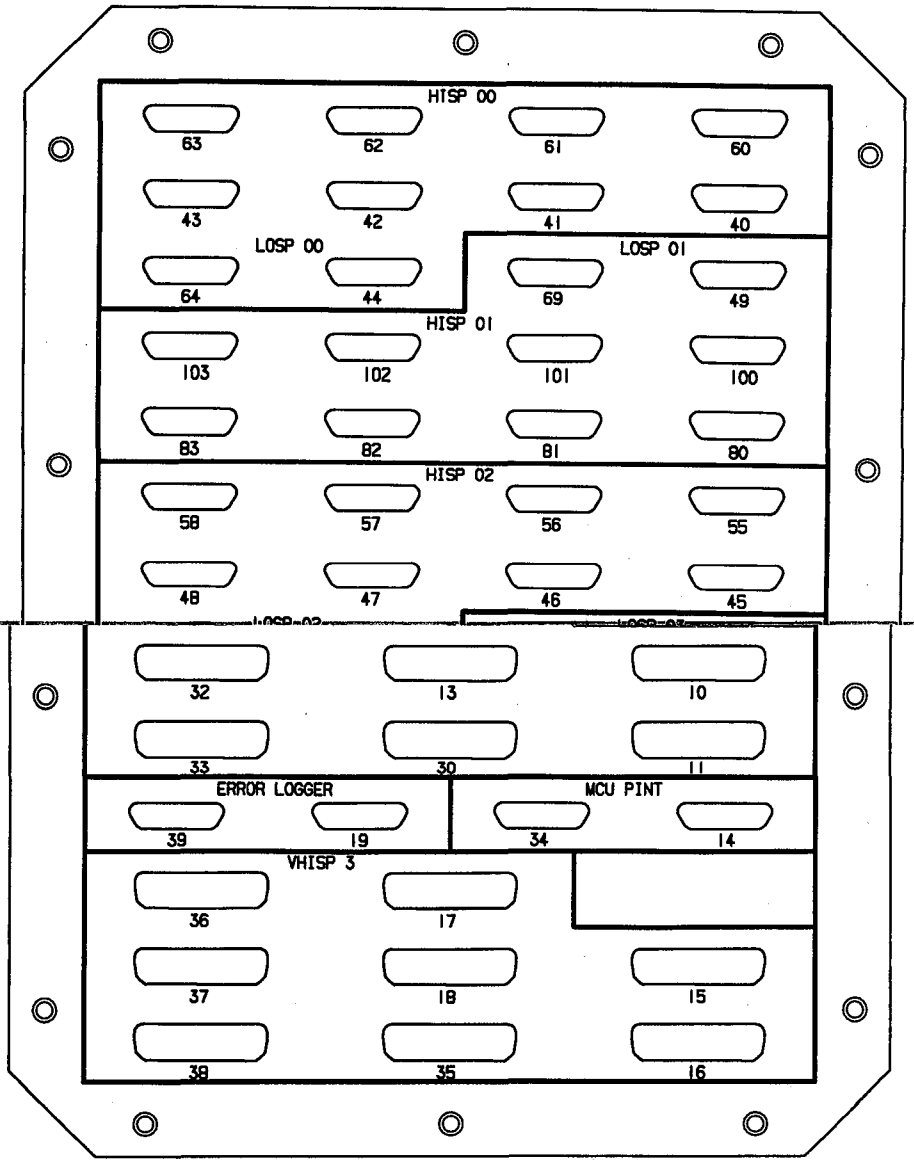

Figure 18. CRAY T916 and CRAY T932 Mainframe Bulkhead Map *(Panel Silkscreening is incorrect and will be changed)*

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