LME User Guide

(CRAY T90™ Series)

HDM-070-A

Cray Research/Silicon Graphics Proprietary

Record of Revision

REVISION	DESCRIPTION
	August 1995. Original printing.
A	August 1997. This revision corresponds to the MT-T2.3.0 offline diagnostic release. This revision supports IO02 modules. It also adds an Appendix that contains descriptions of the test points.

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LME USER GUIDE

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Description of this Document

This document is a user guide for the Logic Monitor Environment (LME) application that is used to control the logic monitor hardware in CRAY T90™ series mainframes.

This document is one component of the LME documentation set, which also includes the following document:

LME Interface Reference, publication number HDM-122-A.

The *LME Interface Reference* describes the LME user interface. It describes the LME base window and all available menu button commands.

Overview

The Logic Monitor Environment (LME) is an X Window System™ based application that enables you to monitor the activity of test points on the CP, SR, IO, and NW modules. LME captures test-point and control data from the logic monitors of the modules that you are monitoring. You can use this data to determine the operation state of the modules. You can also use LME to monitor the P register and current instruction parcel for any CPU.

To control the logic monitor for a module, you use LME to assign a set of parameters, called a parameter set, to the module. A parameter set contains all the information needed to select the type of data that is recorded, the mode used to record the data, the trigger conditions used to stop recording, any test points that are being directed to scope points for access by an external probe, and any breakpoints that are set for the CPUs.

You can use LME to record the following data:

- Test-point data, P register data, and current instruction parcel data for the CP modules
- Test-point data for the SR and IO modules
- Test-point data for the NW modules (LME routes the NW test-point data to the appropriate CP module, and the logic monitor on the CP module records the data.)

LME loads the recorded data into buffers in MWS or SWS memory. Once this data is recorded, you can use LME to view it or save it for later analysis. LME does not include functionality for analyzing the results; you must be able to recognize whether the results indicate an error. You can also use LME to set up breakpoint control for CPUs.

NOTE: The Command Buffer Parser (CBP) application provides commands that you can use to automate the test-point dump process in LME. You can also use CBP commands to analyze test-point dump data. For more information about these CBP commands, refer to the *CBP Runtime Module* document, publication number HDM-071-A.

The following procedure gives a general overview of the process for using LME. This document provides related information for each step of the process.

1. Start LME.
2. Load a window layout (optional).
3. Load a system snapshot (optional).
4. Create the parameter sets.
5. Create the expected data (optional).
6. Assign parameter sets to the modules.
7. Click on Go.
8. Click on Halt (optional).
9. View the results.

For more information about the logic monitor hardware, how it works, and the concepts related to recording with the logic monitors; refer to the *Maintenance Channel* document, publication number HTM-006-B, and the *Triton Maintenance System Engineering Note*, publication number PRN-0957.

Start LME

You can start LME from a UNIX® command prompt, from the OpenWindows™ Workspace menu, or from any environment of the Mainframe Maintenance Environment (MME) application.

NOTE: For information about starting LME from a service center through a hub, refer to the *Remote Support* document, publication number HMM-106-A.

From a UNIX Prompt

To start LME from a UNIX command prompt, enter one of the following commands:

- **`lme`** to use a mainframe front-end interface (FEI) channel
- **`lme -sim`** to use the simulator

NOTE: You may also enter any of the command line options that Table 1 lists.

Table 1. Command Line Options

Option	Description
`-client`	Start the LME client only
`-config` *file*	Configure LME with the configuration data stored in the file specified by *file* LME does not use this option if SCE is running when you start LME.
`-copy` *num*	Connect to maintenance software assigned the copy number specified by *num* **NOTE:** Copy numbers are necessary only when you run multiple copies of LME on the same MWS or SWS (for example, when you run several LME copies with the simulator or when you use LME to support multiple CRAY T90 series mainframes connected to the same MWS or SWS).
`-kill`	Kill any running MME, SCE, or LME applications before starting a new copy of LME
`-l` *file*	Load the window layout stored in the file specified by *file*
`-remote` *host*	Start the LME client only and connect the client to the LME server that is running on the remote host specified by *host*
`-server`	Start the LME server only

You can also use the `lmedump` command from the UNIX prompt. The `lmedump` command performs an automated test-point dump. The `lmedump` command has no command line options.

From the OpenWindows Workspace Menu

You can start LME from the OpenWindows Workspace menu on either an MWS or an SWS.

MWS Workspace Menu Options

Figure 1 shows the OpenWindows Workspace menu options that you should choose on an MWS to start LME with an FEI channel. Choose any copy number.

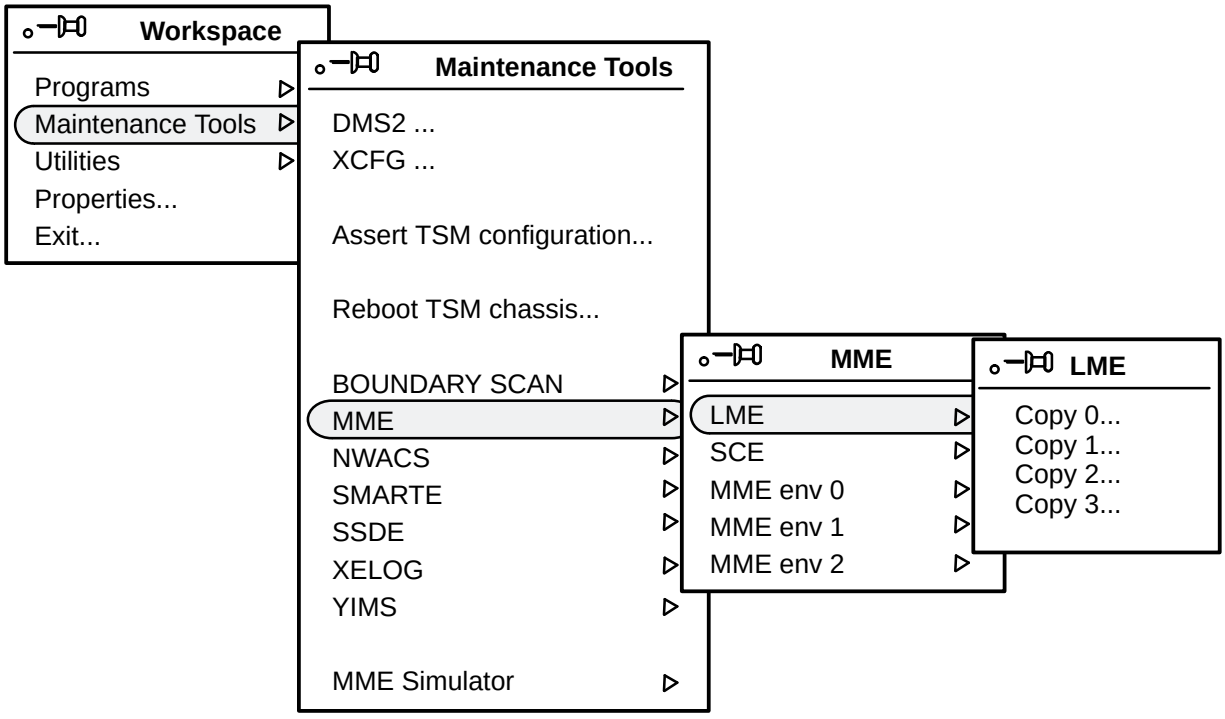


Figure 1. MWS Workspace Menu Options to Start LME with an FEI Channel

Figure 2 shows the OpenWindows Workspace menu options that you should choose on an MWS to start LME with the simulator.

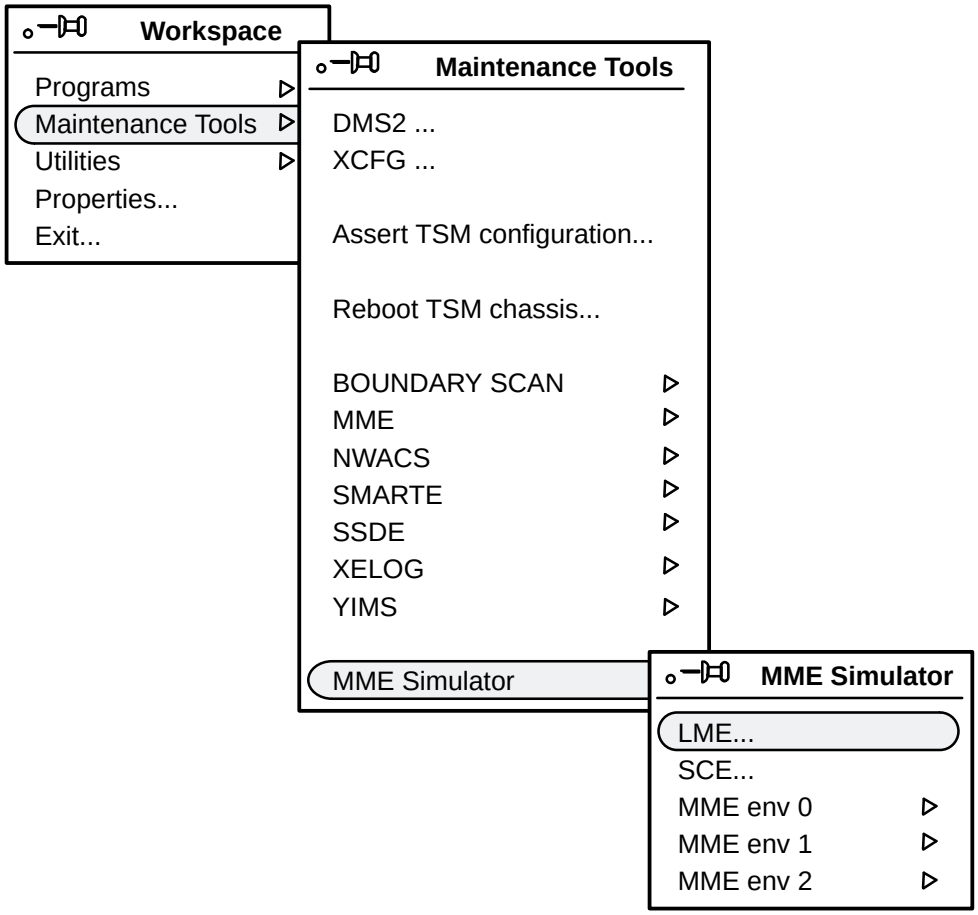


Figure 2. MWS Workspace Menu Options to Start LME with the Simulator

SWS Workspace Menu Options

Figure 3 shows the OpenWindows Workspace menu options that you should choose on an SWS to start LME with an FEI channel. Choose any copy number.

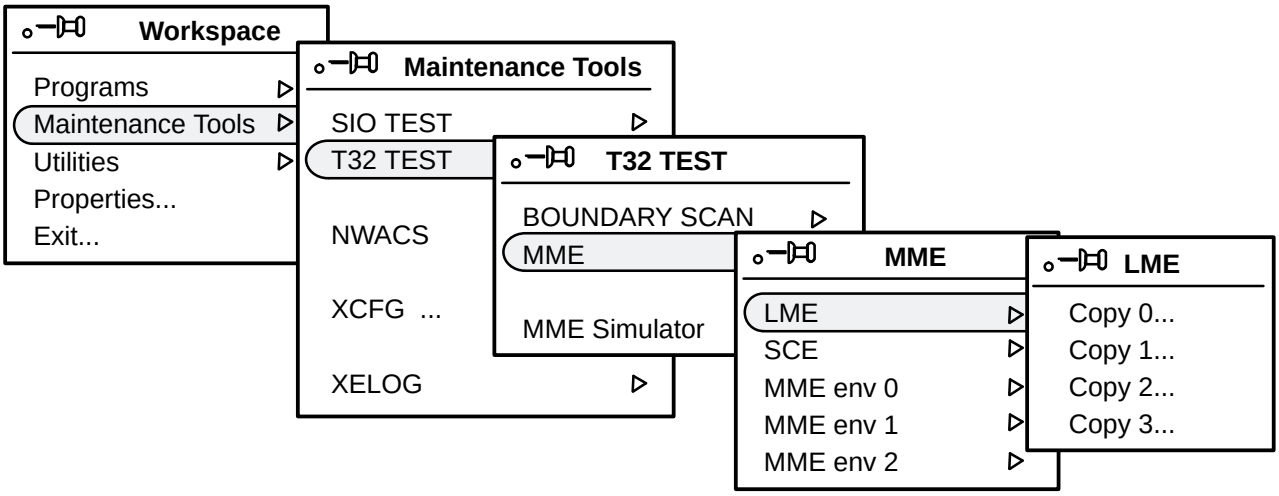


Figure 3. SWS Workspace Menu Options to Start LME with an FEI Channel

Figure 4 shows the OpenWindows Workspace menu options that you should choose on an SWS to start LME with the simulator.

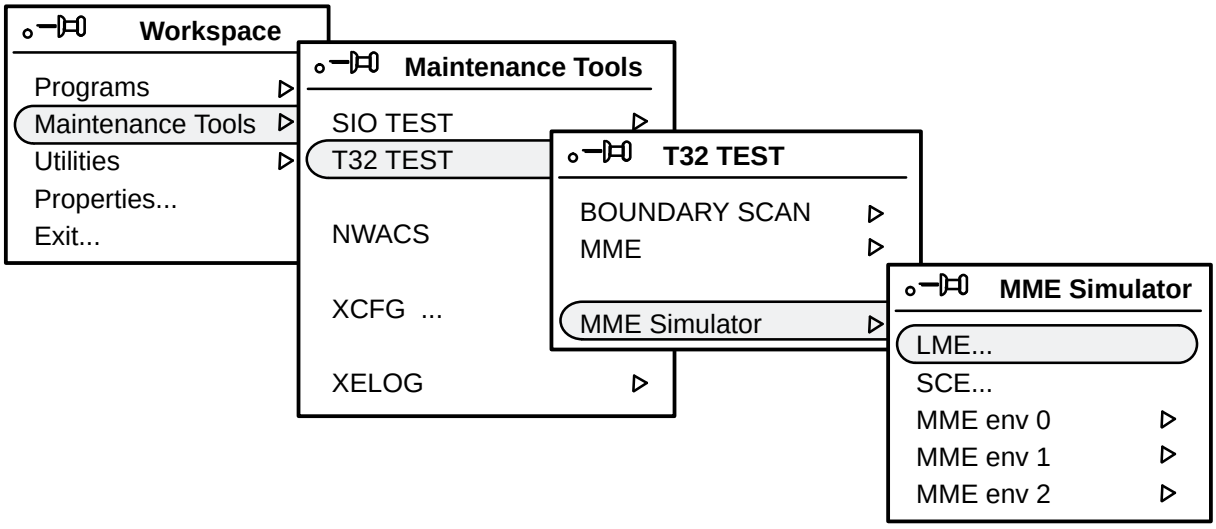


Figure 4. SWS Workspace Menu Options to Start LME with the Simulator

From MME

Choose **Utilities –> Logic Monitor** from the MME base window to start LME from MME.

What Happens When You Start LME?

The following actions occur when you start LME:

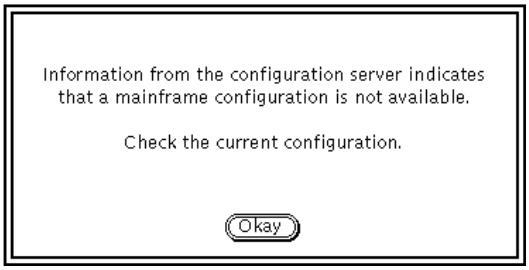
1. The LME server attempts to connect with the System Configuration Environment (SCE) server.

   If LME cannot connect with a running SCE server, LME starts a new SCE server and tries to connect to the new SCE server. (If you specified a configuration file with the `-config` command line option, LME sends this file to SCE through the SCE `-default` command line option. SCE loads the configuration stored in the file.)

2. Once LME establishes a connection with SCE, LME attempts to receive a configuration from SCE:

   - If a configuration is available, SCE provides LME with the components available for use by the maintenance system. LME automatically configures itself to use these components.

   - If a configuration is not available, LME displays the message shown in the following snap:



   When this happens, you need to create a configuration using SCE before you continue using LME. Refer to the *SCE User Guide*, publication number HDM-069-C, for more information about creating a configuration.

Load a Window Layout (Optional)

The File –> Save –> Layout command can save the window layout that you are using. This enables you to have a consistent window layout on the screen each time you use LME. To use a layout again, choose **File –> Load –> Layout** to load the layout.

Refer to the "File –> Save –> Layout" and "File –> Load –> Layout" descriptions in the *LME Interface Reference* document, publication number HDM-122-A, for more information about these commands.

Figure 5 shows an example layout that includes the LME base window, LME: Edit Parameters window, and LME: Test Point Dump/Display window.

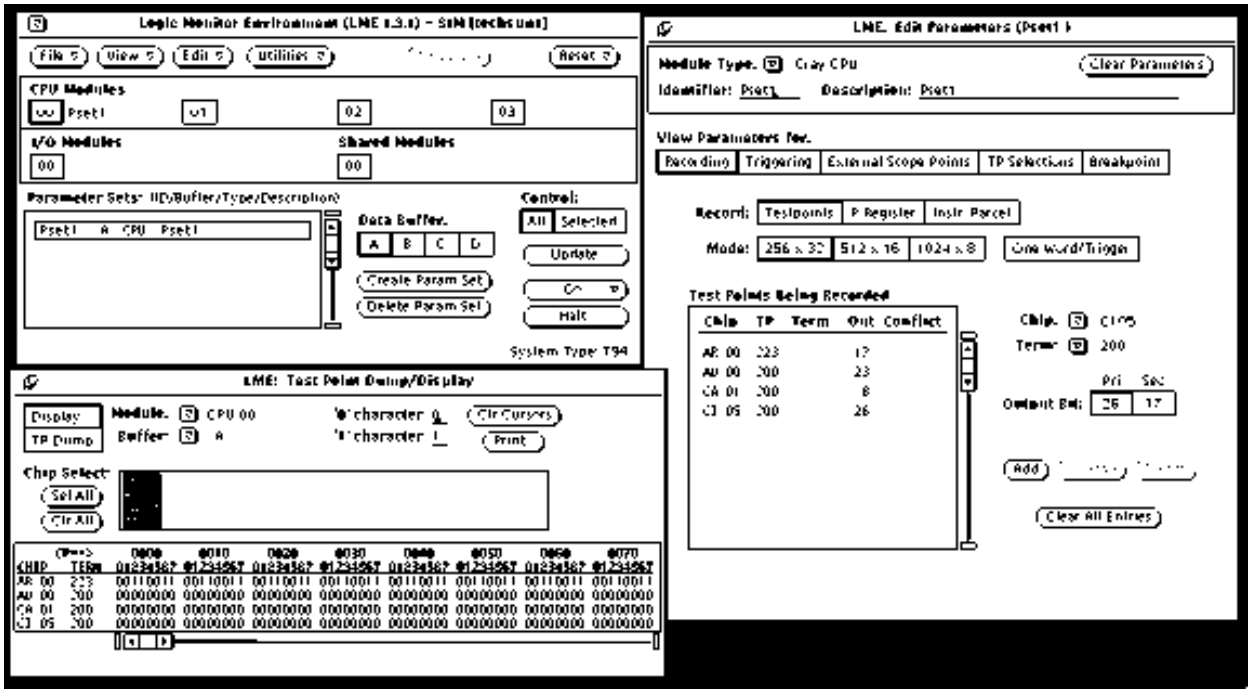


Figure 5. Example Layout

NOTE: You can also load a window layout with the `-l` command line option when you start LME from a UNIX prompt. For more information about the `-l` command line option, refer to Table 1 on page 7.

Load a System Snapshot (Optional)

You can use the File –> Save –> System Snapshot command to save a snapshot of the data from all windows you are using. This enables you to capture all data you are using. Choose **File –> Load –> System Snapshot** to load a system snapshot so you can use it again.

Refer to the "File –> Save –> System Snapshot" and "File –> Load –> System Snapshot" descriptions in the *LME Interface Reference* document, publication number HDM-122-A, for more information about these commands.

NOTE: If you load a layout and a system snapshot, LME returns to the same status that existed when you saved the layout and system snapshot.

Create the Parameter Sets

To set up the parameters for a module, create a parameter set that defines the type of data to record and the conditions for recording the data. To create a parameter set, click on (Create Param Set). This creates a new parameter set in the Parameter Sets scroll box, as shown in Figure 6.

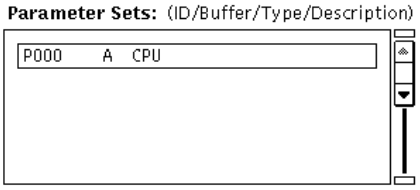


Figure 6. New Parameter Set in the Parameter Sets Scroll Box

Double click on the parameter set in the Parameter Sets scroll box, and the LME: Edit Parameters window for the parameter set appears. Use the LME: Edit Parameters window, shown in Figure 7, to edit the parameter set.

NOTE: You can also use the View –> Parameter Set command to create a new parameter set or to view an existing parameter set.

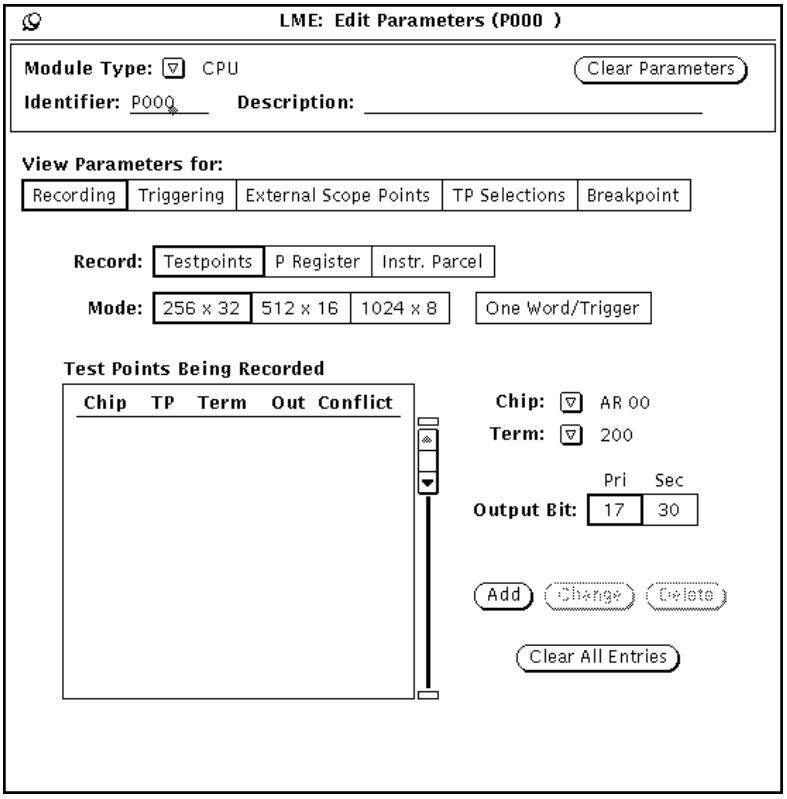


Figure 7. Edit Parameters Window

The following paragraphs describe the parameters in the order in which they appear in the View Parameters for: settings in the LME: Edit Parameters window. You will not need to use all of these parameters for every monitoring session; however, it is helpful to understand all parameters that are available.

Set the Module Type

Use the Module Type: menu to specify the type of module for which you want to create a parameter set. Table 2 shows the options that are available, depending on the mainframe configuration. The LME: Edit Parameters window displays the appropriate parameters for the type of module you select.

Table 2. Available Module Types

Option	Description
CPU † or Cray CPU †	These options specify that you want to create a parameter set for a CP module that uses the Cray Research, Inc. (CRI) floating-point number format. **NOTE:** The CPU and Cray CPU options perform the same function. The option name changes to Cray CPU only when CP modules that use the CRI floating-point number format and CP modules that use the IEEE floating-point format are present in the mainframe.
IEEE CPU †	This option specifies that you want to create a parameter set for a CP module that uses the IEEE floating-point number format. This option is available only when your configuration contains at least one CP module that uses the IEEE floating-point number format.
Shared	This option specifies that you want to create a parameter set for an SR module.
I/O	This option specifies that you want to create a parameter set for an IO01 module.
I/O Rev. 2	This option specifies that you want to create a parameter set for an IO02 module.
Network	This option specifies that you want to create a parameter set for an NW module. This option is available only for CRAY T916™ and CRAY T932™ mainframes; it is not available for CRAY T94™ mainframes because CRAY T94 mainframes do not include NW modules.
(Raw Params)	This option specifies that you want to enter parameters as interpreted octal values (raw parameters). For more information about using the raw parameters, refer to page 30 in this document.

† SCE provides LME with information about the CPU types that are configured for the mainframe. This information comes from the CPU Type parameter in SCE. Choose the **View –> CPU** command in the SCE base window to access this parameter. Refer to the *SCE Interface Reference*, publication number HDM-182-C, for more information.

Define the Identification and Description Information

By default, LME labels parameter sets with P###, where ### increases by one for each new parameter set you create. To change this label, enter a new label in the Identifier field. The label can be any combination of letters or numbers (up to 6 characters). You can provide a more detailed description of the parameter set in the Description field.

Set the Parameters

The parameters for CP, SR, and IO modules are grouped together in the following subsections because you access them through the same View Parameters for: settings.

The parameters for NW modules are available only for CRAY T916 and CRAY T932 mainframes. The "Parameters for NW Modules (CRAY T916 and CRAY T932 Mainframes Only)" subsection on page 27 describes these parameters.

Parameters for CP, SR, and IO Modules

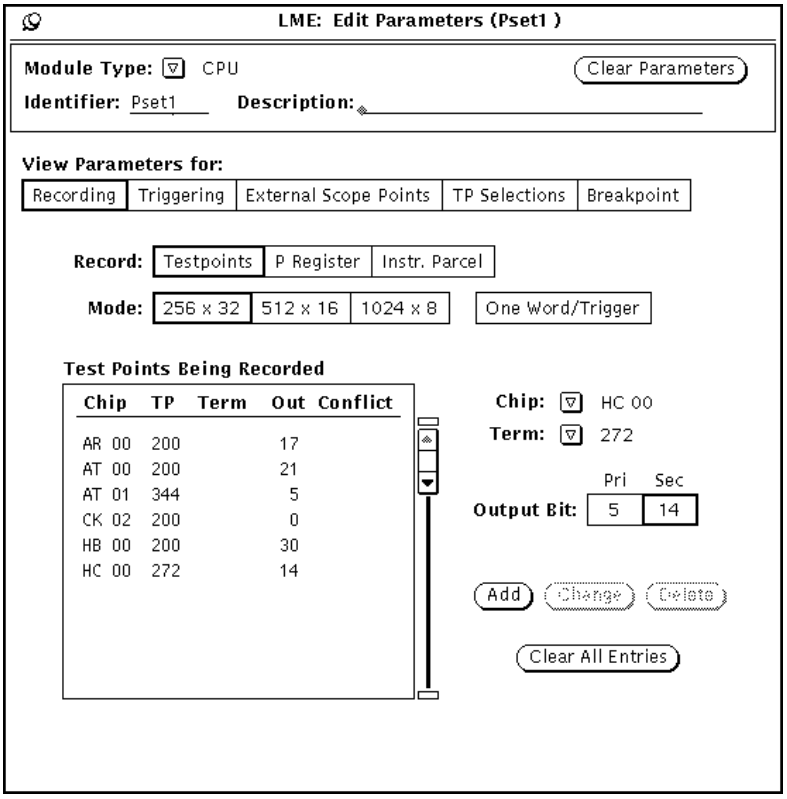
You can use the View Parameters for: settings to set the following parameters for CP, SR, and IO modules:

- Recording parameters
- Triggering parameters
- External scope point parameters
- Test-point selection parameters (with descriptions of the test points)
- Breakpoint parameters (for CP modules only)

Set the Recording Parameters

The recording parameters contain all the data needed to specify what LME will have the logic monitor(s) record. Using LME, you can record test-point data for any CP, SR, or IO module; P register data for any CPU; or current instruction parcel data for any CPU. Perform the following procedure to set the recording parameters:

1. Click on View Parameters for: Recording. The LME: Edit Parameters window displays the recording parameters.



2. Specify the type of data you want to record:

   - If you chose CPU, Cray CPU, or IEEE CPU from the Module Type: ▽, click on Record: Testpoints to record test-point data, on Record: P Register to record the contents of the P register, or on Record: Instr. Parcel to record the current instruction parcel.

     If you are recording the contents of the P register or the current instruction parcel, you do not need to set any other parameters. If you are recording test points, continue with Step 3 to finish setting the required parameters.

   - If you chose Shared, I/O, or I/O Rev. 2 from the Module Type: ▽, you can record only test points, so the Record settings appear gray. Continue with Step 3 to finish setting the required parameters.

3. Specify the recording mode that you want to use to record the test points. Click on Mode: [256 x 32] to record up to 32 test points for 256 clock periods. Click on Mode: [512 x 16] to record up to 16 test points for 512 clock periods. Click on Mode: [1024 x 8] to record up to 8 test points for 1,024 clock periods.

   By default, the logic monitors record the selected data every clock period. If you want the logic monitors to record data only during clock periods when a trigger occurs, click on [One word/Trigger].

4. From the Chip: [▽], choose the chip on which the test point you want to record is located.

5. From the Term: [▽], choose the test point you want to record. You can choose only one test point from each chip. If you choose a different test point for a chip, LME changes the test-point value for the chip everywhere the test point is referenced in the parameter set.

6. Click on (Add) to add the test point to the list of test points the logic monitor should record. The test point appears in the Test Points Being Recorded scroll box.

   NOTE: If you want to see a list of the available test points on a chip and descriptions of the test points, click on View Parameters for: [TP Selections]. Refer to "Select Test Points by Description" on page 25 of this document for more information.

   Use the Output Bit settings to resolve any conflicts that occur between selected test points. Conflicts occur when two or more test points use the same output bit. LME indicates conflicts by placing the same number for each test point in the Conflict column of the Test Points Being Recorded scroll box, as shown in Figure 8. The hardware combines any conflicting data bits with an OR function, so you should resolve any conflicts that occur.

   To resolve a conflict, select the secondary output bit (indicated by the Sec value) for all but one of the conflicting test points and click on (Change).

   NOTE: The secondary bits that you select could conflict with other chosen output bits. You should check for new conflicts and resolve any that occur.

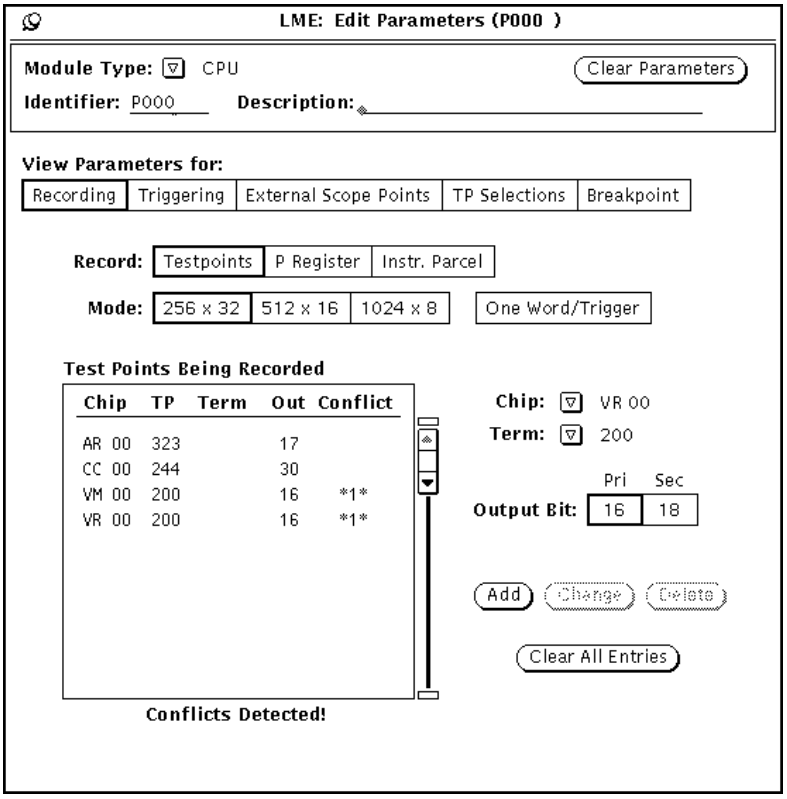


Figure 8. Output Bit Conflict

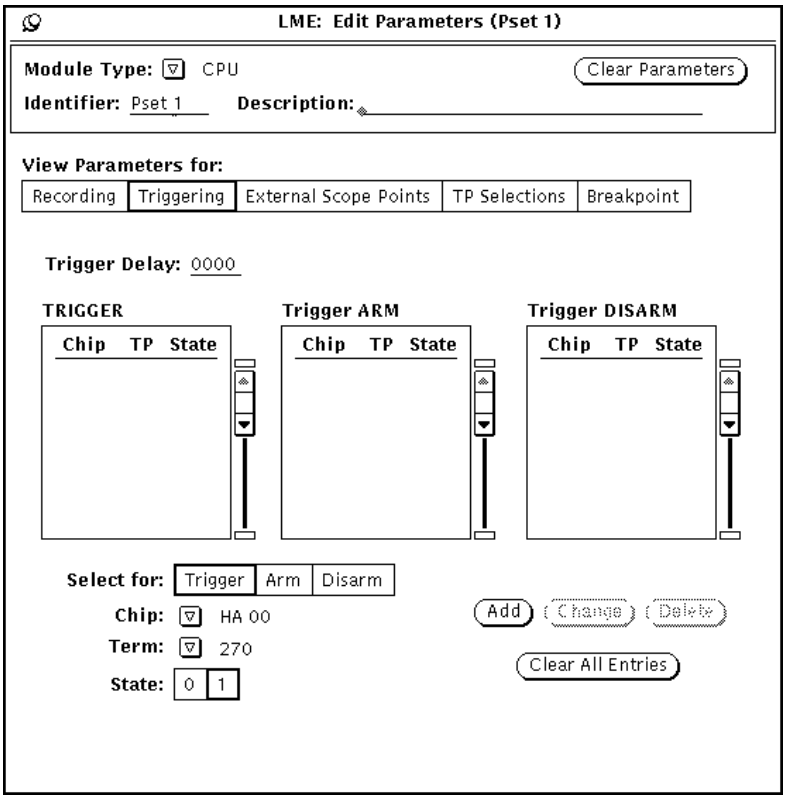
7. Repeat Steps 4 through 6 to select all the test points that you want to record.

You can click on the Change button to change the selected test-point entry. You can click on the Delete button to delete the selected entry. You can click on the Clear All Entries button to delete all entries.

NOTE: If you do not know the test-point number for the test point you want to monitor, you can choose the test point by description. Refer to “Select Test Points by Description” on page 25 of this document.

Set the Triggering Parameters

The triggering parameters specify when the logic monitor(s) should stop recording the selected data. Click on View Parameters for: Triggering to access the triggering parameters. The LME: Edit Parameters window changes to:



The Trigger Delay field specifies how many clock periods the logic monitor should continue recording after a trigger occurs. This enables you to capture additional information after a trigger occurs so that you can see what occurred before and after the trigger condition.

The trigger specifies the condition that causes the logic monitor to stop recording test points. Trigger arm conditions specify an event that must occur before a trigger is recognized and the logic monitor stops recording. The trigger disarm condition specifies an event that cancels the trigger arm condition. The following subsections describe how to create triggers, trigger arm conditions, and trigger disarm conditions.

Creating a Trigger

Perform the following procedure to create triggers. The trigger is a specific state (0 or 1) of a test point.

1. Click on Select for: [Trigger].
2. From the Chip: [▽], choose the chip on which the test point is located.
3. From the Term: [▽], choose the test point that you want to use as the trigger.
4. Click on State: [0] or [1] to specify the state of the test point.
5. Click on (Add) to add the trigger to the TRIGGER scroll box.
6. Repeat Steps 1 through 5 to create additional triggers.

You can click on the (Change) button to change the selected trigger entry. You can click on the (Delete) button to delete the selected entry. You can click on the (Clear All Entries) button to delete all entries.

Creating a Trigger Arm Condition

Perform the following procedure to create trigger arm conditions. The trigger arm condition is a specific state (0 or 1) of a test point.

1. Click on Select for: [Arm].
2. From the Chip: [▽], choose the chip on which the test point is located.
3. From the Term: [▽], choose the test point that you want to use as the trigger.
4. Click on State: [0] or [1] to specify the state of the test point.
5. Click on (Add) to add the trigger to the Trigger ARM scroll box.
6. Repeat Steps 1 through 5 to create additional trigger arm conditions.

You can click on the (Change) button to change the selected trigger arm entry. You can click on the (Delete) button to delete the selected entry. You can click on the (Clear All Entries) button to delete all entries.

Creating a Trigger Disarm Condition

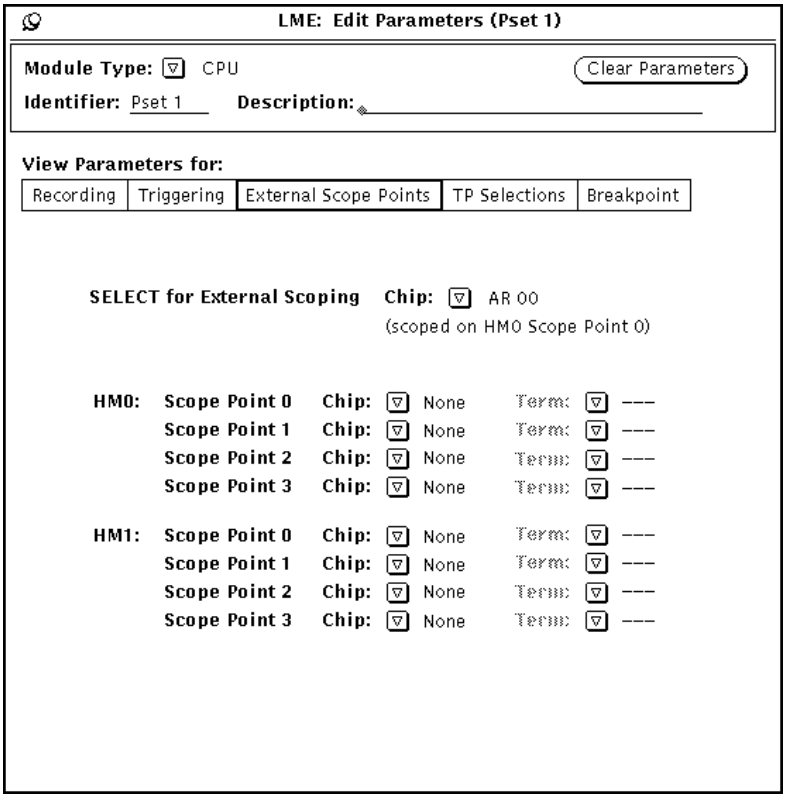
Perform the following procedure to create trigger disarm conditions. The trigger disarm condition is a specific state (0 or 1) of a test point.

1. Click on Select for: [Disarm].
2. From the Chip: [▽], choose the chip on which the test point is located.
3. From the Term: [▽], choose the test point that you want to use as the trigger.
4. Click on State: [0] or [1] to specify the state of the test point.
5. Click on (Add) to add the trigger to the Trigger DISARM scroll box.
6. Repeat Steps 1 through 5 to create additional trigger disarm conditions.

You can click on the (Change) button to change the selected trigger disarm entry. You can click on the (Delete) button to delete the selected entry. You can click on the (Clear All Entries) button to delete all entries.

Set Any External Scoping Points

LME can direct test-point data to the maintenance connector and then to external scope points that are connected to the bulkhead. This enables you to connect an external scope to view the test-point signals. There are eight scope points on each CP, SR, and IO module: four scope points on each HM option. Click on View Parameters for: External Scope Points. The LME: Edit Parameters window changes to:



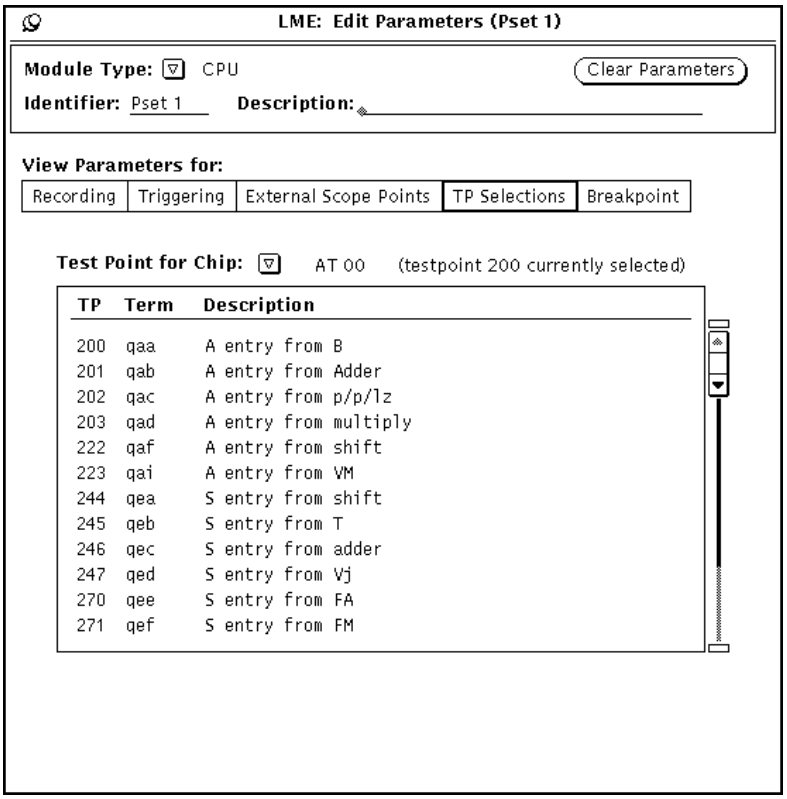
There are two ways to assign the chip and test point to the appropriate scope point:

- If you do not know the appropriate scope point for the chip that you want to scope: from the SELECT for External Scoping Chip:, choose the chip that has the test point. LME assigns the appropriate scope point to the chip. Then, choose the test point from the corresponding Term:. Click on Update to set up the external scope points.

- If you know the appropriate scope point: from the Chip: next to the scope point, choose the chip that has the test point. Then, choose the test point from the corresponding Term:. Click on Update to set up the external scope points.

Select Test Points by Description

If you do not know the number for the test point that you want to monitor, click on View Parameters for: TP Selections. LME displays the available test points on a chip and describes the test points. The LME: Edit Parameters window changes to:

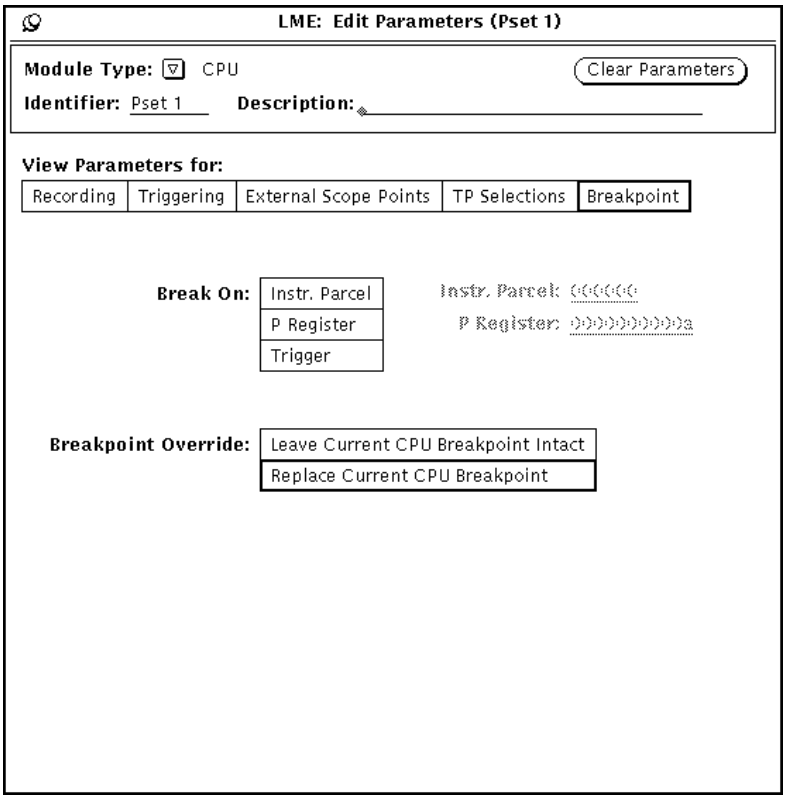


From the Test Point for Chip: , choose the chip for which you want to see the test points and descriptions. The descriptions and Boolean terms for the test points on the selected chip appear in the scroll box.

Click on the test point that you want to select. If you choose a test point on a chip you have already selected to record, LME updates the test-point selection in the Test Points Being Recorded scroll box on the View Parameters for: Recording, View Parameters for: Triggering, and View Parameters for: External Scope Points displays.

Set the CPU Breakpoint Conditions (CPU Parameter Sets Only)

Breakpoints automatically stop CPU execution on specific instruction parcel values, P register values, and triggers. Click on View Parameters for: Breakpoint to set up the breakpoint conditions. The LME: Edit Parameters window changes to:



Perform the following procedure to set the breakpoint parameters:

1. Click on Breakpoint Override: Leave Current CPU Breakpoint Intact to keep the current breakpoint. Click on Breakpoint Override: Replace Current CPU Breakpoint to replace the current breakpoint.

2. Specify the breakpoint condition that you want to use:

   - Click on Break On: Instr. Parcel to stop CPU execution on a specific instruction parcel value; enter the value in the Instr. Parcel field.

   - Click on Break On: P Register to stop CPU execution on a specific P register value; enter the value in the P Register field.

- Click on Break On: [Trigger] to stop CPU execution on a specific trigger; click on View Parameters for: [Triggering] to access the trigger parameters. Refer to "Set the Triggering Parameters" on page 21 of this document for more information about setting the trigger.

LME begins monitoring the breakpoint condition when you click on [Go]. LME displays a hollow stop sign icon (○) next to a CPU to indicate that a breakpoint is set for the CPU. This icon changes to a filled stop sign icon (STOP) when the breakpoint condition occurs.

NOTE: The breakpoint icons disappear when a CPU master clear occurs because a CPU master clear function clears all breakpoints. For example, halting a diagnostic in MME causes a master clear that clears all breakpoints.

Parameters for NW Modules (CRAY T916 and CRAY T932 Mainframes Only)

You can also use LME to monitor the test points on the NW modules in CRAY T916 and CRAY T932 mainframes. (LME routes the NW test-point data through the network ports to the appropriate CP module; then, the logic monitor on the CP module records the data. LME does this because there are no logic monitors on the NW modules.)

To access the parameters for NW modules, choose Network from the Module Type: [▽] in the LME: Edit Parameters window.

You can use the View Parameters for: settings to set the following parameters for NW modules:

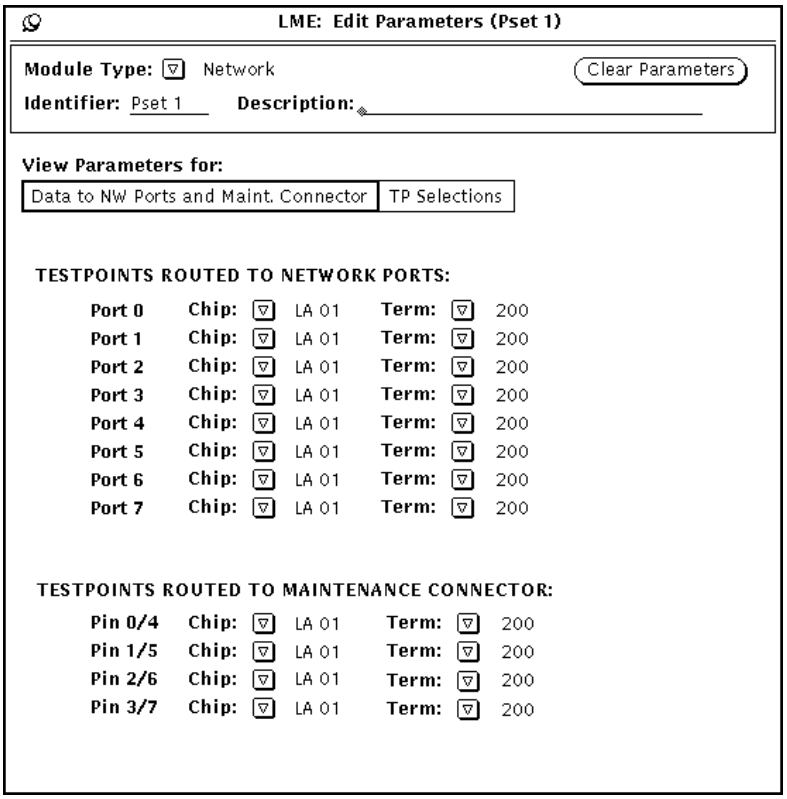
- Test-point routing parameters (route to network ports so the logic monitor on a CP module can record the test points or to the maintenance connector so you can view the test points on an external scope)

- Test-point selection parameters (with descriptions of the test points)

Set the NW Module Test-point Routing Parameters

LME can route NW module test-point data to the network ports, which then send the test points to a CP module. The logic monitor on the CP module can record the test points.

LME can also route NW module test-point data to the maintenance connector and then to external scope points that are connected to the bulkhead. Click on View Parameters for: [Data to NW Ports and Maint. Connector]. The LME: Edit Parameters window changes to:

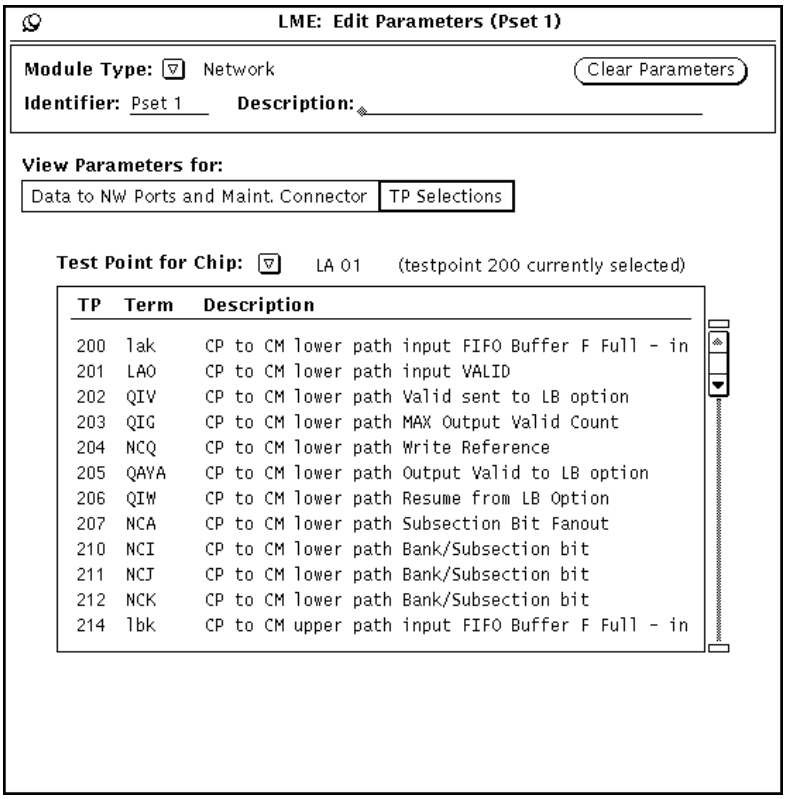


Use the TESTPOINTS ROUTED TO NETWORK PORTS parameters to specify which NW module test points you want to monitor. Because NW modules cannot record test-point data, the test-point data that you select returns to the CP modules through the specified network ports. To access the test-point data sent from an NW module, the logic monitors record test point 0215 for the CJ chips on the CP modules. (The CJ chip that captures the data depends on which side of the NW module contains the test point you want to record.)

Use the TESTPOINTS ROUTED TO MAINTENANCE CONNECTOR parameters to specify which test points you want to route to the maintenance connector. From the maintenance connector, the specified test-point data goes to the external scope points that are connected to the bulkhead. This enables you to connect an external scope to view the test-point signals. Pins 0, 1, 2, and 3 on the maintenance connector return data from the half of a network module that is connected to an even section of memory. Pins 4, 5, 6, and 7 on the maintenance connector return data from the half of a network module that is connected to an odd section of memory

Select NW Module Test Points by Description

If you do not know the number for the NW module test point that you want to monitor, click on View Parameters for: TP Selection. LME displays the available test points on a chip and describes the test points. The LME: Edit Parameters window changes to:



From the Test Point for Chip: , choose the chip for which you want to see the test points and descriptions. The descriptions and Boolean terms for the test points on the selected chip appear in the scroll box.

Click on the test point that you want to select. If you choose a test point on a chip that you have already selected to record, LME updates the test-point selection in the Test Points Being Recorded scroll box on the View Parameters for: [Data to RW Ports and Maint Connector] display.

Using the Raw Parameters

Figure 9 shows the parameter set as *raw parameters*. To view the raw parameters, choose **(Raw Params)** from the Module Type: [▽]. For information about these parameters, refer to the *Triton Maintenance System Engineering Note*, publication number PRN-0957.

If you do not have a thorough understanding of these parameters, use the parameter window shown in Figure 7 on page 15 because that window provides the easiest way to set parameters.

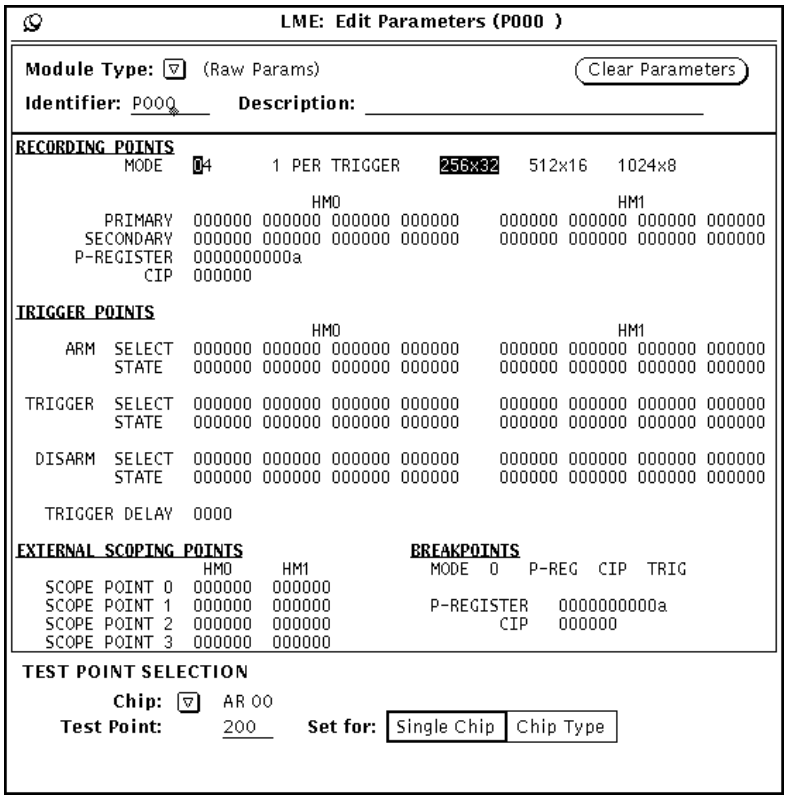


Figure 9. Edit Parameters Window (Raw Format)

NOTE: You must press the Return key after you edit a data value in the LME: Edit Parameters window shown in Figure 9. This causes LME to read the new data values.

Create the Expected Data (Optional)

LME includes one expected data buffer for each parameter set. You can use the expected data buffers to compare the results of a monitoring session to a set of data.

The easiest way to create a set of expected data is to copy the results from a monitoring session of modules that are operating correctly. To do this, use the Module button after the monitoring session has completed. The Module button activates when you click on a parameter set that is displayed next to a CPU. Choose **Module –> Copy Current Buffer to Expected**. This copies the results of the last monitoring session into the expected data buffer for the parameter set.

You can also manually enter a set of expected data. Choose **View –> Expected Data** to access the LME: Exp. Data window for the current parameter set. Figure 10 shows the window that appears. Note that LME formats the window to correspond with the recording mode of the parameter set. Enter the data in this window.

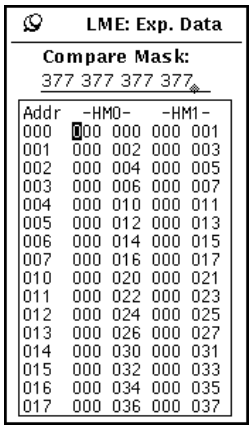


Figure 10. Expected Data Window

Assign Parameter Sets to the Modules

After you have created the parameter sets, you need to assign them to the appropriate modules. In the Parameter Sets scroll box, click on the parameter set you want to use. Then, click on the Data Buffer setting that you want to use to indicate which buffer should receive the data. Finally, click on the module to which you want to assign the parameter set.

NOTE: You may assign a parameter set to more than one module.

Click on Go

In the LME base window, click on Go to start recording data. Two commands are available from the Go button: Go –> One-shot and Go –> Continuous. Refer to the "Controls" subsection of the *LME Interface Reference*, publication number HDM-122-A, for detailed descriptions of these commands.

The logic monitors record data until a corresponding trigger occurs or until you click on Halt.

There are four data buffers (labeled A, B, C, and D) in MWS or SWS memory for each module. When LME receives logic monitor data for a module, LME places the data in the data buffer that you selected with the Data Buffer setting in the LME base window; this buffer is called the *current* buffer for the module.

NOTE: For each module, LME receives the entire contents of the logic monitor data buffer at one time. This buffer contains the last 256, 512, or 1,024 words recorded by the logic monitor, depending on the recording mode.

Click on Halt (Optional)

If you have trigger conditions set, recording will stop when the trigger conditions occur. However, you will need to click on Halt to cause the logic monitors to stop recording data under the following circumstances:

- If you want the logic monitors to stop recording before the logic monitors reach the trigger conditions
- If you did not set any trigger conditions
- If you used the Go –> Continuous option to start the monitoring session
- If you are using the one word per trigger (One word/Trigger) option

View the Results

Once the selected data is recorded, you should view the results to determine the current status of the modules. LME can display the following data:

- The logic monitor data recorded for the module(s)
- The test-point data recorded by the logic monitor
- A comparison of actual logic monitor data with the expected data

Viewing the Logic Monitor Data for a Module

Choose **View –> Module LM Data** to view the logic monitor data that is returned from a module's logic monitor. Refer to the "View –> Module LM Data" description in the *LME Interface Reference* document, publication number HDM-122-A, for more information about this command.

NOTE: You can also double click on the parameter set name (displayed next to the module) in the module area of the LME base window to view the logic monitor data.

Viewing the Test-point Data Recorded by a Logic Monitor

Choose **View –> Test Point Data** to access a window that contains the test-point data. Refer to the "View –> Test Point Data" description in the *LME Interface Reference* document, publication number HDM-122-A, for more information about this command.

Comparing the Returned Logic Monitor Data to Another Set of Data

Choose **Utilities –> Data Compare** to access a window that enables you to compare logic monitor data. Refer to the "Utilities –> Data Compare" description in the *LME Interface Reference* document, publication number HDM-122-A, for more information about this command.

APPENDIX: TEST-POINT DESCRIPTIONS

This Appendix describes the test points that are included on the following modules:

- CP02 module
- CPE1 module (refer to page 117)
- IO01 module (refer to page 153)
- IO02 module (refer to page 176)
- NW01 module (refer to page 202)
- SR01 module (refer to page 212)

CPU Module (CP02) Test Points

This section lists the test points that are built into the options on the CP02 CPU module. A brief description of each option is also included.

NOTE: The following CP02 CPU module options do not have test points: AM, AN, CD, CH, CK, FA, FB, HM, NA, NB, NC, ND, OA, RA, RB, RC, and VS.

AR Option (Revision 1026)

Test Point	Term	Description
200	qaa	A entry from B
201	qab	A entry from adder
202	qac	A entry from population/parity/leading zero
203	qad	A entry from multiply
204	–	–
205	–	–
206	–	–
207	–	–
210	–	–
211	–	–
212	–	–
213	–	–
214	–	–
215	–	–

216	–	–
217	–	–
220	–	–
221	–	–
222	qaf	A entry from shift
223	qai	A entry from VM
224	–	–
225	–	–
226	–	–
227	–	–
230	–	–
231	–	–
232	–	–
233	–	–
234	–	–
235	–	–
236	–	–
237	–	–
240	–	–
241	–	–
242	–	–
243	–	–
244	qea	S entry from shift
245	qeb	S entry from T
246	qec	S entry from adder
247	qed	S entry from V*j*
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–
255	–	–
256	–	–
257	–	–
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–

267	–	–
270	qee	S entry from FA
271	qef	S entry from FM
272	qeg	S entry from reciprocal
273	qeh	S entry from VM
274	–	–
275	–	–
276	–	–
277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–
311	–	–
312	–	–
313	–	–
314	qei	S entry from MM
315	–	–
316	–	–
317	–	–
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–
337	–	–

340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	xzz	Any test point active

AS Option (Revision 1021)

Test Point	Term	Description
200	qaa	A entry from B
201	qab	A entry from adder
202	qac	A entry from population/parity/leading zero
203	qad	A entry from multiply
204	–	–

205	–	–
206	–	–
207	–	–
210	–	–
211	–	–
212	–	–
213	–	–
214	–	–
215	–	–
216	–	–
217	–	–
220	–	–
221	–	–
222	qaf	A entry from shift
223	qai	A entry from VM
224	–	–
225	–	–
226	–	–
227	–	–
230	–	–
231	–	–
232	–	–
233	–	–
234	–	–
235	–	–
236	–	–
237	–	–
240	–	–
241	–	–
242	–	–
243	–	–
244	qea	S entry from shift
245	qeb	S entry from T
246	qec	S entry from adder
247	qed	S entry from V*j*
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–
255	–	–

256	–	–
257	–	–
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	qee	S entry from FA
271	qef	S entry from FM
272	qeg	S entry from reciprocal
273	qeh	S entry from VM
274	–	–
275	–	–
276	–	–
277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–
311	–	–
312	–	–
313	–	–
314	qei	S entry from MM
315	–	–
316	–	–
317	–	–
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–

327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–
337	–	–
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	xzz	Any test point active

AT Option (Revision 1021)

Test Point	Term	Description
200	qaa	A entry from B
201	qab	A entry from adder
202	qac	A entry from population/parity/leading zero
203	qad	A entry from multiply
204	–	–
205	–	–
206	–	–
207	–	–
210	–	–
211	–	–
212	–	–
213	–	–
214	–	–
215	–	–
216	–	–
217	–	–
220	–	–
221	–	–
222	qaf	A entry from shift
223	qai	A entry from VM
224	–	–
225	–	–
226	–	–
227	–	–
230	–	–
231	–	–
232	–	–
233	–	–
234	–	–
235	–	–
236	–	–
237	–	–
240	–	–
241	–	–
242	–	–
243	–	–
244	qea	S entry from shift
245	qeb	S entry from T

246	qec	S entry from adder
247	qed	S entry from V*j*
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–
255	–	–
256	–	–
257	–	–
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	qee	S entry from FA
271	qef	S entry from FM
272	qeg	S entry from reciprocal
273	qeh	S entry from VM
274	–	–
275	–	–
276	–	–
277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–
311	–	–
312	–	–
313	–	–
314	qei	S entry from MM
315	–	–
316	–	–

317	–	–
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–
337	–	–
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–

370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	xzz	Any test point active

AU Option (Revision 1021)

Test Point	Term	Description
200	qaa	A entry from B
201	qab	A entry from adder
202	qac	A entry from population/parity/leading zero
203	qad	A entry from multiply
204	–	–
205	–	–
206	–	–
207	–	–
210	–	–
211	–	–
212	–	–
213	–	–
214	–	–
215	–	–
216	–	–
217	–	–
220	–	–
221	–	–
222	qaf	A entry from shift
223	qai	A entry from VM
224	–	–
225	–	–
226	–	–
227	–	–
230	–	–
231	–	–
232	–	–
233	–	–
234	–	–

235	–	–
236	–	–
237	–	–
240	–	–
241	–	–
242	–	–
243	–	–
244	qea	S entry from shift
245	qeb	S entry from T
246	qec	S entry from adder
247	qed	S entry from V*j*
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–
255	–	–
256	–	–
257	–	–
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	qee	S entry from FA
271	qef	S entry from FM
272	qeg	S entry from reciprocal
273	qeh	S entry from VM
274	–	–
275	–	–
276	–	–
277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–

306	–	–
307	–	–
310	–	–
311	–	–
312	–	–
313	–	–
314	qei	S entry from MM
315	–	–
316	–	–
317	–	–
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–
337	–	–
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–

357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	xzz	Any test point active

BT Option (Revision 1034)

Test Point	Term	Description
200	qpa	Enter new P
201	qqc	Advance P
202	–	–
203	–	–
204	–	–
205	–	–
206	mgh	Parity error
207	–	–
210	–	–
211	–	–
212	–	–
213	–	–
214	–	–
215	–	–
216	–	–
217	–	–
220	–	–
221	–	–
222	qac	B read (005/024)
223	qbb	B write (025)

224	–	–
225	–	–
226	–	–
227	–	–
230	–	–
231	–	–
232	–	–
233	–	–
234	–	–
235	–	–
236	–	–
237	–	–
240	–	–
241	–	–
242	–	–
243	–	–
244	qbj	Return jump (007)
245	qcc	T read (074)
246	qdb	T write (075)
247	–	–
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–
255	–	–
256	–	–
257	–	–
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	qkc	Go 150 – 153
271	qlc	Go 160 – 167 or 170 – 173
272	qmc	Go 174*xxx*
273	–	–
274	–	–

275	–	–
276	–	–
277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–
311	–	–
312	–	–
313	–	–
314	qef	Block B read (034)
315	qff	Block B write (035)
316	qgf	Block T read (036)
317	qhf	Block T write (037)
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–
337	–	–
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–

346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	xzz	Any test point active

CA Option (Revision 5000)

Test Point	Term	Description
200	–	–
201	–	–
202	–	–
203	GGD	Rank E counted A’B’
204	ALY	Half mode
205	ALZ	Upper
206	CBN	Block count is not 0
207	–	–
210	–	–
211	CBJ	Valid out port AB
212	CBK	Valid out port A’B’

213	GGC	Rank E counted AB
214	ALT	Triton mode
215	CPG	Resume counter bit 0
216	CPH	Resume counter bit 1
217	CPI	Resume counter bit 2
220	CEA	Port AB increment bit 0
221	CEB	Port AB increment bit 1
222	CEC	Port AB increment bit 2
223	CED	Port AB increment bit 3
224	CEE	Port AB increment bit 4
225	CEF	Port AB increment bit 5
226	CEG	Port AB increment bit 6
227	CEH	Port AB increment bit 7
230	CKA	Port A’B’ increment bit 0
231	CKB	Port A’B’ increment bit 1
232	CKC	Port A’B’ increment bit 2
233	CKD	Port A’B’ increment bit 3
234	CKE	Port A’B’ increment bit 4
235	CKF	Port A’B’ increment bit 5
236	CKG	Port A’B’ increment bit 6
237	CKH	Port A’B’ increment bit 7
240	LQA	Port AB address bit 0
241	LQB	Port AB address bit 1
242	LQC	Port AB address bit 2
243	LQD	Port AB address bit 3
244	LQE	Port AB address bit 4
245	LQF	Port AB address bit 5
246	LQG	Port AB address bit 6
247	LQH	Port AB address bit 7
250	LSA	Port A’B’ address bit 0
251	LSB	Port A’B’ address bit 1
252	LSC	Port A’B’ address bit 2
253	LSD	Port A’B’ address bit 3
254	LSE	Port A’B’ address bit 4
255	LSF	Port A’B’ address bit 5
256	LSG	Port A’B’ address bit 6
257	LSH	Port A’B’ address bit 7
260	LRV	Valid count AB bit 0
261	LRW	Valid count AB bit 1
262	LTV	Valid count A’B bit 0
263	LTW	Valid count A’B’ bit 1

264	ABQ	Exchange control
265	ABR	Exchange control
266	ABS	Exchange control
267	ABT	Exchange control
270	CBA	Block count bit 0
271	CBB	Block count bit 1
272	CBC	Block count bit 2
273	CBD	Block count bit 3
274	CBE	Block count bit 4
275	CBF	Block count bit 5
276	CBG	Block count bit 6
277	ABU	Exchange control
300	CRA	AB valid out counter decrement bit 0
301	CRB	AB valid out counter decrement bit 1
302	CRC	AB valid out counter decrement bit 2
303	CRD	AB valid out counter decrement bit 3
304	CRE	AB valid out counter decrement bit 4
305	CRF	AB valid out counter decrement bit 5
306	CRG	AB valid out counter decrement bit 6
307	AGK	Double gather
310	CRI	A’B’ valid out counter decrement bit 0
311	CRJ	A’B’ valid out counter decrement bit 1
312	CRK	A’B’ valid out counter decrement bit 2
313	CRL	A’B’ valid out counter decrement bit 3
314	CRM	A’B’ valid out counter decrement bit 4
315	CRN	A’B’ valid out counter decrement bit 5
316	CRO	A’B’ valid out counter decrement bit 6
317	AQE	Hold
320	CAY	00200*k*
321	AFS	Go read V
322	AFT	Go read B/T
323	AFU	Go V*k* type
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–

335	–	–
336	–	–
337	–	–
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	–	–

CB Option (Revision 5001)

Test Point	Term	Description
200	dea	Go B + T + V V*k* –> A
201	dga	Enables –> A

202	dha	IC clear –> A
203	dia	Exchange vector V*k* –> B
204	dja	A*h* feed –> B
205	dka	Hold –> B
206	dma	Generates –> C
207	dna	IC BT vector clear –> C
210	doa	Hold –> Ah pass
211	cya	Rank 1 valid delay
212	cyi	Rank 1 enable pipe 2
213	cze	Hold rank 1
214	gya	Rank 2 valid delay
215	gyi	Rank 2 enable pipe 2
216	gza	Hold rank 2
217	kaa	LAT 1 hit
220	kab	LAT 2 hit
221	kac	LAT 3 hit
222	kad	LAT multiple hit
223	kva	Rank 3 valid delayed
224	kvi	Rank 3 enable pipe 2
225	sja	Dirty flag LAT 1
226	sjb	Mode cache LAT 1
227	sjc	Mode with LAT 1
230	sje	Exchange word number bit 0
231	sjf	Exchange word number bit 1
232	sjg	Exchange word number bit 2
233	sji	LAT 1 low valid
234	sjj	LAT 1 high valid
235	tja	Dirty flag LAT 2
236	tjb	Mode cache LAT 2
237	tjc	Mode with LAT 2
240	tje	Exchange word number bit 0
241	tjf	Exchange word number bit 1
242	tjg	Exchange word number bit 2
243	tji	LAT 2 low valid
244	tjj	LAT 2 high valid
245	uja	Dirty flag LAT 3
246	ujb	Mode cache LAT 3
247	ujc	Mode with LAT 3
250	uje	Exchange word number bit 0
251	ujf	Exchange word number bit 1
252	ujg	Exchange word number bit 2

253	uji	LAT 3 low valid
254	ujj	LAT 3 high valid
255	xdg	Go dump IC
256	xdh	Go B/T
257	xdj	Go V
260	xdk	Go V*k* type
261	xdl	Go VL
262	xhq	Bp base A*h* –> base
263	xhv	Bp limit A*h* –> limit
264	xjl	B/T data valid
265	xjm	B/T done
266	xnn	V*j* data valid
267	xno	Valid counter bit 0
270	xnp	Valid counter bit 1
271	xnq	Valid counter bit 2
272	xpx	Arm release port C / scatter done
273	xpy	Hold port C busy
274	YUA	Configure 4 sections
275	YUB	Configure 8 sections
276	YUC	Configure upper sections
277	YUP	Main checkbyte
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–
311	–	–
312	–	–
313	–	–
314	–	–
315	–	–
316	–	–
317	–	–
320	–	–
321	–	–
322	–	–
323	–	–

324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–
337	–	–
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
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361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–

375	–	–
376	–	–
377	–	–

CC Option (Revision 5001)

Test Point	Term	Description
200	aqa	Resume count bit 0
201	aqb	Resume count bit 1
202	aqc	Resume count bit 2
203	–	–
204	AIA	Exchange data word bit 0
205	AIB	Exchange data word bit 1
206	AIC	Exchange data word bit 2
207	AID	Exchange data word bit 3
210	AIE	Exchange data valid
211	aiw	A/S count = 17
212	aix	LAT count = 17
213	UBO	Exchange writes complete
214	akd	DS one buffer mode
215	AKF	Disable exchanges
216	NBJ	Destination code bit 0
217	NBK	Destination code bit 1
220	NBL	Destination code bit 2
221	NBM	Destination code bit 3
222	NBN	Destination code bit 4
223	NBR	Destination code bit 8
224	NBS	Destination code bit 9
225	NBT	Destination code bit 10
226	NBU	Destination code bit 11
227	NBV	Destination code bit 12
230	bba	Enter LAT A base/limit
231	bbf	Hold LAT A base/limit
232	bbk	Enter LAT A bias
233	bbo	Hold LAT A bias
234	bca	Enter LAT B base/limit
235	bcf	Hold LAT B base/limit
236	bck	Enter LAT B bias
237	bco	Hold LAT B bias
240	bda	Enter LAT C base/limit
241	bdf	Hold LAT C base/limit

242	bdk	Enter LAT C bias
243	bdo	Hold LAT C bias
244	aji	Half mode
245	ajj	Upper
246	AKO	Hold fetch request
247	AKU	DS fetch to address 0
250	ala	Go 32-word fetch phase 12
251	alb	Go single fetch phase 12
252	ALR	Fetch active + 1 phase
253	amy	Decrement fetch count
254	alm	Go 32-word fetch phase 16
255	aln	Go single fetch phase 16
256	alo	DS fetch
257	alp	DS fetch
260	amq	Fetch count bit 0
261	amr	Fetch count bit 1
262	ams	Fetch count bit 2
263	amt	Fetch count bit 3
264	amu	Fetch count bit 4
265	amv	Fetch count bit 5
266	amw	Fetch count bit 6
267	AMX	Fetch count not 0
270	faa	Fetch address bit 0
271	fab	Fetch address bit 1
272	fac	Fetch address bit 2
273	FBQ	Single fetch
274	fbl	No LAT compares
275	fbm	Multiple LAT compares
276	FBV	Fetch valid count bit 0
277	FBW	Fetch valid count bit 1
300	ANL	Increment exchange address
301	ANM	Active exchange requests phase 18
302	ANN	Exchange active to JA
303	ano	Exchange active to ICs
304	KFA	Disabled exchange phase 8
305	anx	Exchange read done to HD
306	any	Exchange write done to HD
307	ANZ	Gate exchange writes
310	aoo	Exchange count bit 0
311	aop	Exchange count bit 1
312	aoq	Exchange count bit 2

313	aor	Exchange count bit 3
314	aos	Exchange count bit 4
315	aot	Exchange count bit 5
316	AOV	Exchange count not 0
317	AOW	Decrement exchange count
320	ape	Exchange read count bit 0
321	apf	Exchange read count bit 1
322	apg	Exchange read count bit 2
323	aph	Exchange read count bit 3
324	ANG	Go exchange phase 14
325	kaa	Exchange address bit 0
326	kab	Exchange address bit 1
327	kac	Exchange address bit 2
330	api	Exchange read
331	KBS	Exchange writes done
332	kbz	Gate P to exchange
333	KCA	Go exchange write phase 8
334	KCH	Exchange route code valid phase 16
335	KCI	Exchange route code bit 0 phase 16
336	KCJ	Exchange route code bit 1 phase 16
337	KCK	Exchange route code bit 2 phase 16
340	KAH	Exchange valid count 0
341	KAI	Exchange valid count 1
342	QBT	I/O valid count 0
343	QBU	I/O valid count 1
344	ATB	I/O request from an H-type option on IO01 or IO02 module
345	ATE	Go I/O reference
346	–	–
347	atz	I/O request to JA
350	AUA	I/O block count bit 0
351	AUB	I/O block count bit 1
352	AUC	I/O block count bit 2
353	AUD	I/O block count bit 3
354	aue	I/O block count bit 4
355	AUF	I/O block count = 1
356	–	–
357	–	–
360	aha	I/O read request
361	ahb	I/O write request
362	AHC	I/O block size = 1
363	–	–

364	–	–
365	qaa	I/O address bit 0
366	qab	I/O address bit 1
367	qac	I/O address bit 2
370	AVD	I/O active + 3 phases
371	PCA	I/O address adder bit 0
372	QBW	Single I/O
373	qby	I/O double
374	–	–
375	–	–
376	–	–
377	–	–

CF Option (Revision 3063)

Test Point	Term	Description
200	ANJ	Half mode
201	ANK	Upper
202	–	–
203	–	–
204	BAA	Port A stack 0 section 2^0
205	BAB	Port A stack 0 section 2^1
206	BAC	Port A stack 0 section 2^2
207	BAD	Port A valid
210	BBA	Port A’ stack 0 section 2^0
211	BBB	Port A’ stack 0 section 2^1
212	BBC	Port A’ stack 0 section 2^2
213	BBD	Port A’ valid
214	BCA	Port B stack 0 section 2^0
215	BCB	Port B stack 0 section 2^1
216	BCC	Port B stack 0 section 2^2
217	BCD	Port B valid
220	BDA	Port B’ stack 0 section 2^0
221	BDB	Port B’ stack 0 section 2^1
222	BDC	Port B’ stack 0 section 2^2
223	BDD	Port B’ valid
224	aja	Port C stack 0 section 2^0
225	ajb	Port C stack 0 section 2^1
226	ajc	Port C stack 0 section 2^2
227	ajd	Port C valid
230	aka	Port C’ stack 0 section 2^0

231	akb	Port C’ stack 0 section 2^1
232	akc	Port C’ stack 0 section 2^2
233	akd	Port C’ valid
234	ala	Port D stack 0 section 2^0
235	alb	Port D stack 0 section 2^1
236	alc	Port D stack 0 section 2^2
237	ald	Port D valid
240	HQI	Section 0 priority count bit 0
241	HQJ	Section 0 priority count bit 1
242	HQK	Section 0 priority count bit 2
243	HQL	Section 0 priority count bit 3
244	HQM	Port D has priority
245	–	–
246	HRI	Section 1 priority count bit 0
247	HRJ	Section 1 priority count bit 1
250	HRK	Section 1 priority count bit 2
251	HRL	Section 1 priority count bit 3
252	HRM	Port D has priority
253	–	–
254	HSI	Section 2 priority count bit 0
255	HSJ	Section 2 priority count bit 1
256	HSK	Section 2 priority count bit 2
257	HSL	Section 2 priority count bit 3
260	HSM	Port D has priority
261	–	–
262	HTI	Section 3 priority count bit 0
263	HTJ	Section 3 priority count bit 1
264	HTK	Section 3 priority count bit 2
265	HTL	Section 3 priority count bit 3
266	HTM	Port D has priority
267	–	–
270	HUI	Section 4 priority count bit 0
271	HUJ	Section 4 priority count bit 1
272	HUK	Section 4 priority count bit 2
273	HUL	Section 4 priority count bit 3
274	HUM	Port D has priority
275	–	–
276	HVI	Section 5 priority count bit 0
277	HVJ	Section 5 priority count bit 1
300	HVK	Section 5 priority count bit 2
301	HVL	Section 5 priority count bit 3

302	HVM	Port D has priority
303	–	–
304	HWI	Section 6 priority count bit 0
305	HWJ	Section 6 priority count bit 1
306	HWK	Section 6 priority count bit 2
307	HWL	Section 6 priority count bit 3
310	HWM	Port D has priority
311	–	–
312	HXI	Section 7 priority count bit 0
313	HXJ	Section 7 priority count bit 1
314	HXK	Section 7 priority count bit 2
315	HXL	Section 7 priority count bit 3
316	HXM	Port D has priority
317	–	–
320	lzi	Hold 0
321	lzj	Hold 1
322	lzk	Hold 2
323	lzl	Hold 3
324	lzm	Hold 4
325	lzn	Hold 5
326	lzo	Hold 6
327	lzp	Hold 7
330	pqs	Section valid 0
331	pqt	Section valid 1
332	pqu	Section valid
333	pqv	Section valid 3
334	pqw	Section valid 4
335	pqx	Section valid 5
336	pqy	Section valid 6
337	pqz	Section valid 7
340	PXA	CPU request count
341	–	–
342	–	–
343	–	–
344	–	–
345	PXG	Port A hold to VA option
346	PXH	Port B hold to VA option
347	PXI	Port C hold to VA option
350	prs	Read ports quiet
351	prt	Write ports quiet
352	pru	CM quiet

353	UAB	CPU stack position
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	–	–

CG Option (Revision 3013)

Test Point	Term	Description
200	–	–
201	qag	V*j* data valid
202	qbd	B/T data valid
203	qcd	A/S data valid
204	qdd	Exchange data valid
205	qha	Move data
206	–	–
207	–	–
210	–	–
211	–	–
212	–	–
213	–	–
214	–	–
215	–	–
216	–	–
217	–	–

220	–	–
221	–	–
222	–	–
223	–	–
224	qia	Section bit 0
225	qib	Section bit 1
226	qic	Section bit 2
227	–	–
230	–	–
231	–	–
232	–	–
233	–	–
234	–	–
235	–	–
236	–	–
237	–	–
240	–	–
241	–	–
242	–	–
243	–	–
244	–	–
245	–	–
246	–	–
247	–	–
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–
255	–	–
256	–	–
257	–	–
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	–	–

271	–	–
272	–	–
273	–	–
274	–	–
275	–	–
276	–	–
277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–
311	–	–
312	–	–
313	–	–
314	–	–
315	–	–
316	–	–
317	–	–
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–
337	–	–
340	–	–
341	–	–

342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	–	–

CI Option (Revision 4001)

Test Point	Term	Description
200	QAH	Valid request
201	XXA	Advance Vf
202	XXE	Vf
203	XXI	CMresume
204	QBH	Valid request
205	XXB	Advance Vf
206	XXF	Vf

207	XXJ	CMresume
210	QCD	Valid request
211	XXC	Advance Vf
212	XXG	Vf
213	XXK	CMresume
214	QDC	Valid request
215	XXD	Advance Vf
216	XXH	Vf
217	XXL	CMresume
220	RFM	CPU write valid
221	RGM	CPU write valid
222	RHM	CPU write valid
223	RIM	CPU write valid
224	RMF	I/O write valid
225	RNF	I/O write valid
226	ROF	I/O write valid
227	RPF	I/O write valid
230	VAU	Write second packet
231	UMC	dwAfull
232	VFA	vAfull
233	XMF	cAfull
234	WAC	diowAfull
235	WUD	Advance CPU write
236	WUM	Advance I/O write
237	YKB	Bad bit
240	YMA	Input reference code 0
241	YMB	Input reference code 1
242	YMC	Input reference code 2
243	YMD	Input reference code 3
244	YME	Input reference code 4
245	YMF	Input reference code 5
246	YMG	Input reference code 6
247	YMH	Input reference code 7
250	YMI	Input reference code 8
251	YMJ	Input reference code 9
252	YMK	Input reference code 10
253	YML	Input reference code 11
254	YMM	Input reference code 12
255	YMN	Input reference code 13
256	XYA	Reference code 0
257	XYB	Reference code 1

260	XYC	Reference code 2
261	XYD	Reference code 3
262	XYE	Reference code 4
263	XYF	Reference code 5
264	XYG	Reference code 6
265	XZA	Reference code 7
266	XZB	Reference code 8
267	XZC	Reference code 9
270	XZD	Reference code 10
271	XZE	Reference code 11
272	XZF	Reference code 12
273	XZG	Reference code 13
274	YAI	Reference type 0
275	YAJ	Reference type 1
276	YAK	Reference type 2
277	YAL	Reference type 3
300	YBI	Write reference
301	YBJ	Write reference
302	YBQ	Valid reference to memory
303	YBR	Valid reference to memory
304	YCC	Section quiet
305	YCI	Write abort reference
306	YEA	Steering bit 0
307	YEB	Steering bit 1
310	YEC	Steering bit 2
311	YED	Steering bit 3
312	YEE	Steering bit 4
313	YEF	Steering bit 5
314	YEG	Steering bit 6
315	YGA	Address bit 0
316	YGB	Address bit 1
317	YGC	Address bit 2
320	YGD	Address bit 3
321	YGE	Address bit 4
322	YGF	Address bit 5
323	YGG	Address bit 6
324	YIA	Iaddr bit 2
325	YIB	Iaddr bit 3
326	YIC	Iaddr bit 4
327	YID	Iaddr bit 5
330	YIE	Iaddr bit 6

331	YIF	Iaddr bit 7
332	YIG	Iaddr bit 8
333	YIH	Iaddr bit 9
334	YII	Iaddr bit 10
335	YIJ	I/O force bit 0
336	YIK	I/O force bit 1
337	YKA	Range error
340	MAA	Set 4 sections
341	MAE	Set 8 sections
342	MAI	Force section bit 2
343	–	–
344	MBA	Enable forcing subsection bit 0
345	MBB	Enable forcing subsection bit 1
346	MBC	Enable forcing subsection bit 2
347	MBD	Enable forcing bank bit 0
350	MBE	Enable forcing bank bit 1
351	MBF	Enable forcing bank bit 2
352	MBG	Enable forcing bank bit 3
352	MBH	Clear all MB configurations
354	MCA	Set subsection bit 0 to 1
355	MCB	Set subsection bit 1 to 1
356	MCC	Set subsection bit 2 to 1
357	MCD	Set bank bit 0 to 1
360	MCE	Set bank bit 1 to 1
361	MCF	Set bank bit 2 to 1
362	MCG	Set bank bit 3 to 1
363	MCH	Clear all MC configurations
364	MDA	Force group bit 0
365	MDB	Force group bit 1
366	MDC	Set group bit 0 to a 1
367	MDD	Set group bit 1 to a 1
370	MDH	Clear all MD configurations
371	MFA	Force CPU to upper 256K
372	MFI	Force I/O to upper 256K
373	–	–
374	NAD	Sanity Code
375	LCI	Interface MC
376	LZJ	Memory MC
377	–	–

CJ Option (Revision 3025)

Test Point	Term	Description
200	awa	Vev resume count 0
201	awb	Vev resume count 1
202	awc	Vod resume count 0
203	awd	Vod resume count 1
204	awe	B/T resume count 0
205	awf	B/T resume count 1
206	awg	A/S resume count 0
207	awh	F/X resume count 0
210	awi	I/O resume count 0
211	agg	Hold
212	aha	Valid
213	AHG	Turn valid off
214	YZC	Sanity code from memory
215	–	–
216	–	–
217	–	–
220	AHI	Maintenance channel return (INV)
221	–	–
222	–	–
223	–	–
224	ayf	Valid in count 0
225	ayg	Valid in count 1
226	ayh	Valid in count 2
227	ayi	Valid in count 3
230	axm	Vev released to CK
231	axn	Vod released to CK
232	axo	B/T released to CK
233	axp	A/S released to CK
234	–	–
235	–	–
236	–	–
237	–	–
240	axq	F/X released to CK
241	axr	I/O released to CK
242	EAC	Correctable error
243	EHA	Enter error information stack
244	EIA	Enter uncorrectable error in error information stack
245	EJA	Clear error information stack

246	FIA	Error information is stacked
247	YZZ	Sanity recognized
250	pdc	Enter stack 1
251	pec	Shift stack 1
252	pfc	Hold stack 1
253	pxi	Stack 1 valid
254	AOF	CPU or I/O write path correctable error
255	AOG	CPU or I/O write path uncorrectable error
256	AOH	CPU or I/O bank readout correctable error
257	AOI	CPU or I/O bank readout uncorrectable error
260	pgc	Enter stack 2
261	phc	Shift stack 2
262	pic	Hold stack 2
263	pxb	Stack 2 valid
264	pjc	Enter stack 3
265	pkc	Shift stack 3
266	plc	Hold stack 3
267	pxc	Stack 3 valid
270	pmc	Enter stack 4
271	pnc	Shift stack 4
272	poc	Hold stack 4
273	pxd	Stack 4 valid
274	–	–
275	–	–
276	–	–
277	–	–
300	ppc	Enter stack 5
301	pqc	Shift stack 5
302	prc	Hold stack 5
303	pxe	Stack 5 valid
304	psc	Enter stack 6
305	ptc	Shift stack 6
306	puc	Hold stack 6
307	pxf	Stack 6 valid
310	–	–
311	–	–
312	–	–
313	–	–
314	–	–
315	–	–
316	–	–

317	–	–
320	pvc	Enter stack 7
321	pwc	Hold stack 7
322	pxg	Stack 7 valid
323	aoy	Stack 0 valid
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–
337	–	–
340	–	–
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365	–	–
366	–	–
367	–	–

370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	–	–

HA Option (Revision 3005)

Test Point	Term	Description
200	JAA	Write address
201	JAB	Write address
202	JAC	Write address
203	JAD	Buffer number
204	JAE	Buffer number
205	JAF	Buffer number
206	JHA	Go write
207	–	–
210	KAL	Read reference register A block length/buffer number
211	KAM	Read reference register A block length/buffer number
212	KAN	Read reference register A block length/buffer number
213	KAO	Read reference register A block length/buffer number
214	KAP	Read reference register A block length/buffer number
215	KAQ	Read reference register A block length/buffer number
216	KAR	Null read (HA0)
217	KAS	Error correction preference bit 0
220	KAT	Error correction preference bit 1
221	KAU	Null read (HA1)
222	–	–
223	–	–
224	KBL	Read reference register B block length/buffer number
225	KBM	Read reference register B block length/buffer number
226	KBN	Read reference register B block length/buffer number
227	KBO	Read reference register B block length/buffer number
230	KBP	Read reference register B block length/buffer number
231	KBQ	Read reference register B block length/buffer number
232	KBR	Null read (HA0)
233	KBS	Error correction preference bit 0
234	KBT	Error correction preference bit 1

235	KBU	Null read (HA1)
236	–	–
237	–	–
240	KDA	Read address bit 0
241	KDB	Read address bit 1
242	KDC	Read address bit 2
243	KDD	Read address bit 3
244	KDE	Read address bit 4
245	KDF	Read address bit 5
246	KEH	Error correction preference bit 0
247	KEI	Error correction preference bit 1
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–
255	–	–
256	–	–
257	–	–
260	LMA	Null read (HA0)
261	LNA	Null read (HA0)
262	LAD	Input reference (HA0,1), Go rd (HA2,3)
263	LRA	Failing edge go read
264	lba	Input block length into A register
265	LEA	I – read A, O – read B
266	LKF	Start new read reference (HA0,1)
267	LYE	End of reference
270	–	–
271	–	–
272	–	–
273	–	–
274	–	–
275	–	–
276	–	–
277	–	–
300	LCA	A register read out
301	LCB	B register read out
302	LYA	A register is full
303	LYB	B register is full
304	LGA	Valid HSR read
305	LHA	Done with current BL

306	LYC	Address = 0
307	LYD	Decrement address
310	–	–
311	–	–
312	–	–
313	–	–
314	NRA	Rank C
315	–	–
316	–	–
317	–	–
320	–	–
321	–	–
322	–	–
323	–	–
324	NPA	Rank B
325	NPB	–
326	LNC	–
327	NHA	SECDED error
330	NIA	Syndrome
331	NIB	Syndrome
332	NIC	Syndrome
333	NID	Syndrome
334	NIE	Syndrome
335	NIF	Syndrome
336	NIG	Syndrome
337	NIH	Syndrome
340	MAA	Data out counter
341	MAB	Data out counter
342	MDB	Data ready
343	–	–
344	POA	Resume
345	prd	No resume and DCNTR = 3
346	–	–
347	–	–
350	PSA	Hold FIFO rank A
351	PSB	Hold FIFO rank B
352	PSC	Hold FIFO rank C
353	PSD	Hold FIFO rank D
354	PFA	Data valid FIFO A
355	PGA	Data valid FIFO B
356	PHA	Data valid FIFO C

357	PIA	Data valid FIFO D
360	AEA	Data bit 0
361	AEB	Data bit 1
362	FAA	Data bit 0
363	FAB	Data bit 1
364	BAA	Data bit 0 HSR (out)
365	BAB	Data bit 1 HSR (out)
366	HAA	Data bit 0 HSR (in)
367	HAB	Data bit 1 HSR (in)
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	–	–

HB Option (Revision 3012)

Test Point	Term	Description
200	QCB	DMA access memory configuration bit
201	QCF	DMA access memory partition selection
202	QCG	DMA access memory partition selection
203	QCH	DMA access use memory partition selection
204	QBL	DMA access alternate word write mode
205	CNB	Data readout control starting memory address bit 0
206	CNC	Data readout control starting memory address bit 1
207	CND	Data readout control starting memory address bit 2
210	AMA	Write data control select lower bits to HA0 phase 4
211	DAA	I/O module interface interrupt request
212	DAB	I/O module interface 033*ijk* response
213	DAC	I/O module interface reference request
214	ECW	Memory write controls go buffer write phase 4
215	EDE	Memory write controls reference designator phase 4+
216	EDF	Memory write controls reference designator phase 4+
217	EDG	Memory write controls reference designator phase 4+
220	EET	Memory write controls write buffer count phase 6+ (+1)
221	EEU	Memory write controls write buffer count phase 6+ (+1)
222	EEV	Memory write controls write buffer count phase 6+ (+1)
223	EEW	Memory write controls write buffer count phase 6+ (+1)

224	EHA	Memory write controls write buffer pointer
225	EHB	Memory write controls write buffer pointer
226	EHC	Memory write controls write buffer pointer
227	EIV	Memory write controls go write request phase 2
230	EQD	Memory write controls go readout at HA0/1
231	EQF	Memory write controls number of go readouts sent to ha0/1
232	EQG	Memory write controls number of go readouts sent to ha0/1
233	EQZ	Memory write controls 2 – 7 write buffers available and no DMA requests
234	ERA	Memory write controls readout buffer pointer
235	ERB	Memory write controls readout buffer pointer
236	ERC	Memory write controls readout buffer pointer
237	ESD	Memory write controls start readout
240	ESI	Memory write controls readout buffer pointer
241	ESJ	Memory write controls readout buffer pointer
242	ESK	Memory write controls readout buffer pointer
243	ESW	Memory write controls start reference request
244	ETA	Memory write controls reference buffer pointer
245	ETB	Memory write controls reference buffer pointer
246	ETC	Memory write controls reference buffer pointer
247	EZF	Memory write controls starting address is odd (HA0 null readout)
250	EZA	Memory write controls readout block count bit 0
251	EZB	Memory write controls readout block count bit 1
252	EZC	Memory write controls readout block count bit 2
253	EZD	Memory write controls readout block count bit 3
254	EZX	Memory write controls HA1 null readout
255	FXU	Memory write controls reference designator to memory readout
256	FXV	Memory write controls reference designator to memory readout
257	FXW	Memory write controls reference designator to memory readout
260	FXX	Memory write controls partition selection to memory readout
261	FXY	Memory write controls partition selection to memory readout
262	GAE	Memory read controls go read reference phase 2
263	GAZ	Memory read controls allow read request (less than 3 buffers full)
264	GAI	Memory read controls buffer 0 busy
265	GAK	Memory read controls buffer 1 busy
266	GAM	Memory read controls buffer 2 busy
267	GAO	Memory read controls buffer 3 busy
270	GBC	Memory read controls go capture buffer 0
271	GCC	Memory read controls go capture buffer 1
272	GDC	Memory read controls go capture buffer 2
273	GEC	Memory read controls go capture buffer 3
274	GGA	Memory read controls first FIFO reference number

275	GGB	Memory read controls first FIFO reference number
276	GGC	Memory read controls first FIFO reference number
277	GGR	Memory read controls first FIFO busy
300	GGE	Memory read controls first FIFO buffer location
301	GGF	Memory read controls first FIFO buffer location
302	GHE	Memory read controls second FIFO buffer location
303	GHF	Memory read controls second FIFO buffer location
304	GHA	Memory read controls second FIFO reference number
305	GHB	Memory read controls second FIFO reference number
306	GHC	Memory read controls second FIFO reference number
307	GHR	Memory read controls second FIFO busy
310	QEO	DMA reference controls enter block length
311	QEQ	DMA reference controls enter starting address
312	QET	DMA reference controls enter write data
313	QEV	DMA reference controls write data captured
314	QEX	DMA reference controls begin DMA sequence (first 37 route code)
315	GIR	Memory read controls third FIFO busy
316	GJE	Memory read controls fourth FIFO buffer location
317	GJF	Memory read controls fourth FIFO buffer location
320	GJA	Memory read controls fourth FIFO reference number
321	GJB	Memory read controls fourth FIFO reference number
322	GJC	Memory read controls fourth FIFO reference number
323	GJR	Memory read controls fourth FIFO busy
324	GLA	Memory read controls buffer 0 in use
325	GLB	Memory read controls buffer 1 in use
326	GLC	Memory read controls buffer 2 in use
327	GLD	Memory read controls buffer 3 in use
330	GLE	Memory read controls buffer 4 in use
331	GLF	Memory read controls buffer 5 in use
332	GLG	Memory read controls buffer 6 in use
333	GLH	Memory read controls buffer 7 in use
334	GOA	Memory read controls read data buffer pointer even references
335	GOB	Memory read controls read data buffer pointer even references
336	GOC	Memory read controls read data buffer pointer even references
337	GOD	Memory read controls go read data
340	GPA	Memory read controls read data buffer pointer odd references
341	GPA	Memory read controls read data buffer pointer odd references
342	GPB	Memory read controls read data buffer pointer odd references
343	GPC	Memory read controls go read data
344	GTA	Memory read controls next buffer readout pointer
345	GTB	Memory read controls next buffer readout pointer

346	GTC	Memory read controls next buffer readout pointer
347	GUT	Memory read controls go SECDED swap phase 4
350	GVI	Memory read controls output block counter phase 2+
351	GVJ	Memory read controls output block counter phase 2+
352	GVK	Memory read controls output block counter phase 2+
353	GVL	Memory read controls output block counter phase 2+
354	GWJ	Memory read controls readout starting address bit 0
355	GWK	Memory read controls readout starting address bit 1
356	GWL	Memory read controls readout starting address bit 2
357	GXC	Memory read controls go readout data to I/O module phase 6+
360	GYA	Memory read controls reference designator for readout
361	GYB	Memory read controls reference designator for readout
362	GYC	Memory read controls reference designator for readout
363	GVB	Memory read controls start new readout sequence
364	QFA	DMA reference controls block count bit 0
365	QFB	DMA reference controls block count bit 1
366	QTA	DMA reference controls data register bit 0
367	QVL	DMA reference controls data register bit 63
370	RAA	DMA reference controls write request pending
371	REW	DMA reference controls increment starting address
372	REX	DMA reference controls decrement block length
373	RGD	DMA reference controls insert read request
374	RIK	DMA reference controls readout reference arriving phase 10
375	RJR	DMA reference controls read request outstanding
376	RJS	DMA reference controls read request outstanding and abandoned
377	RJW	DMA reference controls read terminate sequence request

HC Option (Revision 3004)

Test Point	Term	Description
200	TBA	Write complete counter number 0 bit 0
201	TBB	Write complete counter number 0 bit 1
202	TBC	Write complete counter number 0 bit 2
203	TBD	Write complete counter number 0 bit 3
204	THA	Write complete counter number 1 bit 0
205	THB	Write complete counter number 1 bit 1
206	THC	Write complete counter number 1 bit 2
207	THD	Write complete counter number 1 bit 3
210	TNA	Write complete counter number 2 bit 0
211	TNB	Write complete counter number 2 bit 1
212	TNC	Write complete counter number 2 bit 2

213	TND	Write complete counter number 2 bit 3
214	TTA	Write complete counter number 3 bit 0
215	TTB	Write complete counter number 3 bit 1
216	TTC	Write complete counter number 3 bit 2
217	TTD	Write complete counter number 3 bit 3
220	UBA	Write complete counter number 4 bit 0
221	UBB	Write complete counter number 4 bit 1
222	UBC	Write complete counter number 4 bit 2
223	UBD	Write complete counter number 4 bit 3
224	UHA	Write complete counter number 5 bit 0
225	UHB	Write complete counter number 5 bit 1
226	UHC	Write complete counter number 5 bit 2
227	UHD	Write complete counter number 5 bit 3
230	UNA	Write complete counter number 6 bit 0
231	UNB	Write complete counter number 6 bit 1
232	UNC	Write complete counter number 6 bit 2
233	UND	Write complete counter number 6 bit 3
234	UTA	Write complete counter number 7 bit 0
235	UTB	Write complete counter number 7 bit 1
236	UTC	Write complete counter number 7 bit 2
237	UTD	Write complete counter number 7 bit 3
240	TAQ	Write complete counter number 0 decrement bit 0
241	TAR	Write complete counter number 0 decrement bit 1
242	TAS	Write complete counter number 0 decrement bit 2
243	TAT	Write complete counter number 0 decrement bit 3
244	TGQ	Write complete counter number 1 decrement bit 0
245	TGR	Write complete counter number 1 decrement bit 1
246	TGS	Write complete counter number 1 decrement bit 2
247	TGT	Write complete counter number 1 decrement bit 3
250	TMQ	Write complete counter number 2 decrement bit 0
251	TMR	Write complete counter number 2 decrement bit 1
252	TMS	Write complete counter number 2 decrement bit 2
253	TMT	Write complete counter number 2 decrement bit 3
254	TSQ	Write complete counter number 3 decrement bit 0
255	TSR	Write complete counter number 3 decrement bit 1
256	TSS	Write complete counter number 3 decrement bit 2
257	TST	Write complete counter number 3 decrement bit 3
260	UAQ	Write complete counter number 4 decrement bit 0
261	UAR	Write complete counter number 4 decrement bit 1
262	UAS	Write complete counter number 4 decrement bit 2
263	UAT	Write complete counter number 4 decrement bit 3

264	UGQ	Write complete counter number 5 decrement bit 0
265	UGR	Write complete counter number 5 decrement bit 1
266	UGS	Write complete counter number 5 decrement bit 2
267	UGT	Write complete counter number 5 decrement bit 3
270	UMQ	Write complete counter number 6 decrement bit 0
271	UMR	Write complete counter number 6 decrement bit 1
272	UMS	Write complete counter number 6 decrement bit 2
273	UMT	Write complete counter number 6 decrement bit 3
274	USQ	Write complete counter number 7 decrement bit 0
275	USR	Write complete counter number 7 decrement bit 1
276	USS	Write complete counter number 7 decrement bit 2
277	UST	Write complete counter number 7 decrement bit 3
300	TAW	Write complete counter number 0 increment bit 0
301	TGW	Write complete counter number 1 increment bit 0
302	TMW	Write complete counter number 2 increment bit 0
303	TSW	Write complete counter number 3 increment bit 0
304	UAW	Write complete counter number 4 increment bit 0
305	UGW	Write complete counter number 5 increment bit 0
306	UMW	Write complete counter number 6 increment bit 0
307	USW	Write complete counter number 7 increment bit 0
310	EAA	Sanity code returned from I/O module
311	EAZ	Sanity code detected from I/O module
312	KBQ	Command strobe to I/O module
313	CON	Go data readout to I/O phase 20
314	CTI	Data readout left/right sequencer counter + 1 term bit 0
315	CTJ	Data readout left/right sequencer counter + 1 term bit 2
316	CTK	Data readout left/right sequencer counter + 1 term bit 3
317	FVW	SECDED errors from I/O
320	TEX	Write complete counter number 0 = 0
321	TKX	Write complete counter number 1 = 0
322	TQX	Write complete counter number 2 = 0
323	TWX	Write complete counter number 3 = 0
324	UEX	Write complete counter number 4 = 0
325	UKX	Write complete counter number 5 = 0
326	UQX	Write complete counter number 6 = 0
327	UWX	Write complete counter number 7 = 0
330	QBN	DMA control command 02, 06 write memory
331	QBP	DMA control command 01, 05 read memory
332	WFB	DMA diagnostic mode 150 write path SECDED maintenance mode
333	QAA	DMA control serial input
334	QBD	DMA control route code 35

335	WFF	DMA diagnostic mode 152 read SECDED check byte
336	QEA	DMA control input sequence clock period 4
337	QEB	DMA control input sequence clock period 10 (route code 35)
340	QEE	DMA control input sequence clock period 5
341	QEG	DMA control input sequence clock period 105
342	QEJ	DMA control input sequence clock period 15 (route code 35)
343	QPA	DMA control enter data shift register with read data phase 22
344	QTA	DMA control enter data shift register bit 00
345	QVL	DMA control enter data shift register bit 63
346	RFZ	DMA control return channel to HG0 (output from HB and HC combined)
347	RGA	DMA control return channel to HG0 (output from HB)
350	RGQ	DMA control return channel route code 36 detected
351	RMY	DMA control return channel output counter active
352	RMZ	DMA control return channel output counter at terminal count
353	QDZ	DMA control return channel input counter at terminal count
354	XCA	Maintenance channel pass-throughs mc port<–>share sanity code
355	XCB	Maintenance channel pass-throughs mc port<–>share maintenance channel
356	XCC	Maintenance channel pass-throughs mc port<–>share error logger return
357	XCD	Maintenance channel pass-throughs mc port<–>share sanity code return
360	XCE	Maintenance channel pass-throughs mc port<–>share maintenance channel return
361	XCF	Maintenance channel pass-throughs mc port<–>share error logger
362	XCI	Maintenance channel pass-throughs mc port<–>HG0 sanity code
363	–	–
364	–	–
365	XCL	Maintenance channel pass-throughs mc port<–>hg0 sanity code return
366	–	–
367	CZB	Uncorrectable memory error
370	XCQ	Maintenance channel pass-throughs HG0<–>I/O sanity code
371	XCR	Maintenance channel pass-throughs HG0<–>I/O maintenance channel
372	XCS	Maintenance channel pass-throughs HG0<–>I/O error logger return
373	XCT	Maintenance channel pass-throughs HG0<–>I/O sanity code return
374	XCU	Maintenance channel pass-throughs HG0<–>I/O maintenance channel return
375	XCV	Maintenance channel pass-throughs HG0<–>I/O error logger
376	AMA	I/O write data control select lower bits to HA0
377	AMQ	I/O write data control enter maintenance channel data to HA0/1

HD Option (Revision 4003)

Test Point	Term	Description
200	TOA	Exchange interrupt mode register FNX
201	TOB	Exchange interrupt mode register IMI
202	TOC	Exchange interrupt mode register IDL
203	TOD	Exchange interrupt mode register IPC
204	TOE	Exchange interrupt mode register IIO
205	TOF	Exchange interrupt mode register IIP
206	TOG	Exchange interrupt mode register IRT
207	TOH	Exchange interrupt mode register IMC
210	TOI	Exchange interrupt mode register ICM
211	TOJ	Exchange interrupt mode register IBP
212	TOK	Exchange interrupt mode register FEX
213	TOL	Exchange interrupt mode register IPR
214	TOM	Exchange interrupt mode register IOR
215	TON	Exchange interrupt mode register IFP
216	TOO	Exchange interrupt mode register IUM
217	TOP	Exchange interrupt mode register IRP
220	TOQ	Exchange interrupt mode register IAM
221	TSQ	Exchange interrupt flag register AMI
222	SPE	Accepting I/O interrupts
223	TQD	Interrupt flag holding register PCI
224	SRA	Enable interrupt mode
225	TQF	Interrupt flag holding register ICP
226	TQG	Interrupt flag holding register RTI
227	TQH	Interrupt flag holding register MCU
230	TQI	Interrupt flag holding register MEC
231	TQJ	Interrupt flag holding register BPI
232	REU	Carry into real-time clock
233	REZ	Carry out of real-time clock
234	TQM	Interrupt flag holding register ORE
235	TQN	Interrupt flag holding register FPE
236	TQO	Interrupt flag holding register MEU
237	TQP	Interrupt flag holding register RPE
240	TSA	Exchange interrupt flag register NEX
241	TSB	Exchange interrupt flag register MII
242	TSC	Exchange interrupt flag register DL
243	TSD	Exchange interrupt flag register PCI
244	TSE	Exchange interrupt flag register IOI
245	TSF	Exchange interrupt flag register ICP

246	TSG	Exchange interrupt flag register RTI
247	TSH	Exchange interrupt flag register MCU
250	TSI	Exchange interrupt flag register MEC
251	TSJ	Exchange interrupt flag register BPI
252	TSK	Exchange interrupt flag register EEX
253	TSL	Exchange interrupt flag register PRE
254	TSM	Exchange interrupt flag register ORE
255	TSN	Exchange interrupt flag register FPE
256	TSO	Exchange interrupt flag register MEU
257	TSP	Exchange interrupt flag register RPE
260	SHA	Exchange mode bit register MM
261	SHB	Exchange mode bit register BDM
262	SHC	Exchange mode bit register ESL
263	SHD	Exchange mode bit register TRI
264	SHE	Exchange status bit register BML
265	SHF	Exchange status bit register WS
266	SHG	Exchange status bit register FPS
267	SHH	Exchange status bit register VNU
270	SHP	Exchange mode bit register SCE
271	LAG	Set dirty bits from CB0
272	LBC	Set dirty bits from CB0 cell counter bit 2
273	HAP	Performance monitor update/readout pointer bit 0
274	HAQ	Performance monitor update/readout pointer bit 1
275	HAR	Performance monitor update/readout pointer bit 2
276	HAS	Performance monitor update/readout pointer bit 3
277	HAT	Performance monitor update/readout pointer bit 4
300	TTH	Error exchange request
301	TTI	Error or exit exchange request
302	TTJ	Deadstart exchange request
303	TTO	Block I/O for exchange request
304	TUF	Go exchange from JA
305	TUK	Exchange reads complete
306	TUV	Clear SIE bit (taking I/O interrupt)
307	TUW	Allow HPM and dirty bit entry
310	TVD	Waiting on test and set inst (0034*jk*)
311	TVG	Release required for test and set
312	TVI	Semaphore was set (test and set successful)
313	TVL	Flush command outstanding
314	TVV	Flush response from shared
315	hii	Performance monitor blank registers to zero
316	glz	Performance monitor go increment

317	GOZ	Performance monitor carry out
320	DBI	Release S*i*
321	DBJ	Enter S*i*
322	DBK	Release A*i*
323	DBL	Enter A*i*
324	DBD	*i*,*j* designator bit 0
325	DBE	*i*,*j* designator bit 0
326	DBF	*i*,*j* designator bit 0
327	DCB	Release shared path
330	CFA	0013*j*0, 0014*j*3
331	CFB	0013*j*1, 001302, 001303
332	CFC	0014*j*1, 001402, 0014*j*4
333	CFD	001405, 001406, 001407
334	CFE	0015*jk*, 0017*jk*
335	CFF	002[0–6]*jk*
336	–	–
337	–	–
340	–	–
341	CFK	072*i*00, 073*ij*1
342	CFL	073*ij*5
343	CFM	023*ij*6, 023*ij*7, 027*ij*2,3
344	CGA	001000
345	CGB	0010*jk*, 0011*jk*, 0012*jk*
346	CGD	001600
347	CGE	0034*jk*, 0036*jk*, 0037*jk*
350	CGF	0064*jk*
351	CGG	026*ij*4, 026*ij*5, 026*ij*6, 026*ij*7
352	CGH	033*ijk*
353	CGI	027*ij*6, 027*ij*7
354	CGJ	072*i*02, 072*ij*3, 072*ij*6
355	CGK	073*i*02, 073*ij*3, 073*ij*6
356	CIQ	A*i* RLS code 20 – 23, 40 – 41 from shared
357	CIR	S*i* RLS code 31, 44 from shared
360	LGF	First enter RTC
361	–	–
362	RFA	RTC bit 0
363	RFF	RTC bit 5
364	RFL	RTC bit 11
365	RFR	RTC bit 17
366	RFX	RTC bit 23
367	HUB	Performance monitor busy flag

370	WFB	Performance monitor diagnostic mode (code 162)
371	RPW	Exchange status bit register BDD
372	CGC	0014*j*0, 001600
373	SHI	Exchange status bit register SSB
374	–	–
375	–	–
376	–	–
377	–	–

HF Option (Revision 5010)

Test Point	Term	Description
200	AAA	Current instruction bit 0 phase 4
201	AAB	Current instruction bit 1 phase 4
202	AAC	Current instruction bit 2 phase 4
203	AAD	Current instruction bit 3 phase 4
204	AAE	Current instruction bit 4 phase 4
205	AAF	Current instruction bit 5 phase 4
206	AAG	Current instruction bit 6 phase 4
207	AAH	Current instruction bit 7 phase 4
210	AAI	Current instruction bit 8 phase 4
211	AAL	Current instruction bit 11 phase 4
212	AAM	Current instruction bit 12 phase 4
213	AAN	Current instruction bit 13 phase 4
214	AAO	Current instruction bit 14 phase 4
215	AAP	Current instruction bit 15 phase 4
216	ACP	001 instruction phase 4.5
217	ACR	002 instruction phase 4.5
220	ACS	003 instruction phase 4.5
221	ACU	006 instruction phase 4.5
222	ACV	026 instruction phase 4.5
223	ACW	027 instruction phase 4.5
224	ACX	033 instruction phase 4.5
225	ACY	072 instruction phase 4.5
226	ACZ	073 instruction phase 4.5
227	AGB	Monitor mode
230	ASX	Instruction valid phase 6
231	aij	Select A*j* for designator to shared mod
232	ail	Select A*k* for designator to shared mod
233	AIN	Select *jk* for designator to shared mod
234	AIZ	001500 instruction clear performance monitor

235	AKK	Send upper 32 bits to shared module
236	ALA	Shared command bit 0
237	ALB	Shared command bit 1
240	ALC	Shared command bit 2
241	ALD	Shared command bit 3
242	ALE	Shared command bit 4
243	ALF	Shared command bit 5
244	ASZ	005400 instruction decode
245	AUA	Increment performance monitor 20 phase 8
246	AUB	Increment performance monitor 21 phase 8
247	AUC	Increment performance monitor 22 phase 8
250	AUD	Increment performance monitor 23 phase 8
251	AUE	Increment performance monitor 24 phase 8
252	AUF	Increment performance monitor 25 phase 8
253	AUG	Increment performance monitor 26 phase 8
254	AUH	Increment performance monitor 27 phase 8
255	AVA	Increment performance monitor 10 phase 8
256	AVB	Increment performance monitor 11 phase 8
257	AVC	Increment performance monitor 12 phase 8
260	AVD	Increment performance monitor 13 phase 8
261	AVE	Increment performance monitor 14 phase 8
262	AVF	Increment performance monitor 15 phase 8
263	AVG	Increment performance monitor 16 phase 8
264	AVH	Increment performance monitor 17 phase 8
265	AVI	Increment performance monitor 0 phase 8
266	AVJ	Increment performance monitor 1 phase 8
267	AVK	Increment performance monitor 2 phase 8
270	AVL	Increment performance monitor 3 phase 8
271	AWA	Increment performance monitor 30 phase 8
272	AWB	Increment performance monitor 31 phase 8
273	AWC	Increment performance monitor 32 phase 8
274	AWD	Increment performance monitor 33 phase 8
275	AWE	Increment performance monitor 34 phase 8
276	AWF	Increment performance monitor 35 phase 8
277	AWG	Increment performance monitor 36 phase 8
300	AWH	Increment performance monitor 37 phase 8
301	BCA	Interrupt request from I/O module
302	BCB	033*ijk* response
303	BCN	I/O command, delay shared command
304	BDB	I/O response valid
305	BDC	A*i*/S*i* – I/O response collision

306	CAA	Shared response bit 0
307	CAB	Shared response bit 1
310	CAC	Shared response bit 2
311	CAD	Shared response bit 3
312	CAE	Shared response bit 4
313	CAF	Shared response bit 5
314	CAG	Recognized the sanity code from shared module
315	cba	Shared response 06 set RTC
316	CBK	Enter RTC, no shared module
317	KTB	001500 instruction, master clear sequence phase 8
320	KUA	HPM busy
321	KUI	First kill rank (inhibit if MM')
322	KUX	Active, inhibit kill
323	KVO	Hold performance monitor counters
324	KWA	Reset pointers
325	KXA	Increment pointers
326	MAA	Outstanding CPU memory references bit 0
327	MAB	Outstanding CPU memory references bit 1
330	MAC	Outstanding CPU memory references bit 2
331	MAD	Outstanding CPU memory references bit 3
332	MAE	Outstanding CPU memory references bit 4
333	MAV	CPU memory reference decrement value bit 0
334	MAW	CPU memory reference decrement value bit 1
335	MAX	CPU memory reference decrement value bit 2
336	MAY	CPU memory reference decrement value bit 3
337	MAZ	CPU memory reference decrement value bit 4
340	MHC	No outstanding memory references
341	MAK	Hold CM issue
342	SAA	Memory error to status registers 4 – 6
343	SFP	Status register 4 read
344	SFQ	Status register 5 read
345	SFR	Status register 6 read
346	SFT	Status registers 4 – 6 shifter full
347	SFU	Status registers 4 – 6 shift in error
350	SEU	Status registers 4 – 6 full
351	SEV	Clear status registers 4 – 6
352	SIA	Port A LAT fault
353	SIB	Port A' LAT fault
354	SIC	Port B LAT fault
355	SID	Port B' LAT fault
356	SIE	Port C LAT fault

357	SIF	Port C' LAT fault
360	SIG	Port D LAT fault
361	SIH	Port E LAT fault
362	SIP	LAT fault, ORE
363	SIQ	LAT fault, PRE
364	SKA	RPE error
365	SMJ	Status register 7 read
366	SMN	Status register 7 shifter full
367	SMO	Status register 7 shift in error
370	SMR	Status register 7 full
371	UBA	Response code = 5*x*
372	UGC	Shifted data ready
373	WCA	Share access
374	WCD	Originate I/O commands
375	WCE	Pass through I/O commands
376	WFB	Performance monitor maintenance mode
377	ANB	001501 phase 6

HG Option (Revision 5000)

Test Point	Term	Description
200	ADA	A*i*/S*i* data bit 0 function code
201	ADB	A*i*/S*i* data bit 1 function code
202	ADC	A*i*/S*i* data bit 2 function code
203	ADD	A*i*/S*i* data bit 3 function code
204	ADE	A*i*/S*i* data bit 4 function code
205	ADI	A*i*/S*i* data bit 8 chip type
206	ADJ	A*i*/S*i* data bit 9 chip type
207	ADK	A*i*/S*i* data bit 10 chip type
210	ADL	A*i*/S*i* data bit 11 chip type
211	ADM	A*i*/S*i* data bit 12 chip type
212	ADN	A*i*/S*i* data bit 13 chip type
213	ADO	A*i*/S*i* data bit 14 chip type
214	ADP	A*i*/S*i* data bit 15 chip type
215	ADQ	A*i*/S*i* data bit 16 chip type
216	ADR	A*i*/S*i* data bit 17 chip type
217	ADS	A*i*/S*i* data bit 18 loop address
220	ADT	A*i*/S*i* data bit 19 loop address
221	ADU	A*i*/S*i* data bit 20 loop address
222	ADV	A*i*/S*i* data bit 21 loop address
223	ADW	A*i*/S*i* data bit 22 loop address

224	ADX	A*i*/S*i* data bit 23 loop address
225	AFA	Go 075*i*75 set maintenance mode
226	DAA	I/O response valid
227	DAF	Gate A*i*/S*i* upper 32 bits to shared
230	EAA	Sanity code from mc port
231	EAZ	Successful recognition from mc port
232	ECA	Sanity code from shared
233	WCO	Sanity code recognized from shared
234	EFQ	Selected proper offset for sanity code from I/O port
235	EGQ	Selected proper offset for sanity code from shared port
236	EIF	I/O path selected
237	EIN	Shared path selected
240	EKB	Route code bit 0
241	EKD	Route code bit 2
242	EMI	Route code 30
243	EML	Route code 33
244	EMM	Route code 34
245	EMN	Route code 35
246	emp	Route code 37
247	EMQ	Route code detected
250	EMR	Blank out route code
251	EOL	Route code 33
252	EOM	Route code 34
253	EON	Route code 35
254	EOQ	Maintenance channel return
255	EQL	Capture loop command
256	FAA	Channel initiated request
257	FAF	073*i*75 busy
260	FAG	Maintenance mode
261	FAI	Go channel request
262	FAJ	Go 073*i*75 request
263	FBB	Collision imminent –> send inhibit response
264	FDS	Loop command output register
265	HAA	Sanity code return from I/O path
266	HAZ	Successful recognition
267	JCA	Error information from section 0 bit 0
270	JCB	Error information from section 0 bit 1
271	JGA	Error information from section 1 bit 0
272	JGB	Error information from section 1 bit 1
273	JKA	Error information from section 2 bit 0
274	JKB	Error information from section 2 bit 1

275	JOA	Error information from section 3 bit 0
276	JOB	Error information from section 3 bit 1
277	KCA	Error information from section 4 bit 0
300	KCB	Error information from section 4 bit 1
301	KGA	Error information from section 5 bit 0
302	KGB	Error information from section 5 bit 1
303	KKA	Error information from section 6 bit 0
304	KKB	Error information from section 6 bit 1
305	KOA	Error information from section 7 bit 0
306	KOB	Error information from section 7 bit 1
307	LIA	Correctable memory error
310	LIB	Uncorrectable memory error
311	LLG	CPU and error log priority counter bit 0
312	LLI	CPU and error log priority counter bit 1
313	LLK	CPU and error log priority counter bit 2
314	LMW	Error any section
315	LMX	Error any section
316	LUG	Register parity error bit 0
317	LUH	Register parity error bit 1
320	LUI	Register parity error bit 2
321	LUJ	Register parity error bit 3
322	LUK	Register parity error bit 4
323	LUL	Register parity error bit 5
324	LUV	Register parity error for CPU
325	LVC	Register parity error for error logger
326	LVF	Enter parity error
327	LYA	Shift error to status register
330	LYD	Hold error for error logger
331	DCA	Collision (A*i*/S*i* with I/O response)
332	LVG	Status registers 4 – 6 are full
333	MAA	Error data from I/O
334	MMV	Memory error to status registers 4 – 6
335	MOA	I/O error to error logger
336	MOH	Error channel busy
337	MOP	Memory/RPE error to error logger
340	MOQ	Error logger return to I/O
341	MOR	Error logger data
342	mpf	Enter memory error data
343	MPM	Enter RPE data
344	MPX	Shift data to error log
345	mqe	Go shift error logger data in/out

346	MRE	Start RPE shifting
347	MTQ	Register parity error to SR 7
350	NAZ	Error from I/O
351	NCQ	Error logger response
352	–	–
353	PAB	I/O interrupt
354	–	–
355	–	–
356	–	–
357	WAA	Memory master clear on
360	WAB	Memory master clear off
361	WAC	Memory access master clear on
362	WAD	Memory access master clear off
363	WAE	CPU master clear on
364	WAF	CPU master clear off
365	WAI	Memory sanity code on
366	WAJ	Memory sanity code off
367	WAK	I/O sanity code on
370	WAL	I/O sanity code off
371	WAQ	Reset to default configuration
372	WBH	Logic monitor reset
373	WCA	CPU master clear
374	WCB	Memory access master clear
375	WCE	Memory master clear
376	WDC	CPU stack inverted
377	WGI	Reset chip/counters

IC Option (Revision 5001)

Test Point	Term	Description
200	qmr	Wait fetch words 0 – 3
201	qnh	4 fetch words valid
202	–	–
203	–	–
204	–	–
205	–	–
206	qeb	Exchange active
207	rba	Data resume
210	–	–
211	–	–
212	–	–

213	–	–
214	–	–
215	–	–
216	–	–
217	–	–
220	mdi	Enter P/dump mode
221	mdk	Go branch/parcel pointers
222	mbj	CM path 1 code valid
223	mbl	CM path 2 code valid
224	–	–
225	–	–
226	–	–
227	–	–
230	–	–
231	–	–
232	–	–
233	–	–
234	–	–
235	–	–
236	–	–
237	–	–
240	–	–
241	–	–
242	–	–
243	–	–
244	qya	Conditional branch
245	qzb	Branch indirect first half
246	tbq	Data ready
247	qzd	Branch indirect second half
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–
255	–	–
256	–	–
257	–	–
260	–	–
261	–	–
262	–	–
263	–	–

264	–	–
265	–	–
266	–	–
267	–	–
270	meq	Fetch requests/exchange enable
271	mer	Go dump
272	mes	Load pointers
273	–	–
274	–	–
275	–	–
276	–	–
277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–
311	–	–
312	–	–
313	–	–
314	qjg	Fetch active
315	qqa	Enable first ready
316	qqe	Buffer data valid
317	qql	Branch sequence active
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–

335	–	–
336	–	–
337	–	–
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	qsc	Prefetch sequence
375	qtb	Read done sequence
376	qwa	Jump to B sequence
377	qxi	Jump to constant sequence

JA Option (Revision 3025)

Test Point	Term	Description
200	jza	Vector logical 1 or 2 busy
201	jzb	Vector shift busy

202	jzc	Vector adder busy
203	jzd	Vector floating multiply busy
204	jze	Vector floating add busy
205	jzf	Vector reciprocal busy
206	jzg	Vector matrix multiply busy
207	jzh	Block B or T busy
210	–	–
211	–	–
212	–	–
213	–	–
214	–	–
215	–	–
216	–	–
217	–	–
220	jzi	Common memory port A busy
221	jzj	Common memory port B busy
222	jzk	Common memory port C busy
223	jzl	Shared path busy
224	jzm	Exit resources busy
225	jzn	Exit resources busy
226	jzo	Exit resources busy
227	jzp	Vector mask busy
230	–	–
231	ksc	Hold CM issue
232	ksf	CM quiet
233	–	–
234	ksi	Cache miss active
235	ksl	Reads quiet
236	kso	Writes quiet
237	–	–
240	–	–
241	–	–
242	–	–
243	–	–
244	–	–
245	–	–
246	–	–
247	–	–
250	jdi	A0 busy
251	jdj	A1 busy
252	jdk	A2 busy

253	jdl	A3 busy
254	jdm	A4 busy
255	jdn	A5 busy
256	jdo	A6 busy
257	jdp	A7 busy
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	jei	S0 busy
271	jej	S1 busy
272	jek	S2 busy
273	jel	S3 busy
274	jem	S4 busy
275	jen	S5 busy
276	jeo	S6 busy
277	jep	S7 busy
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	jai	V0 read busy
311	jaj	V1 read busy
312	jak	V2 read busy
313	jal	V3 read busy
314	jam	V4 read busy
315	jan	V5 read busy
316	jao	V6 read busy
317	jap	V7 read busy
320	–	–
321	–	–
322	–	–
323	–	–

324	–	–
325	–	–
326	–	–
327	–	–
330	jbi	V0 write busy
331	jbj	V1 write busy
332	jbk	V2 write busy
333	jbl	V3 write busy
334	jbm	V4 write busy
335	jbn	V5 write busy
336	jbo	V6 write busy
337	jbp	V7 write busy
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–

375	–	–
376	–	–
377	–	–

SS Option (Revision 1022)

Test Point	Term	Description
200	qaf	Enter VM
201	qag	Read VM
202	–	–
203	–	–
204	–	–
205	–	–
206	–	–
207	–	–
210	–	–
211	–	–
212	–	–
213	–	–
214	–	–
215	–	–
216	–	–
217	–	–
220	–	–
221	–	–
222	qba	Gate VM (146/147)
223	qbb	Advance VM readout (146/147)
224	–	–
225	–	–
226	–	–
227	–	–
230	–	–
231	–	–
232	–	–
233	–	–
234	–	–
235	–	–
236	–	–
237	–	–
240	–	–
241	–	–

242	–	–
243	–	–
244	qca	Clear VM (175)
245	qda	Set VM even bit (175)
246	qdb	Advance VM entry pointer (175)
247	qdc	Set VM odd bit (175)
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–
255	–	–
256	–	–
257	–	–
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	qjb	Go population count
271	qjc	Go parity
272	qjd	Go leading zero
273	–	–
274	–	–
275	–	–
276	–	–
277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–
311	–	–
312	–	–

313	–	–
314	qeb	Go double shift
315	qfe	H0 bit
316	pii	Go A type
317	qna	Go Iota
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–
337	–	–
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–

364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	xzz	Any test point active

VA Option (Revision 3001)

Test Point	Term	Description
200	paq	G bit 0
201	par	G bit 1
202	pas	G bit 2
203	pat	G bit 3
204	psj	140 – 147, 175
205	ptc	150 – 157
206	pud	160 – 167, 170 – 173
207	pvz	070*ij*1, 174
210	–	–
211	–	–
212	–	–
213	–	–
214	–	–
215	–	–
216	–	–
217	–	–
220	pyq	Issue
221	pob	076*ijk*
222	ppb	077*ijk*
223	pqb	00200*k*
224	prl	17*x*
225	PYI	CM port A conflict
226	prg	CM port B conflict
227	prh	CM port C conflict
230	–	–

231	–	–
232	–	–
233	–	–
234	–	–
235	–	–
236	–	–
237	–	–
240	–	–
241	–	–
242	–	–
243	–	–
244	–	–
245	–	–
246	–	–
247	–	–
250	rac	Read active V0
251	rbc	Read active V1
252	rcc	Read active V2
253	rdc	Read active V3
254	ric	Write active V0
255	rjc	Write active V1
256	rkc	Write active V2
257	rlc	Write active V3
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	rec	Read active V4
271	rfc	Read active V5
272	rgc	Read active V6
273	rhc	Read active V7
274	rmc	Write active V4
275	rnc	Write active V5
276	roc	Write active V6
277	rpc	Write active V7
300	–	–
301	–	–

302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–
311	–	–
312	–	–
313	–	–
314	qqi	End vector V0
315	qqj	End vector V1
316	qqk	End vector V2
317	qql	End vector V3
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	qqm	End vector V4
335	qqn	End vector V5
336	qqo	End vector V6
337	qqp	End vector V7
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–

353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	–	–

VF Option (Revision 3006)

Test Point	Term	Description
200	uax	VL number 1 data valid
201	ubw	VL number 2 data valid
202	ucw	V adder data valid
203	udw	V shift data valid
204	–	–
205	–	–
206	–	–
207	–	–
210	–	–
211	–	–
212	–	–
213	–	–
214	–	–
215	–	–
216	–	–
217	–	–

220	uew	FM data valid
221	ufx	FA data valid
222	ugw	Reciprocal data valid
223	uhx	MM data valid
224	–	–
225	–	–
226	–	–
227	–	–
230	–	–
231	–	–
232	–	–
233	–	–
234	–	–
235	–	–
236	–	–
237	–	–
240	uiw	CM port A data valid
241	ujw	CM port B data valid
242	ukw	CM port C data valid
243	–	–
244	pnb	140 – 147 logical 1
245	pod	140 – 145 logical 2
246	ppb	154 – 157
247	pqb	150 – 153
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–
255	–	–
256	–	–
257	–	–
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	prb	160 – 167

271	psb	170 – 173
272	ptb	174*xx* 0 – 3
273	pub	174*xx* 4 – 7
274	–	–
275	–	–
276	–	–
277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–
311	–	–
312	–	–
313	–	–
314	qia	Go write V0
315	qib	Go write V1
316	qic	Go write V2
317	qid	Go write V3
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	qie	Go write V4
335	qif	Go write V5
336	qig	Go write V6
337	qih	Go write V7
340	–	–
341	–	–

342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	–	–

VM Option (Revision 1023)

Test Point	Term	Description
200	pma	CM read
201	pna	170 – 173 issued
202	poa	160 – 167 issued
203	ppa	150 – 153 issued
204	–	–
205	–	–
206	–	–

207	–	–
210	–	–
211	–	–
212	–	–
213	–	–
214	–	–
215	–	–
216	–	–
217	–	–
220	pia	V*i* bit 0
221	pib	V*i* bit 1
222	pic	V*i* bit 2
223	pbb	Issue
224	–	–
225	–	–
226	–	–
227	–	–
230	–	–
231	–	–
232	–	–
233	–	–
234	–	–
235	–	–
236	–	–
237	–	–
240	–	–
241	–	–
242	–	–
243	–	–
244	qca	CM path 1 code bit 0
245	qcb	CM path 1 code bit 1
246	qcc	CM path 1 code bit 2
247	qcd	CM path 1 code valid
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–
255	–	–
256	–	–
257	–	–

260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	qda	CM path 2 code bit 0
271	qdb	CM path 2 code bit 1
272	qdc	CM path 2 code bit 2
273	qdd	CM path 2 code valid
274	–	–
275	–	–
276	–	–
277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–
311	–	–
312	–	–
313	–	–
314	pra	174 (k = 0 – 3) issued
315	psa	154 – 157 issued
316	pta	174 (k = 4 – 7) issued
317	–	–
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–

331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–
337	–	–
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	pua	VL number 1
376	pva	VL number 2
377	xzz	Any test point active

VR Option (Revision 1033)

Test Point	Term	Description
200	pbb	Issue
201	–	–
202	–	–
203	–	–
204	–	–
205	–	–
206	mxg	VR parity error
207	mxi	External input monitor
210	–	–
211	–	–
212	–	–
213	–	–
214	–	–
215	–	–
216	–	–
217	–	–
220	–	–
221	–	–
222	pme	CM gather port A
223	pmf	CM gather port B
224	–	–
225	–	–
226	–	–
227	–	–
230	–	–
231	–	–
232	–	–
233	–	–
234	–	–
235	–	–
236	–	–
237	–	–
240	–	–
241	–	–
242	–	–
243	–	–
244	pna	170 – 173 issued
245	poa	160 – 167 issued

246	–	–
247	–	–
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–
255	–	–
256	–	–
257	–	–
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	ppa	150 – 153 issued
271	pqa	076 issued
272	–	–
273	–	–
274	–	–
275	–	–
276	–	–
277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–
311	–	–
312	–	–
313	–	–
314	pra	174 (k = 0 – 3) issued
315	pta	174 (k = 4 – 7) issued
316	–	–

317	–	–
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–
337	–	–
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–

370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	xzz	Any test point active

IEEE CPU Module (CPE1) Test Points

This section lists the test points that are built into the options on the IEEE CPU module. A brief description of each option is also included.

NOTE: The following IEEE CPU module options do not have test points: FC, HI, NE, NF, NG, NH, RD, and RE.

AV Option (Revision 1003)

Test Point	Term	Description
200	qaa	A entry from B
201	qab	A entry from adder
202	qac	A entry from population/parity/leading zero
203	qad	A entry from multiply
204	–	–
205	–	–
206	–	–
207	–	–
210	–	–
211	–	–
212	–	–
213	–	–
214	–	–
215	–	–
216	–	–
217	–	–
220	–	–
221	–	–
222	qaf	A entry from shift
223	qai	A entry from VM
224	–	–
225	–	–
226	–	–
227	–	–
230	–	–
231	–	–
232	–	–
233	–	–
234	–	–
235	–	–
236	–	–

237	–	–
240	–	–
241	–	–
242	–	–
243	–	–
244	qea	S entry from shift
245	qeb	S entry from T
246	qec	S entry from adder
247	qed	S entry from V*j*
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–
255	–	–
256	–	–
257	–	–
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	qee	S entry from FA
271	qef	S entry from FM
272	qeg	S entry from reciprocal
273	qeh	S entry from VM
274	–	–
275	–	–
276	–	–
277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–

310	–	–
311	–	–
312	–	–
313	–	–
314	qei	S entry from MM
315	–	–
316	–	–
317	–	–
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–
337	–	–
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–

361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	xzz	Any test point active

AW Option (Revision 1004)

Test Point	Term	Description
200	qaa	A entry from B
201	qab	A entry from adder
202	qac	A entry from population/parity/leading zero
203	qad	A entry from multiply
204	–	–
205	–	–
206	–	–
207	–	–
210	–	–
211	–	–
212	–	–
213	–	–
214	–	–
215	–	–
216	–	–
217	–	–
220	–	–
221	–	–
222	qaf	A entry from shift
223	qai	A entry from VM
224	–	–
225	–	–

226	–	–
227	–	–
230	–	–
231	–	–
232	–	–
233	–	–
234	–	–
235	–	–
236	–	–
237	–	–
240	–	–
241	–	–
242	–	–
243	–	–
244	qea	S entry from shift
245	qeb	S entry from T
246	qec	S entry from adder
247	qed	S entry from V*j*
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–
255	–	–
256	–	–
257	–	–
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	qee	S entry from FA
271	qef	S entry from FM
272	qeg	S entry from reciprocal
273	qeh	S entry from VM
274	–	–
275	–	–
276	–	–

277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–
311	–	–
312	–	–
313	–	–
314	qei	S entry from MM
315	–	–
316	–	–
317	–	–
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–
337	–	–
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–

350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	xzz	Any test point active

AX Option (Revision 1003)

Test Point	Term	Description
200	qaa	A entry from B
201	qab	A entry from Adder
202	qac	A entry from population/parity/leading zero
203	qad	A entry from multiply
204	–	–
205	–	–
206	–	–
207	–	–
210	–	–
211	–	–
212	–	–
213	–	–
214	–	–

215	–	–
216	–	–
217	–	–
220	–	–
221	–	–
222	qaf	A entry from shift
223	qai	A entry from VM
224	–	–
225	–	–
226	–	–
227	–	–
230	–	–
231	–	–
232	–	–
233	–	–
234	–	–
235	–	–
236	–	–
237	–	–
240	–	–
241	–	–
242	–	–
243	–	–
244	qea	S entry from shift
245	qeb	S entry from T
246	qec	S entry from adder
247	qed	S entry from V*j*
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–
255	–	–
256	–	–
257	–	–
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–

266	–	–
267	–	–
270	qee	S entry from FA
271	qef	S entry from FM
272	qeg	S entry from divide
273	qeh	S entry from VM
274	–	–
275	–	–
276	–	–
277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–
311	–	–
312	–	–
313	–	–
314	qei	S entry from MM
315	–	–
316	–	–
317	–	–
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–

337	–	–
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	xzz	Any test point active

AY Option (Revision 1003)

Test Point	Term	Description
200	qaa	A entry from B
201	qab	A entry from Adder
202	qac	A entry from population/parity/leading zero
203	qad	A entry from multiply

204	–	–
205	–	–
206	–	–
207	–	–
210	–	–
211	–	–
212	–	–
213	–	–
214	–	–
215	–	–
216	–	–
217	–	–
220	–	–
221	–	–
222	qaf	A entry from shift
223	qai	A entry from VM
224	–	–
225	–	–
226	–	–
227	–	–
230	–	–
231	–	–
232	–	–
233	–	–
234	–	–
235	–	–
236	–	–
237	–	–
240	–	–
241	–	–
242	–	–
243	–	–
244	qea	S entry from shift
245	qeb	S entry from T
246	qec	S entry from adder
247	qed	S entry from V*j*
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–

255	–	–
256	–	–
257	–	–
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	qee	S entry from FA
271	qef	S entry from FM
272	qeg	S entry from reciprocal
273	qeh	S entry from VM
274	–	–
275	–	–
276	–	–
277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–
311	–	–
312	–	–
313	–	–
314	qei	S entry from MM
315	–	–
316	–	–
317	–	–
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–

326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–
337	–	–
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–

376	–	–
377	xzz	Any test point active

BU Option (Revision 1007)

Test Point	Term	Description
200	qpa	Enter new P
201	qqc	Advance P
202	–	–
203	–	–
204	–	–
205	–	–
206	mgh	Parity error
207	–	–
210	–	–
211	–	–
212	–	–
213	–	–
214	–	–
215	–	–
216	–	–
217	–	–
220	–	–
221	–	–
222	qac	B read (005/024)
223	qbb	B write (025)
224	–	–
225	–	–
226	–	–
227	–	–
230	–	–
231	–	–
232	–	–
233	–	–
234	–	–
235	–	–
236	–	–
237	–	–
240	–	–
241	–	–
242	–	–

243	–	–
244	qbj	Return jump (007)
245	qcc	T read (074)
246	qdb	T write (075)
247	–	–
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–
255	–	–
256	–	–
257	–	–
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	qkc	Go 150 – 153
271	qlc	Go 160, 161, 165, 166, 170 – 173
272	qmc	Go 174*xxx*
273	–	–
274	–	–
275	–	–
276	–	–
277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–
311	–	–
312	–	–
313	–	–

314	qef	Block B read (034)
315	qff	Block B write (035)
316	qgf	Block T read (036)
317	qhf	Block T write (037)
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–
337	–	–
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–

365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	xzz	Any test point active

HH Option (Revision 1017)

Test Point	Term	Description
200	TOA	Exchange interrupt mode registers FNX
201	TOB	Exchange interrupt mode registers IMI
202	TOC	Exchange interrupt mode registers IDL
203	TOD	Exchange interrupt mode registers IPC
204	TOE	Exchange interrupt mode registers IIO
205	TOF	Exchange interrupt mode registers IIP
206	TOG	Exchange interrupt mode registers IRT
207	TOH	Exchange interrupt mode registers IMC
210	TOI	Exchange interrupt mode registers ICM
211	TOJ	Exchange interrupt mode registers IBP
212	TOK	Exchange interrupt mode registers FEX
213	TOL	Exchange interrupt mode registers IPR
214	TOM	Exchange interrupt mode registers IOR
215	TOT	Exchange interrupt mode registers IOV
216	TOO	Exchange interrupt mode registers IUM
217	TOP	Exchange interrupt mode registers IRP
220	TOQ	Exchange interrupt mode registers IAM
221	TSQ	Exchange interrupt flag registers AMI
222	SPE	Accepting I/O interrupts
223	TQD	Interrupt flag holding registers PCI
224	SRA	Enable interrupt mode
225	TQF	Interrupt flag holding registers ICP
226	TQG	Interrupt flag holding registers RTI
227	TQH	Interrupt flag holding registers MCU
230	TQI	Interrupt flag holding registers MEC
231	TQJ	Interrupt flag holding registers BPI

232	REU	Carry into real–time clock
233	REZ	Carry out of real–time clock
234	TQM	Interrupt flag holding registers ORE
235	TQU	Interrupt flag holding registers UNF
236	TQO	Interrupt flag holding registers MEU
237	TQP	Interrupt flag holding registers RPE
240	TSA	Exchange interrupt flag registers NEX
241	TSB	Exchange interrupt flag registers MII
242	TSC	Exchange interrupt flag registers DL
243	TSD	Exchange interrupt flag registers PCI
244	TSE	Exchange interrupt flag registers IOI
245	TSF	Exchange interrupt flag registers ICP
246	TSG	Exchange interrupt flag registers RTI
247	TSH	Exchange interrupt flag registers MCU
250	TSI	Exchange interrupt flag registers MEC
251	TSJ	Exchange interrupt flag registers BPI
252	TSK	Exchange interrupt flag registers EEX
253	TSL	Exchange interrupt flag registers PRE
254	TSM	Exchange interrupt flag registers ORE
255	TSV	Exchange interrupt flag registers NX
256	TSO	Exchange interrupt flag registers MEU
257	TSP	Exchange interrupt flag registers RPE
260	SHA	Exchange mode bit register MM
261	SHB	Exchange mode bit register BDM
262	SHC	Exchange mode bit register ESL
263	SHJ	Exchange status bit register RM0
264	SHE	Exchange status bit register BML
265	SHF	Exchange status bit register WS
266	SHK	Exchange status bit register RM1
267	SHH	Exchange status bit register VNU
270	SHP	Exchange mode bit register SCE
271	LAG	Set dirty bits from CB0
272	LBC	Set dirty bits from CB0 cell counter bit 2
273	HAP	Performance monitor update/readout pointer bit 0
274	HAQ	Performance monitor update/readout pointer bit 1
275	HAR	Performance monitor update/readout pointer bit 2
276	HAS	Performance monitor update/readout pointer bit 3
277	HAT	Performance monitor update/readout pointer bit 4
300	TTH	Error exchange request
301	TTI	Error or exit exchange request
302	TTJ	Deadstart exchange request

303	TTO	Block I/O for exchange request
304	TUF	Go exchange from JA
305	TUK	Exchange reads complete
306	TUV	Clear SIE bit (taking I/O interrupt)
307	TUW	Allow HPM, and dirty bit entry
310	TVD	Waiting on semaphore test and set instruction (0034*jk*)
311	TVG	Release required for test and set
312	TVI	Semaphore was set (test and set successful)
313	TVL	Flush command outstanding
314	TVV	Flush response from shared (tapped off in middle of filter)
315	hii	Performance monitor blank registers to zero
316	glz	Performance monitor go increment
317	GOZ	Performance monitor carry out
320	DBI	Release S*i*
321	DBJ	Enter S*i*
322	DBK	Release A*i*
323	DBL	Enter A*i*
324	DBD	*i*,*j* designator bit 0
325	DBE	*i*,*j* designator bit 0
326	DBF	*i*,*j* designator bit 0
327	DCB	Release shared path
330	LFI	Cache invalidate CPU dcd 76 phase 2
331	CFB	0016*j*3, 0016*j*[4 – 7], 0013*jk*
332	CFC	0016[1–3]0, 0016[5–7]0, 0014*j*[1–7]
333	LFJ	Cache invalidate CLN DCD 77 phase 2
334	CFE	0015*jk*,0017*jk*
335	CFF	002[0 – 6]*jk*
336	DQD	Floating point error FA pipe 0
337	DRD	Floating point error FA pipe 1
340	CFZ	Valid
341	CFK	072*i*00, 073*ij*1
342	CFL	073*ij*5
343	CFM	023*ij*6, 023*ij*7, 027*ij*2, 027*ij*3
344	CGA	001000
345	CGB	0010*jk*, 0011*jk*, 0012*jk*
346	CGD	001600
347	CGE	0034*jk*, 0036*jk*, 0037*jk*
350	CGF	0064*jk*
351	CGG	026*ij*4, 026*ij*5, 026*ij*6, 026*ij*7
352	CGH	033*ijk*
353	CGI	027*ij*6, 027*ij*7

354	CGJ	072*i*02, 072*ij*3, 072*ij*6
355	CGK	073*i*02, 073*ij*3, 073*ij*6
356	CIQ	A*i* release code 20 – 23, 40 – 41 from shared
357	CIR	S*i* release code 31, 44 from shared
360	LGF	First enter RTC
361	LJA	Invalidate cache
362	RFA	RTC bit 0
363	RFF	RTC bit 5
364	RFL	RTC bit 11
365	RFR	RTC bit 17
366	RFX	RTC bit 23
367	HUB	Performance monitor busy flag
370	WFB	Performance monitor diagnostic mode (code 162)
371	RPY	Exchange status bit register BDD
372	CGC	0014*j*0,001600
373	SHI	Exchange status bit register SSB
374	DSD	Floating point error fm pipe 0
375	DTD	Floating point error fm pipe 1
376	DUB	Floating point error divide/square root pipe 0
377	DVB	Floating point error divide/square root pipe 1

JB Option (Revision 1018)

Test Point	Term	Description
200	jza	Vector logical 1 or 2 busy
201	jzb	Vector shift busy
202	jzc	Vector adder busy
203	jzd	Vector floating multiply busy
204	jze	Vector floating add busy
205	jzf	Vector divide busy
206	jzg	Vector matrix multiply busy
207	jzh	Block B or T busy
210	–	–
211	–	–
212	–	–
213	–	–
214	–	–
215	–	–
216	–	–
217	–	–
220	jzi	Common memory port A busy

221	jzj	Common memory port B busy
222	jzk	Common memory port C busy
223	jzl	Shared path busy
224	jzm	Exit resources busy
225	jzn	Exit resources busy
226	jzo	Exit resources busy
227	jzp	Vector mask busy
230	–	–
231	ksc	Hold CM issue
232	ksf	CM quiet
233	–	–
234	ksi	Cache miss active
235	ksl	Reads quiet
236	kso	Writes quiet
237	–	–
240	–	–
241	–	–
242	–	–
243	–	–
244	–	–
245	–	–
246	–	–
247	–	–
250	jdi	A0 busy
251	jdj	A1 busy
252	jdk	A2 busy
253	jdl	A3 busy
254	jdm	A4 busy
255	jdn	A5 busy
256	jdo	A6 busy
257	jdp	A7 busy
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	jei	S0 busy
271	jej	S1 busy

272	jek	S2 busy
273	jel	S3 busy
274	jem	S4 busy
275	jen	S5 busy
276	jeo	S6 busy
277	jep	S7 busy
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	jai	V0 read busy
311	jaj	V1 read busy
312	jak	V2 read busy
313	jal	V3 read busy
314	jam	V4 read busy
315	jan	V5 read busy
316	jao	V6 read busy
317	jap	V7 read busy
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	jbi	V0 write busy
331	jbj	V1 write busy
332	jbk	V2 write busy
333	jbl	V3 write busy
334	jbm	V4 write busy
335	jbn	V5 write busy
336	jbo	V6 write busy
337	jbp	V7 write busy
340	–	–
341	–	–
342	–	–

343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	–	–

VB Option (Revision 1007)

Test Point	Term	Description
200	paq	G bit 0
201	par	G bit 1
202	pas	G bit 2
203	pat	G bit 3
204	psj	140 – 147, 175
205	ptc	150 – 157
206	pud	160 – 167, 170 – 173
207	pvz	070*ij*1, 174

210	–	–
211	–	–
212	–	–
213	–	–
214	–	–
215	–	–
216	–	–
217	–	–
220	pyq	Issue
221	pob	076*ijk*
222	ppb	077*ijk*
223	pqb	00200*k*
224	prl	17*x*
225	PYI	CM port A conflict
226	prg	CM port B conflict
227	prh	CM port C conflict
230	–	–
231	–	–
232	–	–
233	–	–
234	–	–
235	–	–
236	–	–
237	–	–
240	–	–
241	–	–
242	–	–
243	–	–
244	–	–
245	–	–
246	–	–
247	–	–
250	rac	Read active V0
251	rbc	Read active V1
252	rcc	Read active V2
253	rdc	Read active V3
254	ric	Write active V0
255	rjc	Write active V1
256	rkc	Write active V2
257	rlc	Write active V3
260	–	–

261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	rec	Read active V4
271	rfc	Read active V5
272	rgc	Read active V6
273	rhc	Read active V7
274	rmc	Write active V4
275	rnc	Write active V5
276	roc	Write active V6
277	rpc	Write active V7
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–
311	–	–
312	–	–
313	–	–
314	qqi	End vector V0
315	qqj	End vector V1
316	qqk	End vector V2
317	qql	End vector V3
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–

332	–	–
333	–	–
334	qqm	End vector V4
335	qqn	End vector V5
336	qqo	End vector V6
337	qqp	End vector V7
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	–	–

VE Option (Revision 1005)

Test Point	Term	Description
200	uax	VL number 1 data valid
201	ubw	VL number 2 data valid
202	ucw	V adder data valid
203	udw	V shift data valid
204	–	–
205	–	–
206	–	–
207	–	–
210	–	–
211	–	–
212	–	–
213	–	–
214	–	–
215	–	–
216	–	–
217	–	–
220	uew	FM data valid
221	ufx	FA data valid
222	ugw	Reciprocal data valid
223	uhx	MM data valid
224	–	–
225	–	–
226	–	–
227	–	–
230	–	–
231	–	–
232	–	–
233	–	–
234	–	–
235	–	–
236	–	–
237	–	–
240	UIW	CM port A data valid
241	UJW	CM port B data valid
242	UKW	CM port C data valid
243	–	–
244	pnb	140 – 147 logical 1
245	pod	140 – 145 logical 2

246	ppb	154 – 157
247	pqb	150 – 153
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–
255	–	–
256	–	–
257	–	–
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	prb	160, 161, 165, 166
271	psb	170 – 173, 164
272	ptb	174*xx* 0 – 3
273	pub	174*xx* 4 – 6
274	–	–
275	–	–
276	–	–
277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–
311	–	–
312	–	–
313	–	–
314	qia	Go write V0
315	qib	Go write V1
316	qic	Go write V2

317	qid	Go write V3
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	qie	Go write V4
335	qif	Go write V5
336	qig	Go write V6
337	qih	Go write V7
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–

370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	–	–

VN Option (Revision 1005)

Test Point	Term	Description
200	pma	CM read
201	pna	170 – 173, 167, 164 compare issued
202	poa	160, 161, 165 – 166 issued
203	ppa	150 – 153 issued
204	–	–
205	–	–
206	–	–
207	–	–
210	–	–
211	–	–
212	–	–
213	–	–
214	–	–
215	–	–
216	–	–
217	–	–
220	pia	V*i* bit 0
221	pib	V*i* bit 1
222	pic	V*i* bit 2
223	pbb	Issue
224	–	–
225	–	–
226	–	–
227	–	–
230	–	–
231	–	–
232	–	–
233	–	–
234	–	–

235	–	–
236	–	–
237	–	–
240	–	–
241	–	–
242	–	–
243	–	–
244	qca	CM path 1 code bit 0
245	qcb	CM path 1 code bit 1
246	qcc	CM path 1 code bit 2
247	qcd	CM path 1 code valid
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–
255	–	–
256	–	–
257	–	–
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	qda	CM path 2 code bit 0
271	qdb	CM path 2 code bit 1
272	qdc	CM path 2 code bit 2
273	qdd	CM path 2 code valid
274	–	–
275	–	–
276	–	–
277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–

306	–	–
307	–	–
310	–	–
311	–	–
312	–	–
313	–	–
314	pra	174 (k = 0 – 3) issued
315	psa	154 – 157 issued
316	pta	174 (k = 4 – 7) issued
317	pri	162, 163 issued
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–
337	–	–
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–

357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	pua	VL number 1
376	pva	VL number 2
377	xzz	Any test point active

VQ Option (Revision 1004)

Test Point	Term	Description
200	pbb	Issue
201	–	–
202	–	–
203	–	–
204	–	–
205	–	–
206	mxg	VR parity error
207	mxi	External input monitor
210	–	–
211	–	–
212	–	–
213	–	–
214	–	–
215	–	–
216	–	–
217	–	–
220	–	–
221	–	–
222	pme	CM gather port A
223	pmf	CM gather port B

224	–	–
225	–	–
226	–	–
227	–	–
230	–	–
231	–	–
232	–	–
233	–	–
234	–	–
235	–	–
236	–	–
237	–	–
240	–	–
241	–	–
242	–	–
243	–	–
244	pna	170 – 173, 164, 167 compare issued
245	poa	160, 161, 165 – 166 issued
246	–	–
247	–	–
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–
255	–	–
256	–	–
257	–	–
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	ppa	150 – 153 issued
271	pqa	076 issued
272	–	–
273	–	–
274	–	–

275	–	–
276	–	–
277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–
311	–	–
312	–	–
313	–	–
314	pra	174 (k = 0 – 3) issued
315	pta	174 (k = 4 – 7) issued
316	–	–
317	–	–
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–
337	–	–
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–

346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	xzz	Any test point active

I/O Module (IO01) Test Points

This section lists the test points that are built into the options on IO01 modules. A brief description of each option is also included.

DA Option (Revision 1024)

Test Point	Term	Description
200	CK00	Partial syndrome bits 0
201	CK01	Partial syndrome bits 1
202	CK02	Partial syndrome bits 2
203	CK03	Partial syndrome bits 3
204	CK04	Partial syndrome bits 4
205	CK05	Partial syndrome bits 5
206	CK06	Partial syndrome bits 6
207	CK07	Partial syndrome bits 7
210	CL10	Syndrome bit 0
211	CL11	Syndrome bit 1
212	CL12	Syndrome bit 2
213	CL13	Syndrome bit 3
214	CL14	Syndrome bit 4
215	CL15	Syndrome bit 5
216	CL16	Syndrome bit 6
217	CL17	Syndrome bit 7
220	EBR	Stack data
221	EBB	Hold data rank B
222	EER	Read stacked data
223	ED10	Read pointer
224	EFA	Data valid
225	EFB	Go write reference
226	–	–
227	EBC	Hold data rank C
230	EBD	Hold data rank D
231	EIB	Data readout select
232	FCA	Serial input
233	FCH	SECDED correct off
234	FCJ	Go readout – support channel
235	FIA	Support channel command
236	FCF	Go shift
237	–	–
240	EJB	First go write

241	EKB	Even/odd reference counter
242	EMB	Use alternate checkbits
243	–	–
244	EMA	Alternate checkbit mode
245	–	–
246	–	–
247	–	–
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–
255	–	–
256	–	–
257	–	–
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	–	–
271	–	–
272	–	–
273	–	–
274	–	–
275	–	–
276	–	–
277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–
311	–	–

312	–	–
313	–	–
314	–	–
315	–	–
316	–	–
317	–	–
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	VB00	Support channel serial bit counter
331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	XF00	Syndrome bit 0
337	XF01	Check bit 1
340	XF02	Syndrome bit 2
341	XF03	Check bit 3
342	XF04	Syndrome bit 4
343	XF05	Check bit 5
344	XF06	Syndrome bit 6
345	XF07	Check bit 7
346	XG00	Syndrome bit 0
347	XG01	Syndrome bit 1
350	XG02	Syndrome bit 2
351	XG03	Syndrome bit 3
352	XG04	Syndrome bit 4
353	XG05	Syndrome bit 5
354	XG06	Syndrome bit 6
355	XG07	Syndrome bit 7
356	XM31	Memory to I/O support channel
357	–	–
360	YGA	ECC off for VHISP
361	YGB	ECC off for VHISP
362	–	–

363	YGJ	Alternate checkbit mode VHISP
364	YGK	Alternate checkbit mode HISP0
365	YGL	Alternate checkbit mode HISP1
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	–	–

DB Option (Revision 2001)

Test Point	Term	Description
200	AG0	DD option (I/O request/response channel bit 0)
201	AG1	DD option (I/O request/response channel bit 1)
202	AG2	DD option (I/O request/response channel bit 2)
203	AG3	DD option (I/O request/response channel bit 3)
204	AG4	DD option (I/O request/response channel bit 4)
205	AG5	DD option (I/O request/response channel bit 5)
206	AG6	DD option (I/O request/response channel bit 6)
207	AG7	DD option (I/O request/response channel bit 7)
210	AG8	DD option (I/O request/response channel bit 8)
211	AG9	DD option (I/O request/response channel bit 9)
212	AG10	DD option (I/O request/response channel bit 10)
213	AG11	DD option (I/O request/response channel bit 11)
214	AG12	DD option (I/O request/response channel bit 12)
215	AG13	DD option (I/O request/response channel bit 13)
216	AG14	DD option (I/O request/response channel bit 14)
217	AG15	DD option (I/O request/response channel bit 15)
220	AG16	DD option (I/O request/response channel bit 16)
221	AG17	DD option (I/O request/response channel bit 17)
222	AG18	DD option (I/O request/response channel bit 18)
223	AG19	DD option (I/O request/response channel bit 19)
224	BDA	DD option (go write)
225	FDA	DD option (go read)
226	HDA	DD option (go interrupt/033*ijk*)
227	BDR	DD option (permission to write)

230	BAB	DD option (enter write parcel 0)
231	BAR	DD option (enter write parcel 2)
232	BEA	DD option (select write parcel 0)
233	BEH	DD option (select write parcel 1)
234	FAB	DD option (enter read parcel 0)
235	FAR	DD option (enter read parcel 2)
236	FEA	DD option (select read parcel 0)
237	FEH	DD option (select read parcel 1)
240	AO0	DE option (I/O request/response channel bit 0)
241	AO1	DE option (I/O request/response channel bit 1)
242	AO2	DE option (I/O request/response channel bit 2)
243	AO3	DE option (I/O request/response channel bit 3)
244	AO4	DE option (I/O request/response channel bit 4)
245	AO5	DE option (I/O request/response channel bit 5)
246	AO6	DE option (I/O request/response channel bit 6)
247	AO7	DE option (I/O request/response channel bit 7)
250	AO8	DE option (I/O request/response channel bit 8)
251	AO9	DE option (I/O request/response channel bit 9)
252	AO10	DE option (I/O request/response channel bit 10)
253	AO11	DE option (I/O request/response channel bit 11)
254	AO12	DE option (I/O request/response channel bit 12)
255	AO13	DE option (I/O request/response channel bit 13)
256	AO14	DE option (I/O request/response channel bit 14)
257	AO15	DE option (I/O request/response channel bit 15)
260	AO16	DE option (I/O request/response channel bit 16)
261	AO17	DE option (I/O request/response channel bit 17)
262	AO18	DE option (I/O request/response channel bit 18)
263	AO19	DE option (I/O request/response channel bit 19)
264	BDI	DE option (go write)
265	FDI	DE option (go read)
266	HDI	DE option (go interrupt/033*ijk*)
267	BDV	DE option (permission to write)
270	BBB	DE option (enter write parcel 0)
271	BBR	DE option (enter write parcel 2)
272	BFA	DE option (select write parcel 0)
273	BFH	DE option (select write parcel 1)
274	FBB	DE option (enter read parcel 0)
275	FBR	DE option (enter read parcel 2)
276	FFA	DE option (select read parcel 0)
277	FFH	DE option (select read parcel 1)
300	HAB	DD option (enter interrupt/033*ijk* parcel 0)

301	HAV	DD option (enter interrupt/033*ijk* parcel 3)
302	HEA	DD option (select interrupt/033*ijk* parcel 0)
303	HEH	DD option (select interrupt/033*ijk* parcel 1)
304	HBB	DE option (enter interrupt/033*ijk* parcel 3)
305	HBV	DE option (enter interrupt/033*ijk* parcel 3)
306	HFA	DE option (select interrupt/033*ijk* parcel 0)
307	HFH	DE option (select interrupt/033*ijk* parcel 1)
310	PAB	Load block DD length
311	PAI	Load block DE length
312	PBA	Allow DD read
313	PBE	Allow DE read
314	PBI	Allow DD write
315	PBM	Allow DE write
316	PBQ	Allow DD interrupt/033ijk
317	PBU	Allow DE interrupt/033ijk
320	QB4	Write block length counter bit 4
321	QB3	Write block length counter bit 3
322	QB2	Write block length counter bit 2
323	QB1	Write block length counter bit 1
324	QB0	Write block length counter bit 0
325	BQA	Rank A busy
326	QAA	Data valid
327	QJA	Enable 4 CP check
330	QJQ	4 CP write
331	QC10	Parcel pointer 2^0 – rank A
332	QC11	Parcel pointer 2^1 – rank A
333	QCB	Parcel pointer = null
334	QCI	Parcel pointer >= 1
335	QD2	Write data designator bit 2
336	QD1	Write data designator bit 1
337	QD0	Write data designator bit 0
340	QEB	Go read HISP 0
341	QEC	Go read HISP 1
342	QEE	Go read VHISP 6
343	QEF	Go read VHISP 7
344	QES	Go read LOSP 0 or LOSP 1
345	RAH0	Conflict
346	SAA	Go write reference
347	SAE	SECDED correct off
350	SAI	Support channel readout designator
351	SIA	Interrupt request

352	SJA	033*ijk* response
353	SKA	Reference request
354	SI0	I/O request/response channel bit 0
355	SI1	I/O request/response channel bit 1
356	SI2	I/O request/response channel bit 2
357	SI3	I/O request/response channel bit 3
360	SI4	I/O request/response channel bit 4
361	SI5	I/O request/response channel bit 5
362	SI6	I/O request/response channel bit 6
363	SI7	I/O request/response channel bit 7
364	SI8	I/O request/response channel bit 8
365	SI9	I/O request/response channel bit 9
366	SI10	I/O request/response channel bit 10
367	SI11	I/O request/response channel bit 11
370	SI12	I/O request/response channel bit 12
371	SI13	I/O request/response channel bit 13
372	SI14	I/O request/response channel bit 14
373	SI15	I/O request/response channel bit 15
374	SI16	I/O request/response channel bit 16
375	SI17	I/O request/response channel bit 17
376	SI18	I/O request/response channel bit 18
377	SI19	I/O request/response channel bit 19

DC Option (Revision 1025)

Test Point	Term	Description
200	CK00	Partial syndrome bit 0
201	CK01	Partial syndrome bit 1
202	CK02	Partial syndrome bit 2
203	CK03	Partial syndrome bit 3
204	CK04	Partial syndrome bit 4
205	CK05	Partial syndrome bit 5
206	CK06	Partial syndrome bit 6
207	CK07	Partial syndrome bit 7
210	CL10	Syndrome bit 0
211	CL11	Syndrome bit 1
212	CL12	Syndrome bit 2
213	CL13	Syndrome bit 3
214	CL14	Syndrome bit 4
215	CL15	Syndrome bit 5
216	CL16	Syndrome bit 6

217	CL17	Syndrome bit 7
220	EBR	Stack data
221	EER	Read stacked data
222	EIB	Data readout select
223	ED12	Data readout phase 18
224	EFA	Data valid
225	EFB	Go write reference
226	EBB	Hold data rank B
227	EBC	Hold data rank C
230	EBD	Hold data rank D
231	–	–
232	FCA	Serial input
233	FCH	SECDED correct off
234	FCJ	Go readout – support channel
235	FIA	Support channel command
236	GAA	Sanity code from CPU module
237	GAZ	Successful recognition
240	GBA	Sanity code returned from CPU module
241	GBZ	Successful recognition
242	HCA	Sanity code MC port <–> SHR
243	HCB	Maintenance channel MC port <–> SHR
244	HCD	Sanity code MC port <–> HG0
245	HCM	Sanity code return HG0 <–> I/O
246	HCN	Maintenance channel return HG0 <–> I/O
247	HCO	Error logger HG0 <–> I/O
250	HDA	Command to I/O channel
251	HDB	Command to I/O channel
252	HDC	Command to I/O channel
253	HDD	Command to I/O channel
254	HDE	Command to I/O channel
255	HDF	Command to I/O channel
256	HDG	Command to I/O channel
257	HDH	Command to I/O channel
260	HDI	Command to I/O channel
261	HDJ	Command to I/O channel
262	HDK	Command to I/O channel
263	HDL	Command to I/O channel
264	HDM	Command to I/O channel
265	HDN	Command to I/O channel
266	HDO	Command to I/O channel
267	HDP	Command to I/O channel

270	HDQ	Go command to I/O channel
271	HDR	Go SECDED command
272	HGI	I/O writes complete
273	HGJ	I/O writes complete
274	HGK	I/O writes complete
275	HGL	I/O writes complete
276	HGM	I/O writes complete
277	HGN	I/O writes complete
300	HGO	I/O writes complete
301	HHA	Sanity code return MC port <–> SHR
302	HHB	Maintenance channel return MC port <–> SHR
303	HHC	Sanity code return MC port <–> SHR
304	HHM	Sanity code HG0 <–> I/O
305	HHN	Maintenance ch. HG0 <–> I/O
306	HHO	Error logger return HG0 <–> I/O
307	JAA	Error log from CPU
310	JC17	Double-bit error
311	JC18	Single-bit error
312	JE17	Double-bit error
313	JE18	Single-bit error
314	JG17	Double-bit error
315	JG18	Single-bit error
316	JI00	Serial input
317	kaa	Bit 0 of error scanner
320	KAB	Bit 1 of error scanner
321	KAC	Bit 2 of error scanner
322	LAA	Error from CPU error logger
323	LBA	I/O write error (DC)
324	LCA	I/O read error
325	LDA	I/O write error (CPU)
326	LEA	Channel error from DD
327	LBH	Clear I/O write error
330	LCH	Clear I/O read error
331	LDH	Clear I/O write error
332	LEH	Clear Channel error (DD)
333	LG00	Uncorrectable memory error
334	MA68	Error log output
335	NCQ	Error log return
336	VB00	Support channel serial bit counter
337	WOA	CPU sanity code on
340	WOB	CPU sanity code on (alternate path)

341	XF00	Syndrome bit 0
342	XF01	Check bit 1
343	XF02	Syndrome bit 2
344	XF03	Check bit 3
345	XF04	Syndrome bit 4
346	XF05	Check bit 5
347	XF06	Syndrome bit 6
350	XF07	Check bit 7
351	XG00	Syndrome bit 0
352	XG01	Syndrome bit 1
353	XG02	Syndrome bit 2
354	XG03	Syndrome bit 3
355	XG04	Syndrome bit 4
356	XG05	Syndrome bit 5
357	XG06	Syndrome bit 6
360	XG07	Syndrome bit 7
361	XM31	Memory to I/O support channel serial output
362	CQC	Error correction off
363	CQD	Error logging off
364	XHG	Error correction off
365	XHI	Disable error logger
366	XGM	Double-bit error
367	JD201	Double-bit error
370	JD210	Write channel designators bit 0 (phase 12)
371	JD211	Write channel designators bit 1 (phase 12)
372	JD212	Write channel designators bit 2 (phase 12)
373	JF211	Readout designator 0 (phase 25)
374	JF212	Readout designator 1
375	JF213	Readout designator 2
376	JK00	Channel errors from DE
377	LEI	Channel error from DE

DD Option (Revision 2650)

Test Point	Term	Description
200	WBA	Configuration – LOSP0 – I/O group bit 0
201	WBC	Configuration – LOSP0 – I/O group bit 1
202	WBI	Configuration – LOSP0 – use memory group selections
203	WBK	Configuration – LOSP0 – memory group select bit 0
204	WBM	Configuration – LOSP0 – memory group select bit 1
205	WBQ	Configuration – LOSP0 – LOSP/MISP mode

206	WBS	Configuration – LOSP0 – force memory to upper 256k
207	WBU	Configuration – LOSP0 – channel enable
210	WBW	Configuration – LOSP0 – loopback mode
211	WCI	Configuration – HISP0 – use memory group selections
212	WCK	Configuration – HISP0 – memory group select bit 0
213	WCM	Configuration – HISP0 – memory group select bit 1
214	WCS	Configuration – HISP0 – force memory to upper 256k
215	WCU	Configuration – HISP0 – channel enable
216	WDI	Configuration – HISP1 – use memory group selections
217	WDK	Configuration – HISP1 – memory group select bit 0
220	WDM	Configuration – HISP1 – memory group select bit 1
221	WDS	Configuration – HISP1 – force memory to upper 256k
222	WDU	Configuration – HISP1 – channel enable
223	WJC	Diagnostic mode – LOSP1 – disable SECDED at CPU [121]
224	WJE	Diagnostic mode – LOSP1 – force constant SBCDBD at CPU [125]
225	WJI	Diagnostic mode – LOSP1 – swap data into SECDED at CPU [132]
226	WKI	Diagnostic mode – HISP0 – swap data into SECDED at CPU [132]
227	WLI	Diagnostic mode – HISP1 – swap data into SECDED at CPU [132]
230	WMC	Diagnostic mode – SPPRT – disable SECDED at CPU [121]
231	WME	Diagnostic mode – SPPRT – force constant SBCDBD at CPU [125]
232	WMI	Diagnostic mode – SPPRT – swap data into SECDED at CPU [132]
233	YAV	Test point place holder
234	YAZ	Test point place holder
235	VIJ	PINT channel request awaiting
236	VIQ	MCU interrupt channel request
237	AUL	033*ijk* request to process
240	TAA	LOSPX input parcel counter bit 0
241	TAB	LOSPX input parcel counter bit 1
242	TDN	LOSPX input –> data ready
243	TCS	LOSPX input –> disconnect
244	TFW	LOSPX input –> resume
245	TCZD	LOSPX input –> master clear
246	PXA	Go interrupt request
247	–	–
250	TRA	LOSPX output parcel counter bit 0
251	TRB	LOSPX output parcel counter bit 1
252	TSW	LOSPX output –> ready
253	TTW	LOSPX output –> disconnect
254	TUE	LOSPX output –> resume
255	TRE	LOSPX output data available
256	TQX	LOSPX output serial data input shift sequencer idle

257	PUA	Go 033*ijk* response
260	UPP	LOSPX input serial data channel
261	UQC	LOSPX output serial data channel
262	TIO	Serial control output channel
263	TMR	Serial control input channel
264	NRZ	Interrupt status serial channel
265	NQG	Interrupt status serial controller bit 6
266	NKR	Serial control output channel
267	NKA	Serial control output channel sequencer bit 0
270	MCP	Support output word in buffer
271	MCI	Support output outstanding read request
272	MCA	Support output read reference request
273	MBA	Support output active
274	MAR	Support output interrupt change request
275	MAP	Support output enable interrupts
276	MAE	Support output fatal error
277	MAA	Support output done flag
300	NAO	Serial control channel
301	LGA	Support input buffer in use
302	LFA	Support input write reference request
303	LBA	Support input active
304	LAR	Support input interrupt change request
305	LAP	Support input enable interrupts
306	LAE	Support input fatal error
307	LAA	Support input done flag
310	KDI	LOSP0 output parcel counter bit 0
311	KDJ	LOSP0 output parcel counter bit 1
312	KCA	LOSP0 output read reference request
313	KBA	LOSP0 output active
314	KAR	LOSP0 output interrupt change request
315	KAP	LOSP0 output enable interrupts
316	KAE	LOSP0 output fatal error
317	KAA	LOSP0 output done flag
320	KFV	LOSP0 output disconnect to external
321	KGC	LOSP0 output resume
322	KCI	LOSP0 output 1 word outstanding for reads
323	JCY	LOSP0 input disconnect holding
324	JGI	1 word outstanding write
325	JCT	LOSP0 input disconnect stacked
326	JCA	LOSP0 input parcel counter bit 0
327	JCB	LOSP0 input parcel counter bit 1

330	JJV	LOSP0 input resume to external
331	JKK	LOSP0 input disconnect
332	JFA	LOSP0 input write reference request
333	JBA	LOSP0 input active
334	JAR	LOSP0 input interrupt change request
335	JAP	LOSP0 input enable interrupts
336	JAE	LOSP0 input fatal error
337	JAA	LOSP0 input done flag
340	DOE	HISP0 output address bit 4
341	DOF	HISP0 output address bit 5
342	DOG	HISP0 output address bit 6
343	DOH	HISP0 output address bit 7
344	DJZ	HISP0 output block length = 0
345	EED	HISP0 output reference acknowledge
346	EJT	HISP0 output send next word sequencer start
347	EBA	HISP0 output read reference request
350	DDP	HISP0 output address ready
351	DBK	HISP0 output missing address ready (early transmit data)
352	DBJ	HISP0 output add ready without transmit address or sixth address ready
353	DBI	HISP0 output parity error on address channel
354	DBHE	HISP0 output address counter at zero
355	DAE	HISP0 output data sequence active
356	DAK	HISP0 output address error
357	DAI	HISP0 output error
360	FOE	HISP1 output address bit 4
361	FOF	HISP1 output address bit 5
362	FOG	HISP1 output address bit 6
363	FOH	HISP1 output address bit 7
364	FJZ	HISP1 output block length = 0
365	GED	HISP1 output reference acknowledge
366	GJT	HISP1 output send next word sequencer start
367	GBA	HISP1 output read reference request
370	FDP	HISP1 output address ready
371	FBK	HISP1 output missing address ready (early transmit data)
372	FBJ	HISP1 output add ready without transmit address or sixth address ready
373	FBI	HISP1 output parity error on address channel
374	FBHE	HISP1 output address counter at zero
375	FAE	HISP1 output data sequence active
376	FAK	HISP1 output address error
377	FAI	HISP1 output error

DE Option (Revision 2650)

Test Point	Term	Description
200	WAA	Configuration – VHISP – I/O group bit 0
201	WAC	Configuration – VHISP – I/O group bit 1
202	WAI	Configuration – VHISP – use memory group selections
203	WAK	Configuration – VHISP – memory group select bit 0
204	WAM	Configuration – VHISP – memory group select bit 1
205	WAS	Configuration – VHISP – force memory to upper 256k
206	WAU	Configuration – VHISP – channel enable
207	WBA	Configuration – LOSP1 – I/O group bit 0
210	WBC	Configuration – LOSP1 – I/O group bit 1
211	WBI	Configuration – LOSP1 – use memory group selections
212	WBK	Configuration – LOSP1 – memory group select bit 0
213	WBM	Configuration – LOSP1 – memory group select bit 1
214	WBQ	Configuration – LOSP1 – LOSP/MISP mode
215	WBS	Configuration – LOSP1 – force memory to upper 256k
216	WBU	Configuration – LOSP1 – channel enable
217	WBW	Configuration – LOSP1 – loopback mode
220	WCI	Configuration – HISP0 – use memory group selections
221	WCK	Configuration – HISP0 – memory group select bit 0
222	WCM	Configuration – HISP0 – memory group select bit 1
223	WCS	Configuration – HISP0 – force memory to upper 256k
224	WCU	Configuration – HISP0 – channel enable
225	WDI	Configuration – HISP1 – use memory group selections
226	WDK	Configuration – HISP1 – memory group select bit 0
227	WDM	Configuration – HISP1 – memory group select bit 1
230	WDS	Configuration – HISP1 – force memory to upper 256k
231	WDU	Configuration – HISP1 – channel enable
232	WIC	Diagnostic mode – VHISP – disable SECDED at CPU [121]
233	WIE	Diagnostic mode – VHISP – force constant SBCDBD at CPU [125]
234	WII	Diagnostic mode – VHISP – swap data into SECDED at CPU [132]
235	WJC	Diagnostic mode – LOSP1 – disable SECDED at CPU [121]
236	WJE	Diagnostic mode – LOSP1 – force constant SBCDBD at CPU [125]
237	WJI	Diagnostic mode – LOSP1 – swap data into SECDED at CPU [132]
240	WKC	Diagnostic mode – HISP0 – disable SECDED at CPU [121]
241	WKE	Diagnostic mode – HISP0 – force constant SBCDBD at CPU [125]
242	WLC	Diagnostic mode – HISP1 – disable SECDED at CPU [121]
243	WLE	Diagnostic mode – HISP1 – force constant SBCDBD at CPU [125]
244	YAV	Test point place holder
245	DCQ	Disable ECC HISP0

246	FCQ	Disable ECC HISP1
247	APW	Clear interrupt and error flags (LOSP1 in)
250	AQW	Clear interrupt and error flags (LOSP1 out)
251	ARW	Clear interrupt and error flags VHISP
252	BAHE	Uncorrectable memory error phase 33
253	BEL	LOSP1 channel writes complete
254	BEM	HISP0 channel writes complete
255	BEN	HISP1 channel writes complete
256	BEO	VHISP channel writes complete
257	NRW	Interrupt channel summation serial channel
260	MAN	MCU interrupt request
261	MAP	PINT interrupt request
262	MCY	PINT/MCU timeout depleted
263	VBH	VHISP channel clock off time expired
264	VAH	VHISP channel clock on time expired
265	UBPA	VHISP output block sequencer
266	TFME	VHISP reload input channel clock counter
267	TFI	VHISP input data ready
270	VGA	VHISP channel clock
271	TJZ	VHISP block length = 0
272	URB	VHISP write request acknowledge
273	UDH	VHISP first word of a read block arriving
274	UQA	VHISP write reference request
275	UAA	VHISP read reference request
276	TEQ	VHISP done and empty
277	TCJ	VHISP active and address delay complete
300	TBG	VHISP input mode (from SSD to CPU/main memory)
301	TBE	VHISP block length captured
302	TBC	VHISP current address captured
303	TBA	VHISP clear channel
304	TAR	VHISP interrupt change request
305	TAP	VHISP enable interrupts
306	TAE	VHISP fatal error
307	TAA	VHISP done flag
310	KDI	LOSP0 output parcel counter bit 0
311	KDJ	LOSP0 output parcel counter bit 1
312	KCA	LOSP0 output read reference request
313	KBA	LOSP0 output active
314	KAR	LOSP0 output interrupt change request
315	KAP	LOSP0 output enable interrupts
316	KAE	LOSP0 output fatal error

317	KAA	LOSP0 output done flag
320	KFUE	LOSP0 output disconnect to external
321	KGC	LOSP0 output resume
322	KCI	LOSP0 output 1 word outstanding for reads
323	JCY	LOSP0 input disconnect holding
324	JGI	LOSP0 input 1 word outstanding write
325	JCT	LOSP0 input disconnect stacked
326	JCA	LOSP0 input parcel counter bit 0
327	JCB	LOSP0 input parcel counter bit 1
330	JJUE	LOSP0 input resume to external
331	JKK	LOSP0 input disconnect
332	JFA	LOSP0 input write reference request
333	JBA	LOSP0 input active
334	JAR	LOSP0 input interrupt change request
335	JAP	LOSP0 input enable interrupts
336	JAE	LOSP0 input fatal error
337	JAA	LOSP0 input done flag
340	DOE	HISP0 input address bit 4
341	DOF	HISP0 input address bit 5
342	DOG	HISP0 input address bit 6
343	DOH	HISP0 input address bit 7
344	DJZ	HISP0 input block length = 0
345	EHT	HISP0 input transmit data
346	EHN	HISP0 input no buffers in use
347	EBA	HISP0 input write reference request
350	DDP	HISP0 input address ready
351	DBK	HISP0 input missing address ready (early transmit data)
352	DBJ	HISP0 input add ready without transmit address or sixth address ready
353	DBI	HISP0 input parity error on address channel
354	DBHE	HISP0 input address counter at zero
355	DAE	HISP0 input data sequence active
356	DAK	HISP0 input address error
357	DAI	HISP0 input error
360	FOE	HISP1 input address bit 4
361	FOF	HISP1 input address bit 5
362	FOG	HISP1 input address bit 6
363	FOH	HISP1 input address bit 7
364	FJZ	HISP1 input block length = 0
365	GHT	HISP1 input transmit data
366	GHN	HISP1 input no buffers in use
367	GBA	HISP1 input write reference request

370	FDP	HISP1 input address ready
371	FBK	HISP1 input missing address ready (early transmit data)
372	FBJ	HISP1 input add ready without transmit address or sixth address ready
373	FBI	HISP1 input parity error on address channel
374	FBHE	HISP1 input address counter at zero
375	FAE	HISP1 input data sequence active
376	FAK	HISP1 input address error
377	FAI	HISP1 input error

DM Option (Revision 3002)

Test Point	Term	Description
200	AAA	Sanity code return from shared (though CPU 2)
201	AAZ	Sanity code detected from shared (though CPU 2)
202	ABA	Sanity code return from shared (though CPU 3)
203	ABZ	Sanity code detected from shared (though CPU 3)
204	ACA	Sanity code return from shared (though CPU 4)
205	ACZ	Sanity code detected from shared (though CPU 4)
206	ADA	Sanity code return from shared (though CPU 5)
207	ADZ	Sanity code detected from shared (though CPU 5)
210	AEA	Sanity code return from CPU 2
211	AEZ	Sanity code detected from CPU 2
212	AFA	Sanity code return from CPU 3
213	AFZ	Sanity code detected from CPU 3
214	AGA	Sanity code return from CPU 4
215	AGZ	Sanity code detected from CPU 4
216	AHA	Sanity code return from CPU 5
217	AHZ	Sanity code detected from CPU 5
220	BAA	Sanity code from CPU 2
221	BAZ	Sanity code detected from CPU 2
222	BBA	Sanity code from CPU 3
223	BBZ	Sanity code detected from CPU 3
224	BCA	Sanity code from CPU 4
225	BCZ	Sanity code detected from CPU 4
226	BDA	Sanity code from CPU 5
227	BDZ	Sanity code detected from CPU 5
230	CAA	Sanity code from sanity code generator
231	CAZ	Sanity code detected from sanity code generator
232	DFA	Maintenance channel master clear
233	DEG	Clear sanity code generator
234	EAA	Maintenance channel control

235	EDN	Attention (35)
236	EDP	Reply (37)
237	EEE	External maintenance channel return
240	EGC	Enter data mode
241	EIZ	Wait for response
242	EJJ	Hold data rank 2
243	EJM	Block maintenance channel out
244	EJR	Attention received
245	EJX	Ignore external maintenance channel
246	EKA	Data from external maintenance channel
247	FAA	Maintenance channel return counter bit 0
250	FBA	Count = 4 (capture route code)
251	FCA	Maintenance channel control counter bit 0 (in)
252	FCZ	Count = 5 (control is valid)
253	FEA	Maintenance channel data counter bit 0
254	FFB	Count = 63
255	FGA	Maintenance channel control counter bit 0 (out)
256	FGY	Count not equal to 0
257	GBA	CPU 2 is master
260	GBB	CPU 3 is master
261	GBC	CPU 4 is master
262	GBD	CPU 5 is master
263	GBE	Maintenance channel is master
264	KAA	Maintenance channel in
265	KAB	Maintenance channel in
266	KEA	Route code 20
267	KEB	Route code 21
270	KEC	Route code 22
271	KED	Route code 23
272	kei	Route code 30
273	KEM	Route code 34
274	KHP	Route code detector delay counter bit 0
275	KLB	Maintenance channel to shared via CPU 2
276	KLD	Maintenance channel to shared via CPU 3
277	KLF	Maintenance channel to shared via CPU 4
300	KLH	Maintenance channel to shared via CPU 5
301	KLR	Maintenance channel to logic monitor
302	NAA	Maintenance channel return
303	NAB	Maintenance channel return
304	NBA	Data from maintenance channel
305	NKC	Data tag

306	NKE	Acknowledge
307	NKI	Disconnect, waiting for attention
310	NLO	Send acknowledge
311	PAA	Error log input from CPU 2
312	PFA	Error log input from CPU 3
313	PKA	Error log input from CPU 4
314	PPA	Error log input from CPU 5
315	raa	Error from DC0
316	rab	Error from DC1
317	rac	Error from DC2
320	rad	Error from DC3
321	RBB	Waiting for response
322	RCK	Reporting error from DC0
323	RCL	Reporting error from DC1
324	RCM	Reporting error from DC2
325	RCN	Reporting error from DC3
326	RFA	Error log output to CPU 2
327	RFB	Error log output to CPU 3
330	RFC	Error log output to CPU 4
331	RFD	Error log output to CPU 5
332	RFI	Error log output to external
333	RFJ	Error log control to external
334	RGC	Error log return data from external
335	SAA	DC0 error log input delay counter bit 0
336	SCA	DC1 error log input delay counter bit 0
337	SEA	DC2 error log input delay counter bit 0
340	SGA	DC3 error log input delay counter bit 0
341	SHP	Error log response
342	SHQ	Error log response
343	SKA	Error log out delay counter bit 0
344	TAA	Support channel to DD0 (data)
345	TAB	Support channel to DD0 (control)
346	TBA	Support channel to DD1 (data)
347	TBB	Support channel to DD1 (control)
350	TCA	Support channel to DD2 (data)
351	TCB	Support channel to DD2 (control)
352	TDA	Support channel to DD3 (data)
353	TDB	Support channel to DD3 (control)
354	TEC	Support channel from DD0 – 3 (data)
355	TEB	Support channel from DD0 – 3 (control)
356	WAA	Rearbitrate master sanity code

357	WBQ	Logic monitor reset
360	WCA	I/O master clear quadrant 0
361	WCB	I/O master clear quadrant 1
362	WCC	I/O master clear quadrant 2
363	WCD	I/O master clear quadrant 3
364	WCL	Support channel on DD0
365	WCM	Support channel on DD1
366	WCN	Support channel on DD2
367	WCO	Support channel on DD3
370	TJA	PINT/MCU interrupt to DE0
371	TJD	PINT/MCU interrupt to DE1
372	TJG	PINT/MCU interrupt to DE2
373	TJJ	PINT/MCU interrupt to DE3
374	WAQ	Code 77 reset to default
375	WCE	I/O master clear support chips
376	WGB	DM master clear
377	WGD	Reset chip / counters

DR Option (Revision 1035)

Test Point	Term	Description
200	FA20	Output – data from processor bit n + 0
201	FA24	Output – data from processor bit n + 4
202	FA28	Output – data from processor bit n + 8
203	FA32	Output – data from processor bit n + 12
204	FA36	Output – data from processor bit n + 16
205	FA37	Output – data from processor bit n + 17
206	EC0	Output channel B – data from buffer B bit n + 0
207	EC16	Output channel B – data from buffer B bit n + 16
210	FC8	Output channel D – data from buffer D bit n + 8
211	FC17	Output channel D – data from buffer D bit n + 17
212	GH10	LOSP output – data bit n + 0
213	GH11	LOSP output – data bit n + 1
214	GH12	LOSP output – data bit n + 2
215	GH13	LOSP output – data bit n + 3
216	GH14	LOSP output – data bit n + 4
217	RK10	LOSP output – word B pointer
220	QDB	Output channel B – clear address
221	QDH	Output channel B – go read
222	QDJ	Output channel B – go write
223	RE30	Output channel B – read address bit 0

224	RE31	Output channel B – read address bit 1
225	RE32	Output channel B – read address bit 2
226	RE33	Output channel B – read address bit 3
227	RE34	Output channel B – read address bit 4
230	RE35	Output channel B – read address bit 5
231	RF30	Output channel B – write address bit 0
232	RF31	Output channel B – write address bit 1
233	RF32	Output channel B – write address bit 2
234	RF33	Output channel B – write address bit 3
235	RF34	Output channel B – write address bit 4
236	RF35	Output channel B – write address bit 5
237	RXB	Output channel buffer (B/D) pointer
240	QEB	Output channel D – clear address
241	QEH	Output channel D – go read
242	QEJ	Output channel D – go write
243	RG30	Output channel D – read address bit 0
244	RG31	Output channel D – read address bit 1
245	RG32	Output channel D – read address bit 2
246	RG33	Output channel D – read address bit 3
247	RG34	Output channel D – read address bit 4
250	RG35	Output channel D – read address bit 5
251	RH30	Output channel D – write address bit 0
252	RH31	Output channel D – write address bit 1
253	RH32	Output channel D – write address bit 2
254	RH33	Output channel D – write address bit 3
255	RH34	Output channel D – write address bit 4
256	RH35	Output channel D – write address bit 5
257	RJ10	LOSP input – readout word B pointer
260	QGB	LOSP output – clear address
261	QGF	LOSP output – go read
262	QGK	LOSP output – go write
263	RL40	LOSP output – parcel counter bit 0
264	RL41	LOSP output – parcel counter bit 1
265	RL42	LOSP output – parcel counter bit 2
266	TED1	LOSP output – gate data to register a
267	TEE1	LOSP output – gate data to register b
270	BA0	Input channel A – data bit n + 0
271	BA4	Input channel A – data bit n + 4
272	BA8	Input channel A – data bit n + 8
273	BA12	Input channel A – data bit n + 12
274	BA16	Input channel A – data bit n + 16

275	BA17	Input channel A – data bit n + 17
276	CA0	Input channel C – data bit n + 0
277	CA4	Input channel C – data bit n + 4
300	CA8	Input channel C – data bit n + 8
301	CA12	Input channel C – data bit n + 12
302	CA16	Input channel C – data bit n + 16
303	CA17	Input channel C – data bit n + 17
304	DA10	LOSP input – data bit n + 0
305	DA11	LOSP input – data bit n + 1
306	DA12	LOSP input – data bit n + 2
307	DA13	LOSP input – data bit n + 3
310	DA14	LOSP input – parity bit n + 0
311	aa0	Input channel readout MUX bit n + 0
312	aa4	Input channel readout MUX bit bit n + 8
313	aa8	Input channel readout MUX bit bit n + 16
314	ab0	Input channel readout MUX bit bit n + 0
315	ab4	Input channel readout MUX bit bit n + 8
316	ab8	Input channel readout MUX bit bit n + 16
317	ad0	Input merge data bit n + 0
320	ad4	Input merge data bit n + 4
321	ad8	Input merge data bit n + 8
322	ae0	Input swap data bit n + 0
323	ae4	Input swap data bit n + 4
324	ae8	Input swap data bit n + 8
325	RX34	Output channel even write address bit n + 4
326	RX35	Output channel even write address bit n + 5
327	RX44	Output channel odd write address bit n + 4
330	RX45	Output channel odd write address bit n + 5
331	RA0	Input channel A – read address bit 0
332	RA1	Input channel A – read address bit 1
333	RA2	Input channel A – read address bit 2
334	RA3	Input channel A – read address bit 3
335	RA4	Input channel A – read address bit 4
336	RA5	Input channel A – read address bit 5
337	RB0	Input channel A – write address bit 0
340	RB1	Input channel A – write address bit 1
341	RB2	Input channel A – write address bit 2
342	RB3	Input channel A – write address bit 3
343	RB4	Input channel A – write address bit 4
344	RB5	Input channel A – write address bit 5
345	RK10	LOSP input – sample word B pointer

346	RC0	Input channel C – read address bit 0
347	RC1	Input channel C – read address bit 1
350	RC2	Input channel C – read address bit 2
351	RC3	Input channel C – read address bit 3
352	RC4	Input channel C – read address bit 4
353	RC5	Input channel C – read address bit 5
354	RD0	Input channel C – write address bit 0
355	RD1	Input channel C – write address bit 1
356	RD2	Input channel C – write address bit 2
357	RD3	Input channel C – write address bit 3
360	RD4	Input channel C – write address bit 4
361	RD5	Input channel C – write address bit 5
362	RI0	LOSP input – parcel counter bit 0
363	RI1	LOSP input – parcel counter bit 1
364	RIW	LOSP input – word pointer
365	RJ10	LOSP input – word B pointer
366	DDE	LOSP input – parity error
367	DDJ	LOSP input – enable parity check
370	WA10	HISP address – serial output
371	WDA0	HISP address – sample HISP address
372	WH17	VHISP address/block length – serial input
373	WLB	VHISP address/block length – sample VHISP address/block length
374	WP13	VHISP block length n + 0 through n + 3 – serial input
375	WTB	VHISP block length n + 0 through n + 3 – sample VHISP block length
376	wj0	VHISP address/block length – bit n + 0
377	wr0	VHISP block length – bit n + 0

GigaRing™ I/O Module (IO02) Test Points

This section lists the test points that are built into the options on IO02 modules. A brief description of each option is also included.

DG Option (Revision 1312)

Test Point	Term	Description
200	WFAA	Primary group (group bit 0)
201	WFAE	Primary group (group bit 1)
202	WDBB	Nodes A and B use group bits 2 and 3 (instead of group bits 4 and 5)
203	WDCB	Use memory groups
204	WDDB	Do not block designated 1 traffic from node A/B
205	WJAA	Force all writes to the master I/O group
206	WJEA	Block I/O group entry into the OGM
207	WJIA	Do not discard packets if inactive
210	WJMA	Block writes for 127 of 128 clock periods
211	WJQA	Block reads for 127 of 128 clock periods
212	WJXA	Disable timeout for express MMRs
213	WKAA	OGM parity test (node A)
214	WKEA	OGM parity test (node B)
215	WKIA	Alternate checkbyte mode readout
216	WKMA	Alternate checkbyte mode (node A)
217	WKQA	Alternate checkbyte mode (node B)
220	WEAA	Primary group memory group (group bit 0)
221	WEAE	Primary group memory group (group bit 1)
222	WEBA	Secondary group memory group (group bit 0)
223	WEBE	Secondary group memory group (group bit 1)
224	–	–
225	–	–
226	–	–
227	–	–
230	–	–
231	–	–
232	–	–
233	–	–
234	XCA02	Maintenance channel serial input
235	CWAA	Serial channel writes complete
236	XIG	Synchronize counter 64/128
237	WAC	Dummy term
240	DAAI	Write active

241	DAAK	Reference block completed
242	DAALA	Abort
243	DAANA	Message or error packet
244	DAAOA	Capture parameter
245	DAARA	Go sequence
246	DAAWA	Start/capture parameters
247	DAAXB	Go readout phase
250	DACG	First reference request complete
251	DACI	Second reference request complete
252	DACK	Third reference request complete
253	DACQAH	Reference sequence stuck at
254	DACQA	Go write reference request
255	DACQC	Go write reference request
256	DADU	Go data to CPU
257	DADX	Current block completing
260	DEFI	TCB packet
261	DEFJ	Data packet
262	DEFM	ERRED packet
263	DEFL	Message packet
264	DEGG	Node A/B
265	DEGE	Packet I/O group bit 0
266	DEGF	Packet I/O group bit 1
267	DEHB	Alternate checkbyte mode
270	DFKI	I/O group 0 inactive (kill packet)
271	DFKA	Node A ERRED buffer 1 inactive (pointing at buffer 1)
272	DFKR	Node A ERRED pointing at buffer 0
273	DHAA	Enter ROA
274	–	–
275	DINA	Carry bit for write address increment
276	DINP	Carry bit for write address increment
277	DINL	Carry bit for write address increment
300	EDBE	Go read reference request packet from DQ00 (node A)
301	EDCF	Read request rank valid
302	EDDB	Allow read request (node A)
303	EGAB	Reselect gate terms
304	EEBE	Go read reference request packet from DQ01 (node B)
305	EECF	Read request rank valid
306	EEDB	Allow read request (node B)
307	EHAD	Gate TIB or OGM snoop request
310	EHIA	Node A gated last
311	FAAWE	Read request

312	FALB	Interrupt request update
313	–	–
314	FALE	CA = CA OGM
315	FALF	CA = EA TIB/TCB
316	FCBI	–
317	FCBJ	–
320	FCCA	Allow read request
321	FCDC	Go read request
322	FCIC	Go TCB write request
323	FEAT	OGM request
324	FEAGA	I/O group 0
325	FEAHA	I/O group 1
326	FEAJ	Node A/B
327	FEAR	TIB or OGM snoop request
330	FFAB	Number of read requests required
331	FFAC	Number of read requests required
332	CLDA	Packet flag —> capture packet block length
333	CTCA	Go write to ROA
334	BXBI	Deactivation not required (node A)
335	BXBJ	Deactivation not required (node B)
336	BXBR	Deactivation not required
337	CWAA	Serial channel writes complete
340	CUAD	Designator –, 3, 5, 7 available
341	CUAE	Designator 2, 3, 6, 7 available
342	CUAF	Designator 4, 5, 6, 7 available
343	FTCU	Readout data strobe
344	CWDB	Write designator 1 writes complete
345	CWDC	Write designator 2 writes complete
346	CWDD	Write designator 3 writes complete
347	CWDE	Write designator 4 writes complete
350	CWDF	Write designator 5 writes complete
351	CWDG	Write designator 6 writes complete
352	CWDH	Write designator 7 writes complete
353	CWBD	Writes complete serial channel decode sequencer
354	FRKD	Level 2 reference designator (2 – 4 node A) valid
355	FRLD	Level 1 reference designator (2 – 4 node A) valid
356	FROD	Level 2 reference designator (5 – 7 node B) valid
357	FRPD	Level 1 reference designator (5 – 7 node B) valid
360	HABA	Stoker/outgoing message node A/B
361	HABB	Stoker/outgoing message I/O group 0
362	HABC	Stoker/outgoing message I/O group 1

363	HABD	Stoker/outgoing message I/O (0=outgoing message, 1=TIB/TCB)
364	HAJA	Go outgoing message snoop sequence
365	HAJE	Outgoing message snoop read request
366	HAJI	Outgoing message packet sequence
367	HAJM	Outgoing message packet read request
370	HAJQ	Go TIB sequence
371	HAJS	TIB read request
372	HAJW	TIB/outgoing message sequence aborted
373	HDAA	Timeout counter signal
374	HPAA	TCB sequence pointer bit 0
375	HPAB	TCB sequence pointer bit 1
376	FTCV	Readout data strobe
377	FTCW	TIB/OGM snoop reference

DH Option (Revision 1102)

Test Point	Term	Description
200	–	–
201	–	–
202	–	–
203	–	–
204	–	–
205	–	–
206	–	–
207	–	–
210	aam0	Data bit 0
211	abm0	Data bit 0
212	aca0	Block length bit 0
213	aca1	Block length bit 1
214	aca2	Block length bit 2
215	aca3	Block length bit 3
216	aca4	Block length bit 4
217	aca5	Block length bit 5
220	aca6	Block length bit 6
221	acb	Parity from DTs
222	acc	Parity from DTs
223	fa12	Go write even RAM 0 and 1
224	–	–
225	fa14	Go write odd RAM 6 and 7
226	–	–
227	fab0	Write address bit 0

230	fab1	Write address bit 1
231	fab2	Write address bit 2
232	fab3	Write address bit 3
233	fab4	Write address bit 4
234	fab5	Write address bit 5
235	fab6	Write address bit 6
236	–	–
237	gad0	Read address bit 0 (CPU master address + 1)
240	gad1	Read address bit 1 (CPU master address + 1)
241	gad2	Read address bit 2 (CPU master address + 1)
242	gad3	Read address bit 3 (CPU master address + 1)
243	gad4	Read address bit 4 (CPU master address + 1)
244	gad5	Read address bit 5 (CPU master address + 1)
245	gad6	Read address bit 6 (CPU master address + 1)
246	–	–
247	ged0	Read address bit 0 (snooper master address + 1)
250	ged1	Read address bit 1 (snooper master address + 1)
251	ged2	Read address bit 2 (snooper master address + 1)
252	ged3	Read address bit 3 (snooper master address + 1)
253	ged4	Read address bit 4 (snooper master address + 1)
254	ged5	Read address bit 5 (snooper master address + 1)
255	ged6	Read address bit 6 (snooper master address + 1)
256	–	–
257	jag0	Serial port write completion
260	kac0	CPU channel commands bit 0
261	kac1	CPU channel commands bit 1
262	kac2	CPU channel commands bit 2
263	kac3	CPU channel commands bit 3
264	kac4	CPU channel commands bit 4
265	kac5	CPU channel commands bit 5
266	kac6	CPU channel commands bit 6
267	kac7	CPU channel commands bit 7
270	kac8	CPU channel commands bit 8
271	kac9	CPU channel commands bit 9
272	kac10	CPU channel commands bit 10
273	kac11	CPU channel commands bit 11
274	kac12	CPU channel commands bit 12
275	kac13	CPU channel commands bit 13
276	kac14	CPU channel commands bit 14
277	kac15	CPU channel commands bit 15
300	kac16	CPU channel commands bit 16

301	kac17	CPU channel commands bit 17
302	qaac	Read snoop data
303	qabg	Snoop request 2^0
304	qabh	Snoop request 2^1
305	qcdc	CPU data valid for output stack
306	qcec	Preference select
307	qdbc	Go readout
310	qdda	Insert block length
311	qvaa	CPU data hold 12 even
312	qvab1	CPU data hold 12 even
313	–	–
314	–	–
315	qvaj	–
316	raae	12 valid (even)
317	raag	12 hold (even)
320	raai	12 valid (odd)
321	raak	12 hold (odd)
322	raap	13 valid
323	taa4	Disable error correction (TAA = 1 disable)
324	yha43	Position bit (1 = DH001)
325	quaa	CPU data 12 valid even
326	quba	CPU data 12 valid odd
327	qvbj	CPU data readout prefetch even
330	qvbb	CPU data hold 12 even
331	qvbb1	CPU data hold 12 even
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–
337	–	–
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–

352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	–	–

DN Option (Revision 1202)

Test Point	Term	Description
200	BBA	Request packet (send accept)
201	BBC	Active
202	BBE	Payload packet
203	BBG	Completion packet
204	BCA	Enter bits 56 through 63
205	BDA	Channel 20 output request
206	BDE	Send accept
207	BDG	Data mode
210	BDI	Waiting for reply
211	BDK	Send data to SSMC
212	BDM	Waiting for final reply
213	BDO	Send accept
214	BEH	Enter sanity code generator
215	CBA	Request packet
216	CBC	Accept packet

217	CBE	Payload packet
220	CBG	Completion packet
221	CBK	Output loopback input request
222	CCA	Enter bits 56 through 63
223	COA	Request packet
224	COC	Accept packet
225	COI	Output loopback output
226	ECA	Enter mcr
227	ECD	Hold rank A
230	ECE	Rank B full
231	ECG	RC 35 (disconnect)
232	ECI	RC 36 (data tag)
233	ECK	RC 37 (reply)
234	EDA	Channel 21 output request
235	EDG	Output request
236	EDJ	Waiting for accept
237	EDK	Send reply to SSMC
240	EDL	SSMC not busy
241	EDP	Output data header
242	EFA	Accept packet (from channel)
243	EFC	Request packet (from channel)
244	FDF	Send request
245	FDG	Output request
246	FDJ	Output request
247	FDL	Accept received
250	FDP	Output data header
251	FFA	Accept packet (from channel)
252	FFC	Request packet (from channel)
253	FFF	Waiting for final accept
254	GAA00	Priority counter bit 0
255	GAA01	Priority counter bit 1
256	GAA02	Priority counter bit 2
257	GBH	Stop priority counter
260	JBB03	Super serial maintenance channel
261	JHB	I/O module is master
262	JIA	Found sanity
263	JIE	Lost sanity
264	JIK	Send 27 command
265	JIO	Send 36 command
266	JJA	21 command (route SSMC to supervisory channel)
267	JJD	20 command

270	JJI	Looking for first 1 bit
271	JKA	23 command, route to error log
272	JLA	Route code = 32
273	JLC	Route code = 33
274	JLF	Route code = 37
275	JLL	Route code = 33
276	JOA00	Priority counter for SSMC out (bit 0)
277	JOA01	Priority counter for SSMC out (bit 1)
300	JOA02	Priority counter for SSMC out (bit 2)
301	JOV	Send 26 command to SSMC
302	KAA00	SSMC input counter bit 0
303	KBA00	SSMC output counter bit 0
304	KMA00	Serial input
305	KNC02	Serial output
306	LAB00	Boundary scan data
307	LBC	Boundary scan loop controller function
310	LBG	Boundary scan DMA function
311	LGD	Boundary scan function for this DN option
312	LEA	Test mode
313	LKA	Test data out
314	LLD	Test data in
315	LMD	Test clock return
316	MAB	Shift in
317	MAG	Waiting for data word
320	MBA	Input data
321	MBC	Output data
322	MBI	Send reply/data to SSMC
323	MBN	Gate data to SSMC
324	MBP	Transfer done
325	MBS	Go boundary scan reply to SSMC
326	NBA	BL = 0
327	NCE	Count = 100
330	NAC00	Boundary scan
331	NCA00	Boundary scan data bit counter bit 0
332	PME	Test mode return
333	QBA	Load setup time
334	QBD	Load pulse width
335	QBG	Load hold time
336	QDA	Count = 1
337	RDFB	Continuity line error
340	RDG	Continuity line error from DN option

341	VBA	Sanity code from IO module
342	VBZ	Successful recognition
343	VDA	Valid sanity from any CPU
344	VEA	Sanity code from sanity code generator
345	VEZ	Succesful recognition
346	VHC	Sanity output to IO
347	VGD	Clear sanity code generator
350	WBA	IO module sanity on
351	WBE	Continuity line reporting on
352	WDA00	Continuity line n + 0 on
353	WDA01	Continuity line n + 1 on
354	WDA02	Continuity line n + 2 on
355	WDA03	Continuity line n + 3 on
356	WDA04	Continuity line n + 4 on
357	WDA05	Continuity line n + 5 on
360	WDA06	Continuity line n + 6 on
361	WDA07	Continuity line n + 7 on
362	WDA08	Continuity line n + 8 on
363	WDA09	Continuity line n + 9 on
364	WDA10	Continuity line n + 10 on
365	WDA11	Continuity line n + 11 on
366	LHA00	Loop n + 0
367	LHA01	Loop n + 4
370	JLN	Router code = 30
371	JLK	Clear previous route code
372	KAL	Count = 0
373	KBL	Count = 0
374	JBB79	SSMC serial out
375	BDKA	Request SSMC
376	AFB	Parity error
377	QBF	Counting pulse width

DP Option

LME uses the TA and TB option aliases to access the two sets of test points that are located on the DP option. Refer to “TA Option” and “TB Option” later in this Appendix for descriptions of the test points.

DQ Option (Revision 1301)

Test Point	Term	Description
200	JFB	Snooper busy
201	DNE	Nonbusied ClientEcho
202	DNF	Busied ClientEcho
203	DNG	Nonbusied response
204	DNH	Busied response
205	DRA	DMA engine is busy
206	DOE	Packet-to-node request
207	DOF	Write packet-to-node request
210	DRC	Read command
211	DRD	Read done
212	DRE	Write command
213	DRF	Write done
214	DRG	Waiting for BlkInitResp
215	DAD	Engine timeout
216	DRH	Send BlkDone
217	DRJ	Engine to node is busy
220	DTAA	TCB transfer request
221	DTBA	TCB transfer
222	DTK	Read response count = 0
223	rgaa	Send read request
224	DTM	Cc < Nc
225	DTM	Cs < Ns
226	DTO	Cs = 0
227	DTR	VC2 busy
230	DTS	VC3 busy
231	DTT	Error packet
232	DTU	ReadBlkDoneResp
233	DTV	WriteBlkDoneResp
234	WFC	Force engine 1 busy
235	WFE	Force echoes busy
236	WFG	Force echoes non–busy
237	WFI	Force Response busy
240	KAD	Virtual channel 0
241	KAE	Virtual channel 1
242	KAF	Virtual channel 2
243	KAG	Virtual channel 3
244	KAK	Parity error
245	QCR	Responder header word

246	QCS	VC1 response
247	QCT	VC1 header
250	QCA	Hold VC1 first response
251	QCB	Hold VC0 first response
252	QCC	Hold VC0 second response
253	QLA	Enter WriteResp
254	QLJ	Send WriteResp
255	QLHA	Responder busy
256	QLN	Allow WriteResp
257	QLT	WriteResp buffer full
260	RAD	Rank A valid
261	RBD	Rank B valid
262	RDA	Use rank A/B next
263	RGJ	Response read reference busy
264	RHA	Send read request
265	RMCA	Read request stack full
266	–	–
267	–	–
270	WBE	Group 0 on
271	WBG	Group 1 on
272	WBI	Group 2 on
273	WBK	Group 3 on
274	WFK	Force response nonbusy
275	WFM	Block reload NodeLc
276	WFO	Block reload NodeLs
277	KFB	First word valid
300	HBD	TIB data available
301	HCA	Using DMA engine 0
302	DTL	BL not 0
303	HDA00	Counter for reading TIB
304	HEA	Go read TIB
305	JAE	Count = 0
306	JBA	Decrement BL
307	JBC	Send auxiliary data
310	kab	Valid flag
311	KAC	Data flag
312	KAO149	Error bit
313	KAQ149	Error bit
314	KBB	Virtual channel 0 busy
315	KBS	BL error VC0
316	KBO	VC0 scrubbed packet

317	KCB	Virtual ch. 1 busy
320	kcs	BL error VC1
321	KDB	Virtual channel 2 busy
322	KEB	Virtual channel 3 busy
323	KEO	VC3 scrubbed packet
324	LBA	Engine 0 transfer busy
326	LCA	Engine 0 send packet
327	KGI	Group is turned off
330	LCG	Engine to node request
331	LCK	Load output from engine
332	LFF	Buffer full
333	LMC64	Last word flag
334	lmc65	Engine data to node
335	LME	Read reference request to CPU
336	LMF	Go write packet
337	NBA	Engine 0 transfer busy
341	NGA00	C buffer go write
342	QAA	ReadBlkDone
343	qad	WriteBlkDone
344	QAG	ReadBlkInit
345	QAJ	WriteBlkInit
346	qam	Write
347	qap	Read
350	qas	MaintWrite
351	QAV	MaintRead
352	QDD	Send VC0
353	QDP	Send VC0
354	QED	Send VC1 1st word
355	qep	Send VC0 1st word
356	HBW	Abort engine
357	QFP	Send VC0 1st word
360	QKC	Response for this node
361	QLF	Holding WriteResp
362	QLG	Holding ReadResp response
363	HBU	Bad TIB available
364	VAG	SCX clock
365	VFE	Sample even
366	VGE	Sample odd
367	VHE	Output even
370	VIE	Output odd
371	WBA	No flow control (force Cc < Nc)

372	WBB	No flow control (force Cs < Ns)
373	WBC	Group bits 2 and 3
374	WCU	Enter NodeLC/NodeLS
375	WCV	Enter Tc/Ts/Rc/Rs
376	WFA	Force engine 0 busy
377	KMZ	Sequence number match

DT Option (Revision 1102)

Test Point	Term	Description
0200	aaa	Data bit 0 (IAA)
201	dea0	Data bit 0 (IBA)
202	dec0	Data bit 0 or 8 (IBJ)
203	qfca0	Enter C 0
204	qfca1	Enter C 1
205	qfca2	Enter C 2
206	qfca3	Enter C 3
207	qfca4	Enter C 4
210	qfca5	Enter C 5
211	qfca6	Enter C 6
212	qfca7	Enter C 7
213	qfca8	Enter C 8
214	qfca9	Enter C 9
215	qfca10	Enter C 10
216	qfca11	Enter C 11
217	qfca12	Enter C 12
220	qfca13	Enter C 13
221	qfca14	Enter C 14
222	qfca15	Enter C 15
223	gjaa	Readout C address bit 0
224	gjab	Readout C address bit 1
225	gjac	Readout C address bit 2
226	gjad	Readout C address bit 3
227	qiac2	Load engine data
230	qiaa2	Enter engine data
231	laa2	Enter test parity
232	qiae1	Load fast data
233	qiad3	Force error code
240	eh00	Level 1 parity generation node interface
241	eh01	Level 1 parity generation node interface
242	eh02	Level 1 parity generation node interface

243	eb02	Parity bit to RAM 0 – 3
244	ee02	Parity bit to RAM 4 – 7
246	faf0	Write address bit 0
247	faf1	Write address bit 1
250	faf2	Write address bit 2
251	faf3	Write address bit 3
252	faf4	Write address bit 4
253	faf5	Write address bit 5
254	fcb0	Write address bit 0
255	fcb1	Write address bit 1
256	fcb2	Write address bit 2
257	fcb3	Write address bit 3
260	fcb4	Write address bit 4
261	fcb5	Write address bit 5
262	ffa0	Go write RAM 0
263	ffa1	Go write RAM 1
264	ffa2	Go write RAM 2
265	ffa3	Go write RAM 3
266	ffa4	Go write RAM 4
267	ffa5	Go write RAM 5
270	ffa6	Go write RAM 6
271	ffa7	Go write RAM 7
272	gaa0	Read address bit 0
273	gaa1	Read address bit 1
274	gaa2	Read address bit 2
275	gaa3	Read address bit 3
276	gaa4	Read address bit 4
277	gaa5	Read address bit 5
300	gaa6	Read address bit 6
301	gaa7	Read address bit 7
302	gaa8	Read address bit 8
303	gaa9	Read address bit 9
304	gje	Advance read address buffer C
305	gje2	Gate first packet
306	gje4	Gate second packet
307	qab	Go write RAMs
310	qeg	Enter C from node A
311	qeh	Enter C from node B
312	raav2	Force even
313	rabv2	Force odd
314	raaa	Data bit 0 node interface

315	raba	Data bit 0 node interface
316	rbda	Data bit 0 node interface A
317	rbav	Sample node A even
320	rcav	Sample node B even
321	valid_a1	Gate node A data
322	valid_b1	Gate node B data
323	rdaa	Clock input
324	rdac	Clock input
325	yi0	Position bit
326	rbbv	Sample Node A odd
327	rcbv	Sample node B odd

SX Option (Revision 2100)

Group 0

Test Point	Term	Description
0	dcdr0	Insert slip symbol (slip1a)
1	dcdr1	Insert slip symbol (slip1a)
2	ebfrn0	Ring clock resync (sync3)
3	ebfrn1	Ring clock resync (sync3)
4	ncdr0	Data enable to bypass0 (go_ncdr)
5	ncdr1	Data enable to bypass1 (go_ncdr)
6	bypass0	Output full from parser0 (rk1full)
7	bypass1	Output full from parser1 (rk1full)
10	sendcntl1	Sendbuffer queue overflow (fifo_overflow)
11	sendcntl0	Sendbuffer queue overflow (fifo_overflow)
12	vc_top	Last symbol of packet to send buffers (qvc_lst_sym_mux1)
13	bypass0	Bypass buffer address wrapped (bypass_overflow)
14	bypass1	Bypass buffer address wrapped (bypass_overflow)
15	–	–
16	–	–
17	rcv0	Positive receive channel data bit 1 (scanda[1])

Group 1

Test Point	Term	Description
0	dcdr0	First half cycle of frame (q2)
1	dcdr1	First half cycle of frame (q2)
2	ebfrn0	Positive clock edge change detected (poschange)

3	ebfrn1	Positive clock edge change detected (poschange)
4	ncdr0	Encoder RAM write address – read address bit 0 (addr_diff[0])
5	ncdr1	Encoder RAM write address – read address bit 0 (addr_diff[0])
6	bypass0	Bypass RAM write address – read address (bypass_empty)
7	bypass1	Bypass RAM write address – read address (bypass_empty)
10	vc_top	Client reset (lreset)
11	vc_chan0	VC0 active (qvc_readout1)
12	sendcntl0	Send data is available – to bypass (senddataavail)
13	sendcnt1	Send data is available – to bypass (senddataavail)
14	sendcntl0	Two words are left to output from a buffer (2wdstogo)
15	sendcntl1	Two words are left to output from a buffer (2wdstogo)
16	vcrec_top	Receive VC0 active (qvc0_active[3])
17	rcv0	Positive receive channel data bit 0 (scanda[0])

Group 2

Test Point	Term	Description
0	dcdr0	Second half cycle of frame (q5)
1	dcdr1	Second half cycle of frame (q5)
2	ebfrn0	Negative clock edge change detected (negchange)
3	ebfrn1	Negative clock edge change detected (negchange)
4	ncdr0	Encoder RAM write address – read address bit 1 (addr_diff[1])
5	ncdr1	Encoder RAM write address – read address bit 1 (addr_diff[1])
6	bypass0	Request send buffer (send_bfr_req)
7	bypass1	Request send buffer (send_bfr_req)
10	vcrec_top	Receive VC1 active (qvc1_acive[3])
11	out_port	Express flag from client (mmr_express)
12	vc_chan1	VC1 active (qvc_readout1)
13	vc_chan0	VC0 negative small buffers are all full (qvc_sneg_full)
14	vc_chan1	VC1 negative small buffers are all full (qvc_sneg_full)
15	vc_chan2	VC2 negative small buffers are all full (qvc_sneg_full)
16	vc_chan3	VC3 negative small buffers are all full (qvc_sneg_full)
17	vcrec_top	Receive VC2 active (qvc2_active[3])

Group 3

Test Point	Term	Description
0	dcdr0	Positive data sym full (rk2afull)
1	dcdr1	Positive data sym full (rk2afull)
2	ebfrn0	Select positive or negative phase (phase_sel)
3	ebfrn1	Select positive or negative phase (phase_sel)

4	ncdr0	Encoder RAM write address – read address bit 2 (addr_diff[2])
5	ncdr1	Encoder RAM write address – read address bit 2 (addr_diff[2])
6	bypass0	Go bit in idle reg (idle_reg[0])
7	bypass0	Go bit in idle reg (idle_reg[0])
10	sendcntl0	From bypass (qsendsymbols)
11	sendcntl1	From bypass (qsendsymbols)
12	out_port	Valid flag from client (Valid)
13	vc_chan2	VC2 active (qvc_readout1)
14	vc_chan0	VC0 positive small buffers are all full (qvc_spos_full)
15	vc_chan1	VC1 positive small buffers are all full (qvc_spos_full)
16	vc_chan2	VC2 positive small buffers are all full (qvc_spos_full)
17	vc_chan3	VC3 positive small buffers are all full (qvc_spos_full)

Group 4

Test Point	Term	Description
0	ncdr0	Frame pulse is valid (validfrm)
1	ncdr1	Frame pulse is valid (validfrm)
2	ebfrn0	Slip symbol detected (slip1)
3	ebfrn1	Slip symbol detected (slip1)
4	ncdr0	Output frame to transmitters (outframe)
5	ncdr1	Output frame to transmitters (outframe)
6	bypass0	Ap bit in idle reg (idle_reg[1])
7	bypass1	Ap bit in idle reg (idle_reg[1])
10	sendcntl0	MMR send buffer has been sent (qclearmmrfull)
11	sendcntl1	MMR send buffer has been sent (qclearmmrfull)
12	out_port	Data flag from client (Data_flag)
13	vc_chan3	VC3 active (qvc_readout1)
14	vc_chan0	VC0 neg large buffers are all full (qvc_lneg_full)
15	vc_chan1	VC1 neg large buffers are all full (qvc_lneg_full)
16	vc_chan2	VC2 neg large buffers are all full (qvc_lneg_full)
17	vc_chan3	VC3 neg large buffers are all full (qvc_lneg_full)

Group 5

Test Point	Term	Description
0	dcdr0	Frame error positive phase (frmerrp)
1	dcdr1	Frame error positive phase (frmerrp)
2	ebfrn0	Posfull or negfull from ebfr.ring (outfull)
3	ebfrn1	Posfull or negfull from ebfr.ring (outfull)
4	vcrec_top	Receive VC3 active (qvc3_active[3])

5	vcrec_top	Last symbol to in_port (VC_Last_Symbol_r)
6	bypass0	Cd bit in idle reg (idle_reg[2])
7	bypass1	Cd bit in idle reg (idle_reg[2])
10	parser0	Buffer for maint reads/writes if full (Qbuffullmnt_r)
11	parser1	Buffer for maint reads/writes if full (Qbuffullmnt_r)
12	out_port	Command decode bit 0 from client (cmd_dcd[0])
13	scxtop	Positive ring clock shifted 270 degrees (Pos_rclkbcore)
14	vc_chan0	VC0 positive large buffers are all full (qvc_lpos_full)
15	vc_chan1	VC1 positive large buffers are all full (qvc_lpos_full)
16	vc_chan2	VC2 positive large buffers are all full (qvc_lpos_full)
17	vc_chan3	VC3 positive large buffers are all full (qvc_lpos_full)

Group 6

Test Point	Term	Description
0	dcdr0	Frame error negative phase (frmerrn)
1	dcdr1	Frame error negative phase (frmerrn)
2	ebfrn0	Ring clock (rclk)
3	ebfrn1	Ring clock (rclk)
4	out_port	Data bit 0 from client (C_data[0])
5	–	–
6	bypass0	MUX select bit 0 to bigmux (mux_select[0])
7	bypass1	MUX select bit 0 to bigmux (mux_select[0])
10	out_port	Command decode bit 1 from client (cmd_dcd[1])
11	vcrec_top	VC0 symbol credits = 0 (vc0_sym_min)
12	vcrec_top	VC1 symbol credits = 0 (vc1_sym_min)
13	vcrec_top	VC2 symbol credits = 0 (vc2_sym_min)
14	vcrec_top	VC3 symbol credits = 0 (vc3_sym_min)
15	–	–
16	ebfrn0	75 MHz node clock (node_clock)
17	ebfrn1	75 MHz node clock (node_clock)

Group 7

Test Point	Term	Description
0	scxtop	Positive ring clock shifted 90 degrees (Pos_rclkacore)
1	scxtop	Tap controller is active (tap_active)
2	scxtop	75 MHz node clock (node_clock)
3	scxtop	75 MHz node clock (node_clock)
4	scxtop	Clock from client (client_clock)
5	scxtop	Power-on reset (POR)

6	bypass0	MUX select bit 1 to bigmux (mux_select[1])
7	bypass1	MUX select bit 1 to bigmux (mux_select[1])
10	vcrec_chan0	VC0 receive packet credits = 0 (vc_pkt_min)
11	vcrec_chan1	VC1 receive packet credits = 0 (vc_pkt_min)
12	vcrec_chan2	VC2 receive packet credits = 0 (vc_pkt_min)
13	vcrec_chan3	VC3 receive packet credits = 0 (vc_pkt_min)
14	sendcntl0	Sendbuffer queue underflow (fifo_underflow)
15	sendcntl1	Sendbuffer queue underflow (fifo_underflow)
16	parser0	Parity error in parser (badparityup or badparitylow)
17	parser1	Parity error in parser (badparityup or badparitylow)

TA Option

NOTE: The TA option is an alias that LME uses to access one set of test points on the DP option. (The TB option is the alias that LME uses to access the other set of test points on the DP option.)

Test Point	Term	Description
200	CCA	Snooper busy
201	CCB	Discard packet
202	CCC	Error flag
203	CCE	Message packet
204	CCF00	Total buffer space bit 0
205	CCF01	Total buffer space bit 1
206	CCF02	Total buffer space bit 2
207	CCF03	Total buffer space bit 3
210	CCF04	Total buffer space bit 4
211	CCF05	Total buffer space bit 5
212	CCF06	Total buffer space bit 6
213	CCF07	Total buffer space bit 7
214	CCF08	Total buffer space bit 8
215	CCG	Buffer space available
216	CCH	Overcommitted
217	CCI00	VC1 packet acknowledges
220	CCI01	VC1 packet acknowledges
221	GAT	Go write buffer 2 node A
222	CCJ00	VC2 packet acknowledges
223	CCJ01	VC2 packet acknowledges
224	GFC	Buffer C reference request node A
225	CCK	VC1 packet acknowledges
226	CCL	VC2 packet acknowledges

227	CAN	Readout data available
230	CCM00	Number of words in dh buffer
231	CCM01	Number of words in dh buffer
232	CCM02	Number of words in dh buffer
233	CCM03	Number of words in dh buffer
234	CCM04	Number of words in dh buffer
235	CCM05	Number of words in dh buffer
236	CCM06	Number of words in dh buffer
237	GGA	Express packet node A
240	CCO	Allow Annex™ reference
241	DEA	Snooper busy
242	DEB	Error packet
243	DAE00	Buffer write address bit 0
244	EAA45	Bit 45 from node chip
245	EAA46	Bit 46 from node chip
246	EAA49	Bit 49 from node chip
247	EAA44	Bit 44 from node chip
250	DAE05	Buffer write address bit 5
251	DAE06	Buffer write address bit 6
252	DEC00	Number of words in buffer 1 bit 0
253	DEC01	Number of words in buffer 1 bit 1
254	DEC02	Number of words in buffer 1 bit 2
255	DEC03	Number of words in buffer 1 bit 3
256	DEC04	Number of words in buffer 1 bit 4
257	DEC05	Number of words in buffer 1 bit 5
260	DED00	Number of word acknowledges
261	DED01	Number of word acknowledges
262	DED02	Number of word acknowledges
263	ECC18	Bit 18 from node chip
264	DAE01	Buffer write address bit 1
265	DAE02	Buffer write address bit 2
266	DAE03	Buffer write address bit 3
267	DAE04	Buffer write address bit 4
270	DAO	Readout data available
271	DFA	Snooper busy
272	DFB	Error packet
273	DBE00	Buffer write address bit 0
274	DBE01	Buffer write address bit 1
275	DBE02	Buffer write address bit 2
276	DBE03	Buffer write address bit 3
277	DBE04	Buffer write address bit 4

300	DBE05	Buffer write address bit 5
301	GDB	–
302	DFC00	Number of words in buffer 1 bit 0
303	DFC01	Number of words in buffer 1 bit 1
304	DFC02	Number of words in buffer 1 bit 2
305	DFC03	Number of words in buffer 1 bit 3
306	DFC04	Number of words in buffer 1 bit 4
307	DFC05	Number of words in buffer 1 bit 5
310	DFD00	Number of word acknowledges bit 0
311	DFD01	Number of word acknowledges bit 1
312	DFD02	Number of word acknowledges bit 2
313	DFD03	Number of word acknowledges bit 3
314	DFD04	Number of word acknowledges bit 4
315	DFD05	Number of word acknowledges bit 5
316	GGC	Express packet leaving B1
317	GGF	Express packet leaving B1
320	DBO	Readout data available
321	MCA	Buffer available
322	mcb	VC1 word acknowledges available
323	MCC	VC3 header available
324	MCD	Engine to node request
325	MCE	Go VC3
326	MCF	Go read header
327	MCG	Go read data buffer
330	MCH	Decrement word acknowledge
331	MAE	Valid flag
332	MCJ	Write header
333	MCK	Read response header
334	MCL	VC0 acknowledges = 0
335	MCM	VC1 acknowledges = 0
336	MCN	VC3 acknowledges = 0
337	MCO	VC0 committed words >= 12
340	MCP	VC0 buffer full, stop engine
341	MCQ	Write response counter = 0
342	MCR	Write response buffer full
343	MCS	Response buffer full
344	MCT	Response buffer full
345	MCU	Read request stack full
346	MCV	MWRRESP counter = 0
347	EAD	DH buffer read, node A
350	EAO	Data flag

351	ECA01	Virtual channel 0 node A
352	ECB01	Virtual channel 0 node B
353	EBC	Virtual channel 1 or 2 node A
354	EEB09	Go write buffer
355	EEB10	Type flag 0
356	EEB11	Last word flag
357	EEB12	Scrubbed packet flag
360	GBB	Last word flag node B
361	GBF	Go read node B
362	GDQ	Go VC0 reference node A
363	GDS	Go VC3 reference node A
364	EAR	Parity error
365	WCA	Hard reset Node A
366	WCC	Soft reset Node A
367	WCE	Client reset Node A
370	WFC	Force parity maintenance node A group 0
371	WFE	Force parity maintenance node A group 1
372	WFG	Force parity maintenance node A group 2
373	WFI	Force parity maintenance node A group 3
374	WFS	Force word acknowledges = 1 Node B
375	WFU	Force echoes to error stream node A
376	WFW	Force echoes to error stream node B
377	EAH	Node A clock

TB Option

NOTE: The TB option is an alias that LME uses to access one set of test points on the DP option. (The TA option is the alias that LME uses to access the other set of test points on the DP option.)

Test Point	Term	Description
200	CDA	Snooper busy node B
201	CDB	Discard packet node B
202	CDC	Error flag node B
203	CDE	Message packet node B
204	CDF00	Total buffer space bit 0 node B
205	CDF01	Total buffer space bit 1 node B
206	CDF02	Total buffer space bit 2 node B
207	CDF03	Total buffer space bit 3 node B
210	CDF04	Total buffer space bit 4 node B
211	CDF05	Total buffer space bit 5 node B

212	CDF06	Total buffer space bit 6 node B
213	CDF07	Total buffer space bit 7 node B
214	CDF08	Total buffer space bit 8 node B
215	CDG	Buffer space available
216	CDH	Overcommitted
217	CDI00	VC1 packet acknowledges
220	CDI01	VC1 packet acknowledges
221	GBT	Go write buffer 2 node B
222	CDJ00	VC2 packet acknowledges
223	CDJ01	VC2 packet acknowledges
224	GFE	Buffer C to buffer 2 node B
225	CDK	VC1 packet acknowledges
226	CDL	VC2 packet acknowledges
227	CBN	Readout data available
230	CDM00	Words in dh buffer bit 0
231	CDM01	Words in dh buffer bit 1
232	CDM02	Words in dh buffer bit 2
233	CDM03	Words in dh buffer bit 3
234	CDM04	Words in dh buffer bit 4
235	CDM05	Words in dh buffer bit 5
236	CDM06	Words in dh buffer bit 6
237	GGD	Express packet node B
240	CDO	Allow Annex reference
241	DGA	Snooper busy
242	DGB	Error packet
243	DCE00	Buffer write address bit 0
244	DCE01	Buffer write address bit 1
245	DCE02	Buffer write address bit 2
246	DCE03	Buffer write address bit 3
247	DCE04	Buffer write address bit 4
250	DCE05	Buffer write address bit 5
251	DCE06	Buffer write address bit 6
252	DGC00	Number of words in buffer 1 bit 0
253	DGC01	Number of words in buffer 1 bit 1
254	DGC02	Number of words in buffer 1 bit 2
255	DGC03	Number of words in buffer 1 bit 3
256	DGC04	Number of words in buffer 1 bit 4
257	DGC05	Number of words in buffer 1 bit 5
260	DGD00	Number of word acknowledges
261	DGD01	Number of word acknowledges
262	DGD02	Number of word acknowledges

263	ECC43	Bit 43 from node chip
264	DAQ	Increment word acknowledge
265	DEE	Buffer full
266	DCQ	Increment word acknowledge
267	DGE	Buffer full
270	DCO	Readout data available
271	DHA	Snooper busy
272	DHB	Error packet
273	DDE00	Buffer write address bit 0
274	DDE01	Buffer write address bit 1
275	DDE02	Buffer write address bit 2
276	DDE03	Buffer write address bit 3
277	DDE04	Buffer write address bit 4
300	DDE05	Buffer write address bit 5
301	GEB	–
302	DHC00	Number of words in buffer 1
303	DHC01	Number of words in buffer 1
304	DHC02	Number of words in buffer 1
305	DHC03	Number of words in buffer 1
306	DHC04	Number of words in buffer 1
307	DHC05	Number of words in buffer 1
310	DHD00	Number of word acknowledges
311	DHD01	Number of word acknowledges
312	DHD02	Number of word acknowledges
313	DHD03	Number of word acknowledges
314	DHD04	Number of word acknowledges
315	DHD05	Number of word acknowledges
316	GFMB	Buffer C to B2 node A
317	GFNB	Buffer C to B2 node B
320	DDO	Readout data available
321	MDA	Buffer available
322	mdb	VC1 word acks available
323	MDC	VC3 header available
324	MDD	Engine to node request
325	MDE	Go VC3
326	MDF	Go read header
327	MDG	go read data buffer
330	MDH	Decrement word acknowledge
331	MBE	Valid flag
332	MDJ	Write header
333	MDK	Read response header

334	MDL	VC0 acks = 0
335	MDM	VC1 acks = 0
336	MDN	VC3 acks = 0
337	MDO	VC0 committed words >= 12
340	MDP	VC0 buffer full, stop engine
341	MDQ	Write response counter = 0
342	MDR	Write response buffer full
343	MDS	Response buffer full
344	MDT	Response buffer full
345	MDU	Read request stack full
346	MDV	MWRRESP counter = 0
347	EAE	DH buffer read
350	EBE	Virtual channel 1 or 2 node B
351	EBF	Virtual channel 3 node A
352	EBG	Virtual channel 3 node B
353	EBJ	Express flag
354	EEB13	Type flag 1
355	EEB14	Force parity maintenance
356	GAB	Last word flag
357	GAF	Go read node A
360	GDU	Go C buffer reference
361	GEQ	Go VC0 reference
362	GES	Go VC3 reference
363	GEU	Go C buffer reference
364	WCG	Hard reset node B
365	WCI	Soft reset node B
366	WCK	Client reset node B
367	WFA	Force word acknowledges = 1(node A)
370	WFK	Force parity maintenance node B group 0
371	WFM	Force parity maintenance node B group 1
372	WFO	Force parity maintenance node B group 2
373	WFQ	Force parity maintenance node B group 3
374	EAK	Node chip clock
375	EALC	–
376	EAMC	–
377	GCA	–

Network Module (NW01) Test Points

This section lists the test points that are built into the options on the network module. A brief description of each option is also included.

LA Option (Revision 1005)

Test Point	Term	Description
200	lak	CP-to-CM lower path input FIFO buffer F full – inverted
201	LAO	CP-to-CM lower path input valid
202	QIV	CP-to-CM lower path valid sent to LB option
203	QIG	CP-to-CM lower path maximum output valid count
204	NCQ	CP-to-CM lower path write reference
205	QAYA	CP-to-CM lower path output valid to LB option
206	QIW	CP-to-CM lower path resume from LB option
207	NCA	CP-to-CM lower path subsection bit fanout
210	NCI	CP-to-CM lower path bank/subsection bit
211	NCJ	CP-to-CM lower path bank/subsection bit
212	NCK	CP-to-CM lower path bank/subsection bit
213	–	–
214	lbk	CP-to-CM upper path input FIFO buffer F full – inverted
215	LBO	CP-to-CM upper path input valid
216	QJV	CP-to-CM upper path valid sent to LB option
217	QJG	CP-to-CM upper path maximum output valid count
220	NCS	CP-to-CM upper path write reference
221	QAZA	CP-to-CM upper path output valid to LB option
222	QJW	CP-to-CM upper path resume from LB option
223	NCE	CP-to-CM upper path subsection bit fanout
224	NCL	CP-to-CM upper path bank/subsection bit
225	NCM	CP-to-CM upper path bank/subsection bit
226	NCN	CP-to-CM upper path bank/subsection bit
227	–	–
230	LEB	CM-to-CP processor n + 0 output buffer full
231	LFB	CM-to-CP processor n + 1 output buffer full
232	NLA	CM-to-CP resume to subsection n + 0
233	NMA	CM-to-CP resume to subsection n + 1
234	lcj1	CM-to-CP input valid from subsection n + 0
235	lci1	CM-to-CP shift input flags for subsection n + 0
236	lca	CM-to-CP input FIFO buffer A full for subsection n + 0
237	lcc	CM-to-CP input FIFO buffer B full for subsection n + 0

240	lce	CM-to-CP input FIFO buffer C full for subsection n + 0
241	lcg	CM-to-CP input FIFO buffer D full for subsection n + 0
242	ecl	CM-to-CP processor n + 0 selected for subsection n + 0
243	ecm	CM-to-CP processor n + 1 selected for subsection n + 0
244	ldj1	CM-to-CP input valid from subsection n + 1
245	ldi1	CM-to-CP shift input flags for subsection n + 1
246	lda	CM-to-CP input FIFO buffer A full for subsection n + 1
247	ldc	CM-to-CP input FIFO buffer B full for subsection n + 1
250	lde	CM-to-CP input FIFO buffer C full for subsection n + 1
251	ldg	CM-to-CP input FIFO buffer D full for subsection n + 1
252	fcl	CM-to-CP processor n + 0 selected for subsection n + 1
253	fcm	CM-to-CP processor n + 1 selected for subsection n + 1
254	QKK	CM-to-CP processor n + 0 maximum valids sent
255	QLK	CM-to-CP processor n + 1 maximum valids sent
256	QKT	CM-to-CP resume from processor n + 0
257	QLT	CM-to-CP resume from processor n + 1
260	NIX	CM-to-CP valid to processor n + 0
261	NKX	CM-to-CP valid to processor n + 1
262	–	–
263	–	–
264	YYO	Sanity code
265	YYR	Sanity detected
266	YYU	Maintenance channel return
267	YYX	Test point return
270	QYI	Upper CP-to-CM enable valids and master clears
271	QYR	Code detected from upper memory
272	QXI	Lower CP-to-CM enable valids and master clears
273	QXR	Code detected from lower memory
274	–	–
275	–	–
276	–	–
277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–

311	–	–
312	–	–
313	–	–
314	–	–
315	–	–
316	–	–
317	–	–
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–
337	–	–
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–

362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	–	–

LB Option (Revision 1003)

Test Point	Term	Description
200	kab	Input A output A request buffer full
201	kae	Input A output B request buffer full
202	kah	Input A output C request buffer full
203	kak	Input A output D request buffer full
204	lab	Input A FIFO buffer A full
205	lad	Input A FIFO buffer B full
206	laf	Input A FIFO buffer C full
207	lah	Input A FIFO buffer D full
210	LAN	Input A valid reference
211	JAJ	Resume to input A
212	aay	Input A write reference in FIFO buffer A – inverted
213	–	–
214	kbb	Input B output A request buffer full
215	kbe	Input B output B request buffer full
216	kbh	Input B output C request buffer full
217	kbk	Input B output D request buffer full
220	lbb	Input B FIFO buffer A full
221	lbd	Input B FIFO buffer B full
222	lbf	Input B FIFO buffer C Full
223	lbh	Input B FIFO buffer D Full
224	LBN	Input B valid reference
225	JBJ	Resume to input B
226	bay	Input B write reference in FIFO buffer A – inverted

227	–	–
230	kcb	Input C output A request buffer full
231	kce	Input C output B request buffer full
232	kch	Input C output C request buffer full
233	kck	Input C output D request buffer full
234	lcb	Input C FIFO buffer A full
235	lcd	Input C FIFO buffer B full
236	lcf	Input C FIFO buffer C full
237	lch	Input C FIFO buffer D full
240	LCN	Input C valid reference
241	JCJ	Resume to input C
242	cay	Input C write reference in FIFO buffer A – inverted
243	–	–
244	kdb	Input D output A request buffer full
245	kde	Input D output B request buffer full
246	kdh	Input D output C request buffer full
247	kdk	Input D output D request buffer full
250	ldb	Input D FIFO buffer A full
251	ldd	Input D FIFO buffer B full
252	ldf	Input D FIFO buffer C full
253	ldh	Input D FIFO buffer D full
254	LDN	Input D valid reference
255	JDJ	Resume to input D
256	day	Input D write reference in FIFO buffer A – inverted
257	–	–
260	keb	Output A buffer
261	NAX	Output A valid reference
262	QIG	Output A maximum valid count
263	QIO	Resume from output A
264	kfb	Output B buffer
265	NBX	Output B valid reference
266	QJG	Output B maximum valid count
267	QJO	Resume from output B
270	kgb	Output C buffer
271	NCX	Output C valid reference
272	QKG	Output C maximum valid count
273	QKO	Resume from output C
274	khb	Output D buffer
275	NDX	Output D valid reference
276	QLG	Output D maximum valid count
277	QLO	Resume from output D

300	lea	Input E FIFO buffer A full
301	lec	Input E FIFO buffer B full
302	lee	Input E FIFO buffer C full
303	leg	Input E FIFO buffer D full
304	KID	Input E output E request buffer full
305	KIG	Input E output F request buffer full
306	KIJ	Input E output G request buffer full
307	KIM	Input E output H request buffer full
310	LEM	Input E valid reference
311	JFI	Resume to input E
312	LFM	Input F valid reference
313	JGI	Resume to input F
314	lfa	Input F FIFO buffer A full
315	lfc	Input F FIFO buffer B full
316	lfe	Input F FIFO buffer C full
317	lfg	Input F FIFO buffer D full
320	KJD	Input F output E request buffer full
321	KJG	Input F output F request buffer full
322	KJJ	Input F output G request buffer full
323	KJM	Input F output H request buffer full
324	KKD	Input G output E request buffer full
325	KKG	Input G output F request buffer full
326	KKJ	Input G output G request buffer full
327	KKM	Input G output H request buffer full
330	LGM	Input G valid reference
331	JHI	Resume to input G
332	LHM	Input G valid reference
333	JII	Resume to input H
334	lha	Input H FIFO buffer A full
335	lhc	Input H FIFO buffer B full
336	lhe	Input H FIFO buffer C full
337	lhg	Input H FIFO buffer D full
340	KLD	Input H output E request buffer full
341	KLG	Input H output F request buffer full
342	KLJ	Input H output G request buffer full
343	KLM	Input H output H request buffer full
344	KMA	Output buffer E full
345	NIZ	Output E valid reference
346	RIO	Resume from output E
347	RIH	Output E maximum valid count
350	KNA	Output buffer F full

351	NJZ	Output F valid reference
352	RJO	Resume from output F
353	RJH	Output F maximum valid count
354	KOA	Output buffer G full
355	NKZ	Output G valid reference
356	RKO	Resume from output G
357	RKH	Output G maximum valid count
360	KPA	Output buffer H full
361	NLZ	Output H valid reference
362	RLO	Resume from output H
363	RLH	Output H maximum valid count
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	–	–

LC Option (Revision 1008)

Test Point	Term	Description
200	lab	Input FIFO buffer A full processor n + 0 to memory
201	lad	Input FIFO buffer B full processor n + 0 to memory
202	laf	Input FIFO buffer C full processor n + 0 to memory
203	lah	Input FIFO buffer D full processor n + 0 to memory
204	LAK	Shift processor n + 0 input FIFOs
205	LAL	Valid reference for processor n + 0
206	AIO	Write reference for processor n + 0
207	AIJ0	Steer Processor n + 0 to subsection n + 0
210	AIJ1	Steer processor n + 0 to subsection n + 1
211	NIB	Resume to processor n + 0
212	AIK	Processor n + 0 control bit 0
213	AIL	Processor n + 0 Control bit 1
214	lbb	Input FIFO buffer A full processor n + 1 to memory
215	lbd	Input FIFO buffer B full processor n + 1 to memory

216	lbf	Input FIFO buffer C full processor n + 1 to memory
217	lbh	Input FIFO buffer D full processor n + 1 to memory
220	LBK	Shift processor n + 1 input FIFOs
221	LBL	Valid reference for processor n + 1
222	BIO	Write reference for processor n + 1
223	BIJ0	Steer processor n + 1 to subsection n + 0
224	BIJ1	Steer processor n + 1 to subsection n + 1
225	NID	Resume to processor n + 1
226	BIK	Processor n + 1 control bit 0
227	BIL	Processor n + 1 control bit 1
230	lcb	Input FIFO buffer A full memory to processor lower path
231	lcd	Input FIFO buffer B full memory to processor lower path
232	lcf	Input FIFO buffer C full memory to processor lower path
233	lch	Input FIFO buffer D full memory to processor lower path
234	lcj	Input FIFO buffer E full memory to processor lower path
235	lcl	Input FIFO buffer F full memory to processor lower path
236	lcn	Memory to processor input valid lower path
237	rit	Valid to processor lower path
240	rih	Maximum output valid count for processor lower path
241	riv	Enable valid detection due to good sanity code lower path
242	ris	Resume from processor lower path
243	nfa	Memory to processor lower path destination code bit 0 FIFO A
244	nfb	Memory to processor lower path destination code bit 1 FIFO A
245	nfc	Memory to processor lower path destination code bit 2 FIFO A
246	nfd	Memory to processor lower path destination code bit 3 FIFO A
247	nfe	Memory to processor lower path destination code bit 4 FIFO A
250	ldb	Input FIFO buffer A full memory to processor upper path
251	ldd	Input FIFO buffer B full memory to processor upper path
252	ldf	Input FIFO buffer C full memory to processor upper path
253	ldh	Input FIFO buffer D full memory to processor upper path
254	ldj	Input FIFO buffer E full memory to processor upper path
255	ldl	Input FIFO buffer F full memory to processor upper path
256	ldn	Memory to processor input valid upper path
257	rjt	Valid to processor upper path
260	rjh	Maximum output valid count for processor upper path
261	rjv	Enable valid detection due to good sanity code upper path
262	rjs	Resume from processor upper path
263	nff	Memory to processor upper path destination code bit 0 FIFO A
264	nfg	Memory to processor upper path destination code bit 1 FIFO A
265	nfh	Memory to processor upper path destination code bit 2 FIFO A
266	nfi	Memory to processor upper path destination code bit 3 FIFO A

267	nfj	Memory to processor upper path destination code bit 4 FIFO A
270	lea	Processor to memory output buffer 0 full flag
271	lec	Enable processor n + 0 to subsection n + 0 output
272	led	Enable processor n + 1 to subsection n + 0 output
273	lei	Write reference detected going out to subsection n + 0 output
274	qkl	Subsection n + 0 maximum output valid count
275	qks	Resume from subsection n + 0
276	qkb	Subsection n + 0 output valid count = 1
277	qkd	Subsection n + 0 output valid count = 2
300	lfa	Processor to memory output buffer 1 full flag
301	lfc	Enable processor n + 0 to subsection n + 1 output
302	lfd	Enable processor n + 1 to subsection n + 1 output
303	lfi	Write reference detected going out to subsection n + 1 output
304	qll	Subsection n + 1 maximum output valid count
305	qls	Resume from subsection n + 1
306	qlb	Subsection n + 1 output valid count = 1
307	qld	Subsection n + 1 output valid count = 2
310	–	–
311	–	–
312	–	–
313	–	–
314	–	–
315	–	–
316	–	–
317	–	–
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–
337	–	–

340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–
362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	–	–

Shared Module (SR01) Test Points

This section lists the test points that are built into the options on the shared module. A brief description of each option is also included.

NOTE: The SR option does not have test points.

SA Option (Revision 1040)

Test Point	Term	Description
200	pdqb0	CPU 8 fast respond resume from SB
201	phqb0	CPU 0 fast respond resume from SB
202	plqb0	CPU 9 fast respond resume from SB
203	ppqb0	CPU 1 fast respond resume from SB
204	miia0	CPU type reference resume from SC
205	mlia0	CLN type reference resume from SC
206	puab0	Fast respond command to SB bit 0
207	puab1	Fast respond command to SB bit 1
210	puab2	Fast respond command to SB bit 2
211	puab3	Fast respond command to SB bit 3
212	puab4	Fast respond command to SB bit 4
213	puab5	Fast respond command to SB bit 5
214	puaa0	Fast respond valid command
215	puaa1	Fast respond local type reference
216	puad0	Fast respond illegal steering pointer
217	puae0	Fast respond flush/steering pointer
220	puae1	Fast respond flush/steering pointer
221	uadw0	Valid sanity code detected from CPU
222	–	–
223	–	–
224	–	–
225	–	–
226	–	–
227	–	–
230	–	–
231	–	–
232	–	–
233	–	–
234	–	–
235	–	–
236	–	–
237	–	–

240	–	–
241	–	–
242	–	–
243	–	–
244	–	–
245	–	–
246	–	–
247	–	–
250	–	–
251	–	–
252	–	–
253	–	–
254	–	–
255	–	–
256	–	–
257	–	–
260	–	–
261	–	–
262	–	–
263	–	–
264	–	–
265	–	–
266	–	–
267	–	–
270	–	–
271	–	–
272	–	–
273	–	–
274	–	–
275	–	–
276	–	–
277	–	–
300	–	–
301	–	–
302	–	–
303	–	–
304	–	–
305	–	–
306	–	–
307	–	–
310	–	–

311	–	–
312	–	–
313	–	–
314	–	–
315	–	–
316	–	–
317	–	–
320	–	–
321	–	–
322	–	–
323	–	–
324	–	–
325	–	–
326	–	–
327	–	–
330	–	–
331	–	–
332	–	–
333	–	–
334	–	–
335	–	–
336	–	–
337	–	–
340	–	–
341	–	–
342	–	–
343	–	–
344	–	–
345	–	–
346	–	–
347	–	–
350	–	–
351	–	–
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	–	–
361	–	–

362	–	–
363	–	–
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	–	–

SB Option (Revision 1035)

Test Point	Term	Description
200	daaa0	CPU remote return command bit 0
201	daaa1	CPU remote return command bit 1
202	daaa2	CPU remote return command bit 2
203	daaa3	CPU remote return command bit 3
204	daaa4	CPU remote return command bit 4
205	daaa5	CPU remote return command bit 5
206	diaa0	CPU 8 remote return resume flag M
207	dica0	CPU 8 remote return resume flag N
210	diea0	CPU 8 remote return resume flag O
211	diga0	CPU 8 remote return resume flag P
212	dlaa0	CPU 0 remote return resume flag M
213	dlca0	CPU 0 remote return resume flag N
214	dlea0	CPU 0 remote return resume flag O
215	dlga0	CPU 0 remote return resume flag P
216	doaa0	CPU 9 remote return resume flag M
217	doca0	CPU 9 remote return resume flag N
220	doea0	CPU 9 remote return resume flag O
221	doga0	CPU 9 remote return resume flag P
222	draa0	CPU 1 remote return resume flag M
223	drca0	CPU 1 remote return resume flag N
224	drea0	CPU 1 remote return resume flag O
225	drga0	CPU 1 remote return resume flag P
226	duaa0	CPU 8/0/9/1 remote return valid flag M

227	duca0	CPU 8/0/9/1 remote return valid flag N
230	duea0	CPU 8/0/9/1 remote return valid flag O
231	duga0	CPU 8/0/9/1 remote return valid flag P
232	dyaq0	CPU 8/0/9/1 remote return shift control
233	–	–
234	–	–
235	–	–
236	–	–
237	–	–
240	eaaa0	CPU local return command bit 0
241	eaaa1	CPU local return command bit 1
242	eaaa2	CPU local return command bit 2
243	eaaa3	CPU local return command bit 3
244	eaaa4	CPU local return command bit 4
245	eaaa5	CPU local return command bit 5
246	euaa0	CPU local return valid flag A
247	euca0	CPU local return valid flag B
250	euea0	CPU local return valid flag C
251	euga0	CPU local return valid flag D
252	eyaq0	CPU local return shift control
253	–	–
254	–	–
255	–	–
256	–	–
257	–	–
260	faaa0	CPU fast respond return command bit 0
261	faaa1	CPU fast respond return command bit 1
262	faaa2	CPU fast respond return command bit 2
263	faaa3	CPU fast respond return command bit 3
264	faaa4	CPU fast respond return command bit 4
265	faaa5	CPU fast respond return command bit 5
266	fiaa0	CPU fast respond forced data
267	fqba0	CPU no respond valid flag
270	fqda0	–
271	fqfa0	–
272	fqha0	–
273	frma0	CPU no respond valid
274	ftaa0	–
275	fuaa0	CPU fast respond valid flag
276	fuca0	–
277	fuea0	–

300	geba0	CPU remote return valid control
301	gfba0	CPU remote return effective valid control
302	gmba0	CPU local return valid control
303	gnba0	CPU local return effective valid control
304	guba0	CPU fast respond return valid control
305	gvba0	CPU fast respond return effective valid control
306	haba0	CPU local return wins contention
307	hbba0	CPU fast respond return wins contention
310	hcba0	CPU remote return wins contention
311	–	
312	–	
313	–	
314	–	
315	–	
316	–	
317	–	
320	jmaa0	CPU return second packet
321	jnaa0	CPU return shutdown
322	joaa0	CPU return with I/O in progress
323	jpca0	CPU return SRPE second packet
324	JRQE0	Read lowest interrupt channel valid counter
325	JSAE0	Read lowest interrupting channel valid
326	QQAE0	Real-time clock (RTC) valid
327	QPQE0	RTC valid counter
330	–	
331	–	
332	–	
333	–	
334	–	
335	–	
336	–	
337	–	
340	naaa0	CPU return RTC wins
341	naba0	CPU return flush wins
342	naca0	CPU return command 051 wins
343	nada0	CPU return instruction 033 wins
344	nbba0	CPU return shutdown in progress
345	niaa0	CPU return flush command in progress
346	nkba0	CPU return shutdown by flush command in progress
347	pdaa0	CPU return instruction 033 source normal return
350	pkma0	CPU return instruction 033 source timer = 0

3351	qaca0	CPU return shutdown by RTC
352	–	–
353	–	–
354	–	–
355	–	–
356	–	–
357	–	–
360	siba0	CPU return command 051 valid flag
361	sida0	
362	sifa0	
363	sjaa0	CPU return command 051 valid
364	smaa0	CPU return shutdown by command 051
365	tmca0	Valid remote shared
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	–	–

SC Option (Revision 1035)

Test Point	Term	Description
200	aae1	Input A broadcast detach detected (inverted)
201	–	–
202	–	–
203	–	–
204	law	Input A shift input FIFOs for cluster commands (inverted)
205	lak	Input A load buffer A FIFO for cluster commands (inverted)
206	lal	Input A load buffer B FIFO for cluster commands (inverted)
207	lam	Input A load buffer C FIFO for cluster commands (inverted)
210	lbw	Input A shift input FIFOs for CPU commands (inverted)
211	lbk	Input A load buffer A FIFO for CPU commands (inverted)
212	lbl	Input A load buffer B FIFO for CPU commands (inverted)
213	–	–
214	bae1	Input B broadcast detach detected (inverted)
215	–	–

216	–	–
217	–	–
220	ldw	Input B shift input FIFOs (inverted)
221	ldk	Input B load buffer A FIFO for cluster commands (inverted)
222	ldl	Input B load buffer B FIFO for cluster commands (inverted)
223	ldm	Input B load buffer C FIFO for cluster commands (inverted)
224	lew	Input B shift input FIFOs for CPU commands (inverted)
225	lek	Input B load buffer A FIFO for CPU commands (inverted)
226	lel	Input B load buffer B FIFO for CPU commands (inverted)
227	–	–
230	cae1	Input C broadcast detach detected (inverted)
231	–	–
232	–	–
233	–	–
234	lgw	Input C shift input FIFOs (inverted)
235	lgk	Input C load buffer A FIFO for cluster commands (inverted)
236	lgl	Input C load buffer B FIFO for cluster commands (inverted)
237	lgm	Input C load buffer C FIFO for cluster commands (inverted)
240	lhw	Input C shift input FIFOs for CPU commands (inverted)
241	lhk	Input C load buffer A FIFO for CPU commands (inverted)
242	lhl	Input C load buffer B FIFO for CPU commands (inverted)
243	–	–
244	dae1	Input D broadcast detach detected (inverted)
245	–	–
246	–	–
247	–	–
250	ljw	Input D shift input FIFOs (inverted)
251	ljk	Input D load buffer A FIFO for cluster commands (inverted)
252	ljl	Input D load buffer B FIFO for cluster commands (inverted)
253	ljm	Input D load buffer C FIFO for cluster commands (inverted)
254	lkw	Input D shift input FIFOs for CPU commands (inverted)
255	lkk	Input D load buffer A FIFO for CPU commands (inverted)
256	lkl	Input D load buffer B FIFO for CPU commands (inverted)
257	–	–
260	lmc0	Input A load cluster 00 – 05 output request buffer (inverted)
261	lmc3	Input A load cluster 06 – 11 output request buffer (inverted)
262	lmc6	Input A load cluster 12 – 17 output request buffer (inverted)
263	lmg0	Input A output request buffer 00 – 05 buffer full (inverted)
264	lmg3	Input A output request buffer 06 – 11 buffer full (inverted)
265	lmg6	Input A output request buffer 12 – 17 buffer full (inverted)
266	lmj1	Input A all output request buffers empty (inverted)

267	–	–
270	loc0	Input B load cluster 00 – 05 output request buffer (inverted)
271	loc3	Input B load cluster 06 – 11 output request buffer (inverted)
272	loc6	Input B load cluster 12 – 17 output request buffer (inverted)
273	log0	Input B output request buffer 00 – 05 buffer full (inverted)
274	log3	Input B output request buffer 06 – 11 buffer full (inverted)
275	log6	Input B output request buffer 12 – 17 buffer full (inverted)
276	loj1	Input B all output request buffers empty (inverted)
277	–	–
300	lqc0	Input C load cluster 00 – 05 output request buffer (inverted)
301	lqc3	Input C load cluster 06 – 11 output request buffer (inverted)
302	lqc6	Input C load cluster 12 – 17 output request buffer (inverted)
303	lqg0	Input C output request buffer 00 – 05 buffer full (inverted)
304	lqg3	Input C output request buffer 06 – 11 buffer full (inverted)
305	lqg6	Input C output request buffer 12 – 17 buffer full (inverted)
306	lqj1	Input C all output request buffers empty (inverted)
307	–	–
310	lsc0	Input D load cluster 00 – 05 output request buffer (inverted)
311	lsc3	Input D load cluster 06 – 11 output request buffer (inverted)
312	lsc6	Input D load cluster 12 – 17 output request buffer (inverted)
313	lsg0	Input D output request buffer 00 – 05 buffer full (inverted)
314	lsg3	Input D output request buffer 06 – 11 buffer full (inverted)
315	lsg6	Input D output request buffer 12 – 17 buffer full (inverted)
316	lsj1	Input D all output request buffers empty (inverted)
317	–	–
320	lto	Enable input A request buffer to CPU output (inverted)
321	ltp	Enable input B request buffer to CPU output (inverted)
322	ltq	Enable input C request buffer to CPU output (inverted)
323	ltr	Enable input D request buffer to CPU output (inverted)
324	MAY	Resume from cluster 0/1 output
325	mau	Output counter count = 2 for cluster 0/1 output (inverted)
326	MBY	Resume from cluster 2/3 output
327	mbu	Output counter count = 2 for cluster 2/3 output (inverted)
330	MCY	Resume from cluster 4/5 output
331	mcu	Output counter count = 2 for cluster 4/5 output (inverted)
332	MDY	Resume from cluster 6/7 output
333	mdu	Output counter count = 2 for cluster 6/7 output (inverted)
334	MEY	Resume from cluster 8/9 output
335	meu	Output counter count = 2 for cluster 8/9 output (inverted)
336	MFY	Resume from cluster 10/11 output
337	mfu	Output counter count = 2 for cluster 10/11 output (inverted)

340	MGY	Resume from cluster 12/13 output
341	mgu	Output counter count = 2 for cluster 12/13 output (inverted)
342	MHY	Resume from cluster 14/15 output
343	mhu	Output counter count = 2 for cluster 14/15 output (inverted)
344	MIY	Resume from cluster 16/17 output
345	miu	Output counter count = 2 for cluster 16/17 output (inverted)
346	–	–
347	–	–
350	mjb	Lower SD output valid count = 1 (inverted)
351	mjd	Lower SD output valid count = 2 (inverted)
352	mji	Lower SD output Resume from SD option (inverted)
353	mjj	Add 1 to lower SD output counter (inverted)
354	mkb	Upper SD output valid count = 1 (inverted)
355	mkd	Upper SD output valid count = 2 (inverted)
356	mki	Upper SD output resume from SD option (inverted)
357	mkj	Add 1 to upper SD output counter (inverted)
360	naa	Resume to n + 0 input (inverted)
361	nae	Resume to n + 1 input (inverted)
362	nai	Resume to R4 input (inverted)
363	nam	Resume to R5 input (inverted)
364	–	–
365	–	–
366	–	–
367	–	–
370	–	–
371	–	–
372	–	–
373	–	–
374	–	–
375	–	–
376	–	–
377	–	–

SD Option (Revision 1022)

Test Point	Term	Description
200	lkn	SR0 reference to output n + 0 request buffer (inverted)
201	lko	SR0 reference to output n + 1 request buffer (inverted)
202	lkp	SR0 reference to output R4 request buffer (inverted)
203	lkq	SR0 reference to output R5 request buffer (inverted)
204	fay	SR0 broadcast reference to n + 0 request buffer (inverted)

205	fby	SR0 broadcast reference to n + 1 request buffer (inverted)
206	–	–
207	–	–
210	lln	SR1 reference to output n + 0 request buffer (inverted)
211	llo	SR1 reference to output n + 1 request buffer (inverted)
212	llp	SR1 reference to output R4 request buffer (inverted)
213	llq	SR1 reference to output R5 request buffer (inverted)
214	fey	SR1 broadcast reference to n + 0 request buffer (inverted)
215	ffy	SR1 broadcast reference to n + 1 request buffer (inverted)
216	–	–
217	–	–
220	lmn	SR2 reference to output n + 0 request buffer (inverted)
221	lmo	SR2 reference to output n + 1 request buffer (inverted)
222	lmp	SR2 reference to output R4 request buffer (inverted)
223	lmq	SR2 reference to output R5 request buffer (inverted)
224	fiy	SR2 broadcast reference to n + 0 request buffer (inverted)
225	fjy	SR2 broadcast reference to n + 1 request buffer (inverted)
226	–	–
227	–	–
230	lnn	SR3 reference to output n + 0 request buffer (inverted)
231	lno	SR3 reference to output n + 1 request buffer (inverted)
232	lnp	SR3 reference to output R4 request buffer (inverted)
233	lnq	SR3 reference to output R5 request buffer (inverted)
234	fmy	SR3 broadcast reference to n + 0 request buffer (inverted)
235	fny	SR3 broadcast reference to n + 1 request buffer (inverted)
236	–	–
237	–	–
240	lon	SR4 reference to output n + 0 request buffer (inverted)
241	loo	SR4 reference to output n + 1 request buffer (inverted)
242	lop	SR4 reference to output R4 request buffer (inverted)
243	loq	SR4 reference to output R5 request buffer (inverted)
244	gay	SR4 broadcast reference to n + 0 request buffer (inverted)
245	gby	SR4 broadcast reference to n + 1 request buffer (inverted)
246	–	–
247	–	–
250	lpn	SR5 reference to output n + 0 request buffer (inverted)
251	lpo	SR5 reference to output n + 1 request buffer (inverted)
252	lpp	SR5 reference to output R4 request buffer (inverted)
253	lpq	SR5 reference to output R5 request buffer (inverted)
254	gey	SR5 broadcast reference to n + 0 request buffer (inverted)
255	gfy	SR5 broadcast reference to n + 1 request buffer (inverted)

256	–	–
257	–	–
260	lqn	SR6 reference to output n + 0 request buffer (inverted)
261	lqo	SR6 reference to output n + 1 request buffer (inverted)
262	lqp	SR6 reference to output R4 request buffer (inverted)
263	lqq	SR6 reference to output R5 request buffer (inverted)
264	giy	SR6 broadcast reference to n + 0 request buffer (inverted)
265	gjy	SR6 broadcast reference to n + 1 request buffer (inverted)
266	–	–
267	–	–
270	lrn	SR7 reference to output n + 0 request buffer (inverted)
271	lro	SR7 reference to output n + 1 request buffer (inverted)
272	lrp	SR7 reference to output R4 request buffer (inverted)
273	lrq	SR7 reference to output R5 request buffer (inverted)
274	gmy	SR7 broadcast reference to n + 0 request buffer (inverted)
275	gny	SR7 broadcast reference to n + 1 request buffer (inverted)
276	–	–
277	–	–
300	lsn	SR8 reference to output n + 0 request buffer (inverted)
301	lso	SR8 reference to output n + 1 request buffer (inverted)
302	lsp	SR8 reference to output R4 request buffer (inverted)
303	lsq	SR8 reference to output R5 request buffer (inverted)
304	gqy	SR8 broadcast reference to n + 0 request buffer (inverted)
305	gry	SR8 broadcast reference to n + 1 request buffer (inverted)
306	–	–
307	–	–
310	ltn	CPU reference to output n + 0 request buffer (inverted)
311	lto	CPU reference to output n + 1 request buffer (inverted)
312	ltp	CPU reference to output R4 request buffer (inverted)
313	ltq	CPU reference to output R5 request buffer (inverted)
314	guy	CPU broadcast reference to n + 0 request buffer (inverted)
315	gvy	CPU broadcast reference to n + 1 request buffer (inverted)
316	–	–
317	–	–
320	lub	Group A output n + 0 buffer full
321	lud	Group A output n + 1 buffer full
322	luf	Group A output R4 buffer full
323	luh	Group A output R5 buffer full
324	lvb	Group B output n + 0 buffer full
325	lvd	Group B output n + 1 buffer full
326	lvf	Group B output R4 buffer full

327	lvh	Group B output R5 buffer full
330	qig	Gate group A to n + 0 output
331	qih	Gate group B to n + 0 output
332	–	–
333	–	–
334	qjg	Gate group A to n + 1 output
335	qjh	Gate group B to n + 1 output
336	–	–
337	–	–
340	qkg	Gate group A to R4 output
341	qkh	Gate group B to R4 output
342	–	–
343	–	–
344	qlg	Gate group A to R5 output
345	qlh	Gate group B to R5 output
346	–	–
347	–	–
350	MAJ	Resume from n + 0/0
351	MBJ	Resume from n + 0/1
352	MCJ	Resume from n + 0/2
353	MDJ	Resume from n + 0/3
354	MEJ	Resume from n + 1/0
355	MFJ	Resume from n + 1/1
356	MGJ	Resume from n + 1/2
357	MHJ	Resume from n + 1/3
360	maf	Output n + 0/0 valid reference count = 3
361	mbf	Output n + 0/1 valid reference count = 3
362	mcf	Output n + 0/2 valid reference count = 3
363	mdf	Output n + 0/3 valid reference count = 3
364	mef	Output n + 1/0 valid reference count = 3
365	mff	Output n + 1/1 valid reference count = 3
366	mgf	Output n + 1/2 valid reference count = 3
367	mhf	Output n + 1/3 valid reference count = 3
370	mih	Output R4 valid reference count = 4
371	mii	Output R4 valid reference going out
372	mij	Output R4 resume from remote
373	–	–
374	mjh	Output R4 valid reference count = 4
375	mji	Output R4 valid reference going out
376	mjj	Output R4 resume from remote
377	–	–

SM Option (Revision 1007)

Test Point	Term	Description
200	aag	Sanity Code input from IO module master port 0
201	acg	Sanity Code input from IO module master port 1
202	aeg	Sanity Code input from IO module master port 2
203	agg	Sanity Code input from IO module master port 3
204	aig	Sanity Code input from IO module master port 4
205	BAB	Maintenance channel input to go to the maintenance channel router
206	SCB	Shared position from conn–SM
207	qag	Select Remote shared board or all attached CPUs
210	fag	Select Slave port 0 – CPU 8 (from SM0) or CPU 12 (from SM1)
211	gag	Select Slave port 1 – CPU 0 (from SM0) or CPU 4 (from SM1)
212	hag	Select Slave port 2 – CPU 9 (from SM0) or CPU 13 (from SM1)
213	jag	Select Slave port 3 – CPU 1 (from SM0) or CPU 5 (from SM1)
214	kag	Select Slave port 4 – CPU 10 (from SM0) or CPU 14 (from SM1)
215	lag	Select Slave port 5 – CPU 2 (from SM0) or CPU 6 (from SM1)
216	mag	Select Slave port 6 – CPU 11 (from SM0) or CPU 15 (from SM1)
217	nag	Select Slave port 7 – CPU 3 (from SM0) or CPU 7 (from SM1)
220	ABD	Lock in sync counter recognition for master port 0
221	ADD	Lock in sync counter recognition for master port 1
222	AFD	Lock in sync counter recognition for master port 2
223	AHD	Lock in sync counter recognition for master port 3
224	AJD	Lock in sync counter recognition for master port 4
225	vac	Valid remote shared
226	pib	Error logger from other SM chip arbitration request
227	qib	Error logger from remote shared module arbitration request
230	fib	Slave port 0 – CPU 8 or CPU 12 (arbitration request)
231	gib	Slave port 1 – CPU 0 or CPU 4 (arbitration request)
232	hib	Slave port 2 – CPU 9 or CPU 13 (arbitration request)
233	jib	Slave port 3 – CPU 1 or CPU 5 (arbitration request)
234	kib	Slave port 4 – CPU 10 or CPU 14 (arbitration request)
235	lib	Slave port 5 – CPU 2 or CPU 6 (arbitration request)
236	mib	Slave port 6 – CPU 11 or CPU 15 (arbitration request)
237	nib	Slave port 7 – CPU 3 or CPU 7 (arbitration request)
240	ABS	Resync delayed sanity code for master port 0
241	ADS	Resync delayed sanity code for master port 1
242	AFS	Resync delayed sanity code for master port 2
243	AHS	Resync delayed sanity code for master port 3
244	AJS	Resync delayed sanity code for master port 4
245	AKL	Sanity code enable from other SM

246	pin	Error logger from other SM chip – playback mode after a delayed grant
247	qin	Error logger from remote shared module – playback mode after a delayed grant
250	fin	Slave port 0 – CPU 8 or CPU 12 – playback mode after a delayed grant
251	gin	Slave port 1 – CPU 0 or CPU 4 – playback mode after a delayed grant
252	hin	Slave port 2 – CPU 9 or CPU 13 – playback mode after a delayed grant
253	jin	Slave port 3 – CPU 1 or CPU 5 – playback mode after a delayed grant
254	kin	Slave port 4 – CPU 10 or CPU 14 – playback mode after a delayed grant
255	lin	Slave port 5 – CPU 2 or CPU 6 – playback mode after a delayed grant
256	min	Slave port 6 – CPU 11 or CPU 15 – playback mode after a delayed grant
257	nin	Slave port 7 – CPU 3 or CPU 7 – playback mode after a delayed grant
260	ABP	Maintenance channel + error logger return input for master port 0
261	ADP	Maintenance channel + error logger return input for master port 1
262	AFP	Maintenance channel + error logger return input for master port 2
263	AHP	Maintenance channel + error logger return input for master port 3
264	AJP	Maintenance channel + error logger return input for master port 4
265	alg	Sanity code recognizer from other SM chip
266	PIZ	Error logger from other SM chip, quick data path with playback path
267	QIZ	Error logger from remote shared module, quick data with playback path
270	FIZ	Slave port 0 – CPU 8 or CPU 12 – quick data with playback path
271	GIZ	Slave port 1 – CPU 0 or CPU 4 – quick data with playback path
272	HIZ	Slave port 2 – CPU 9 or CPU 13 – quick data with playback path
273	JIZ	Slave port 3 – CPU 1 or CPU 5 – quick data with playback path
274	KIZ	Slave port 4 – CPU 10 or CPU 14 – quick data with playback path
275	LIZ	Slave port 5 – CPU 2 or CPU 6 – quick data with playback path
276	MIZ	Slave port 6 – CPU 11 or CPU 15 – quick data with playback path
277	NIZ	Slave port 7 – CPU 3 or CPU 7 – quick data with playback path
300	EER	Arbitration between error loggers, with no lockout and granted
301	dbl	Error input from sr001 or sr006, start bit or valid bit
302	dal	Error input from sr000 or sr005, start bit or valid bit
303	ccb	Loop controller, new start pulse on a reselect (37) code.
304	UBI	Error logger output, count >= 78, hold count and drop lockout
305	RAO	Masterclear to logic monitor
306	pjb	Error logger from other SM chip, create 5-bit ELR word when granted
307	qjb	Error logger from remote shared module, create 5-bit ELR word when granted
310	fjc	Slave port 0 – CPU 8 or CPU 12 – create 5-bit ELR word when granted
311	gjc	Slave port 1 – CPU 0 or CPU 4 – create 5-bit ELR word when granted
312	hjc	Slave port 2 – CPU 9 or CPU 13 – create 5-bit ELR word when granted
313	jjc	Slave port 3 – CPU 1 or CPU 5 – create 5-bit ELR word when granted
314	kjc	Slave port 4 – CPU 10 or CPU 14 – create 5-bit ELR word when granted

315	ljc	Slave port 5 – CPU 2 or CPU 6 – create 5-bit ELR word when granted
316	mjc	Slave port 6 – CPU 11 or CPU 15 – create 5-bit ELR word when granted
317	njc	Slave port 7 – CPU 3 or CPU 7 – create 5-bit ELR word when granted
320	ABX	Drive sanity code return if we are recognizing for master port 0
321	ADX	Drive sanity code return if we are recognizing for master port 1
322	AFX	Drive sanity code return if we are recognizing for master port 2
323	AHX	Drive sanity code return if we are recognizing for master port 3
324	UCF	Error logger output, block start bits while counter nonzero
325	anc	Second level arbitration for master port, home port is in other SM
326	pmx	Error logger from other SM chip, count sticks at zero
327	qmx	Error logger from remote shared module, count sticks at zero
330	fmx	Slave port 0 – CPU 8 or CPU 12 – count sticks at zero
331	gmx	Slave port 1 – CPU 0 or CPU 4 – count sticks at zero
332	hmx	Slave port 2 – CPU 9 or CPU 13 – count sticks at zero
333	jmx	Slave port 3 – CPU 1 or CPU 5 – count sticks at zero
334	kmx	Slave port 4 – CPU 10 or CPU 14 – count sticks at zero
335	lmx	Slave port 5 – CPU 2 or CPU 6 – count sticks at zero
336	mmx	Slave port 6 – CPU 11 or CPU 15 – count sticks at zero
337	nmx	Slave port 7 – CPU 3 or CPU 7 – count sticks at zero
340	ABY	Drive out MC return if not the master, master port 0
341	ADY	Drive out MC return if not the master, master port 1
342	AFY	Drive out MC return if not the master, master port 2
343	AHY	Drive out MC return if not the master, master port 3
344	UBL	Error logger output, waiting for ELR; cannot start next output
345	and	Second level arbitration for master port, home port is in other SM
346	SAG	Shared position and chip position, delay local copy to match chip-to-chip copy
347	QLA	Error logger from other SM chip, successful recognition of SCR
350	FLA	Slave port 0 – CPU 8 or CPU 12 – successful recognition of SCR
351	GLA	Slave port 1 – CPU 0 or CPU 4 – successful recognition of SCR
352	HLA	Slave port 2 – CPU 9 or CPU 13 – successful recognition of SCR
353	JLA	Slave port 3 – CPU 1 or CPU 5 – successful recognition of SCR
354	KLA	Slave port 4 – CPU 10 or CPU 14 – successful recognition of SCR
355	LLA	Slave port 5 – CPU 2 or CPU 6 – successful recognition of SCR
356	NLA	Slave port 6 – CPU 11 or CPU 15 – successful recognition of SCR
357	NLA	Slave port 6 – CPU 11 or CPU 15 – successful recognition of SCR
360	ABZ	Drive out error logger if the master for master port 0
361	ADZ	Drive out error logger if the master for master port 1
362	AFZ	Drive out error logger if the master for master port 2
363	AHZ	Drive out error logger if the master for master port 3
364	BGF	Logic monitor interface, data from HM0 (and HM1) if SM0

365	APC	Sanity code to remote shared
366	cea	Loop controller, each loop 0
367	ceb	Loop controller, each loop 1
370	BGB	Logic monitor interface, select logic monitor
371	RBC	Reset from either no sanity code or test mode masterclear to other chips
372	eak	Local error logger, request to arbitrate if error bit is latched
373	eex	Mod-4 counter signal for arbitration between error loggers
374	BBY	Maintenance channel router, valid code, deselect previous
375	bdx	Maintenance channel router, data to the CPUs includes route code only if it is a continuation, and 24-phase delay if going to all attached CPUs
376	eao	Local error logger, sending 64-bit EL message
377	BBW	Maintenance channel router, valid code, is a continuation