CRAY T90™ Series
Hardware Reference Booklet

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Record of Revision

Each time this manual is fully revised and reprinted, all change packets to the previous version are incorporated into the new version, and the new version is assigned an alphabetical revision level, which is indicated in the publication number on each page of the manual. A revised manual does not usually contain change bars.

Each time this booklet is revised and reprinted, all changes issued against the previous version are incorporated into the new version, and the new version is indicated by a new date in the footer.

Changes to part of a page are indicated by a change bar in the margin directly opposite the change. A change bar in the footer indicates that most, if not all, of the page is new. If the booklet is rewritten, the revision level changes but the manual does not contain change bars.

Revision	Description
	May 1995. Original printing.
A	June 1995. Corrects references to chassis quadrants and CPU numbering and adds module maps for CP02 and shared modules.
B	July 1995. Corrects references to chassis quadrants and CPU numbering.
C	October 1995. Corrects references to chassis map for CRAY T916 memory module numbering.
D	June 1996. Adds information about the CM03, IO02, and CPE1 modules, and EZIF controller error codes.
E	March 1997. Adds information about the MWS and OWS cabling and the network module.

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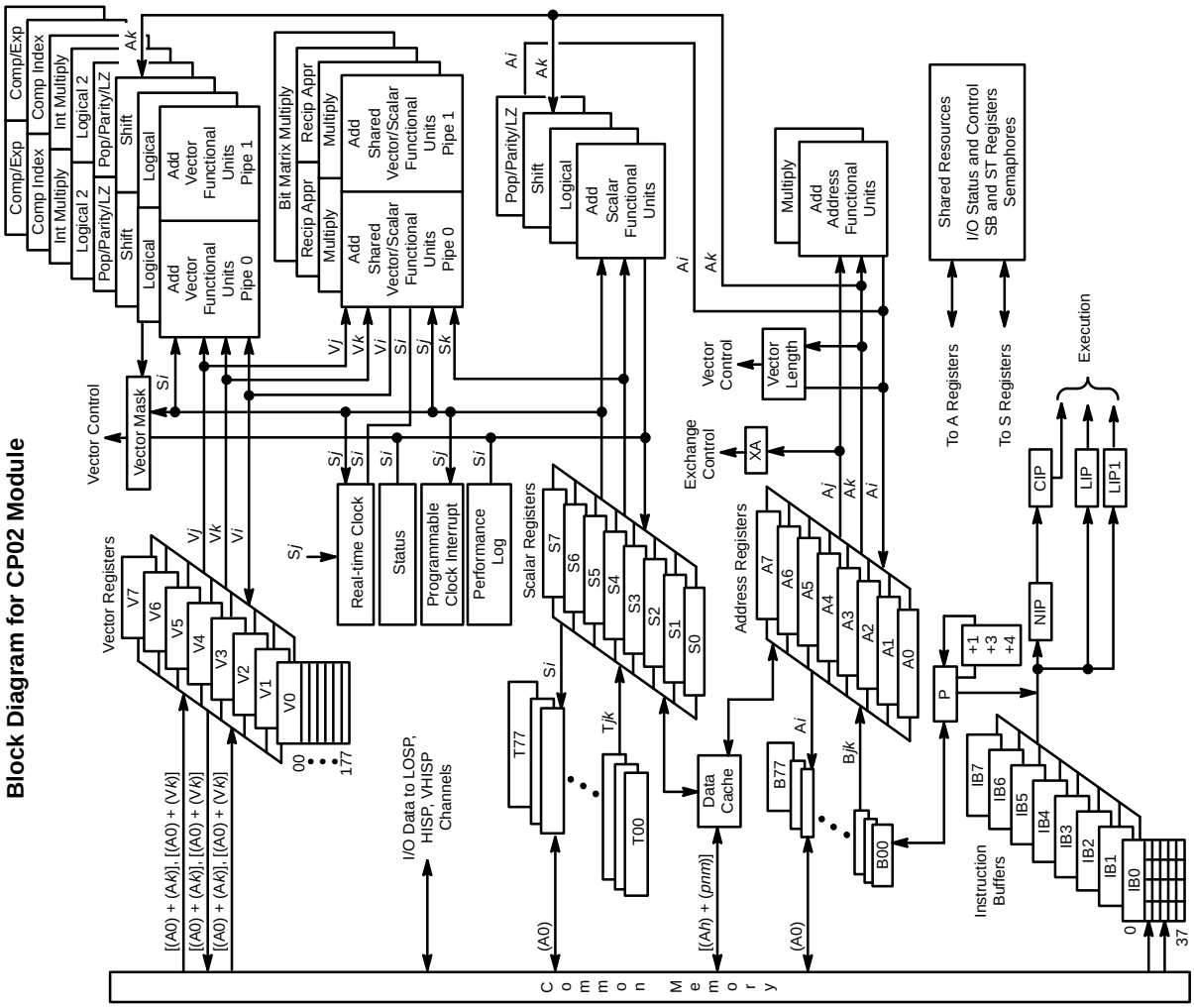
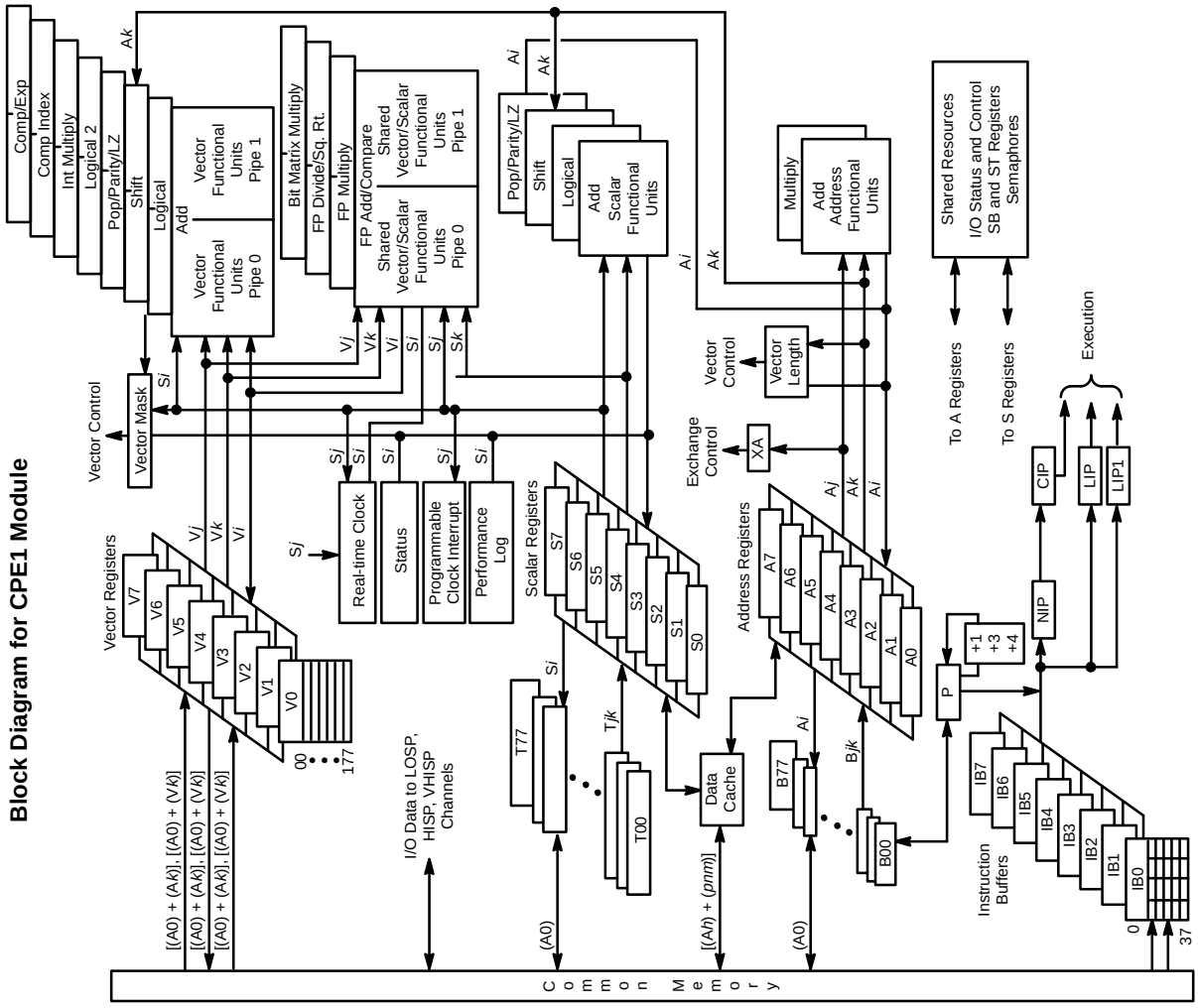
Block Diagram for CP02 Module



Block Diagram for CPE1 Module



Exchange Package

Memory – Absolute

```
ADX 00000000000100
P   0000010135c A0 000000 000000 000000 000000 S0 000000 000000 000000 000000
PN  000         A1 000000 000000 000000 000000 S1 000000 000000 000000 000000
XA  0006000     A2 000000 000000 000000 000000 S2 000000 000000 000000 000000
EA0 0006000     A3 000000 000000 000000 000000 S3 000000 000000 000000 000000
EA1 0006000     A4 000000 000000 000000 000000 S4 000000 000000 000000 000000
EA2 0006000     A5 000000 000000 000000 000000 S5 000000 000000 000000 000000
EA3 0006000     A6 000000 000000 000000 000000 S6 000000 000000 000000 000000
EA4 0006000     A7 000000 000000 000000 000000 S7 000000 000000 000000 000000

CN 000     MODES 000 BR RST EBM    IM 00000000 II III FII III III IFI III III
VL 000               DM MCR SDM               RU FOP EBC MRI IPD MNA XNU ODN
                     D1 OEI LM                PM PRR XPM CTP OCL IXM IXX VVV

STATUS 00 XNU ODN 000 SS **V FWB   IF 00000000 RM FOP EBM MRI IPD MNA XNU ODN
          IXN VVV     BB **N PSM              PE PRR EPE CTC OCL IEM IXN VIV
          SSS SSS     MU **U S L              EU EEE XIC UIP II  IXI   F FVI
```

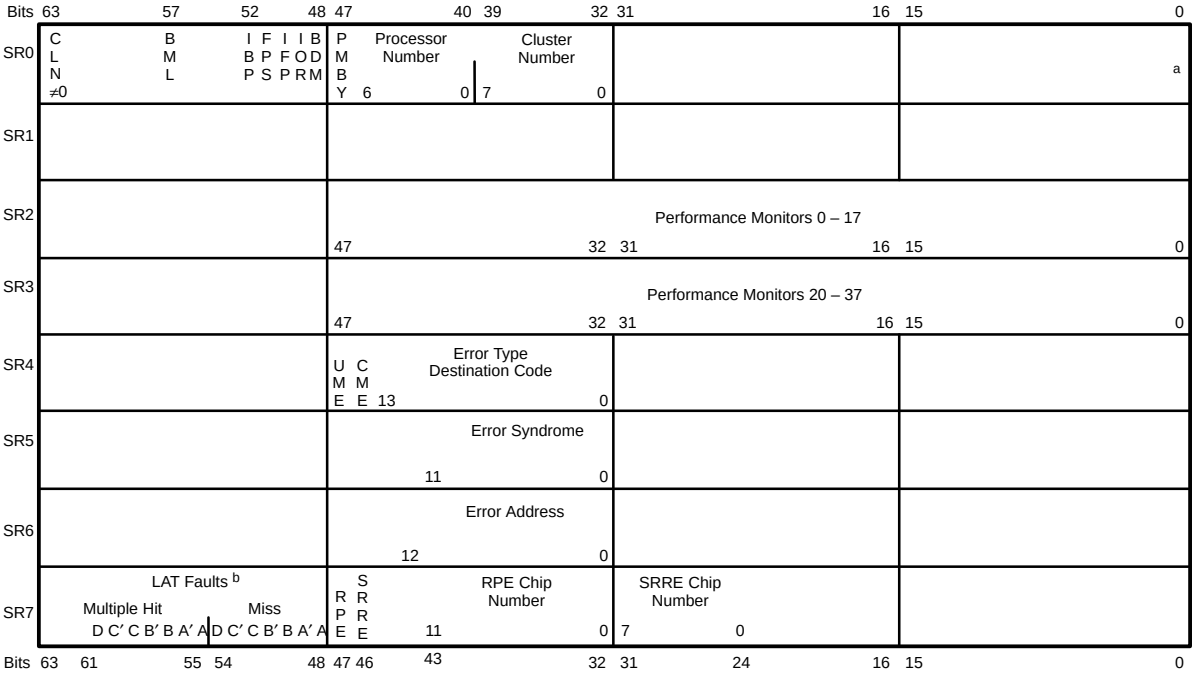
	Interrupt Modes
INV	FP invalid ‡
IDV	FP divide by zero ‡
IOV	FP overlflow ‡
IUN	FP underflow ‡
INX	FP not exact ‡
IXI	FP exceptional input ‡
IAM	Address multiply range error ‡
FNX	Enable flag on normal exit
IMI	001*ij*≠0 or 033 instruction
IDL	Deadlock
IPC	Programmable Clock
IIO	I/O
IIP	Interprocessor interrupt
IRT	Real-time clock
IMC	MCU interrupt
ICM	Correctable memory error
IBP	Breakpoint
FEX	Enable flag on error exit
IPR	Program range error
IOR	Operand range error
IFP	Floating point error †
IUM	Uncorretable memory error
IRP	Register parity error

† Not used in CPE1 Module
‡ Not used in CP02 Module

	Modes
MM	Monitor mode
BDM	Bi-directional memory
ESL	Enable 2nd vector logical
TRI	Triton mode †
SCE	Scalar cache enable
RM0	FP rounding mode Bit 0
RM1	FP rounding mode bit 1
BDD	Bi-directional disable

	Status
BML	Bit matrix multiply loaded
WS	Waiting on semaphore
FPS	FP error status †
VNU	Vectors not used
SBU	Status bit - monitor mode
SBM	Status bit - user mode
NVS	FP invalid ‡
DVS	FP divide by zero ‡
OVS	FP overflow ‡
UNS	FP underflow ‡
NXS	FP not exact ‡
XIS	FP exceptional input ‡

Status Registers for CP02 Module

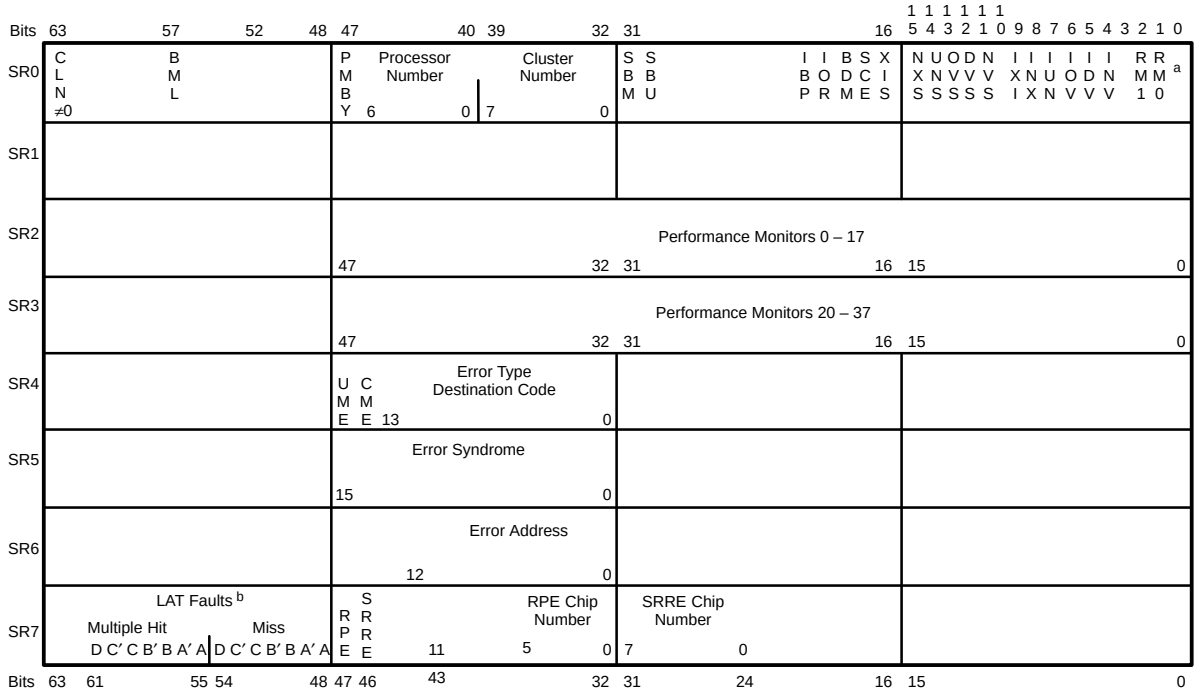


[a] SR0 bit 0 = monitor mode · maintenance mode · not (SR7 busy)

[b] SR7 bits 48 – 61 are set when a LAT fault occurs on the specified memory port

NOTES: Undefined areas can contain any value.
Status register read instruction 073*ij*1 S*i* SR*j* (Reading SR2 – SR7 is privileged to monitor mode.)

Status Registers for CPE1 Module



[a] SR0 bit 0 = monitor mode · maintenance mode · not (SR7 busy)

[b] SR7 bits 48 – 61 are set when a LAT fault occurs on the specified memory port

NOTES: Undefined areas can contain any value.
Status register read instruction 073*ij*1 S*i* SR*j* (Reading SR2 – SR7 is privileged to monitor mode.)
Status register write instruction 073*ij*5 SR*j* S*i* (*j* = 0 or 7 only)
Instruction 073*i*05 (SR0 S*i*) writes SR0 bits 1 through 31. The other bits of SR0 and all bits of SR1 through SR7 are read only.
Instruction 073*i*75 (SR7 S*i*) sends a command to the maintenance channel. This instruction is priviliged to monitor mode and maintenance mode.
SBU and SBM are status bits provided for software. SBM can be written only in monitor mode.

Destination Codes

Destination	Bit													
	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Cache read	1	1	1	–	Word									
V register read	1	1	0	Register			–	Element						
S register read	1	0	1	Register			0	–						
A register read	1	0	1	Register			1	–						
T register read	1	0	0	–			0	–	Register					
B register read	1	0	0	–			1	–	Register					
Fetch read	0	1	1	Group				Word						
I/O read	0	1	0	Type				Word						
Exchange read	0	0	1	–				Word						
I/O write	0	0	0	Type			1							
Processor write	0	0	0	–	0	1	0	A/S						
Reconfigure	0	0	0	–	1	1	0	–						
Memory error	0	0	0	–	0	0	0	–						

NOTE: These codes are on Status Register 4, bits 32 – 45. They show the destination for the data on a memory read.

Syndrome Chart for 1 Bit in Error

Syndrome	Bit	Syndrome	Bit	Syndrome	Bit	Syndrome	Bit	Syndrome	Bit
0001	64	0501	32	2021	43	3321	47	5170	57
0002	67	0504	33	2024	6	3612	20	5200	55
0004	65	0520	34	2120	11	3621	46	5212	19
0010	68	0525	35	2125	13	4000	75	5242	61
0020	66	0555	37	2133	15	4012	18	5250	56
0025	7	0571	36	2136	14	4042	59	5330	58
0040	69	1000	74	2401	44	4050	22	5505	5
0052	23	1012	17	2420	38	4240	27	5542	63
0100	70	1202	48	2425	8	4247	30	6426	10
0105	0	1210	49	2500	39	4252	29	6612	21
0124	12	1236	52	2505	3	4255	31	7051	25
0200	73	1240	50	2521	45	4427	9	7105	4
0212	16	1252	51	2524	40	4742	62	- -	- -
0250	28	1266	53	2664	42	5002	60	- -	- -
0400	71	2000	72	2744	41	5040	54	- -	- -
0405	1	2005	2	3053	26	5052	24	- -	- -

Syndrome Chart for 2 Bits (1 Byte) in Error

Syndrome	Bits	Syndrome	Bits	Syndrome	Bits	Syndrome	Bits	Syndrome	Bits
0003	64, 67	1417	1, 17	3476	9, 25	6366	15, 31	7634	41, 57
0014	65, 68	1703	32, 48	4717	4, 20	6371	14, 30	7700	39, 55
0060	66, 69	1714	33, 49	5475	10, 26	6663	47, 63	7717	3, 19
0077	7, 23	1733	37, 53	6000	72, 75	7163	46, 62	7763	45, 61
0300	70, 73	1747	36, 52	6017	2, 18	7403	44, 60	7774	40, 56
0317	0, 16	1760	34, 50	6063	43, 59	7460	38, 54	6377	13, 29
0374	12, 28	1777	35, 51	6074	6, 22	7477	8, 24	– –	– –
1400	71, 74	3317	5, 21	6360	11, 27	7554	42, 58	– –	– –

Syndrome Decoding Rules

Syndrome Rule	Example: Syndrome Bytes [a]						Error Description
	5	4	3	2	1	0	
Syndrome = 0	0	0	0	0	0	0	No error occurred.
Even number of bytes in error	00	00	01	00	01	00	Double- or multiple-byte error.
1 byte is in error	00	01	00	00	00	00	Checkbyte error. The byte indicates which check bits are in error.
3 or 5 bytes are in error	00	01	01	00	00	01	Single-byte error in data field.

[a] 00 = Good Byte
01, 10, 11 = Bad Byte

EZIF Error Messages

Error Message	Cause	Action
No Current Flow!! Reading Was: <voltage>mV Minimum Limit: 1mV.	Actuator cable open or disconnected. Heater loop open. Controller failure.	Check actuation cable connection and replace if necessary. Troubleshoot heater loop. Replace controller.
Excess Current Draw!! Reading Was: <voltage>mV. Maximum Limit: 220mV.	Heater loop shorted. Controller failure. Heater being cooled by some means.	Troubleshoot heater loop. Replace controller. Ensure that the system is completely pumped down so that the connectors are not in contact with the dielectric coolant.
Regulation Fault!! Reading Was: <voltage>mV. Maximum Limit: <200 or 170> mV	Heater loop shorted. Controller failure. Heater being cooled by some means.	Troubleshoot heater loop. Replace controller. Ensure that the system is completely pumped down so that the connectors are not in contact with the dielectric coolant.
Regulation Fault!! Reading Was: <voltage>mV. Maximum Limit: 130 mV	Heater loop shorted. Controller failure. Heater being cooled by some means	Troubleshoot heater loop. Replace controller. Ensure that the system is completely pumped down so that the connectors are not in contact with the dielectric coolant.
Regulation Fault!! Reading Was: <voltage>mV. Maximum Limit: <upper_limit>mV.	Heater loop shorted. Controller failure. Heater being cooled by some means.	Troubleshoot heater loop. Replace controller. Ensure that the system is completely pumped down so that the connectors are not in contact with the dielectric coolant.

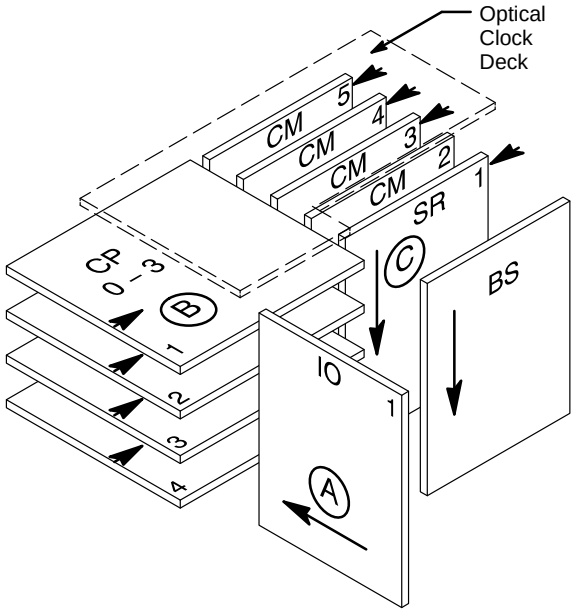
EZIF Error Messages

Error Message	Cause	Action
Regulation Time-out!! Reading Was: <voltage>mV. Maximum Limit: <160 or 170>mV.	Heater loop shorted. Controller failure. Heater being cooled by some means.	Troubleshoot heater loop. Replace controller. Ensure that the system is completely pumped down so that the connectors are not in contact with the dielectric coolant.
PRI=Bad SEC=Bad	Primary/Secondary heater matched the configuration for the selected module; resistance errors occurred.	Troubleshoot heater loop.
PRI=Open SEC=Open	Primary/Secondary heater did not match the configuration for the selected module; all pins measure open.	Troubleshoot heater loop.
PRI=CM/IO4/SR4/SIB4 SEC=CM/IO4/SR4/SIB4	Primary/Secondary heater did not match the configuration for the selected module; it matched the configuration for a CM, IO4, SR4, or SIB4 module.	Troubleshoot heater loop.
PRI=CP SEC=CP	Primary/Secondary heater did not match the configuration for the selected module; it matched the configuration for a CP module.	Troubleshoot heater loop.

EZIF Error Messages

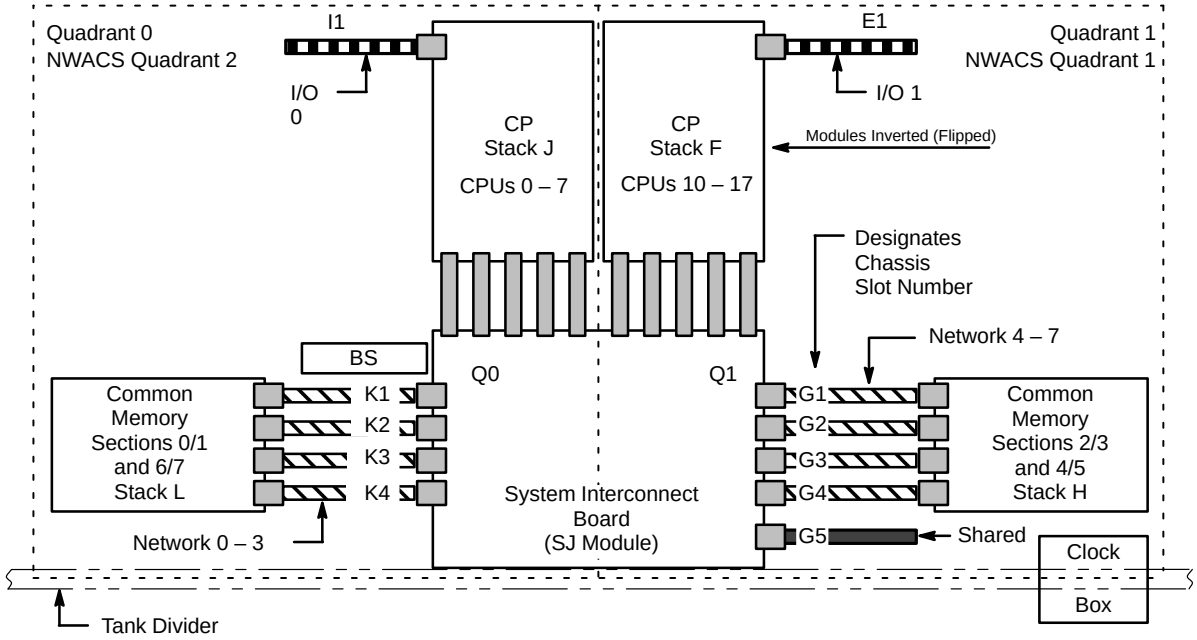
Error Message	Cause	Action
PRI=NW SEC=NW	Primary/Secondary heater did not match the configuration for the selected module; it matched the configuration for an NW module.	Troubleshoot heater loop.
PRI=SR8 SEC=SR8	Primary/Secondary heater did not match the configuration for the selected module; it matched the configuration for an SR8 module.	Troubleshoot heater loop.
PRI=SIB5 SEC=SIB5	Primary/Secondary heater did not match the configuration for the selected module; it matched the configuration for an SIB5 module.	Troubleshoot heater loop.
PRI=CPIO/Single SEC=CPIO/Single	Primary/Secondary heater did not match the configuration for the selected module; it matched the configuration for a CPIO/single module.	Troubleshoot heater loop.
PRI=Invalid SEC=Invalid	Primary/Secondary heater did not match the configuration for the selected module or any other module.	Troubleshoot heater loop.

Module Chassis Map for CRAY T94 System

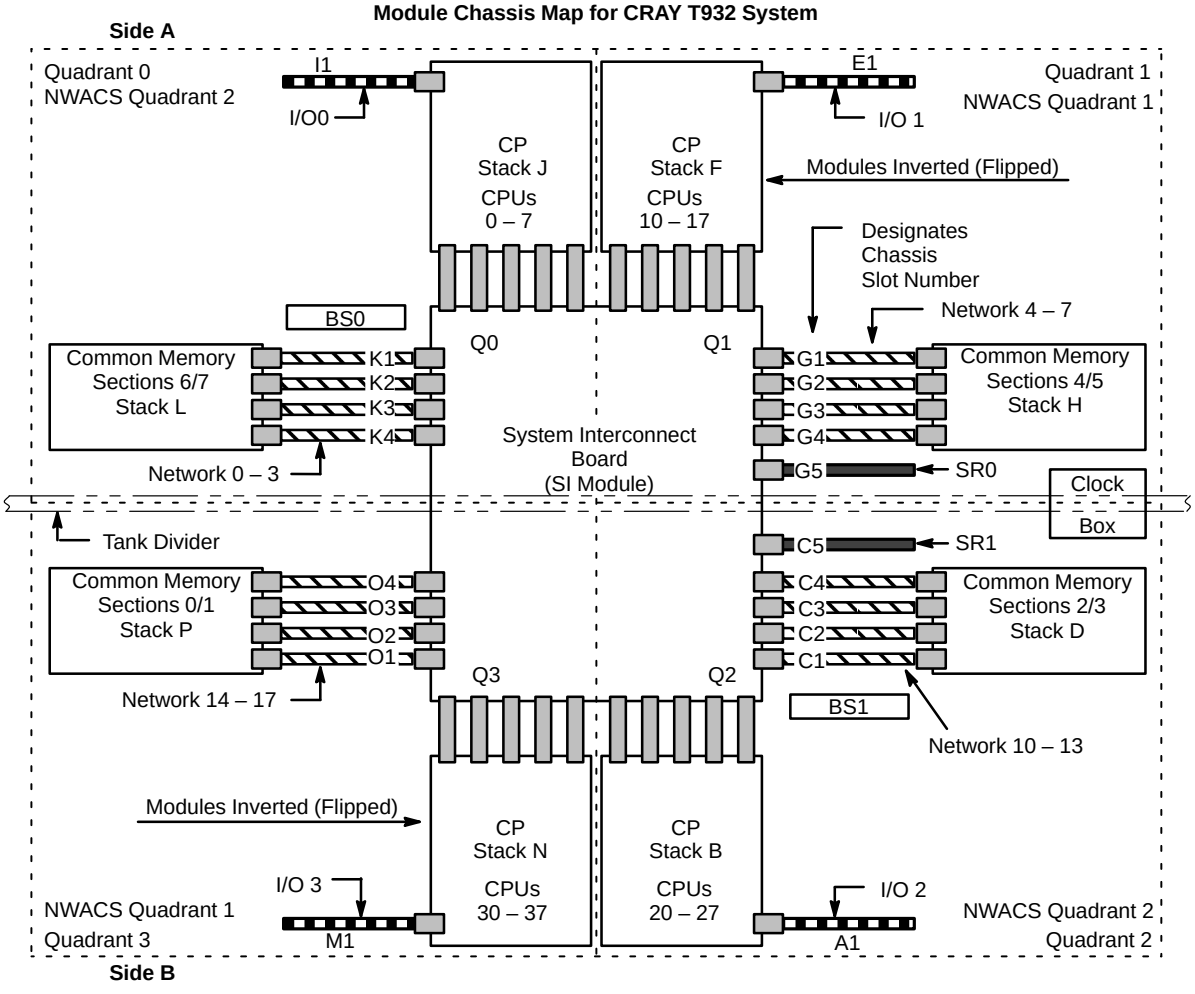


NOTE: Arrows indicate direction of module insertion into the chassis.

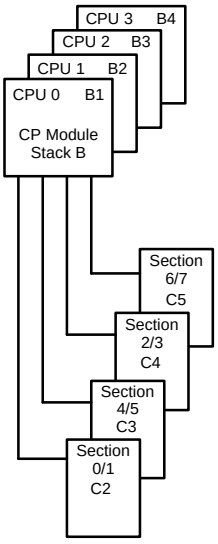
Module Chassis Map for CRAY T916 System



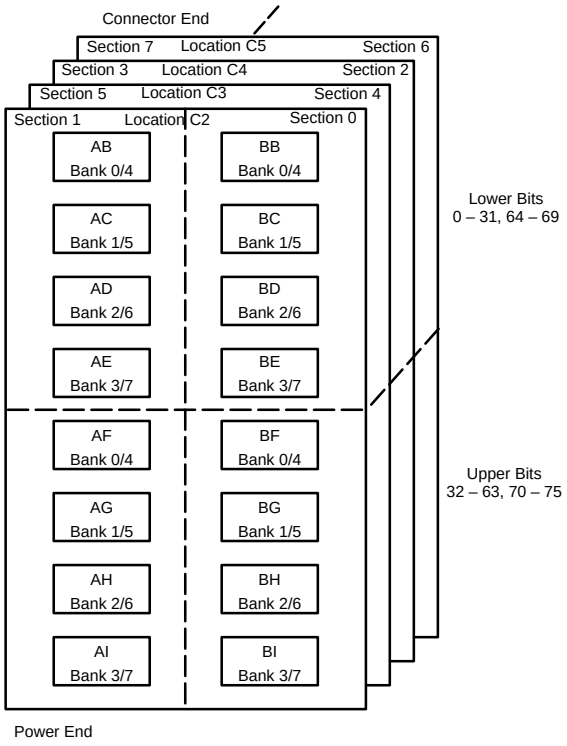
Module Chassis Map for CRAY T932 System



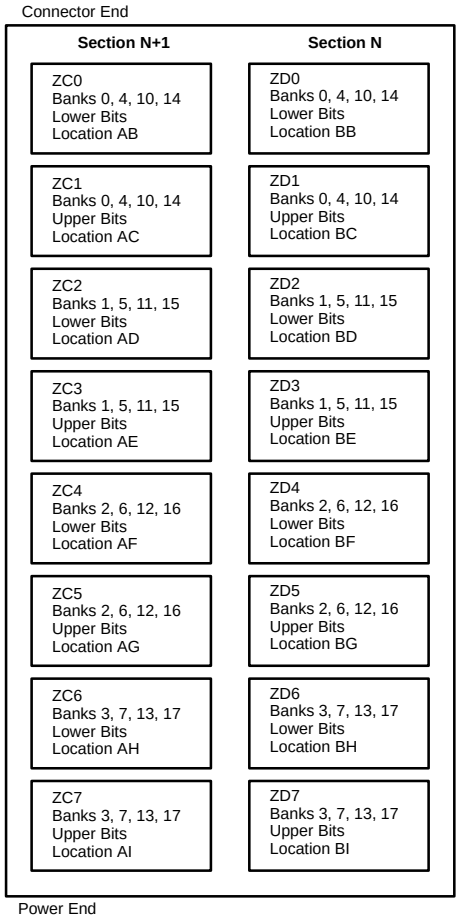
CRAY T94 Memory Chassis Map



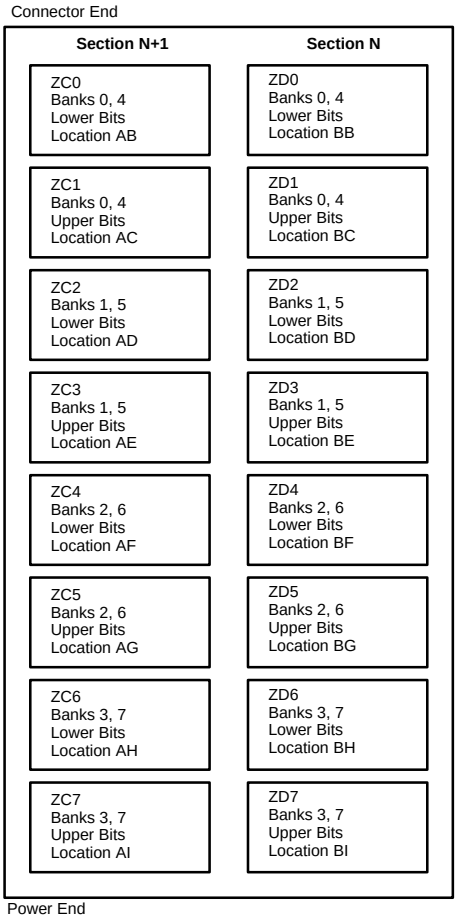
CRAY T94 Bank Layout
for CM02 Module



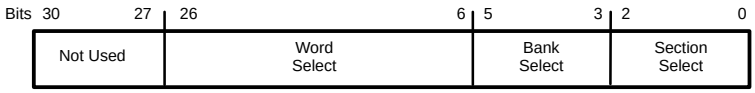
CRAY T94 Bank Layout for Synchronous CM03 Module



CRAY T94 Bank Layout for Asynchronous CM03 Module



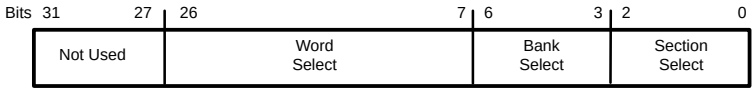
CRAY T94 Memory Address for CM02 Module



CRAY T94 System Configuration for CM02 Module

Module Counts			Configuration				Address Bits			
Processor	Network	Memory	Sections	Subsections	Banks	MWords	Section	Subsection	Bank	Word
1 to 4	0	4	8	1	64	128	00, 01, 02	–	03, 04, 05	06 – 30
1 to 4	0	4	8	1	32	64	00, 01, 02	–	03, 04	05 – 29
1 to 4	0	2	4	1	32	64	00, 01	–	02, 03, 04	05 – 29
1 to 4	0	2	4	1	16	32	00, 01	–	02, 03	04 – 28

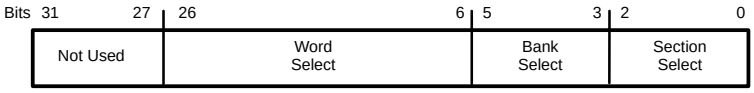
CRAY T94 Memory Address for Synchronous CM03 Module



CRAY T94 System Configuration for Synchronous CM03 Module

Module Counts			Configuration				Address Bits			
Processor	Network	Memory	Sections	Subsections	Banks	MWords	Section	Subsection	Bank	Word
1 to 4	0	4	8	1	128	128	00, 01, 02	–	03, 04, 05, 06	07 – 31
1 to 4	0	4	8	1	64	64	00, 01, 02	–	03, 04, 05	05 – 30
1 to 4	0	2	4	1	64	64	00, 01	–	02, 03, 04, 05	05 – 30
1 to 4	0	2	4	1	32	32	00, 01	–	02, 03, 04	04 – 29

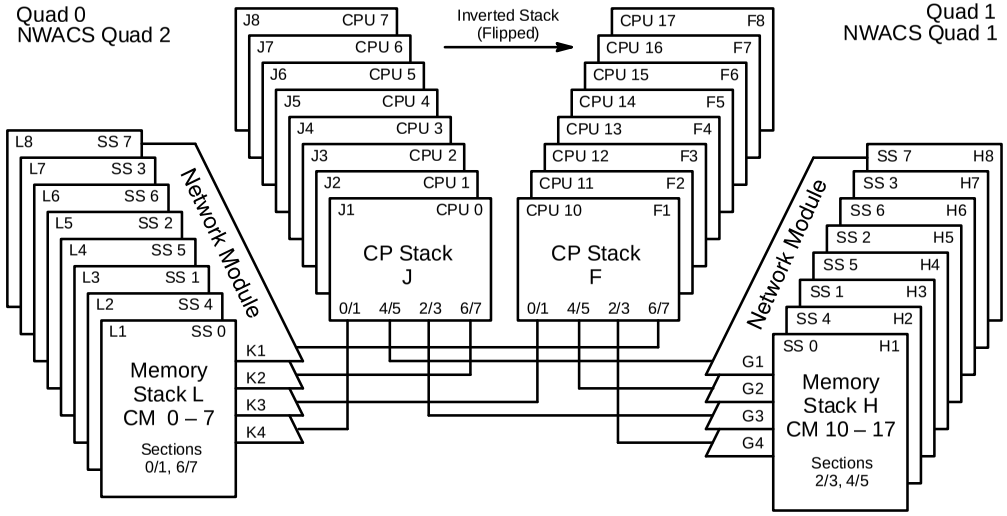
CRAY T94 Memory Address for Asynchronous CM03 Module



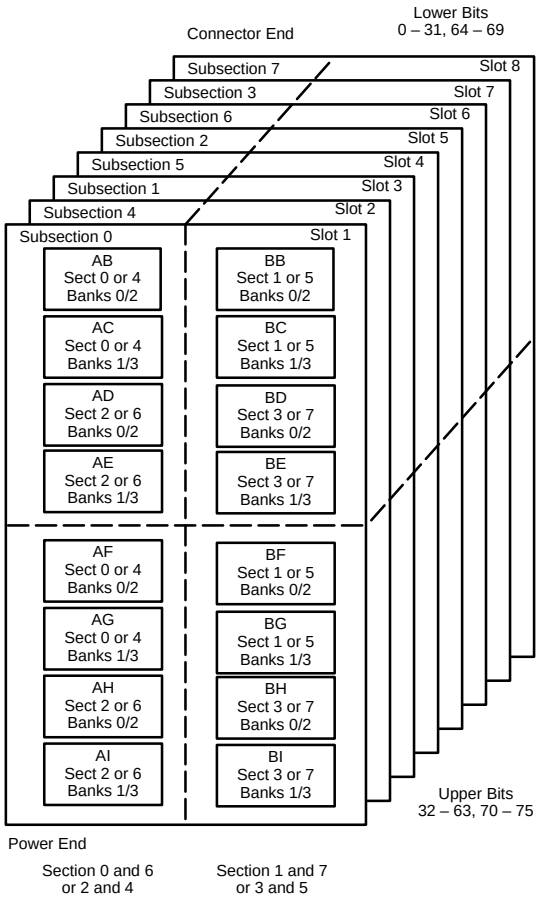
CRAY T94 System Configuration for Asynchronous CM03 Module

Module Counts			Configuration				Address Bits			
Processor	Network	Memory	Sections	Subsections	Banks	MWords	Section	Subsection	Bank	Word
1 to 4	0	4	8	1	64	128	00, 01, 02	–	03, 04, 05	06 – 31
1 to 4	0	4	8	1	32	64	00, 01, 02	–	03, 04	05 – 30
1 to 4	0	2	4	1	32	32	00, 01, 02	–	02, 03, 04	05 – 30
1 to 4	0	2	4	1	16	32	00, 01	–	02, 03	04 – 29

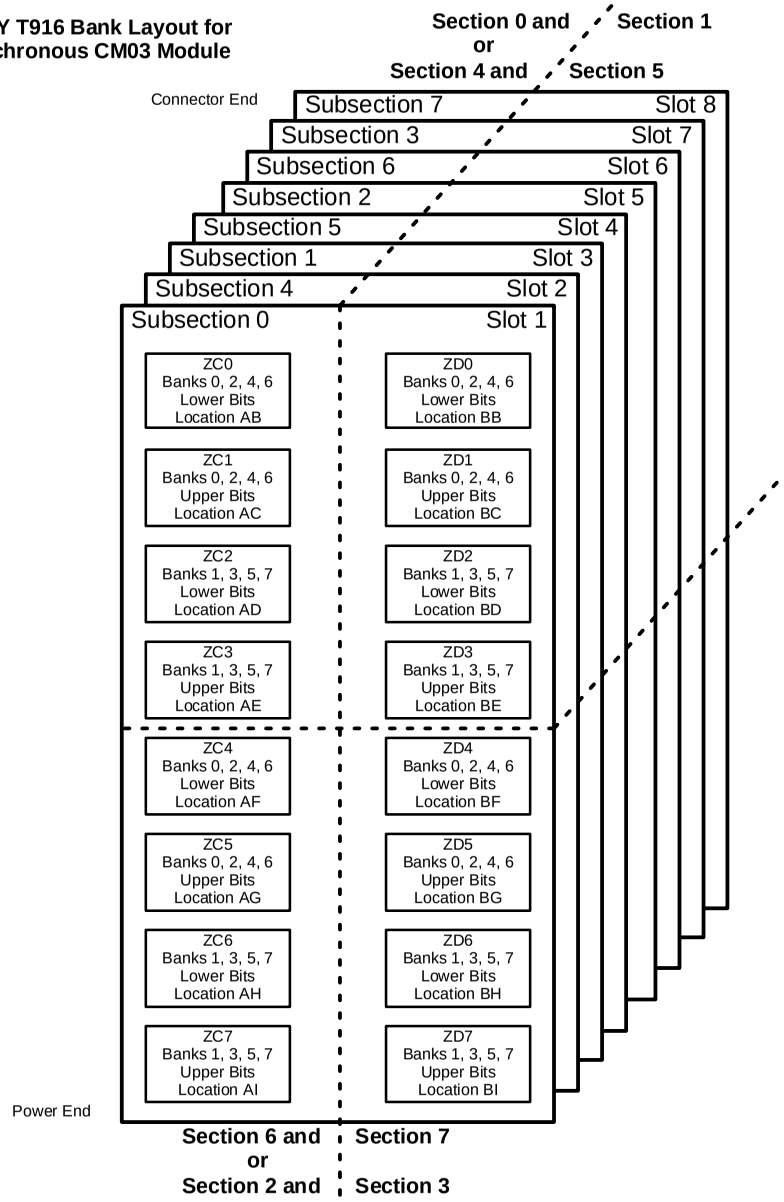
CRAY T916 Memory Chassis Map



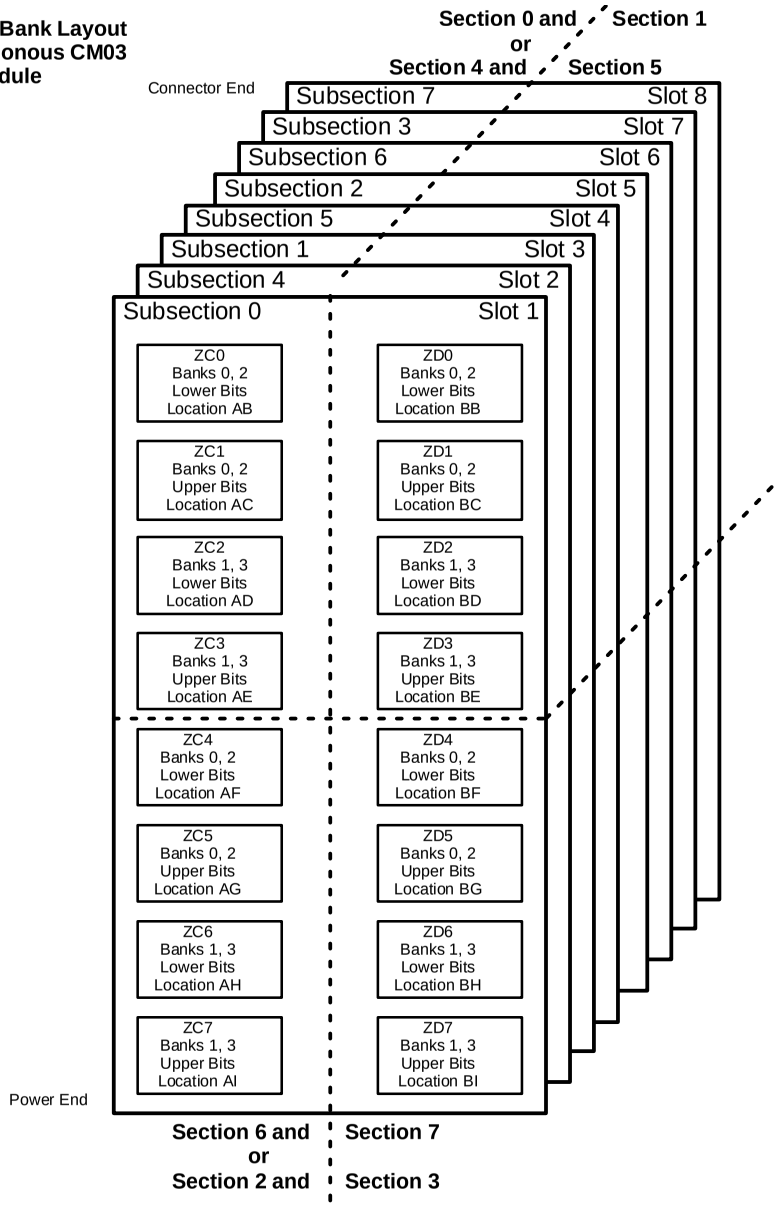
CRAY T916 Bank Layout for CM02 Module



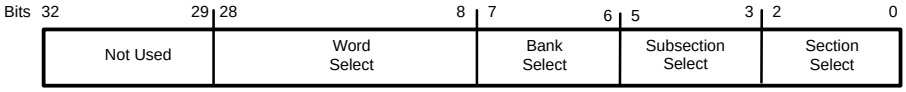
CRAY T916 Bank Layout for Synchronous CM03 Module



CRAY T916 Bank Layout for Asynchronous CM03 Module



CRAY T916 Memory Address for CM02 Module

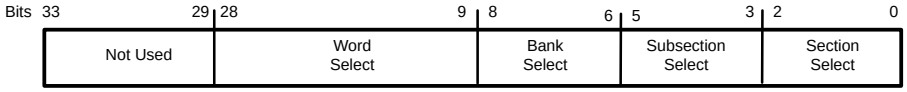


CRAY T916 System Configuration for CM02 Module

Module Counts			Configuration				Address Bits			
Processor	Network	Memory	Sections	Subsections	Banks	MWords	Section	Subsection	Bank	Word
4 to 8	4	8	8	4	128	256	00, 01, 02	03, 04	05, 06	07 – 31
4 to 8 [a]	4	8	8	2	64	128	00, 01, 02	03	04, 05	06 – 30
4 to 8 [a]	2	8	4	4	64	128	00, 01	02, 03	04, 05	06 – 30
4 to 8 [a]	2	4	4	2	32	64	00, 01	02	03, 04	05 – 29
4 to 8	4	16	8	8	256	512	00, 01, 02	03, 04, 05	06, 07	08 – 32
4 to 8 [a]	4	8	8	4	128	256	00, 01, 02	03, 04	05, 06	07 – 31
4 to 8 [a]	2	8	4	8	128	256	00, 01	02, 03, 04	05, 06	07 – 31
4 to 8 [a]	2	4	4	4	64	128	00, 01	02, 03	04, 05	06 – 30
8 to 16	8	16	8	8	256	512	00, 01, 02	03, 04, 05	06, 07	08 – 32
8 to 16 [a]	8	8	8	4	128	256	00, 01, 02	03, 04	05, 06	07 – 31
8 to 16 [a]	4	8	4	8	128	256	00, 01	02, 03, 04	05, 06	07 – 31

[a] This indicates a degraded or partitioned system; the system is not usually sold with this configuration.

CRAY T916 Memory Address for Synchronous CM03 Module

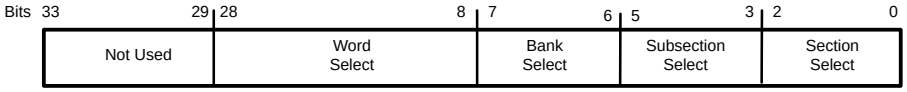


CRAY T916 System Configuration for Synchronous CM03 Module

Module Counts			Configuration				Address Bits			
Processor	Network	Memory	Sections	Subsections	Banks	MWords	Section	Subsection	Bank	Word
4 to 8	4	8	8	4	256	256	00, 01, 02	03, 04	05, 06, 07	08 – 32
4 to 8 [a]	4	8	8	2	128	128	00, 01, 02	03	04, 05, 06	07 – 31
4 to 8 [a]	2	8	4	4	128	128	00, 01	02, 03	04, 05, 06	07 – 31
4 to 8 [a]	2	4	4	2	64	64	00, 01	02	03, 04, 05	06 – 30
4 to 8	4	16	8	8	512	512	00, 01, 02	03, 04, 05	06, 07, 08	09 – 33
4 to 8 [a]	4	8	8	4	256	256	00, 01, 02	03, 04	05, 06, 07	08 – 32
4 to 8 [a]	2	8	4	8	256	256	00, 01	02, 03, 04	05, 06, 07	08 – 32
4 to 8 [a]	2	4	4	4	128	128	00, 01	02, 03	04, 05, 06	08 – 31
8 to 16	8	16	8	8	512	512	00, 01, 02	03, 04, 05	06, 07, 08	09 – 33
8 to 16 [a]	8	8	8	4	256	256	00, 01, 02	03, 04	05, 06, 07	08 – 32
8 to 16 [a]	4	8	4	8	256	256	00, 01	02, 03, 04	05, 06, 07	08 – 32
8 to 16 [a]	4	8	4	4	128	128	00, 01	02, 03	04, 05, 06	07 – 31

[a] This indicates a degraded or partitioned system; the system is not usually sold with this configuration.

CRAY T916 Memory Address for Asynchronous CM03 Module

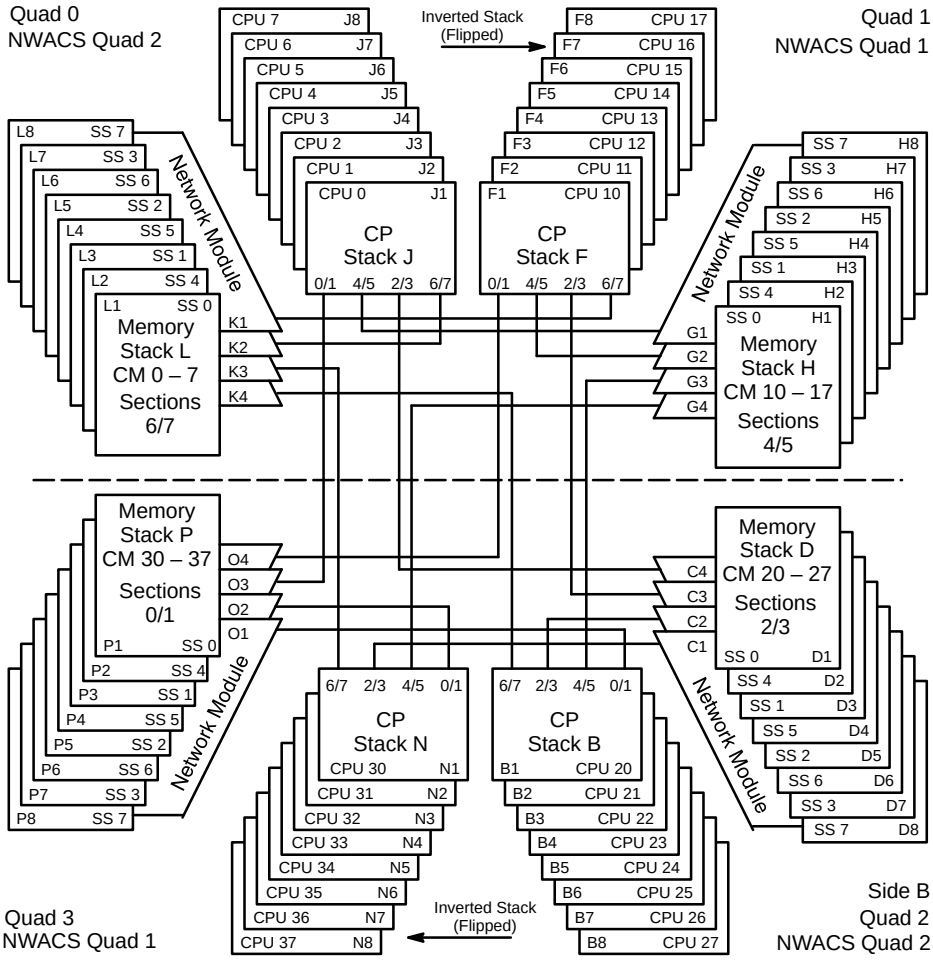


CRAY T916 System Configuration for Asynchronous CM03 Module

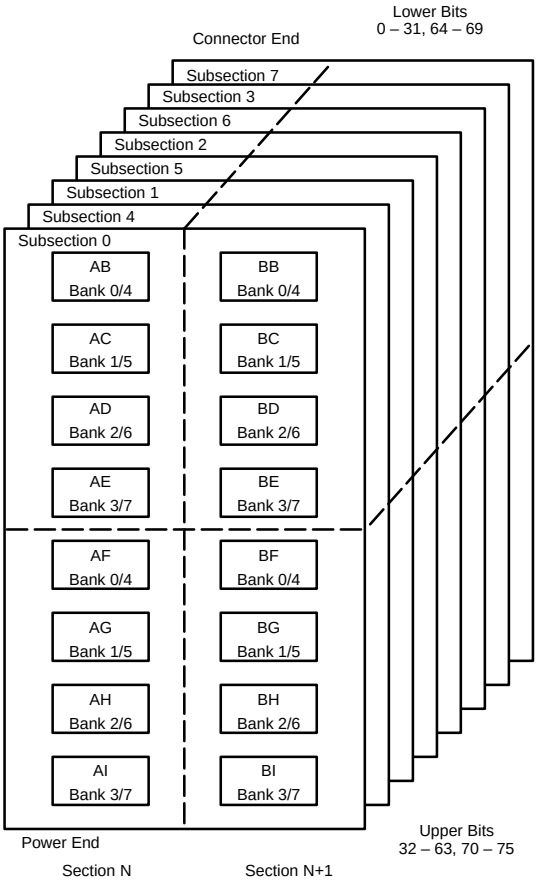
Module Counts			Configuration				Address Bits			
Processor	Network	Memory	Sections	Subsections	Banks	MWords	Section	Subsection	Bank	Word
4 to 8	4	8	8	4	128	256	00, 01, 02	03, 04	05, 06	07 – 32
4 to 8 [a]	4	8	8	2	64	128	00, 01, 02	03	04, 05	06 – 31
4 to 8 [a]	2	8	4	4	64	128	00, 01	02, 03	04, 05	06 – 31
4 to 8 [a]	2	4	4	2	32	64	00, 01	02	03, 04	05 – 30
4 to 8	4	16	8	8	256	512	00, 01, 02	03, 04, 05	06, 07	08 – 33
4 to 8 [a]	4	8	8	4	128	256	00, 01, 02	03, 04	05, 06	07 – 32
4 to 8 [a]	2	8	4	8	128	256	00, 01	02, 03, 04	05, 06	07 – 32
4 to 8 [a]	2	4	4	4	64	128	00, 01	02, 03	04, 05	06 – 31
8 to 16	8	16	8	8	256	512	00, 01, 02	03, 04, 05	06, 07	08 – 33
8 to 16 [a]	8	8	8	4	128	256	00, 01, 02	03, 04	05, 06	07 – 32
8 to 16 [a]	4	8	4	8	128	256	00, 01	02, 03, 04	05, 06	07 – 32
8 to 16 [a]	4	8	4	4	64	128	00, 01	02, 03	04, 05	06 – 31

[a] This indicates a degraded or partitioned system; the system is not usually sold with this configuration.

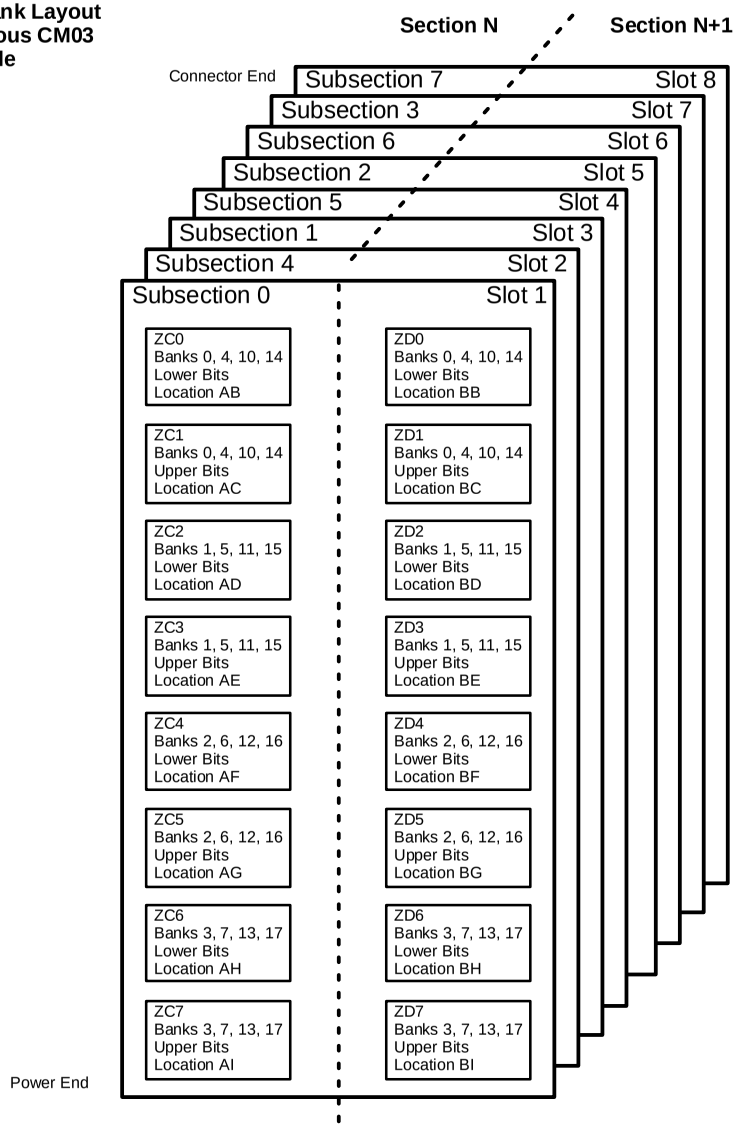
CRAY T932 Memory Chassis Map



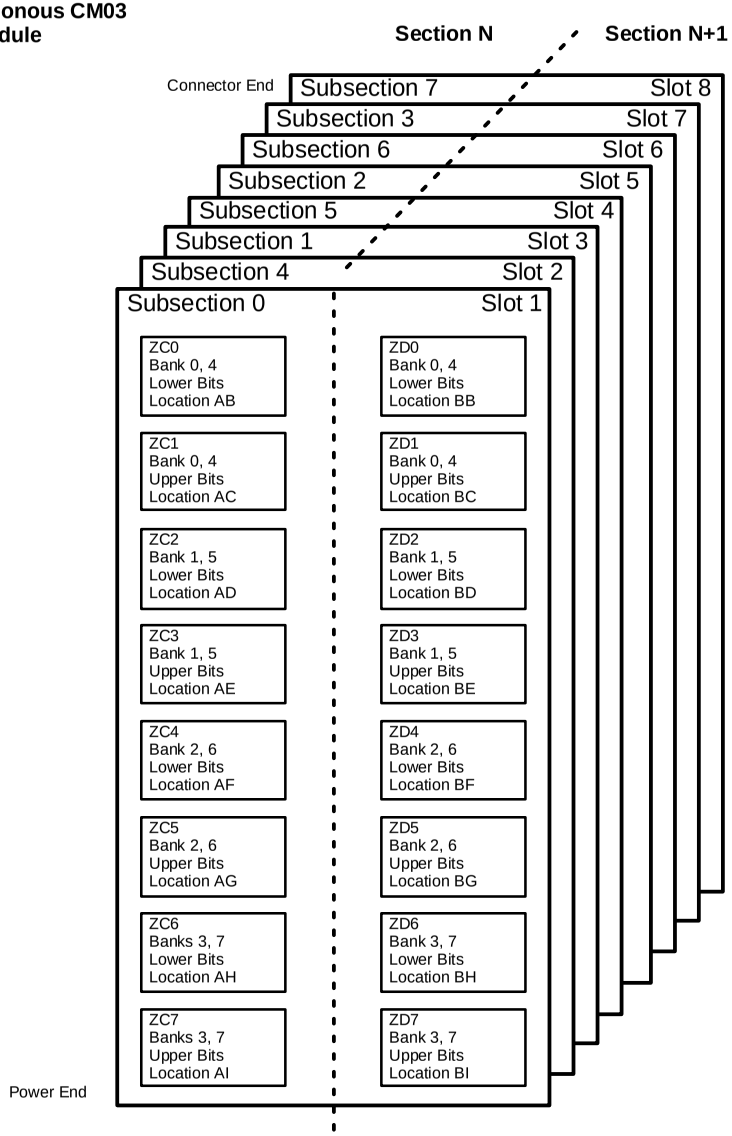
CRAY T932 Bank Layout for CM02 Module



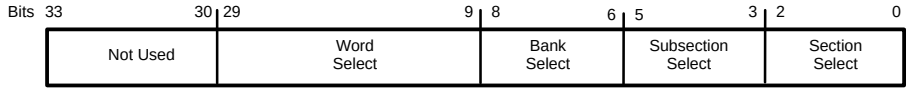
CRAY T932 Bank Layout for Synchronous CM03 Module



CRAY T932 Bank Layout for Asynchronous CM03 Module



CRAY T932 Memory Address for CM02 Module

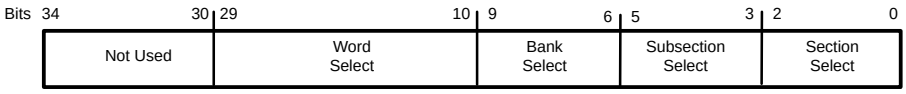


CRAY T932 System Configuration for CM02 Module

Module Counts			Configuration				Address Bits			
Processor	Network	Memory	Sections	Subsections	Banks	MWords	Section	Subsection	Bank	Word
8	4	32	8	8	512	1,024	00, 01, 02	03, 04, 05	06, 07, 08	09– 33
8	4	16	8	4	256	512	00, 01, 02	03, 04	05, 06, 07	08 – 32
8 [a]	4	8	8	2	128	256	00, 01, 02	03	04, 05, 06	07 – 31
8	8	8	8	2	128	256	00, 01, 02	03	04, 05, 06	07 – 31
8 [a]	8	8	8	2	64	128	00, 01, 02	03	04, 05	06 – 30
8 [a]	4	4	4	2	64	128	00, 01	02	03, 04, 05	06 – 30
8 [a]	4	4	4	2	32	64	00, 01	02	03, 04	05 – 29
8 to 16	8	16	8	4	256	512	00, 01, 02	03, 04	05, 06, 07	08 – 32
8 to 16 [a]	8	16	8	4	128	256	00, 01, 02	03, 04	05, 06	07 – 31
8 to 16 [a]	8	8	8	2	128	256	00, 01, 02	03	04, 05, 06	07 – 31
8 to 16 [a]	4	8	4	4	128	256	00, 01	02, 03	04, 05, 06	07 – 31
16	16	16	8	4	256	512	00, 01, 02	03, 04	05, 06, 07	08 – 32
16 [a]	16	16	8	4	128	256	00, 01, 02	03, 04	05, 06	07 – 31
16 [a]	16	8	8	2	128	256	00, 01, 02	03	04, 05, 06	07 – 31
16 [a]	8	8	4	4	128	256	00, 01	02, 03	04, 05, 06	07 – 31
16 to 32	16	32	8	8	512	1,024	00, 01, 02	03, 04, 05	06, 07, 08	09 – 33
16 to 32 [a]	16	32	8	8	256	512	00, 01, 02	03, 04, 05	06. 07	08 – 32
16 to 32 [a]	16	16	8	4	256	512	00, 01, 02	03, 04	05, 06, 07	08 – 32
16 to 32 [a]	8	16	4	8	256	512	00, 01	02, 03, 04	05, 06, 07	08– 32

[a] This indicates a degraded or partitioned system; the system is not usually sold with this configuration.

CRAY T932 Memory Address for Synchronous CM03 Module

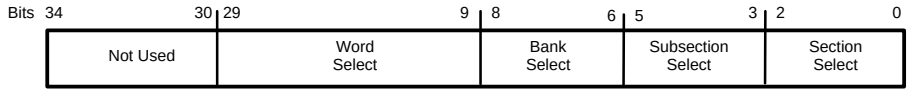


CRAY T932 System Configuration for Synchronous CM03 Module

Module Counts			Configuration				Address Bits			
Processor	Network	Memory	Sections	Subsections	Banks	MWords	Section	Subsection	Bank	Word
8	4	32	8	8	1,024	1024	00, 01, 02	03, 04, 05	06, 07, 08, 09	10 – 34
8	4	16	8	4	512	512	00, 01, 02	03, 04	05, 06, 07, 08	09 – 33
8 [a]	4	8	8	2	256	256	00, 01, 02	03	04, 05, 06. 07	08 – 32
8	8	8	8	2	256	256	00, 01, 02	03	04, 05, 06. 07	08 – 32
8 [a]	8	8	8	2	128	128	00, 01, 02	03	04, 05, 06	07 – 31
8 [a]	4	4	4	2	128	128	00, 01	02	03, 04, 05. 06	07 – 31
8 [a]	4	4	4	2	64	64	00, 01	02	03, 04. 05	06 – 30
8 to 16	8	16	8	4	512	512	00, 01, 02	03, 04	05, 06, 07, 08	09 – 33
8 to 16 [a]	8	16	8	4	256	256	00, 01, 02	03, 04	05, 06, 07	08 – 32
8 to 16 [a]	8	8	8	2	256	256	00, 01, 02	03	04, 05, 06. 07	08 – 32
8 to 16 [a]	4	8	4	4	256	256	00, 01	02, 03	04, 05, 06, 07	08 – 32
16	16	16	8	4	512	512	00, 01, 02	03, 04	05, 06, 07. 08	09 – 33
16 [a]	16	16	8	4	256	256	00, 01, 02	03, 04	05, 06, 07	08 – 32
16 [a]	16	8	8	2	256	256	00, 01, 02	03	04, 05, 06, 07	08 – 32
16 [a]	8	8	4	4	256	256	00, 01	02, 03	04, 05, 06. 07	08 – 32
16 to 32	16	32	8	8	1,024	1024	00, 01, 02	03, 04, 05	06, 07, 08. 09	10 – 34
16 to 32 [a]	16	32	8	8	512	512	00, 01, 02	03, 04, 05	06. 07, 08	09 – 33
16 to 32 [a]	16	16	8	4	512	512	00, 01, 02	03, 04	05, 06, 07. 08	09 – 33
16 to 32 [a]	8	16	4	8	512	512	00, 01	02, 03, 04	05, 06, 07, 08	09 – 33

[a] This indicates a degraded or partitioned system; the system is not usually sold with this configuration.

CRAY T932 Memory Address for Asynchronous CM03 Module



CRAY T932 System Configuration for Asynchronous CM03 Module

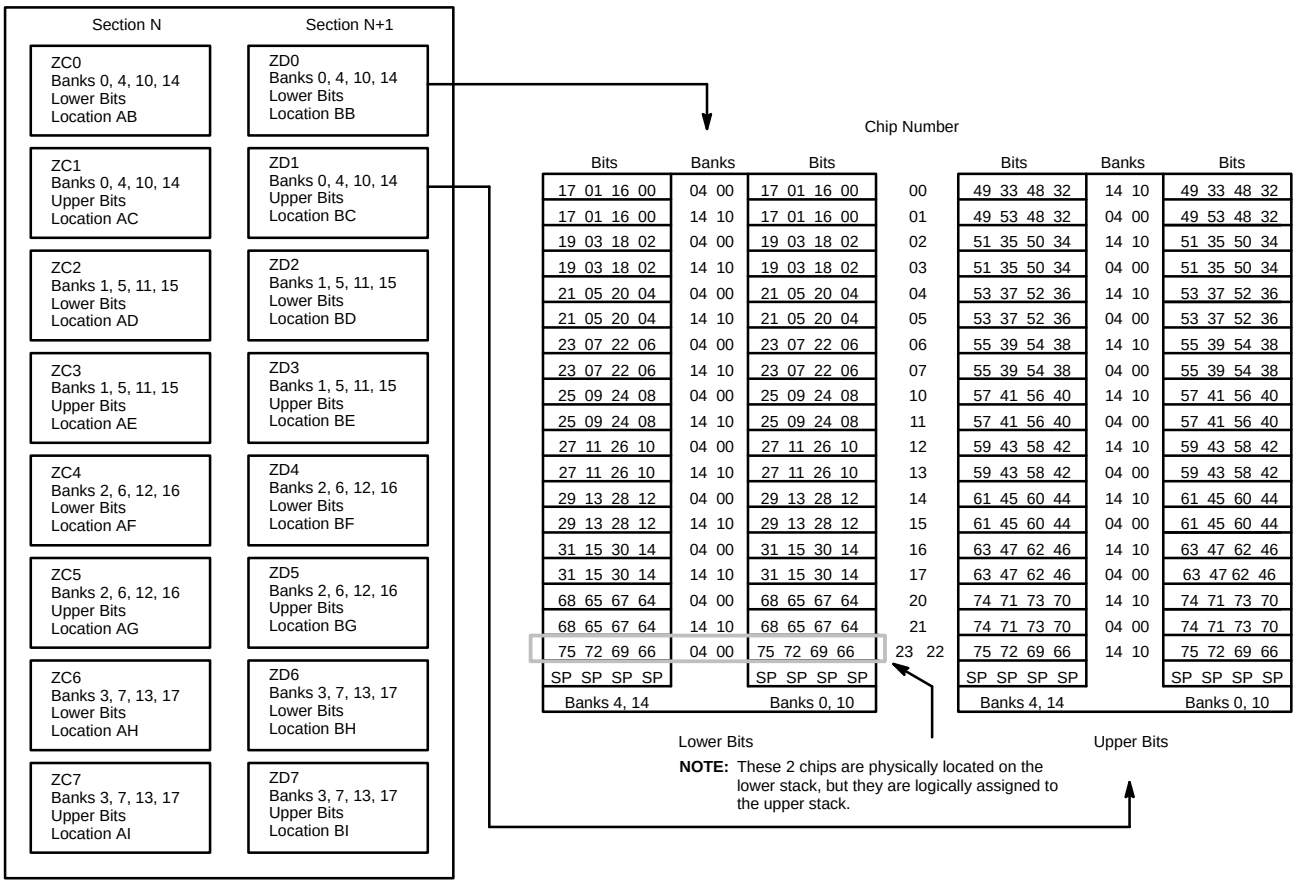
Module Counts			Configuration				Address Bits			
Processor	Network	Memory	Sections	Subsections	Banks	MWords	Section	Subsection	Bank	Word
8	4	32	8	8	512	1,024	00, 01, 02	03, 04, 05	06, 07, 08	09– 34
8	4	16	8	4	256	512	00, 01, 02	03, 04	05, 06, 07	08 – 33
8 [a]	4	8	8	2	128	256	00, 01, 02	03	04, 05, 06	07 – 32
8	8	8	8	2	128	256	00, 01, 02	03	04, 05, 06	07 – 32
8 [a]	8	8	8	2	64	128	00, 01, 02	03	04, 05	06 – 31
8 [a]	4	4	4	2	64	128	00, 01	02	03, 04, 05	06 – 31
8 [a]	4	4	4	2	32	64	00, 01	02	03, 04	05 – 30
8 to 16	8	16	8	4	256	512	00, 01, 02	03, 04	05, 06, 07	08 – 33
8 to 16 [a]	8	16	8	4	128	256	00, 01, 02	03, 04	05, 06	07 – 32
8 to 16 [a]	8	8	8	2	128	256	00, 01, 02	03	04, 05, 06	07 – 32
8 to 16 [a]	4	8	4	4	128	256	00, 01	02, 03	04, 05, 06	07 – 32
16	16	16	8	4	256	512	00, 01, 02	03, 04	05, 06, 07	08 – 33
16 [a]	16	16	8	4	128	256	00, 01, 02	03, 04	05, 06	07 – 32
16 [a]	16	8	8	2	128	256	00, 01, 02	03	04, 05, 06	07 – 32
16 [a]	8	8	4	4	128	256	00, 01	02, 03	04, 05, 06	07 – 32
16 to 32	16	32	8	8	512	1,024	00, 01, 02	03, 04, 05	06, 07, 08	09 – 34
16 to 32 [a]	16	32	8	8	256	512	00, 01, 02	03, 04, 05	06. 07	08 – 33
16 to 32 [a]	16	16	8	4	256	512	00, 01, 02	03, 04	05, 06, 07	08 – 33
16 to 32 [a]	8	16	4	8	256	512	00, 01	02, 03, 04	05, 06, 07	08 – 33

[a] This indicates a degraded or partitioned system; the system is not usually sold with this configuration.

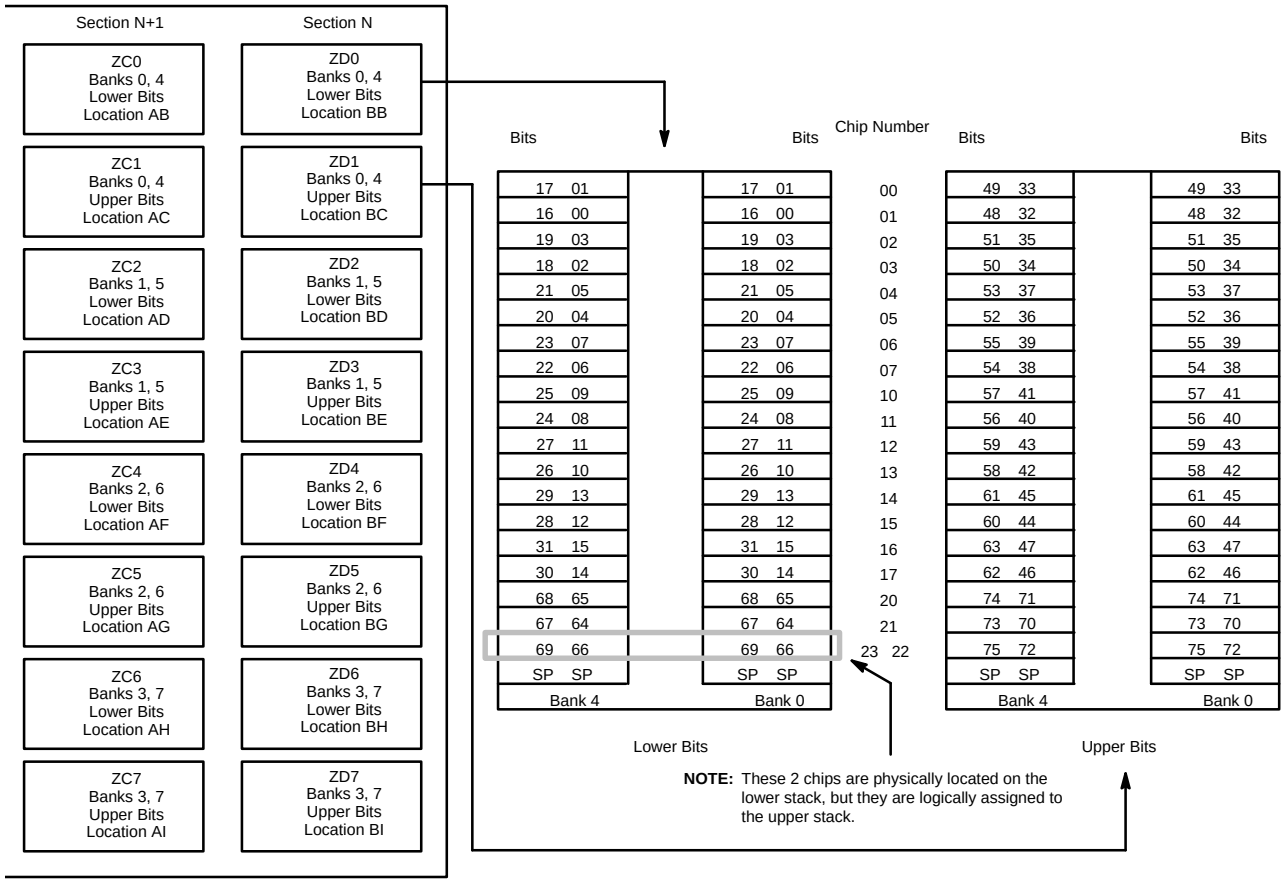
Bit Layout for CM02 Module

	Bank 4, 5, 6, or 7		Bank 0, 1, 2, or 3		
Chip	D0/Q0	D1/Q1	D0/Q0	D1/Q1	Chip
BA	0 (32)	16 (48)	0 (32)	16 (48)	AA
BB	1 (33)	17 (49)	1 (33)	17 (49)	AB
BC	2 (34)	18 (50)	2 (34)	18 (50)	AC
BD	3 (35)	19 (51)	3 (35)	19 (51)	AD
BE	4 (36)	20 (52)	4 (36)	20 (52)	AE
BF	5 (37)	21 (53)	5 (37)	21 (53)	AF
BG	6 (38)	22 (54)	6 (38)	22 (54)	AG
BH	7 (39)	23 (55)	7 (39)	23 (55)	AH
BI	8 (40)	24 (56)	8 (40)	24 (56)	AI
BJ	9 (41)	25 (57)	9 (41)	25 (57	AJ
BK	10 (42)	26 (58)	10 (42)	26 (58)	AK
BL	11 (43)	27 (59)	11 (43)	27 (59	AL
BM	12 (44)	28 (60)	12 (44)	28 (60)	AM
BN	13 (45)	29 (61)	13 (45)	29 (61)	AN
BO	14 (46)	30 (62)	14 (46)	30 (62)	AO
BP	15 (47)	31 (63)	15 (47)	31 (63)	AP
BQ	64 (70)	67 (73)	64 (70)	67 (73)	AQ
BR	65 (71)	68 (74)	65 (71)	68 (74)	AR
BS	66 (72)	69 (75)	66 (72)	69 (75)	AS

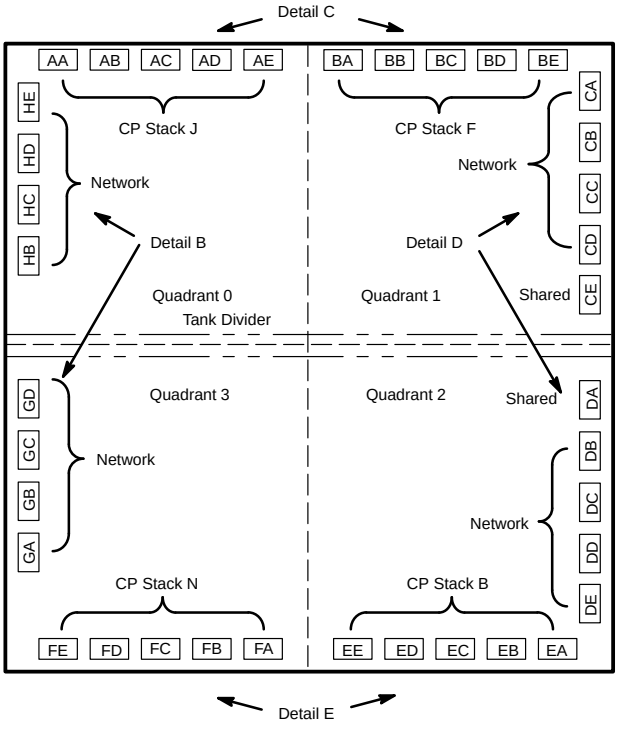
Bit Layout for Synchronous CM03 Memory Module



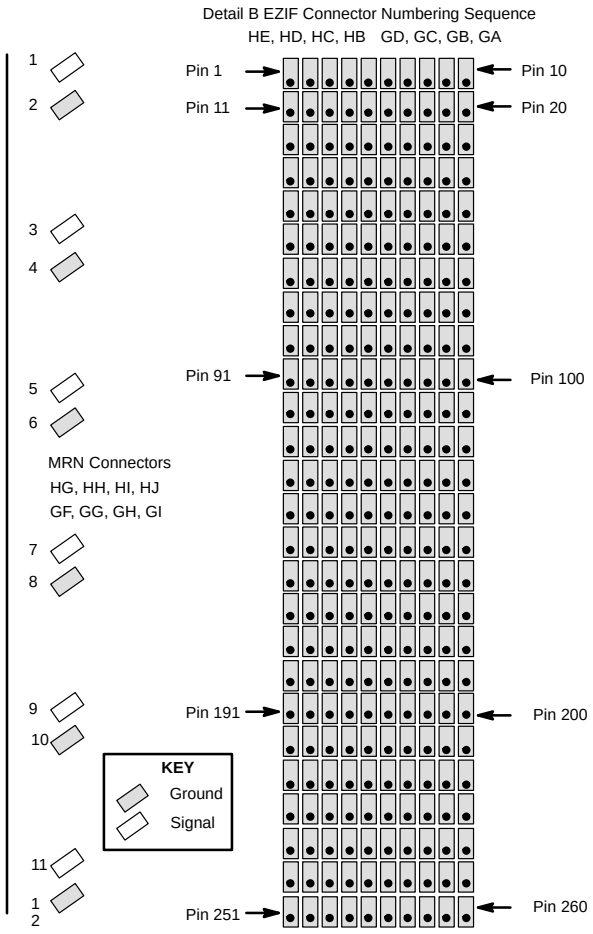
Bit Layout for Asynchronous CM03 Memory Module



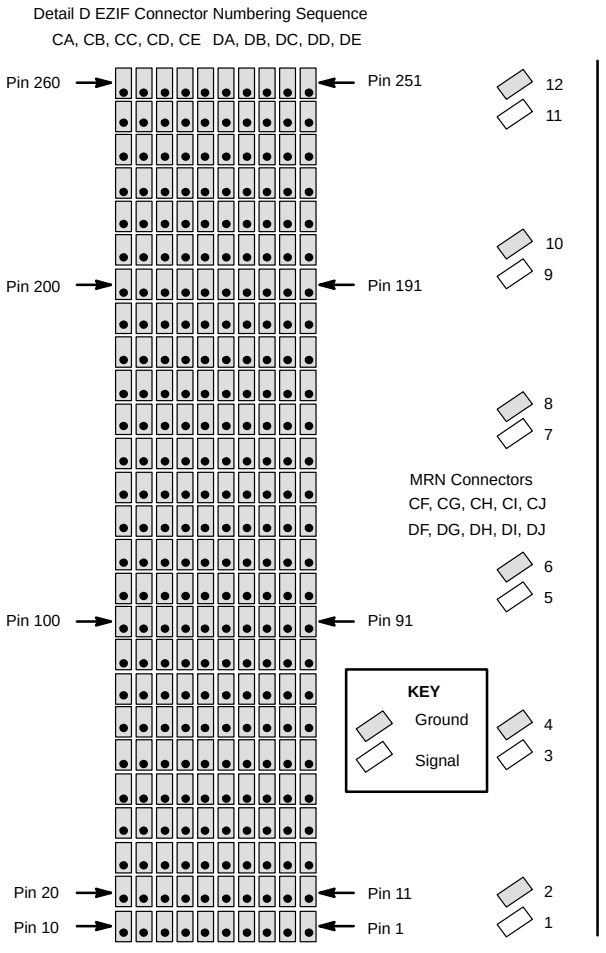
SIB Connector Layout

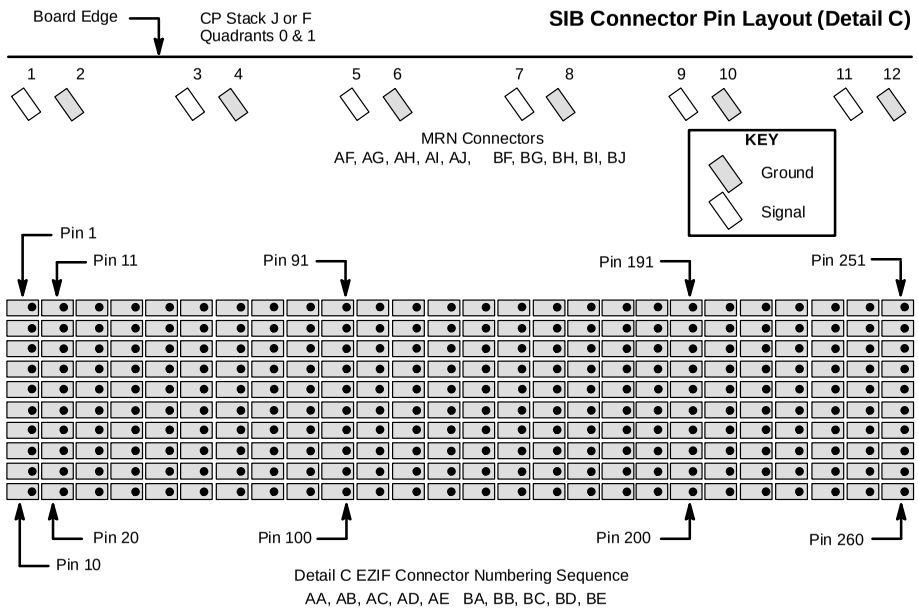


SIB Connector Pin Layout (Detail B)

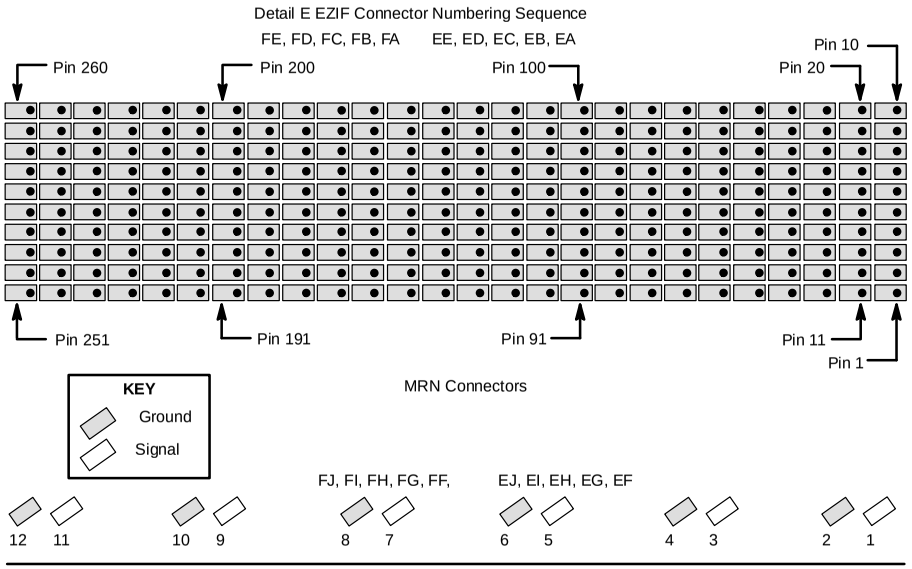


SIB Connector Pin Layout (Detail D)

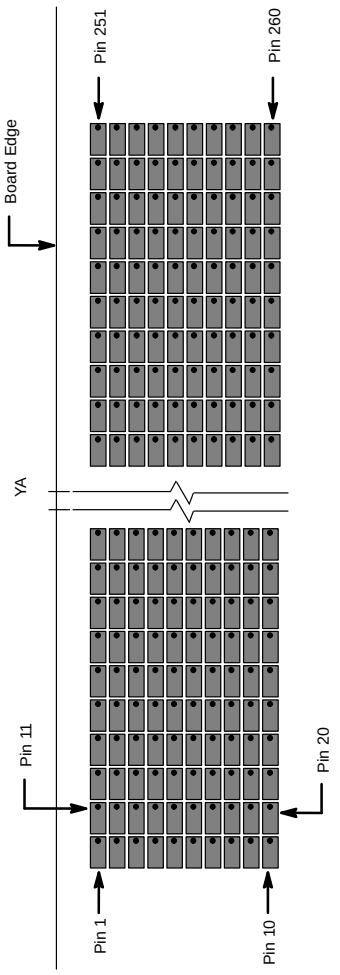



SIB Connector Pin Layout (Detail C)
Board Edge
CP Stack J or F
Quadrants 0 & 1
1 2 3 4 5 6 7 8 9 10 11 12
MRN Connectors
AF, AG, AH, AI, AJ, BF, BG, BH, BI, BJ
KEY
Ground
Signal
Pin 1
Pin 11
Pin 91
Pin 191
Pin 251
Pin 20
Pin 100
Pin 200
Pin 260
Pin 10
Detail C EZIF Connector Numbering Sequence
AA, AB, AC, AD, AE BA, BB, BC, BD, BE

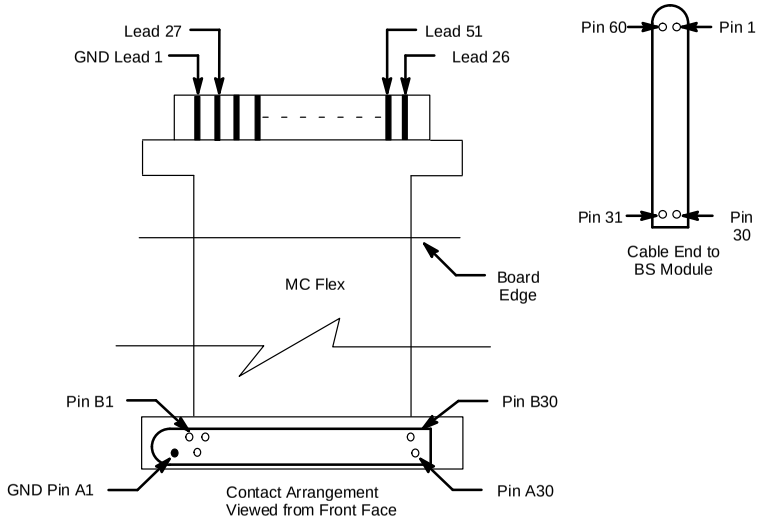
SIB Connector Pin Layout (Detail E)



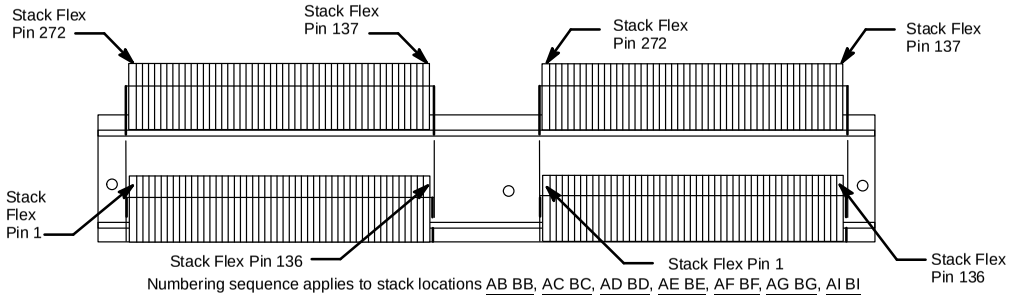
Edge Connector for CM02/03
Viewed from Layer 1



Maintenance Connector for CM02/03

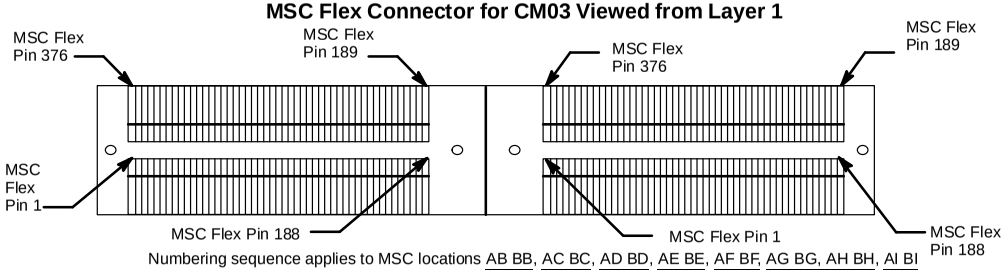


MSC Flex Connector for CM02 Viewed from Layer 1



Numbering sequence applies to stack locations AB BB, AC BC, AD BD, AE BE, AF BF, AG BG, AI BI

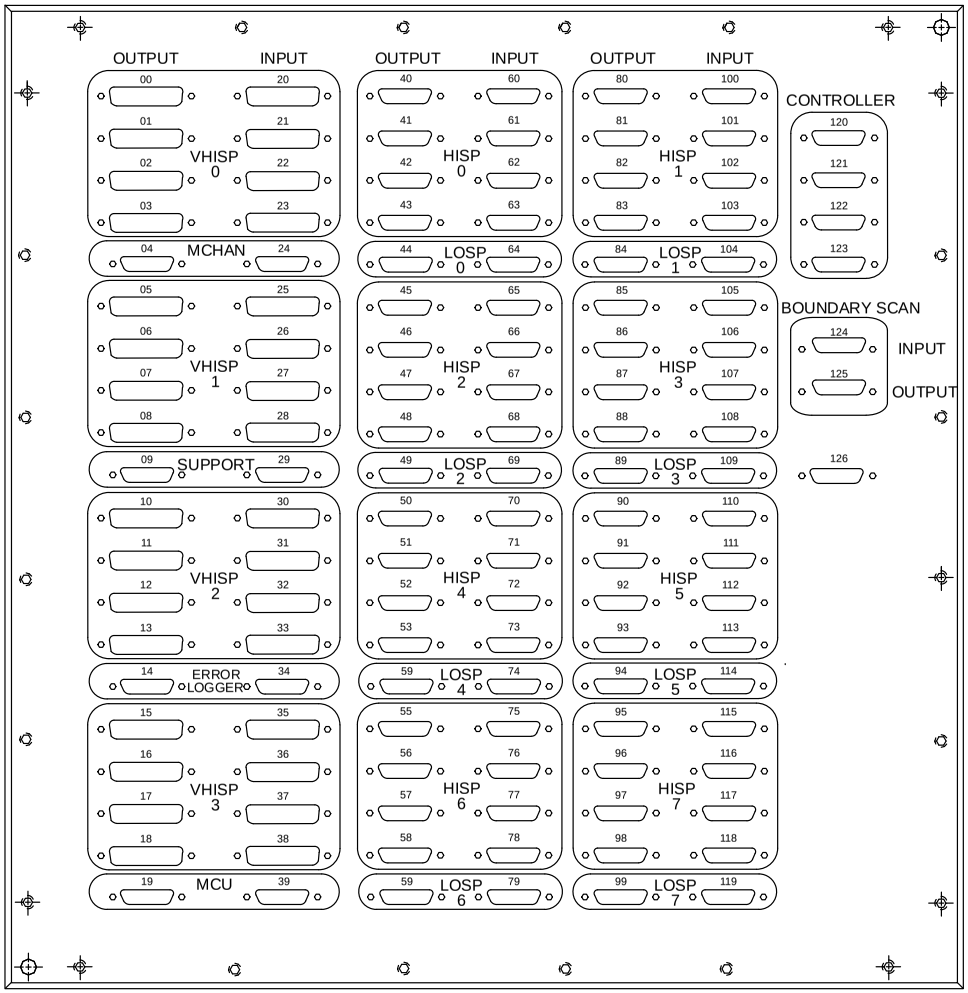
MSC Flex Connector for CM03 Viewed from Layer 1



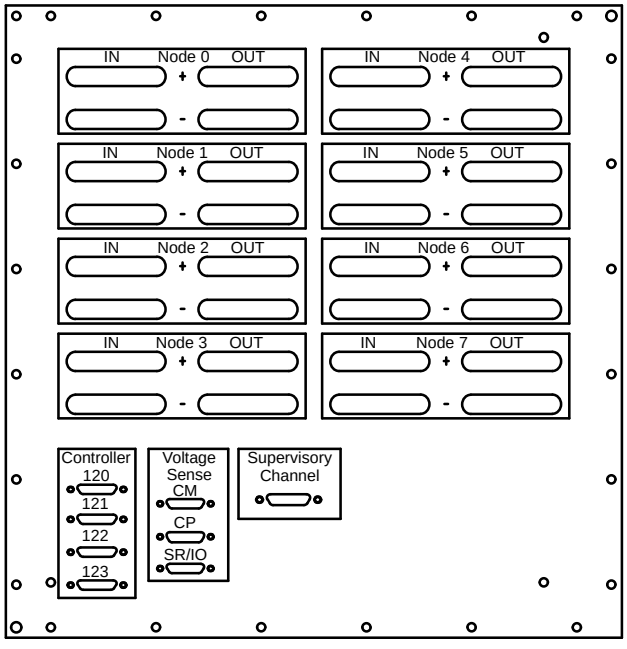
Numbering sequence applies to MSC locations AB BB, AC BC, AD BD, AE BE, AF BF, AG BG, AH BH, AI BI

Chip Pinouts

Cable Bulkhead for CRAY T94 System (IO01 Module)



Cable Bulkhead for CRAY T94 System
(IO02 Module)



See next page for node assignments.

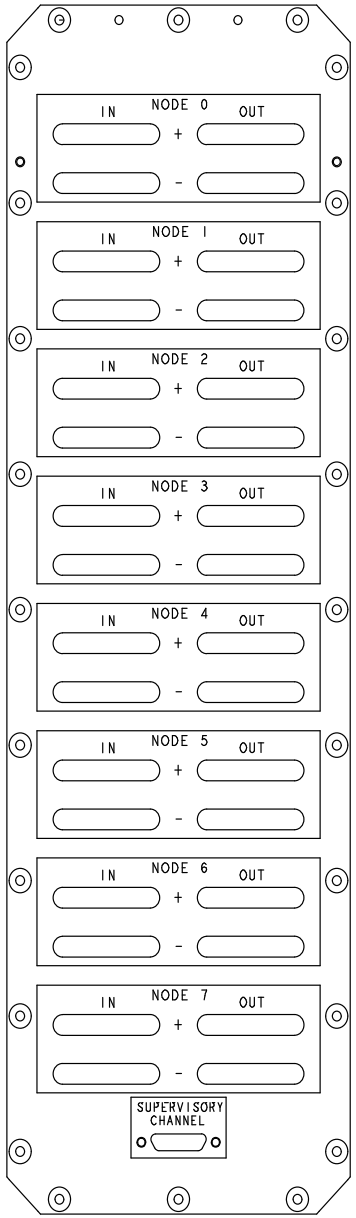
Node/Quad Assignments for IO02 Module (Upright)

Bulkhead Channel Designator	IO Module Quad Designator
Node 0	Quad 0 Node A
Node 1	Quad 0 Node B
Node 2	Quad 1 Node A
Node 3	Quad 1 Node B
Node 4	Quad 2 Node A
Node 5	Quad 2 Node B
Node 6	Quad 3 Node A
Node 7	Quad 3 Node B

Node/Quad Assignments for IO02 Module (Inverted) at Chassis Locations E1, M1

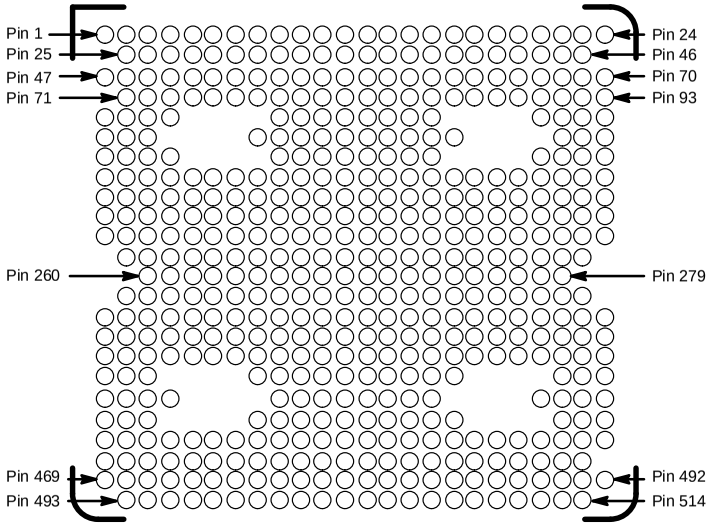
Bulkhead Channel Designator	IO Module Quad Designator
Node 0	Quad 3 Node A
Node 1	Quad 3 Node B
Node 2	Quad 2 Node A
Node 3	Quad 2 Node B
Node 4	Quad 1 Node A
Node 5	Quad 1 Node B
Node 6	Quad 0 Node A
Node 7	Quad 0 Node B

Cable Bulkhead for CRAY T916 and CRAY T932 Systems (IO2 Module)



See previous page for node assignments.

IO1/2 Fuzz-button Connector Pin Assignments



I/O Channel Assignments (CRAY T94 System)

IO Module	CPU Physical Number	Shared Rel. CPU Number	IO Module Quadrant	VHISP Number	LOSP Number	HISP Number	Support Channel Number
A	0	0	0	20	100/101,102/103	400, 401	60/61
	1	1	1	21	104/105,106/107	402, 403	
	2	2	2	22	110/111,112/113	404, 405	
	3	3	3	23	114/115,116/117	406, 407	

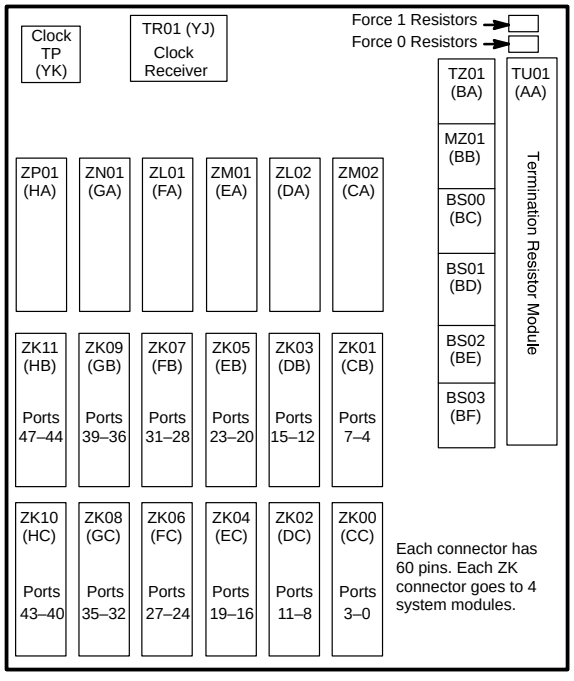
I/O Channel Assignments (CRAY T916 System)

IO Module	CPU Physical Number	Shared Rel. CPU Number	IO Module Quadrant	VHISP Number	LOSP Number	HISP Number	Support Channel Number
I	2	2	0	20	100/101,102/103	400, 401	
	3	3	1	21	104/105,106/107	402, 403	60/61
	4	4	2	22	110/111,112/113	404, 405	
	5	5	3	23	114/115,116/117	406, 407	
E	12	12	3	24	120/121,122/123	410, 411	
	13	13	2	25	124/125,126/127	412, 413	
	14	14	1	26	130/131,132/133	414, 415	60/61
	15	15	0	27	134/135,136/137	416, 417	

I/O Channel Assignments (CRAY T932 System)

IO Module	CPU Physical Number	IO Module Quadrant	VHISP Number	LOSP Number	HISP Number	Support Channel Number
A	22	0	30	140/141,142/143	420, 421	
	23	1	31	144/145,146/147	422, 423	64/65
	24	2	32	150/151,152/153	424, 425	
	25	3	33	154/155,156/157	426, 427	
E	12	3	24	120/121,122/123	410, 411	
	13	2	25	124/125,126/127	412, 413	
	14	1	26	130/131,132/133	414, 415	62/63
	15	0	27	134/135,136/137	416, 417	
I	2	0	20	100/101,102/103	400, 401	
	3	1	21	104/105,106/107	402, 403	60/61
	4	2	22	110/111,112/113	404, 405	
	5	3	23	114/115,116/117	406, 407	
M	32	3	34	160/161,162/163	430, 431	
	33	2	35	164/165,166/167	432, 433	
	34	1	36	170/171,172/173	434, 435	66/67
	35	0	37	174/175,176/177	436, 437	

Boundary Scan Connector Layout



Boundary Scan Module Connectors for CRAY T94 System

Connector Location	Port Numbers	Destination
CB	7 – 4	C1, A1
EB	23 – 20	C5, C4, C3, C2
FA, EA	– –	Maintenance Channel from bulkhead
GA	– –	Control System
GB	39 – 36	B1, B2, B3, B4
HA	– –	Maintenance Connector
DA, CA	– –	Passon Channel from IO module

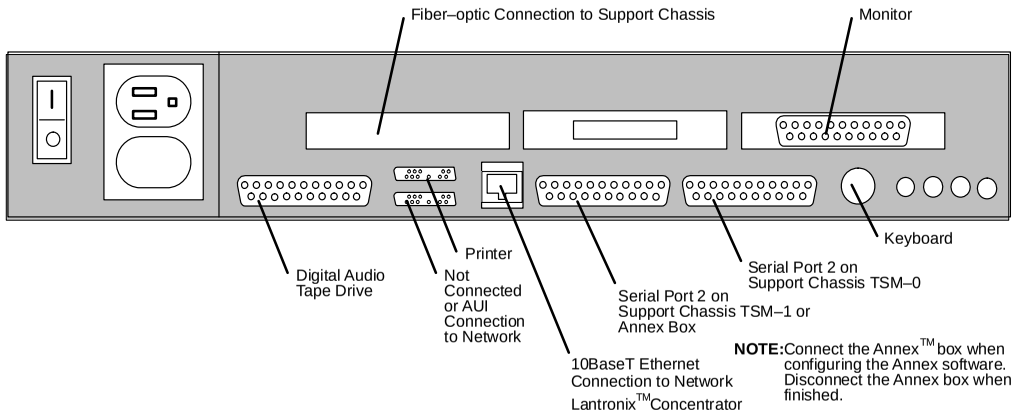
Boundary Scan Module Connectors for CRAY T916 and CRAY T932 Systems (Quadrants 0 and 1)

Connector Location	Port Numbers	Module Destination		External Destination
		Stack	Number	
HA	– –	– –	– –	Maintenance Connector
HB	47 – 44	H	1 – 4	– –
HC	43 – 40	L	1 – 4	– –
GA	– –	– –	– –	Control System
GB	39 – 36	H	5 – 8	– –
GC	35 – 32	L	5 – 8	
FA, EA	– –	– –	– –	Maintenance Channel from bulkhead
FB	31 – 28	G5, E, I		– –
FC	27 – 24	Spare		– –
EB	23 – 20	G	1 – 4	– –
EC	19 – 16	K	1 – 4	– –
DB	15 – 12	F	1 – 4	– –
DC	11 – 8	J	1 – 4	– –
CB	7 – 4	F	5 – 8	– –
CC	3 – 0	J	5 – 8	– –
DA, CA	– –	– –	– –	Passon Channel from IO module

Boundary Scan Module Connectors for CRAY T932 System (Quadrands 2 and 3)

Connector Location	Port Number	Module Destination		External Destination
		Stack	Number	
HA	– –	– –	– –	Maintenance Connector
HB	47 – 44	P	1 – 4	– –
HC	43 – 40	D	1 – 4	– –
GA	– –	– –	– –	Control System
GB	39 – 36	P	5 – 8	– –
GC	35 – 32	D	5 – 8	
FA, EA	– –	– –	– –	Maintenance Channel from bulkhead
FB	31 – 28	G5, A, M		– –
FC	27 – 24	Spare		– –
EB	23 – 20	O	1 – 4	– –
EC	19 – 16	C	1 – 4	– –
DB	15 – 12	N	1 – 4	– –
DC	11 – 8	J	1 – 4	
CB	7 – 4	N	5 – 8	– –
CC	3 – 0	B	5 – 8	– –
DA, CA	– –	– –	– –	Passon Channel from IO module

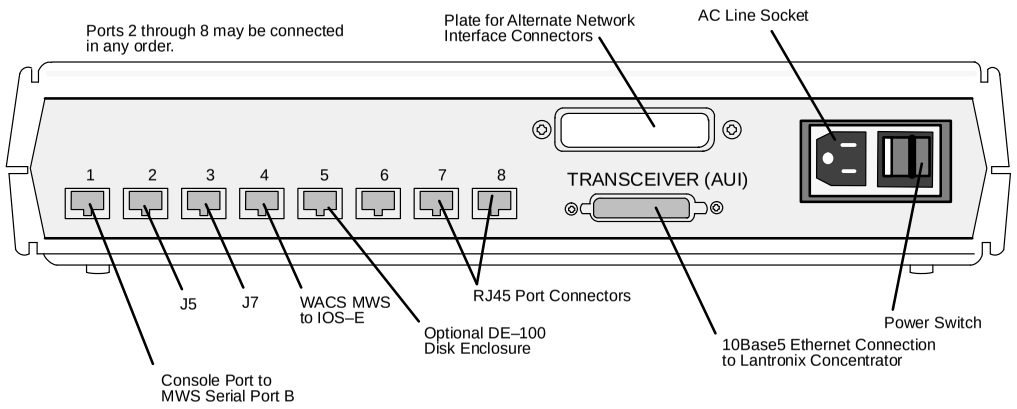
MWS Connectors



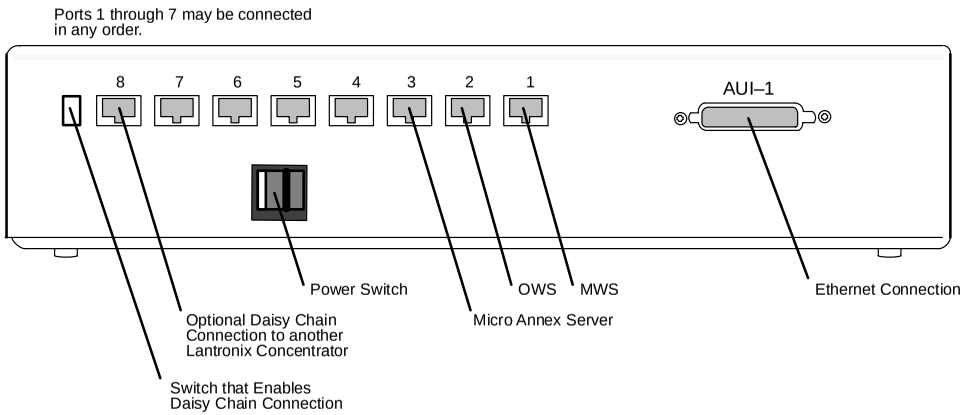
NOTE: Connect the Annex™ box when configuring the Annex software. Disconnect the Annex box when finished.

OWS Connectors

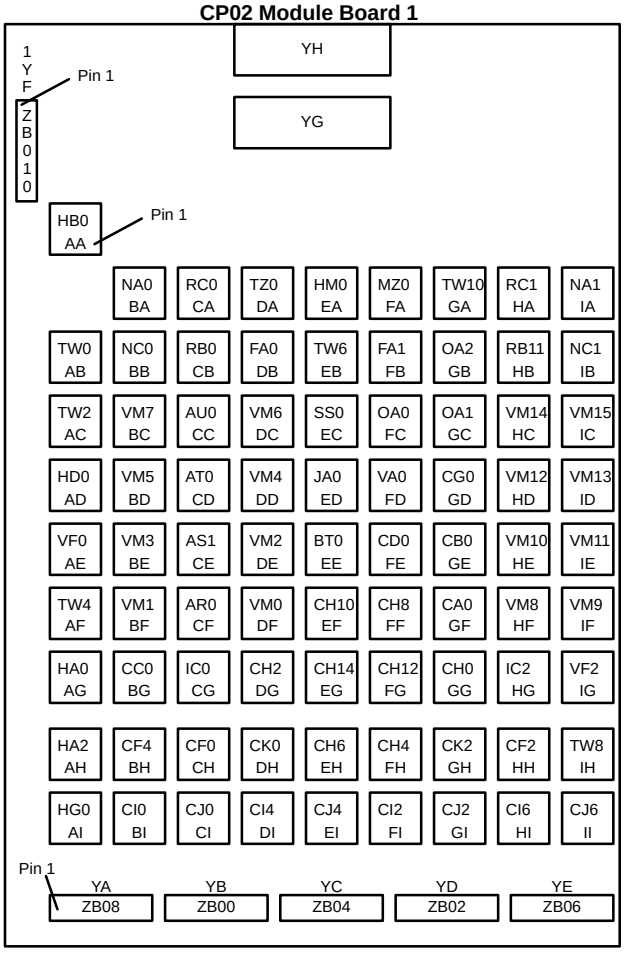
Micro Annex™ Connectors



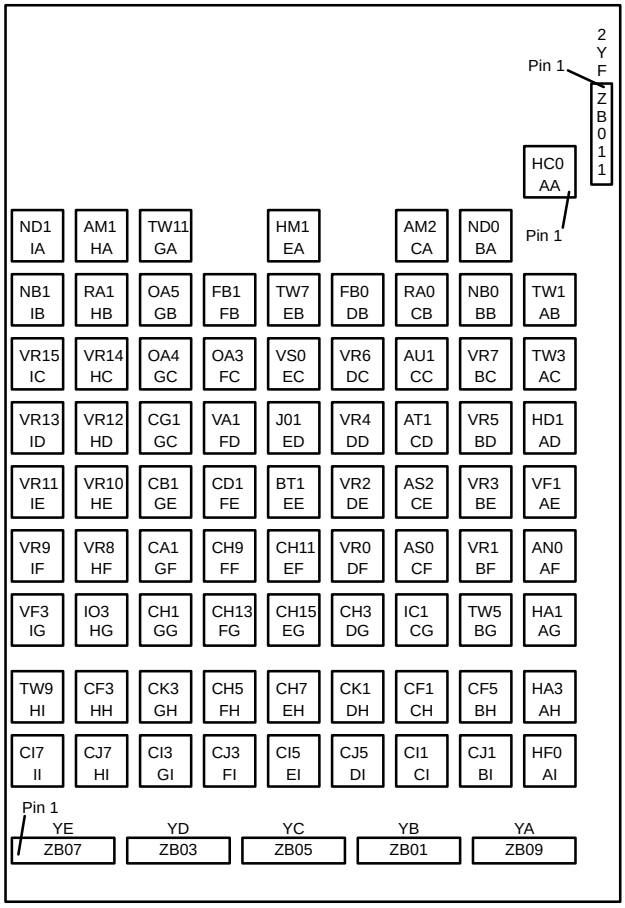
Lantronix Concentrator Connectors



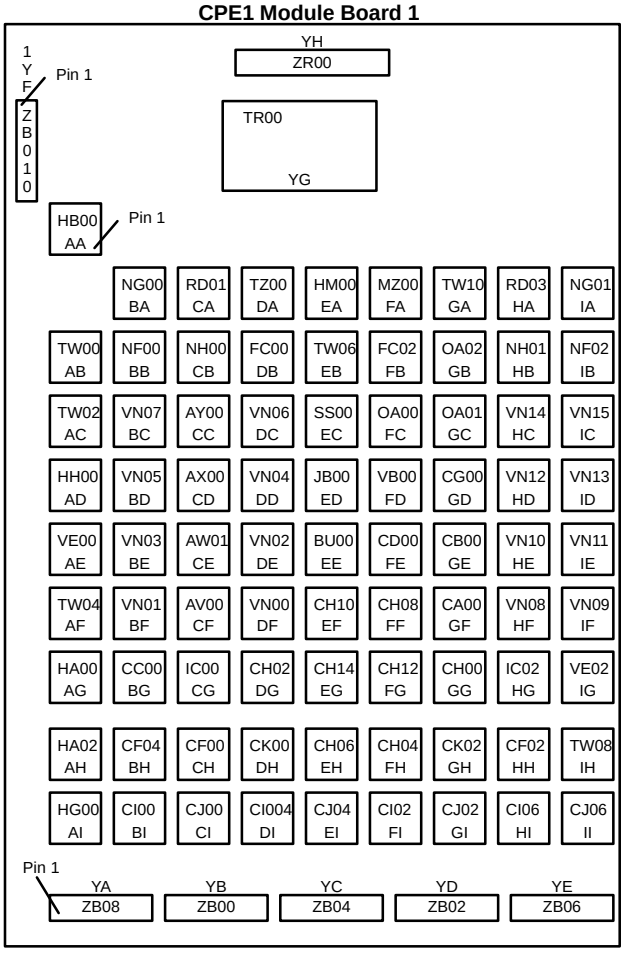
CP02 Module Board 1



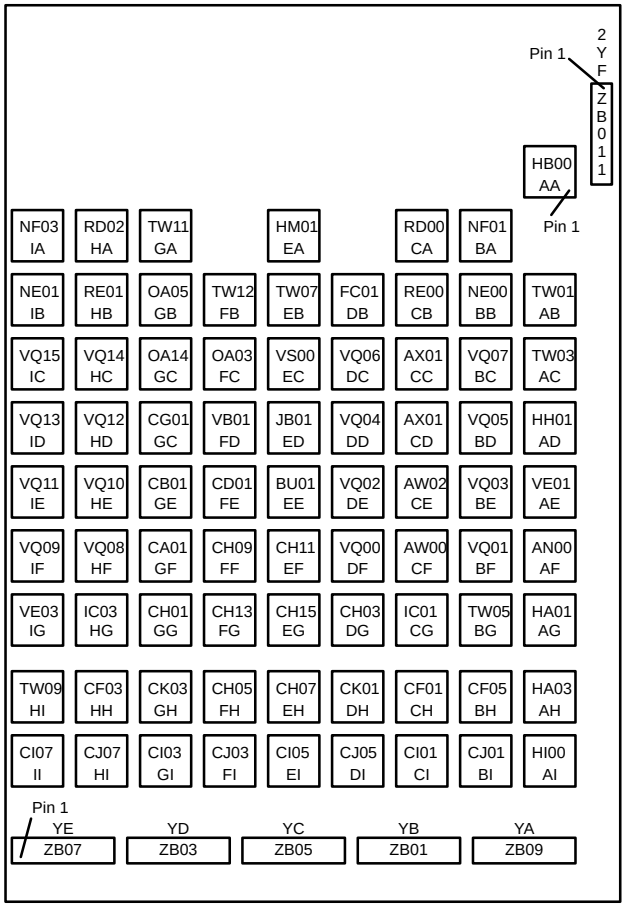
CP02 Module Board 2



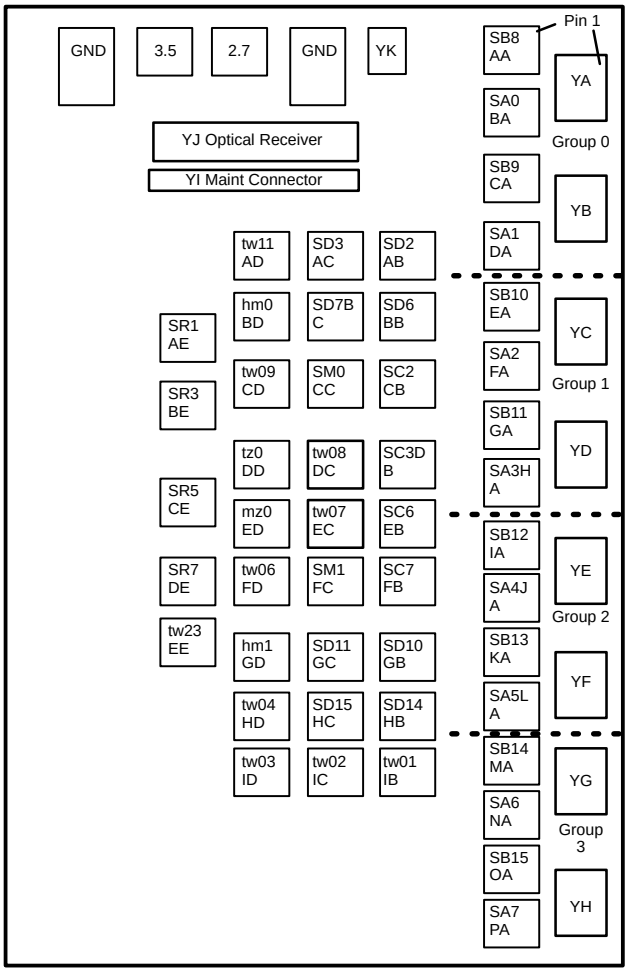
CPE1 Module Board 1



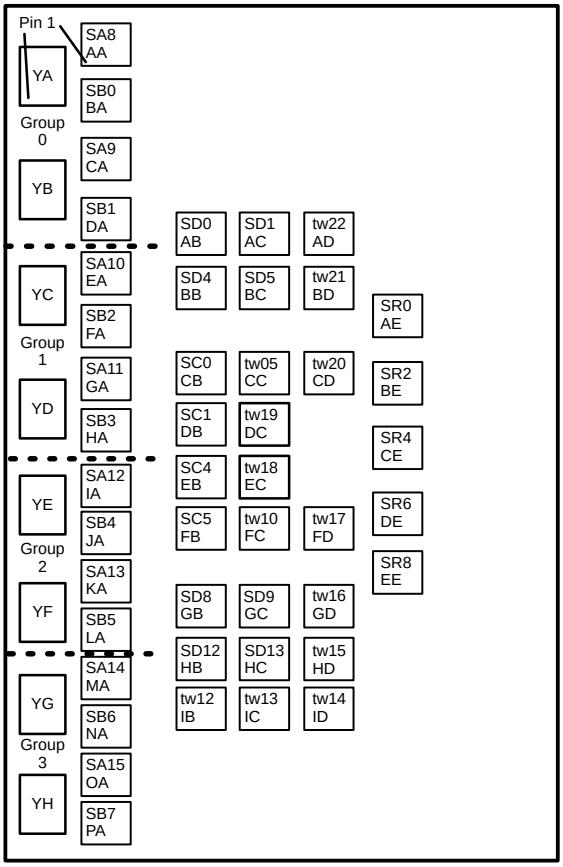
CPE1 Module Board 2



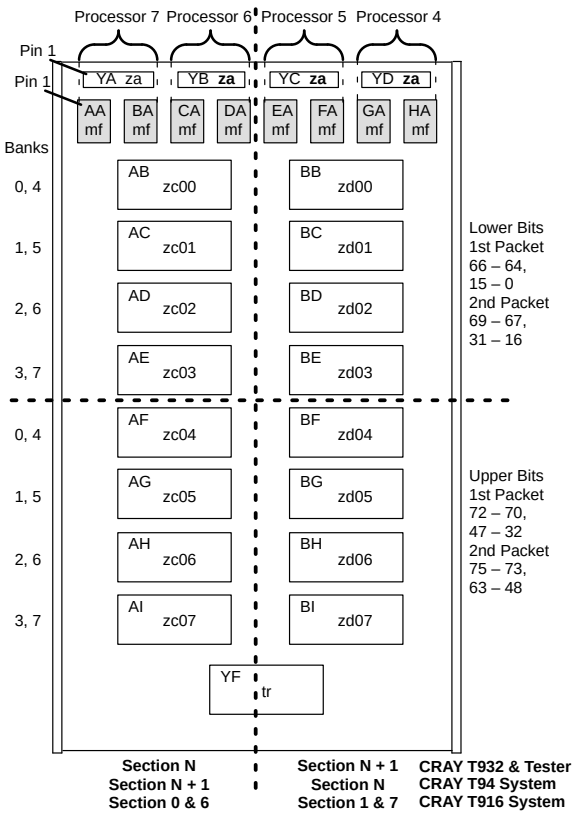
SR01 Module Board 1



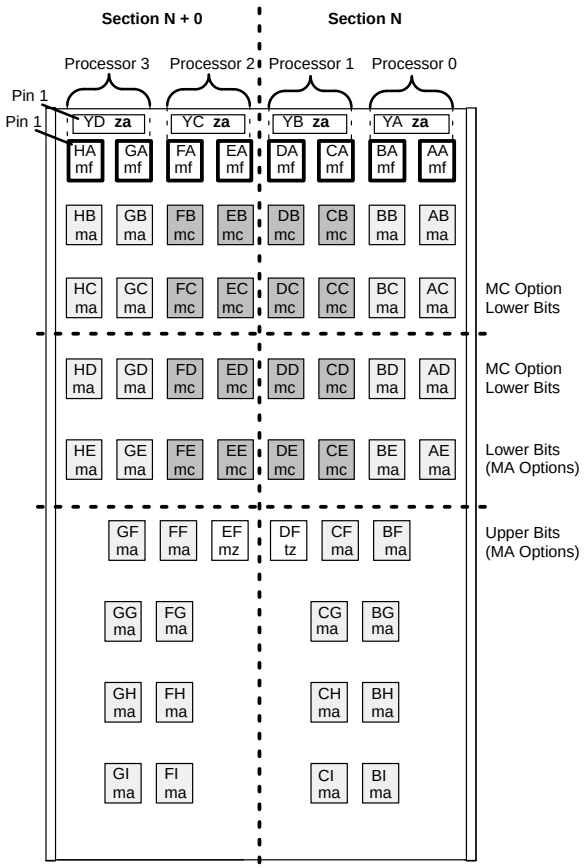
SR01 Module Board 2



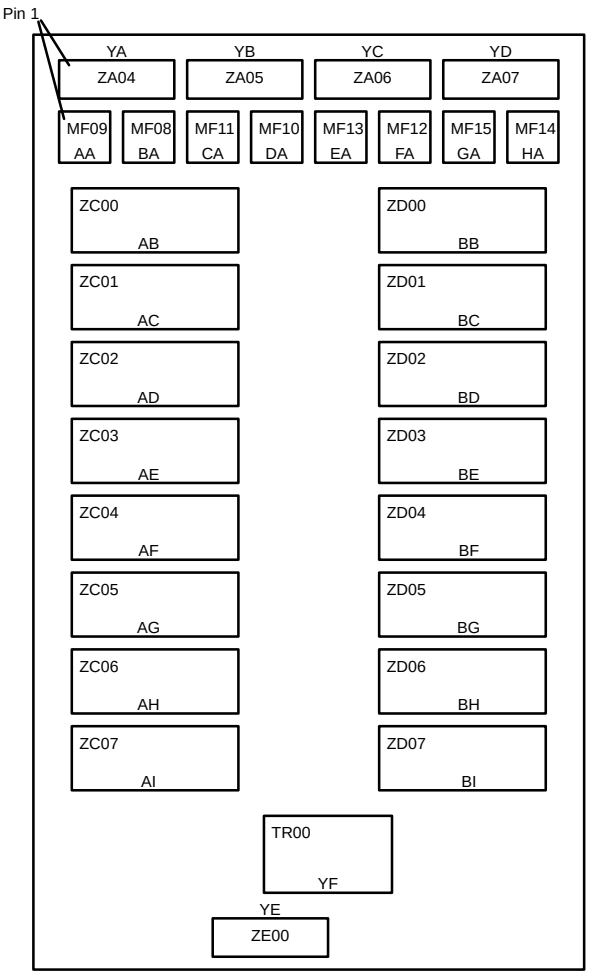
CM02 Module Board 1



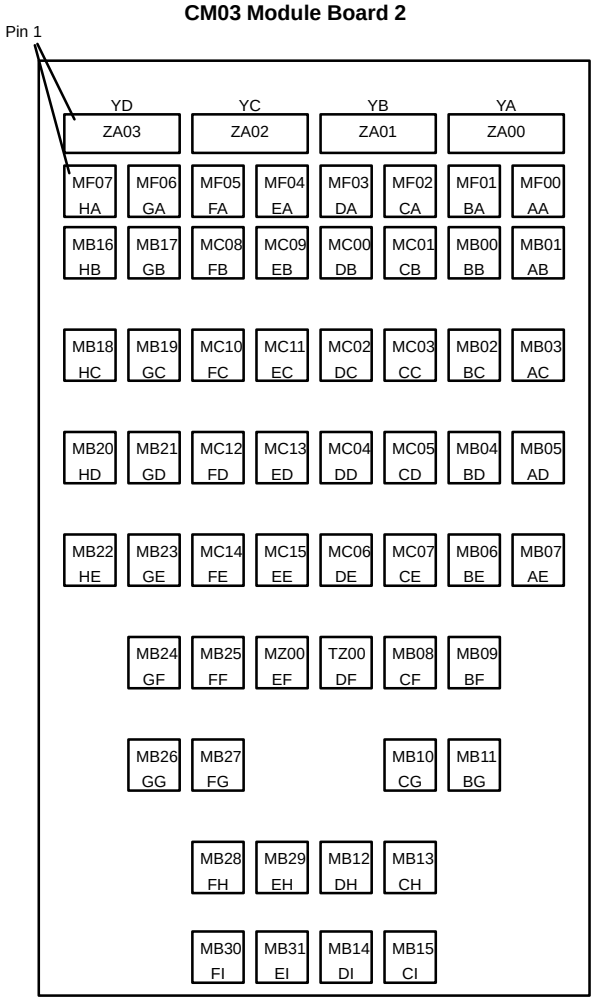
CM02 Module Board 2



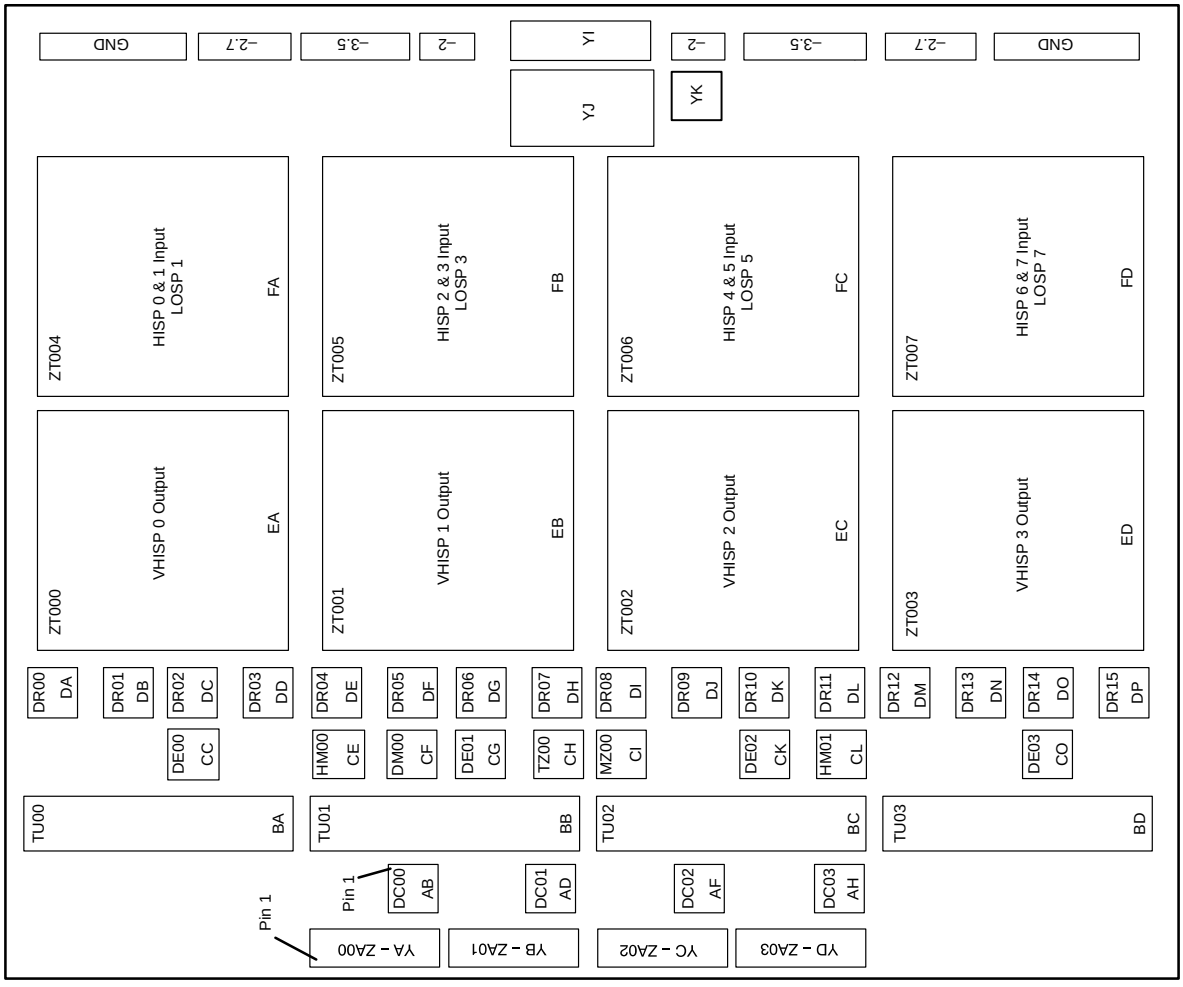
CM03 Module Board 1



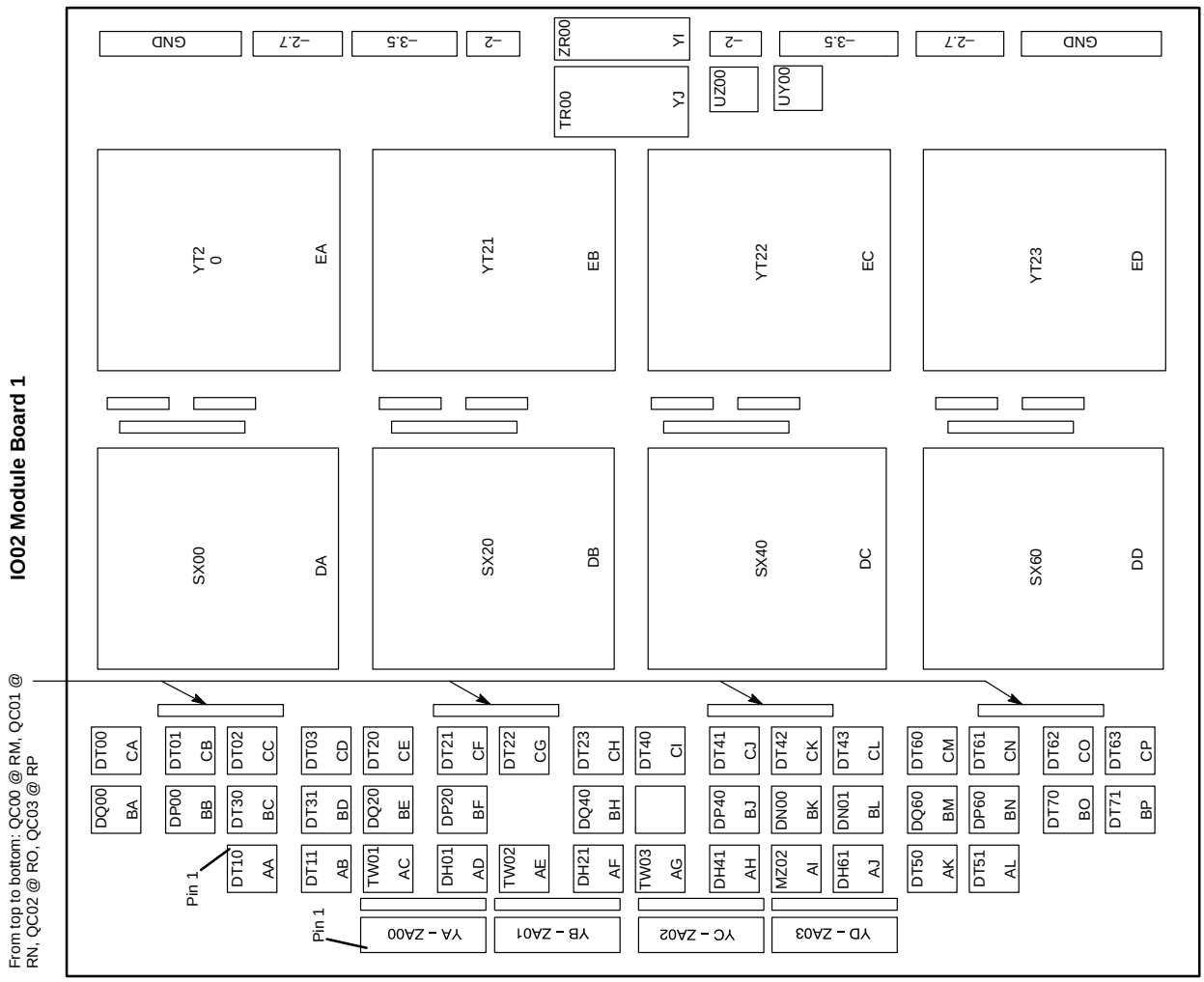
CM03 Module Board 2



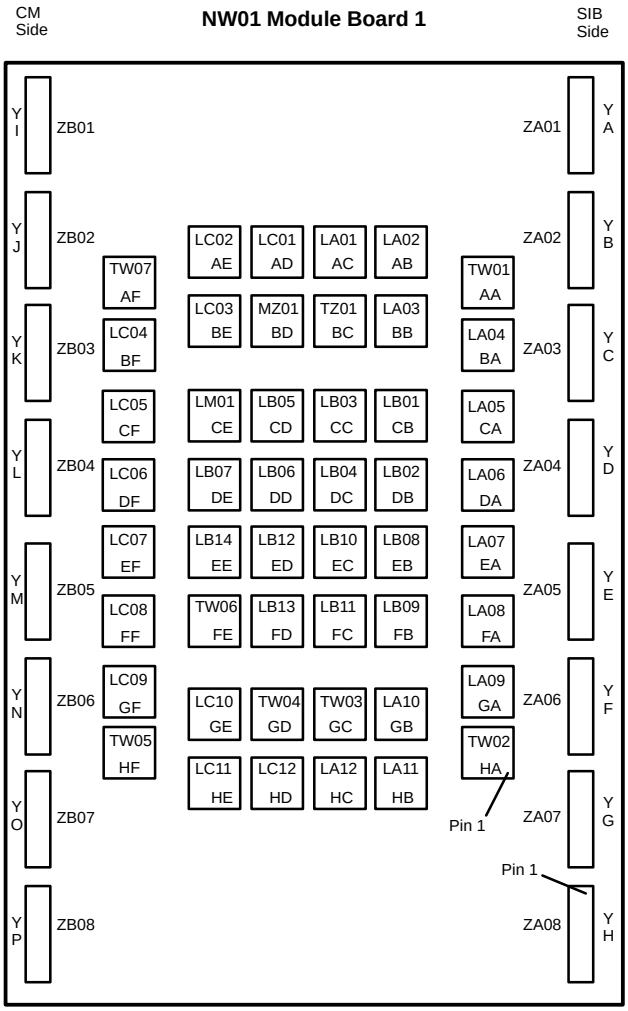
IO01 Module Board 1

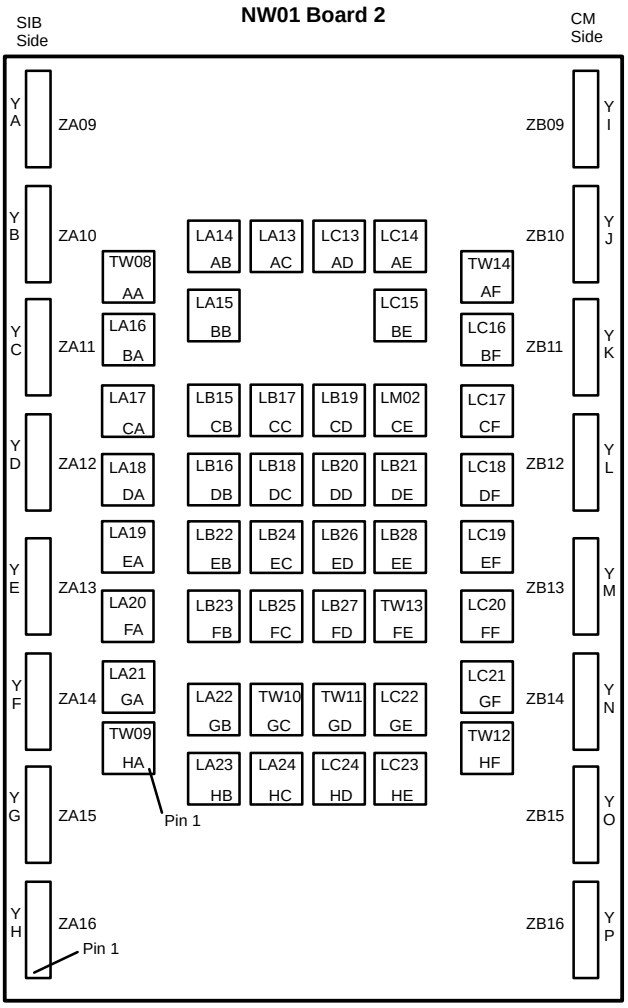


IO01 Module Board 2
GND
–2.7
–3.5
–2
–2
–3.5
–2.7
GND
ZT012
HISP 0 & 1 Output
LOSP 0
FA
ZT013
HISP 2 & 3 Output
LOSP 2
FB
ZT014
HISP 4 & 5 Output
LOSP 4
FC
ZT015
HISP 6 & 7 Output
LOSP 6
FD
ZT008
VHISP 0 Input
Maintenance
EA
ZT009
VHISP 1 Input
Support
EB
ZT010
VHISP 2 Input
Error Logger
EC
ZT011
VHISP 3 Input
MCU
ED
DR16 DA
DR17 DB
DR18 DC
DR19 DD
DR20 DE
DR21 DF
DR22 DG
DR23 DH
DR24 DI
DR25 DJ
DR26 DK
DR27 DL
DR28 DM
DR29 DN
DR30 DO
DR31 DP
DD00 CB
DD01 CF
DD02 CJ
DD03 CN
TU04
BA
TU05
BB
TU06
BC
TU07
BD
Pin 1
DB00 AA
DA00 AB
DB01 AC
DA01 AD
DB02 AE
DA02 AF
DB03 AG
DA03 AH
Pin 1
YA – ZA04
YB – ZA05
YC – ZA06
YD – ZA07


IO02 Module Board 1
From top to bottom: QC00 @ RM, QC01 @ RN, QC02 @ RO, QC03 @ RP
Pin 1
Pin 1
YA – ZA00
YB – ZA01
YC – ZA02
YD – ZA03
SX00
DA
SX20
DB
SX40
DC
SX60
DD
YT20
EA
YT21
EB
YT22
EC
YT23
ED
GND
–2.7
–3.5
–2
ZR00
Y1
TR00
YJ
UZ00
UY00
–2
–3.5
–2.7
GND
DT00 CA
DQ00 BA
DT10 AA
DT01 CB
DP00 BB
DT11 AB
DT02 CC
DT30 BC
TW01 AC
DT03 CD
DT31 BD
DH01 AD
DT20 CE
DQ20 BE
TW02 AE
DT21 CF
DP20 BF
DH21 AF
DT22 CG
TW03 AG
DT23 CH
DQ40 BH
DH41 AH
DT40 CI
DT41 CJ
DP40 BJ
MZ02 AI
DN00 BK
DH61 AJ
DT42 CK
DN01 BL
DT50 AK
DT43 CL
DQ60 BM
DT51 AL
DT60 CM
DP60 BN
DT61 CN
DT70 BO
DT62 CO
DT71 BP
DT63 CP

IO02 Module Board 2
GND
–2.7
–3.5
–2
–2
–3.5
–2.7
GND
YT24 EA
YT25 EB
YT26 EC
YT27 ED
SX01 DA
SX21 DB
SX41 DC
SX61 DD
DT04 CA
DT05 CB
DT06 CC
DT07 CD
DT24 CE
DT25 CF
DT26 CG
DT27 CH
DT44 CI
DT45 CJ
DT46 CK
DT47 CL
DT64 CM
DT65 CN
DT66 CO
DT67 CP
TW04 BA
DQ01 BB
DT32 BC
DT33 BC
HM00 BD
DQ21 BF
MZ01 BG
MZ00 BH
TZ01 BI
DQ41 BJ
DN02 BK
DN03 BL
HM01 BM
DQ61 BN
DT72 BO
DT73 BP
Pin 1
DT12 AA
DT13 AB
DG00 AC
DH00 AD
DH20 AE
DH20 AF
DG40 AG
DH40 AH
DG60 AI
DH60 AJ
DT52 AK
DT53 AL
Pin 1
YA – ZA04
YB – ZA05
YC – ZA06
YD – ZA07


CM Side
NW01 Module Board 1
SIB Side
YI
ZB01
ZA01
YA
YJ
ZB02
ZA02
YB
YK
ZB03
ZA03
YC
YL
ZB04
ZA04
YD
YM
ZB05
ZA05
YE
YN
ZB06
ZA06
YF
YO
ZB07
ZA07
YG
YP
ZB08
ZA08
YH
LC02 AE
LC01 AD
LA01 AC
LA02 AB
TW07 AF
TW01 AA
LC03 BE
MZ01 BD
TZ01 BC
LA03 BB
LC04 BF
LA04 BA
LC05 CF
LM01 CE
LB05 CD
LB03 CC
LB01 CB
LA05 CA
LC06 DF
LB07 DE
LB06 DD
LB04 DC
LB02 DB
LA06 DA
LC07 EF
LB14 EE
LB12 ED
LB10 EC
LB08 EB
LA07 EA
LC08 FF
TW06 FE
LB13 FD
LB11 FC
LB09 FB
LA08 FA
LC09 GF
LA09 GA
LC10 GE
TW04 GD
TW03 GC
LA10 GB
TW05 HF
TW02 HA
LC11 HE
LC12 HD
LA12 HC
LA11 HB
Pin 1
Pin 1


NW01 Board 2
SIB Side
CM Side
YA
ZA09
ZB09
YI
YB
ZA10
ZB10
YJ
YC
ZA11
ZB11
YK
YD
ZA12
ZB12
YL
YE
ZA13
ZB13
YM
YF
ZA14
ZB14
YN
YG
ZA15
ZB15
YO
YH
ZA16
ZB16
YP
TW08 AA
LA14 AB
LA13 AC
LC13 AD
LC14 AE
TW14 AF
LA15 BB
LC15 BE
LA16 BA
LC16 BF
LA17 CA
LB15 CB
LB17 CC
LB19 CD
LM02 CE
LC17 CF
LA18 DA
LB16 DB
LB18 DC
LB20 DD
LB21 DE
LC18 DF
LA19 EA
LB22 EB
LB24 EC
LB26 ED
LB28 EE
LC19 EF
LA20 FA
LB23 FB
LB25 FC
LB27 FD
TW13 FE
LC20 FF
LA21 GA
LA22 GB
TW10 GC
TW11 GD
LC22 GE
LC21 GF
TW09 HA
LA23 HB
LA24 HC
LC24 HD
LC23 HE
TW12 HF
Pin 1
Pin 1

Notes

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