



Dear Registrant:

Software Training courses are skills based. Each is designed to help participants acquire the set of skills that is listed in the Software Training Catalog course description. The learning log for a course is a simple tool that allows individuals to set proficiency goals for each skill and then to track progress toward those goals. The learning logs for the courses you are registered for are attached.

We suggest that you review with your supervisor the list of skills addressed in each course from the perspective of the tasks that you perform on the job. Ideally you and your supervisor would agree upon goal levels for each of the skills. This would give you a map of where to best expend time and energy. During each course there will be opportunities to test proficiency in each skill and to track progress on the learning logs for the course. There is also a comprehensive test given at the end of each course to review and reinforce the key concepts introduced.

We look forward to seeing you in Eagan.

Sincerely,

A handwritten signature in cursive script that reads "Barbara J. Brunzell".

Barbara J. Brunzell
Software Publications and Training Manager

cc: Registrant's supervisor

C R A Y R E S E A R C H, I N C.
Software Training

655 - A Lone Oak Drive
Eagan, Minnesota 55121
(800) 284-2729

To: Ed Barnard (000742)
CRAY RESEARCH, INC.
655-F Lone Oak Drive
Eagan MN 55121
Site: MH

From: June Erickson
Registrar

Date: Mar 07, 1991

Subject: REGISTRATION CONFIRMATION

-
This is to confirm that you have been registered for the following training course(s) on the date(s) indicated below:

Class: I/O Subsystem Operating System Internals - IOS
Class Dates: Mar 11, 1991 through Mar 22, 1991
Class Hours: 8:30-5:00-except 2nd W 2:00pm-11:00pm-2nd Th 2:00pm-11:00p.m.
Night lab: 2nd Wed. (2:00 p.m.-11:00 p.m.) & an optional lab the 2nd Thurs.
Class ends at noon on the 2nd Friday.
Customers must have a signed Cray Research software license for UNICOS and a verified AT&T UNIX System V (release 3.0 or higher) license or specifically licensed for COS.

Unless otherwise noted above, classes will be held at the Software Training Center Building (address above).

If there are any changes necessary, please notify me immediately. All rescheduling must be done no later than (2) weeks prior to the beginning date of each class.

Thank you for your cooperation.

CC: Marti Bancroft
Cray Research, Inc.
655-F Lone Oak Drive
Eagan MN 55121

~~Rachel Pettit
Cray Research (UK) Ltd.
Cray House, London Road
Bracknell
Berkshire RG12 2SY
ENGLAND~~

Table 1. Summary of the data sets used in the study.

Dataset	Number of Samples	Number of Features	Number of Classes
Dataset 1	1000	100	10
Dataset 2	2000	200	20
Dataset 3	5000	500	50
Dataset 4	10000	1000	100
Dataset 5	20000	2000	200
Dataset 6	50000	5000	500
Dataset 7	100000	10000	1000
Dataset 8	200000	20000	2000
Dataset 9	500000	50000	5000
Dataset 10	1000000	100000	10000

The datasets are generated using a random process. Each dataset is a collection of samples, where each sample is a vector of features. The number of features and the number of classes increase linearly with the number of samples. The data is split into training and testing sets. The training set is used to train the model, and the testing set is used to evaluate the model's performance.

IOS Operating System Internals Class

AGENDA for 1st Week
Mar. 11 - 22, 1991

CHAPTER	TOPIC	PRESENTER	DATE/DAY/TIME
1	Introduction	Leon Vann	3-11/Mon/8:30-11:30
	Hardware Overview	" "	
2	APML Syntax	" "	
3	APML Pseudos	" "	/1:00-4:30
4	APML Macros	" "	
5	CSIM Testing	Leon Vann	3-12/Tue/8:30-11:30
	Terminal Time	" "	
6	Operating Sys Overview	" "	/1:00-4:30
7	Resources	" "	
	Terminal Time	" "	/4:30-
8	Software Structures	Leon Vann	3-13/Wed/8:30-11:30
10	Overlays	" "	/1:00-3:30
	Terminal Time	" "	/3:30-
9	Inter-IOP Communication	Leon Vann	3-14/Thr/8:30-11:30
11	The Kernel	" "	/1:00-4:00
	Terminal Time	" "	/4:00-
12	Deadstart/Initialization	Leon Vann	3-15/Fri/8:30-11:30
13	IOS Generation	Stuart Johnson	/1:00-4:00
	Terminal Time	Leon Vann	/4:00-

Class	Section	Days	Time	Room	Instructor	Prerequisites
ENGR 101	001	Tu	10:00-11:00	101	Dr. Smith	ENGR 100
ENGR 101	002	Th	10:00-11:00	102	Dr. Smith	ENGR 100
ENGR 101	003	Mo	10:00-11:00	103	Dr. Smith	ENGR 100
ENGR 101	004	We	10:00-11:00	104	Dr. Smith	ENGR 100
ENGR 101	005	Fr	10:00-11:00	105	Dr. Smith	ENGR 100
ENGR 101	006	Sa	10:00-11:00	106	Dr. Smith	ENGR 100
ENGR 101	007	Su	10:00-11:00	107	Dr. Smith	ENGR 100
ENGR 101	008	Mo	11:00-12:00	108	Dr. Smith	ENGR 100
ENGR 101	009	Th	11:00-12:00	109	Dr. Smith	ENGR 100
ENGR 101	010	Mo	12:00-1:00	110	Dr. Smith	ENGR 100
ENGR 101	011	Th	12:00-1:00	111	Dr. Smith	ENGR 100
ENGR 101	012	Mo	1:00-2:00	112	Dr. Smith	ENGR 100
ENGR 101	013	Th	1:00-2:00	113	Dr. Smith	ENGR 100
ENGR 101	014	Mo	2:00-3:00	114	Dr. Smith	ENGR 100
ENGR 101	015	Th	2:00-3:00	115	Dr. Smith	ENGR 100
ENGR 101	016	Mo	3:00-4:00	116	Dr. Smith	ENGR 100
ENGR 101	017	Th	3:00-4:00	117	Dr. Smith	ENGR 100
ENGR 101	018	Mo	4:00-5:00	118	Dr. Smith	ENGR 100
ENGR 101	019	Th	4:00-5:00	119	Dr. Smith	ENGR 100
ENGR 101	020	Mo	5:00-6:00	120	Dr. Smith	ENGR 100
ENGR 101	021	Th	5:00-6:00	121	Dr. Smith	ENGR 100
ENGR 101	022	Mo	6:00-7:00	122	Dr. Smith	ENGR 100
ENGR 101	023	Th	6:00-7:00	123	Dr. Smith	ENGR 100
ENGR 101	024	Mo	7:00-8:00	124	Dr. Smith	ENGR 100
ENGR 101	025	Th	7:00-8:00	125	Dr. Smith	ENGR 100
ENGR 101	026	Mo	8:00-9:00	126	Dr. Smith	ENGR 100
ENGR 101	027	Th	8:00-9:00	127	Dr. Smith	ENGR 100
ENGR 101	028	Mo	9:00-10:00	128	Dr. Smith	ENGR 100
ENGR 101	029	Th	9:00-10:00	129	Dr. Smith	ENGR 100
ENGR 101	030	Mo	10:00-11:00	130	Dr. Smith	ENGR 100
ENGR 101	031	Th	10:00-11:00	131	Dr. Smith	ENGR 100
ENGR 101	032	Mo	11:00-12:00	132	Dr. Smith	ENGR 100
ENGR 101	033	Th	11:00-12:00	133	Dr. Smith	ENGR 100
ENGR 101	034	Mo	12:00-1:00	134	Dr. Smith	ENGR 100
ENGR 101	035	Th	12:00-1:00	135	Dr. Smith	ENGR 100
ENGR 101	036	Mo	1:00-2:00	136	Dr. Smith	ENGR 100
ENGR 101	037	Th	1:00-2:00	137	Dr. Smith	ENGR 100
ENGR 101	038	Mo	2:00-3:00	138	Dr. Smith	ENGR 100
ENGR 101	039	Th	2:00-3:00	139	Dr. Smith	ENGR 100
ENGR 101	040	Mo	3:00-4:00	140	Dr. Smith	ENGR 100
ENGR 101	041	Th	3:00-4:00	141	Dr. Smith	ENGR 100
ENGR 101	042	Mo	4:00-5:00	142	Dr. Smith	ENGR 100
ENGR 101	043	Th	4:00-5:00	143	Dr. Smith	ENGR 100
ENGR 101	044	Mo	5:00-6:00	144	Dr. Smith	ENGR 100
ENGR 101	045	Th	5:00-6:00	145	Dr. Smith	ENGR 100
ENGR 101	046	Mo	6:00-7:00	146	Dr. Smith	ENGR 100
ENGR 101	047	Th	6:00-7:00	147	Dr. Smith	ENGR 100
ENGR 101	048	Mo	7:00-8:00	148	Dr. Smith	ENGR 100
ENGR 101	049	Th	7:00-8:00	149	Dr. Smith	ENGR 100
ENGR 101	050	Mo	8:00-9:00	150	Dr. Smith	ENGR 100
ENGR 101	051	Th	8:00-9:00	151	Dr. Smith	ENGR 100
ENGR 101	052	Mo	9:00-10:00	152	Dr. Smith	ENGR 100
ENGR 101	053	Th	9:00-10:00	153	Dr. Smith	ENGR 100
ENGR 101	054	Mo	10:00-11:00	154	Dr. Smith	ENGR 100
ENGR 101	055	Th	10:00-11:00	155	Dr. Smith	ENGR 100
ENGR 101	056	Mo	11:00-12:00	156	Dr. Smith	ENGR 100
ENGR 101	057	Th	11:00-12:00	157	Dr. Smith	ENGR 100
ENGR 101	058	Mo	12:00-1:00	158	Dr. Smith	ENGR 100
ENGR 101	059	Th	12:00-1:00	159	Dr. Smith	ENGR 100
ENGR 101	060	Mo	1:00-2:00	160	Dr. Smith	ENGR 100
ENGR 101	061	Th	1:00-2:00	161	Dr. Smith	ENGR 100
ENGR 101	062	Mo	2:00-3:00	162	Dr. Smith	ENGR 100
ENGR 101	063	Th	2:00-3:00	163	Dr. Smith	ENGR 100
ENGR 101	064	Mo	3:00-4:00	164	Dr. Smith	ENGR 100
ENGR 101	065	Th	3:00-4:00	165	Dr. Smith	ENGR 100
ENGR 101	066	Mo	4:00-5:00	166	Dr. Smith	ENGR 100
ENGR 101	067	Th	4:00-5:00	167	Dr. Smith	ENGR 100
ENGR 101	068	Mo	5:00-6:00	168	Dr. Smith	ENGR 100
ENGR 101	069	Th	5:00-6:00	169	Dr. Smith	ENGR 100
ENGR 101	070	Mo	6:00-7:00	170	Dr. Smith	ENGR 100
ENGR 101	071	Th	6:00-7:00	171	Dr. Smith	ENGR 100
ENGR 101	072	Mo	7:00-8:00	172	Dr. Smith	ENGR 100
ENGR 101	073	Th	7:00-8:00	173	Dr. Smith	ENGR 100
ENGR 101	074	Mo	8:00-9:00	174	Dr. Smith	ENGR 100
ENGR 101	075	Th	8:00-9:00	175	Dr. Smith	ENGR 100
ENGR 101	076	Mo	9:00-10:00	176	Dr. Smith	ENGR 100
ENGR 101	077	Th	9:00-10:00	177	Dr. Smith	ENGR 100
ENGR 101	078	Mo	10:00-11:00	178	Dr. Smith	ENGR 100
ENGR 101	079	Th	10:00-11:00	179	Dr. Smith	ENGR 100
ENGR 101	080	Mo	11:00-12:00	180	Dr. Smith	ENGR 100
ENGR 101	081	Th	11:00-12:00	181	Dr. Smith	ENGR 100
ENGR 101	082	Mo	12:00-1:00	182	Dr. Smith	ENGR 100
ENGR 101	083	Th	12:00-1:00	183	Dr. Smith	ENGR 100
ENGR 101	084	Mo	1:00-2:00	184	Dr. Smith	ENGR 100
ENGR 101	085	Th	1:00-2:00	185	Dr. Smith	ENGR 100
ENGR 101	086	Mo	2:00-3:00	186	Dr. Smith	ENGR 100
ENGR 101	087	Th	2:00-3:00	187	Dr. Smith	ENGR 100
ENGR 101	088	Mo	3:00-4:00	188	Dr. Smith	ENGR 100
ENGR 101	089	Th	3:00-4:00	189	Dr. Smith	ENGR 100
ENGR 101	090	Mo	4:00-5:00	190	Dr. Smith	ENGR 100
ENGR 101	091	Th	4:00-5:00	191	Dr. Smith	ENGR 100
ENGR 101	092	Mo	5:00-6:00	192	Dr. Smith	ENGR 100
ENGR 101	093	Th	5:00-6:00	193	Dr. Smith	ENGR 100
ENGR 101	094	Mo	6:00-7:00	194	Dr. Smith	ENGR 100
ENGR 101	095	Th	6:00-7:00	195	Dr. Smith	ENGR 100
ENGR 101	096	Mo	7:00-8:00	196	Dr. Smith	ENGR 100
ENGR 101	097	Th	7:00-8:00	197	Dr. Smith	ENGR 100
ENGR 101	098	Mo	8:00-9:00	198	Dr. Smith	ENGR 100
ENGR 101	099	Th	8:00-9:00	199	Dr. Smith	ENGR 100
ENGR 101	100	Mo	9:00-10:00	200	Dr. Smith	ENGR 100

Class Website
 Test & Review
 Learning Log
 Course Evaluation
 Faculty of Manager

IOS Operating System Internals Class

AGENDA for 2nd Week
Mar. 11 - 22, 1990

CHAPTER	TOPIC	PRESENTER	DATE/DAY/TIME
14	Disks	Leon Vann	3-18/Mon/8:30-11:30
15	Logical Devices	" "	/1:00-2:00
23	Debugging Aids	" "	/2:15-3:00
	Terminal Time	" "	/3:00-
	Front Ends		
16	NSC	Leon Vann	3-19/Tue/8:30-11:30
17	VME	" "	
18	FEI	" "	
19	COMM	" "	
21	User Channel I/O	" "	/1:00-3:00
22	HSX/HIPPI	" "	
	Terminal Time	" "	/3:00-
20	Tapes/BMX	Leon Vann	3-20/Wed/8:30-11:30
24	Dump Analysis(1st Dump)	" "	/1:00-4:30
	Dedicated Lab Time	" "	/17:00-23:00
24	Dump Analysis(2nd Dump)	Leon Vann	3-21/Thr/8:30-11:30
	New Features (7.0)	Stuart Johnson	/1:00-2:00
	Model E IOS	Jeff Koniges	/2:00-3:00
	Dedicated Lab Time	Leon Vann	/17:00-23:00
	Class Wrapup		
	Test & Review	Leon Vann	3-22/Fri/8:30-11:00
	Learning Logs		
	Course Evaluation		
	Review by Manager		

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To IOS Course Enrollees:

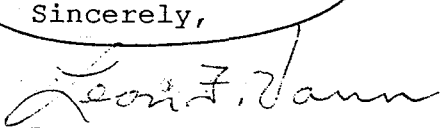
This is a packet of pre-course materials that will aid in preparing you to enter the Cray I/O Subsystem Architecture, APML and Operating System Internals course.

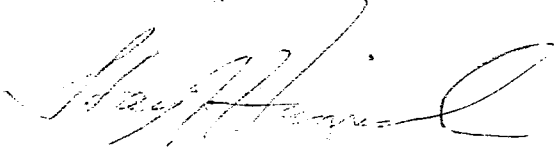
PLEASE try to allow yourself enough pre-course study time so that the exercises in the pre-course workbooks can be COMPLETED PRIOR TO CLASS. We realize that this may not always be possible so we have included a list of priorities. Please consult the priority list below and do AS MUCH of the pre-course work as you have time for.

- 1) Learning APML using the self-study workbook and the APML manual SM-0036 is of utmost importance. Knowledge of how to read APML is essential in any intimate contact you have with the IOS operating system, since it is written exclusively in APML. PRIOR EXPOSURE TO THE MATERIAL PROVIDED IN THIS PACKET WILL BE ASSUMED OF THOSE IN CLASS, and time will be spent only in reviewing APML, not teaching it "from the beginning".
- 2) Learning the IOS architecture is vital to understanding why various portions of the operating system are written as they are. Also, a knowledge of the hardware will allow you to understand any programming restraints you may encounter, as well as how to write efficient code. PRIOR EXPOSURE TO THE MATERIAL PROVIDED IN THIS PACKET WILL BE ASSUMED of those in class, and time will be spent only in reviewing the hardware at the block diagram level or higher.
- 3) Understanding all the material listed on the recommended reading list is vital to filling in any gaps in your knowledge of IOS that may be left even after the classroom lectures and the various exercises you will be asked to work through. The IOS class will not teach everything there is to know about the IOS, but it aims to teach you where you can find anything you need to know. A basic knowledge of the information covered by the reading lists is assumed in class.

If you have questions regarding the course, please call one of us at (612) 452-9410. We are looking forward to meeting you.

Sincerely,


Leon F. Vann


Stacy J. Heinrich

IOS Instructors
Software Training

INPUT / OUTPUT SUBSYSTEM PRE-COURSE PACKET

THIS PRE-COURSE PACKET:

...is intended to prepare you to attend the CRAY I/O Subsystem Class.

SKILLS ASSUMED:

Assembler experience (if only from TR-APML Self-Study Workbook)

Ability to use Unix on the Training Pyramid system to enter, edit and submit a program for execution on the Cray (a user guide is available in Mendota Heights.)

A general familiarity with the concepts of dump reading and analysis

A general familiarity with common data structures, such as linked lists, queues, and branch tables

BEFORE COMING TO CLASS:

Read the IOS Architecture Self-Study Workbook and the APML Self-Study Workbook, included in this pre-course packet, and do the exercises at the end of each chapter. This should require approximately twelve to sixteen hours of work. In class, this information will be reviewed only.

Read or review the items on the Recommended Reading List (enclosed).

IF CONVENIENT, PLEASE BRING TO CLASS (IOS 5.0 versions!):

SM-0036	APML Reference Manual
SQ-0059	APML Reference For COS and UNICOS (Card)
SG-0051 -or- SG-2005	IOS Operator's Guide For {COS UNICOS}
HR-0081	IOS Model C Hardware Reference Manual
CSM-1009-0000	IOS Models C/D System Programmer Reference
TR-IA	IOS Architecture Self-Study Workbook
TR-APML	APML Self-Study Workbook

IF YOU HAVE QUESTIONS:

Call Leon Vann or Stacy Heinrich, IOS Instructors, at (612) 683-3800

INPUT / OUTPUT SUBSYSTEM PRE-COURSE PACKET

ENCLOSURES:

TR-IA	IOS Architecture Self-Study Workbook
TR-APML	APML Self-Study Workbook
SM-0036	APML Reference Manual
SQ-0059	APML Reference For COS and UNICOS (Card)

Course Daily Schedule
Learning Log
Recommended Reading List Summary

DAILY SCHEDULE

MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY
Architecture Overview	Terminal Time	Resources Structures	Overlays	System Generation
APML Overview including Macros and Pseudos CSIM	IOS Overview	Inter-IOP Communication	The Kernel Initialization	Work Time

MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY
Subsystems	Subsystems IOS Development	9:00 AM Subsystems Terminal Time	10:00 AM Dump Analysis	History Trace Test & Review Evaluation
Terminal Time	Terminal Time	Debug Aids Dump Analysis		
		Dedicated Lab 4pm-10pm	Dedicated Lab (if needed) 4pm-10pm	9/8/89

Student Learning Log

I/O Subsystem Operating System Internals

IOS

Participant Name: _____

Supervisor Name: _____

Region/Country/Division: _____

Class Start Date: _____

Instructor Name: _____

Competency Levels

- 0 No experience and knowledge
- 1 Needs help with all parts of the task
- 2 Can do parts of a task requiring the skill
- 3 Can do the task with periodic assistance
- *4 Needs no assistance
- 5 No assistance, fast and accurate
- 6 No assistance, fast and accurate under pressure
- 7 No assistance, can lead others

Skills - At the end of the course the learner is able to:									
Read APLM source code, and interpret IOP machine code									
Write APLM source code									
Code Kernel Service Request functions									
Test APLM code using CSIM									
Write an IOS overlay and test using CSIM and dedicated lab time									
List each software subsystem, its functions and main components									
List resources available to help configure an IOS									
Use system generation utilities and procedures to build IOS binaries									
Deadstart and operate the IOS									
Use IOS utilities to aid in problem resolution									
Use IOS debugger to debug an overlay									
Locate important tables and resident overlays in an IOS dump									
Locate, in dump and listings, the \$PUNTIF that stopped the system									
Interpret IOS dump trace entries to determine why the system failed									
Competency Levels	0	1	2	3	*4	5	6	7	N/A

This learning log is intended as an aid to the learner in establishing goals and plotting progress. It is not intended as an indicator of job performance and therefore should not be used in determining future job actions.

* Maximum level discernible by the instructor in an instructional environment.

INPUT / OUTPUT SUBSYSTEM PRE-COURSE PACKET

UNICOS Recommended Reading List

SR-2022 UNICOS ADMINISTRATOR COMMANDS REFERENCE

adstape

bind

fdmp

make

SG-2059A CSIM USER'S GUIDE FOR UNICOS

Section 1.2: Starting CSIM

Section 2.1: Interactive Hardware Definition

Section 4.2: Running a Simulated System

Section 5.7: Stopping the Simulation

Section 7: Miscellaneous Directives

Appendix D.2: IOS Simulation Example - Booting from the Expander

-or-

Appendix D.3: Sample VME Simulation

SG-2005D IOS OPERATOR'S GUIDE FOR UNICOS

Appendix B: Startup Procedure

Appendix C: IOS File Editor (to edit startup parameter file)

Appendix D: IOS Dump Programs

SM-0042G FRONT-END PROTOCOL INTERNAL REFERENCE

Section 1: Introduction

Section 2: General Concepts

SG-0307A IOS ADMINISTRATOR'S GUIDE

Section 1.2: Generation Procedures Under UNICOS

Section 2: IOS System Configuration

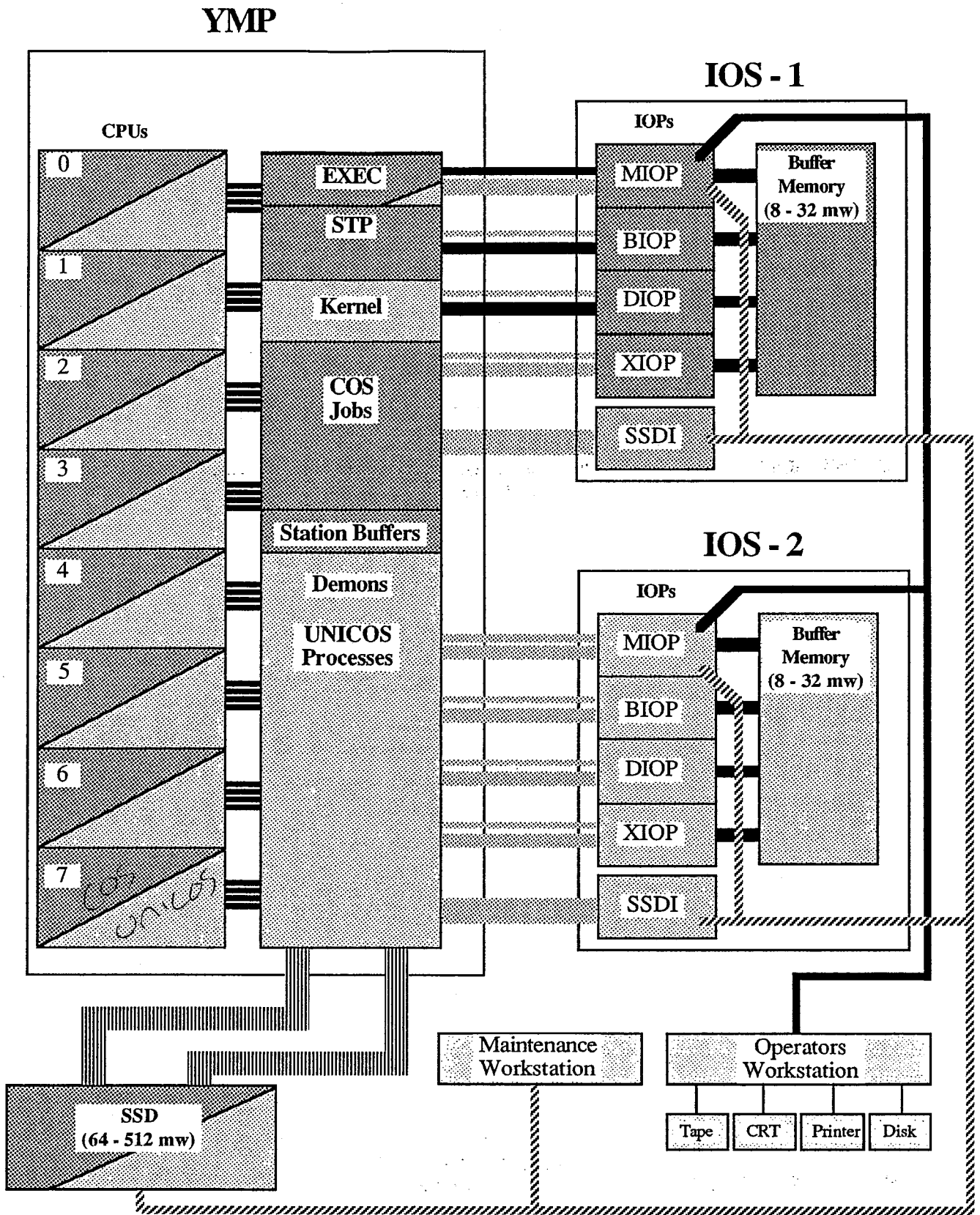
Section 4.1: History Trace

Section 4.2: Debugger

Appendix A: IOS Installation Parameters

Y-MP 8 32 - GOS

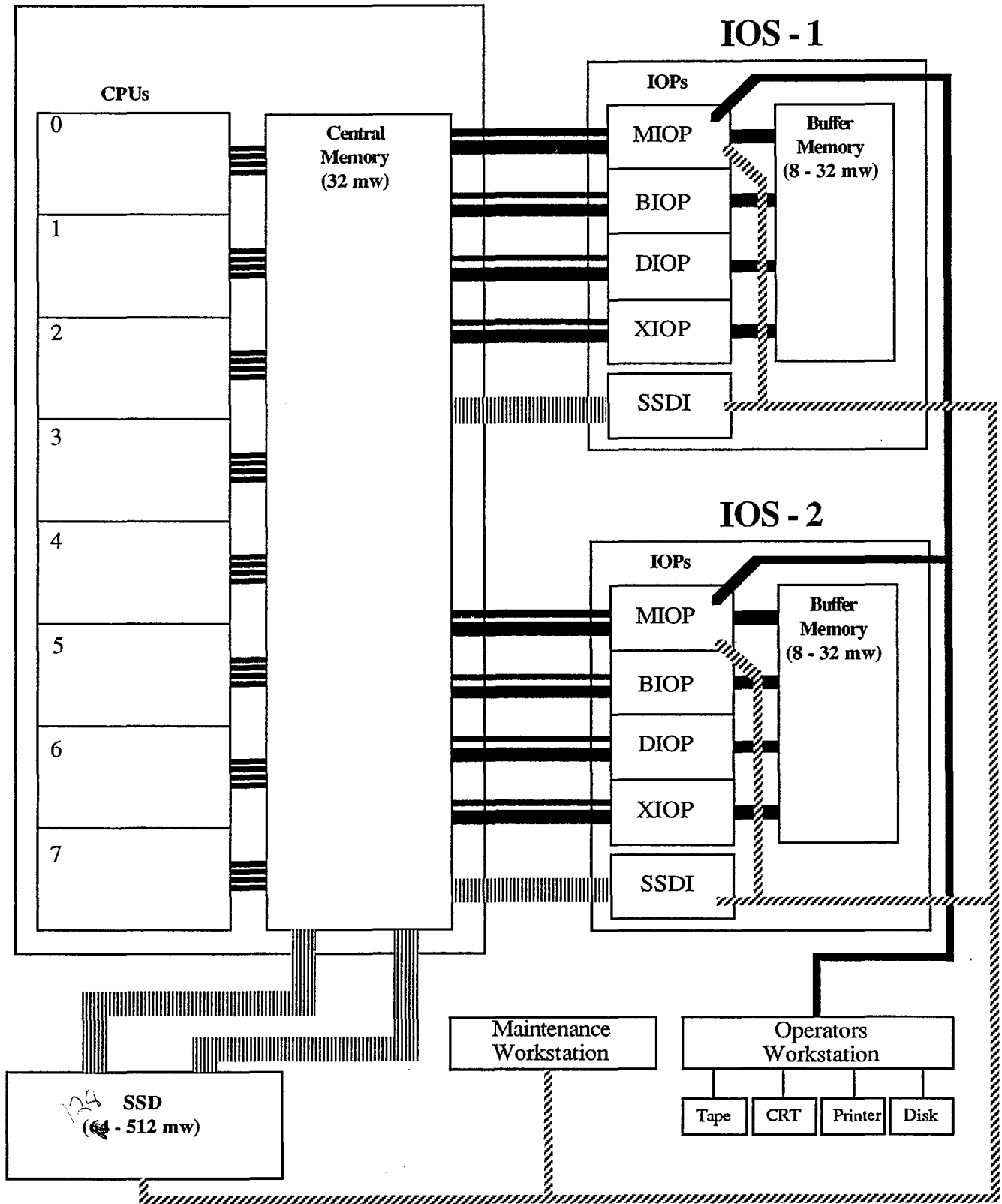
1.17 COS
4.0 UNICOS



Cray Proprietary

Y-MP 8 32

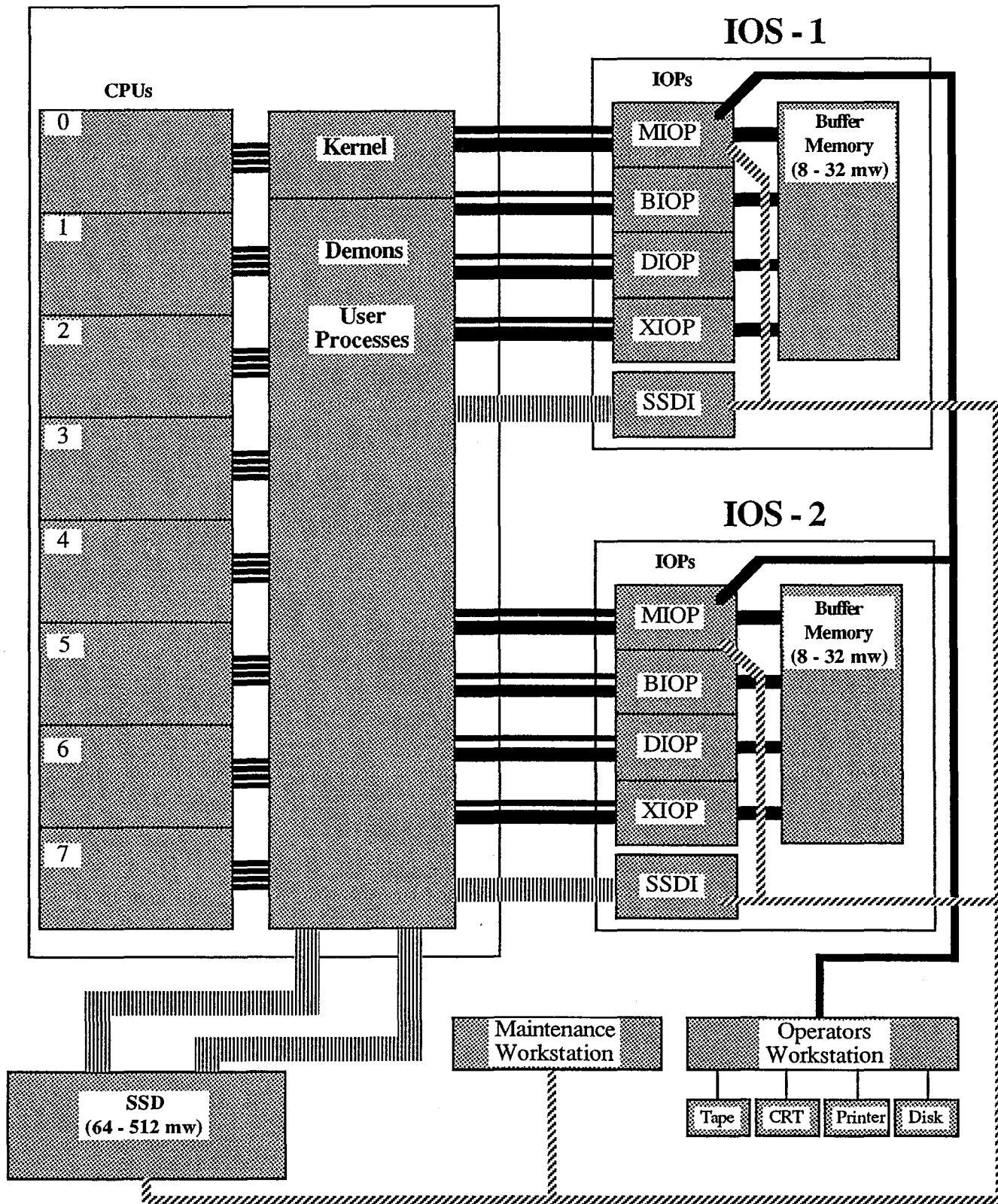
YMP



Cray Proprietary

Y-MP 8 32 - UNICOS

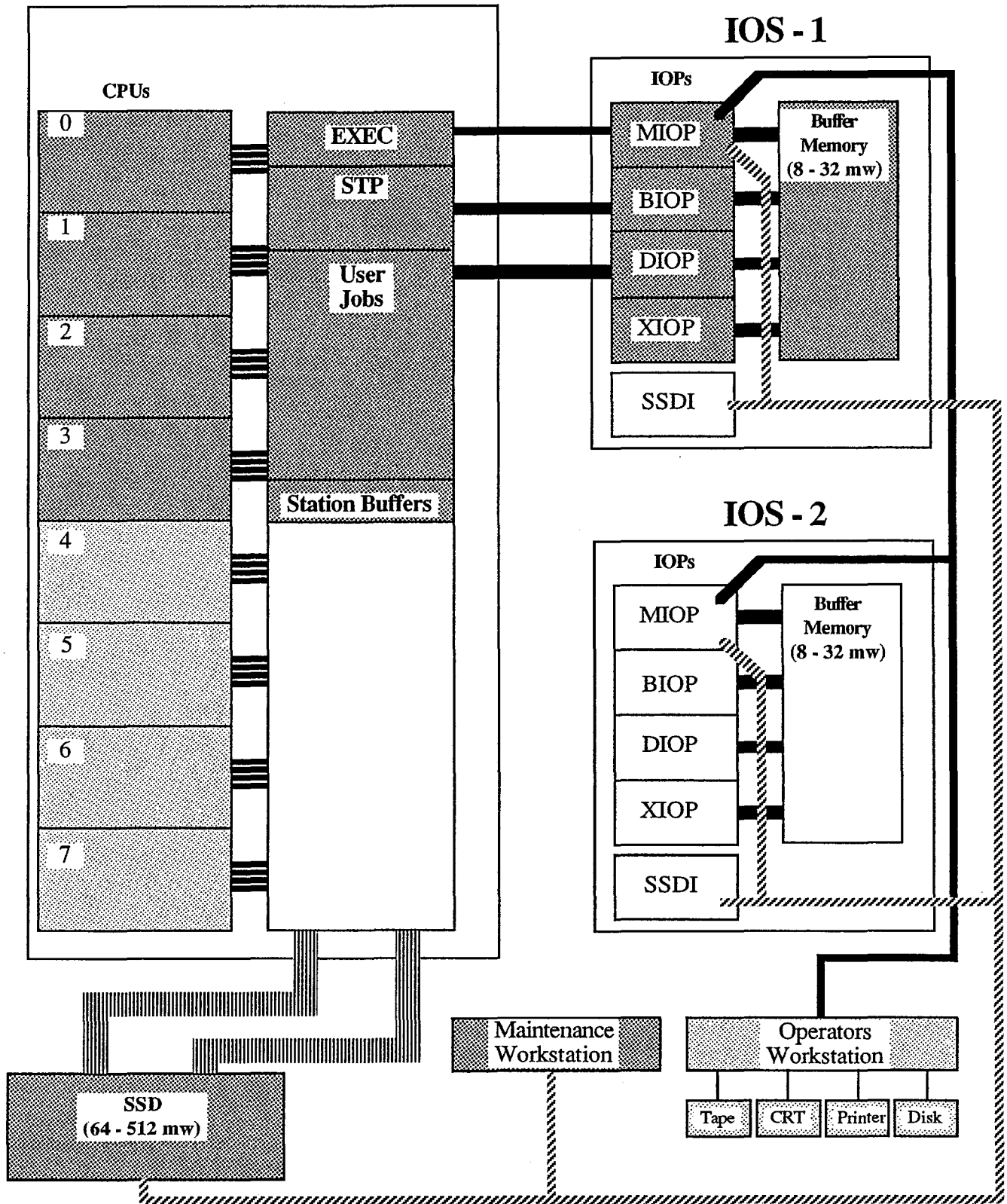
YMP



Cray Proprietary

Y-MP 8 32 - COS

YMP



Cray Proprietary

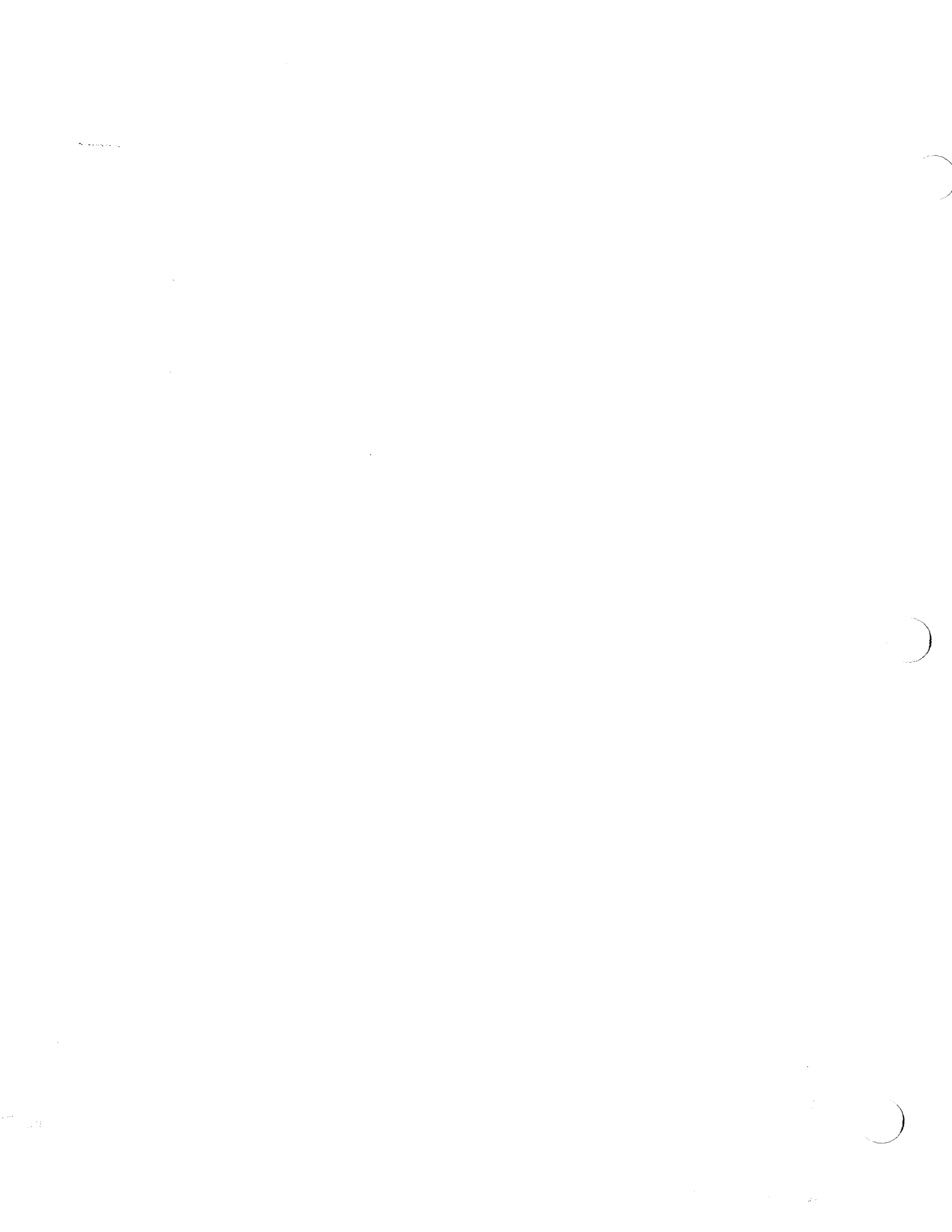


CRAY Y-MP Course Outline

- Monday - 8:30 - Introduction
- 8:45 - Physical description of Hardware
- 9:45 - The new technology.
- 10:45 - Description of Memory
- 1 p.m. - Exchange Process
- 2:15 - Instruction Fetch
- 3:30 - Instruction Issue
- Tuesday - 8:30 - Shared Registers
- 9:30 - Functional units and
Computational registers
- 1 p.m. - Software Overview
- Wednesday - 8:30 - Y-MP Instruction set
- 9:30 - The assembler and
new instructions

Jane
Norman
- instructor

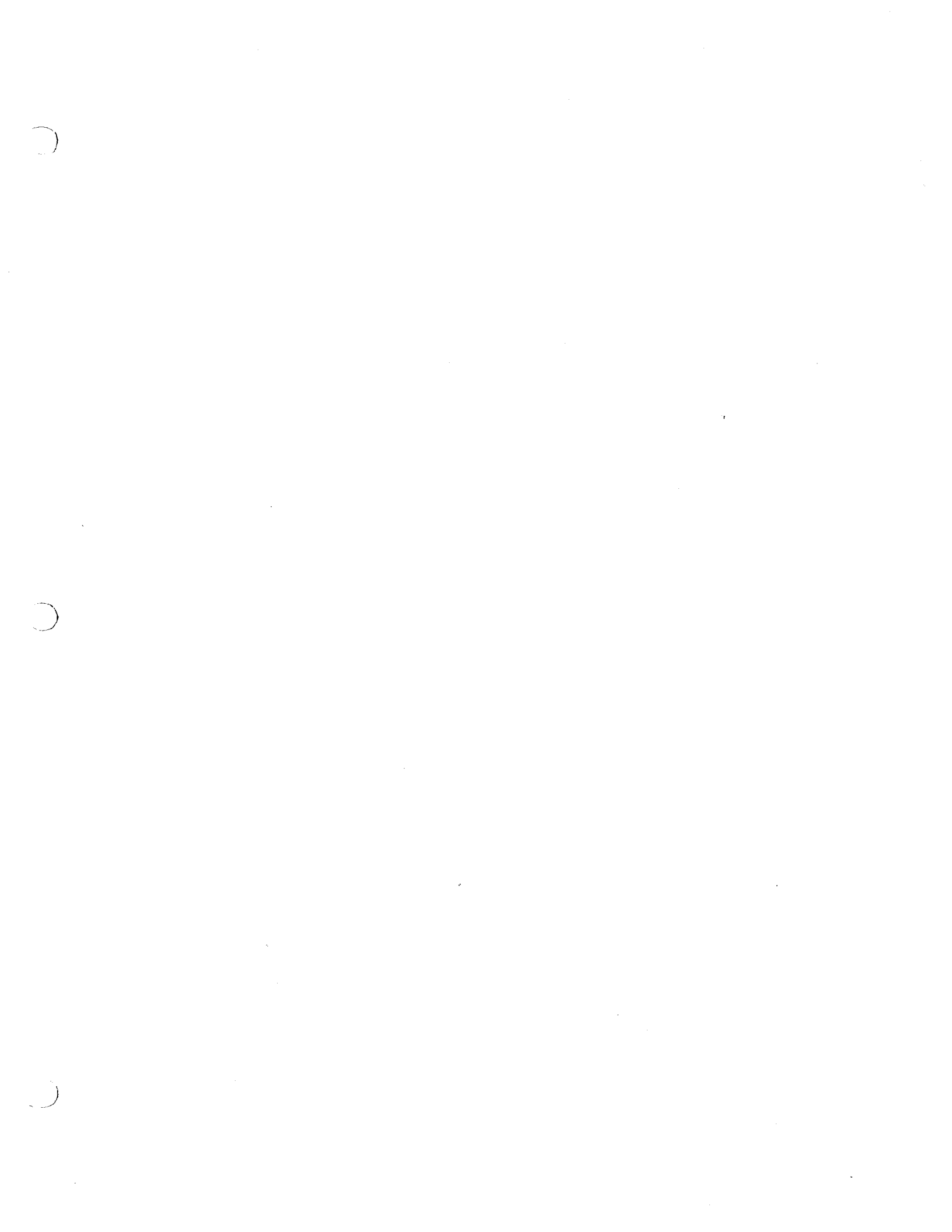
Kevin
Sexton
(Sexton, Hagen
to U)



CLASS ROSTERCourse YCALDate 2-8-88Instructor Jane Norman

We will have a class roster typed up with local and "permanent" address for your use. Please include only those addresses that you want to share with the rest of the class.

NAME As you want it to appear on the certificate (in parenthesis the name you want to be referred to by)	Local Address and phone #	Permanent or work address and phone number
Koushik Ghosh	681-3688	CRI 1333 Northland Dr., MH
Karl Feind	681-3034	CRI 1440 Northland Dr, MH
Steve Tucker	681-3327	CRI 1440 Northland Dr., MH
Melissa Mason	681-3185	CRI 1440 Northland Dr., MH
James Kruchowski	542-2000	CRI - Chippewa Falls, WI 715-726-1211
Jack Thompson	681-3118	1440 Northland Dr., MH
Steve Brown	681-5722	1345 Northland Dr., MH
Jim Kohn	681-5623	1345 Northland Dr., MH
Rich Klamann	Holiday Inn	LANL Mail B296 Los Alamos, NM 87544
Glen Peterson	681-3272	1440 Northland Dr., MH
Zbiginiew Karwowski	681-3294	1440 Northland Dr., MH
Larry Scott	681-5862	1345
Pete Bucheger	681-5846	1345
Sean Murphy	681-3127	1440
Hu Sheng	Compri Hotel RM 510	CRI - Petroleum Region 5847 San Felipe Suite 3000 Houston, TX 77057 713-965-758
Franz-Karl Schmatzer Paul Wells	Cedars Edina 681-3143	Cray Germany - Munich 1440



Buffer Memory Read Data

HINT: on the R terms — DMA R + 3 is mixed loop 50/51 with 1405
R2 - R87

HINT: on the 2BZ B20 - B27 is shared terms with CPU

Addressing

Hint:

Some As on the write to Buffer memory except that control is different

TERM F0, F1, F2, F3, F4, F5, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15

TP : D16, D44, D10, D18, D27, D33, D5, D25, C42, C67, C38, C46, C40, C70, C72, C48

GØ - G15 → VØ - V15

TERM: W0, W1, W2, W3, W4, W5, W6, W7, W8, W9, W10, W11, W12, W13, W14, W15

TP : D19, D44, D30, D17, D1, D4, D13, D15, C39, C71, C60, C58, C28, C54, C22, C24

W0-W15 → V20-V37 → RØ - R15

2BP

Even Buffer

TERM: G0, G1, G2, G3, G4, G5, G6, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G17

TP : C46, C44, C42, C38, C33, C35, C29, C31, C26, C25, D31, D50, D42, D35, D38, D40, D49, D48

ØDØ Buffer

TERM: G20, G21, G22, G23, G24, G25, G26, G27, G28, G29, G30, G31, G32, G33, G34, G35, G36, G37

TP : C48, C52, C50, C40, C18, C15, C4, C12, D23, D21, D29, D27, D36, D33, D31, D43, D46, D44
GØ - G37 → H20 - H37

TERM: J0, J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17

TP : C60, C53, C47, C51, C19, C32, C22, C21, C24, D30, D34, D59, D41, D54, D51, D45, D66, D62

Buffer Memory Pool - DATA

2NR:

Exp-219 → 1A6-119

TERM: B0, B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19

TP: B58', B16', B22', B60', B57', B56', B55', B54', A1', A3', A2', A11', A5', A15', A07', A13', A22', A18', A17', A52

TERM: C0, C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19

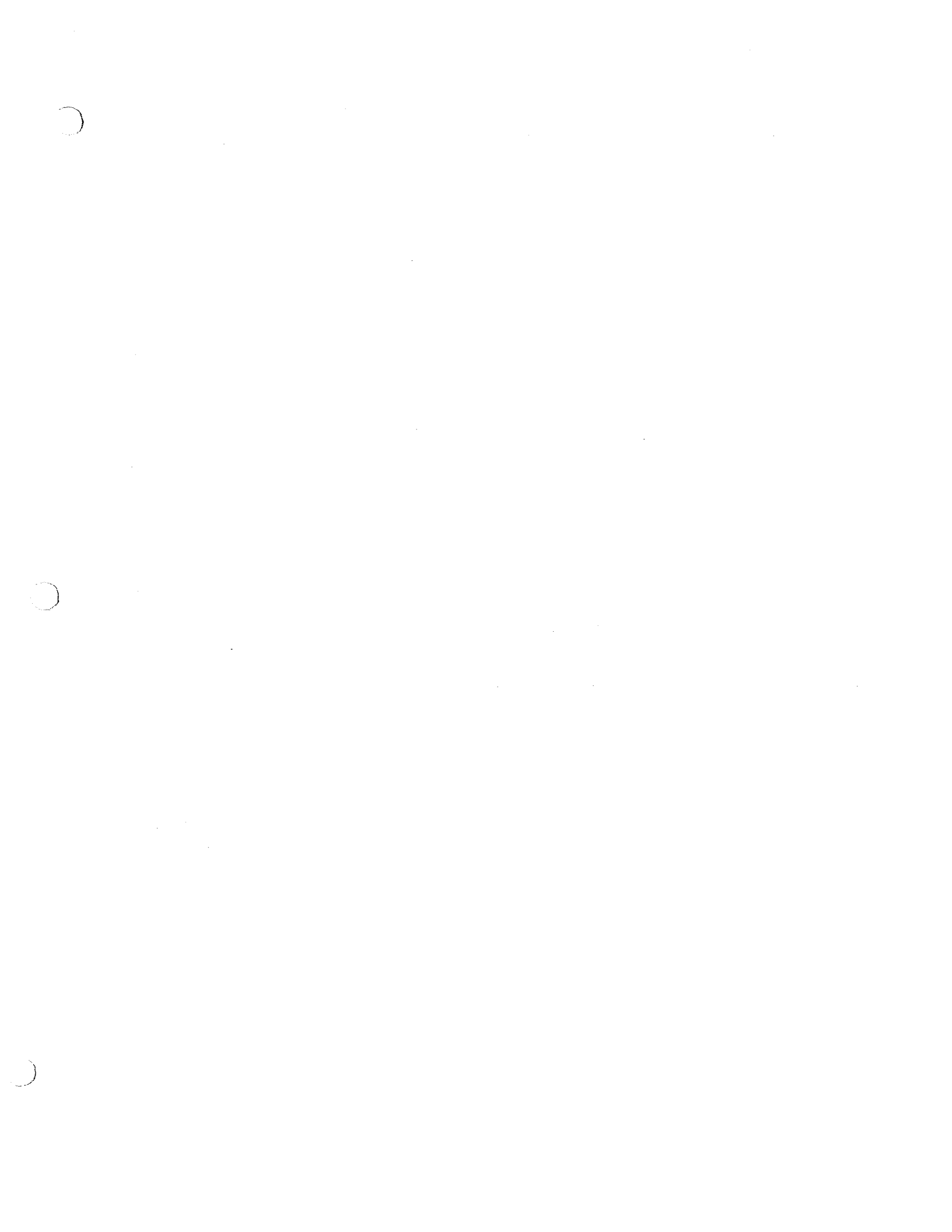
TP: B67', B68', B70', B72', B59', B61', B65', B63', A10', A8', A6', A4', A18', A16', A12', A14', A21', A16', A14', A62

TERM: D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19

TP: D8', D7', D12', D1', D3', D2', D6', D9', C63', C46', C36', C44', C45', C26', C68', C49'

TERM: E0, E1, E2, E3, E4, E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, E15

TP: D8', D2', D67', D70', D59', D1', D65', D63', C8', C3', C1', C25', C23', C12', C7'



2BH0

TERM:

B50, B51, B52, B53, B54, B55, B56, B57, B58, B59, B60, B61, B62, B63, B64, B65, B66, B67, B68, B69

IP:

B06, B03, B04, B35, B29, B29, B63, B59, B61, B14, B10, B12, B38, B36, B40, B72, B67, B70, A13, A05

TERM:

B70, B71, B72, B73

IP:

A00, A11, A16, A15

Incrementor: C terms - D terms

2NA:

↳ R32 - R55

HINT:

A terms, C terms, D terms, E terms, F terms

All terms are shared by all processors
↳ R terms

Form kas and cas lines for: Address for RFB
↳ Form kas and cas lines for: Address for RFB

2NK:

HINT I term go directly to R term no TP for 2NK → 2NA

0

0

0

11

Address for write to buffer memory

Addressing Local Memory & Block Length

2¹⁸L: $2^4 - 2^{15}$

Loss 50/51:
E terms

TERM: 004, 005, 006, 007, 008, 009, 010, 011, 012, 013, 014, 015

TP: 004', 003', 010', 025', 050', 052', 068', 061', 050', 057', 006', 008'

Block length

TERM: 024, 025, 026, 027, 028, 029, 030, 031, 032, 033

TP: 001, 005, 002, 007, 053, 051, 071, 053, 069, 001

FO4 - FIS → R28 - R39

* HINT - The 2BC use same terms for 20s A 50/51 as Buffer memory (DMA3)
For Address I/O

C

C

C

Grp of data

TERM: H0, H1, H2, H3, H4, H5, H6, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16
H17

IP: B19, B32, B36, B38, A47, A50, A44, A44, 015, 014, 017, 020, C68, C67, C64, C63, C51
C50

TERM: J0, J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17

IP: B10, B12, B16, B18, A62, A65, A55, A57, 001, 002, 004, 003, C53, C54, C57, C62, A38, A3C

J18, J19
A42, A35

TERM: K0, K1, K2, K3, K4, K5, K6, K7, K8, K9, K10, K11, K12, K13, K14, K15, K16, K17, K18, K19

B13, B20, B31, B35, A64, A57, A48, A40, 005, 008, 009, 010, C49, C61, C60, C59, B46, B43, B42, B44

R0-219 → 2YB

2NW:

2BU → 2NW
RØØ-17 → AØ-A17

Proc AØ:

TERM:

AØ, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17

TP:

B70', B63', B68', B50', A12', A16', A10', A25', A29', Ø72', Ø52', Ø10', Ø14', C28', C32', C34', C33', C38

PROC A1:

TERM:

BØ, B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17.

TP:

B69', B58', B61', B52', AØ9', A14', AØ3', A19', A27', Ø67', Ø48', Ø38', Ø46', Ø39', C42', C45', C25', C41'

Proc A3:

TERM:

DØ, Ø1, Ø2, Ø3, Ø4, Ø5, Ø6, Ø7, Ø8, Ø9, Ø10, Ø11, Ø12, Ø13, Ø14, Ø15, Ø16, Ø17

TP:

B72', B65', B55', B59', A1', A5', A18', A2Ø, A24', Ø70', Ø55', Ø50', Ø31', C19', C27', CØ8, C33, C3Ø'

Group Ø = EØ - E17

BUTTER Memory Write - Data

Hint 1 make sure loop 5051 are working because they use same DMA port. out of the 2B2 -> 2BU

2BU Even Buffer

TERM: C00, C01, C02, C03, C04, C05, C06, C07, C08, C09, C10, C11, C12, C13, C14, C15, C16, C17

IP: C08', C06', C03', C04', C23', C28', C14', C10', C31', C33', C29', C17', C44', C42', C40', C38', C57', C59'

ODD Buffer

TERM: C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37

IP: D70', D69', D71', D72', D61', D66', D68', D67', D65', D63', D65', D64', D55', D57', D59', D60', D58', D46'

E00 - 17 Even Buffer
E20 - 37 odd Buffer

TERM: R00, R01, R02, R03, R04, R05, R06, R07, R08, R09, R10, R11, R12, R13, R14, R15, R16, R17

IP: C69, C72, C70, C67, C71, C68', C68, C66, C65', D02, D04', D03, D10, D28, D01, D32, D19', D21'

Map showing the destination of a block of words in the SSD module for a 32 Mword SSD.

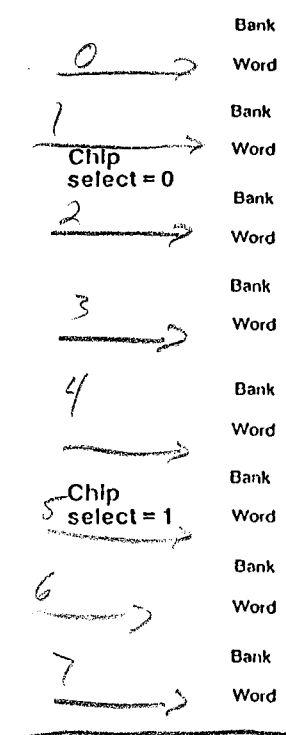
		Section															
		0			1			2			3						
Chip select = 0	Bank	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
	Word	0	2	4	6												
	Bank	4	5	6	7	4	5	6	7	4	5	6	7	4	5	6	7
	Word	20	22	24	26												
Chip select = 1	Bank	10	11	12	13	10	11	12	13	10	11	12	13	10	11	12	13
	Word	40	42	44	46												
	Bank	14	15	16	17	14	15	16	17	14	15	16	17	14	15	16	17
	Word	60	62	64	66												
		Group 0															
Chip select = 0	Bank	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
	Word	1	3	5	7												
	Bank	4	5	6	7	4	5	6	7	4	5	6	7	4	5	6	7
	Word	21	23	25	27												
Chip select = 1	Bank	10	11	12	13	10	11	12	13	10	11	12	13	10	11	12	13
	Word	41	43	45	47												
	Bank	14	15	16	17	14	15	16	17	14	15	16	17	14	15	16	17
	Word	61	63	65	67												
		Group 1															
Chip select = 0	Bank	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
	Word	10	12	14	16												
	Bank	4	5	6	7	4	5	6	7	4	5	6	7	4	5	6	7
	Word	30	32	34	36												
Chip select = 1	Bank	10	11	12	13	10	11	12	13	10	11	12	13	10	11	12	13
	Word	50	52	54	56												
	Bank	14	15	16	17	14	15	16	17	14	15	16	17	14	15	16	17
	Word	70	72	74	76												
		Group 2															
Chip select = 0	Bank	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
	Word	11	13	15	17												
	Bank	4	5	6	7	4	5	6	7	4	5	6	7	4	5	6	7
	Word	31	33	35	37												
Chip select = 1	Bank	10	11	12	13	10	11	12	13	10	11	12	13	10	11	12	13
	Word	51	53	55	57												
	Bank	14	15	16	17	14	15	16	17	14	15	16	17	14	15	16	17
	Word	71	73	75	77												
		Group 3															

Map showing the destination of a block of words in the SSD module for a 128 Mword SSD.

Section

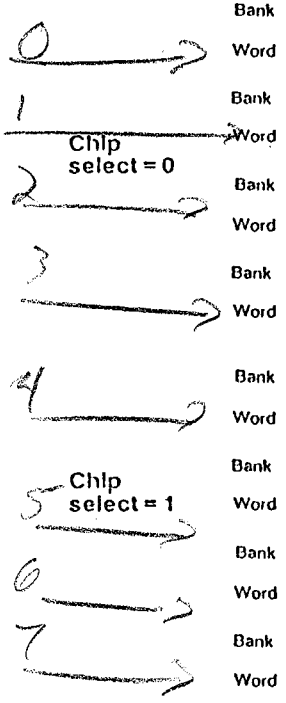
0 1 2 3

Assume
Starting
At Addr.
0



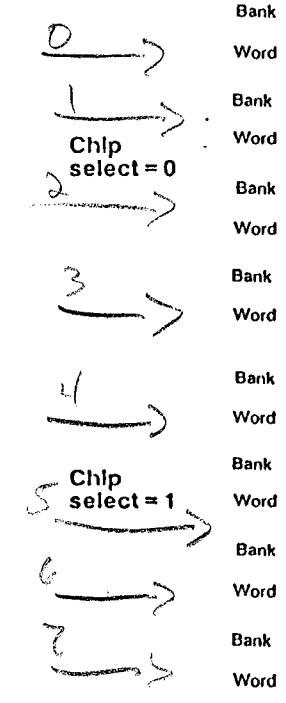
Bank	0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
Word	0 2 4 6	10 12 14 16	20 22 24 26	30 32 34 36
Bank	4 5 6 7	4 5 6 7	4 5 6 7	4 5 6 7
Word	40 42 44 46	50 52 54 56	60 62 64 66	70 72 74 76
Bank	10 11 12 13	10 11 12 13	10 11 12 13	10 11 12 13
Word				
Bank	14 15 16 17	14 15 16 17	14 15 16 17	14 15 16 17
Word				

Group 0



Bank	0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
Word	1 3 5 7	11 13 15 17	21 23 25 27	31 33 35 37
Bank	4 5 6 7	4 5 6 7	4 5 6 7	4 5 6 7
Word	41 43 45 47	51 53 55 57	61 63 65 67	71 73 75 77
Bank	10 11 12 13	10 11 12 13	10 11 12 13	10 11 12 13
Word				
Bank	14 15 16 17	14 15 16 17	14 15 16 17	14 15 16 17
Word				

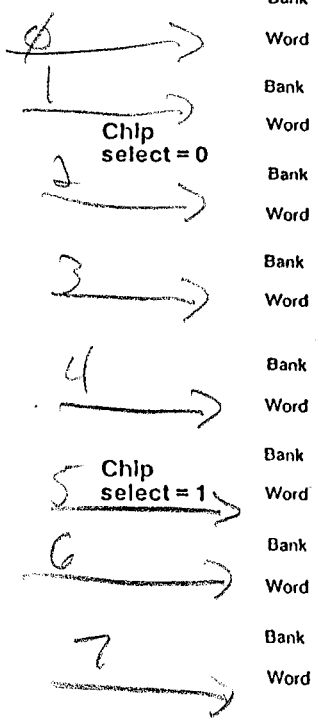
Group 1



Bank	0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
Word				
Bank	4 5 6 7	4 5 6 7	4 5 6 7	4 5 6 7
Word				
Bank	10 11 12 13	10 11 12 13	10 11 12 13	10 11 12 13
Word				
Bank	14 15 16 17	14 15 16 17	14 15 16 17	14 15 16 17
Word				

Group 2

(RAS lines)



Bank	0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
Word				
Bank	4 5 6 7	4 5 6 7	4 5 6 7	4 5 6 7
Word				
Bank	10 11 12 13	10 11 12 13	10 11 12 13	10 11 12 13
Word				
Bank	14 15 16 17	14 15 16 17	14 15 16 17	14 15 16 17
Word				

Group 3

Map showing the destination of a block of words in the SSD module for a 64 Mword SSD.

		Section			
		0	1	2	3
Chlp select = 0	Bank	0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
	Word	0 2 4 6	10 12 14 16		
	Bank	4 5 6 7	4 5 6 7	4 5 6 7	4 5 6 7
	Word	20 22 24 26	30 32 34 36		
Chlp select = 1	Bank	10 11 12 13	10 11 12 13	10 11 12 13	10 11 12 13
	Word	40 42 44 46	50 52 54 56		
	Bank	14 15 16 17	14 15 16 17	14 15 16 17	14 15 16 17
	Word	60 62 64 66	70 72 74 76		
Chlp select = 0	Bank	0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
	Word				
	Bank	4 5 6 7	4 5 6 7	4 5 6 7	4 5 6 7
	Word				
Chlp select = 1	Bank	10 11 12 13	10 11 12 13	10 11 12 13	10 11 12 13
	Word				
	Bank	14 15 16 17	14 15 16 17	14 15 16 17	14 15 16 17
	Word				
Chlp select = 0	Bank	0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
	Word	1 3 5 7	11 13 15 17		
	Bank	4 5 6 7	4 5 6 7	4 5 6 7	4 5 6 7
	Word	21 23 25 27	31 33 35 37		
Chlp select = 1	Bank	10 11 12 13	10 11 12 13	10 11 12 13	10 11 12 13
	Word	41 43 45 47	51 53 55 57		
	Bank	14 15 16 17	14 15 16 17	14 15 16 17	14 15 16 17
	Word	61 63 65 67	71 73 75 77		
Chlp select = 0	Bank	0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
	Word				
	Bank	4 5 6 7	4 5 6 7	4 5 6 7	4 5 6 7
	Word				
Chlp select = 1	Bank	10 11 12 13	10 11 12 13	10 11 12 13	10 11 12 13
	Word				
	Bank	14 15 16 17	14 15 16 17	14 15 16 17	14 15 16 17
	Word				
Chlp select = 0	Bank	0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
	Word				
	Bank	4 5 6 7	4 5 6 7	4 5 6 7	4 5 6 7
	Word				
Chlp select = 1	Bank	10 11 12 13	10 11 12 13	10 11 12 13	10 11 12 13
	Word				
	Bank	14 15 16 17	14 15 16 17	14 15 16 17	14 15 16 17
	Word				
Chlp select = 0	Bank	0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
	Word				
	Bank	4 5 6 7	4 5 6 7	4 5 6 7	4 5 6 7
	Word				
Chlp select = 1	Bank	10 11 12 13	10 11 12 13	10 11 12 13	10 11 12 13
	Word				
	Bank	14 15 16 17	14 15 16 17	14 15 16 17	14 15 16 17
	Word				

*Error boeger
Banks*

SSD MODEL C

	A	B	C	D		
71		2YB	00-03	2YB	2YB	47
70		2YB	04-07	2YB	2YB	46
68		2YB	08-11	2YB	2YB	45
66		2YB	12-15	2YB	2YB	44
64		2YB	16-19	2YB	2YB	43
		GROUP 0	20-23	2YB	2YB	42
62		2YB	24-27	2YB	2YB	41
60		2YB	28-31	2YB	2YB	40
58		2YB	32-35	2YB	2YB	39
56		2YB	36-39	2YB	2YB	38
54		2YB	40-43	2YB	2YB	37
		SECTION 0	44-47	2YB	2YB	36
37		2YB	48-51	2YB	2YB	35
36		2YB	52-55	2YB	2YB	34
35		2YB	56-59	2YB	2YB	33
34		2YB	60-63	2YB	2YB	32
33		2YB	64-67	2YB	2YB	31
32		2YB	68-71	2YB	2YB	30
31		2YB	72-75	2YB	2YB	29
30		2YB	76-79	2YB	2YB	28
29		2YB	80-83	2YB	2YB	27
28		2YB	84-87	2YB	2YB	26
27		2YB	88-91	2YB	2YB	25
26		2YB	92-95	2YB	2YB	24
25		2YB	96-99	2YB	2YB	23
24		2YB	100-103	2YB	2YB	22
23		2YB	104-107	2YB	2YB	21
22		2YB	108-111	2YB	2YB	20
21		2YB	112-115	2YB	2YB	19
20		2YB	116-119	2YB	2YB	18
19		2YB	120-123	2YB	2YB	17
18		2YB	124-127	2YB	2YB	16
17		2YB	128-131	2YB	2YB	15
16		2YB	132-135	2YB	2YB	14
15		2YB	136-139	2YB	2YB	13
14		2YB	140-143	2YB	2YB	12
13		2YB	144-147	2YB	2YB	11
12		2YB	148-151	2YB	2YB	10
11		2YB	152-155	2YB	2YB	9
10		2YB	156-159	2YB	2YB	8
9		2YB	160-163	2YB	2YB	7
8		2YB	164-167	2YB	2YB	6
7		2YB	168-171	2YB	2YB	5
6		2YB	172-175	2YB	2YB	4
5		2YB	176-179	2YB	2YB	3
4		2YB	180-183	2YB	2YB	2
3		2YB	184-187	2YB	2YB	1
2		2YB	188-191	2YB	2YB	0
1		2YB	192-195	2YB	2YB	0
0		2YB	196-199	2YB	2YB	0
0		2YB	200-203	2YB	2YB	1
1		2YB	204-207	2YB	2YB	2
2		2YB	208-211	2YB	2YB	3
3		2YB	212-215	2YB	2YB	4
4		2YB	216-219	2YB	2YB	5
5		2YB	220-223	2YB	2YB	6
6		2YB	224-227	2YB	2YB	7
7		2YB	228-231	2YB	2YB	8
8		2YB	232-235	2YB	2YB	9
9		2YB	236-239	2YB	2YB	10
10		2YB	240-243	2YB	2YB	11
11		2YB	244-247	2YB	2YB	12
12		2YB	248-251	2YB	2YB	13
13		2YB	252-255	2YB	2YB	14
14		2YB	256-259	2YB	2YB	15
15		2YB	260-263	2YB	2YB	16
16		2YB	264-267	2YB	2YB	17
17		2YB	268-271	2YB	2YB	18
18		2YB	272-275	2YB	2YB	19
19		2YB	276-279	2YB	2YB	20
20		2YB	280-283	2YB	2YB	21
21		2YB	284-287	2YB	2YB	22
22		2YB	288-291	2YB	2YB	23
23		2YB	292-295	2YB	2YB	24
24		2YB	296-299	2YB	2YB	25
25		2YB	300-303	2YB	2YB	26
26		2YB	304-307	2YB	2YB	27
27		2YB	308-311	2YB	2YB	28
28		2YB	312-315	2YB	2YB	29
29		2YB	316-319	2YB	2YB	30
30		2YB	320-323	2YB	2YB	31
31		2YB	324-327	2YB	2YB	32
32		2YB	328-331	2YB	2YB	33
33		2YB	332-335	2YB	2YB	34
34		2YB	336-339	2YB	2YB	35
35		2YB	340-343	2YB	2YB	36
36		2YB	344-347	2YB	2YB	37
37		2YB	348-351	2YB	2YB	38
38		2YB	352-355	2YB	2YB	39
39		2YB	356-359	2YB	2YB	40
40		2YB	360-363	2YB	2YB	41
41		2YB	364-367	2YB	2YB	42
42		2YB	368-371	2YB	2YB	43
43		2YB	372-375	2YB	2YB	44
44		2YB	376-379	2YB	2YB	45
45		2YB	380-383	2YB	2YB	46
46		2YB	384-387	2YB	2YB	47
47		2YB	388-391	2YB	2YB	48

Part 1

KMP Channel

KMP Channel -> Part 2

*Group
Part
c/1*

*Group
part*

2/3

Part 2

IOP MODEL C S/N 101

HTV-0699

15-30

	A	B	C	D	
72	2YH ERROR LOG	2YI MAINTENANCE DATA	2YB-5 00-03	2YB-5 00-03	49
71	2YJ MAINTENANCE CONTROL	3TO-1 1ST CLOCK	2YB-5 04-07	2YB-5 04-07	48
69					
68	2YP 00-07	3TC-1 2ND CLOCK	2YB-5 08-11	2YB-5 08-11	47
67					
66		2YF GROUP 0 WRITE	2YB-5 12-15	2YB-5 12-15	46
65	HISP BUFFER	2YF GROUP 0 READ SECDED	2YB-5 16-19	2YB-5 16-19	45
64					
63		2YF GROUP 1 WRITE	2YB-5 20-23	2YB-5 20-23	44
62					
61					
60	2YP 32-39	2YF GROUP 1 READ	2YB-5 24-27	2YB-5 24-27	43
59					
58	2YO HISP ADDRESS/BL	2YG GROUP CONTROL	2YB-5 28-31	2YB-5 28-31	42
57					
56	2YP 40-47	2YM ADDRESS	2YB-5 32-35	2YB-5 32-35	41
55					
54	HISP BUFFER	2YK MAIN CONTROL	2YB-5 36-39	2YB-5 36-39	40
53					
52					
51	2YP 50-57		2YB-5 40-43	2YB-5 40-43	39
50					
49	2YR HISP CONTROL	DATA FANIN FANOUT	2YB-5 44-47	2YB-5 44-47	38
48					
47					
46	2YZ 00-23		2YB-5 48-51	2YB-5 48-51	37
45					
44					
43	VHISP DATA		2YB-5 52-55	2YB-5 52-55	36
42					
41					
40					
39		2NR BUFFER MEMORY PRO 0,1 SEC 0,2	2YB-5 56-59	2YB-5 56-59	35
38					
37		2NR READ DATA PRO 2,3 SEC 1,3	2YB-5 60-63	2YB-5 60-63	34
36	2YZ 48-71		2YB-5 64-67	2YB-5 64-67	33
35					
34	2YY VHISP CONTROL		2YB-5 68-71	2YB-5 68-71	32
33					
32					
31	2IK LOSP4 OUTPUT	2NC CONTROL	2YB-5 00-03	2YB-5 00-03	31
30					
29	2IL LOSP4 ACCUMULATOR	2NX XOVER 0,1 2,3	2YB-5 04-07	2YB-5 04-07	30
28					
27	2II LOSP4 CONTROL	2BWO SEC 0 0-7 LOCAL	2YB-5 08-11	2YB-5 08-11	29
26					
25	2IJ LOSP4 INPUT	2BWI SEC 1 0-7	2YB-5 12-15	2YB-5 12-15	28
24					
23	2IS HISP INPUT	2BW2 SEC 2 0-7 MEMORY	2YB-5 16-19	2YB-5 16-19	27
22					
21	2IR HISP OUTPUT	2BWS SEC 3 0-7	2YB-5 20-23	2YB-5 20-23	26
20					
19	2BWO SEC 0 0-7 LOCAL	2BR ACCUMULATOR REGISTERS ODD	2YB-5 24-27	2YB-5 24-27	25
18					
17	2BWI SEC 1 0-7	2BR ADDER	2YB-5 28-31	2YB-5 28-31	24
16					
15	2BW2 SEC 2 0-7 MEMORY	2BI INSTRUCTION STACK	2YB-5 32-35	2YB-5 32-35	23
14	2BW3 SEC 3 0-7	2BT ISSUE CONTROL	2YB-5 36-39	2YB-5 36-39	22
13					
12	2BR EVEN BITS	2BN LOCAL MEMORY CONTROL	2YB-5 40-43	2YB-5 40-43	21
11	2BR ACCUMULATOR REGISTERS ODD BITS	2BW4 SEC 0 8-15 LOCAL	2YB-5 44-47	2YB-5 44-47	20
10					
9	2BA ADDER	2BW5 SEC 1 8-15	2YB-5 48-51	2YB-5 48-51	19
8					
7	2BI INSTRUCTION STACK	2BW6 SEC 2 8-15 MEMORY	2YB-5 52-55	2YB-5 52-55	18
6					
5	2BT ISSUE CONTROL	2BW7 SEC 3 8-15	2YB-5 56-59	2YB-5 56-59	17
4					
3	2BN LOCAL MEMORY CONTROL		2YB-5 60-63	2YB-5 60-63	16
2					
1					
0					
0	2BW4 SEC 0 LOCAL	2BB I/O ADDRESS	2YB-5 64-67	2YB-5 64-67	15
1	2BW5 SEC 1 8-15	2BH EXIT STACK	2YB-5 68-71	2YB-5 68-71	14
2					
3	2BW6 SEC 2 8-15 MEMORY	2BK HSP LOSP MOS CONTROL	2YB-5 72-75	2YB-5 72-75	13
4	2BW7 SEC 3 8-15	2BL ADDRESS, BL REGISTERS	2YB-5 76-79	2YB-5 76-79	12
5					
6	2BB I/O ADDRESS	2BM CONSOLE I/O INTERRUPTS	2YB-5 80-83	2YB-5 80-83	11
7					
8	2BH EXIT STACK	2BP HISP OUTPUT LOSP MOS INP	2YB-5 84-87	2YB-5 84-87	10
9					
10	2BK HSP LOS MOS CONTROL	2BQ HISP INPUT SECDED	2YB-5 88-91	2YB-5 88-91	9
11					
12	2BL ADDRESS, BL REGISTERS	2BU HISP BYPASS LOSP MOS OUT	2YB-5 92-95	2YB-5 92-95	8
13					
14	2BM CONSOLE I/O INTERRUPTS	2IH DMA0 EXPANDER INTR.	2YB-5 96-99	2YB-5 96-99	7
15					
16	2BP HISP OUTPUT LOSP MOS INP	2IJ DMA1 LSP4	2YB-5 100-103	2YB-5 100-103	6
17	2BQ HISP INPUT SECDED	2IK DMA2 INPUT	2YB-5 104-107	2YB-5 104-107	5
18					
19	2BU HISP BYPASS LOSP MOS OUT	2II DMA1 LSP4	2YB-5 108-111	2YB-5 108-111	4
20					
21	2PK DMA0 BMC4	2II DMA2 CONTROL	2YB-5 112-115	2YB-5 112-115	3
22	2PK DMA1 DATA	2IL DMA1 LSP4	2YB-5 116-119	2YB-5 116-119	2
23	2PK DMA2	2IL DMA2 ACCUMULATOR	2YB-5 120-123	2YB-5 120-123	1
24					
25	2PJ DMA0 BMC4	2IK DMA1 LSP4	2YB-5 124-127	2YB-5 124-127	0
26	2PJ DMA1 CONTROL	2IK DMA2 OUTPUT	2YB-5 128-131	2YB-5 128-131	0
27	2PJ DMA2	2IX ERROR MULTIPLEX	2YB-5 132-135	2YB-5 132-135	0
28					
29	2PT DMA0 CH 20 BMC4	3TC-1 2ND CLOCK	2YB-5 136-139	2YB-5 136-139	0
30	2PI DMA0 CH 21	3TO-2 1ST CLOCK	2YB-5 140-143	2YB-5 140-143	0
31	2PI DMA0 CH 22 CHANNEL	2BV DEADSTART / MASTER CLR	2YB-5 144-147	2YB-5 144-147	0
32	2PI DMA0 CH 23		2YB-5 148-151	2YB-5 148-151	0
33					
34	2PI DMA1 CH 24 BMC4	2IE DMA0 CH 20 DCU5	2YB-5 152-155	2YB-5 152-155	0
35	2PI DMA1 CH 25	2IE DMA0 CH 21	2YB-5 156-159	2YB-5 156-159	0
36	2PI DMA1 CH 26 CHANNEL	2IE DMA0 CH 22 INTERFACE	2YB-5 160-163	2YB-5 160-163	0
37	2PI DMA1 CH 27	2IE DMA0 CH 23	2YB-5 164-167	2YB-5 164-167	0
38					
39	2PI DMA2 CH 30 BMC4	2IE DMA1 CH 24 DCU5	2YB-5 168-171	2YB-5 168-171	0
40	2PI DMA2 CH 31	2IE DMA1 CH 25	2YB-5 172-175	2YB-5 172-175	0
41	2PI DMA2 CH 32 CHANNEL	2IE DMA1 CH 26 INTERFACE	2YB-5 176-179	2YB-5 176-179	0
42	2PI DMA2 CH 33	2IE DMA1 CH 27	2YB-5 180-183	2YB-5 180-183	0
43					
44	2PL DMA0 BMC4	2IE DMA2 CH 30 DCU5	2YB-5 184-187	2YB-5 184-187	0
45	2PL DMA0	2IE DMA2 CH 31	2YB-5 188-191	2YB-5 188-191	0
46	2PL DMA1 LEVEL	2IE DMA2 CH 32 INTERFACE	2YB-5 192-195	2YB-5 192-195	0
47	2PL DMA1	2IE DMA2 CH 33	2YB-5 196-199	2YB-5 196-199	0
48					
49	2PL DMA2 TRANS	2IE DMA5 CH 37	2YB-5 200-203	2YB-5 200-203	0
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71					
72	2AZ HSP 6-9 ERR		2AZ HSP 2-5 ERR		72

NOTE: DMA3 PROC LOSP/MOS
DMA4 PROC HISP
HMM-0705

CRAY X-MP/216

C		D		E		F		G		H		I		J	
BANK 28/34	BANK 28/34	1ST LEVEL MULTIPLY	SCALAR REGISTER	VECTOR OPERAND DATA	VECTOR REGISTER	BANK 30/36	BANK 30/36								
BANK 24/30	BANK 24/30	2ND LEVEL MULT. LOWER BITS	SCALAR REGISTER	VECTOR OPERAND DATA	VECTOR REGISTER	BANK 26/32	BANK 26/32								
BANK 20/24	BANK 20/24	2ND LEVEL MULT. CENTER	SCALAR REGISTER	VECTOR OPERAND DATA	VECTOR REGISTER	BANK 22/26	BANK 22/26								
BANK 16/20	BANK 16/20	1ST LEVEL MULT. & EXPNT.	SCALAR REGISTER	VECTOR OPERAND DATA	VECTOR REGISTER	BANK 18/22	BANK 18/22								
ADDRESS	ADDRESS	FINAL LEVEL MULT.	SCALAR REGISTER	VECTOR OPERAND DATA	VECTOR REGISTER	ADDRESS	ADDRESS								
READ DATA	READ DATA	MULT. EXPNT. & CONTROL	SCALAR REGISTER	VECTOR OPERAND DATA	VECTOR REGISTER	READ DATA	READ DATA								
ADDRESS	ADDRESS	FINAL LEVEL MULT. UPPER BITS	SCALAR REGISTER	VECTOR OPERAND DATA	VECTOR REGISTER	ADDRESS	ADDRESS								
BANK 12/14	BANK 12/14	1ST LEVEL MULTIPLY	MEMORY DATA SELECTION	ADDRESS REGISTER	ADDRESS REGISTER	BANK 14/16	BANK 14/16								
BANK 8/10	BANK 8/10	VECTOR LOGICAL	MEMORY DATA SELECTION	ADDRESS REGISTER	ADDRESS REGISTER	BANK 10/12	BANK 10/12								
BANK 4/04	BANK 4/04	FINAL RESULT	MEMORY DATA SELECTION	ADDRESS REGISTER	ADDRESS REGISTER	BANK 6/06	BANK 6/06								
BANK 0/00	BANK 0/00	FINAL SUM A1 SORD X B2	MEMORY DATA SELECTION	ADDRESS REGISTER	ADDRESS REGISTER	BANK 2/02	BANK 2/02								
WRITE DATA	WRITE DATA	FORM A1 SORD X B2 UPPER	MEMORY DATA SELECTION	ADDRESS REGISTER	ADDRESS REGISTER	WRITE DATA	WRITE DATA								
WRITE DATA	WRITE DATA	FORM A1 SORD X B2 LOWER	MEMORY DATA SELECTION	ADDRESS REGISTER	ADDRESS REGISTER	WRITE DATA	WRITE DATA								
BANK 1/01	BANK 1/01	FORM A1 SORD X B2 UPPER	MEMORY DATA SELECTION	ADDRESS REGISTER	ADDRESS REGISTER	BANK 3/03	BANK 3/03								
BANK 5/05	BANK 5/05	FORM A1 SORD X B2 LOWER	MEMORY DATA SELECTION	ADDRESS REGISTER	ADDRESS REGISTER	BANK 7/07	BANK 7/07								
BANK 9/11	BANK 9/11	AI SQUARED X BI	MEMORY DATA SELECTION	ADDRESS REGISTER	ADDRESS REGISTER	BANK 11/13	BANK 11/13								
BANK 13/15	BANK 13/15	FL. RECIP. LOOK-UP TABLE	MEMORY DATA SELECTION	ADDRESS REGISTER	ADDRESS REGISTER	BANK 15/17	BANK 15/17								
ADDRESS	ADDRESS	FORCED 0	MEMORY DATA SELECTION	ADDRESS REGISTER	ADDRESS REGISTER	ADDRESS	ADDRESS								
READ DATA	READ DATA	REAL TIME CLOCK	MEMORY DATA SELECTION	ADDRESS REGISTER	ADDRESS REGISTER	READ DATA	READ DATA								
ADDRESS	ADDRESS	MASTER CLOCK & FANOUT	MEMORY DATA SELECTION	ADDRESS REGISTER	ADDRESS REGISTER	ADDRESS	ADDRESS								
BANK 17/21	BANK 17/21	CLOCK FANOUT	MEMORY DATA SELECTION	ADDRESS REGISTER	ADDRESS REGISTER	BANK 19/23	BANK 19/23								
BANK 21/25	BANK 21/25	REAL TIME CLOCK	MEMORY DATA SELECTION	ADDRESS REGISTER	ADDRESS REGISTER	BANK 23/27	BANK 23/27								
BANK 25/31	BANK 25/31	SHARED REGISTERS	MEMORY DATA SELECTION	ADDRESS REGISTER	ADDRESS REGISTER	BANK 27/33	BANK 27/33								
BANK 29/35	BANK 29/35	INSTRUCTION BUFFER	MEMORY DATA SELECTION	ADDRESS REGISTER	ADDRESS REGISTER	BANK 31/37	BANK 31/37								