CRAY RESEARCH, INC.

655-A Lone Oak Drive, Eagan, MN 55121 • Telephone: (612) 683-3800 FAX: (612) 683-3899

Dear Registrant:

Software Training courses are skills based. Each is designed to help participants acquire the set of skills that is listed in the Software Training Catalog course description. The learning log for a course is a simple tool that allows individuals to set proficiency goals for each skill and then to track progress toward those goals. The learning logs for the courses you are registered for are attached.

We suggest that you review with your supervisor the list of skills addressed in each course from the perspective of the tasks that you perform on the job. Ideally you and your supervisor would agree upon goal levels for each of the skills. This would give you a map of where to best expend time and energy. During each course there will be opportunities to test proficiency in each skill and to track progress on the learning logs for the course. There is also a comprehensive test given at the end of each course to review and reinforce the key concepts introduced.

We look forward to seeing you in Eagan.

Sincerely,

Barbara J. Brunzell

Barbara J. Brunzell
Software Publications and Training Manager

cc: Registrant's supervisor

C R A Y R E S E A R C H, I N C.
Software Training

655 - A Lone Oak Drive
Eagan, Minnesota 55121
(800) 284-2729

To: Ed Barnard (000742)
CRAY RESEARCH, INC.
655-F Lone Oak Drive
Eagan MN 55121
Site: MH

From: June Erickson
Registrar

Date: Mar 07, 1991

Subject: REGISTRATION CONFIRMATION

-

This is to confirm that you have been registered for the following training course(s) on the date(s) indicated below:

Class: I/O Subsystem Operating System Internals - IOS
Class Dates: Mar 11, 1991 through Mar 22, 1991
Class Hours: 8:30-5:00-except 2nd W 2:00pm-11:00pm-2nd Th 2:00pm-11:00p.m.
Night lab: 2nd Wed. (2:00 p.m.-11:00 p.m.) & an optional lab the 2nd Thurs.
Class ends at noon on the 2nd Friday.
Customers must have a signed Cray Research software license for UNICOS and a verified AT&T UNIX System V (release 3.0 or higher) license or specifically licensed for COS.

Unless otherwise noted above, classes will be held at the Software Training Center Building (address above).

If there are any changes necessary, please notify me immediately. All rescheduling must be done no later than (2) weeks prior to the beginning date of each class.

Thank you for your cooperation.

CC: Marti Bancroft
Cray Research, Inc.
655-F Lone Oak Drive
Eagan MN 55121

Rachel Pettit
Cray Research (UK) Ltd.
Cray House, London Road
Bracknell
Berkshire RG12 2SY
ENGLAND

IOS Operating System Internals Class

AGENDA for 1st Week
Mar. 11 - 22, 1991

CHAPTER	TOPIC	PRESENTOR	DATE/DAY/TIME
	Introduction	Leon Vann	3-11/Mon/8:30-11:30
1	Hardware Overview	" "	
2	APML Syntax	" "	
3	APML Pseudos	" "	/1:00-4:30
4	APML Macros	" "	
5	CSIM Testing	Leon Vann	3-12/Tue/8:30-11:30
	Terminal Time	" "	
6	Operating Sys Overview	" "	/1:00-4:30
7	Resources	" "	
	Terminal Time	" "	/4:30-
8	Software Structures	Leon Vann	3-13/Wed/8:30-11:30
10	Overlays	" "	/1:00-3:30
	Terminal Time	" "	/3:30-
9	Inter-IOP Communication	Leon Vann	3-14/Thr/8:30-11:30
11	The Kernel	" "	/1:00-4:00
	Terminal Time	" "	/4:00-
12	Deadstart/Initialization	Leon Vann	3-15/Fri/8:30-11:30
13	IOS Generation	Stuart Johnson	/1:00-4:00
	Terminal Time	Leon Vann	/4:00-

Class Meetings

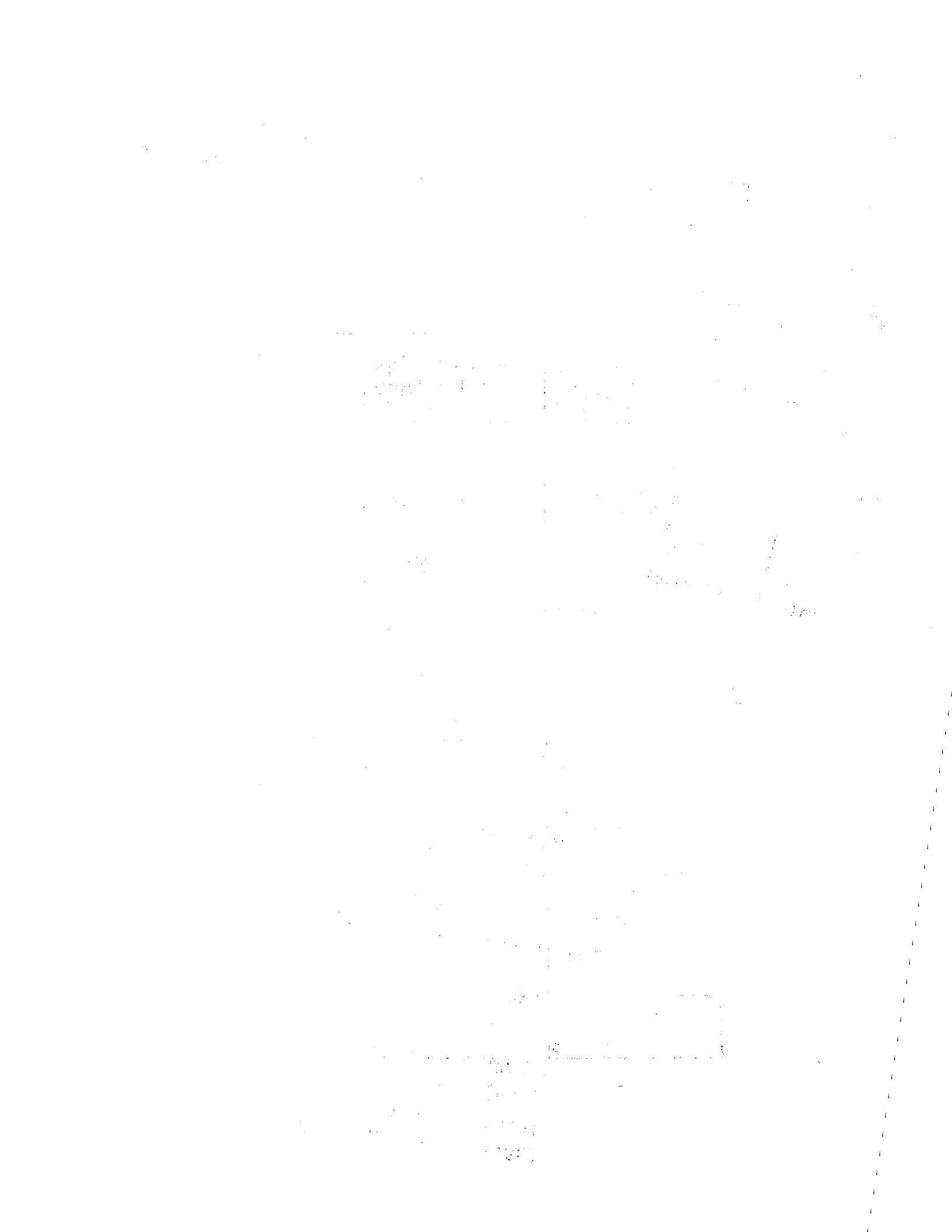
Test & Review	Leon Vann	3:30-4:30/5:30-11:00
Laboratory Lab		
Course Introduction		
Business of Management		

Dedicated Lab Time	Leon Vann	12:00-2:00
New Features (5.0)	Stu Johnson	2:00-3:00
Xcode 5 IDE	Jeff Kopcho	2:00-3:00
Demo Analysis(Grad Only)	Leon Vann	3:30-4:30/5:30-11:30
Dedicated Lab Time		12:00-2:00
Prep Analysis (Demo)		2:00-11:30

IOS Operating System Internals Class

AGENDA for 2nd Week
Mar. 11 - 22, 1990

CHAPTER	TOPIC	PRESENTOR	DATE/DAY/TIME
14	Disks	Leon Vann	3-18/Mon/8:30-11:30
15	Logical Devices	" "	/1:00-2:00
23	Debugging Aids	" "	/2:15-3:00
	Terminal Time	" "	/3:00-
	Front Ends		
16	NSC	Leon Vann	3-19/Tue/8:30-11:30
17	VME	" "	
18	FEI	" "	
19	COMM	" "	
21	User Channel I/O	" "	/1:00-3:00
22	HSX/HIPPI	" "	
	Terminal Time	" "	/3:00-
20	Tapes/BMX	Leon Vann	3-20/Wed/8:30-11:30
24	Dump Analysis(1st Dump)	" "	/1:00-4:30
	Dedicated Lab Time	" "	/17:00-23:00
24	Dump Analysis(2nd Dump)	Leon Vann	3-21/Thr/8:30-11:30
	New Features (7.0)	Stuart Johnson	/1:00-2:00
	Model E IOS	Jeff Koniges	/2:00-3:00
	Dedicated Lab Time	Leon Vann	/17:00-23:00
Class Wrapup			
	Test & Review	Leon Vann	3-22/Fri/8:30-11:00
	Learning Logs		
	Course Evaluation		
	Review by Manager		



To IOS Course Enrollees:

This is a packet of pre-course materials that will aid in preparing you to enter the Cray I/O Subsystem Architecture, APML and Operating System Internals course.

PLEASE try to allow yourself enough pre-course study time so that the exercises in the pre-course workbooks can be COMPLETED PRIOR TO CLASS. We realize that this may not always be possible so we have included a list of priorities. Please consult the priority list below and do AS MUCH of the pre-course work as you have time for.

1) Learning APML using the self-study workbook and the APML manual SM-0036 is of utmost importance. Knowledge of how to read APML is essential in any intimate contact you have with the IOS operating system, since it is written exclusively in APML. PRIOR EXPOSURE TO THE MATERIAL PROVIDED IN THIS PACKET WILL BE ASSUMED OF THOSE IN CLASS, and time will be spent only in reviewing APML, not teaching it "from the beginning".

2) Learning the IOS architecture is vital to understanding why various portions of the operating system are written as they are. Also, a knowledge of the hardware will allow you to understand any programming restraints you may encounter, as well as how to write efficient code. PRIOR EXPOSURE TO THE MATERIAL PROVIDED IN THIS PACKET WILL BE ASSUMED of those in class, and time will be spent only in reviewing the hardware at the block diagram level or higher.

3) Understanding all the material listed on the recommended reading list is vital to filling in any gaps in your knowledge of IOS that may be left even after the classroom lectures and the various exercises you will be asked to work through. The IOS class will not teach everything there is to know about the IOS, but it aims to teach you where you can find anything you need to know. A basic knowledge of the information covered by the reading lists is assumed in class.

If you have questions regarding the course, please call one of us at (612)452-9410. We are looking forward to meeting you.

Sincerely,

Leon F. Vann

Stacy J. Heinrich

IOS Instructors
Software Training

INPUT / OUTPUT SUBSYSTEM PRE-COURSE PACKET

THIS PRE-COURSE PACKET:

...is intended to prepare you to attend the CRAY I/O Subsystem Class.

SKILLS ASSUMED:

Assembler experience (if only from TR-APML Self-Study Workbook)

Ability to use Unix on the Training Pyramid system to enter, edit and submit a program for execution on the Cray (a user guide is available in Mendota Heights.)

A general familiarity with the concepts of dump reading and analysis

A general familiarity with common data structures, such as linked lists, queues, and branch tables

BEFORE COMING TO CLASS:

Read the IOS Architecture Self-Study Workbook and the APML Self-Study Workbook, included in this pre-course packet, and do the exercises at the end of each chapter. This should require approximately twelve to sixteen hours of work. In class, this information will be reviewed only.

Read or review the items on the Recommended Reading List (enclosed).

IF CONVENIENT, PLEASE BRING TO CLASS (IOS 5.0 versions!):

SM-0036	APML Reference Manual
SQ-0059	APML Reference For COS and UNICOS (Card)
SG-0051 -or- SG-2005	IOS Operator's Guide For {COS|UNICOS}
HR-0081	IOS Model C Hardware Reference Manual
CSM-1009-0000	IOS Models C/D System Programmer Reference
TR-IA	IOS Architecture Self-Study Workbook
TR-APML	APML Self-Study Workbook

IF YOU HAVE QUESTIONS:

Call Leon Vann or Stacy Heinrich, IOS Instructors, at (612) 683-3800

INPUT / OUTPUT SUBSYSTEM PRE-COURSE PACKET

ENCLOSURES:

TR-IA	IOS Architecture Self-Study Workbook
TR-APML	APML Self-Study Workbook
SM-0036	APML Reference Manual
SQ-0059	APML Reference For COS and UNICOS (Card)

Course Daily Schedule
Learning Log
Recommended Reading List Summary

DAILY SCHEDULE

MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY
Architecture Overview	Terminal Time	Resources Structures	Overlays	System Generation
APML Overview including Macros and Pseudos CSIM	IOS Overview	Inter-IOP Communication	The Kernel Initialization	Work Time

MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY
Subsystems	Subsystems IOS Development	9:00 AM Subsystems Terminal Time	10:00 AM Dump Analysis	History Trace Test & Review Evaluation
Terminal Time	Terminal Time	Debug Aids Dump Analysis		
		Dedicated Lab **4pm-10pm**	Dedicated Lab (if needed) **4pm-10pm**	9/8/89

Student Learning Log

I/O Subsystem Operating System Internals

IOS

Participant Name:_____

Supervisor Name:_____

Region/Country/Division:_____

Class Start Date:_____

Instructor Name:_____

Competency Levels
0 No experience and knowledge
1 Needs help with all parts of the task
2 Can do parts of a task requiring the skill
3 Can do the task with periodic assistance
*4 Needs no assistance
5 No assistance, fast and accurate
6 No assistance, fast and accurate under pressure
7 No assistance, can lead others

Skills - At the end of the course the learner is able to:									
Read APML source code, and interpret IOP machine code									
Write APML source code									
Code Kernel Service Request functions									
Test APML code using CSIM									
Write an IOS overlay and test using CSIM and dedicated lab time									
List each software subsystem, its functions and main components									
List resources available to help configure an IOS									
Use system generation utilities and procedures to build IOS binaries									
Deadstart and operate the IOS									
Use IOS utilities to aid in problem resolution									
Use IOS debugger to debug an overlay									
Locate important tables and resident overlays in an IOS dump									
Locate, in dump and listings, the $PUNTIF that stopped the system									
Interpret IOS dump trace entries to determine why the system failed									
Competency Levels	0	1	2	3	*4	5	6	7	N/A

This learning log is intended as an aid to the learner in establishing goals and plotting progress. It is not intended as an indicator of job performance and therefore should not be used in determining future job actions.

* Maximum level discernible by the instructor in an instructional environment.

UNICOS Recommended Reading List

SR-2022 **UNICOS ADMINISTRATOR COMMANDS REFERENCE**

adstape
bind
fdmp
make

SG-2059A **CSIM USER'S GUIDE FOR UNICOS**

Section 1.2: Starting CSIM
Section 2.1: Interactive Hardware Definition
Section 4.2: Running a Simulated System
Section 5.7: Stopping the Simulation
Section 7: Miscellaneous Directives
Appendix D.2: IOS Simulation Example - Booting from the Expander
-or-
Appendix D.3: Sample VME Simulation

SG-2005D **IOS OPERATOR'S GUIDE FOR UNICOS**

Appendix B: Startup Procedure
Appendix C: IOS File Editor (to edit startup parameter file)
Appendix D: IOS Dump Programs

SM-0042G **FRONT-END PROTOCOL INTERNAL REFERENCE**

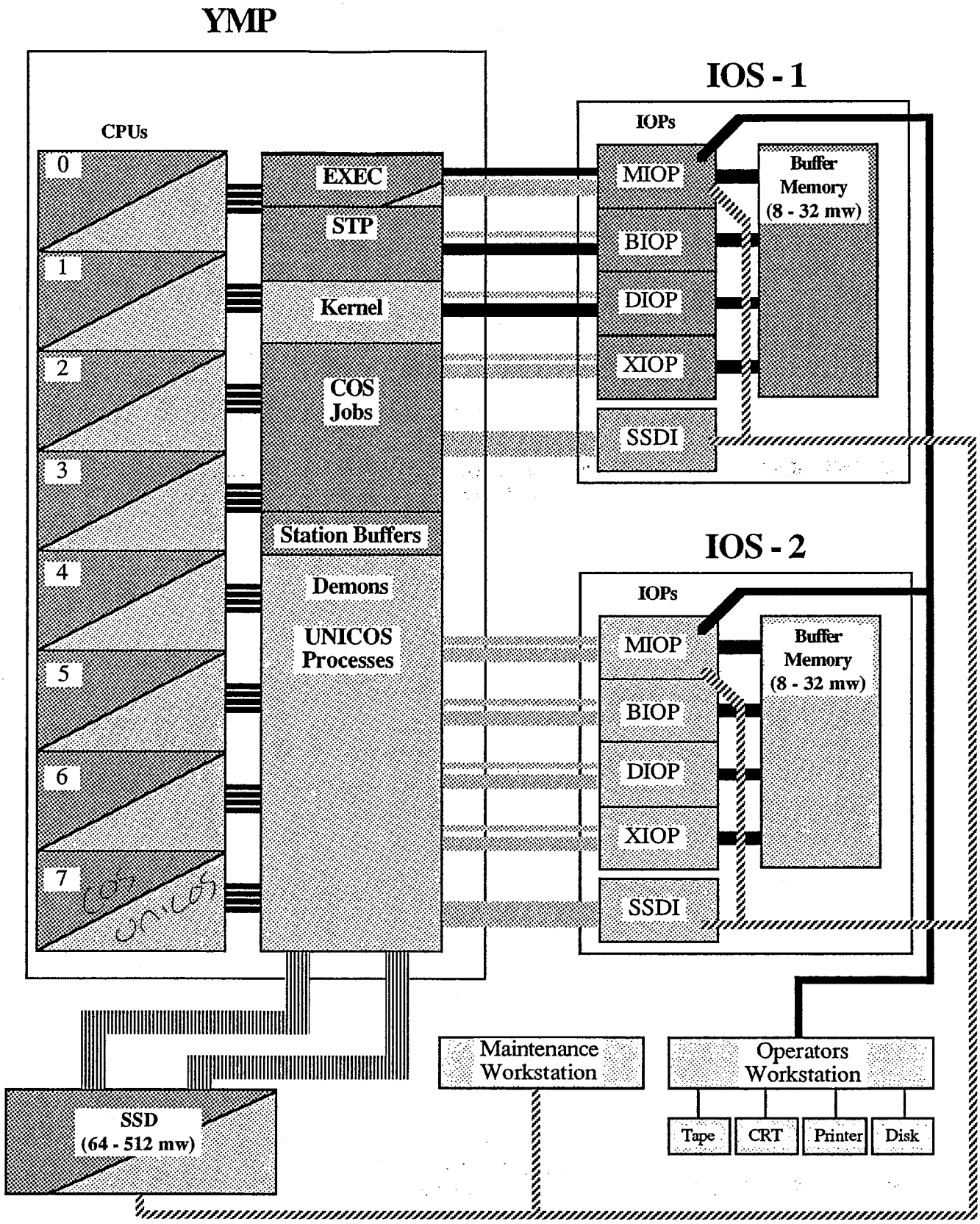
Section 1: Introduction
Section 2: General Concepts

SG-0307A **IOS ADMINISTRATOR'S GUIDE**

Section 1.2: Generation Procedures Under UNICOS
Section 2: IOS System Configuration
Section 4.1: History Trace
Section 4.2: Debugger
Appendix A: IOS Installation Parameters

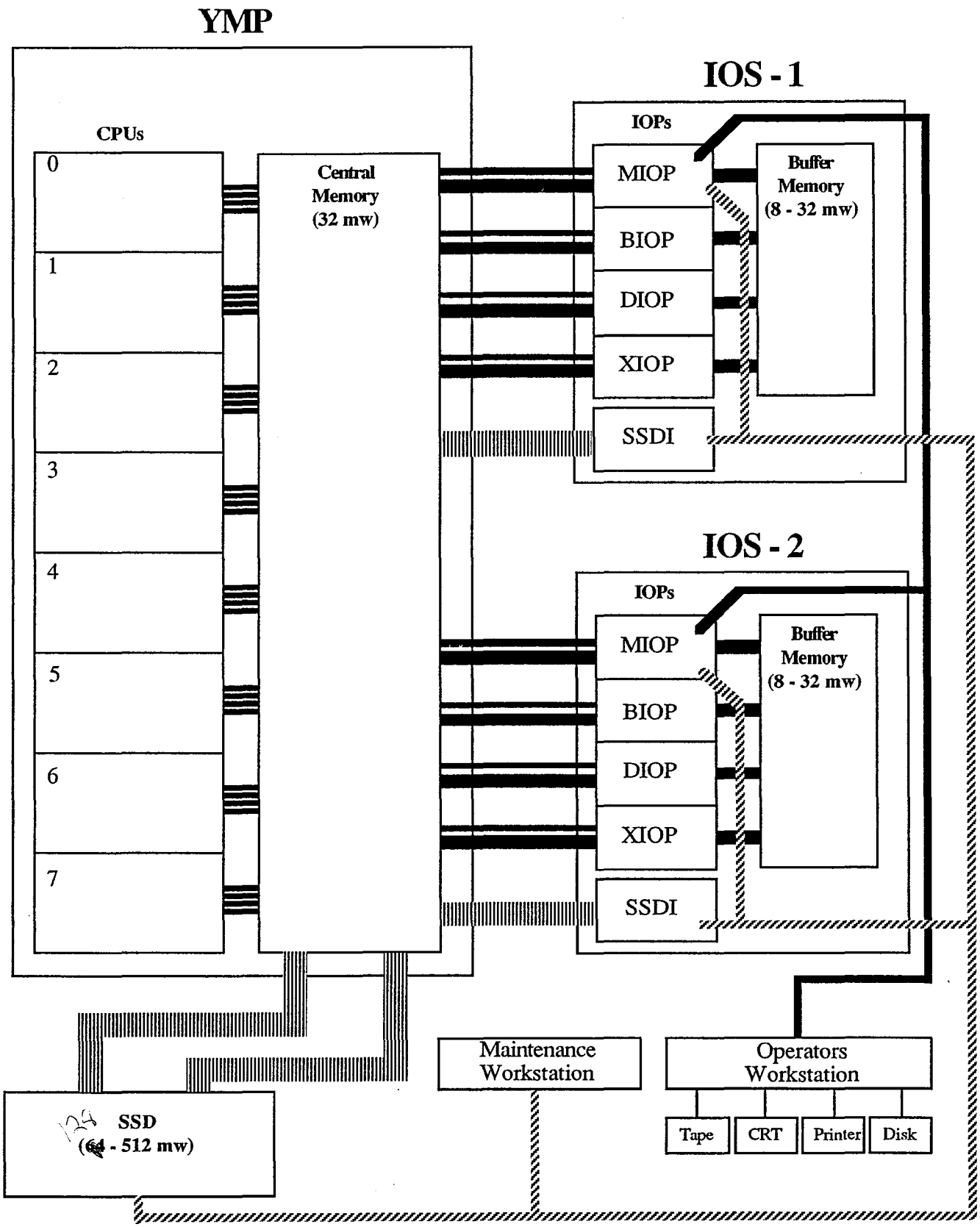
1.17 COS
4.0 UNICOS

Y-MP 8 32 - GOS



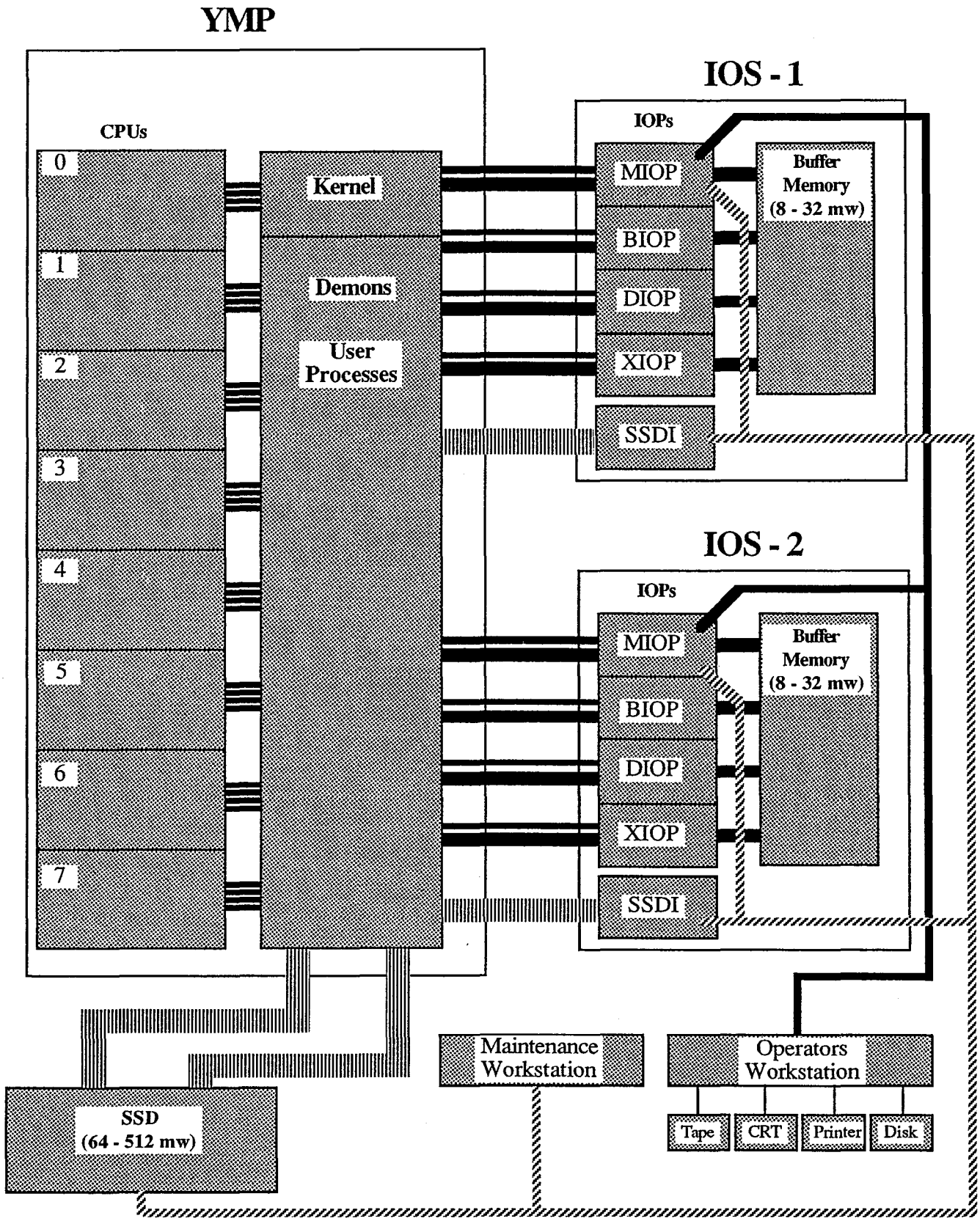
Cray Proprietary

Y-MP 8 32



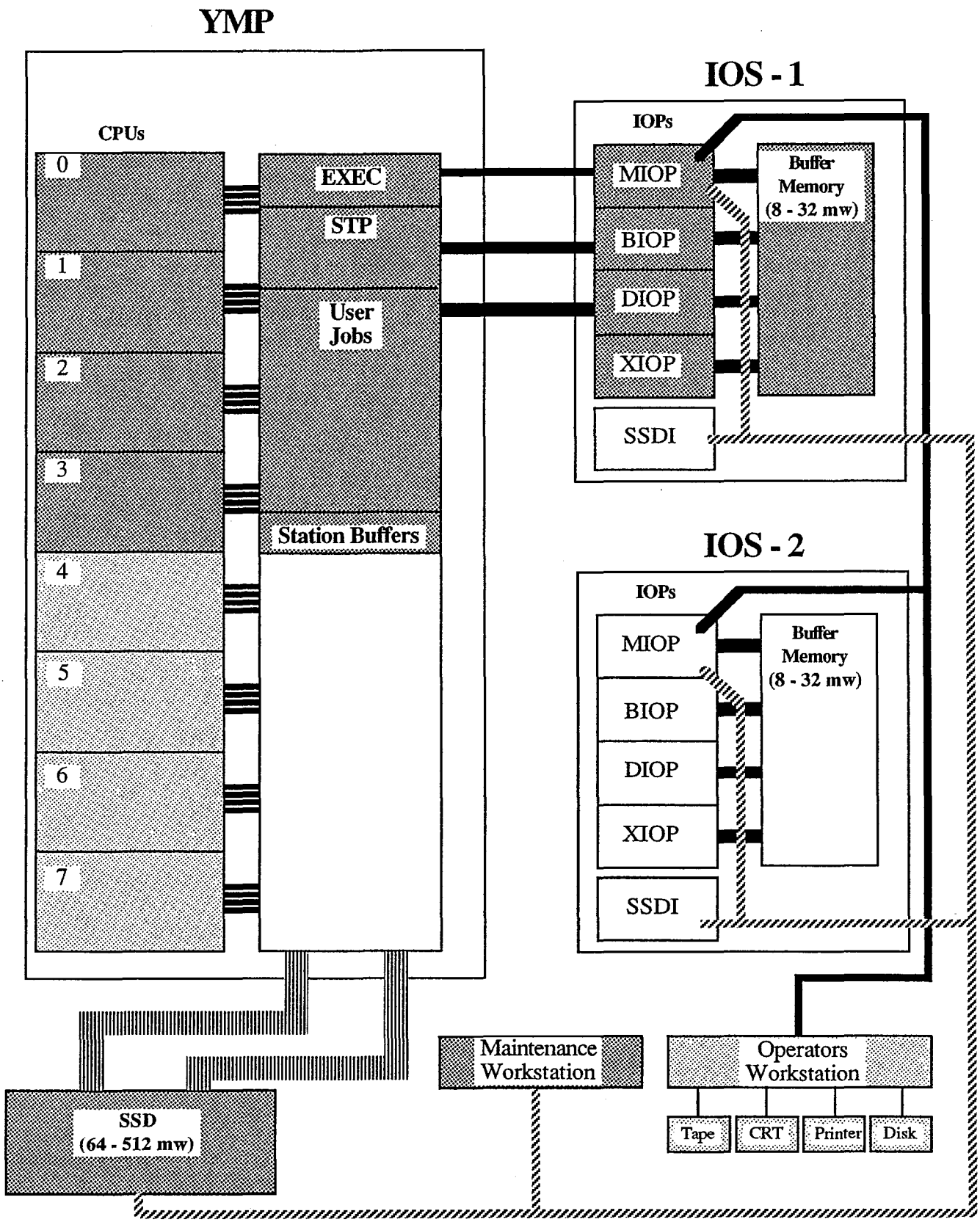
Cray Proprietary

Y-MP 8 32 - UNICOS



Cray Proprietary

Y-MP 8 32 - COS



Cray Proprietary

CRAY Y-MP Course Outline

Monday -	8:30 -	Introduction
	8:45 -	Physical description of Hardware
	9:45 -	The new technology.
	10:45 -	Description of Memory
	1 p.m. -	Exchange Process
	2:15 -	Instruction Fetch
	3:30 -	Instruction Issue
Tuesday -	8:30 -	Shared Registers
	9:30 -	Functional units and Computational registers
	1 p.m. -	Software Overview
Wednesday -	8:30 -	Y-MP Instruction set
	9:30 -	The assembler and new instructions

Jane Norman - instructor

Kevin Stenhagen

CLASS ROSTER

Course YCAL Date 2-8-88 Instructor Jane Norman

We will have a class roster typed up with local and "permanent" address for your use. Please include only those addresses that you want to share with the rest of the class.

NAME As you want it to appear on the certificate (in parenthesis the name you want to be referred to by)	Local Address and phone #	Permanent or work address and phone number
Koushik Ghosh	681-3688	CRI 1333 Northland Dr., MH
Karl Feind	681-3034	CRI 1440 Northland Dr, MH
Steve Tucker	681-3327	CRI 1440 Northland Dr., MH
Melissa Mason	681-3185	CRI 1440 Northland Dr., MH
James Kruchowski	542-2000	CRI - Chippewa Falls, WI 715-726-1211
Jack Thompson	681-3118	1440 Northland Dr., MH
Steve Brown	681-5722	1345 Northland Dr., MH
Jim Kohn	681-5623	1345 Northland Dr., MH
Rich Klamann	Holiday Inn	LANL Mail B296 Los Alamos, NM 87544
Glen Peterson	681-3272	1440 Northland Dr., MH
Zbiginiew Karwowski	681-3294	1440 Northland Dr., MH
Larry Scott	681-5862	1345
Pete Bucheger	681-5846	1345
Sean Murphy	681-3127	1440
Hu Sheng	Compri Hotel RM 510	CRI - Petroleum Region 5847 San Felipe Suite 3000 Houston, TX 77057 713-965-758
Franz-Karl Schmatzer	Cedars Edina	Cray Germany - Munich
Paul Wells	681-3143	1440

Buffer Memory Read Data

HINT: on the R terms — DMA Port 3 is muxed Loop 50/51 with MOS R72 - R87

HINT: on the 2BE B20 - B27 is shared terms with CPU

Addressing

Hint:
Some As on the write to Buffer memory except that control is different

TERM: F0, F1, F2, F3, F4, F5, F6, F7, F8, F10, F11, F12, F13, F14, F15

TP: D16', D14', D10', D18', D27', D23', D5', D25', C42', C67', C38', C46', C40', C70', C72', C48'

G0 – G15 → V0 – V15

TERM: W0, W1, W2, W3, W4, W5, W6, W7, W8, W9, W10, W11, W12, W13, W14, W15

TP: D19', D24', D30', D17', D1', D4', D13', D15', C39', C71', C60', C58', C28', C54', C22', C24'

W0 – W15 → V20 – V37 → R0 – R15

2BP

Even Buffer

TERM: G0, G1, G2, G3, G4, G5, G6, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G17

TP: C46', C44', C42', C38', C33', C35', C29', C31', C26', D25', D31', D50', D42', D35', D38', D40', D49', D48'

ODD Buffer

TERM: G20, G21, G22, G23, G24, G25, G26, G27, G28, G29, G30, G31, G32, G33, G34, G35, G36, G37

TP: C48', C52', C50', C40', C18', C15', C14', C12', D23', D21', D29', D27', D36', D33', D37', D43', D46', D44'

G0 – G37 → H0 – H37

TERM: J0, J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17

TP: C60', C53', C47', C51', C19', C32', C22', C21', C24', D30', D34', D59', D41', D54', D51', D45', D66', D62'

Buffer Memory Read → DATA

2NR:

I0 – I19 → A0 – A19

↳ TERM: B0, B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B

TP: B58', B66', BC2', BC0', B57', B56', B55', B54', A1', A3', A2', A11', A5', A15', A07', A13', A22', A48', A47', A52

TERM: C0, C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19

TP: B67', B68', B70', B72', B59', B61', B65', B63', A10', A8', A6', A4', A18', A16', A12', A14', A21', AC6', A64', A62'

TERM: D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19

TP: D8', D7', D12', A11', D3', D2', D6', D9', C63', C66', C56', C64', C65', E26', C68', C69'.

TERM: E0, E1, E2, E3, E4, E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, E15

TP: D68', D72', D67', D70', D59', D61', D65', D63', C6', C8', C3', C1', C25', C23', C12', C7'

2BH

TERM: B50, B51, B52, B53, B54, B55, B56, B57, B58, B59, B61, B61, B62, B63, B64, B65 B66, B67, B68, B69

TP: B06', B03', B04', B35', B27', B29', B63', B59', B61', B14', B10', B12', B38', B36', B40', B72', B67', B70', A13', A05'

TERM: B70, B71, B72, B73

TP: A20', A14', A16', A15'

Incrémentor: C terms - D terms

↳ R32' - R55'

2NA:

HINT: A terms, C terms, D terms, E terms, F terms

↳ R terms

All terms are stored by All processors muxed in At the A terms

- Form Ras and Cas Lines for : Address for 2NB

2NK:

HINT I term go directly to R term no TP for 2NK -> 2NA

Address for write to Buffer Memory

Addressing Local Memory & Block Length

Losp 50/51: E terms

2BL: $2^4 - 2^{15}$

TERM: D04, D05, D06, D07, D08, D09, D10, D11, D12, D13, D14, D15

TP: D04', D03', D20', D25', 050', D52', C68', C61', C50', C57', C06', C08'

Block length

TERM: D24, D25, D26, D27, D28, D29, D30, D31, D32, D33

TP: 001, 005, D02, 007, D53, D51, C71, C53, C69, 101

F04 – F15 ⟶ R28 – R39

* HINT - The 2BC use same terms for Losp 50/51 as Buffer memory (DMA3) For Address I/O

Group Ø Data

TERM: HØ, H1, H2, H3, H4, H5, H6, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17

TP: B19, B32', B36', B38', A47', A50', A41', A44', D15', D14', D17', D20', C68', C67', C64', C63', C51, C50

TERM: JØ, J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17

TP: B10', B12', B16', B18', A62', A65', A55', A57', D01', D02', D04', D03', C53', C54', C57', C62', A38', A36', J18, J19, A42', A35'

TERM: kØ, k1, k2, k3, k4, k5, k6, k7, k8, k9, k10, k11, k12, k13, k14, k15, k16, k17, k18, k19

TP: B23', B20', B31', B33', A64', A57', A48', A40', D05', D08', D09', D10', C49', C61', C60', C59', B46', B48', B42', B44'

RØ- R19 → 2Y B

2NW:

2BU → 2NW
R00-17 → A0-A17

Proc A0:

TERM: A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17

TP: B70', B63', B68', B50', A12', A16', A10', A25', A29', D72', D52', D40', D44', C28', C32', C34', C23', C38'

PROC A1:

TERM: B0, B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17.

TP: B69', B58', B61', B52', A09', A14', A03', A19', A27', D67', D48', D38', D46', C39', C42', C45', C25', C41'

Proc A3:

TERM: D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17

TP: B72', B65', B55', B59', A4', A5', A18', A20', A24', D70', D55', D50', D31', C29', C27', C08, C33, C30'

Group 0 = E0 - E17

Butter Memory Write - Data

- Hint 1 make sure Losp 50/51 are working because they use same DMA Port. out of the 2BE → 2BU

2BU:

Even Buffer

TERM: C00, C01, C02, C03, C04, C05, C06, C07, C08, C09, C10, C11, C12, C13, C14, C15, C16, C17

TP: C08', C06', C03', C04', C23', C20', C14', C10', C31', C33', C29', C27', C44', C42', C40', C38', C57', C59'

ODD Buffer

Term: C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37

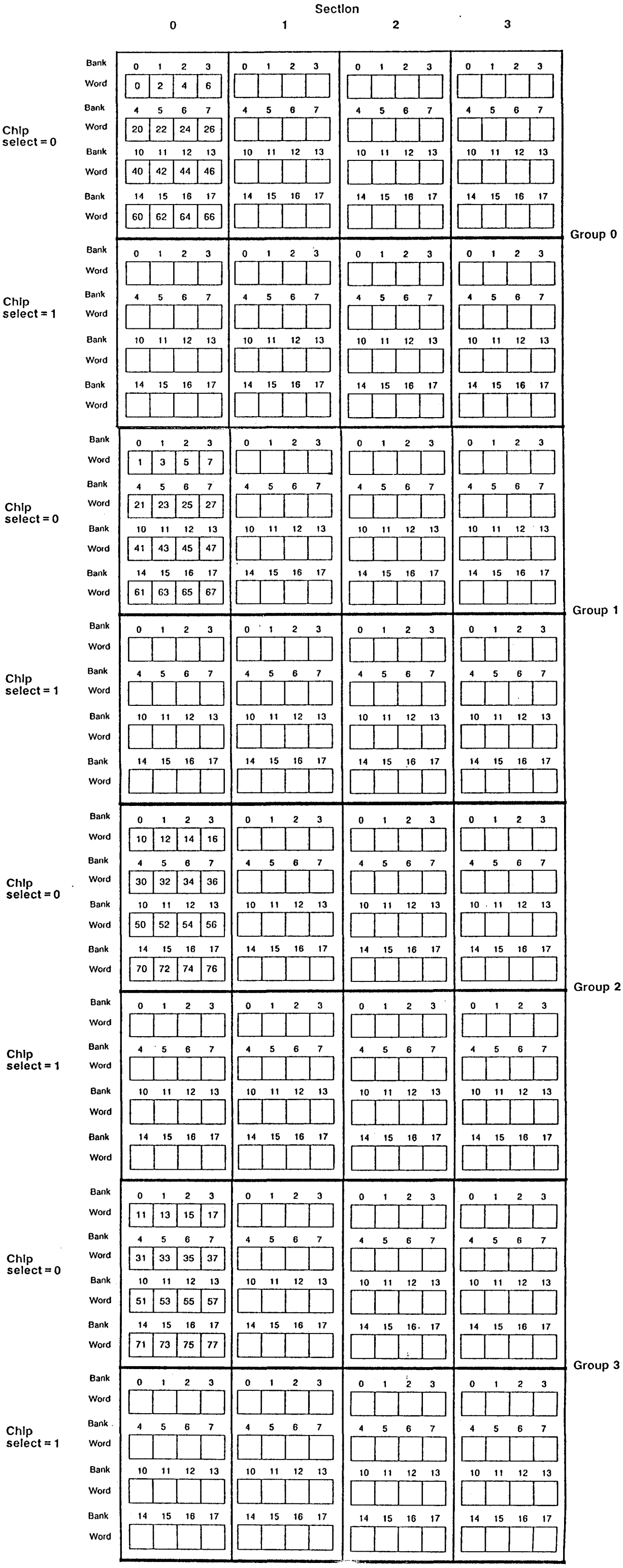
TP: D70', D69', D71', D72', D61', D66', D68', D67', D62', D63', D65', D64', D55', D57', D59', D60', D38', D40'

E00 - 17 Even Buffer
E20 - E37 odd Buffer

TERM: R00, R01, R02, R03, R04, R05, R06, R07, R08, R09, R10, R11, R12, R13, R14, R15, R16, R17

TP: C69, C72, C70, C67, C71, C68', C60, C66, C65, D02, D04', D03, D20, D28, D01, D32, D19', D21'

Map showing the destination of a block of words in the SSD module for a 32 Mword SSD.



Map showing the destination of a block of words in the SSD module for a 128 Mword SSD.

Section

	0	1	2	3
Bank	0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
0 → Word	0 2 4 6	10 12 14 16	20 22 24 26	30 32 34 36
Bank	4 5 6 7	4 5 6 7	4 5 6 7	4 5 6 7
1 → Word (Chip select = 0)	40 42 44 46	50 52 54 56	60 62 64 66	70 72 74 76
Bank	10 11 12 13	10 11 12 13	10 11 12 13	10 11 12 13
2 → Word				
Bank	14 15 16 17	14 15 16 17	14 15 16 17	14 15 16 17
3 → Word				
Bank	0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
4 → Word				
Bank	4 5 6 7	4 5 6 7	4 5 6 7	4 5 6 7
5 → Word (Chip select = 1)				
Bank	10 11 12 13	10 11 12 13	10 11 12 13	10 11 12 13
6 → Word				
Bank	14 15 16 17	14 15 16 17	14 15 16 17	14 15 16 17
7 → Word				

Group 0

	0	1	2	3
Bank	0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
0 → Word	1 3 5 7	11 13 15 17	21 23 25 27	31 33 35 37
Bank	4 5 6 7	4 5 6 7	4 5 6 7	4 5 6 7
1 → Word (Chip select = 0)	41 43 45 47	51 53 55 57	61 63 65 67	71 73 75 77
Bank	10 11 12 13	10 11 12 13	10 11 12 13	10 11 12 13
2 → Word				
Bank	14 15 16 17	14 15 16 17	14 15 16 17	14 15 16 17
3 → Word				
Bank	0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
4 → Word				
Bank	4 5 6 7	4 5 6 7	4 5 6 7	4 5 6 7
5 → Word (Chip select = 1)				
Bank	10 11 12 13	10 11 12 13	10 11 12 13	10 11 12 13
6 → Word				
Bank	14 15 16 17	14 15 16 17	14 15 16 17	14 15 16 17
7 → Word				

Group 1

	0	1	2	3
Bank	0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
0 → Word				
Bank	4 5 6 7	4 5 6 7	4 5 6 7	4 5 6 7
1 → Word (Chip select = 0)				
Bank	10 11 12 13	10 11 12 13	10 11 12 13	10 11 12 13
2 → Word				
Bank	14 15 16 17	14 15 16 17	14 15 16 17	14 15 16 17
3 → Word				
Bank	0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
4 → Word	0 2 4 6	10 12 14 16	20 22 24 26	30 32 34 36
Bank	4 5 6 7	4 5 6 7	4 5 6 7	4 5 6 7
5 → Word (Chip select = 1)	40 42 44 46	50 52 54 56	60 62 64 66	70 72 74 76
Bank	10 11 12 13	10 11 12 13	10 11 12 13	10 11 12 13
6 → Word				
Bank	14 15 16 17	14 15 16 17	14 15 16 17	14 15 16 17
7 → Word				

Group 2

	0	1	2	3
Bank	0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
0 → Word				
Bank	4 5 6 7	4 5 6 7	4 5 6 7	4 5 6 7
1 → Word (Chip select = 0)				
Bank	10 11 12 13	10 11 12 13	10 11 12 13	10 11 12 13
2 → Word				
Bank	14 15 16 17	14 15 16 17	14 15 16 17	14 15 16 17
3 → Word				
Bank	0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
4 → Word	1 3 5 7	11 13 15 17	21 23 25 27	31 33 35 37
Bank	4 5 6 7	4 5 6 7	4 5 6 7	4 5 6 7
5 → Word (Chip select = 1)	41 43 45 47	51 53 55 57	61 63 65 67	71 73 75 77
Bank	10 11 12 13	10 11 12 13	10 11 12 13	10 11 12 13
6 → Word				
Bank	14 15 16 17	14 15 16 17	14 15 16 17	14 15 16 17
7 → Word				

Group 3

Map showing the destination of a block of words in the SSD module for a 64 Mword SSD.

Section

	0	1	2	3	
Chip select = 0	Bank 0 1 2 3 Word 0 2 4 6	Bank 0 1 2 3 Word 10 12 14 16	Bank 0 1 2 3 Word	Bank 0 1 2 3 Word	
	Bank 4 5 6 7 Word 20 22 24 26	Bank 4 5 6 7 Word 30 32 34 36	Bank 4 5 6 7 Word	Bank 4 5 6 7 Word	
	Bank 10 11 12 13 Word 40 42 44 46	Bank 10 11 12 13 Word 50 52 54 56	Bank 10 11 12 13 Word	Bank 10 11 12 13 Word	
	Bank 14 15 16 17 Word 60 62 64 66	Bank 14 15 16 17 Word 70 72 74 76	Bank 14 15 16 17 Word	Bank 14 15 16 17 Word	Group 0
Chip select = 1	Bank 0 1 2 3 Word	Bank 0 1 2 3 Word	Bank 0 1 2 3 Word	Bank 0 1 2 3 Word	
	Bank 4 5 6 7 Word	Bank 4 5 6 7 Word	Bank 4 5 6 7 Word	Bank 4 5 6 7 Word	
	Bank 10 11 12 13 Word	Bank 10 11 12 13 Word	Bank 10 11 12 13 Word	Bank 10 11 12 13 Word	
	Bank 14 15 16 17 Word	Bank 14 15 16 17 Word	Bank 14 15 16 17 Word	Bank 14 15 16 17 Word	
Chip select = 0	Bank 0 1 2 3 Word 1 3 5 7	Bank 0 1 2 3 Word 11 13 15 17	Bank 0 1 2 3 Word	Bank 0 1 2 3 Word	
	Bank 4 5 6 7 Word 21 23 25 27	Bank 4 5 6 7 Word 31 33 35 37	Bank 4 5 6 7 Word	Bank 4 5 6 7 Word	
	Bank 10 11 12 13 Word 41 43 45 47	Bank 10 11 12 13 Word 51 53 55 57	Bank 10 11 12 13 Word	Bank 10 11 12 13 Word	
	Bank 14 15 16 17 Word 61 63 65 67	Bank 14 15 16 17 Word 71 73 75 77	Bank 14 15 16 17 Word	Bank 14 15 16 17 Word	Group 1
Chip select = 1	Bank 0 1 2 3 Word	Bank 0 1 2 3 Word	Bank 0 1 2 3 Word	Bank 0 1 2 3 Word	
	Bank 4 5 6 7 Word	Bank 4 5 6 7 Word	Bank 4 5 6 7 Word	Bank 4 5 6 7 Word	
	Bank 10 11 12 13 Word	Bank 10 11 12 13 Word	Bank 10 11 12 13 Word	Bank 10 11 12 13 Word	
	Bank 14 15 16 17 Word	Bank 14 15 16 17 Word	Bank 14 15 16 17 Word	Bank 14 15 16 17 Word	
Chip select = 0	Bank 0 1 2 3 Word	Bank 0 1 2 3 Word	Bank 0 1 2 3 Word	Bank 0 1 2 3 Word	
	Bank 4 5 6 7 Word	Bank 4 5 6 7 Word	Bank 4 5 6 7 Word	Bank 4 5 6 7 Word	
	Bank 10 11 12 13 Word	Bank 10 11 12 13 Word	Bank 10 11 12 13 Word	Bank 10 11 12 13 Word	
	Bank 14 15 16 17 Word	Bank 14 15 16 17 Word	Bank 14 15 16 17 Word	Bank 14 15 16 17 Word	Group 2
Chip select = 1	Bank 0 1 2 3 Word	Bank 0 1 2 3 Word	Bank 0 1 2 3 Word	Bank 0 1 2 3 Word	
	Bank 4 5 6 7 Word	Bank 4 5 6 7 Word	Bank 4 5 6 7 Word	Bank 4 5 6 7 Word	
	Bank 10 11 12 13 Word	Bank 10 11 12 13 Word	Bank 10 11 12 13 Word	Bank 10 11 12 13 Word	
	Bank 14 15 16 17 Word	Bank 14 15 16 17 Word	Bank 14 15 16 17 Word	Bank 14 15 16 17 Word	
Chip select = 0	Bank 0 1 2 3 Word	Bank 0 1 2 3 Word	Bank 0 1 2 3 Word	Bank 0 1 2 3 Word	
	Bank 4 5 6 7 Word	Bank 4 5 6 7 Word	Bank 4 5 6 7 Word	Bank 4 5 6 7 Word	
	Bank 10 11 12 13 Word	Bank 10 11 12 13 Word	Bank 10 11 12 13 Word	Bank 10 11 12 13 Word	
	Bank 14 15 16 17 Word	Bank 14 15 16 17 Word	Bank 14 15 16 17 Word	Bank 14 15 16 17 Word	Group 3
Chip select = 1	Bank 0 1 2 3 Word	Bank 0 1 2 3 Word	Bank 0 1 2 3 Word	Bank 0 1 2 3 Word	
	Bank 4 5 6 7 Word	Bank 4 5 6 7 Word	Bank 4 5 6 7 Word	Bank 4 5 6 7 Word	
	Bank 10 11 12 13 Word	Bank 10 11 12 13 Word	Bank 10 11 12 13 Word	Bank 10 11 12 13 Word	
	Bank 14 15 16 17 Word	Bank 14 15 16 17 Word	Bank 14 15 16 17 Word	Bank 14 15 16 17 Word	

Error logger
Banks

SSD MODEL C

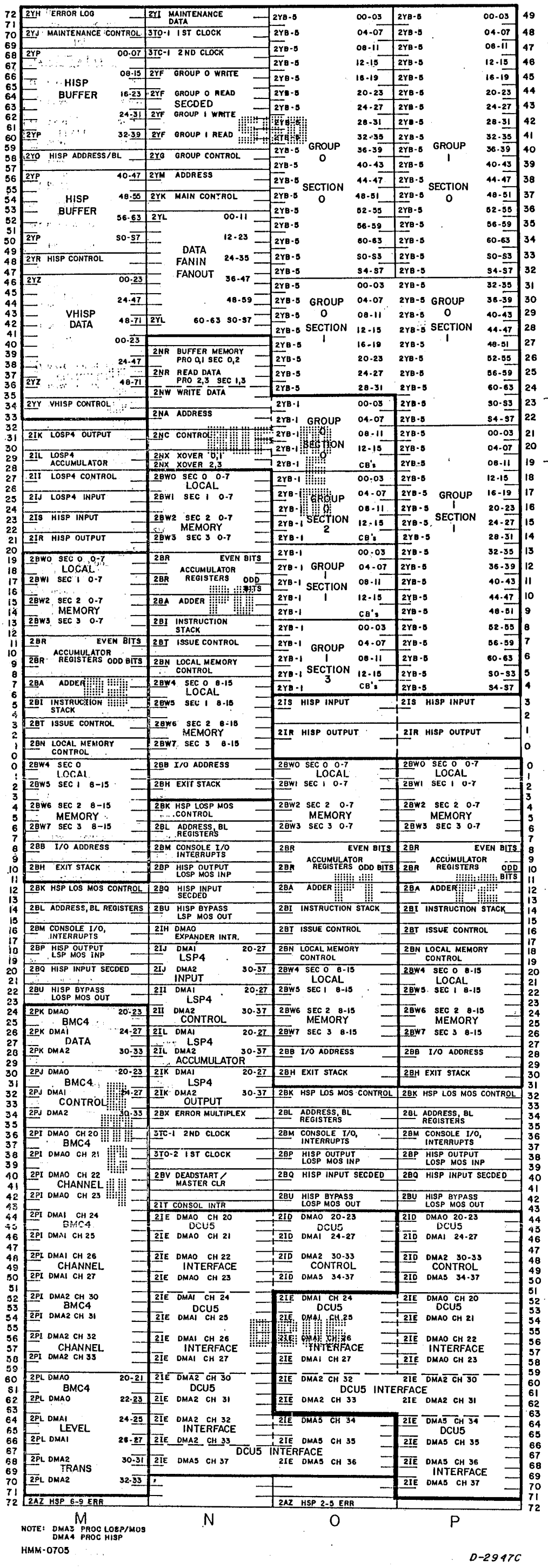
	A	B	C	D	
71		2YB 00-03	2YB	2YB	47
70		2YB 04-07	2YB	2YB	46
68		2YB 08-11	2YB	2YB	45
66		2YB 12-15	2YB	2YB	44
64		2YB 16-19 GROUP 0	2YB GROUP 0	2YB GROUP 0	43
62		2YB 20-23	2YB	2YB	42
60		2YB 24-27	2YB	2YB	41
58		2YB 28-31	2YB	2YB	40
56		2YB 32-35	2YB	2YB	39
54		2YB 36-39	2YB	2YB	38
		2YB 40-43 SECTION 0	2YB SECTION 1	2YB SECTION 2	37
52	3TO SYSTEM CLOCK	2YB 44-47	2YB	2YB	36
	3TC CLOCK FANOUT	2YB 48-51	2YB	2YB	35
50	2YH ERROR LOG	2YB 52-55	2YB	2YB	34
48	2YJ MAINTENANCE CONTROL	2YB 56-59	2YB	2YB	33
46	2YI MAINTENANCE DATA	2YB 60-63	2YB	2YB	32
44	2YG GROUP 0,1 CONTROL	2YB S0-S3	2YB	2YB	31
42	2YF GROUP 0 WRITE ERROR CORRECTION	2YB S4-S7	2YB	2YB	30
40	2YF GROUP 0 READ ERROR CORRECTION	2YB 00-03	2YB 24-27	2YB 48-51	29
38	2YF GROUP 1 WRITE ERROR CORRECTION	2YB 04-07	2YB 28-31	2YB 52-55	28
36	2YF GROUP 1 READ ERROR CORRECTION	2YB 08-11 GROUP 0	2YB 32-35 SECTION 3	2YB 56-59	27
34	2YZ 00-23	2YB 12-15	2YB 36-39	2YB 60-63	26
32	2YZ VHISP 24-47	2YB 16-19	2YB 40-43	2YB S0-S3	25
30	2YZ VHISP 48-71	2YB 20-23	2YB 44-47	2YB S4-S7	24
28	2YZ VHISP 00-23	2YB 00-03	2YB	2YB	23
26	2YZ VHISP 24-47	2YB 04-07	2YB	2YB	22
24	2YZ 48-71	2YB 08-11	2YB	2YB	21
22	2YY VHISP 0 CONTROL	2YB 12-15	2YB	2YB	20
20	2YC SYSTEM ADDRESS	2YB 16-19 GROUP 1	2YB GROUP 1	2YB GROUP 1	19
18	2YD SYSTEM CONTROL	2YB 20-23	2YB	2YB	18
16	2YU CROSSOVER	2YB 24-27	2YB	2YB	17
14	2YZ 00-23	2YB 28-31	2YB	2YB	16
12	2YZ VHISP 24-47	2YB 32-35	2YB	2YB	15
10	2YZ VHISP 48-71	2YB 36-39	2YB	2YB	14
8	2YZ VHISP 00-23	2YB 40-43	2YB	2YB	13
6	2YZ VHISP 24-47	2YB 44-47 SECTION 0	2YB SECTION 1	2YB SECTION 2	12
4	2YZ VHISP 48-71	2YB 48-51	2YB	2YB	11
2	2YY VHISP 1 CONTROL	2YB 52-55	2YB	2YB	10
0	2YF GROUP 2 WRITE ERROR CORRECTION	2YB 56-59	2YB	2YB	9
0	2YF GROUP 2 READ ERROR CORRECTION	2YB 60-63	2YB	2YB	8
2	2YF GROUP 3 WRITE ERROR CORRECTION	2YB S0-S3	2YB	2YB	7
4	2YF GROUP 3 READ ERROR CORRECTION	2YB S4-S7	2YB	2YB	6
6	2YG GROUP 2,3 CONTROL	2YB 00-03	2YB 24-27	2YB 48-51	5
8	2YE 00-07	2YB 04-07	2YB 28-31	2YB 52-55	4
10	2YE DATA FANIN/OUT 08-15	2YB 08-11 GROUP 1	2YB 32-35 SECTION 3	2YB 56-59	3
12	2YE 16-23	2YB 12-15	2YB 36-39	2YB 60-63	2
14	2YE 24-31	2YB 16-19	2YB 40-43	2YB S0-S3	1
16	2YE 32-39	2YB 20-23	2YB 44-47	2YB S4-S7	0
18	2YE 40-47	2YB 00-03	2YB	2YB	0
20	2YE 48-55	2YB 04-07	2YB	2YB	1
22	2YE 56-63	2YB 08-11	2YB	2YB	2
24	2YE S0-S7	2YB 12-15	2YB	2YB	3
26	3TC CLOCK FANOUT	2YB 16-19 GROUP 2	2YB GROUP 2	2YB GROUP 2	4
28	2YP HISP 0,1 DATA BUFFER	2YB 20-23	2YB	2YB	5
30	2YP	2YB 24-27	2YB	2YB	6
32	2YP	2YB 28-31	2YB	2YB	7
34	2YP	2YB 32-35	2YB	2YB	8
36	2YP	2YB 36-39	2YB	2YB	9
38	2YP	2YB 40-43 SECTION 0	2YB SECTION 1	2YB SECTION 2	10
40	2YØ HISP 0,1 ADDRESS & BLK LENGTH	2YB 44-47	2YB	2YB	11
42	2YP HISP 0,1 DATA BUFFER	2YB 48-51	2YB	2YB	12
44	2YP	2YB 52-55	2YB	2YB	13
46	2YP	2YB 56-59	2YB	2YB	14
48	2YP	2YB 60-63	2YB	2YB	15
50	2YR HISP 0-3	2YB S0-S3	2YB	2YB	16
52	2YP HISP 2,3 DATA BUFFER	2YB S4-S7	2YB	2YB	17
54	2YP	2YB 00-03	2YB 24-27	2YB 48-51	18
56	2YP	2YB 04-07	2YB 28-31	2YB 52-55	19
58	2YP	2YB 08-11 GROUP 2	2YB 32-35 SECTION 3	2YB 56-59	20
60	2YP	2YB 12-15	2YB 36-39	2YB 60-63	21
62	2YØ HISP 2,3 ADDRESS & BLK LENGTH	2YB 16-19	2YB 40-43	2YB S0-S3	22
64	2YP HISP 2,3 DATA BUFFER	2YB 20-23	2YB 44-47	2YB S4-S7	23
66	2YP	2YB 24-27	2YB	2YB	24
68	2YP	2YB 28-31	2YB	2YB	25
70	2YP	2YB 32-35	2YB	2YB	26
71		2YB 36-39	2YB	2YB	27
		2YB 40-43	2YB	2YB	28
		2YB 44-47 GROUP 3	2YB GROUP 3	2YB GROUP 3	29
		2YB 48-51	2YB	2YB	30
		2YB 52-55	2YB	2YB	31
		2YB 56-59	2YB	2YB	32
		2YB 60-63	2YB	2YB	33
		2YB S0-S3 SECTION 0	2YB SECTION 1	2YB SECTION 2	34
		2YB S4-S7	2YB	2YB	35
		2YB 00-03	2YB 24-27	2YB 48-51	36
		2YB 04-07	2YB 28-31	2YB 52-55	37
		2YB 08-11 GROUP 3	2YB 32-35 SECTION 3	2YB 56-59	38
		2YB 12-15	2YB 36-39	2YB 60-63	39
		2YB 16-19	2YB 40-43	2YB S0-S3	40
		2YB 20-23	2YB 44-47	2YB S4-S7	41
		2YB 24-27	2YB	2YB	42
		2YB 28-31	2YB	2YB	43
		2YB 32-35	2YB	2YB	44
		2YB 36-39	2YB	2YB	45
		2YB 40-43	2YB	2YB	46
		2YB 44-47	2YB	2YB	47

M N O P

HMM-0605

D-1901

IOP MODEL C S/N 101

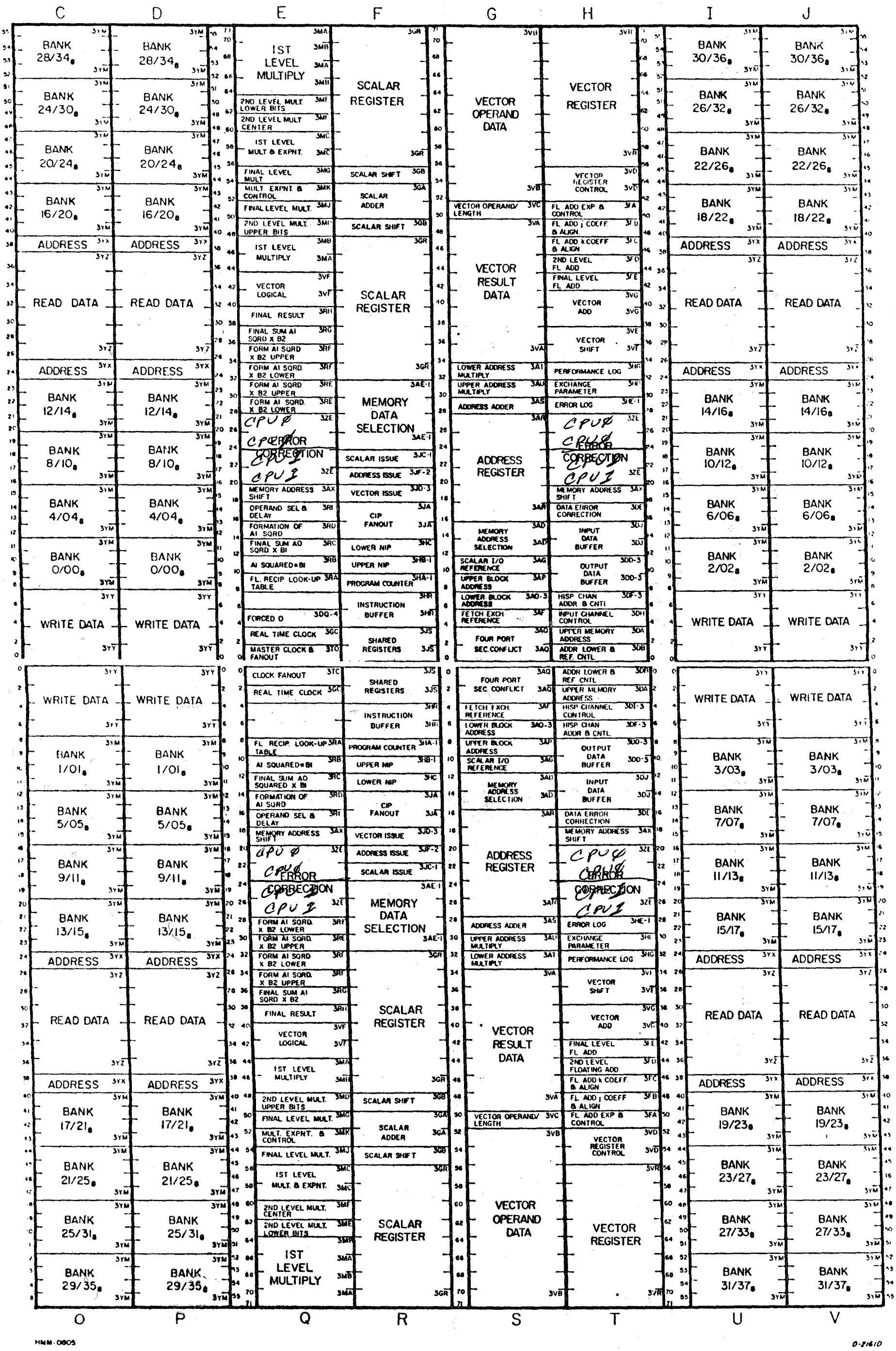


NOTE: DMA3 PROC LOSP/MOS
DMA4 PROC HISP

HMM-0705

D-2947C

CRAY X-MP/216



HMM-0805

D-21610