CRAY RESEARCH, INC.

CRAY X-MP AND CRAY-1® COMPUTER SYSTEMS

IOS TABLE DESCRIPTIONS INTERNAL REFERENCE MANUAL

SM-0007

RECORD OF REVISION

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Each time this manual is revised and reprinted, all changes issued against the previous version in the form of change packets are incorporated into the new version and the new version is assigned an alphabetic level. Between reprints, changes may be issued against the current version in the form of change packets. Each change packet is assigned a numeric designator, starting with 01 for the first change packet of each revision level.

Every page changed by a reprint or by a change packet has the revision level and change packet number in the lower righthand corner. Changes to part of a page are noted by a change bar along the margin of the page. A change bar in the margin opposite the page number indicates that the entire page is new; a dot in the same place indicates that information has been moved from one page to another, but has not otherwise changed.

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Revision	Description
	May, 1983 - Original printing.
01	January, 1984 - This change packet brings the manual into agreement with version 1.13 of COS.
02	October, 1984 - This change packet brings the manual into agreement with version 1.14 of COS. Changes were made to: Console Support Tasks Shared Memory, I/O Stream Control Table, and Station-shared Logic Memory. Two sections were also added: section 8, User Channel Tables, and section 9, DD-49 Disk Tables.

PREFACE

This publication is part of a set of manuals written for programmers, analysts, and field engineers who have the responsibility of installing, debugging, and modifying the software produced by Cray Research, Inc. (CRI).

This manual describes tables for the portions of the Cray Operating System (COS) executing in the I/O Subsystem. Publications in this set that describe the internal design of COS software are:

SM-0017	FORTRAN (CFT) Internal Reference Manual
SM-0040	COS EXEC/STP/CSP Internal Reference Manual
SM-0041	COS Product Set Internal Reference Manual
SM-0042	Front-End Protocol Internal Reference Manual
SM-0045†	COS Table Descriptions Internal Reference Manual
SM-0046	IOS Software Internal Reference Manual
SM-0072	COS Simulator (CSIM) Internal Reference Manual

Manuals in the set that define procedures and external features or tools needed for installing and maintaining CRI software are:

SM-0043	COS Operational Procedures Reference Manual
SM-0044	COS Operational Aids Reference Manual
SR-0073	COS Simulator (CSIM) Reference Manual

† This manual is available only on tape. See your CRI site analyst for information.

CONTENTS

KERNEL TABLES AND QUEUES (continued)

TABLE

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INTRODUCTION 1

The tables and queues in this manual are organized and labeled according to the I/O Subsystem software divisions they primarily serve. The divisions and associated labels (K, C, N, S, B, T) follow.

- K Kernel tables and queues
- C Concentrator tables
- N NSC activity tables
- S Station tables
- B Block multiplexer tables
- T Tape Exec tables

The format for tables in this manual is variable because all tables are not constructed in the same way. For example, field names (assigned with the FIELD macro) are present for all of the station tables but for few of the Kernel tables. Also, while most tables are based on 16-bit parcels, a few are constructed of 64-bit words. Similarly, the parcel numbers in Kernel tables are defined in octal; the parcel numbers for most other tables, however, are given in decimal.

KERNEL TABLES AND QUEUES 2

Kernel tables and queues in this section are used in all of the I/O Processors in an I/O Subsystem unless otherwise noted.

ACTIVITY DESCRIPTOR (AD@)

An Activity Descriptor contains control information about an activity that is necessary to the Kernel. The Kernel establishes an Activity Descriptor in the free memory section of Local Memory for each activity when that activity is created. The Activity Descriptor remains in Local Memory until the activity terminates.

Field	Parcel	Bits	Description
AD@QL	0	0-15	Link for queues
AD@AL	1	0-15	Link to existing Activity Descriptors
AD@PRI	2	0-15	Priority of activity
AD@MSU	3	0-15	Buffer Memory address (high-order bits) of software stack if not resident
AD@MSL	4	0-15	Buffer Memory address (low-order bits) of software stack if not resident
AD@SIZ	5	0-15	Size of software stack in 64-bit words
	6-7	0-15	Unused
AD@SMD	10	0-15	Link to next storage module to activate, if activity is idle. If activity is executing, this parcel is a link to the current SMOD.
AD@FLG	11	0-15	Flags:
	11	1	Activity type: 0 Normal activity 1 Demon activity

Field	Parcel	Bits	Description
AD@FU	12	0-15	Reserved for function code of current request
AD@RC	13	0-15	Response code on Kernel calls
AD@P1	14	0-15	Parameter 1 save cell on service requests
AD@P2	15	0-15	Parameter 2 save cell on service requests
AD@P3	16	0-15	Parameter 3 save cell on service requests
AD@P4	17	0-15	Parameter 4 save cell on service requests
AD@NM	20-23	0-15	ASCII name of root overlay

AMSG DAL QUEUE (MIMDALQ)

This queue is a linked list of Disk Activity Links (DALs) containing messages to be processed by the AMSG overlay.

Parcel	Bits	Description
0	0-15	Pointer to first DAL on this queue
1	0-15	Pointer to last DAL on this queue
2	0-15	Count of DALs on queue

BUFFER MEMORY DISK BUFFER ALLOCATE TABLE (BBDISK BB@)

This table controls allocation of disk buffers in Buffer Memory. Each processor has a reserved area in Buffer Memory for its buffers.

Field	Word	Bits	Description
BB@IND	0	0-15	Bit map search index. This index allows a circular scan of the bit map and thus circular allocation of disk buffers.
BB@USE	1	0-15	Number of disk buffers in use
BB@TOT	2	0-15	Number of disk buffers defined
BB@MAP	3	0-15	Local Memory parcel address of bit map. The bit map contains a bit for each defined disk buffer. A 1 bit indicates a buffer available for assignment; a 0 bit indicates a buffer in use.
BB@SHF	4	0-15	Disk buffer word size expressed as a power of two
BB@BAU	5	0-15	(High-order bits) Buffer Memory address of the area reserved for disk buffers for this IOP
BB@BAL	6	0-15	(Low-order bits) Buffer Memory address of the area reserved for disk buffers for this IOP
BB@LEN	7	-	Equate defining length of table

BUFFER MEMORY MESSAGE ALLOCATE TABLE (BBDAL BB@)

This table controls allocation of message packets (DALs) in Buffer Memory. Each processor has a reserved area in Buffer Memory for its message packets.

Field	Word	Bits	Description
BB@IND	0	0-15	Bit map search index. This index allows a circular scan of the bit map and thus circular allocation of message packets.
BB@USE	1	0-15	Number of message packets in use
BB@TOT	2	0-15	Number of message packets defined
BB@MAP	3	0-15	Local Memory parcel address of bit map. The bit map contains a bit for each defined message packet. A 1 bit indicates a packet available for assignment; a 0 bit indicates a packet in use.
BB@SHF	4	0-15	Message packet word size expressed as a power of two
BB@BAU	5	0-15	(High-order bits) Buffer Memory address of the area reserved for message packets for this IOP
BB@BAL	6	0-15	(Low-order bits) Buffer Memory address of the area reserved for message packets for this IOP
BB@LEN	7	-	Equate defining length of table

BUFFER MEMORY SOFTWARE STACK ALLOCATE TABLE (BBSOFT BB@)

This table controls allocation of software stacks in Buffer Memory. Each processor has a reserved area in Buffer Memory for its software stacks.

Field	Word	Bits	Description
BB@IND	0	0-15	Bit map search index. This index allows a circular scan of the bit map and thus circular allocation of software stacks.
BB@USE	1	0-15	Number of software stacks in use
BB@TOT	2	0-15	Number of software stacks defined
BB@MAP	3	0-15	Local Memory parcel address of bit map. The bit map contains a bit for each defined disk buffer. A 1 bit indicates a buffer available for assignment; a 0 bit indicates a buffer in use.
BB@SHF	4	0-15	Disk buffer word size expressed as a power of two
BB@BAU	5	0-15	(High-order bits) Buffer Memory address of the area reserved for software stacks for this IOP
BB@BAL	6	0-15	(Low-order bits) Buffer Memory address of the area reserved for software stacks for this IOP
BB@LEN	7	-	Equate defining length of table

C PACKET - ERROR CHANNEL LOG INFORMATION (ER$)

This request for error information to log is output to the mainframe only.

Label	Parcel	Description
	0	Destination (DA@DID)
	1	Source (DA@SID)
	2	Unused
	3	Type: 1 Memory error 2 Disk error 3 Turns off error logging 4 Turns on error logging 5 Tape error
ER$ST0	4	Status: 1 BIOP Local Memory error 2 IOP-2 Local Memory error 4 IOP-3 Local Memory error 10 Buffer Memory error 20 Central Memory error 40 100 Mbyte channel input A error 100 100 Mbyte channel output B error 200 100 Mbyte channel input C error 400 100 Mbyte channel output D error
ER$ST1	5	First error parameter. The value varies according to the type of error being reported. (See section 3 of the I/O Subsystem Reference Manual, CRI publication HR-0030.)
ER$ST2	6	Second error parameter. For a Buffer Memory or Central Memory error, this field contains the low-order 16 bits of the error address. Otherwise, it is 0.
ER$ST3	7	Third error parameter. For a Buffer Memory or Central Memory error, this field contains the high-order bits of the error address. Otherwise, it is 0.
	8-23	Unused

CHANNEL TO IOP CONVERSION TABLE (MATT)

This table translates a channel into a logical I/O Processor identifier. It is set up at initialization to reflect the I/O Processor in which it resides.

Parcel	Bits	Description
0	0-15	For MIOP, contains a value of 1 to translate channel 6 to BIOP
1	0-15	For MIOP, contains a value of 2 to translate channel 10_8 to DIOP
2	0-15	For MIOP, contains a value of 3 to translate channel 12_8 to XIOP

CRT CHANNEL TABLE (BCRT)

The CRT Channel Table comprises a series of pointers that locate the CRT Table for each channel pair defined. The channel pairs are represented in octal.

Parcel	Bits	Description
0	0-15	Address of CRT Table for channel pair 40-41, CRT A
1	0-15	Address of CRT Table for channel pair 42-43, CRT B
2	0-15	Address of CRT Table for channel pair 44-45, CRT C
3	0-15	Address of CRT Table for channel pair 46-47, CRT D

CRT DEMON INTERRUPT QUEUE (CRTQU)

This table maintains input characters from the IOP's display/consoles from the time they are received by the Kernel interrupt processor until the CRT demon activity (overlay CRTDEM) processes them.

Parcel	Bits	Description
0	0-15	Address of start of queue
1	0-15	Address of end of queue
2	0-15	Current entry in queue
3	0-15	Next entry in queue
4	0-15	Entry count
5	0-15	Overflow count
6-15	0-7	Input byte in ASCII, if channel is an input channel
	8-15	Channel number

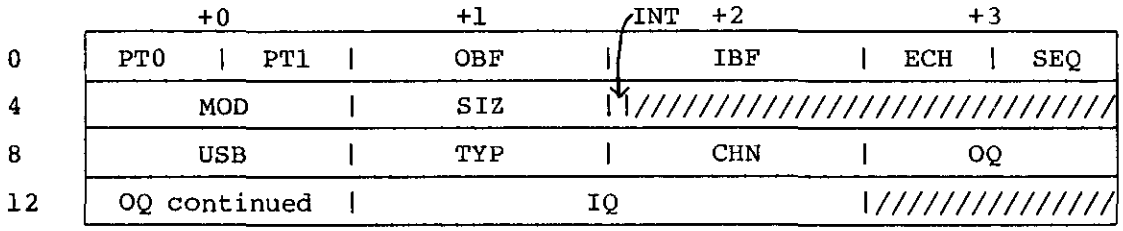
CRT I/O QUEUES (BIQU/BOQU)

The CRT I/O queues form a linked list of Activity Descriptors that are waiting for input or output. Each CRT channel has two parcels for input and two for output.

Label	Parcel	Bits	Description
BIQU	0-7	0-15	Input queues for four CRTs
BOQU	0-7	0-15	Output queues for four CRTs

CRT TABLE (TT@)

This table controls I/O for any CRT that has been defined in AMAP. A table is set up for each CRT during system initialization. The CRT Channel Table (BCRT) contains pointers to these tables.



Field	Parcel	Bits	Description
TT@PT0	0	0-7	Pointer to next character in buffer for input or output
TT@PT1	0	8-15	Pointer to last character in buffer for input or output
TT@OBF	1	0-15	Output message address
TT@IBF	2	0-15	Address of buffer to receive response to message
TT@ECH	3	0-7	A copy of the character keyed in at the CRT
TT@SEQ	3	8-15	Sequence number for function
TT@MOD	4	0-15	Mode of CRT: 0 Not busy 1 Input 2 Output 3 Start a message 10_8 CRT is usurped by an activity
TT@SIZ	5	0-15	Input buffer length
TT@INT	6	0	Input interrupted flag
	6	1-15	Unused
	7	0-15	Unused
TT@USB	8	0-15	Kernel buffer for unsolicited input

Field	Parcel	Bits	Description
TT@TYP	9	0-15	Type of CRT: CF$1440 (0) TEC 1440 CF$455 (1) TEC 455 CF$SOROC (2) SOROC CF$AMPEX (3) AMPEX
TT@CHN	10	0-15	Output channel number
TT@OQ	11-12	0-15	Output queue
TT@IQ	13-14	0-15	Input queue
	15	0-15	Unused

DAL CHAIN DESCRIPTOR (EDES)

This is a linked list of Local Memory Disk Activity Links (DALs), each of which is 40_8 parcels in size.

Parcel	Bits	Description
0	0-15	First entry in DAL chain
1	0-15	Last entry in DAL chain
2	0-15	Population count of DALs in chain

DEMONS INDEX TABLE (DEMONS)

Each entry contains the address of the Activity Descriptor for a demon or zero if the demon has not been created. An entry is allocated and an index (D$*demon*) is defined using the DEAMON macro. An entry address is established using the CREATE macro with the DPTR parameter set to the demon index (D$*demon*).

Parcel	Bits	Description
n	0-15	Activity Descriptor pointer for demon with index (D$*demon*) *n*.

DISK ACTIVITY LINK (DA@)

This table contains the general format for all communication packets between the I/O Subsystem and the mainframe as well as between individual IOPs within the I/O Subsystem.

DAL header:

0	DA@LNK	DA@IFC	DA@DL0	DA@DL1
4	DA@ACT	DA@MES	DA@HP0	//////////////

DAL entry:

8	DA@DID	DA@SID	
.			
.			
.			
.			
28			

Field	Parcel	Bits	Description
DA@LNK	0	0-15	Link cell. Used to chain DALs together.
DA@IFC	1	0-15	Internal function code. This cell contains a code which affects the disposition of the packet.
DA@DL0	2	0-15	Address of DAL in Buffer Memory, high-order bits
DA@DL1	3	0-15	Address of DAL in Buffer Memory, low-order bits
DA@ACT	4	0-15	Activity Descriptor of DAL owner
DA@MES	5	0-15	Message sent across A-A channel
DA@HP0	6	0-15	Header parameter 0. Used to return address of input DAL to polling activity
	7	0-15	Unused

Field	Parcel	Bits	Description
DA@DID	8	0-15	Destination ID of packet.

Input packet:

ID	Value	Description
RQ$DISK	A	Disk request
RQ$STAT	B	Station response to a poll
RQ$BMX0	D	Tape request
RQ$ECHO	E	Echo packet
RQ$INIT1	I	Initialization response
RQ$INIT2	J	Initialization response
RQ$PERF	S	Response to statistics request

Output packet:

ID	Value	Description
RQ$CPU	C1	CPU destination ID

Field	Parcel	Bits	Description
DA@SID	9	0-15	Source ID of packet (following)

Input packet:

ID	Value	Description
RQ$CPU	C1	CPU source ID

Output packet:

ID	Value	Description
RQ$DISK	A	Disk response
RQ$STAT	B	Station request
RQ$ERRR	C	Error information
RQ$TAPE	D	Tape response
RQ$ECHO	E	Echo response
RQ$INIT1	I	Initialization request
RQ$INIT2	J	Initialization request
RQ$PERF	S	Statistics request

DISK ACTIVITY LINK, EXECUTABLE (KD@/DA@)

Executable Disk Activity Links (EDALs) are built from information contained in a master DAL. Each EDAL controls the transfer of one sector of I/O from disk to Central Memory or from Central Memory to disk. The first 8 parcels (0-7) contain the standard DAL header.

Label	Field	Parcel	Bits	Description
KD@DEST	DA@DID	8	0-15	Address of master DAL that spawned this EDAL
KD@LFLG	DA@SID	9	0-15	Flag. If 1, this is the last EDAL for this master DAL.
KD@MSEQ	DA@SEQ	10	0-15	Sequence number of this EDAL among all EDALs for this master
KD@DATL	DA@DAT	11	0-15 0 1 2	Data location: On disk or in Central Memory In Local Memory In Buffer Memory
KD@TOTL	DA@TOT	12	0-15	Address of original copy of this EDAL
KD@BPU	DA@CM0	20	0-15	High-order bits of the starting address in Central Memory of the source or destination of the data, depending on the function to be performed.
KD@BPL	DA@CM1	21	0-15	Low-order bits of the starting address in Central Memory of the source or destination of the data, depending on the function to be performed.
KD@CMD		22	0-15	Function and status codes
	DA@FC	22	0-7	One of the following function codes: 1 Read data 2 Write data 3 Read partial sector (internal function code) 4 Write partial sector (internal function code) 5 Read before write (internal function code) 7 Read from disk to specified Buffer Memory address

Label	Field	Parcel	Bits	Description
KD@CMD	DA@FC (continued)			
			10	Write from Buffer Memory address to disk
			12	Reserved
			14	Write and interrupt when data gets to Buffer Memory (write behind)
			21	Internal I/O; read from disk to Buffer Memory.
			22	Internal I/O; write from Buffer Memory to disk.
KD@CHN		23	0-15	IOP and channel numbers
	DA@TYP	23	0-4	Device type
	DA@IOP	23	5-6	I/O Processor to which the request should be directed (BIOP is 1, IOP-2 is 2, and IOP-3 is 3)
	DA@CHN	23	7-15	Channel on which the I/O is to be performed
KD@HED		24	0-15	Cylinder and head numbers where I/O is to begin. On unrecovered errors, the cylinder and head of the error.
	DA@CYL	24	0-10	Cylinder number
	DA@HED	24	11-15	Head group for the I/O
KD@SEC		25	0-15	Sector number and, for partial sector I/O, the word offset from the beginning of the sector where data transfer begins. On unrecovered errors, the sector of the data in error.
	DA@SEC	25	0-6	Sector number
	DA@OFF	25	7-15	For partial sector I/O, the word offset from the beginning of the sector.
KD@SZU	DA@LN0	26	0-15	High-order bits of the length of the I/O transfer in 64-bit words.

Label	Field	Parcel	Bits	Description
KD@SZL	DA@LN1	27	0-15	Low-order bits of the length of the I/O transfer in 64-bit words. For partial sector I/O, this value need not be a multiple of 512; for normal sector I/O, it must.
KD@BFU	DA@BM0	28	0-15	High-order bits of the address of the Buffer Memory data buffer. If more than one is necessary, this location is a pointer to a list of data buffers.
KD@BFL	DA@BM1	29	0-15	Low-order bits of the address of the Buffer Memory data buffer.
KD@LOC	DA@LOC	31	0-15	Address of the local buffer being used

DISK ACTIVITY LINK, MASTER (KD@/DA@)

The master Disk Activity Link is a message packet created by a request from the Cray mainframe. DALs also pass message information between I/O Processors that synchronizes activity within the I/O Subsystem. The first 8 parcels (0-7) contain the standard DAL header.

Label	Field	Parcel	Bits	Description
KD@DEST	DA@DID	8	0-15	Destination indicator. If this parcel contains an ASCII Cl, the MIOP recognizes the request as destined to the Cray mainframe. If it is set to an ASCII A, the request is for disk I/O.
KD@LFLG	DA@SID	9	0-15	Source ID. This is used for I/O requests that originate in the I/O Subsystem. If set to ASCII Cl, the request is for disk I/O.
KD@MSEQ	DA@SEQ	10	0-15	Number of executable DALs already set up
KD@DATL	DA@DAT	11	0-15	On a read request only, the number of reads completed
KD@TOTL	DA@TOT	12	0-15	Number of full sectors to be read or written in partial sector I/O
	DA@UNS	16	0-3	Number of physical units in striped group for which this unit is a member
	DA@TRQ	16	4-7	Number of requests sent to physical units for a striped group request
	DA@FRS	16	8-11	Number of final responses received from physical units for a striped group request
	DA@EFS	16	12-15	Number of early responses received from units for a striped group request. Applies to write requests only.
	DA@LCH	17	4-9	Logical channel number of striped group

Label	Field	Parcel	Bits	Description
	DA@LUE	17	10-15	Unit position of last unit with an error. Used for error reporting.
	DA@SQN	18	0-7	Sequence number of the striped group request
		18	8-15	Upper 8 bits of address in parcel 19 (total of 24 bits)
		19	0-15	Mainframe request identifier, used when status is returned to indicate to the mainframe which I/O request this packet defines. This field includes an address in Central Memory where I/O information is located.
KD@BPU	DA@CM0	20	0-15	High-order bits of the starting address in Central Memory of the source or destination of the data, depending on the function to be performed.
KD@BPL	DA@CM1	21	0-15	Low-order bits of the starting address in Central Memory of the source or destination of the data, depending on the function to be performed.
KD@CMD		22	0-15	Function and status codes
	DA@FC	22	0-7	One of the following function codes: 1 Read data 2 Write data 3 Read partial sector (internal function code) 4 Write partial sector (internal function code) 5 Read before write (internal function code) 7 Read from disk to specified Buffer Memory address 10 Write from Buffer Memory address to disk 12 Reserved

Label	Field	Parcel	Bits	Description
KD@CMD	DA@FC (continued)			
			14	Write and interrupt when data gets to Buffer Memory (write behind)
			21	Internal I/O; read from disk to Buffer Memory.
			22	Internal I/O; write from Buffer Memory to disk.
	DA@RC	22	8-15	Status returned by the I/O Subsystem to indicate success or failure of the request:
			0	Request completed successfully
			13_8	Corrected data error
			14_8	Uncorrected data error
			15_8	Unrecovered hardware error
KD@CHN		23	0-15	IOP and channel numbers
	DA@TYP	23	0-4	Device type
	DA@IOP	23	5-6	I/O Processor to which the request should be directed (BIOP is 1, IOP-2 is 2, and IOP-3 is 3)
	DA@CHN	23	7-15	Channel on which the I/O is to be performed
KD@HED		24	0-15	Cylinder and head numbers where I/O is to begin. On unrecovered errors, the cylinder and head of the error.
	DA@CYL	24	0-10	Cylinder number
	DA@HED	24	11-15	Head group for the I/O
KD@SEC		25	0-15	Sector number and, for partial sector I/O, the word offset from the beginning of the sector where data transfer begins. On unrecovered errors, the sector of the data in error.
	DA@SEC	25	0-6	Sector number
	DA@OFF	25	7-15	For partial sector I/O, the word offset from the beginning of the sector

Label	Field	Parcel	Bits	Description
KD@SZU	DA@LN0	26	0-15	High-order bits of the length of the I/O transfer in 64-bit words. If unrecovered error, high-order bits of size of successful transfer.
KD@SZL	DA@LN1	27	0-15	Low-order bits of the length of the I/O transfer in 64-bit words. For partial sector I/O, this value need not be a multiple of 512; for normal sector I/O, it must. If unrecovered error, low-order bits of size of successful transfer.
KD@BFU	DA@BM0	28	0-15	High-order bits of the address of the Buffer Memory data buffer. If more than one is necessary, this location is a pointer to a list of data buffers.
KD@BFL	DA@BM1	29	0-15	Low-order bits of the address of the Buffer Memory data buffer
	DA@WBH	31	0-15	Next write-behind sector sequence number

DISK CONTROL BLOCK TABLE (DCCB)

The Channel Control Block contains a pointer to a disk control block for each defined disk channel. The channel numbers are in octal. This table is used only by Kernel software executing in the BIOP or the DIOP.

Parcel	Bits	Description
0	0-15	Address of disk control block for channel 20
1	0-15	Address of disk control block for channel 21
2	0-15	Address of disk control block for channel 22
3	0-15	Address of disk control block for channel 23
4	0-15	Address of disk control block for channel 24
5	0-15	Address of disk control block for channel 25
6	0-15	Address of disk control block for channel 26
7	0-15	Address of disk control block for channel 27
10	0-15	Address of disk control block for channel 30
11	0-15	Address of disk control block for channel 31
12	0-15	Address of disk control block for channel 32
13	0-15	Address of disk control block for channel 33
14	0-15	Address of disk control block for channel 34
15	0-15	Address of disk control block for channel 35
16	0-15	Address of disk control block for channel 36
17	0-15	Address of disk control block for channel 37

DISK CONTROL BLOCK (DD@/DB@)

The Disk Control Block (DCB) contains a broad range of control information for disk operations. Each disk channel that is defined has a Disk Control Block. This table is used only by Kernel software executing in the BIOP or DIOP. The Channel Control Block (DCCB) contains a pointer to each of these tables.

Label	Field	Parcel	Bits	Description
DD@FLG	DB@FLG	0	0-15	Disk Activity flag; a bit, when set, indicates the corresponding activity is taking place on the channel.
			15	Read
			14	Write
			13	Read ahead
			12	Seek
	DBF@ER	0	11	Error recovery
	DBF@DS	0	10	Disabled, waiting for data or a local disk buffer
	DBF@RT	0	9	On an interrupt, disk interrupt answering immediately gives control back to the error recovery activity, which has been pushed on DCB parcels 34 and 35.
	DBF@CR	0	6	Disk interrupt answering signals the DISK demon to create ERRECK.
DD@NOW		1	0-15	Current cylinder and head
	DB@CYL	1	0-10	Cylinder
	DB@HED	1	11-15	Head
DD@EDL	DB@EDL	2	0-15	Executable DAL queue head; queue contains DALs to be executed FIFO for this channel.
	DB@EDT	3	0-15	Executable DAL queue tail
	DB@QLN	4	0-15	Executable DAL queue population
DD@MDL	DB@MDL	5	0-15	Master DAL queue head
	DB@MDT	6	0-15	Master DAL queue tail
DD@CHN		7	0-15	Disk type and channel
	DB@SEL	7	0-1	Select/deselect bits; if bit 0 is 1, disk is deselected; if 1 is 1, channel was used in the last quantum period.

Label	Field	Parcel	Bits	Description
	DB@TYP	7	2-6	Disk type: DSK$DD19 DSK$DD29
	DB@CHN	7	7-15	Channel number
DD@RAK	DB@RAK	8	0-15	Read ahead count constant, RA$NUM
DD@RAF	DB@RAF	9	0-15	Count of sectors read ahead for current request
DD@INF	DB@INF	10	0-15	Pointer to read ahead information, which follows the Disk Control Block
DD@SUC	DB@SUC	11	0-15	Count of times read request satisfied by data in read ahead buffer
DD@DNQ	DB@DNQ	12	0-15	Executable DAL done queue head; this queue is processed by the DISK demon.
	DB@DNT	13	0-15	Executable DAL done queue tail
	DB@RD0	14	0-15	Count of sectors read on disk unit (high-order)
DD@RDS	DB@RD1	15	0-15	Count of sectors read (low-order)
DD@ERS	DB@ERS	16	0-15	Count of errors on disk unit
DD@UNS	DB@UNS	17	0-15	Count of unrecoverable errors on disk unit
	DB@WR0	18	0-15	Count of sectors written on disk unit (high-order)
DD@WRS	DB@WR1	19	0-15	Count of sectors written (low-order)
		20	0-15	Unused

Label	Field	Parcel	Bits	Description
DD@EFLG	DB@EFL	21	0-15	Error Recovery flag defining type of error. 0 Interlock, disk not ready 1 Timed out by software 2 Seek failure 3 Read data error 4 Write data error 5 Seek error 6 Miscellaneous errors
		26	0-15	Unused
DD@ECYL		22	0-15	Cylinder and head of last error
	DB@ECY	22	0-10	Cylinder
	DB@EHD	22	11-15	Head
DD@ESEC	DB@ESC	24	0-15	Sector and offset of last error
DD@STAT	DB@STS	25	0-15	Original error status from which recovery is being attempted
DD@INLK	DB@INL	26	0-15	Interlock status
DD@DKA1	DB@DKA	27	0-15	Cylinder register status on a software-detected seek error
DD@POP	DB@PP0	28	0-15	First entry in push/pop cell for error recovery, when waiting for interrupt in response to recovery attempts
	DB@PP1	29	0-15	Last entry in push/pop cell
DD@TEMS	DB@TEM	30	0-15	Temporary disk status; status of interim error recovery attempts.
DD@DEM	DB@DEM	31	0-15	Disk demon link queue
DD@TMO	DB@TMO	32-35	0-15	Disk timer entry
DD@IN	DB@IN	36	0-15	Read ahead input pointer
DD@OUT	DB@OUT	37	0-15	Read ahead output pointer
DD@UNF	DB@UNF	38	0-15	Read ahead last pointer

The read-ahead information for a disk unit follows the Disk Control Block (DCB). An area is allocated for each sector to be read. Parcel 12 of the DCB points to the first read-ahead area, and parcel 10 contains a count of the number of areas allocated.

Field	Parcel	Bits	Description
RA@DAT	0	0-15	Flag indicating location of data: 0 On disk or in Central Memory 1 In Local Memory 2 In Buffer Memory
RA@CYL	1	0-10	Cylinder of sector to be read ahead
RA@HED	1	11-15	Head of sector to be read ahead
RA@SEC	2	0-6	Sector to be read ahead
RA@BM0	3	0-15	Address of data if in Buffer Memory (high-order)
RA@BM1	4	0-15	Address of data if in Buffer Memory (low-order)
RA@LOC	5	0-15	Address of data if in Local Memory

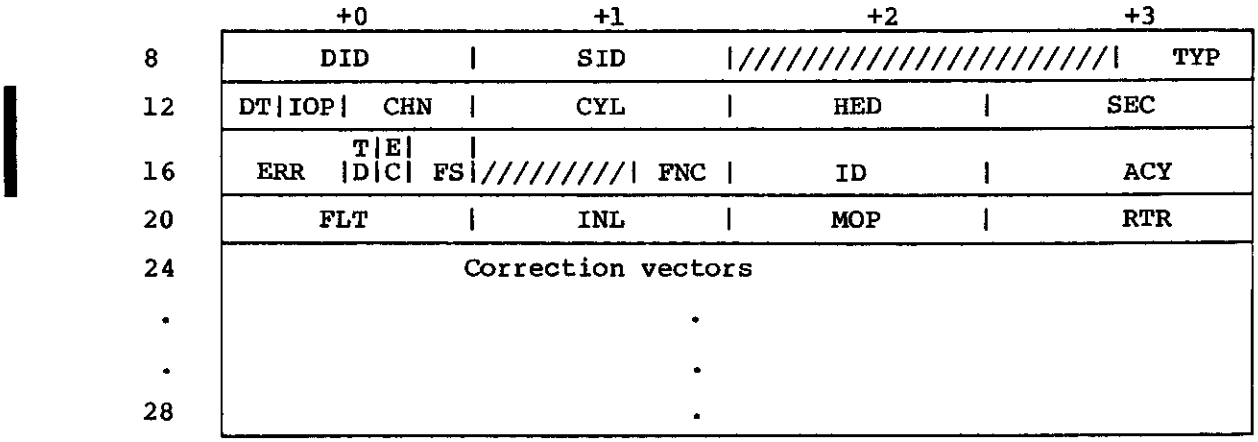
DISK DEMON QUEUE (DISKQ)

The disk demon queue contains the Disk Control Blocks (DCBs) for the disk units requesting services from the disk demon. The queue thread runs through the field DB@DEM in the DCB. This queue is used only by Kernel software executing in the BIOP or DIOP.

Label	Description
DISKQ	Address of first DCB on the queue. This is 0 if the queue is empty.
DISKQT	Address of the last DCB on the queue. This is 0 if the queue is empty.

DISK ERROR PACKET (DE@)

The REPORT overlay builds the disk error packet and sends it to the mainframe for logging. The first eight parcels (0-7) contain DAL control information.



Field	Parcel	Bits	Description
DE@DID	8	0-15	Destination ID
DE@SID	9	0-15	Source ID
DE@TYP	11	8-15	Packet type (2 = Disk error packet)
DE@DT	12	0-6	Device type: DSK$DD19 DSK$DD29
DE@IOP	12	7-9	IOP number
DE@CHN	12	10-15	Channel number
DE@CYL	13	0-15	Cylinder of request
DE@HED	14	0-15	Head group
DE@SEC	15	0-15	Sector number
DE@ERR	16	0-7	Error type: 0 Interlock 1 Timeout 2 ID error 3 Read data error 4 Write data error 5 Hardware-detected seek error 6 Miscellaneous

Field	Parcel	Bits	Description
DE@TD	16	8	Data transfer direction: 0 Write 1 Read
DE@EC	16	9	Error Correction flag: 0 Error correction not used 1 Error correction used
DE@FS	16	12-15	Final error status: DAR$REC Recovered DAR$COR Corrected DAR$UNC Uncorrected DAR$UNR Unrecovered
DE@FNC	17	12-15	Disk function in error:
		12	seek
		13	unused
		14	write
		15	read
DE@ID	18	0-15	Cylinder number from ID field, reported on an ID error
DE@ACY	19	0-15	Cylinder status register, reported on an ID error
DE@FLT	20	0-15	Original fault status
DE@INL	21	0-15	Interlock status
DE@MOP	22	0-15	Margin/Offset parameters
		0-8	Margin select: 0 Normal 1 Early 2 Late
		9-10	Offset direction: 0 Towards perimeter of disk 1 Towards center of disk
		11-15	Offset magnitude
DE@RTR	23	0-15	Retry count
DE@CV	24-31	0-15	Correction vector buffer; used by the FIRECODE overlay when attempting to correct a read data error.
	24-25	0-15	Correction vector 0
	26-27	0-15	Correction vector 1
	28-29	0-15	Correction vector 2
	30-31	0-15	Correction vector 3

DISK STRIPED GROUP DEVICE TABLE (BD@)

This table describes the striped group tables. The DCCB Table in MIOP contains pointers to these device tables based on their channel numbers.

Field	Parcel	Bits	Description
BD@TYP	0	0-15	Device type, LDV$DSK
BD@NUM	1	0-15	Number of units in group
BD@PUT	2	0-15	Address of physical unit table
BD@IQU	3-5	0-15	Input request queue
BD@HDS	6	0-15	Number of heads per cylinder of each physical unit
BD@SPT	7	0-15	Sectors per track
BD@SQN	8	0-7	Sequence number of last request

PHYSICAL UNIT TABLE (PUT@)

This table is pointed to by BD@PUT in the striped group device table (BD@).

Field	Parcel	Bits	Description
PUT@PN	0	8-9	Unit IOP number
PUT@CH	0	10-15	Unit channel number

ERROR LOG BUFFER TABLE (ERRBUFF)

The Error Log Buffer Table maintains the address of a 1000_8-word circular buffer in Buffer Memory that holds error log information. This table is used only by Kernel software executing in the MIOP.

Parcel	Bits	Description
0-1	0-15	Buffer Memory address of error log buffer
2	0-15	Current pointer in buffer

Each entry in the buffer is four parcels long and contains the following information:

Parcel	Bits	Description
0	0-15	Status
1	0-15	Error word
2-3	0-15	Address, either in Buffer Memory or Central Memory, where the error occurred

For a more detailed description of an entry, see the I/O Subsystem Reference Manual, CRI publication HR-0030.

ERROR LOG TABLE (ERRLOG)

The Error Log Table logs errors detected by the I/O Subsystem error detection logic in MIOP. This table is used only by Kernel software executing in the MIOP.

The table contains one entry for each of the following types of errors:

IOP0 Local Memory errors
IOP1 Local Memory errors
IOP2 Local Memory errors
IOP3 Local Memory errors
Central Memory errors (single bit)
Central Memory errors (multibit)
Buffer Memory single-bit memory errors
Buffer Memory multibit memory errors
High-speed channel 1 (input) errors
High-speed channel 1 (output) errors
High-speed channel 2 (input) errors
High-speed channel 2 (output) errors

For a more detailed description of an entry, see the I/O Subsystem Reference Manual, CRI publication HR-0030.

Table header:

Field	Parcel	Bit	Description
	0	0-15	Table identifier - ASCII ER
ER@FLG	1	0-15	0 = Logging enabled
ER@CNT	2	0-15	Count of errors logged since logging was last enabled
ER@TOT	3	0-15	Total number of errors logged

Table entry:

Field	Parcel	Bit	Description
ER@El1	0	0-15	Data from ERA:l1 instruction
ER@El2	1	0-15	Data from ERA:12 instruction if applicable

Field	Parcel	Bits	Description
ER@E13	2	0-15	Data from ERA:13 instruction if applicable
ER@NUM	3	0-15	Count of errors of this type

EXPANDER CHANNEL DEVICE TABLE (EXPDCT)

The Expander Channel Device Table is the control table for the printer, tape, and disk connected to the MIOP through the expander channel. This table is used only by Kernel software executing in the MIOP.

Printer table:

Field	Parcel	Bits	Description
XD@NAM	0	0-15	Device name (ASCII)
XD@UNT	1	0-15	Unit name (ASCII)
XD@DVN	2	0-15	Physical device number
XD@OVL	3	0-15	Overlay number
	4	0-15	Reserved
	5	0-15	Reserved
	6	0-15	Reserved
	7	0-15	Reserved
XD@USR	8	0-15	Device user activity address
XD@QUE	9	0-15	Device push queue
	10	0-15	Reserved
XD@OPR	11	0-7	Operator request
XD@OFF	11	8-11	Device On/off flag
	11	12-15	Reserved
XD@MOD	12	0-15	Device mode
XD@KEY	13	0-15	Device assignment key
XD@STT	14	0-15	Device status
XD@STB	15	0-15	B register
XD@STC	16	0-15	C register
XD@IPN	17	0-7	Interrupt Pending flag
XD@IRT	17	8-15	Interrupt Returned flag
	18	0-15	Reserved
PX@LIN	19	0-15	Current line number
PX@PLW	20	0-7	Paper Low flag
	21	8-15	Reserved

Tape table:

Field	Parcel	Bits	Description
XD@NAM	0	0-15	Device name (ASCII)
XD@UNT	1	0-15	Unit name (ASCII)
XD@DVN	2	0-15	Physical device number
XD@OVL	3	0-15	Overlay number
	4	0-15	Reserved
	5	0-15	Reserved
	6	0-15	Reserved
	7	0-15	Reserved
XD@USR	8	0-15	Device user activity address
XD@QUE	9	0-15	Device push queue
	10	0-15	Reserved
XD@OPR	11	0-7	Operator request
XD@OFF	11	8-11	Device On/off flag
	11	12-15	Reserved
XD@MOD	12	0-15	Device mode
XD@KEY	13	0-15	Device assignment key
XD@STT	14	0-15	Device status
XD@STB	15	0-15	B register
XD@STC	16	0-15	C register
XD@IPN	17	0-7	Interrupt Pending flag
XD@IRT	17	8-15	Interrupt Returned flag
MX@FLN	18	0-15	Current file number
MX@OPN	19	0-15	Just Opened flag
MX@LFC	20	0-15	Last function code
MX@RLN	21	0-15	Record length returned
MX@LNG	22	0-15	Record length requested

Disk table:

Field	Parcel	Bits	Description
XD@NAM	0	0-15	Device name (ASCII)
XD@UNT	1	0-15	Unit name (ASCII)
XD@DVN	2	0-15	Physical device number
XD@OVL	3	0-15	Overlay number
DX@MC	4	0-15	Cylinders per disk
DX@MH	5	0-15	Heads per cylinder
DX@MB	6	0-15	Blocks per head
DX@MS	7	0-15	Sectors per block
XD@USR	8	0-15	Device user activity address
XD@QUE	9	0-15	Device push queue
	10	0-15	Reserved
XD@OPR	11	0-7	Operator request
XD@OFF	11	8-11	Device On/off flag
	11	12-15	Reserved
XD@MOD	12	0-15	Device mode
XD@KEY	13	0-15	Device assignment key
XD@STT	14	0-15	Device status
XD@STB	15	0-15	B register
XD@STC	16	0-15	C register
XD@IPN	17	0-7	Interrupt Pending flag
XD@IRT	17	8-15	Interrupt Returned flag
	18	0-15	Reserved
DX@CYL	19	0-15	Cylinder number
DX@HD	20	0-15	Head number

Field	Parcel	Bits	Description
DX@SCT	21	0-15	Sector number
DX@LFC	22	0-15	Last function code

I/O BUFFER CHAIN DESCRIPTOR (EBUF)

The I/O buffer chain descriptor contains a linked list of available I/O buffers in Local Memory. Each buffer is 512 words long.

Parcel	Bits	Description
0	0-15	Pointer to first entry in I/O buffer chain
1	0-15	Pointer to last entry in I/O buffer chain
2	0-15	Population count of I/O buffers in chain
3	0-15	Maximum population of chain

I/O PROCESSOR ID TABLE (EIDA)

Each I/O Processor contains a single-parcel table to hold the processor number. Values from 0 to 3 are legal. After deadstart, the ID is also kept in Kernel register R!%MYID.

Parcel	Bits	Description
0	0-15	Identifying number for this I/O Processor: 0 MIOP 1 BIOP 2 IOP-2 3 IOP-3

IMMEDIATE MESSAGE QUEUE (MIMMQ)

Messages that are completely contained in the accumulator are queued in the immediate message queue for processing by the AMSG overlay.

Parcel	Bits	Description
0	0-15	Beginning of queue area
1	0-15	End of queue area
2	0-15	Pointer to current entry
3	0-15	Next entry to fill
4	0-15	Number of entries in use
5	0-15	Error count
6-45	0-15	Queue body. Each entry contains the 16 bits of information passed across the accumulator channel from another IOP.

IMMEDIATE TAPE REQUESTS QUEUE (TIMQU)

TIMQU is the DAL queue for bypass activity.

Parcel	Bits	Description
0-1	0-15	Wait queue
2-4	0-15	DAL queue

INPUT CHANNEL TABLE (CPI@)

This table shows the input channel from the mainframe to the MIOP.

Field	Parcel	Bits	Description
CPI@ON	0	0	Input channel on if set
CPI@CN	0	7-15	Input channel number
CPI@ST	1	0-15	Last input channel status
CPI@CA	2	0-15	Last input channel address
CPI@DA	3	0-15	Active input DAL address
CPI@PQ	4-6	0-15	Input channel poll queue
CPI@CQ	7-9	0-15	Input channel demon (CDEM) queue
CPI@DP	10	0-15	Disk request population
CPI@UI	11	0-15	Unexpected interrupts

OUTPUT CHANNEL TABLE (CPO@)

This table shows the output channel from the MIOP to the mainframe.

Field	Parcel	Bits	Description
CPO@ON	0	0	Output channel on if set
CPO@DS	0	1	Mainframe deadstart in progress if set
CPO@LK	0	2	Initialization in progress if set
CPO@CN	0	7-15	Output channel number
CPO@ST	1	0-15	Last output channel status
CPO@CA	2	0-15	Last output channel address
CPO@DA	3	0-15	Active output channel DAL
CPO@QU	4-6	0-15	Output channel queue of DALs to send
CPO@TM	7-10	0-15	Output channel timer entry

IOP MESSAGE CHANNEL QUEUES FOR ACOM (MAAQ)

Each I/O Processor has an entry in this table to queue the input requests from other I/O Processors for processing by the ACOM overlay.

Parcel	Bits	Description
0	0-15	MIOP message queue address in Local Memory
1-2	0-15	Address of Buffer Memory area (high-order and low-order bits) for MIOP
3	0-15	MIOP input channel
4	0-15	BIOP message queue address in Local Memory
5-6	0-15	Address of Buffer Memory area (high-order and low-order bits) for BIOP
7	0-15	BIOP input channel
10	0-15	DIOP message queue address in Local Memory
11-12	0-15	Address of Buffer Memory area (high-order and low-order bits) for DIOP
13	0-15	DIOP input channel
14	0-15	XIOP message queue address in Local Memory
15-16	0-15	Address of Buffer Memory area (high-order and low-order bits) for XIOP
17	0-15	XIOP input channel

IOP MESSAGE CHANNEL QUEUES FOR BCOM (MBAQ)

This table serves as a queue for input requests from other I/O Processors to be processed by the BCOM overlay.

Parcel	Bits	Description
0	0-15	MIOP message queue address in Local Memory
1	0-15	Address of Buffer Memory area (high-order and low-order bits) for MIOP
3	0-15	MIOP input channel
4	0-15	BIOP message queue address in Local Memory
5-6	0-15	Address of Buffer Memory area (high-order and low-order bits) for BIOP
7	0-15	BIOP input channel
10	0-15	IOP-2 message queue address in Local Memory
11-12	0-15	Address of Buffer Memory area (high-order and low-order bits) for IOP-2
13	0-15	IOP-2 input channel
14	0-15	IOP-3 message queue address in Local Memory
15-16	0-15	Address of Buffer Memory area (high-order and low-order bits) for IOP-3
17	0-15	IOP-3 input channel

IOP TO CHANNEL CONVERSION TABLE (MATX)

This table translates logical I/O Processor identifiers into channel numbers. It is initialized by overlay SYSS to reflect its own channel configuration.

Parcel	Bits	Description
0	0-15	For MIOP, contains a value of 6 to translate BIOP to channel 6
1	0-15	For MIOP, contains a value of 10_8 to translate DIOP to channel 10_8
2	0-15	For MIOP, contains a value of 12_8 to translate XIOP to channel 12_8

KERNEL CENTRAL PROCESSOR QUEUE (ECPQ)

The IOP central processor queue for the Kernel is a linked list of Activity Descriptors that are eligible to run. They are ordered according to priority, with the smallest number signifying the highest priority.

Parcel	Bits	Description
0	0-15	Address of the head of the IOP central processor queue
1	0-15	Last entry in the queue

KERNEL INTERRUPT JUMP TABLE (EITB)

Each entry contains the address of the routine to process the interrupts on a different channel. The table is ordered by channel number. Channels 40-47 are not handled by the Interrupt Jump Table. The table is set initially for the MIOP configuration and is initialized by SYSS in other I/O Processors.

Parcel	Bits	Description
n	0-15	Interrupt-handling routine for channel *n*

LOCAL MEMORY BLOCK HEADER (MD@)

This header precedes each block of memory in the Local Memory overlay space. The block following may be the header for the overlay space, the trailer for the overlay space, memory available for assignment, or an overlay. The parcel numbers for this table are in decimal.

Field	Parcel	Bits	Description
MD@ID	0	0-15	Header identifier: MD$ID (ASCII MD)
MD@SUC	1	0-15	Adjacent block list forward pointer
MD@PRE	2	0-15	Adjacent block list backward pointer
MD@TYP	3	0-15	Block type: MD$HEAD Header or trailer entry MD$FREE Available for assignment MD$OLAY Overlay area† MD$BUF Buffer space†
MD@FOR	4	0-15	Memory search list forward pointer
MD@BAK	5	0-15	Memory search list backward pointer
MD@OVT	6	0-15	Address of Overlay Table entry if MD@TYP = MD$OLAY
MD@LEN	8	-	Equate defining length of table

† Deferred implementation

LOCAL MEMORY FREE CHAIN (EMEM)

This is a linked list of areas of Local Memory available for allocation. Areas are ordered by size, with the smallest size coming first. If two sizes are equal, the lowest address is first.

Parcel	Bits	Description
0	0-15	First entry on chain
1	0-15	Last entry on chain
2	0-15	Size of free memory at initialization

OUTPUT QUEUE POINTER TABLE (MAOQ)

The Output Queue Pointer Table contains a pointer to the IOP output message queue in Local Memory for each I/O Processor.

Parcel	Bits	Description
0	0-15	Output queue pointer for MIOP
1	0-15	Output queue pointer for BIOP
2	0-15	Output queue pointer for DIOP (0, if no DIOP)
3	0-15	Output queue pointer for XIOP (0, if no XIOP)

Queue format:

A queue exists for each channel handling communications between I/O Processors. This queue controls output messages to each processor and consists of accumulator values sent to the receiving processor when the channel becomes available. The queue is set up in Local Memory by the system initialization in the MIOP; an entry in the table MAOQ points to it. Each table takes the following form:

Parcel	Bits	Description
0	0-15	Beginning of queue area
1	0-15	End of queue area plus one
2	0-15	First entry in current list
3	0-15	First entry in empty list (next to be filled)
4	0-15	Number of entries in use
5	0-15	Errors and problems
6	0-15	Help flag: 0 Queue is not full Nonzero Queue is full, channel is disabled
7	0-15	Channel busy flag: 0 Channel is inactive Nonzero Channel is busy

Parcel	Bits	Description
10	0-15	Head of queue for waiting activities
11	0-15	Tail of queue for waiting activities
12	0-15	Queue entries
⋮		
n		

OVERLAY TABLE ENTRY (OT@)

The Overlay Table contains an entry for each defined overlay. Each entry holds information used by the Kernel when its associated overlay is called.

Field names SM@NUM and SM@FST define subfields within OT@PAR and do not have parcel attributes. That is, they are for use with the RGET and RPUT macros rather than the GET, PUT, and STORE family of macros.

Field	Parcel	Bits	Description
OT@WRD	0	0-11	Overlay length in words
OT@MUP	0	12-15	High-order bits of overlay address in Buffer Memory
OT@MLO	1	0-15	Low-order bits of overlay address in Buffer Memory
OT@PAR	2	0-15	Parameter register descriptor:
SM@NUM	-	0-6	Number of registers
SM@FST	-	7-15	First operand register
OT@LOC	3	0-15	Overlay address in Local Memory; 0 if not resident.
OT@LEN	4	-	Equate defining length of entry

POPCELL CHAIN DESCRIPTOR (MPOPCELL)

This 2-parcel descriptor points to the popcell chain. Popcells are set up when an ALERT message is processed from another I/O Processor. An Activity Descriptor is associated with each popcell. When the activity owning the popcell does a RETURN, which terminates its activity, the popcell is removed from the chain and its memory is deallocated.

Parcel	Bits	Description
0-1	0-15	Pointer to chain of popcells

SOFTWARE STACK POINTERS (ESCR and ESMD)

These pointers locate the software stack area in Local Memory and the scratch area in which a software stack is set up for a CREATE service request.

Parcel	Bits	Description
0	0-15	Pointer to software stack scratch area
1	0-15	Pointer to software stack area

STORAGE MODULE (SM@)

A storage module saves information relating to the operating environment of an overlay.

Each overlay is assigned a storage module when it executes. When the overlay temporarily surrenders control, the contents of relevant registers and other necessary information are loaded into the SMOD. Once the overlay regains control, values from the SMOD are restored to enable the overlay to continue execution with the correct operating environment.

Field names SM@NUM and SM@FST define subfields within SM@REG and do not have parcel attributes. That is, they are for use with the RGET and RPUT macros rather than the GET, PUT, and STORE family of macros.

The parcel numbers are given in decimal.

Field	Parcel	Bits	Description
SM@ACT	0	0-15	Activity address
SM@PRE	1	0-15	Link to previous SMOD (0 if this is the first)
SM@LEN	2	0-15	Size of this SMOD in parcels
SM@CAL	3	0-15	Overlay ID of caller (address of entry in Overlay Table)
	4-5	0-15	Unused
SM@A	6	0-15	Accumulator contents
SM@B	7	0-15	B register contents
SM@C	8	0-15	Carry flag
SM@E	9	0-15	Exit stack pointer
SM@P	10	0-15	(E) relative to base address
SM@REG	11	0-15	Operand register descriptor:
SM@NUM		0-6	Number of operand registers saved
SM@FST		7-15	First operand register saved

Field	Parcel	Bits	Description
SM@SAV	12 - *n*	0-15	Operand registers (177_8 maximum)
	n+1 - *n*+E	0-15	Exit stack (addresses relative to base address)
	n+E+1	0-15	Global registers (appended to the software stack only when the software stack must be swapped to Buffer Memory)

TAPE DEMON QUEUE OF REQUESTS (BXQQ)

Requests are placed on this queue for BMXDEM.

Parcel	Bits	Description
0	0-15	Queue address
1	0-15	Pointer to end of queue
2	0-15	Pointer to current entry in queue
3	0-15	Number of entries in use
4	0-15	Error count
5-24	0-15	Queue body; one entry each for 16 channels.

TDEM0 READ REVERSE REQUEST QUEUE (BYQQ)

This queue is the request queue for the read reverse data handler.

Parcel	Bits	Description
0	0-15	First entry in queue
1	0-15	Last entry in queue
2	0-15	Current entry in queue
3	0-15	Next entry in queue
4	0-15	Number of entries in queue
5	0-15	Overflow count
6-13	0-15	Queue body

TDEM1 PUSH QUEUE (TDMQ)

This queue is where TDEM1 waits to be called by BCOM.

Label	Parcel	Bits	Description
TDMQ	0-1	0-15	Push queue

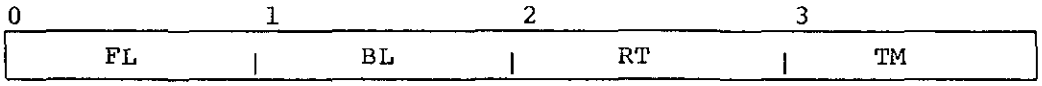
TIMER QUEUE HEADER (RTCQUE)

RTCQUE is the base of the system event timer queue. All events currently being timed are linked to RTCQUE. See TMR@.

Parcel	Bits	Description
0	0-15	Forward Link
1	0-15	Backward Link

EVENT TIMER ENTRY (TMR@)

The event timer entry is used to link onto the event timer queue (RTCQUE) in order to regain control if an expected event does not occur within a specified amount of time.



Field	Parcel	Bits	Description
TMR@FL	0	0-15	Forward queue link. Maintained by timer.
TMR@BL	1	0-15	Backward queue link. Maintained by timer.
TMR@RT	2	0-15	Timeout handler routine address. Set by creator of entry. Specifies where to go if time expires.
TMR@TM	3	0-15	Time quantum in tenths of a second. Maintained by timer.

TRACE CONTROL TABLE (TLOC)

The Trace Control Table is used by the trace package to determine the events to trace and where to store the information.

Parcel	Bits	Description
0	0-15	Address of local buffer
1	0-15	High-order bits of Buffer Memory address of buffer
2	0-15	Low-order bits of Buffer Memory address of buffer
3	0-15	Local Memory pointer
4	0-15	Buffer Memory pointer
5	0-15	Buffer Memory buffer write control
6-11	0-15	Event code bit map; if a bit is set to 0, do not trace the corresponding event. Initially the map is set to all ones.
12-15	0-15	Channel bit map; if a bit is set to 0, do not trace for the corresponding channel. Initially the map is set to all ones.
16-22	0-15	Function bit map; if a bit is set to 0, do not trace the corresponding function. Initially the map is set to all ones.
23-33	0-15	Temporary storage

CONCENTRATOR TABLES (LM@/DT@) 3

The tables and descriptors in this section are used by the I/O Subsystem concentrator. The concentrator tables are used in the MIOP only. Tables in this section are defined in terms of 64-bit words and the word numbers are given in decimal.

CONCENTRATOR TABLE (CT$ID)

The Concentrator Table is a Kernel-resident table containing addresses and information used by one or more I/O Subsystem concentrators. This table is used only by Kernel software executing in the MIOP. The Concentrator Table is of variable size. Its size is determined at assembly time by the number of concentrators and the maximum number of logical IDs to be logged on. The following representation assumes two concentrators, referred to as concentrator 0 and concentrator 1, and a maximum of eight logical IDs.

Parcel	Bits	Description
0	0-15	ASCII constant ID. This constant is used to help find this location in a dump.
1-40	0-15	Table of logged on IDs. Each logical ID (this example assumes that eight can be logged on) has a 4-parcel entry. Parcels 1 through 4 following are repeated through parcel 40; therefore, only the first 4-parcel entry (parcels 1-4) and the last (37-40) are included in this table description.
1	0-15	Unused
2	0-15	2-character ID
3-4	0-15	Buffer Memory address of Descriptor Table
37	0-15	Unused
38	0-15	2-character ID
39-40	0-15	Buffer Memory address of Descriptor Table

Parcel	Bits	Description
41	0-15	ASCII constant MQ. This constant helps find this location in a dump.
42	0-15	Queue address for MSGIO in the BIOP
43	0-15	ASCII constant CQ. This constant helps find this location in a dump.
44	0-15	Address of the queue that interfaces between CONCI and CONCO for concentrator 0
45	0-15	Address of the queue that interfaces between CONCI and CONCO for concentrator 1
46	0-15	ASCII constant MC. This constant helps find this location in a dump.
47	0-15	Concentrator 0 message count of packets going over the 6 Mbyte channel. When it reaches 377, the count starts over at 0.
50	0-15	Concentrator 1 message count of packets going over the 6 Mbyte channel
51	0-15	ASCII constant RQ. This constant helps find this location in a dump.
52-53	0-15	Queue for concentrator 0 onto which the Kernel pushes FEREAD while it awaits input
54-55	0-15	Queue for concentrator 1 onto which the Kernel pushes FEREAD while it awaits input
56	0-15	ASCII constant WQ. This constant helps find this location in a dump.
57-60	0-15	Queue for concentrator 0 onto which the Kernel pushes FEWRIT while it awaits output
61-62	0-15	Queue for concentrator 1 onto which the Kernel pushes FEWRIT while it awaits output
63	0-15	ASCII constant IC. This constant helps find this location in a dump.
64	0-15	Physical input channel for concentrator 0
65	0-15	Physical input channel for concentrator 1

Parcel	Bits	Description
66	0-15	ASCII constant LM. This constant helps find this location in a dump.
67	0-15	Local Memory address of buffer area allocated to concentrator 0
70	0-15	Local Memory address of buffer area allocated to concentrator 1
71	0-15	ASCII constant MO. This constant helps find this location in a dump.
72	0-15	Message ordinal assigned to concentrator 0
73	0-15	Message ordinal assigned to concentrator 1

DESCRIPTOR TABLE

The Descriptor Table contains pointers that locate the address in Local Memory of the descriptor for each input and output stream.

Field	Word	Bits	Description
LM@CKZ	0	8-15	Checksum size
LM@MIS	0	16-23	Maximum number of input streams
LM@MOS	0	24-31	Maximum number of output streams
LM@MAS	0	32-39	Maximum number of active streams
LM@MSS	0	40-47	Maximum number of subsegments
LM@SSG	0	48-63	Subsegment size
LM@LID	1	0-15	Logical ID
DT@IST0	2	32-63	Input stream pointer; Buffer Memory address of the descriptor for stream 0.
DT@IST1	3	32-63	Input stream pointer; Buffer Memory address of the descriptor for stream 1.
DT@IST2	4	32-63	Input stream pointer; Buffer Memory address of the descriptor for stream 2.
DT@IST3	5	32-63	Input stream pointer; Buffer Memory address of the descriptor for stream 3.
DT@IST4	6	32-63	Input stream pointer; Buffer Memory address of the descriptor for stream 4.
DT@IST5	7	32-63	Input stream pointer; Buffer Memory address of the descriptor for stream 5.
DT@IST6	8	32-63	Input stream pointer; Buffer Memory address of the descriptor for stream 6.
DT@IST7	9	32-63	Input stream pointer; Buffer Memory address of the descriptor for stream 7.
DT@IST8	10	32-63	Input stream pointer; Buffer Memory address of the descriptor for stream 8.
DT@OST0	11	32-63	Output stream pointer; Buffer Memory address of the descriptor for stream 0.

Field	Word	Bits	Description
DT@OST1	12	32-63	Output stream pointer; Buffer Memory address of the descriptor for stream 1.
DT@OST2	13	32-63	Output stream pointer; Buffer Memory address of the descriptor for stream 2.
DT@OST3	14	32-63	Output stream pointer; Buffer Memory address of the descriptor for stream 3.
DT@OST4	15	32-63	Output stream pointer; Buffer Memory address of the descriptor for stream 4.
DT@OST5	16	32-63	Output stream pointer; Buffer Memory address of the descriptor for stream 5.
DT@OST6	17	32-63	Output stream pointer; Buffer Memory address of the descriptor for stream 6.
DT@OST7	18	32-63	Output stream pointer; Buffer Memory address of the descriptor for stream 7.
DT@OST8	19	32-63	Output stream pointer; Buffer Memory address of the descriptor for stream 8.

STREAM DESCRIPTOR (SD@)

The stream descriptor contains information relative to a streaming operation, including the addresses of data in Buffer Memory. Each stream descriptor must be fully contained within one 512-word Buffer Memory block. Each stream descriptor must be large enough to contain pointers for an entire segment.

Field	Word	Bits	Description
SD@NSS	0	0-7	Number of subsegments
SD@ENT	0	8-15	Number of entries (*n*) in stream descriptor
SD@OFF	0	16-31	Offset to first word used in first buffer
SD@MBD	0	32-63	Buffer Memory data bit count
SD@USE	1	0-15	Number of words used in last buffer
SD@ADR	2-*n*	32-63	Buffer Memory buffer addresses

NSC ACTIVITY TABLES 4

The following tables and their descriptions are used by the NSC activity.

FRONT-END CHANNEL ORDINAL RESERVATION TABLE (COR@)

The COR tables are created at system initialization time. There is one COR table for each of the maximum number of front ends concurrently logged on through all NSC Adapter channels.

Field	Parcel	Bits	Description
COR@AC	0	0	Active flag
COR@OF	0	1	Ordinal Off flag
COR@OR	0	8-15	FE ordinal
COR@ID	1	0-15	Assigned NID table

FRONT-END CHANNEL INFORMATION TABLE (FEI@)

The FEI tables are created at system initialization time. One FEI table is created for each physical channel pair configured as a front-end interface.

Field	Parcel	Bits	Description
Header:			
FEI@TN	0	0-15	ASCII identifier
FEI@ON	1	0-15	FE channel ordinal table
Entry:			
FEI@AC	0	0	Channel Active flag
FEI@II	0	1	Initialization in progress
FEI@TM	0	2	Termination in progress
FEI@OF	0	3	Channel Off flag
FEI@VA	0	4	VAX-A adapter type
FEI@VB	0	5	VAX-B adapter type
FEI@CT	0	8-15	Channel type (CH$..)
FEI@CO	1	1-6	Channel ordinal
FEI@CH	1	8-15	Physical channel (input)
FEI@TB	2	0-15	NSCIO table
FEI@TR	3	0-15	Timeout handler address

INPUT STATUS BUFFER (NSB@)

This table describes the input status buffer used to read status from the NSC AI30 adapter. The status buffer is physically a part of the NIO Table (NIO@IB).

Field	Parcel	Bits	Description
NSB@ST	0	0-7	Error status field
*	0	0-1	Unused
NSB@CP	0	2	Cray parity error
NSB@RA	0	3	Receiver abort
NSB@MR	0	4	Message received
NSB@OA	0	5	Operation aborted
NSB@FR	0	6	Function reject
NSB@PE	0	7	Parity errror
NSB@LF	0	8-15	Last function code
NSB@NT	1	0	No trunks available
NSB@IT	1	1	Internal timeout
NSB@RR	1	2	Response reject
NSB@DC	1	3	Data check word
NSB@TP	1	4	Trunk parity error
NSB@RE	1	5	256 retries
NSB@TR	1	6	Transmitter reject
NSB@IR	1	7	Invalid response
NSB@T0	1	8	Trunk 0 available
NSB@T1	1	9	Trunk 1 available
NSB@T2	1	10	Trunk 2 available
NSB@T3	1	11	Trunk 3 available
NSB@HF	1	12	Header fail

Field	Parcel	Bits	Description
NSB@TT	1	13	Trunk timeout
NSB@BR	1	14	Buffer and control reserved
NSB@TV	1	15	Trunk reserved
NSB@RJ	2	0	Reject
NSB@BZ	2	1	Busy
NSB@TS	2	2	Trunk reserve
NSB@DR	2	3	Device reserve
NSB@FG	2	4	Flag reject
NSB@IF	2	5	Illegal function received
NSB@DE	2	6	Data check error
NSB@SB	2	7	Sequence bit
*	2	8	Unused
NSB@MI	2	9	Message received
NSB@NC	2	10	Normal completion
NSB@AB	2	11	Abnormal completion
*	2	12-15	Unused
NSB@CA	3	0-7	Compressed address
NSB@EC	3	8-15	Error code (values in hex):

NSE$ACT (1)	Adapter receiving or assigning data
NSE$ICL (2)	Incorrect message length
NSE$NSA (3)	No space to input data
NSE$BTB (6)	Data block too big
NSE$IFC (7)	Illegal function code
NSE$PRS (A)	Not enough parameters
NSE$TMP (B)	Too many parameters
NSE$NED (C)	Not enough data sent
NSE$TMD (D)	Too much data sent
NSE$DAC (E)	Data accepted by Cray mainframe

Field	Parcel	Bits	Description
NSB@EC (continued)			NSE$CDE (F) Cray mainframe read too much data NSE$NMQ (10) No message queued for Cray mainframe NSE$CRQ (12) Cray mainframe quit early during DMA NSE$APE (13) Parity error from adapter to Cray mainframe NSE$TTA (14) Trunk transmission error NSE$DRV (15) Device reserved to adapter NSE$TTR (16) Trunk retries exhausted NSE$ADS (17) Adapter failed to send assigned data NSE$PFC (18) Parity error from Cray mainframe IOS detected error codes: NSE$TMO (376) Timeout NSE$CHE (377) IOS detected channel error

MESSAGE PROPER (MP@)

This table describes the Message Proper, which is used for communication between trunks on the NSC A130 Adapter. The Message Proper is physically a part of the NIO Table (NIO@MP).

Field	Parcel	Bits	Description
MP@TRT	0	0-3	Trunks to try (transmit)
MP@TRR	0	4-7	Trunks to try (receive)
*	0	8-11	Unused
MP@EXC	0	13	Exception message
MP@BUR	0	14	Burst mode
MP@AD	0	15	Associated data
MP@ACC	1	0-15	Access data
MP@DID	2	0-15	Destination address
MP@SID	3	0-15	Source address
*	4-7	0-15	Unused
MP@LCP	8-31	0-15	LCP

NSC FRONT-END ID TABLE (NID@)

The NSCID tables are created by the NSCIO routine when an NSC channel is initialized. There is one table created for each of the maximum number of front ends concurrently logged on through all NSC adapter channels.

Field	Parcel	Bits	Description
NID@ID	0	0-15	Logical FE ID
NID@AC	1	0	NID active flag
NID@LO	1	1	FE-initiated logoff flag
NID@TM	1	2	Termination in progress flag
NID@XF	1	3	Transfer in progress
NID@OR	1	8-15	Assigned FE ordinal
NID@TB	2	0-15	NSCIO table address
NID@FE	3	0-15	FEI table pointer
NID@OM	4-7	0-15	Message Proper routing word
NID@CT	8	0-15	Concentrator table address
NID@MC	9	0-15	Message count
NID@WL	10-11	0-15	NSCIO write link

NSCIO TABLE DEFINITION (NIO@)

The NSCIO Table is the control table for I/O between the IOS and an A130 NSC Adapter. The table is created by the NSC routine when an NSC channel is initialized.

Field	Parcel	Bits	Description
NIO@IB	0-3	0-15	Status input buffer
NIO@OB	4-7	0-15	Function output buffer
NIO@MP	8-15	0-15	Message Proper header
NIO@LC	16-39	0-15	LCP (part of Message Proper)
NIO@MQ	40-42	0-15	Wait-for-message queue
NIO@AQ	43-44	0-15	Wait-for-interrupt queue
NIO@WC	45-46	0-15	Write request queue
NIO@HC	47	0-15	Collision counter (hard)
NIO@SC	48	0-15	Collision counter (soft)
NIO@EC	49	0-15	Error counter
NIO@WM	50	0	Wait for message flag
*	50	1-7	Unused
NIO@CH	50	8-15	Input channel number
NIO@CA	51	0-15	Current channel address
NIO@ST	52	0-15	Channel status
NIO@TM	53-56	0-15	NSC I/O timer entry

WRITE REQUEST LINK (NWC@)

This table describes the NIO@WC write request queue and NID@WL write request links.

Field	Parcel	Bits	Description
NWC@FL	0	0-15	Forward link
NWC@BL	1	0-15	Back link

OUTPUT FUNCTION BUFFER (NFB@)

This table describes the output function buffer, used to send functions to the NSC A130 Adapter. This buffer is physically a part of the NIO Table (NIO@OB).

Field	Parcel	Bits	Description
*	0-2	0-15	Unused
*	3	0-7	Unused
NFB@FC	3	8-15	Function code:

NFB$TM	05	Transmit message
NFB$TD	09	Transmit data
NFB$TLD	0D	Transmit last data
NFB$TLM	11	Transmit local message
NFB$IM	25	Input message
NFB$ID	29	Input data
NFB$ST	41	Read status
NFB$DX	51	Dump extension registers
NFB$RS	A1	Read statistics
NFB$RCS	A5	Read and clear statistics
NFB$SE	C1	Set test
NFB$WB	C5	Set address and length
NFB$RB	C9	Read buffer
NFB$CA	E1	Clear adapter
NFB$EO	E5	End operation
NFB$WFM	E9	Wait for message

STATION TABLES (C$) 5

The I/O Subsystem station software uses information from the tables described in this section. Station tables are defined with decimal parcel or word numbers.

CONSOLE DRIVER TABLE

This table is used by the station tasks doing console output. It is addressed by the global register %STCON.

Field	Parcel	Bits	Description
C$MOSU	0	0-15	Buffer Memory address of screen image buffer (high-order bits)
C$MOSL	1	0-15	Buffer Memory address of screen image buffer (low-order bits)
C$TYPE	2	0-15	Console type: CF$455 TEC 455 CF$SOROC SOROC IQ 120 CF$AMPEX AMPEX Dialogue 80
C$DEV	3	0-15	Device address (0-3)
C$LBO	4	0-15	Line buffer byte offset
C$COL	5	0-15	Column number of cursor address
C$LINE	6	0-15	Line number of cursor address
C$CLIN	7	0-15	Command line number
C$SCRL	8	0-15	First line of the scroll area
C$LOCK	9-11	0-15	Console interface interlock (LOCK, UNLOCK macros)
C$LBUF	12-*n*	0-15	Driver scratch storage
C$IBUF	*n*+1	0-15	Driver scratch storage through *m*

CONSOLE SUPPORT TASKS SHARED MEMORY ($C@/$D@/$F@/$L@/$T@/$R@/$B@)

This memory is shared by the tasks KEYBD, CLI, and DISPLAY. It is addressed by the global register %CLI.

Field	Parcel	Bits	Description
$C@DEV	0	0-15	Device address
$C@TYP	1	0-15	Device type
$C@CPL	2	0-15	Characters per line
$C@LST	3	0-15	Last display line
$C@DIS	4	0-15	Display starting line number
$C@CNT	5	0-15	Display line count
$D@TYP	6	0-15	Current display type
$D@OD	7	0-15	Old display type
$D@OVL	8	0-15	Active display overlay number
$D@FRM	9	0-15	Display frame number
$D@QUE	10	0-15	Display Queue flags
$D@LFT	11	0-15	Debug display left descriptor
$D@RGT	12	0-15	Default debug mode
$D@MOD	13	0-15	Debug display right descriptor
$D@TSK	14	0-15	Default COS task number
$D@JOB	15	0-15	Default JSQ number
$D@IOP	16	0-15	Current IOP designator
$D@JTN	17	0-15	Job task number
$D@INT	18	0-15	Default refresh rate
$D@MON	19	0-15	Local memory address for MONITOR
$D@SCI	20	0-15	Display scroll interval
$D@SCT	21	0-15	Display scroll timer

Field	Parcel	Bits	Description
$D@PAR	22	0-15	Optional display parameters, parameter 1
$D@P2	23	0-15	Optional display parameters, parameter 2
$D@P3	24	0-15	Optional display parameters, parameter 3
$D@P4	25	0-15	Optional display parameters, parameter 4
$D@GRN	26-29	0-15	Current generic resource name
$D@NST	30	0-15	NSC table address
$D@NSA	31	0-15	NSC request type (0=local/1=remote)
$F@FLG	32	0-15	Flag bits
$F@PSE		3	Command File Paused flag
$F@FIL		4	Command file open flag
$L@DIS	33-35	0-15	Display interface interlock
$T@KEY	36-38	0-15	Keyboard task termination queue
$T@DIS	39-41	0-15	Display task termination queue
$R@CLI	42-44	0-15	CLI keyboard input activation queue
$R@DIS	45-47	0-15	Display task queue
$D@DEB	48-151	0-15	Debug display descriptors
$B@CF	152-174	0-15	Command file buffer
$B@CB	175-177	0-15	Input circular buffer
$B@DIS	200-517	0-15	Display stack
$B@CLI	518-710	0-15	CLI stack

DEBUG DISPLAY DESCRIPTOR (DD@)

This descriptor contains the information to be displayed for one of the 26 debug displays.

Field	Parcel	Bits	Description
DD@CHR	0	0-4	Display character minus the ordinal value of an ASCII A, leaving a value of between 0 and 25
DD@DEF	0	5	Default Ordinal flag: DO$DEF Use default ordinal $D@TSK or $D@JOB
DD@INF	0	7-9	Information type: DI$B B registers DI$T T registers DI$V V registers DI$MEM Memory DI$XP Exchange package
DD@FOR	0	10-12	Display format: DF$WORD Word DF$PAR Parcel DF$FP Floating-point DF$INS Instruction DF$XP Exchange package
DD@MOD	0	13-15	Display mode: DM$DEF Use default mode $D@MOD DM$EXEC COS Executive DM$TASK COS task DM$JOB COS job DM$IOP IOP DM$MOS Buffer Memory
DD@ORD	1	0-15	Job sequence number or task number
DD@ADU	2	0-15	Memory address or register number (high-order bits)
DD@ADL	3	0-15	Memory address or register number (low-order bits)

I/O STREAM CONTROL TABLE (IO@)

The I/O Stream Control Table is used for STAGEIN-PROTOCOL and STAGEOUT-PROTOCOL task communications.

Field	Parcel	Bits	Description
IO@NUM	0	0-15	Stream number
IO@FLG	1	0-15	Stream state: 0 Not active Nonzero Active
IO@SGN	2	0-15	Current segment number
IO@SBC	3	0-15	Segment bit count
IO@SGU	4	0-15	Message segment Buffer Memory address (high-order bits)
IO@SGL	5	0-15	Message segment Buffer Memory address (low-order bits)
IO@MES	6	0-15	Message LCP descriptor address (offset into overlay LCP)
IO@FC	7	0-15	Input stream function code (defined in overlay UPDATE): ISF$OPEN Open stream ISF$WRIT Send dataset segment to mainframe ISF$END Close stream ISF$PPN Postpone dataset transfer ISF$CAN Cancel output stream function code; dataset transfer. OSF$READ Read dataset segment OSF$SVD Close stream OSF$PPN Postpone dataset transfer OSF$CAN Cancel dataset transfer
IO@STA	8	0-15	Stream state (see TR@STA†)
IO@CRA	9	0-15	Mainframe state (see TR@VAL†)
IO@RES	10	0-15	Response code (see IOC@RC†)

† Refer to I/O Stream State Transition Table entry.

Field	Parcel	Bits	Description
IO@QUE	11,12	0-15	PUSH queue used while waiting for response from PROTOCOL task
IO@JOB	13-16	0-15	Name of job associated with staged dataset
IO@DN	17-20	0-15	Dataset name
IO@SIZ	21	0-15	Dataset size in 512-word blocks
IO@FM	22	0-15	Dataset format
IO@DC	23	0-15	Disposition code
IO@DCT	24	0-15	Device control table address
IO@DEV	25	0-15	Device type
IO@KEY	26	0-15	Device access key
IO@OPT	27	0-15	Device specific options
IO@VOL	28-31	0-15	Volume ID (ASCII)
IO@DIR	32-39	0-15	Directory ID (ASCII)
IO@FIL	40-47	0-15	File name (ASCII)
IO@DOC	48-51	0-15	Printer document name (ASCII)

I/O STREAM STATE TRANSITION TABLE ENTRY (TR@/IOC@/IOS@)

The State Transition Table generates a new stream state based on the current state and the response SCB. Each table entry consists of two parcels.

Field	Parcel	Bits	Description
TR@VAL	0	0-15	Validation and mainframe state information; 177777_8 if the end of the table.
TR@STA	1	0-15	Next state

After TR@VAL or TR@STA is read into an operand register, subfields may be referenced using the RGET and RPUT macros.

Field	Parcel	Bits	Description
IOC@BT	NA	0-11	Received SCB validation bit map 0 MCL 1 CAN 2 PPN 3 SVD 4 SVG 5 END 6 SUS 7 RCV 8 SND 9 PTR 10 RTS 11 IDL
IOC@IO	NA	13	Mainframe I/O state (input stream only): 0 Not ready for data 1 Ready to receive segment
IOC@RC	NA	14-15	Input stream response code: 0 None ISR$OK Request processed ISR$PPN Postpone transfer ISR$CAN Cancel transfer Output stream response code: 0 None OSR$OK Request processed OSR$END END SCB received OSR$CAN Cancel transfer

Field	Parcel	Bits	Description
IOS@SB	NA	0-3	Stream control byte to send to the mainframe
IOS@IO	NA	4	Stream I/O state: 0 No I/O 1 Message to be sent or received
IOS@AV	NA	5	Stream availability: 0 Stream available for assignment 1 Stream unavailable
IOS@TB	NA	6-15	State transition table address (offset into overlay UPDATE)

KEYBOARD COMMAND TABLE ENTRY (CK@)

Each entry in the Keyboard Command Table defines a valid operator command.

Field	Parcel	Bits	Description
CK@OVL	0	0-15	Number of the overlay used to process command. This field contains 177777_8 if it is the end of the table.
CK@PAR	1	0-15	Parameter associated with command
CK@MIN	2	0-7	Minimum number of characters required to match against CK@KEY
CK@LEN	2	8-15	Byte length of CK@KEY
CK@KEY†	3-*n*	0-15	Command keyword

† Field is defined with CFIELD macro instead of FIELD macro and is not accessible to GET and PUT macros.

KEYBOARD INPUT CIRCULAR BUFFER (CB@)

The keyboard buffer holds characters entered at the station console.

Field	Parcel	Bits	Description
CB@IN	0	0-15	Input character byte offset (relative to the start of the buffer CB@IN)
CB@OUT	1	0-15	Output character byte offset
CB@FST	2	0-15	Byte offset of first character in CB@BUF
CB@LST	3	0-15	Byte offset of last character in CB@BUF
CB@BUF†	4-23	0-15	Input character buffer

† Field is defined with CFIELD macro instead of FIELD macro and is not accessible to GET and PUT macros.

LCP DESCRIPTOR TABLE (DO@)

The LCP descriptor generates or validates the link control package for a message.

Field	Parcel	Bits	Description
DO@MC	0	0-15	Message code
DO@SBC	1	0-15	Segment bit count source: ET$NONE None ET$STREM From IO@SBC in Stream Control Table ET$SPEC From DO@VAL: 100_8 > SGBC > DO@VAL (validation only) ET$VALUE From DO@VAL
DO@VAL	2	0-15	Segment bit count value, if required; it is 0 otherwise.
DO@STN	3	0-15	Stream number source: ET$NONE None ET$STREM From IO@NUM in Stream Control Table
DO@MSC	4	0-15	Message subcode processing (validation only): ET$NONE None ET$SPEC Validate MSC and map to a response code

OPERATOR STREAM CONTROL TABLE (OP@)

The Operator Stream Control Table is used for CLI-PROTOCOL and DISPLAY-PROTOCOL task communications.

Field	Parcel	Bits	Description
OP@FLG	0	0-15	Status flag: 0 Inactive 1 Request for message to be sent 2 Message being processed
OP@GEN	1	0-15	Send message LCP descriptor address (offset into overlay LCP)
OP@VER	2	0-15	Response message LCP descriptor address (offset into overlay LCP)
OP@SGB	3	0-15	Send message/response segment bit count
OP@SGU	4	0-15	Send message/response Buffer Memory address (high-order bits)
OP@SGL	5	0-15	Send message/response Buffer Memory address (low-order bits)
OP@RES	6-8	0-15	Queue used while waiting for response message (WATCH, SIGNAL macros)

PROTOCOL TASK LOCAL MEMEORY (PT@)

This Local Memory area, allocated by the PROTOCOL task, is addressed by the global register %PROT.

Field	Parcel	Bits	Description
PT@MN	0	0-15	Mainframe interface message number
PT@IST	1-9	0-15	Buffer Memory offsets for the input stream descriptor tables; 0 if stream is not defined. The first entry is for the operator stream.
PT@OST	10-18	0-15	Buffer Memory offsets for the output stream descriptor tables; 0 if stream is not defined.
PT@PAN	19	0-15	Response word for acquire request; this is used if another request is being processed.
PT@PHI	20	0-15	Buffer Memory address of secondary acquire request segment (high-order bits)
PT@PLO	21	0-15	Buffer Memory address of secondary acquire request segment (low-order bits)
PT@XST	22	0-15	Acquire processing state: 0 No request being processed 1 Request active
PT@XAN	23	0-15	Response word for primary acquire request
PT@XHI	24	0-15	Buffer Memory address of primary acquire request segment (high-order bits)
PT@XLO	25	0-15	Buffer Memory address of primary acquire request segment (low-order bits)
PT@STK	26	0-15	PROTOCOL task stack area
PT@TAB	27-*n*	0-15	I/O Stream Control Tables; one for each defined input and output stream.

S PACKET - STATISTICS (PKT$)

Mainframe answers a statistics request with this packet.

Label	Parcel	Description
	0	Destination (DAD@DIO)
	1	Source (DA@SID)
	2-10	Unused
PKT$SYS	11	Percentage of mainframe time used by operating system
	12-14	Unused
PKT$IDL	15	Percentage of mainframe time idle
	16-18	Unused
PKT$USR	19	Percentage of mainframe time taken by users
	20-22	Unused
PKT$BLK	23	Percentage of mainframe time blocked

STATION MESSAGE MAP ENTRY (MP)

The STMSG overlay makes an entry in the station message map when it receives a station message from the mainframe. The map holds 64 entries of two 64-bit words each. An entry is removed when a reply is returned. The station message map is cleared and messages are released during logoff.

Field	Word	Bits	Description
MPUSE	0	0	Flag signaling entry in use
MPFP	0	16-23	Forward pointer in chain of entries
MPBP	0	24-31	Backward pointer in chain of entries
MPBMU	0	32-47	High-order bits of message address in Buffer Memory
MPBML	0	48-63	Low-order bits of message address in Buffer Memory
MPRRQ	1	0	Reply required flag
MPOLD	1	1	Flag signaling that message was received on previous day
MPVUD	1	2	Flag signaling that message was already viewed
MPURG	1	3	Flag signaling an urgent message
MPPRI	1	16-19	Priority of message
MPWC	1	24-31	Word count of message
MPMN	1	32-47	Message number
MPTIM	1	48-63	Time message was received

STATION SHARED BUFFER MEMORY (W@)

This Buffer Memory buffer is shared by the station tasks. The address is stored in the SS@HI and SS@LO fields of the station-shared Local Memory.

Field	Word	Bits	Description
W@OLCP	0-15	0-63	Output link control package
W@ILCP	6-11	0-63	Input link control package
W@DSTB	12-31	0-63	I/O Descriptor Table (DSTB)
W@STREAM	32-*n*	0-63	Stream Descriptor Tables; one for each defined input and output stream.

STATION-SHARED LOCAL MEMORY (SS@)

This memory is shared by the station tasks. It is addressed by the global register %STAT.

Field	Parcel	Bits	Description
SS@NUM	0	0-15	Count of active consoles
SS@ORD	1	0-15	Ordinal for station channel
SS@HI	2	0-15	Buffer Memory buffer address (high-order bits)
SS@LO	3	0-15	Buffer Memory buffer address (low-order bits)
SS@ID	4	0-15	Station ID
SS@TID	5-8	0-15	Station terminal ID
SS@DID	9	0-15	Default station ID
SS@DTI	10-13	0-15	Default station TID
SS@IST	14	0-15	Input stream count
SS@OST	15	0-15	Output stream count
SS@AST	16	0-15	Active stream count
SS@RET	17	0-15	Message retry count
SS@POL	18	0-15	Message poll interval
SS@IN	19	0-15	First Input Stream Control Table
SS@OUT	20	0-15	First Output Stream Control Table
SS@FRE	21	0-15	Number of message slots free
SS@MMX	22	0-15	Maximum number of station messages per segment
SS@SMC	23	0-15	Station message chain start
SS@CHN	24	0-15	End of message chain index
SS@RQM	25	0-15	Reply requested message count
SS@LCP	26	0-15	LCP buffer

Field	Parcel	Bits	Description
SS@SML	27	0-7	New station message limit
SS@MN	27	8-15	Current message number
SS@MPX	28	0-15	Message map index
SS@FLG	29	0-15	Flag bits
SS@IQ	30	0-15	Queuing flag
SS@QST	31	0-15	Queue status
SS@QHI	32	0-15	Buffer Memory address of dataset header (high-order bits)
SS@QLO	33	0-15	Buffer memory address of dataset header (low-order bits)
SS@QKY	34	0-15	Device access key
SS@QAQ	35	0-15	Acquire flag
SS@QDV	36	0-15	Input device
SS@QBK	37	0-15	Blocking flag
SS@QDR	38-45	0-15	Disk directory name
SS@QFL	46-53	0-15	Tape file number/disk file name
SS@QCC	54	0-7	Blocking control character
SS@QNR	54	8-15	No Rewind flag
SS@OP	55-57	0-15	Operator message interlock
SS@MSG	58-60	0-15	Station message interlock
SS@PRO	61-63	0-15	Protocol task queue
SS@REQ	64-66	0-15	Protocol task activiation
SS@TAB	67-127	0-15	Stream table

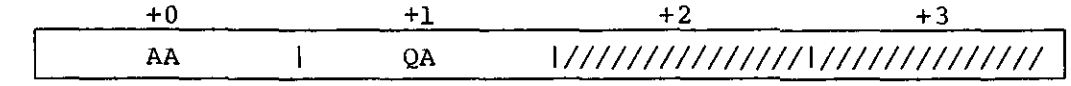
Field	Parcel	Bits	Description
SS@PRO	57-59	0-15	Communication area for PROTOCOL task
SS@REQ	60-63	0-15	Task request communication area for PROTOCOL task activation
SS@TAB	64-*n*	0-15	Operator Stream Control Table
SS@SIZ	*n*+1	0-15	Amount of shared memory required

BLOCK MULTIPLEXER TABLES 6

The following tables are used by the block multiplexer channel software. Parcel numbers for tables in this section are given in decimal.

ALTERNATE ACTIVITY TABLE (PRW@)

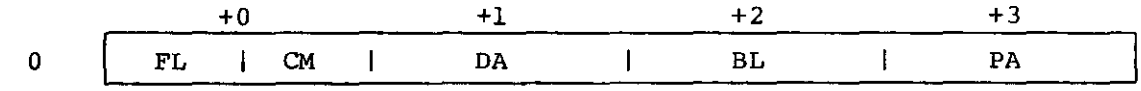
The Alternate Activity Table (PRW@) is set up by the device activity as an appendum to the CPW interface. It contains information necessary to activate an activity to handle the movement of data during a data transfer. A pointer to the PRW is entered in each CPW for which the activity is to be activated (CPW@PA).



Field	Parcel	Bits	Description
PRW@AA	0	0-15	Activity address. This field contains the activity descriptor address of the activity to be activated.
PRW@QA	1	0-15	Queue address. This field contains the address of a queue where the address of the CRW associated with the device is placed.

CHANNEL PROGRAM WORD (CPW@)

The Channel Program Word is an external table used to communicate between a BMX device driver and the BMX channel driver. The CPW control flags contain information as to the structure and processing of a CPW list.



Field	Parcel	Bits	Description
CPW@FL	0	0-7	Channel flags

Control flags:

FL$CC		0-7	Command chain. Command chaining specifies that when ending status is received for the current command, processing of the next CPW in the list should begin immediately. Command chaining is sustained if no abnormal status conditions are encountered.
FL$CD	0	6	Chain data. Chain data is only valid for commands which cause data to be transferred. It is used when a single buffer cannot contain all of the data to be transferred. Chain data specifies that the next CPW is a continuation of the current one and contains the necessary information to sustain the data transfer after the current buffer has been exhausted. The continuation CPWs are termed control words.
FL$ID	0	5	Indirect address. The indirect address flag indicates that the current CPW contains a pointer to a circular list of control words to be used to sustain a data transfer. This flag is valid only in conjunction with data transfer commands. The control word list pointers are contained in the CPW@DA (Top of List) and CPW@BL (Bottom of List) in the current CPW.

Field	Parcel	Bits	Description
CPW@CM	0	8-15	Command. The command field contains the physical command to be issued to the device. A single exception is the transfer-in channel command (CM$TIC), which is a software command indicating that the current CPW is a pointer to another CPW to be processed. The pointer is located in the CPW@DA field of the CPW. The CM$TIC command is used to form CPW loops. See section 4 for an example.

The command field is not valid for control word CPWs.

All BMX device commands are formed by adding modifier bits to the following set of channel commands:

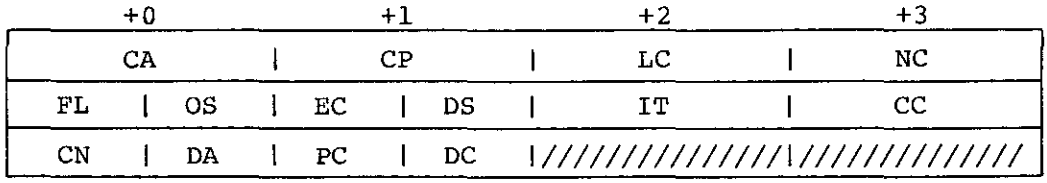
CM$WRT	(1)	Write
CM$RD	(2)	Read
CM$NO	(3)	No-op
CM$SNS	(4)	Sense
CM$TIC	(10)	Transfer-in-channel
CM$RDR	(14)	Read Reverse

Field	Parcel	Bits	Description
CPW@DA	1	0-15	Data address. This field contains the buffer address (must be on word boundary) for the current data transfer with the following two exceptions: If indirect address flag (FL$ID) is set, this field points to the head of a circular control word list. If the command (CPW@CM) is a TIC (transfer-in channel), this field contains a pointer to the CPW to be processed.
CPW@BL	2	0-15	Byte length. This field contains the byte count for the data buffer (CPW@DA) with the following exception: If the indirect address flag (FL$ID) is set, this field points to the tail of the circular control word list.

Field	Parcel	Bits	Description
CPW@PA	3	0-15	Alternate activity. This field, when nonzero, contains a pointer to an Activity Descriptor and queue address for an activity that is to be activated to process data during a data transfer.

CHANNEL RESPONSE WORD (CRW@)

This table is used as a communication area between the BMX channel driver and a device activity. Physically, the CRW exists as a header to each Device Control Table.



Field	Parcel	Bits	Description
CRW@CA	0	0-15	Current CPW address. This field contains the current CPW address. Initially, this field is set by the device activity upon starting I/O. Once I/O has started, the BMX channel driver updates the field to reflect the current CPW being processed.
CRW@CP	1	0-15	Command CPW address. This field is maintained by the BMX channel driver. It contains the address of the CPW from which the current command was issued.
CRW@LC	2	0-15	Last CPW address. This field contains the address of the last CPW processed. It is used by the data handler on reads to determine the buffer length and address of the last data transferred.
CRW@NC	3	0-15	Next CPW address. This field contains the address of the next CPW to be processed. It is used by the data handler on writes to determine the buffer length and address to be filled for the next transfer.
CRW@FL	4	0-7	Flags:
FL$CUA		0	Control unit assign. This flag is set by the device activity and indicates that the device path for the current I/O is to be the same as the one used on the last I/O.

Field	Parcel	Bits	Description
FL$CUS		1	Control unit switch. This flag is set by the device activity to indicate that the device path for the current I/O is to be different from the one used on the previous I/O.
FL$RDY		2	Buffer ready. This flag is used to detect software overrun conditions. The flag is set by the data handler activity each time a buffer of data is processed. The flag is checked and cleared by the BMX channel interrupt handler. If the flag is not set when the interrupt handler is ready to switch buffers, a software overrun condition is detected.
CRW@OS	4	8-15	Operation status. This field contains the operation status returned from the BMX channel driver to the device activity.
OS$IP	(1)		Interrupt pending on ending status
OS$BZ	(2)		I/O in progress
OS$DN	(3)		Ending status received; no abnormal status exists.
OS$ER	(4)		Abnormal status condition exists.
OS$IE	(5)		Interface error. Previously completed control list has not been updated.
CRW@EC	5	0-7	Error code. This field contains error code information received from the Channel Table (CHT@EC).
ES$DBI	(1)		Double interrupt. Two interrupts have occurred and have been processed since the data handler last executed.

Field	Parcel	Bits	Description
ES$SOR	(2)		Software overrun. The device activity or the data handler fell behind the channel during a chained data transfer.
ES$CHE	(3)		Channel error. A channel error was detected from the input tags received from the last interrupt.
ES$DTO	(4)		Device timeout. The device activity did not receive control from the current I/O within the allotted time.
ES$CTO	(5)		Channel timeout. An interrupt was not received from the channel within the allotted time.
ES$BRE	(6)		Byte count register error. The count in the byte count register did not match the expected value.
ES$DRE	(7)		Data register error. One of the data buffer address registers did not contain the expected value.
CRW@DS	5	8-15	Device status. This field contains the last hardware status returned from the device, which is copied from the channel table (CHT@DS).
CRW@IT	6	0-15	Input tags. This field contains the input tags received on the last interrupt.
CRW@CC	7	0-15	Record count. This field is incremented by the BMX channel driver at the completion of each data transfer command.
CRW@CN	8	0-7	Channel number. This field contains the number of last channel used to issue I/O to the device.
CRW@DA	8	8-15	Device address. This field contains the physical address of the path last used to issue I/O to the device.

Field	Parcel	Bits	Description
CRW@PC	9	0-8	Previous command. This field contains the last physical command issued to the device.
CRW@DC	9	8-15	Device ordinal. This field contains the logical device ordinal assigned to the device.

CHANNEL TABLE (CHT@)

Each BMX channel configured has a Channel Table associated with it.

	+0	+1	+2	+3
0	NC	CO	NP	NI
4	BU	BL	CF	CL
8	C1	IT	DS	Flags | CN
12	EC | RI	CR	RA	////////////

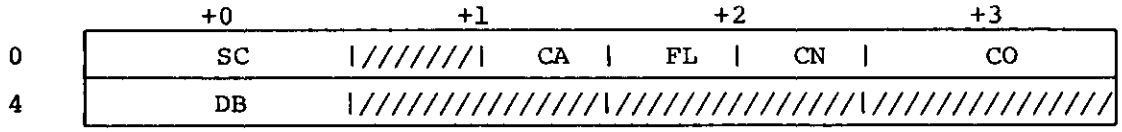
Field	Parcel	Bits	Description
CHT@NC	0	0-15	Channel link. The channel link is used when placing the Channel Table on the BMX channel driver queue (XCIQ).
CHT@CO	1	0-15	Channel owner. This field, when nonzero, contains the address of the control unit table to which the channel is assigned.
CHT@NP	2	0-15	Sequence code. This field contains the current channel program sequence code. KIC$IR (0) Immediate return from interrupt KIC$SC (1) Start command chain KIC$AC (2) Advance command chain KIC$AD (3) Advance data chain KIC$SR (4) Start request-in sequence KIC$CR (5) Continue request-in sequence KIC$ER (6) End request-in sequence KIC$WI (7) Wait for next interrupt
CHT@NI	3	0-15	Next CPW address. This field contains the address of the CPW from which the interrupt handler finds the buffer address and length to continue a data transfer.
CHT@BU	4	0-15	Channel byte count. This field is incremented by the number of bytes transferred following each interrupt during a data transfer.
CHT@BL	5	0-15	

Field	Parcel	Bits	Description
CHT@CF	6	0-15	Channel wait queue. This queue is used by device activities to wait for the channel to become available.
CHI@CL	7	0-15	Second parcel of channel wait queue
CHT@Cl	8	0-15	Control unit chain. This field contains a pointer to the first control unit table in the chain for a control unit attached to the channel.
CHT@IT	9	0-15	Input tags. This field contains the last input tags received from the channel.
CHT@DS	10	0-15	Device status. This field contains the last device status received during I/O on the channel.
CHT@FL	11	0-7	Control flags:
CHT@UP		0	Up/down. This flag indicates the current configured state of the channel. If set, the channel is down.
CHT@ZZ		1	Configuration. This flag is used by BMXCPU during configuration to mark the channel processed.
CHT@DN		2	Channel done. This flag indicates the state of the channel done flag at the time of the last interrupt.
CHT@BZ		3	Channel busy. This flag indicates the state of the channel busy flag at the time of the last interrupt.
CHT@CN	11	8-15	Channel number. This field contains the physical channel number with which the table is associated.
CHT@EC	12	0-7	Error code. This field contains a channel or software-detected error code. See CRW@EC.
CHT@RI	12	8-15	Request-in count. This field contains a count of the number of request-in interrupts pending on the channel.

Field	Parcel	Bits	Description
CHT@CR	13	0-15	CRW address. This field contains the CRW address associated with the current or last device to which I/O was performed from the channel.
CHT@RA	14	0-15	Request-in address. This field contains the physical device address from the last request-in sequence processed on the channel.

CONTROL UNIT TABLE (CUT@)

There is a Control Unit Table (CUT@) assigned to each configured control unit.

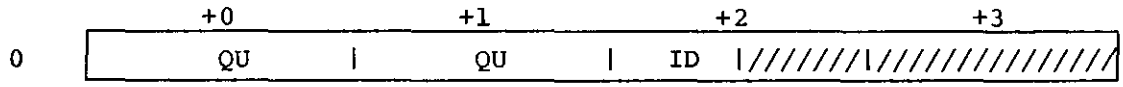


Field	Parcel	Bits	Description
CUT@SC	0	0-15	Link to next Control Unit Table. This field contains a pointer to the next Control Unit Table in the chain of control units that begins at the channel (CHT@Cl).
CUT@CA	1	8-15	Control unit address. This field contains the physical 4-bit, left-justified address of the control unit.
CUT@FL	2	0-7	Control flags:
CUT@UP		0	Up/down flag. This flag indicates the configured state of the control unit. If clear, the control unit is up. If set, the control unit is down.
CUT@ZZ		1	Configuration flag. This flag is used by BMXCPU during configuration to detect that the control unit has been processed once.
CUT@NA		2	Not available. This flag, when set, indicates that the control unit is not available for assignment due to the channel being down.
CUT@BZ		3	Control Unit Busy flag. This flag, when set, indicates that the control unit is not available for assignment due to a control unit busy status. This flag clears when control unit end status is returned.

Field	Parcel	Bits	Description
CUT@CN	2	8-15	Channel. This field contains the number of the channel to which the control unit is connected.
CUT@CO	3	0-15	Control unit owner. This field, when nonzero, contains the address of the device table to which the control unit is assigned.
CUT@DB	4	0-15	Device bank. This field contains the address of the Device Bank Table associated with the Control Unit Table.

CONTROL-UNIT BANK TABLE (CBT@)

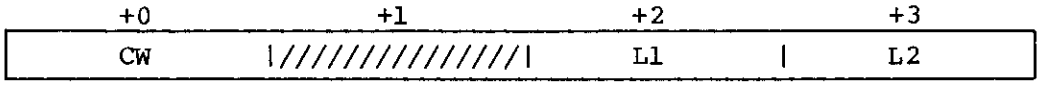
The Control-unit Bank Table contains a list of pointers to the Control Unit Tables which comprise the bank. The list is preceded by a header containing the following:



Field	Parcel	Bits	Description
CBT@QU	0	0-15	Bank queue. The Control-unit Bank queue is where device activities are suspended while waiting for one of the control units in the bank to become available for assignment.
	1	0-15	
CBT@ID	2	0-7	Bank ID. This field contains the logical ID of the bank assigned at configuration time.

CONTROL WORD LIST HEADER (IAW@)

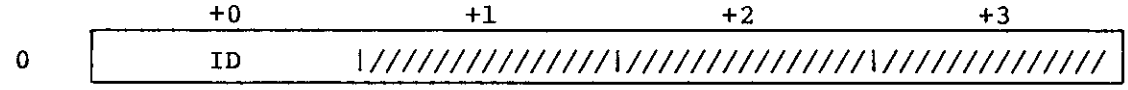
Each indirect address control word list is preceded by a header (IAW@).



Field	Parcel	Bits	Description
IAW@CW	0	0-15	Control word. This field contains control flags used to maintain validity checks on the control word list. Control flags:
CW@DN		0	List done. This flag is set after the list has been completed for the command. It is checked prior to starting a data transfer using the list, and, if set, causes an error (OS$IE) to be returned to the device activity.
CW@WR		1	Wrap flag. The Wrap flag is set prior to the advance from the last control word in a list to the first. The device activity is reactivated to update the list. If the Wrap flag is still set when the BMX channel driver is ready to process the first control word, a software overrun condition is detected and the error is returned to the device activity.
IAW@L1	2	0-15	Record length (upper)
IAW@L2	3	0-15	Record length (lower). This field contains the current bytes transferred for the control word list. This field is cleared at the start of the I/O transfer and is updated as each transfer between the device and a buffer from the list completes.

DEVICE BANK TABLE (DBT@)

The Device Bank Table consists of a header followed by a list of device tables associated with the devices in the bank.



Field	Parcel	Bits	Description
DBT@ID	0	0-15	Bank ID. This field contains the logical ID for the bank.

DEVICE TABLE (BDV@)

Each configured device has an associated BMX Device Table.

	+0	+1	+2	+3
0	DT | DO |///////| UN |////////////|			CB
4	DS |///////|	flags	AI	CR
8	////////////|	TQ	TQ	LC

Field	Parcel	Bits	Description
BDV@DT	0	0-7	Device type. This field contains the type of device being driven. Currently, tape is the only device type supported.
BDV@DO	0	8-15	Device ordinal. This field contains the logical device ordinal assigned at configuration time.
BDV@UN	1	8-15	Device path. This field contains the physical address of the last path used to issue I/O to the device. The field consists of a 4-bit control unit address followed by a 4-bit device address.
BDV@CB	3	0-15	Control unit bank. This field contains a pointer to the Control-unit Bank Table associated with the device.
BDV@DS	4	0-7	Device status. This field contains the last hardware status received from the device.
BDV@FL	5		Flag word
BDV@CM	5	0-1	Channel mode. This field contains the channel mode or interface type used between the channel and control unit.

Field	Parcel	Bits	Description
BDV@CT	5	2-3	Command type. This field contains the command type of the last command issued to the device. CTY$IN (1) Data input CTY$OUT (2) Data output CTY$CTL (3) Control
BDV@OS	5	4-7	Operation status. This field contains the last operation status for the device. See CRW@OS.
BDV@RI	5	8	Request-in pending. This field is set when a request-in interrupt is pending for the device. It is cleared when the interrupt is received.
BDV@ER	5	9	Error. This field is set when an error status is received from the device. It is cleared when a sense command is issued.
BDV@NR	5	9	Not ready. This field is set when the device is armed to return an interrupt caused by manual intervention.
BDV@RS	5	10	Restart CPW. This field is cleared to indicate that the current CPW is being restarted due to an encountered busy status.
BDV@UP	5	11	Device up. This field is set to indicate that the device has been configured up.
BDV@AI	6	0-15	Device owner. This field contains the activity descriptor address of the activity that the device is open to.
BDV@CR	7	0-15	CRW address. This field contains the address of the CRW associated with the device.

Field	Parcel	Bits	Description
BDV@TQ	9	0-15	Task queue. The device activity suspends itself on the device task queue while waiting for the I/O to complete.
BDV@LC	11	0-15	Last control unit. This field contains a pointer into the Control-unit Bank Table that points to the control unit used on the last I/O to the device.

TAPE EXEC TABLES 7

The Tape Exec tables provide data definitions for magnetic tape support. They are part of the XIOP software. The parcel numbers for tables in this section are in decimal.

BLOCK OR RECORD CONTROL WORD DESCRIPTION (CW@)

This table is used for both block and record control words. The format for a block control word is as follows:

Field	Parcel	Bits	Description
CW@MOD	0	0-3	Control word type: MD$BCW (0) Block control word MD$EOR (10) End-of-record MD$EOF (16) End-of-file MD$EOD (17) End-of-data
CW@DBF	0	11	Bad Data flag. When set, specifies that a data error occurred while reading the data between this control word and the next.
CW@NUL	0	12	Null Data flag. When set, specifies the end of valid data in the sector.
CW@BL0	1	15	High-order bit of block number
CW@BL1	2	0-15	Block number continued
CW@BL2	3	0-6	Low-order bits of block number
CW@FWI	3	7-15	Forward index. The number of words of data between this control word and the next.

The format for a record control word follows.

Field	Parcel	Bits	Description
CW@MOD	0	0-3	Mode: MD$BCW (0) Block control word MD$EOR (10) End-of-record MD$EOF (16) End-of-file MD$EOD (17) End-of-data
CW@UBC	0	4-9	Unused bit count. The unused bit count is a count of number of bits in the last word of the record that is not data. For tapes, this count is always a byte multiple.
CW@DBF	0	11	Bad Data flag
CW@PFU	1	4-15	High-order bits of previous field index. This is a count of the number of 512-word blocks previous to the current one in the current file.
CW@PFL	2	0-7	Low-order bits of previous field index. This is a count of the number of 512-word blocks previous to the current one in the current file.
CW@PRU	2	8-15	High-order bits of previous record index. This is a count of the number of 512-word blocks previous to the current one in the current record.
CW@PRL	3	0-6	Low-order bits of previous record index. This is a count of the number of 512-word blocks previous to the current one in the current record.
CW@FWI	3	7-15	Forward index. The number of words of data between this control word and the next.

DATA STREAM CONTROL TABLE (CU@/NX@/BF@)

XIOP area:

	+0	+1	+2	+3
0	TOP	BTM	PTR	BPT
4	NCW	Control word for BCW and RCW information		
8	BCW/RCW info.	ERU	ERL	BKP
12	VMS	TMS	////////////////////////////	

BIOP area:

	+0	+1	+2	+3
0	TOP	BTM	PTR	BPT
4	TPU	TPL	BKP	////////////

Buffer list:

	+0	+1	+2	+3
0	ADU	ADL	STA RLU	RLL/LNG
⋮		⋮		
n	ADU	ADL	STA RLU	RLL/LNG

XIOP area:

Parcels 5 through 8 of the XIOP area constitute a control word. This word contains the next BCW/RCW information to be written if the operation is an interchange read.

Field	Parcel	Bits	Description
CU@TOP	0	0-15	Top of buffer list. This is an offset from the top of the DSC to the first buffer descriptor available.
CU@BTM	1	0-15	Bottom of buffer list. This is an offset from the top of the DSC to the last buffer descriptor available.
CU@PTR	2	0-15	Current descriptor pointer. This is an offset from the top of the DSC to the next buffer descriptor to use.
CU@BPT	3	0-15	Offset into the current buffer where the next data is to be moved

Field	Parcel	Bits	Description
CU@NCW	4	0-15	Offset into the current buffer where the next BCW/RCW information is to be written if the function is an interchange read
CU@ERU	13	0-15	High-order bits of the Buffer Memory buffer used to snap the XIOP area of the DSC at the start of each record. Pointers are restored from this buffer in case of error recovery.
CU@ERL	14	0-15	Low-order bits of the error-save buffer
CU@BKP	15	0-15	Offset from the top of the DSC to the descriptor in which the current physical record began
CU@VMS	16	0-15	Valid sector count from the TCB. This is saved with the DSC if the function is suspended for data hold.
CU@TMS	17	0-15	Total sector count from the TCB. This is saved with the DSC during data hold.
CU@RLU	18	0-15	Length (bytes) of record being written
CU@RLL	19	0-15	

BIOP area:

Field	Parcel	Bits	Description
NX@TOP	0	0-15	Top of buffer list. This is an offset from the top of the DSC to the first buffer descriptor available.
NX@BTM	1	0-15	Bottom of buffer list. This is an offset from the top of the DSC to the last buffer descriptor available.
NX@PTR	2	0-15	Offset from the top of the DSC to the next descriptor

Field	Parcel	Bits	Description
NX@BPT	3	0-15	Offset into the current buffer where the next data is to be moved
NX@TPU	4	0-15	High-order bits of the number giving the total bytes transferred from the mainframe for the current block (writes only)
NX@TPL	5	0-15	Low-order bits of current block byte count
NX@BKP	6	0-15	Offset from the top of the DSC to the descriptor where the current record began (writes only)

Buffer descriptor word:

Each buffer descriptor in the buffer list contains the following fields. The contents of parcel 3 depend on the function.

Field	Parcel	Bits	Description
BF@ADU	0	0-15	High-order bits of buffer address in Buffer Memory
BF@ADL	1	0-15	Low-order bits of buffer address in Buffer Memory
BF@STA	2	0-3	Status of buffer. This field indicates special information about the buffer: MD$BOR Beginning of record. On writes, this status is used to detect the descriptor in which a record begins. MD$ERR Error data. On reads, this status specifies that the buffer contains data read during an unrecovered data error.
BF@RLU	2	4-15	High-order bits of record length. This field and the BF@RLL field are valid only in conjunction with MD$BOR. They contain the byte length of the record beginning in the buffer.

Field	Parcel	Bits	Description
BF@RLL	3	0-15	Low-order bits of record length
BF@LNG	3	0-15	Number of bytes of data in buffer (on reads only)

READ REVERSE BUFFER TABLE (RB@)

Header:

Field	Parcel	Bits	Description
RB@NXT	0	0-15	Pointer to next buffer
RB@LST	1	0-15	Pointer to last buffer

Entry:

Field	Parcel	Bits	Description
RB@MSU	0	0-15	High-order bits of buffer address in Buffer Memory
RB@MSL	1	0-15	Low-order bits of buffer address in Buffer Memory
RB@POS	2	0-15	Current pointer
RB@CNT	3	0-15	Byte count of buffer

TAPE CONTROL BLOCK (DC@)

The Tape Control Block (TCB) is composed of a channel response word (CRW) area, a table area, and a channel program word (CPW) area. Only the table area fields are defined here. The CRW and CPW fields are defined among the block multiplexer tables.

CRW area:

	+0				+1				+2		+3	
0	CA				CP				LC		NC	
4	FL	OS		EC		DS			IT		CC	
8	CN	DA		PC		DC			////////////		////////////	

Table area:

	+0			+1			+2		+3	
12	DSU			DSL			BFA		BFB	
16	BFZ			Flags			DAL		QUA	
20	QUA continued			QUB					DHU	
24	DHL			MSG						
28	BRQ			HSU			HSL		TSC	TBC
32	FSC			VMS			TMS		RSC	RBC
36	BLK			BCM			DMS		QRS	

CPW structure:

	+0	+1	+2	+3
40	CPM			
52	C0T			
68	C0B			
72	C1T			
88	C1B			
92	PRW			
96	LIM			

Field	Parcel	Bits	Description
DC@DSU	12	0-15	High-order bits of the Buffer Memory resident Data Stream Control Table address. The table is assigned at open time and controls the data stream for this device.
DC@DSL	13	0-15	Low-order bits of the Buffer Memory resident Data Stream Control Table address
DC@BFA	14	0-15	Pointer to data buffer A, a local buffer used to move data between the device and Buffer Memory. This buffer is allocated only for a read or write request. It is released when the I/O is complete.
DC@BFB	15	0-15	Pointer to data buffer B
DC@BFZ	16	0-15	Size of buffers. Contains the length (in bytes) of the A and B buffers.
DC@CHK	17	5	Checksum flag. This flag is set at the beginning of each tape block (record). It indicates to the data handler that a checksum is to be computed and stored in the reply packet.
DC@ERR	17	6	Abnormal condition flag. This is set when one of the routines in the device activity finds an abnormal condition. It causes the device activity to wait for a request from TQM with the next-valid-packet flag set to indicate that TQM is aware of the condition.
DC@IOF	17	7	I/O active flag. This is set when a tape is currently being read or written. It allows incoming requests to be merged with the current I/O, and it allows I/O to continue without the overhead of reinitiating I/O for each new request.
DC@BDN	17	8	Buffer manager lock flag. The buffer manager sets and clears this flag. It prevents simultaneous access to the buffer manager by more than one routine in a device activity.

Field	Parcel	Bits	Description
DC@BIG	17	9	Large Block Encountered flag. This flag is set when a block larger than the allocated Buffer Memory is encountered.
DC@ERP	17	11	Command Chaining Delay flag. This is set by the data handler to prevent the release of data for which status has not been received from the device. This occurs during command chaining due to the data handler running ahead of the device in expectation of the next block (record).
DC@RDR	17	12	Read Recovery flag. This flag is set during recovery attempts following a read data error. It prevents the movement of data from Buffer Memory to the mainframe.
DC@EOF	17	13	End of file detected on a read
DC@DAL	18	0-15	Pointer to current DAL. This field contains the address of the current request packet.
DC@QUA	19-20	0-15	Wait queue for new requests. The device activity pushes itself onto this queue when waiting for requests from the mainframe.
DC@QUB	21-22	0-15	Wait queue for BIOP response. The device activity pushes itself onto this queue when waiting for the BIOP to reply in response to a request to move data between the mainframe and Buffer Memory.
DC@DHU	23	0-15	High-order bits of saved DSC address. This is the address of the primary DSC when a second DSC is in use.
DC@DHL	24	0-15	Low-order bits of saved DSC address
DC@MSG	25-27	0-15	DAL queue. Requests from the mainframe are placed here prior to execution.

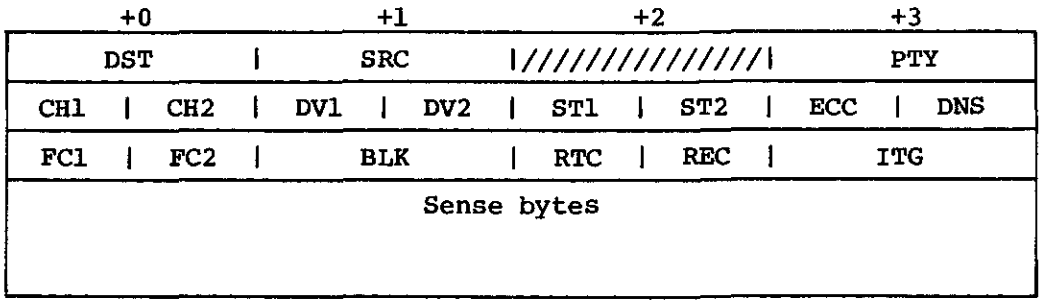
Field	Parcel	Bits	Description
DC@BRQ	28	0-15	Outstanding requests in BIOP. This contains a count of the number of requests for which replies are outstanding from the BIOP.
DC@HSU	29	0-15	High-order bits of current Central Memory address. It is the address to which data is next moved, and is valid during reads only.
DC@HSL	30	0-15	Low-order bits of current Central Memory address
DC@TSC	31	0-7	Transferred sectors. This contains the number of sectors of data moved to the mainframe but not reported to TQM. This field exists because data is moved to the mainframe before status is returned from the device. These sectors are reported to TQM when good status is returned.
DC@TBC	31	8-15	Transferred blocks
DC@FSC	32	0-15	Count of sectors in Buffer Memory moved to the mainframe but not deallocated
DC@VMS	33	0-15	Count of valid sectors in Buffer Memory. During reads, this field contains the number of sectors of data in Buffer Memory for which good status was returned by the device. It tells the device activity that when any of these sectors are moved to the mainframe, an immediate reply can be sent to TQM. During a write, this field contains the number of physical records in Buffer Memory waiting to be written to the device.
DC@TMS	34	0-15	Count of total sectors in Buffer Memory. This contains the total number of sectors of data in Buffer Memory that were not moved to the mainframe. It tells how many sectors of the current request can be moved immediately from Buffer Memory to the mainframe. DC@VMS then tells how many

Field	Parcel	Bits	Description
DC@TMS (continued)			of the sectors moved can be replied to immediately and how many must be stored in DC@TSC until the next good status is returned from the device.
DC@RSC	35	0-7	Requested sector count. This contains the number of sectors requested by the mainframe to be transferred. It is incremented as new requests for data are received that cannot be immediately transferred and decremented when sectors are moved to the mainframe (for reads only).
DC@RBC	35	8-15	Requested block count. This contains the number of blocks (records) to be moved from the device to Buffer Memory. It is incremented as new requests to move blocks from tape are received and decremented when a block is completely moved from the device to Buffer Memory (reads only).
DC@BLK	36	0-15	Current tape position. This contains the current block (record) position on the tape.
DC@BCM	37	0-15	Read reverse table pointer. This contains the address of a table used during reverse read recovery. The table contains Buffer Memory addresses to which data is moved.
DC@DMS	38	0-15	Count of delayed sectors. The data handler uses this field to track the number of sectors of data that are delayed from release due to command chaining.
DC@QRS	39	0-15	Requested sectors queued. This field contains the number of sectors of data requested by the mainframe while the device activity was attempting to read data error recovery.
DC@CPM	40-51	0-15	CPW master list
DC@C0T	52-67	0-15	Top of CPW slave list 0

Field	Parcel	Bits	Description
DC@C0B	68-71	0-15	Bottom of CPW slave list 0
DC@C1T	72-87	0-15	Top of CPW slave list 1
DC@C1B	88-91	0-15	Bottom of CPW slave list 1
DC@PRW	92-95	0-15	PRW word
DC@LIM	96	0-15	TCB limit

TAPE ERROR PACKET (EP@)

The TERROR overlay builds the tape error packet and sends it to the mainframe for logging. The first eight parcels (0-7) contain DAL control information.



Field	Parcel	Bits	Description
EP@DST	8	0-15	Packet destination ID
EP@SRC	9	0-15	Packet source ID
EP@PTY	11	0-15	Packet subtype, which describes the error type
EP@CH1	12	0-7	Initial channel in use
EP@CH2	12	8-15	Last channel used during recovery
EP@DV1	13	0-7	Initial device path (that is, control unit)
EP@DV2	13	8-15	Last device path used in recovery
EP@ST1	14	0-7	Initial device status when error occurred
EP@ST2	14	8-15	Last status at end of recovery
EP@ECC	15	0-7	Error code. The error code is the actual sense bit offset.
EP@DNS	15	8-15	Tape density in effect for this device
EP@FC1	16	0-7	Command issued to the device before the command that caused the error

Field	Parcel	Bits	Description
EP@FC2	16	8-15	Command issued to the device that caused the error
EP@BLK	17	0-15	Current position
EP@RTC	18	0-7	Retry count. This is the number of retries attempted before the error was recovered or deemed irrecoverable.
EP@REC	18	8-15	Recovery flag: =0 Recovered ≠0 Not recovered
EP@ITG	19	0-15	Input tags
Sense bytes	20-31	0-15	Sense bytes read from the control unit for the failing device at the time the error occurred. See table 7-1 for a description of the sense bytes.

Table 7-1. Sense byte descriptions

Byte	Code	Value	Meaning
Sense bytes 0-1: Unit check			
0	SB$CMR	0	Command reject
0	SB$IVR	1	Intervention required
0	SB$BOC	2	Bus out check
0	SB$EQC	3	Equipment check
0	SB$DTC	4	Data check
0	SB$OVR	5	Overrun
0	SB$WCZ	6	Word count 0
0	SB$DCC	7	Data converter check
1	SB$NSE	8	Noise
1	SB$TUA	9	Tape unit status A
1	SB$TUB	10	Tape unit status B
1	SB$7TR	11	7-track feature
1	SB$LPT	12	Load point detect
1	SB$WST	13	Write status set
1	SB$FPT	14	File protect set
1	SB$NCP	15	Not capable
Sense byte 2: Track in error			

Table 7-1. Sense byte descriptions (continued)

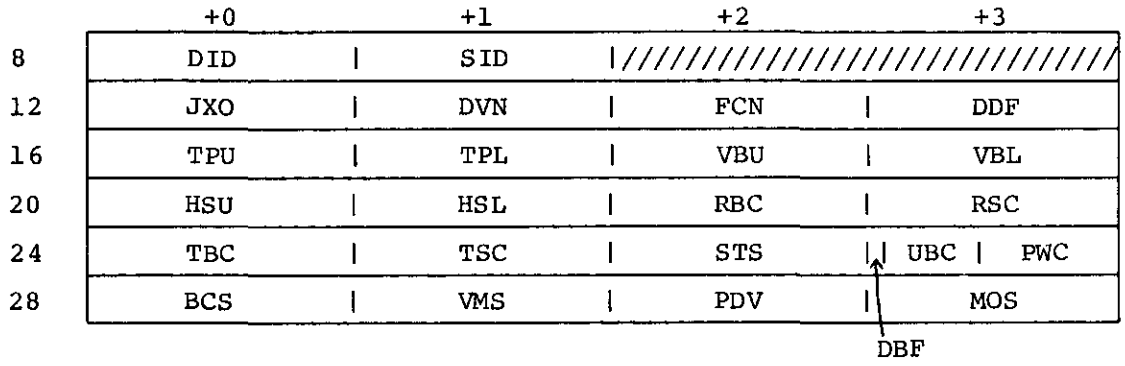
Byte	Code	Value	Meaning
Sense bytes 3-5: Data and equipment checks			
3	SB$VRC	24	Vertical redundancy check
3	SB$LRC	25	Longitudinal redundancy check
3	SB$SKW	26	Skew error
3	SB$CRC	27	Cyclic redundancy check
3	SB$ECC	28	Error correction check
3	SB$PHS	29	Phase mode
3	SB$BKW	30	Backward
3	SB$CCC	31	GCR internal compare error
4	SB$MPE	32	MP hardware error
4	SB$RJT	33	Tape unit reject
4	SB$TPI	34	Tape indicate
4	SB$WTC	35	Write trigger error
4	SB$LWR	37	Loop write-to-read
4	SB$TUC	38	Tape unit check
5	SB$WTM	42	Tapemark error
5	SB$IDB	43	ID burst check
5	SB$SRC	44	Start read check
5	SB$PRC	45	Partial record
5	SB$PST	46	Postamble check
Sense byte 6: Tape unit			
6	SB$WCE	49	Write current failure
6	SB$DBD	50	Double density
6	SB$TUM	51	IBM mode
6	SB$TM0	52	Tape unit model
6	SB$TM1	53	Tape unit model
6	SB$TM2	54	Tape unit model
6	SB$TM3	55	Tape unit model
Sense byte 7: Ready/drop source			
7	SB$LFL	56	Lamp failure
7	SB$RBL	57	Tape bottom left
7	SB$TBR	58	Tape bottom right
7	SB$RST	59	Reset hit
7	SB$DSE	60	Data security erase
7	SB$ERH	61	Erase head failure
7	SB$ABP	62	Air bearing pressure
7	SB$LDF	63	Load failure

Table 7-1. Sense byte descriptions (continued)

Byte	Code	Value	Meaning
Sense bytes 8-10: MP detected errors			
8	SB$IBG	64	IBG detect
8	SB$EBR	67	Early begin readback
8	SB$CBC	68	Control burst check
8	SB$SBR	69	Slow begin readback
8	SB$SER	70	Slow end readback
8	SB$VRR	71	Velocity retry/restart
9	SB$GRC	72	GCR correction
9	SB$VWC	73	Write velocity change
9	SB$CBF	74	Channel buffer check
9	SB$GCR	76	GCR capable
9	SB$TCU	79	Control unit reserved
10	SB$CSR	80	Command status reject
10	SB$CNR	82	Control status reject
10	SB$RBC	83	Read back check
10	SB$DRC	84	Dynamic reversal check
10	SB$TSC	85	Tach start check
10	SB$VLC	87	Velocity check
Sense bytes 11-12: MAL-1 ROS/MP errors			
11	SB$BBC	88	B bus check
11	SB$ROS	90	Low-order bits ROS check
11	SB$HIC	91	High IC/BR or high ROS check
11	SB$MPD	92	Microprogram detected error
11	SB$DBC	93	D bus error
11	SB$BR1	95	BR condition 1 error
12	SB$BB2	96	B bus pointer to LSR check
12	SB$LR2	98	Low-order bits ROS check
12	SB$HR2	99	High-order bits ROS check
12	SB$MP2	100	Microprogram detected error
12	SB$DB2	101	D bus error
12	SB$BR2	103	Branch register error
Miscellaneous errors			
12	SB$UNK	120	Unknown error
12	SB$CHN	121	IOP channel error
12	SB$NXT	122	Go to next error bit

TAPE REQUEST PACKET (TQ@)

The first eight parcels (0-7) of the Tape Request DAL contain the standard DAL header. Of the remaining parcels, parcels 8 and 9 (TX@DID and TQ@SID) are fields common to all packets exchanged between the mainframe and IOS. Tape Exec does not use the TQ@JXO, TQ@VBU, and TQ@VBL fields. The input fields (containing request information from the Tape Queue Manager (TQM) in the mainframe for the Tape Exec in the IOS) are as follows: TQ@DVN, TQ@FCN, TQ@DDF, TQ@TPU, TQ@TPL, TQ@HSU, TQ@HSL, TQ@RBC, TQ@RSC, and TQ@PDV. The output fields (containing reply information from the Tape Exec to TQM) are as follows: TQ@TBC, TQ@TSC, TQ@STS, TQ@DBF, TQ@UBC, TQ@PWC, TQ@BCS, TQ@VMS, and TQ@MOS.



Field	Parcel	Bits	Description
TQ@DID	8	0-15	Destination ID. This field applies to all packets exchanged between the mainframe and the IOS. On input, the destination ID is used to direct the request to the proper routine.
TQ@SID	9	0-15	Sender ID. This field applies to all packets exchanged between the mainframe and the IOS. The source ID specifies the sender of the request. On output, the destination ID and the source ID are exchanged before sending a response back to the mainframe.
	10-11	0-15	Unused
TQ@JXO	12	0-15	Offset to the Job Execution Table (not used by Tape Exec)
TQ@DVN	13	0-15	Device number. This links the request to the appropriate device handler and data stream.

Field	Parcel	Bits	Description
TQ@FCN	14	0-15	Function code to be executed (in octal):

FC$READ	(1)	Read block
FC$WRITE	(2)	Write tape block
FC$MOUNT	(3)	Mount and connect device
FC$FREE	(4)	Free device
FC$UNLD	(5)	Unload tape
FC$REWND	(6)	Rewind tape
FC$CREAD	(7)	Continue read
FC$EOF	(10)	Write tapemark
FC$RWND1	(11)	Write partial and tapemark
FC$FWFIL	(12)	Search forward file
FC$FWSPC	(13)	Space forward
FC$BKFIL	(14)	Search backward file
FC$BKSPC	(15)	Space backward
FC$UNSOL	(16)	Unsolicited XIOP status
FC$CHNGE	(17)	Change device configuration
FC$REPOS	(20)	Reposition tape
FC$VERIF	(21)	Verify tape position
FC$ERASE	(22)	Erase tape
FC$BURN	(23)	Data security erase
FC$RMNT	(24)	Remount
FC$RWND2	(25)	Write two EOFs and rewind
FC$UNLD1	(26)	Write one EOF and unload
FC$UNLD2	(27)	Write two EOFs and unload

TQ@DDF	15	0-15	Dataset Description flags. The flags act as modifiers to the function code.
DD@BMX		0-1	Reserved
DD@RRN		2	Bypass read recovery
DD@PCW		3	Use partial-word count
DD@DVB		4	Data unblocked
DD@LBW		5	Last block write
DD@NVP		6	Next valid packet
DD@DNS		7-8	Tape density
DD@FRM		9-10	Dataset format
DD@DUD		11	Discard user data
DD@DLD		12	Discard label data
DD@HLD		13	Hold data in Buffer Memory
DD@SNC		14	Sync on data in current request

Field	Parcel	Bits	Description
TQ@DDF (continued)			
DD@STG		14	Staged tape dataset
DD@ONL		15	Online tape dataset
TQ@TPU	16	0-15	High-order bits of the maximum tape block size, in bytes. This is used to determine the amount of Buffer Memory needed to fulfill the request. It is also used to determine physical record length on transparent format writes.
TQ@TPL	17	0-15	Low-order bits of the maximum tape block size, in bytes
TQ@VBU	18	0-15	High-order bits of the volume block count
TQ@VBL	19	0-15	Low-order bits of the volume block count
TQ@HSU	20	0-15	High-order bits of Central Memory address
TQ@HSL	21	0-15	Low-order bits of Central Memory address
TQ@RBC	22	0-15	Requested block count. This contains the number of physical blocks (records) to move between the device and Buffer Memory.
TQ@RSC	23	0-15	Requested sector count. This contains the number of sectors (512-words each) to be moved between Buffer Memory and the mainframe.
TQ@TBC	24	0-15	Transferred block count. This is used to write replies only. It specifies the number of physical records moved from the mainframe to Buffer Memory.
TQ@TSC	25	0-15	Transferred sector count. This contains the number of sectors (512-word each) moved from Buffer Memory to the mainframe.

Field	Parcel	Bits	Description
TQ@STS	26	0-15	Status field. This contains flags that tell TQM the current state of the device and data.
ST@BTR		0	Block transferred. One block (record) was moved between the device and Buffer Memory.
ST@DTR		1	Data transferred. Data was tranferred between Buffer Memory and the mainframe. TQ@TSC specifies the amount.
ST@EOF		2	End of file. An end-of-file tapemark was encountered during a read or was written due to a request. This flag is always accompanied by ST@BTR.
ST@BIG		3	Block too big. This flag applies to reads only. It is set when data is read into Local Memory from the device and no more Buffer Memory is allocated to hold it.
ST@LST		4	Lost data. This is set when the tape goes off the end of the reel.
ST@URE		5	Unrecovered error. This is set when a data error returned from the device is irrecoverable.
ST@NRW		6	No write ring. This is set when a write is attempted on a device on which a tape has been loaded with no write ring.
ST@BOT		7	Beginning of tape encountered. This is set when load point on a tape is detected.
ST@EOT		8	End of tape encountered. This is set when the end-of-tape marker is detected (writes only).
ST@RDY		9	Device not ready. This is set when an attempt is made to use a device that is not ready.

Field	Parcel	Bits	Description
TQ@STS (continued)			
ST@RST		10	Reset hit. This is set when the reset button has been hit during an operation to the device.
ST@NOP		11	Device not operational. This is set when a device is not operational.
ST@NCP		12	Not capable. This is set when a device is not capable of executing a function. A common example is when a NRZI tape is loaded on a device without NRZI read capability.
ST@WFE		13	Write format error. This is set when the data handler in BIOP (or DIOP) runs into an error in the data being moved from the mainframe to Buffer Memory. Examples are interchange record larger than the size specified in the request or a control word out of place.
ST@DAL		14	DAL protocol error. This is set when an error is detected in the request itself.
TQ@DBF	27	0	Bad Data flag. This specifies that the last sector of the count in TQ@TSC contains bad data due to an unrecovered data error during a read.
TQ@UBC	27	1-6	Unused bit count. This specifies the number of unused bits in the last word of the last sector sent in the current reply.
TQ@PWC	27	7-15	Partial word count. This specifies the number of words of data in the last sector sent in the current reply. It is used only if the sector is not full.

Field	Parcel	Bits	Description
TQ@BCS	28	0-15	Block checksum. This contains a number computed from the data read or written. It is valid only when accompanied by the block-transferred flag (ST@BTR). This number is recomputed for each block.
TQ@VMS	29	0-15	Valid sector/block count. When reading, this field contains the number of sectors in Buffer Memory that can be transferred. When writing, it contains the number of records ready to be written to tape.
TQ@PDV	30	0-15	Previous device. This is used in conjunction with the remount function (FC$RMNT). It specifies the number of the device on which the previous reel of a multivolume job was processed. It finds the data stream that was attached to that device and attaches it to the device specified by TQ@DVN.
TQ@MOS	31	0-15	Available Buffer Memory sector count. This field contains the current number of sectors (512 words each) of Buffer Memory available for allocation by the XIOP.

The following fields in the tape packet are valid only for the change configuration (FC$CHNGE) function.

Field	Parcel	Bits	Description
TQ@CHN	12	8-15	Channel number
TQ@CNT	13	0-7	Control unit ID
TQ@DEV	13	8-15	Device ordinal
TQ@OPC	15	11	Op code: 1 = Down
TQ@DVC	15	12	Device change
TQ@CUC	15	13	Control unit change
TQ@CHC	15	14	Channel change

Field	Parcel	Bits	Description
TQ@TYP	15	15	Configuration type: 1 = Single component 0 = CNT to be processed
TQ@HLN	18	0-15	Header length of CNT
TQ@ELN	19	0-15	Entry length of CNT

XIOP-BIOP PACKET DEFINITIONS

Field	Parcel	Bits	Description
DA@ID	8	0-15	Destination ID
DA@TCB	12	0-15	TCB address
DA@DVN	13	0-15	Device number
DA@FCN	14	0-15	Function code (in octal):
			FC$READ (1) Read block
			FC$WRITE (2) Write tape block
			FC$MOUNT (3) Mount and connect device
			FC$FREE (4) Free device
			FC$UNLD (5) Unload tape
			FC$REWND (6) Rewind tape
			FC$CREAD (7) Continue read
			FC$EOF (10) Write tapemark
			FC$RWND1 (11) Write partial and tapemark
			FC$UPFLE (12) Search forwards file
			FC$UPSPC (13) Space forwards
			FC$BKFLE (14) Search backwards file
			FC$BKSPC (15) Space backwards
			FC$UNSOL (16) Unsolicited XIOP status
			FC$CHNGE (17) Change device configuration
			FC$REPOS (20) Reposition tape
			FC$VERIF (21) Verify tape position
			FC$ERASE (22) Erase tape
			FC$BURN (23) Data security erase
			FC$RMNT (24) Remount
			FC$RWND2 (25) Write two EOFs and rewind
			FC$UNLD1 (26) Write one EOF and unload
			FC$UNLD2 (27) Write two EOFs and unload
DA@DDF	15	0-15	Dataset Description flags:
DA@FMT		9-10	Dataset format
DA@TPU	16	0-15	High-order bits of the maximum tape block size, in bytes
DA@TPL	17	0-15	Low-order bits of the maximum tape block size, in bytes

Field	Parcel	Bits	Description
DA@DSU	18	0-15	High-order bits of the DSC address
DA@DSL	19	0-15	Low-order bits of the DSC address
DA@HSU	20	0-15	High-order bits of Central Memory address
DA@HSL	21	0-15	Low-order bits of Central Memory address
DA@RSC	23	0-15	Requested sector count
DA@TSC	25	0-15	Transferred sector count
DA@STA	26	0-15	Status field
DA@DBF	27	0	Bad Data flag
DA@UBC	27	1-6	Unused bit count
DA@PWC	27	7-15	Partial word count
DA@TBC	28	0-15	Block checksum

USER CHANNEL TABLES 8

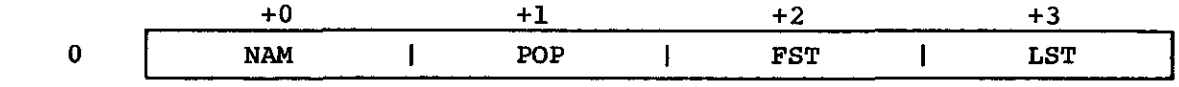
The user channel tables in this section provide data definitions for user channel I/O. User channel tables are part of the MIOP software. Parcel numbers for tables in this section are given in decimal notation.

USER CHANNEL TABLE (UC@)

Input and output channels in the user channel tables are separate; two UCT entries exist for a channel pair. The global register %UCT contains a pointer to the UCT header.

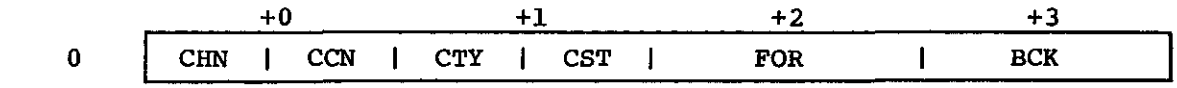
User channel table entries are stored as a double-linked list in local memory. A Channel Shell activity and its corresponding driver activity communicate through a UCT entry.

Header:

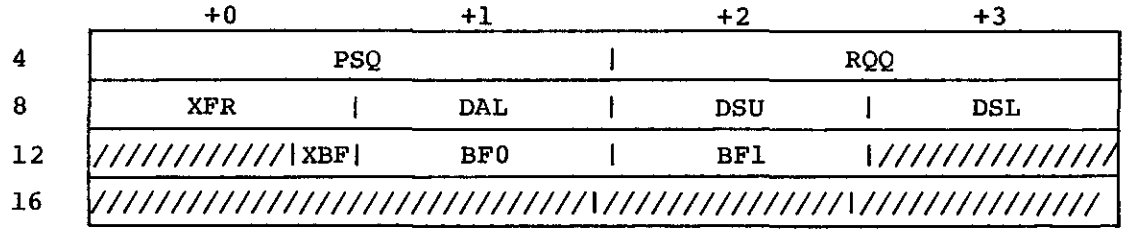


Field	Parcel	Bits	Description
UC@NAM	0	0-15	Table name ("UC")
UC@POP	1	0-15	Table population
UC@FST	2	0-15	First table entry address
UC@LST	3	0-15	Last table entry address

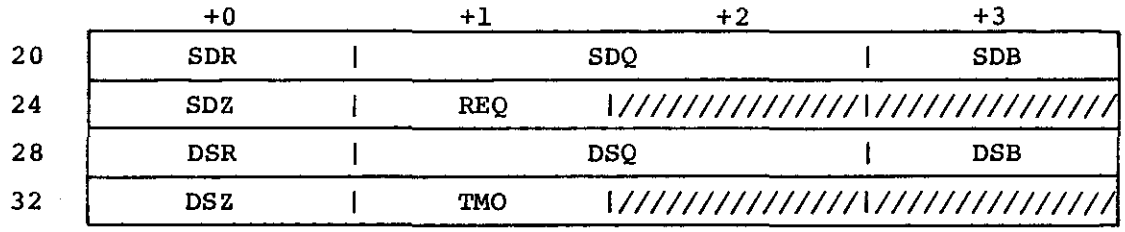
Entry:



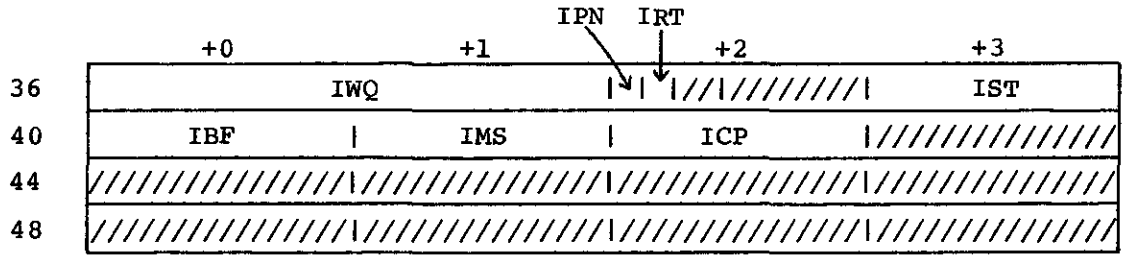
Shell storage:



Interface storage:



Driver storage:



Field	Parcel	Bits	Description
UC@CHN	0	0-7	Physical channel number. Even numbers designate input channels, odd numbers designate output channels.
UC@CCN	0	8-15	Co-channel number. Physical channel number of other half (input or output) of the channel pair.
UC@CTY	1	0-7	Channel type
UC@CST	1	8-15	Channel status. Indicates the status of the most recent channel request.
UC@FOR	2	0-15	Table link (forward). Pointer to next entry in the UCT list.

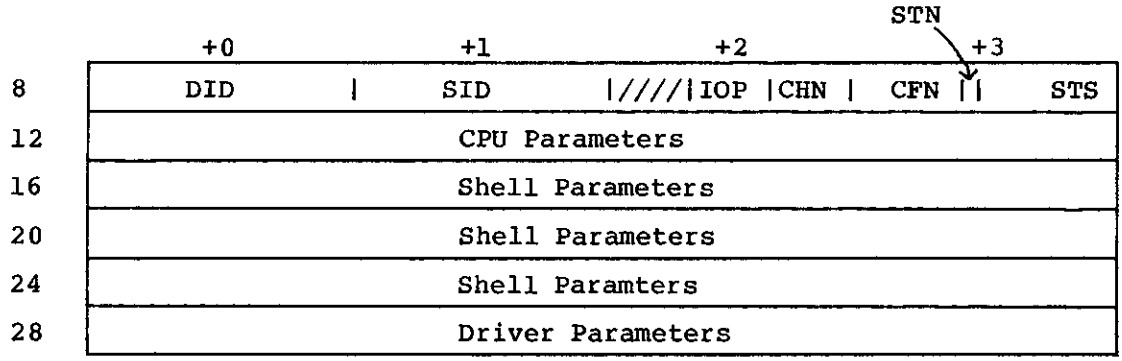
Field	Parcel	Bits	Description
UC@BCK	3	0-15	Table link (backward). Pointer to prior entry in the UCT list.
UC@PSQ	4-5	0-15	Processor Shell wait queue. Shell will push itself on this queue when waiting for next mainframe request.
UC@RQQ	6-7	0-15	Request queue. F-packets waiting to be serviced by the Shell.
UC@XFR	8	0-15	Data transfer pop cell address. Address used to AWAKE Data Transfer activity in BIOP. The Data Transfer activity is created at channel open and terminated at channel close.
UC@DAL	9	0-15	Data transfer DAL address. Address of command packet passed to the Data Transfer activity in BIOP for moving data between Central Memory and Buffer Memory.
UC@DSU	10	0-15	High-order bits of address of buffer descriptor table in Buffer Memory. The buffer descriptor table is allocated at channel open and deallocated at channel close.
UC@DSL	11	0-15	Low-order bits of address of buffer descriptor table in Buffer Memory.
	12	0-14	Reserved
UC@XBF	12	15	Extra Local Buffer flag. When set to 1 by the channel driver during open, indicates that Shell and driver are to use double buffering for I/O.
UC@BF0	13	0-15	Local buffer 0 address
UC@BF1	14	0-15	Local buffer 1 address. Valid when double buffering between Shell and driver.
	15-19	0-15	Reserved
UC@SDR	20	0-15	Shell SIGNAL/Driver WATCH request code. Indicates the operation to be performed by the driver activity.

Field	Parcel	Bits	Description
			Codes are as follows: 3 = Open 4 = Close 5 = Read 6 = Read-last 7 = Write 8 = Write-last 9-31 = Reserved 32-255 = Driver function
UC@SDQ	21-22	0-15	Shell SIGNAL/Driver WATCH queue
UC@SDB	23	0-15	Request buffer address. The local memory address of the buffer containing the data to be written to the channel or read from the channel.
UC@SDZ	24	0-15	Request buffer size. Number of bytes to write or read.
UC@REQ	25	0-15	Current F-packet request address in local memory. Driver may need to examine the F-packet for special parameters.
	26-27	0-15	Reserved
UC@DSR	28	0-15	Driver SIGNAL/Shell WATCH response code. Indicates the driver response to the last Shell request. Codes are as follows: 0 = Complete 1 = Continue 2 = No operation 3-31 = Reserved 32-127 = Error
UC@DSQ	29-30	0-15	Driver SIGNAL/Shell WATCH queue
UC@DSB	31	0-15	Response buffer address. Local memory address of buffer containing the data written to the channel or read from the channel.
UC@DSZ	32	0-15	Response buffer size. Number of bytes written or read.

Field	Parcel	Bits	Description
UC@TMO	33	0-15	I/O timeout limit (measured in tenths of seconds). Supplied by mainframe on channel open request.
	34-35	0-15	Reserved
UC@IWQ	36-37	0-15	Interrupt wait queue. Driver activity TPUSHes onto this queue after I/O is initiated on a channel.
UC@IPN	38	0	Interrupt Pending flag. Indicates that the driver has started I/O when set, but the interrupt has not yet occurred.
UC@IRT	38	1	Interrupt Returned flag. Indicates that an interrupt has occurred on the channel when set.
	38	2-15	Reserved
UC@IST	39	0-15	Interrupt status. Value obtained from the channel after last interrupt occurred.
UC@IBF	40	0-15	Interrupt buffer address. Ending local memory address of data transferred during last I/O on the channel.
UC@IMS	41	0-15	Interrupt millisecond time. Value of millisecond timer when last interrupt occurred on the channel.
UC@ICP	42	0-15	Interrupt clock period time. Number of 2 clock period intervals within the current millisecond when last interrupt occurred on the channel.
	43-51	0-15	Driver storage. Use of this area is defined by the Channel Driver activity.

USER CHANNEL REQUEST PACKET (CR@)

The I/O Subsytem receives requests for channel functions from the mainframe in a 6-word packet on the low-speed channel to MIOP. Responses to these requests are sent by MIOP to the mainframe as a 6-word packet. The first 8 parcels (0-7) of the request DAL contain the standard DAL header. The packet format is as follows:



Field	Parcel	Bits	Description
CR@DID	8	0-15	Destination ID. This field applies to all packets exchanged between the mainframe and the IOS. On input, the destination ID is used to direct the request to the proper routine.
CR@SID	9	0-15	Source ID. This field applies to all packets exchanged between the mainframe and the IOS. The source ID specifies the sender of the request. On output, the destination ID and the source ID are exchanged before sending a response back to the mainframe.
	10	0-6	Reserved for mainframe
CR@IOP	10	7-9	IOP number. IOP on which the channel is located. 0 = MIOP, 1 = BIOP, etc.
CR@CHN	10	10-15	Physical channel number. Even numbers designate input channels, odd numbers designate output channels.
CR@CFN	11	0-7	Request function code. Codes are as follows:

Field	Parcel	Bits	Description
			3 = Open 4 = Close 5 = Read 6 = Read-hold 7 = Read-read 8 = Write 9 = Write-hold 10 = Write-write 11-31 = Reserved 32-255 = Driver function
CR@STN	11	8	Response status number. Indicates that response status applies to first half of 2-part requests (i.e., Read-hold, Read-read) when 0. When this is a 1, it indicates that the response applies to the second half of 2-part requests.
CR@STS	11	9-15	Response status code. Codes are as follows: 0 = OK 3 = Protocol error 4 = Illegal channel 5 = Illegal function 6 = Illegal driver 7 = Data address error 8 = Data length error 9-31 = Reserved 32-127 = Driver Status

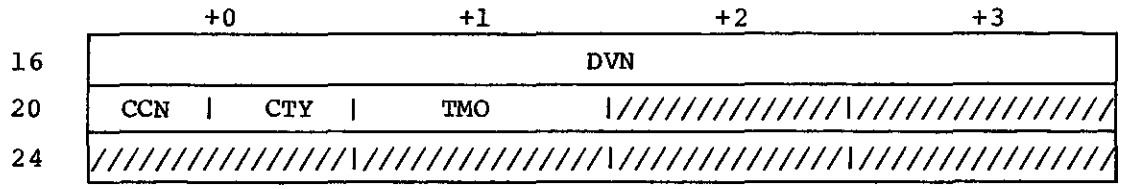
The part of the packet labeled CPU Parameters (parcels 12 through 15) contains information for the mainframe. For detailed information about CPU Parameters, see the section on Subsystem Support in the CRAY-OS Version 1 Reference Manual, publication SR-0011.

The part of the packet labeled Shell Parameters (parcels 16 through 27) contains information for the User Channel Shell. User Channel Shell software is described later in this section and in the IOS Software Internal Reference Manual, CRI publication SM-0046.

The part of the packet labeled Driver Parameters (parcels 28 through 31) contains information for the Channel Driver. Site personnel who work with the packet determine the contents of the Driver Parameters. See individual driver descriptions for detailed information on this site-dependent section of the packet.

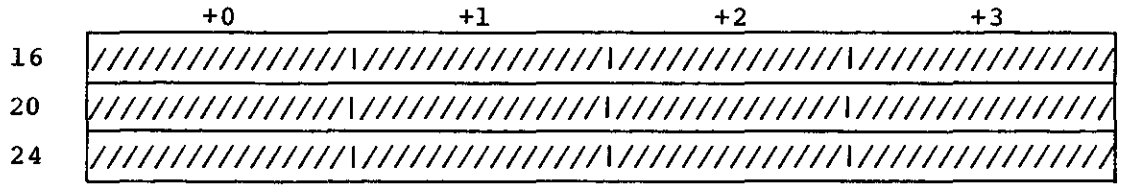
The part of the packet labeled Shell Parameters (parcels 16 through 27) is defined according to the value assigned to the function code CFN (parcel 11, bits 0 through 7). Depending on the value assigned to CFN, the Shell Parameters are defined as described in the Open function, Close function, Read and Write functions, or Driver function. Table descriptions of each of these functions follow.

Open function



Field	Parcel	Bits	Description
CR@DVN	16-19	0-15	Driver Name (ASCII). Left-justified, blank filled name of driver overlay. Maximum of 8 alphanumeric characters.
CR@CCN	20	0-7	Co-channel number. Physical channel number of other half (input or output) of the channel pair.
CR@CTY	20	8-15	Channel type
CR@TMO	21	0-15	I/O timeout limit (tenths of seconds)
	22-27	0-15	Reserved for Shell

Close function



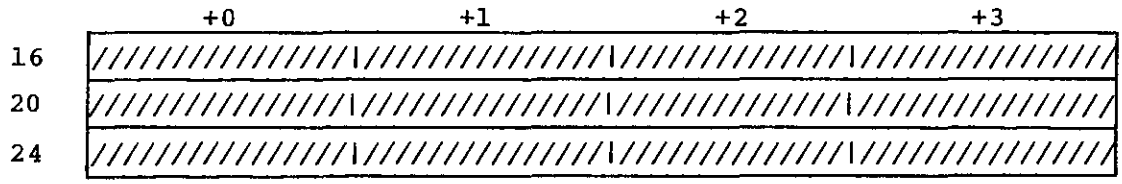
Field	Parcel	Bits	Description
	16-27	0-15	Reserved for Shell

Read and Write functions

	+0	+1	+2	+3
16	C1U	C1L	C2U	C2L
20	D1U	D1L	D2U	D2L
24	T1U	T1L	T2U	T2L

Field	Parcel	Bits	Description
CR@C1U	16	0-15	High-order bits of Central Memory address 1
CR@C1L	17	0-15	Low-order bits of Central Memory address 1
CR@C2U	18	0-15	High-order bits of Central Memory address 2
CR@C2L	19	0-15	Low-order bits of Central Memory address 2
CR@D1U	20	0-15	High-order bits of data length 1
CR@D1L	21	0-15	Low-order bits of data length 1
CR@D2U	22	0-15	High-order bits of data length 2
CR@D2L	23	0-15	Low-order bits of data length 2
CR@T1U	24	0-15	High-order bits of transfer length 1
CR@T1L	25	0-15	Low-order bits of transfer length 1
CR@T2U	26	0-15	High-order bits of transfer length 2
CR@T2L	27	0-15	Low-order bits of transfer length 2

Driver function



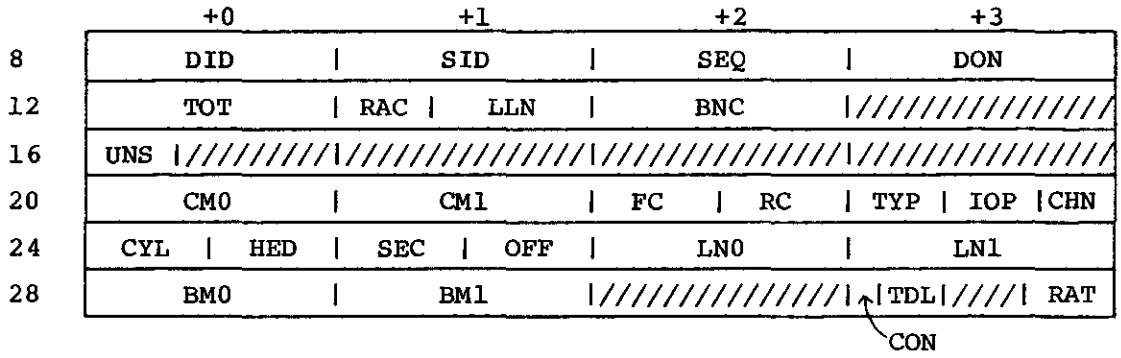
Field	Parcel	Bits	Description
	16-27	0-15	Reserved for Driver

DD-49 DISK TABLES 9

The DD-49 Disk Tables provide data definitions for DD-49 disk support. The parcel numbers for tables in this section are in decimal.

DD-49 DISK REQUEST PACKET (DL@)

The Disk Request Packet (DAL) contains the request information from the mainframe and control information used by the I/O Subsystem for DD-49 disk requests. The packet header (parcels 0-7) is the same as the standard DAL header.



Field	Parcel	Bits	Description
DL@DID	8	0-15	Destination ID
DL@SID	9	0-15	Source ID
DL@SEQ	10	0-15	MEMIO sequence number; indicates the number of sector requests made to MEMIO.
DL@DON	11	0-15	Number of sectors read/written to disk
DL@TOT	12	0-15	Total number of sectors for the request
DL@RAC	13	0-5	Read-ahead or write-behind count
DL@LLN	13	6-15	Last sector length

Field	Parcel	Bits	Description
DL@BNC	14	0-15	Block Check flag and number
DL@UNS	16	0-3	Number of physical units in striped disk group
DL@CM0	20	0-15	Central Memory address (high-order bits)
DL@CM1	21	0-15	Central Memory address (low-order bits)
DL@FC	22	0-7	Function code from mainframe (DAF$)
DL@RC	22	8-15	Response code to mainframe (DAR$)
DL@TYP	23	0-4	Device type (DSK$)
DL@IOP	23	5-6	IOP number
DL@CHN	23	7-15	Channel number
DL@CYL	24	0-10	Starting cylinder number
DL@HED	24	11-15	Starting head group number
DL@SEC	25	0-6	Starting sector number
DL@OFF	25	7-15	Word offset into starting sector
DL@LN0	26	0-15	Transfer word length (high-order bits)
DL@LN1	27	0-15	Transfer word length (low-order bits)
DL@BM0	28	0-15	Buffer Memory address (high-order bits); used by internal disk requests.
DL@BM1	29	0-15	Buffer Memory address (low-order bits); used by internal disk requests.
DL@CON	31	0	Continue flag; used to chain across write requests.
DL@TDL	31	1-3	Transfer data location; used to control data routed through Buffer Memory (BP$).
	31	4-9	Unused
DL@RAT	31	10-15	Total read-aheads used for this request

DD-49 DISK CONTROL BLOCK (DK@)

The Disk Control Block (DCB) serves as the Main Control Table for disk operations. There is one DCB for each disk channel defined. The Channel Control Block (DCCB) contains a pointer to each DCB.

	+0	+1	+2	+3
0	ID	ACT	flags | SRV	CYL
4	/| HED | SEC	RAC	|/| RAH | RAS	SEL|TYP|CHN
8	RAD	FLB	LLB	CLB
12	DL0	DL1	DNQ	DNT
16	RD0	RD1	WR0	WR1
20	SK0	SK1	RA0	SRA
24	PP0	PP1	MC0	MC1
28	ERR	UNR	STS	LNK
32	SL0	RL0	OV0	HD0
36	TMO	(I/O timeout entry)		
40	ST1	WBD	ST2	ACC

Field	Parcel	Bits	Description
DK@ID	0	0-15	Table ID - ASCII 'D4'
DK@ACT	1	0-15	Channel Activity flags; when a flag is set, the corresponding activity is taking place:
DKF@IM		7	Immediate Return flag; used by error recovery.
DKF@ER		8	Error Recovery flag
DKF@RL		9	Unit Release flag
DKF@SL		10	Unit Select flag
DKF@HD		11	Head Select flag
DKF@SK		12	Seek flag
DKF@RA		13	Read-ahead flag
DKF@WR		14	Write flag
DKF@RD		15	Read flag

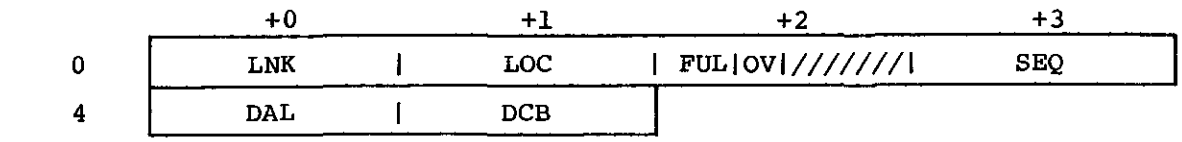
Field	Parcel	Bits	Description
DK@LMA	2	0	Indicates the next Local Memory address register to use
DK@ABT	2	1	Abort Read-ahead flag
DK@ADD	2	2	Indicates the next Local Memory Address register to check for error
DK@EWB	2	3	Signal for early status
DK@CNG	2	4	Chaining flag
DK@SRV	2	5-15	Disk Service flags; when a flag is set, the corresponding service is to be performed by D4DEM:
DKS@RS		14	Some resource is unavailable; attempt to restart I/O.
DKS@CR		15	A disk error has occurred; create the error recovery activity.
DK@CYL	3	0-15	Current cylinder
DK@HED	4	2-6	Current head group
DK@SEC	4	7-15	Current sector
DK@RAC	5	0-15	Starting read-ahead cylinder or ending write-behind cylinder
DK@RAH	6	2-6	Starting read-ahead head group or ending write-behind head group
DK@RAS	6	7-15	Starting read-ahead sector or ending write-behind sector
DK@SEL	7	0	Channel Select flag; channel is selected when the flag is set.
DK@TYP	7	2-6	Device type (DSK$)
DK@CHN	7	7-15	Channel number
DK@RAD	8	0-15	Number of read-aheads done
DK@FLB	9	0-15	Pointer to first Local Buffer entry
DK@LLB	10	0-15	Pointer to last Local Buffer entry

Field	Parcel	Bits	Description
DK@CLB	11	0-15	Pointer to current Local Buffer entry
DK@DL0	12	0-15	Address of first DAL on queue
DK@DL1	13	0-15	Address of last DAL on queue
DK@DNQ	14	0-15	Address of first DAL on done queue
DK@DNT	15	0-15	Address of last DAL on done queue
DK@RD0	16	0-15	Channel read count (high-order bits)
DK@RD1	17	0-15	Channel read count (low-order bits)
DK@WR0	18	0-15	Channel write count (high-order bits)
DK@WR1	19	0-15	Channel write count (low-order bits)
DK@SK0	20	0-15	Channel seek count (high-order bits)
DK@SK1	21	0-15	Channel seek count (low-order bits)
DK@RA0	22	0-15	Channel read-ahead count
DK@SRA	23	0-15	Count of successful read-ahead sectors
DK@PP0	24	0-15	Error recovery push cell (first)
DK@PP1	25	0-15	Error recovery push cell (last)
DK@MC0	26	0-15	MCB address (high-order bits)
DK@MC1	27	0-15	MCB address (low-order bits)
DK@ERR	28	0-15	Error count
DK@UNR	29	0-15	Unrecovered error count
DK@STS	30	0-15	Error status save cell
DK@LNK	31	0-15	DCB link cell
DK@SL0	32	0-15	Channel select count
DK@RL0	33	0-15	Channel release count
DK@OV0	34	0-15	Software overrun count

Field	Parcel	Bits	Description
DK@HD0	35	0-15	Channel head select count
DK@TMO	36-39	0-15	Disk timer entry
DK@ST1	40	0-15	Error status cell 1
DK@WBD	41	0-15	Count of write-behinds done
DK@ST2	42	0-15	Error status cell 2
DK@ACC	43	0-15	Most recent accumulator parameter issued to disk; used in error checks.

LOCAL BUFFER ENTRY (LB@)

The Local Buffer Entry is used for Local Memory Buffer control. One entry exists for each dedicated Local Memory buffer being used by the disk channel. These entries serve as requests to the MEMIO overlay to move a sector of data to or from Local Memory. The Local Buffer entries immediately follow the DCB.



Field	Parcel	Bits	Description
LB@LNK	0	0-15	Link cell
LB@LOC	1	0-15	Local Memory Buffer address
LB@FUL	2	0	Local Buffer Full flag
LB@OV	2	1	Software Overrun flag
LB@SEQ	3	0-15	Sector sequence number; used for block number check.
LB@DAL	4	0-15	Pointer to associated DAL
LB@DCB	5	0-15	Pointer to associated DCB

BUFFER MEMORY CONTROL BLOCK (CB@)

The Buffer Memory Control Block (MCB) is a Buffer Memory resident table used to control the flow of disk data through Buffer Memory. One MCB exists for each disk channel defined. The associated DCB contains a pointer to the MCB. This table consists of three distinct parts:

- BIOP control information
- DIOP control information
- A circular list of buffer entries.

	+0	+1	+2	+3
word 0	DD@TOP	DD@BOT	DD@DCB	DD@PTR
1	BB@TOP	BB@BOT	BB@DTR	BB@PTR
2	//////////////////////////////		CB@BM0	CB@BM1
:			:	
n	//////////////////////////////		CB@M0	CB@BM1

DIOP control information:

Field	Parcel	Bits	Description
DD@TOP	0	0-15	Offset to top of buffer list
DD@BOT	1	0-15	Offset to bottom of buffer list
DD@DCB	2	0-15	Associated DCB address
DD@PTR	3	0-15	Offset to next buffer to use

BIOP control information:

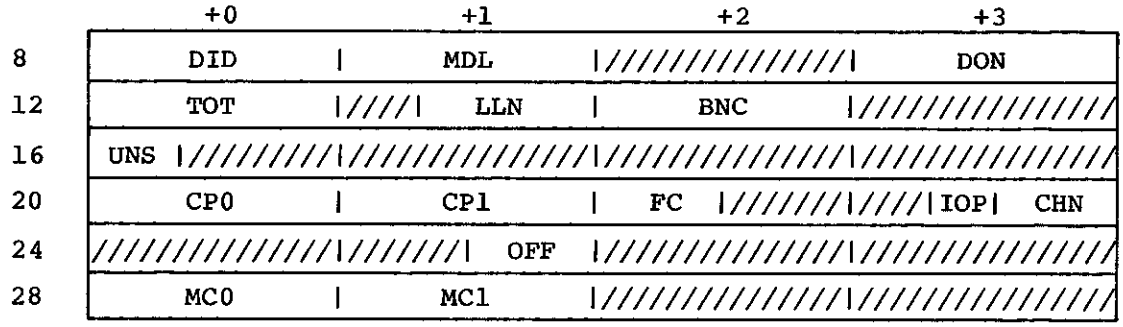
Field	Parcel	Bits	Description
BB@TOP	0	0-15	Offset to top of buffer list
BB@BOT	1	0-15	Offset to bottom of buffer list
BB@DTR	2	0-15	Current DTR (data transfer request) address
BB@PTR	3	0-15	Offset to next buffer to use

Buffer entry:

Field	Parcel	Bits	Description
CB@BM0	2	0-15	Buffer Memory address (high-order bits)
CB@BM1	3	0-15	Buffer Memory address (low-order bits)

DATA TRANSFER REQUEST (TR@)

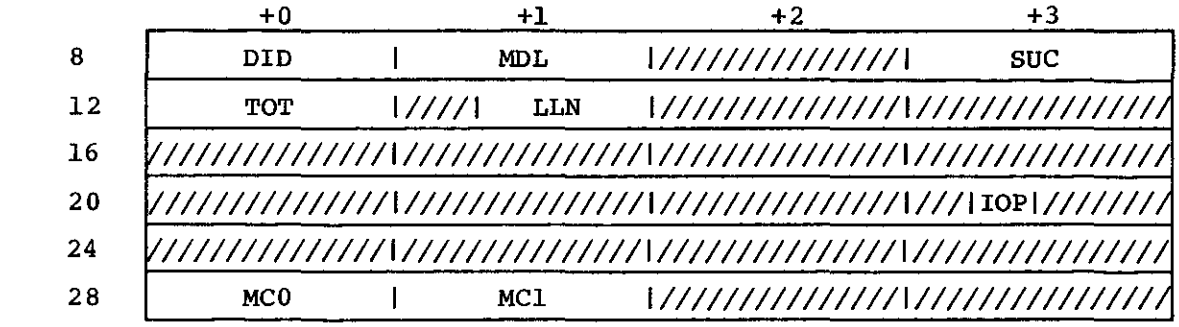
The Data Transfer Request (DTR) is used to make requests to the TRANSFR overlay. It contains the information necessary to move data between Buffer Memory and Central Memory. The first 9 parcels (0-8) of the DTR are the same as those in the DD-49 Disk Request Packet.



Field	Parcel	Bits	Description
DL@DID	8	0-15	Destination ID
TR@MDL	9	0-15	Originating DAL address
TR@DON	11	0-15	Number of sectors transfered
TR@TOT	12	0-15	Total number of sectors to transfer
TR@LLN	13	6-15	Last sector length
TR@BNC	14	0-15	Block Check flag and number
TR@UNS	16	0-3	Number of physical units in striped disk group
TR@CP0	20	0-15	Central Memory address (high-order bits)
TR@CP1	21	0-15	Central Memory address (low-order bits)
TR@FC	22	0-7	Function code from mainframe
TR@IOP	23	5-6	IOP number of disk
TR@CHN	23	7-15	Channel number of disk
TR@OFF	25	7-15	Word offset into starting sector
TR@MC0	28	0-15	MCB (Buffer Memory control block) address (high-order bits)
TR@MC1	29	0-15	MCB address (low-order bits)

ABORT TRANSFER REQUEST (AR@)

The Abort Transfer Request (ATR) is used to terminate movement of data between Buffer Memory and Central Memory before the completion of a DTR. This packet is sent to the TRANSFR overlay in the event of an unrecoverable disk error. The first 9 parcels (0-8) of the DTR are the same as those in the DD-49 Disk Request Packet.



Field	Parcel	Bits	Description
DL@DID	8	0-15	Destination ID
AR@MDL	9	0-15	Originating DAL address
AR@SUC	11	0-15	Number of successful sectors to transfer
AR@TOT	12	0-15	Total number of sectors to transfer
AR@LLN	13	6-15	Last sector length
AR@IOP	23	5-6	IOP number of disk
AR@MC0	28	0-15	MCB (Buffer Memory control block) address (high-order bits)
AR@MC1	29	0-15	MCB address (low-order bits)

DD-49 DISK ERROR MESSAGE (EM@)

The Disk Error Message is sent to the mainframe to be logged in the $SYSTEMLOG on each occurrance of a DD-49 disk error.

	+0	+1	+2	+3
0	DT |IOP|CHN|ERR|	CYL	|FS|HED| SEC	FNC | RTR
4	CTL	GEN	S00	S01
8	S02	S03	S04	S05
12	S06	S07	S08	S09
16	S10	S11	S12	S13
20	S14	S15	S16	S17
24	S18	S19	S20	S21
28	S22	S23	|OFF|////////////////////|	CAL|EC
32	COR	(Data correction information)		
36		(Data correction information continued)		
40	EXP	ACT	FCT	FGE
44	FFC	OES	FES	VSF
48	//			
52	//			
56	//			

Field	Parcel	Bits	Description
EM@DT	0	0-6	Device type: DSK$DD49
EM@IOP	0	7-9	IOP number
EM@CHN	0	10-15	Channel number
EM@ERR	1	0-3	Major error type: IE$SLCT (0) Unit select IE$SEEK (1) Cylinder select IE$READ (2) Read process IE$WRIT (3) Write process IE$RLSE (4) Unit release
EM@CYL	1	4-15	Expected cylinder

Field	Parcel	Bits	Description
EM@FS	2	0-3	Final error status: DAR$REC (1) Recovered DAR$COR (O'13) Corrected DAR$UNC (O'14) Uncorrected DAR$UNR (O'15) Unrecovered
EM@HED	2	4-6	Expected head group
EM@SEC	2	7-15	Expected sector number
EM@FNC	3	0-7	Disk function (DK$):
		0	LMA (Local Memory Address) register 1
		1	Unit release
		2	Unit select
		3	Head select
		4	Seek
		5	LMA register 0
		6	Write
		7	Read
EM@RTR	3	8-15	Retry count
EM@CTL	4	0-15	Original controller status
EM@GEN	5	0-15	Original drive general status
EM@S00	6-29	0-15	Start of selected statuses 0-23 (24 parcels in length)
EM@OFF	30	0-3	Offset enable and direction
EM@CAL	31	14	Recalibrate flag: 0 Drive not recalibrated 1 Drive was recalibrated
EM@EC	31	15	Error Correction flag: 0 Error correction not used 1 Error correction used
EM@COR	32	0-15	Start of data correction information (8 parcels in length)
EM@EXP	40	0-15	Expected Local Memory address
EM@ACT	41	0-15	Actual Local Memory address
EM@FCT	42	0-15	Final controller status (on unrecovered errors)

Field	Parcel	Bits	Description
EM@FGE	43	0-15	Final drive general status (on unrecovered errors)
EM@FFC	44	0-15	Final disk function on unrecovered errors (DK$):
		0-1	Unused
		2	Compute correction vectors
		3	Recalibrate
		4	Read status register 0
		5	Reset
		6	Return to 0
		7	Clear faults
		8	LMA register 1
		9	Unit release
		10	Unit select
		11	Head select
		12	Seek
		13	LMA register 0
		14	Write
		15	Read
EM@OES	45	0-15	Original recovery status: S$OKAY (0) Okay S$DONE (1) DN set when not expected S$BUSY (2) DN and BZ both set S$STAT0 (3) Status register 0 miscompare S$STAT1 (4) Status register 1 miscompare S$NCLR (5) Unable to clear DN and BZ S$ILMA (6) Initial LMA echo error S$FLMA (7) Final LMA echo error S$TOUT (8) Software timeout
EM@FES	46	0-15	Final recovery status (on unrecovered errors): see EM@OES definitions
EM@VSF	47	0-15	New velocity scale factors (on seek errors during which recalibration was performed)

DD-49 RETRY COUNT TABLE (R@)

The Retry Count Table is used by DD-49 disk error recovery to maintain retry information. This table immediately follows the Disk Error Message.

	+0		+1		+2		+3	
0	TYP		TOTC	TOTL	TMRC	TMRL	NRYC	NRYL
4	BZC	BZL	IPEC	IPEL	SEQC	SEQL	INVC	INVL
8	FNCC	FNCL	CATC	CATL	SKRC	SKRL	OVRC	OVRL
12	ECCC	ECCL	ILMC	ILML	FLMC	FLML	//////////	
16	//							

Field	Parcel	Bits	Description
R@TYP	0	0-15	Major error type: IE$SLCT (0) Unit select IE$SEEK (1) Cylinder select IE$READ (2) Read process IE$WRIT (3) Write process IE$RLSE (4) Unit release
R@TOTC	1	0-7	Total retry count
R@TOTL	1	8-15	Total retry limit
R@TMRC	2	0-7	Timeout reset count
R@TMRL	2	8-15	Timeout reset limit
R@NRYC	3	0-7	Not ready retry count
R@NRYL	3	8-15	Not ready retry limit
R@BZC	4	0-7	Busy response count
R@BZL	4	8-15	Busy response limit
R@IPEC	5	0-7	Input parity error count
R@IPEL	5	8-15	Input parity error limit
R@SEQC	6	0-7	Sequence operation in progress count
R@SEQL	6	8-15	Sequence operation in progress limit
R@INVC	7	0-7	Invalid command count
R@INVL	7	8-15	Invalid command limit

Field	Parcel	Bits	Description
R@FNCC	8	0-7	Function lost count
R@FNCL	8	8-15	Function lost limit
R@CATC	9	0-7	Catastrophic error count
R@CATL	9	8-15	Catastrophic error limit
R@SKRC	10	0-7	Seek retry count
R@SKRL	10	8-15	Seek retry limit
R@OVRC	11	0-7	Overrun retry count
R@OVRL	11	8-15	Overrun retry limit
R@ECCC	12	0-7	ECC (error correction code) error count
R@ECCL	12	8-15	ECC error limit
R@ILMC	13	0-7	Initial LMA (Local Memory address) echo error count
R@ILML	13	8-15	Initial LMA echo error limit
R@FLMC	14	0-7	Final LMA echo error count
R@FLML	14	8-15	Final LMA echo error limit

DD-49 DISK DEMON QUEUE

The DD-49 disk demon queue is a linked list of DCB's (disk control blocks) requesting services from the D4DEM demon overlay. The queue thread runs through the field DK@DEM in the DCB. This queue resides in the Kernel.

Label	Description
DD49Q	Address of first DCB on the queue
DD49QT	Address of last DCB on the queue

IOP MESSAGE CHANNEL QUEUE FOR ICOM (MIAQ)

This table serves as a queue for input requests from other I/O processors to be processed by the ICOM overlay. The MIAQ table resides in the Kernel.

Parcel	Bits	Description
0	0-15	MIOP message queue address in Local Memory
1-2	0-15	Address of Buffer Memory area (high-order and low-order bits) for MIOP
3	0-15	MIOP input channel
4	0-15	BIOP message queue address in Local Memory
5-6	0-15	Address of Buffer Memory area (high-order and low-order bits) for BIOP
7	0-15	BIOP input channel
8	0-15	IOP-2 message queue address in Local Memory
9-10	0-15	Address of Buffer Memory area (high-order and low-order bits) for IOP-2
11	0-15	IOP-2 input channel
12	0-15	IOP-3 message queue address in Local Memory
13-14	0-15	Address of Buffer Memory area (high-order and low-order bits) for IOP-3
15	0-15	IOP-3 input channel

MEMIO DEMON QUEUES

The MEMIO demon queues serve as request queues for the MEMIO demon overlay. There are three distinct queues: HSPIQ, HSPOQ, and MOSQ. The separation of the queues allows MEMIO to overlap I/O on all three memory channels. Each request is a Local Buffer Entry (LB@). Requests are linked through the field LB@LNK and are served in a FIFO manner. These queues reside in the Kernel.

Label	Description
HSPIQ	Address of the first LMA (Local Memory address) request for the 100 Mbyte in-channel (first of 2 parcels)
HSPOQ	Address of the first LMA request for the 100 Mbyte out-channel (first of 2 parcels)
MOSQ	Address of the first LMA request for the Buffer Memory channel (first of 2 parcels)

TRANSFR DEMON QUEUE

The TRANSFR demon queue is a linked list of DTRs (data transfer requests) requesting services from the TRANSFR demon overlay. The queue thread runs through the field DA@LNK in the DTR header. This queue resides in the Kernel.

Label	Description
DTRANQ	Address of first DTR on the queue (first of 2 parcels)

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