PREFACE

This technical note describes the operation of the Cray Research, Inc. (CRI) BMC-5 Block Multiplexer Controller and channels for use with the CRI I/O Subsystem (IOS). The BMC-5 channel interfaces the Auxiliary I/O Processor with IBM† or IBM-compatible peripheral devices, including devices using the IBM data streaming protocol.

This publication is written to assist engineers and programmers interested in the hardware design and programming requirements of the BMC-5.

Section 1 gives a general description of the BMC-5. Section 2 describes the data characteristics of the block multiplexer channel. Section 3 describes each block multiplexer channel function.

The I/O Subsystem Model C Hardware Reference Manual, CRI publication HR-0081, describes the environment in which the BMC-5 is used.

The IBM publication IBM System/360 and System/370 Interface Channel to Control Unit Original Equipment Manufacturer's Information is helpful.

For information on the CRI BMC-4 Block Multiplexer Channel (which does not support Data Streaming) see the I/O Subsystem Hardware Reference Manual, CRI publication HR-0030.

† IBM is a registered trademark of the International Business Machines Corporation.

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GENERAL DESCRIPTION 1

The Cray Research, Inc. (CRI) BMC-5 Block Multiplexer Controller interfaces an Auxiliary I/O Processor DMA port with up to four IBM-type channels. These channels drive one or more IBM-compatible control units, which in turn drive peripheral devices including equipment using the IBM data streaming protocol. The four channels operate asynchronously and compete only for Local Memory references.

A block multiplexer channel operates in either selector channel mode, block mulitplexer mode, or data streaming mode. All IBM commands are possible. The IBM channel modes and their transfer rates are shown in table 1-1.

Table 1-1. IBM Channel Characteristics

Protocol	Maximum Transfer Rate
Selector	0.75 Mbytes/s
Block Multiplexer	0.75 Mbytes/s
Block Multiplexer, High-speed Option	1.6 Mbytes/s
Data Streaming	3.0 Mbytes/s

The BMC-5 consists of one control module, one buffer module, and from one to four channel modules (one channel per channel module). All modules are installed in the I/O Subsystem (IOS) chassis to allow fast communication with the I/O Processor (IOP).

All CRI computer systems currently using an IOS with the BMC-4 Block Mulitplexer Controller can be upgraded to the BMC-5. When upgrading from the BMC-4 to the BMC-5, the modules are directly substituted in the same chassis slots.

Each channel features command chaining, data chaining, detection of retry status, I/O error alert, high-speed option, and data streaming. Command

functions from the IOP control the channel operation (see the Block Multiplexer Channel Functions section for details on programming the BMC-5).

Much of the control is performed by means of a microcode sequencer that executes firmware routines stored in Read Only Memory (ROM). The microcode sequencer handles the control signal sequences and data sequences needed for each protocol mode. Each channel module contains an independent microcode sequencer.

Data buffers are used to match the speeds of the IOP Local Memory and the channel. Two double buffers are used to assure smooth data flow.

Figure 1-1 illustrates the flow of data through the channels and controller.

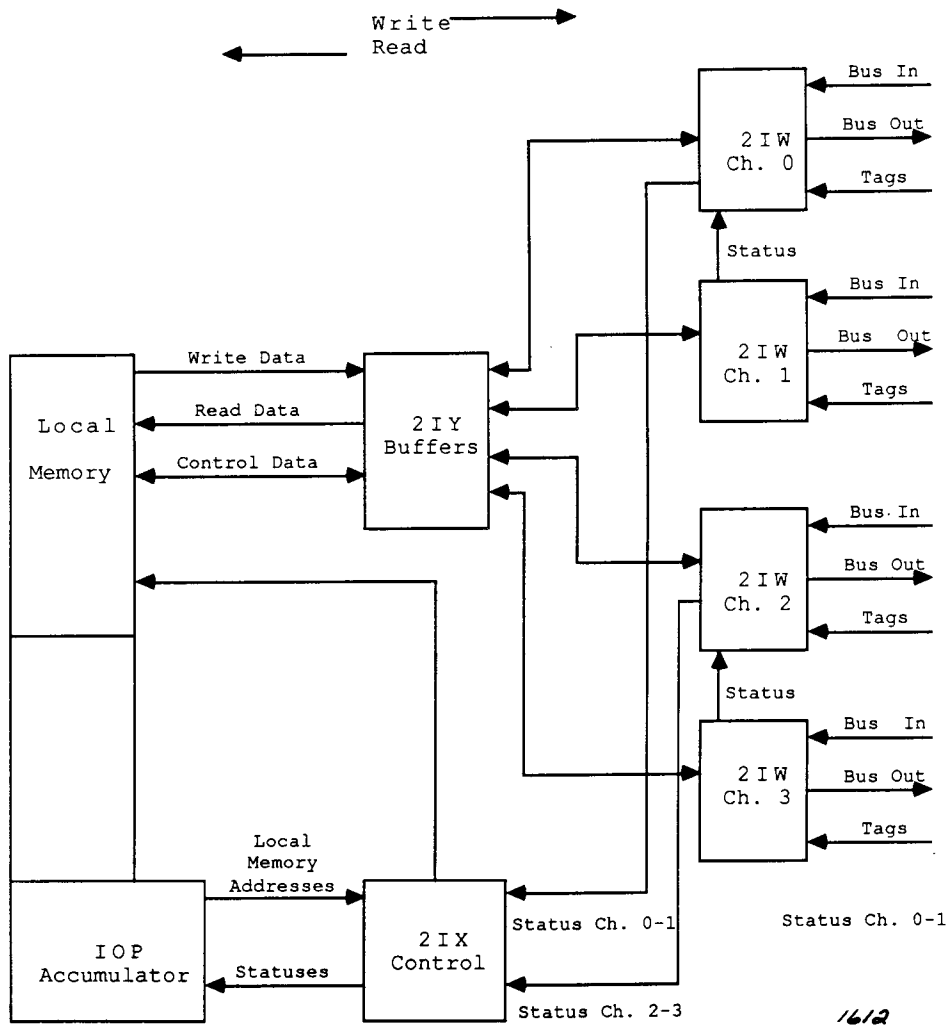

Figure 1-1. BMC-5 Block Diagram

CHANNEL DATA CHARACTERISTICS 2

This section describes the data characteristics of the BMC-5 block multiplexer channel. This section and section 3, Block Mulitplexer Channel Functions, describe the Cray I/O Processor (IOP) programming for the BMC-5 Block Multiplexer Controller.

A block multiplexer channel operates in either selector channel mode, block mulitplexer mode or data streaming mode. All IBM commands are available. Each channel features command chaining, data chaining, detection of retry status, I/O error alert, high-speed option, and data streaming.

TRANSFER RATES

The block multiplexer channel data rate is determined by cable length and signal turnaround time within the IBM control unit. For each byte of data or control information that is sent, an appropriate response signal or signals must be received. The resulting data rate limit is about 6.4 Mbits/s, or 800 Kbytes/s. IBM-compatible peripheral controllers that use the high-speed option (requiring an additional pair of control lines) can achieve about 12.8 MBits/s, or 1.6 MBytes/s. An IOS capable of running in data streaming mode can attain a data rate of 24 MBits/s or 3 MBytes/s.

DATA HANDLING

The channel interfaces the 8-bit IBM channel to the 16-bit I/O Processor Local Memory. The channel assembles the 8-bit IBM bytes into 16-bit parcels, and disassembles the parcels into 8-bit bytes.

As shown in figure 2-1, the BMC-5 reads four 16-bit parcels from Local Memory and sends out eight 8-bit bytes to the block multiplexer channel. Four more 16-bit parcels are read into buffers in the controller while the channel transmits the first group.

The BMC-5 reads eight 8-bit bytes from the channel and writes four 16-bit parcels into Local Memory. If a read operation from the channel terminates with a byte length that does not assemble into 4 parcels, the last Local Memory write includes unpredictable data in the last parcels.

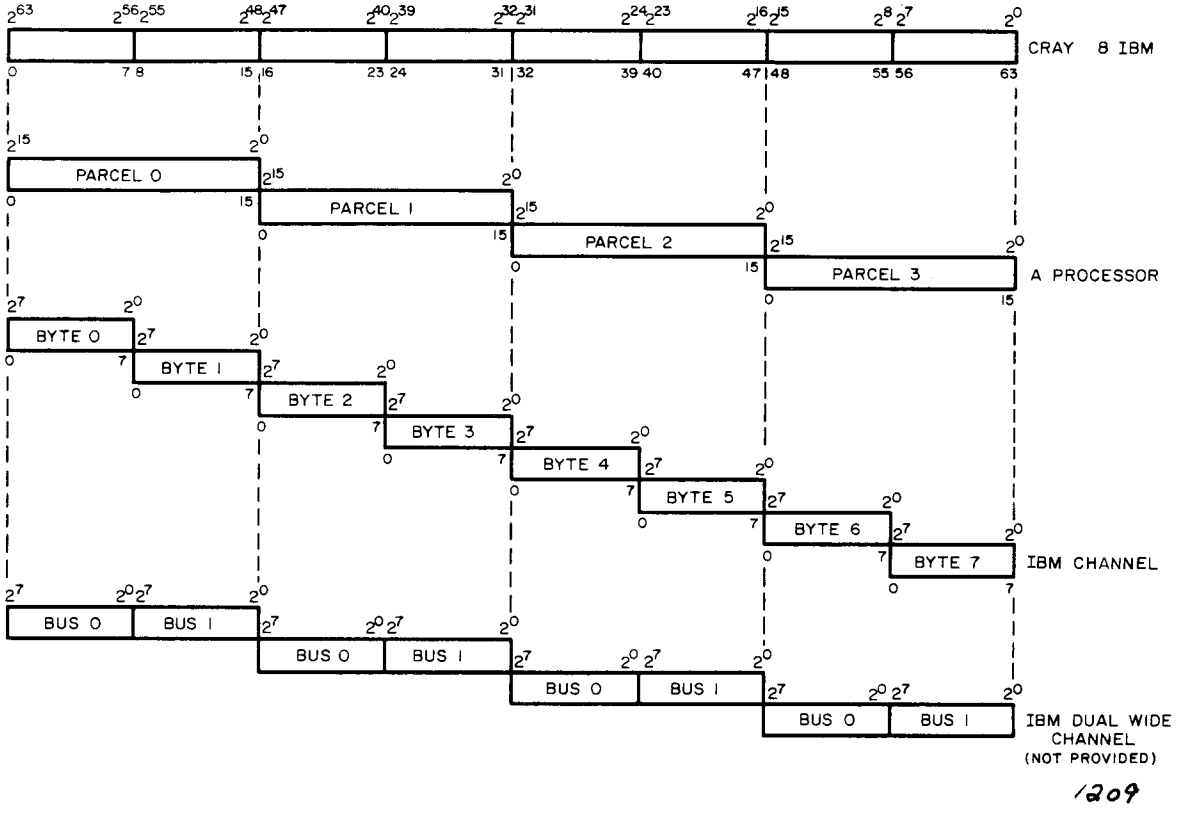

Figure 2-1. BMC-5 Data Assembly/Disassembly

RECORD SIZE

Data records can be any number of bytes long, except zero. However, data chaining must be used for record lengths greater than 65,535 bytes.

For IBM tape records, an odd length header field can be read and stored at one memory area and the following data field can be stored at a different memory area, beginning at a different 64-bit word boundary. The data chaining feature permits a single, large record to be broken into any size convenient for movement through Local Memory and storage in Buffer Memory. This process is under program control by I/O functions to the block multiplexer channel.

PARITY

All address, status, and data inputs to the IOP are checked for odd parity. Odd parity is generated for all address, control, and data outputs from the IOP.

INTERRUPTS

All interrupts can be enabled or disabled for any block mutlitplexer channel. If interuupts are enabled and a BMA : 1 through BMA : 5 function completes, an interrupt request is set. If an interrupt is selected for an input tag line such as request-in, the interrupt request sets when the request-in line goes to a logical 1. These interrupts are cleared by the BMA : 0 command.

When data chaining and interrupts are enabled, an interrupt request is set each time the byte counter decrements to 0 and memory references are complete through that particular block of data. The BMA : 0 or the BMA : 14 command clears this interrupt.

BLOCK MULTIPLEXER CHANNEL FUNCTIONS

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The block multiplexer channel functions are summarized in table 3-1 and are explainded in detail on the following pages. The command mnemonic BMA refers to channel A, BMB refers to channel B, BMC refers to channel C, and so on. Refer to the I/O Subsystem Model C Reference Manual to determine actual IOP accumulator channel numbers.

Table 3-1. BMC-5 Commands

Command	Description
BMA : 0	Clear channel control
BMA : 1	Send reset functions
BMA : 2	Channel command
BMA : 3	Read request-in address (wait request-in)
BMA : 4	Single byte I/O
BMA : 5	Maintenance delay
BMA : 6	Clear channel interrup enable flag
BMA : 7	Set channel interrupt enable flag
BMA : 10	Read Local Memory address
BMA : 11	Read byte count
BMA : 12	Read status
BMA : 13	Read input tags
BMA : 14	Enter Local Memory address

Table 3-1. BMC-5 Commands (continued)

Command	Description
BMA : 15	Enter byte count
BMA : 16	Enter device address
BMA : 17	Enter output tags

BMA : 0 - CLEAR CHANNEL CONTROL

This function clears the Channel Busy and Done flags and all output tags except Operational-Out (OP-OUT) and Suppress-Out (SUP-OUT). No parameters are required. This function also clears interrupt conditions, if interrupts are disabled by a previous BMA : 6 function. Since the BMA : 0 function cannot be interlocked using the Channel Done flag, allow a 12 clock-period (CP) delay before issuing the next function to the channel.

BMA : 1 - SEND RESET FUNCTION

This function performs several required reset functions for the equipment. Bits 2^1 and 2^0 of the accumulator content are used as a parameter to select the specific reset function. The other accumulator bits are ignored. Table 3-2 lists the parameter bits and their specific reset function. A description of each specific reset function follows the table.

Table 3-2. Send Reset Function Selections

Parameter Bits		Selection
2^1	2^0	
0	0	Clear all output lines
0	1	Interface disconnect
1	0	Selective reset
1	1	System reset

PARAMETER xxxxx0 - CLEAR ALL OUTPUT TAG LINES

This parameter clears all output tag lines and clears the BUS 0 Out data lines. The channel initially clears the Channel Done flag and sets the Channel Busy flag. Upon completion, the Channel Done flag sets, and the Channel Busy flag clears.

PARAMETER xxxxx1 - INTERFACE DISCONNECT

This parameter sends an interface disconnect function to the currently selected control unit. The function initially clears the Channel Done flag and sets the Channel Busy flag. Sending the Interface Disconnect functions consists of dropping the selct-out and hold-out tag lines while holding the address-out tag line high.

The control unit responds to the interface disconnect by clearing all input tag lines to the BMC-5. When the control unit reaches the normal ending point in its sequence, it attempts to gain selection to present accumulated status to the BMC-5. The interface disconnect function itself does not generate any status.

The device path for the peripheral device remains busy after it receives an interface disconnect until the device-end status is accepted by the BMC-5.

The function should complete in about 7 microseconds. When it completes, the IOP Channel Done flag sets, and the Channel Busy flag clears.

The IOP Channel Done flag sets and the Channel Busy flag remains set if the operational-in signal from the equipment does not clear within 6 microseconds from the function issue, indicating the error condition.

PARAMETER xxxxx2 - SELECTIVE RESET

This parameter performs the selective reset function, clearing and resetting the currently selected peripheral device only. At the start, the Channel Done flag clears and the Channel Busy flag sets. The function sets the operational-out and suppress-out tags. About 250 nanoseconds later, the function clears the operational-out, hold-out, and select-out tags. Holding suppress-out set and dropping operational-out is the selective reset signal to the control unit.

The control unit responds to the selective reset by dropping the operational-in tag and resetting the currently selected peripheral device. The status of the peripheral device is also reset. If a data transfer was in process at the peripheral device, the transfer continues to a normal stopping point, then stops. The device-end status of the

peripheral device is retained for transfer to the IOS channel after the selective reset.

The ready or not ready state of the control unit is generally not changed by the selective reset function. The function completes in about 7 microseconds, at which time the IOS Channel Busy flag clears and the Channel Done flag sets.

PARAMETER xxxxx3 - SYSTEM RESET

This parameter selects the system reset function. The system reset function resets all peripheral devices and control units that are on-line. The status for each peripheral device is also reset. The Channel Done flag clears and the Channel Busy flag sets at the beginning of execution. Next, the Channel Busy flag clears operational-out and suppress-out concurrently.

The control unit responds to the system reset by dropping the operational-in tag. The system reset causes all of the on-line control units and peripheral devices to be reset.

The function completes in about 6 microseconds, at which time the IOS Channel Done flag sets and the Channel Busy flag clears. Input tag lines that are not reset by the system reset function cause both the Channel Busy and Channel Done flags to set, indicating an error condition.

BMA : 2 - CHANNEL COMMAND

This function sends commands to the control units. The specific command is selected by the accumulator bits at the same time the function issues. Many of the commands require prior functions to set up interface registers (for example, the Local Memory Address register, the Byte Count register, and the Device Address register). At the beginning of the execution, the Channel Done flag clears and the Channel Busy flag sets. When the function completes, the Channel Busy flag clears and the Channel Done flag sets. Table 3-3 shows IBM command bit accumulator values assigned to each command name. Bits 2^0 through 2^7 are command bits for the BMA : 2 parameter; accumulator bits 2^{15} through 2^8 are not used.

The specific modifier codes and the particular mode that will be set depend on the IBM-type control unit and the peripheral device used. Refer to the applicable IBM control unit and device manuals for the actual interpretations of each command.

Table 3-3. IBM Command Bit Assignments

Command Name	IBM Command Bits								
	P	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Test	P	M	M	M	M	0	0	0	0
Test I/O	1	0	0	0	0	0	0	0	0
Sense	P	M	M	M	M	0	1	0	0
Sense ID	1	1	1	1	0	0	1	0	0
Read Backward	P	M	M	M	M	1	1	0	0
Write	P	M	M	M	M	M	M	0	1
Read	P	M	M	M	M	M	M	1	0
Control	P	M	M	M	M	M	M	1	1

M = Modifier Bit
P = Parity Bit

All commands begin with an initial selection sequence in which the command byte is sent to the control unit. The initial selection sequence ends with either an ending status (channel-end or channel-end with device-end), a zero status, or an error status. To a command calling for transfer of status, control, or data bytes, a zero status signifies that the transfer can begin. All commands except Test I/O can require a data transfer to complete the command function.

A data-type transfer ends when the byte count decrements to zero and no data chaining condition exists. The data-type transfer also ends when status-in is received in response to service-out or data-out.

The Channel Done flag does not set until the processing of the control sequence is completed and data (if required) is transferred to or from Local Memory. The Channel Busy flag clears if no errors are detected.

Figure 3-1 shows the IBM signal sequence for a read to the I/O Processor.

BMA : 3 - READ REQUEST-IN ADDRESS

This function clears the Channel Done flag and sets the Channel Busy flag. When it is necessary for a control unit to send the device address and status to the channel, it raises the request-in tag line. This function recognizes the request-in tag and stores the device address.

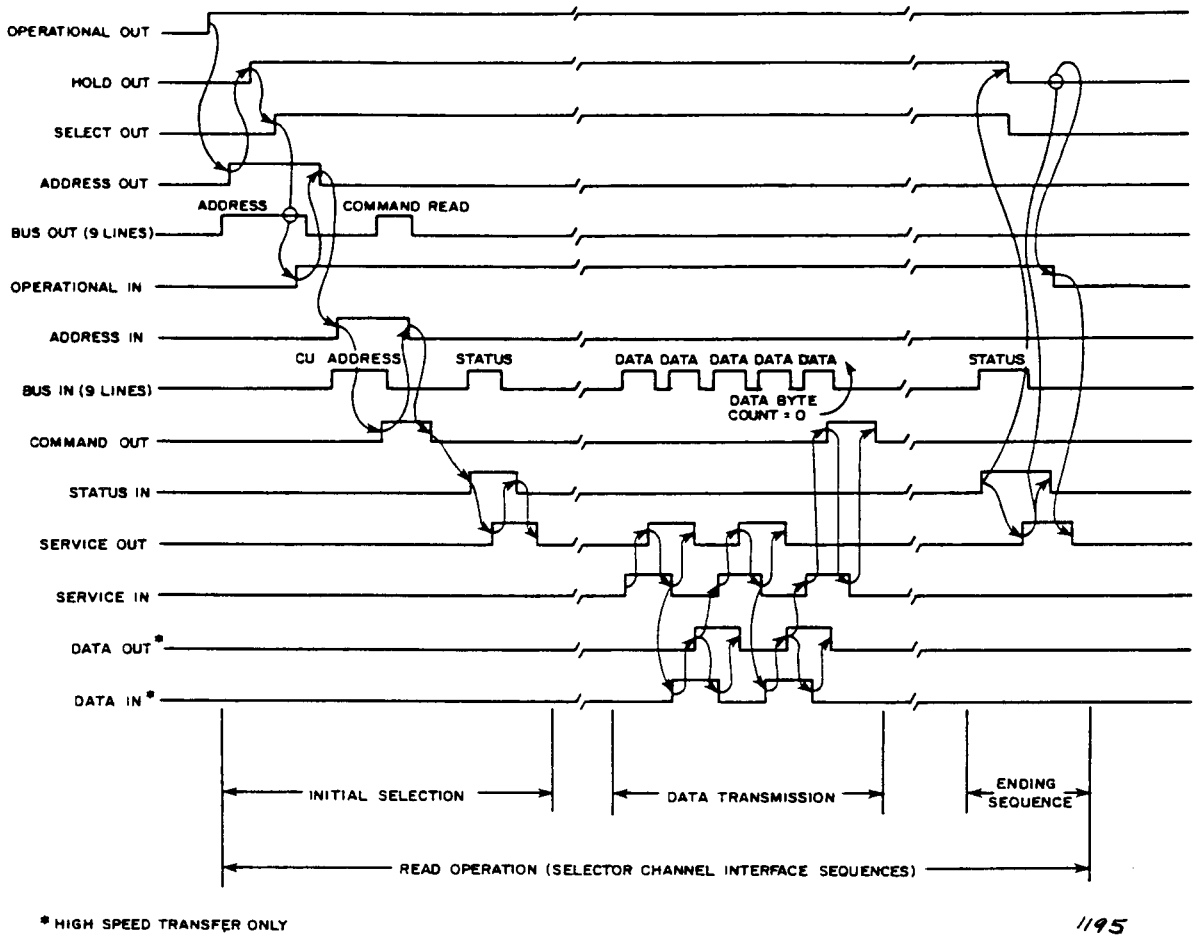

Figure 3-1. BMC-5 Channel Read Sequence

This function may begin in one of two ways depending on values stored in the IOP accumulator when the function issues.

If the accumulator equals zero, the request-in tag line is checked to see if it is active. If the tag line is active, the sequence proceeds as described below. If it is not active, the function ends and sets the Channel Done flag and clears the Channel Busy flag.

If the accumulator equals three, the channel waits for the request-in line to be active. If request-in is detected or goes active when the function issues, the sequence proceeds as follows. Time-out protection should be provided in the IOP software to prevent waiting indefinitely for request-in to go active.

The sequence then proceeds to accept the device address byte presented on the Bus-0 In lines. Byte parity is checked to ensure address validity. The device address is stored in the status register.

At this point, the operation can proceed in two different ways, depending on the value of bit 2^5 in the mode register. Figure 3-2 shows the sequences.

If mode bit 2^5 equals 0, and no parity error was detected, the sequence ends with Channel Done set and Channel Busy cleared.

If mode bit 2^5 equals 1, the BMA : 4 command sequence (see the following description) automatically begins to start the transfer of the status and address to the IOP. This saves the processing of one interrupt and the issuing of one BMA : 4 function.

BMA : 4 - SINGLE-BYTE I/O

This function loads the IOP accumulator with 1 byte of status information. The function initially clears the Channel Done flag and sets the Channel Busy flag. The operational-in and address-in input tag lines are checked to see if they are active; the sequence waits until they become active. When they are active, the command-out tag line is set indicating the control unit can proceed. The control unit sends the single byte of status information that the channel loads into the status register. The sequence is shown in the lower part of figure 3-2. The Channel Busy flag clears (if there was no parity error) and the Channel Done flag sets after the status byte is stored.

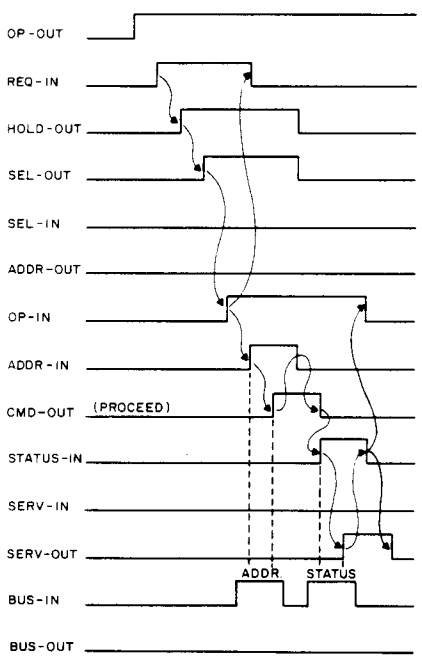

Figure 3-2. BMA : 3 and 4 Request-in Channel Sequences

NOTE

If asynchronous data and status processing takes place in interrupt mode, request-in must be cleared and disable before issuing the BMA : 3 function in the following way:

```
BMA : 6             .Clear request-in
A = 0
BMA : 16            .Disable request-in
BMA : 0             .Clear interrupt
```

A constant interrupt occurs if this procedure is not followed.

BMA : 5 - MAINTENANCE DELAY

This function sets delays for maintenance purposes. Initially, the Channel Done flag clears and the Channel Busy flag sets. The channel then performs one of the following delays, depending on the value in the IOP accumulator:

Accumulator Value	Delay
0	10 microseconds
1	5 microseconds
2	2.5 microseconds
3	1 microseconds

The Channel Done flag sets and the Channel Busy flag clears after the delay times out, with the exception of the 1-microsecond delay. After the 1 microsecond delay, both the Channel Done and Channel Busy flags are set. This is an error condition for maintenance purposes only.

BMA : 6 - CLEAR CHANNEL INTERRUPT ENABLE FLAG

This function clears the Channel Interrupt Enable flag, preventing the channel from interrupting the IOP. The IOP monitors the Channel Done flag. When the Interrupt Enable flag clears, the Channel Done flag does not reach the IOP. This function does not affect the Channel Done and Channel Busy flags.

BMA : 7 - SET CHANNEL INTERRUPT ENABLE FLAG

This function sets the Channel Interrupt Enable flag, allowing the channel to interrupt the IOP. The channel interrupts the IOP whenever any of the following conditions occur†:

- Channel Done flag sets
- Request-in tag line goes active and request-in interrupt select mode has been selected by a BMA : 16 function
- During data chaining, the byte counter has decremented to 0 and the last Local Memory referecne is complete for that segment of data

After a data chaining interrupt, a BMA : 6 and BMA : 7 function sequence should be performed to reset the logic.

BMA : 10 - READ LOCAL MEMORY ADDRESS

This function transfers the current Local Memory Address from the channel Local Memory Address register into the IOP accumulator. The channel logic contains two Local Memory Address registers to support data chaining. When this function issues, the value of accumulator bit 2^0 determines the register to be read. Bit 2^0 of the value returned to the accumulator identifies the register that is the source of the address.

Bit 2^1 in the value returned to the accumulator is set if data chaining is used. Table 3-4 lists the response bits sent to the accumulator.

Function BMA : 10 can be perfomed at any time relative to control functions.

NOTE

When a BMA : 14, 15, 16, or 17 function is to be followed immediately by a BMA : 10 or 11 function, a single instruction delay (012000_8) must be inserted between the functions to ensure that the Local Memory Address returned will be for the expected channel.

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† Allow 1 CP before checking the interrupt channel number (IOR : 10).

Table 3-4. Read Local Memory Address Response Bits

Accumulator Bit	Meaning
2^0	Register select status
2^1	Data-chaining flag status (1 = data-chaining)
2^2	Local Memory address 2^2
2^3	Local Memory address 2^3
2^4	Local Memory address 2^4
2^5	Local Memory address 2^5
2^6	Local Memory address 2^6
2^7	Local Memory address 2^7
2^8	Local Memory address 2^8
2^9	Local Memory address 2^9
2^{10}	Local Memory address 2^{10}
2^{11}	Local Memory address 2^{11}
2^{12}	Local Memory address 2^{12}
2^{13}	Local Memory address 2^{13}
2^{14}	Local Memory address 2^{14}
2^{15}	Local Memory address 2^{15}

Function BMA : 10 has a programming restriction due to timing in the IOP Adder and Shifter. The restriction applies if the IOP instruction preceding a BMA : 10 function is any of the following: 4 through 7, 12, 13, 16, 17, 22, 23, 32, 33, 44 through 47, 52, 53, 62, or 63. In these cases insert a logical product instruction 011 or 015 with the *d* or *k* fields set to all 1's, between the above listed instruction and the BMA : 10 function.

BMA : 11 - READ BYTE COUNTER

The byte counter records the number of bytes remaining in a data transfer. The counter is initially loaded with a value by a BMA : 15 enter byte count function. The counter decrements byte-to-byte to 0; upon reaching 0, the channel interrupts the IOP to terminate the transfer. A transfer terminated by a control unit rather than by decrementing the byte counter to 0 can result in a nonzero value remaining in the counter. If data chaining is requested, each segment transfer decrements the byte counter to 0, and the counter is reloaded for the next segment transfer. This function does not affect the Channel Busy and Channel Done flags.

Due to the fixed timing in the IOP, this function must be issued twice in succession to get a current byte counter status to the IOP accumulator. The first execution moves the byte counter status to the block multiplexer controller. The second execution moves the status to the IOP accumulator.

Function BMA : 11 can be used to verify the accumulator fanout, the intermediate Byte Counter Status register in the block multiplexer controller, and the status path back to the IOP accumulator. Issuing a BMA : 15 function loads the byte count into the Byte Counter Status register in the block multiplexer controller. The next BMA : 11 function reads the byte count back from the Byte Counter Status register to the IOP accumulator. The second BMA : 11 function performs as described above.

NOTE

When a BMA : 14, 15, 16, or 17 function is to be followed immediately by a BMA : 10 or 11 function, a single instruciton delay (012000_8) must be inserted between the functions to ensure that the Local Memory Address returned will be for the expected channel.

BMA : 12 - READ STATUS AND ADDRESS

The Status register holds the device address and status mode bits that were read from the block multiplexer channel. This function reads the status/address information into the IOP accumulator. Table 3-5 shows the status/address bits as they arrive in the accumulator. This function does not affect the Channel Busy and Channel Done flags.

Due to the fixed timing in the IOP, function BMA : 12 must be executed twice in immediate succession to get valid status/address information to the IOP accumulator. The first execution moves the current status/address to the block multiplexer controller. The second execution moves the status/address to the IOP accumulator.

This function can verify the accumulator fanout, the intermediate Status register in the block multiplexer controller, and the status path back to the IOP accumulator. Issuing a BMA : 16 function loads address and mode bits into the block multiplexer controller Status register. The next BMA : 12 function reads the status/address back to the accumulator.

Table 3-5. BMA : 12 Status/Address Bits

Accumulator Bit	Meaning
2^0	Status 2^0
2^1	Status 2^1
2^2	Status 2^2
2^3	Status 2^3
2^4	Status 2^4
2^5	Status 2^5
2^6	Status 2^6
2^7	Status 2^7
2^8	Address 2^0
2^9	Address 2^1
2^{10}	Address 2^2
2^{11}	Address 2^3
2^{12}	Address 2^4
2^{13}	Address 2^5
2^{14}	Address 2^6
2^{15}	Address 2^7

BMA : 13 READ INPUT TAGS

This function reads the states of the input tag lines and transfers the values to the IOP accumulator. Due to the fixed timing in the IOP, this function must be exectued twice in immediate succession to get valid input tags to the accumulator. The first execution brings the input tags from the channel logic to the Intermediate Output Tags register. The second execution moves the input tags to the IOP accumulator. This function does not affect the Channel Busy and Channel Done flags.

Table 3-6 lists the input tags and the accumulator bit positions assigned to each tag. Some of the bits returned to the accumulator are status bits rather than input tags. Their descriptions are included in the table.

This function can verify the accumulator fanout, the Intermediate Output Tags register, and the path back to the accumulator. Issuing a BMA : 17 function loads the accumulator parcel into the controller Intermediate Output Tags register into the accumulator, and stages the input tags into the Intermediate Output Tags register. The second BMA : 13 function brings the stored input tags from the register to the IOP accumulator.

Table 3-6. BMA : 13 Read Input Tags Accumulator Bits

Accumulator Bit	Name	Description
2^0	Operational In	
2^1	Address In	
2^2	Disconnect In	
2^3	Select In	
2^4	Request In	
2^5	Service In	
2^6	Data In	
2^7	Status In	
2^8	Metering In	
2^9	Retry Status	When set, Command Retry is being requested
2^{10}	Data Streaming	When set, Data Streaming is selected
2^{11}	Data Buffer Pointer	Shows which Data Buffer is being used (0 or 1)
2^{12}	Address Miscompare	When set, the incoming Device Address does not match the one sent out
2^{13}	Byte Count Zero	When set, the planned number of bytes (byte count) has been transferred
2^{14}	PROM Parity Error	When set, a parity error was found on the control word read from the microsequencer Programmable Read Only Memory
2^{15}	BUS-IN Parity Error	When set, a parity error was found on the data or address on the Bus-In lines

BMA : 14 - LOAD LOCAL MEMORY ADDRESS

This function loads the current accumulator parcel into the controller Local Memory Address register. This parcel becomes the starting address in IOP Local Memory for the transfer. The Channel Busy and Channel Done flags are not altered by this function.

Two Local Memory Address registers are maintained for data chaining. They are addressed by the 2^0 bit of the accumulator. Data chaining must begin with Local Memory Address register 0 and alternate between the 0 and 1 registers as segments are transferred.

Select data chaining by setting bit 2^1 in the accumulator parcel before issuing this function. When set, data chaining is set and remains set for the rest of the transfer. This function automatically clears the data chaining interrupt after a data transfer has completed.

Table 3-7 lists the accumulator bits for function BMA : 14.

Table 3-7. BMA : 14 Load Local Memory Address Accumulator Bits

Accumulator Bit	Meaning
2^0	Local Memory Address register file select
2^1	Data-chaining flag
2^2	Local Memory Address 2^2
2^3	Local Memory Address 2^3
2^4	Local Memory Address 2^4
2^5	Local Memory Address 2^5
2^6	Local Memory Address 2^6
2^7	Local Memory Address 2^7
2^8	Local Memory Address 2^8
2^9	Local Memory Address 2^9
2^{10}	Local Memory Address 2^{10}
2^{11}	Local Memory Address 2^{11}
2^{12}	Local Memory Address 2^{12}
2^{13}	Local Memory Address 2^{13}
2^{14}	Local Memory Address 2^{14}
2^{15}	Local Memory Address 2^{15}

BMA : 15 - ENTER BYTE COUNT

This function loads the accumulator contents into either the Byte Counter or the Next Byte Count register. The first BMA : 15 function following a BMA : 14 function enters the accumulator contents into the Byte Counter. When a second BMA : 15 immediately follows the first BMA :15, the second accumulator contents are entered into the Next Byte Count register. The Channel Busy and Channel Done flags are not affected by this function.

The transfer from the Next Byte Count register to the Byte Counter is done automatically between data segments during data chaining. Channel commands requiring no data, parameters, or status must establish a byte count of 0. The maximum byte count is 65,535 bytes.

BMA : 16 - ENTER DEVICE ADDRESS/MODE

This function loads the accumulator contents into the Device Address register. The Device Address register contains the address for the active peripheral device, as well as several operating mode bits for the controller. The device address can be a combination of peripheral controller address bits and peripheral device address bits.

The Channel Done and Channel Busy flags are not affected by this function. Table 3-8 shows the BMA : 16 Device Address register bits, name, and a description of the mode bits.

Table 3-8. BMA : 16 Device Address Accumulator Bits

Accumulator Bit	Name	Description
2^0	Address/data out 2^0	
2^1	Address/data out 2^1	
2^2	Address/data out 2^2	
2^3	Address/data out 2^3	
2^4	Address/data out 2^4	
2^5	Address/data out 2^5	
2^6	Address/data out 2^6	
2^7	Address/data out 2^7	
2^8	Skip flag	When set, prohibits storing data into Local Memory during read transfers
2^9	Stack Status flag	When set, a status byte has been sent to the controller from the device but has not yet been accepted. The status byte is held at the device.
2^{10}	Command chaining mode select 2^0	See text and table 3-9
2^{11}	Command chaining mode select 2^1	See text and table 3-9
2^{12}	Request-In Interrupt enable	Enables arrival of Request-In to generate IOP interrupt
2^{13}	Mode bit 2^5	Automatic transfer of status and address in BMA : 3
2^{14}	Channel mode select 2^0	See text and table 3-10
2^{15}	Channel mode select 2^1	See text and table 3-10

Bits 2^8 through 2^{15} of the accumulator parameter are called mode bits and are re-established during each BMA : 16 function. They operate as follows.

Bit 2^8 is the mode bit for the Skip flag. When set, it prohibits storing data into Local Memory during read data transfers.

Bit 2^9 is the mode bit for the Stack Status flag.

Bit 2^{10} and 2^{11} select the mode in which command chaining will be used. Table 3-9 shows the translation of these mode bits.

Table 3-9. Command Chaining Mode Selections

Parameter Bits		Selection
2^{11}	2^{10}	
0	0	No chaining
0	1	Chain if channel-end status is detected
1	0	Chain if device-end status is detected
1	1	Chain if either channel-end status or device-end status is detected

Parameter Bits 2^{12} and 2^{13} select the mode in which interrupts are generated. Refer to the previous explanation of the BMA : 3 function.

Parameter Bits 2^{14} and 2^{15} select the type of channel protocol to be used. The selection is shown in table 3-10.

Table 3-10. Channel Protocol Selections

Parameter Bits		Selection
2^{15}	2^{14}	
0	0	Selector channel
0	1	Data streaming channel
1	0	Block multiplexer channel
1	1	Reserved

BMA : 17 - ENTER OUTPUT TAGS

This function enters the accumulator content into the Output Tags register. Direct program control of the output tags allows the use of special control and diagnostic sequences. This function does not alter the Channel Busy and Channel Done flags.

Bits 2^0 through 2^9 are output tags; bits 2^{10} through 2^{15} are control bits used for maintenance and diagnostic purposes. Table 3-11 shows the accumulator bit assignments for the BMA : 17 function.

Table 3-11. BMA : 17 Output Tags Register Bits

Accumulator Bit	Meaning
2^0	Operational out
2^1	Address out
2^2	Hold out
2^3	Select out
2^4	Command out
2^5	Service out
2^6	Data out
2^7	Suppress out
2^8	Metering out
2^9	Mark 0 out
2^{10}	Gate address to Bus 0 out

Table 3-11. BMA : 17 Output Tags Register Bits

Accumulator Bit	Meaning
2^{11}	Strobe Bus 0 In to Address register
2^{12}	Clock out
2^{13}	Inhibit parity error
2^{14}	Force Bus out parity
2^{15}	Test point for program sync

The following subsections describe the function control bits 2^{10} through 2^{15}.

BIT 2^{10} - GATE ADDRESS TO BUS 0 OUT

Setting this bit in the accumulator parameter transfers the device address from the Device Address register (bits 2^0 through 2^7) directly to the Bus 0 Out 2^0 - 2^7 data lines.

BIT 2^{11} - STROBE BUS 0 IN TO ADDRESS REGISTER

Setting this bit in the accumulator parameter transfers the Bus 0 In data bits to the Device Address register.

BIT 2^{12} - CLOCK OUT

When this bit is set in the accumulator, the Clock-out tag line is set to a logical one. The tag line is steady until the next function issues to change the operation or to change this accumulator parameter bit.

BIT 2^{13} - INHIBIT PARITY ERROR

Setting this bit in the accumulator parameter prevents reporting parity errors that occur on the Bus 0 In data lines. This feature is for maintenance purposes. This mode stays set until it is cleared by a BMA : 17 function with this parameter bit cleared in the accumulator.

BIT 2^{14} - FORCE BUS 0 OUT PARITY

When this bit is set in the accumulator, the Bus 0 Out Parity bit is toggled from its normal correct state. In this mode, the current byte being sent over the bus is accompained by an incorrect parity bit state, so each byte should trigger a parity error at the peripheral controller or peripheral device. This mode is set for only one byte transfer.

BIT 2^{15} - TESTPOINT FOR PROGRAM SYNC

Setting this bit in the accumulator parameter causes a 2IW module test point to go to a logical 1 state. This test point can be monitored, by a field engineer using an oscilloscope, to determine the time when this BMA : 17 function issues. The test point clears when the next function issues.

PROGRAMMING EXAMPLES

The following examples illustrate two programming sequences for the block multiplexer channel. Example 1 shows the function sequence used to read a tape record of unknown length. Example 2 shows how to rewind the tape.

Example 1:

$Accumulator_8$	Function	Description
000000	BMA : 14	Set IOMA = 0 (arbitrary)
000000	BMA : 15	Set byte count = 0
000025	BMA : 16	Set device address (0-255)
000323	BMA : 2	Select GCR tape mode
	Wait for "Done"	
BUFA+2	BMA : 14	Set IOMA, chaining flag Buffer A
BUFB+3	BMA : 14	Set IOMA, chaining flag Buffer B
000005	BMA : 15	Set byte count Buffer A (header)
001000	BMA : 15	Set byte count Buffer B (1-65535)
000002	BMA : 2	Function read forward command
	Wait for interrupt	

Example 1 (continued):

$Accumulator_8$	Function	Description
BUFA+2	BMA : 14	Set IOMA, chaining flag, Buffer A
001000	BMA : 15	Set byte count Buffer A
		(1-65535)
	Wait for interrupt	Process header
BUFB+3	BMA : 14	Set IOMA, chaining flag Buffer B
001000	BMA : 15	Set byte count Buffer B
	Wait for interrupt	Transfer Buffer B to Buffer Memory
BUFA+2	BMA : 14	Set IOMA, chaining flag Buffer A
001000	BMA : 15	Set byte count Buffer A (1-65535)
	Wait for interrupt	Transfer Buffer A to Buffer Memory
	"Done" set	
	BMA : 11	
1000-X	BMA : 11	Read byte counter for residue transfer X bytes, Buffer B to Buffer Memory
	BMA : 12	
	BMA : 12	Verify device status
	BMA : 13	
	BMA : 13	Check input P.E. etc.

Example 2:

$Accumulator_8$	Function	Description
000000	BMA : 14	Set IOMA = 0 (arbitrary)
000000	BMA : 15	Set byte count = 0
000025	BMA : 16	Set device address (0-255)
000007	BMA : 2	REWIND function
	Wait for "Done"	
	Check for "Busy"	"Busy" set indicates error
	BMA : 12	

Example 2 (continued):

Accumulator$_8$	Function	Description
	BMA : 12	Verify device address and status
	BMA : 13	
	BMA : 13	Check for other errors

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