IOS™ Model E Hardware Maintenance Manual

CMM-xxxx-PR2

2/91
PRELIMINARY INFORMATION

Cray Research Proprietary

Cray Research, Inc.

Any shipment to a country outside of the United States requires a letter of assurance from Cray Research, Inc.

Requests for copies of Cray Research, Inc. publications should be directed to:

CRAY RESEARCH, INC.
Logistics
6251 South Prairie View Road
Chippewa Falls, WI 54729

Comments about this publication should be directed to:

CRAY RESEARCH, INC.
Hardware Publications and Training
770 Industrial Blvd.
Chippewa Falls, WI 54729

Reader Comment Form

Title: **IOS™ Model E Hardware Maintenance Manual** **Number:** **CMM-xxxx-PR2**

Your feedback on this publication will help us provide better documentation in the future. Please take a moment to answer the few questions below.

For what purpose did you primarily use this manual?

_____Troubleshooting
_____Tutorial or introduction
_____Reference information
_____Classroom use
_____Other - please explain _____

Using a scale from 1 (poor) to 10 (excellent), please rate this manual on the following criteria and explain your ratings:

_____Accuracy _____
_____Organization _____
_____Readability _____
_____Physical qualities (binding, printing, page layout) _____
_____Amount of diagrams and photos _____
_____Quality of diagrams and photos _____

Completeness (Check one)

_____Too much information _____
_____Too little information _____
_____Just the right amount of information

Your comments help Hardware Publications and Training improve the quality and usefulness of your publications. Please use the space provided below to share your comments with us. When possible, please give specific page and paragraph references. We will respond to your comments in writing within 48 hours.

NAME_____
JOB TITLE_____
FIRM_____
ADDRESS_____
CITY_____STATE_____ZIP_____
DATE_____

[or attach your business card]

CRAY RESEARCH, INC.

CUT ALONG THIS LINE

Fold

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY CARD

FIRST CLASS PERMIT NO 6184 ST. PAUL, MN

POSTAGE WILL BE PAID BY ADDRESSEE

CRAY RESEARCH, INC.

Attn: Hardware Publications & Training
770 Industrial Boulevard
Chippewa Falls, WI 54729

Fold

STAPLE

Record of Revision

Each time this manual is revised and reprinted, all changes issued against the previous version are incorporated into the new version, and the new version is assigned an alphabetic level which is indicated in the publication number on each page of the manual.

Changes to part of a page are indicated by a change bar in the margin directly opposite the change. A change bar in the footer indicates that most, if not all, of the page is new. If the manual is rewritten, the revision level changes but the manual does not contain change bars.

REVISION	DESCRIPTION
	November 1990 - Preliminary Information.
	February 1991 - Preliminary version for classroom use only. Sections 1 and 9 have been updated.

CONTENTS

1 INTRODUCTION

2 I/O PROCESSOR

3 CLUSTER INTERFACE AND WORKSTATION INTERFACE

4 BUFFER BOARD

5 HCM HIGH-SPEED/LOW-SPEED QUARTER BOARD

6 CCA1 LOW-SPEED QUARTER BOARD

7 DCA1 DISK DRIVE QUARTER BOARD

8 DCA2 IPI DISK DRIVE CONTROLLER QUARTER BOARD

9 TCA1 TAPE CONTROLLER QUARTER BOARD

10 HCA3/HCA4 HIPPI QUARTER BOARDS

FIGURES

FIGURES (continued)

TABLES

1 INTRODUCTION

The IOS Model E is divided into clusters and operates with a 6.25 ns clock. There are a maximum of eight clusters in an IOS-E chassis or four in a CRAY Y-MP4E chassis or two in a CRAY Y-MP2E chassis. Each cluster has from one to five I/O processors (IOPs). All five IOPs are identical; they contain the same components and execute the same instruction set. However, there are two types of IOPs in each cluster: IOP MUX and the EIOPs. The only difference between the IOP MUX and the EIOPs are the devices they control. There is one IOP MUX and it controls the high-speed (HISP) channels to the mainframe and solid-state storage device (SSD) and the low-speed (LOSP) channels to the mainframe. There are from one to four EIOPs and they control the channel adapters that connect the I/O subsystem (IOS) to peripheral devices such as disk drives, tape drives, and communication channels. Refer to Figure 1-1 for a functional IOS-E cluster block diagram.

The IOS-E has another configuration called a single IOP cluster. In this configuration there is only one IOP. This IOP acts as the IOP MUX and EIOP0. The single IOP controls the HISPs to the mainframe and SSD, the LOSP to the mainframe, and the peripheral devices.

The IOS-E keeps the IOPs, channel adapters, HISPs, and LOSPs operating on the same time with the use of a sync pulse. The sync pulse is sent to all the hardware from the buffer board every 37.5 ns, which is equal to once every 6 clock periods (CPs).

The buffer board has 20_8 circular buffers to buffer the data between the central processing unit (CPU) and the peripheral devices. Each buffer holds 64K words. Each word is 64 bits of data and 8 check bits. The memory chips are 64K x 4 with a 18.75 ns access time. Each EIOP controls four of the buffers. The HISPs can write to and read from all buffers. Each channel adapter can write to and read from one buffer only. Each buffer has four pointers that are used to read and write the buffer: a, b, A, and B. The channel adapters use the a and b pointers. The HISP and channels 26 and 27 use the A and B pointers. The a and b pointers read and write the buffer board from sync 0 to 2. The A and B pointers read and write the buffer board from sync 3 to 5.

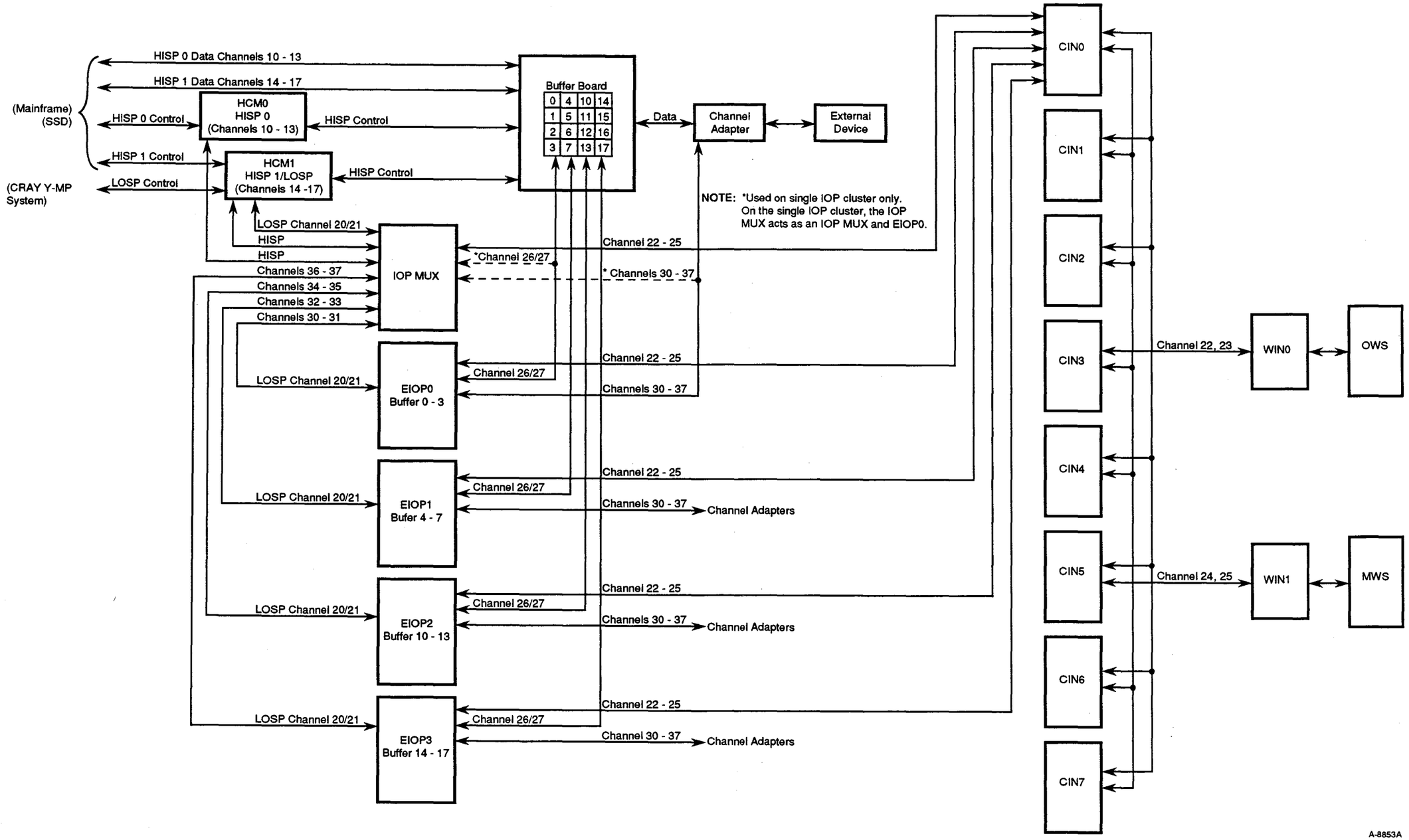


Figure 1-1. Cluster Block Diagram

Power Side → Cooling Side

IOP Module

A3 HCM1 (F) Channel 14 - 17, LOSP 20/21	A2 CIN (N)	A1 IOP MUX (F)	A0 HCM0 (N) Channel 10 - 13
B3 EIOP3 (F)	B2 EIOP2 (N)	B1 EIOP1 (F)	B0 EIOP0 (N)

Buffer Module

BUF 12 -- EIOP2 34/35 BUF 13 -- EIOP2 36/37	BUF 10 -- EIOP2 30/31 BUF 11 -- EIOP2 32/33	BUF 2 -- EIOP0 34/35 BUF 3 -- EIOP0 36/37	BUF 0 -- EIOP0 30/31 BUF 1 -- EIOP0 32/33
BUF 16 -- EIOP3 34/35 BUF 17 -- EIOP3 36/37	BUF 14 -- EIOP3 30/31 BUF 15 -- EIOP3 32/33	BUF 6 -- EIOP1 34/35 BUF 7 -- EIOP1 36/37	BUF 4 -- EIOP1 30/31 BUF 5 -- EIOP1 32/33

Channel Adapter Module

A3 CA - 12 (N) EIOP2 34/35	A2 CA - 10 (N) EIOP2 30/31	A1 CA - 2 (N) EIOP0 34/35	A0 CA - 0 (N) EIOP0 30/31
B3 CA - 13 (N) EIOP2 36/37	B2 CA - 11 (N) EIOP2 32/33	B1 CA - 3 (N) EIOP0 36/37	B0 CA - 1 (N) EIOP0 32/33

Channel Adapter Module

A3 CA - 17 (N) EIOP3 36/37	A2 CA - 15 (N) EIOP3 32/33	A1 CA - 7 (N) EIOP1 36/37	A0 CA - 5 (N) EIOP1 32/33
B3 CA - 16 (N) EIOP3 34/35	B2 CA - 14 (N) EIOP3 30/31	B1 CA - 6 (N) EIOP1 34/35	B0 CA - 4 (N) EIOP1 30/31

Clock Module

A3 Not Used (F)	A2 WIN1 (MWS) (N)	A1 WIN0 (OWS) (F)	A0 Not Used (N)
Clock	Clock	Clock	Clock

NOTE: (N) = Normal Position on Cold Plate
(F) = Flipped Position on Cold Plate

A-8921A

Figure 1-2. Cluster Module Layout

The operator's workstation (OWS) and the maintenance workstation (MWS) have the ability to communicate directly with all IOPs through the cluster interfaces (CIN) and workstation interfaces (WIN). There are two WINs; one is connected to the OWS and the other is connected to the MWS. Both WINs are connected to all the CINs. There are from one to eight CINs. Each cluster has its own CIN and each IOP of that cluster is connected to the CIN.

IOS-E Modules

There are four modules for each cluster, plus a clock module that is shared by all clusters. The IOS-E modules can be comprised of full boards, half boards, or quarter boards. Each module has only one cold plate, so there is only an A and a B side. Refer to Figure 1-2 for a module block diagram.

The first module consists of the five IOP quarter boards, two HCM quarter boards, and one CIN quarter board. The second module is the buffer module. The buffer module has a full board on each side and is the only module that uses jumper pins to connect the A and B boards. The third module is for the channel adapters belonging to EIOP0 and 2. The fourth module is for the channel adapters belonging to EIOP1 and 3. The channel adapters can be full, half, or quarter boards. The clock module has two WIN quarter boards on the A side and a full clock board on the B side. A dummy quarter board is used when there is no quarter board needed. The dummy board has a burn foil on it.

I/O Processor

Each IOP is a 16-bit (1-parcel) computer designed to control data transfers in and out of the IOS. Each IOP executes a set of 128 instructions. Refer to Section 7, "I/O Processor Instruction Set," of the IOS Model E System Programmer Reference Manual (CSM-xxxx-PR1) for detailed information about each instruction.

Each IOP contains four major sections: control section, computation section, local memory section, and the I/O section. Refer to Section 2, "I/O Processor," of the IOS Model E System Programmer Reference Manual (CSM-xxxx-PR1) for detailed information about the IOP.

The control section fetches and decodes instructions, and controls branches, interrupts, and subroutine calls and returns. Its major components are the instruction stack, program address (P) register, next instruction parcel (NIP) register, current instruction parcel (CIP) register, exit stack, and real-time clock (RTC).

The computation section provides temporary data storage and performs logical, arithmetic, and shift operations. Its major components are the accumulator, add and shift functional units, operand registers, B register, and base register.

The local memory section contains 64K parcels of random access memory (RAM) which is protected with single-error correction/double-error detection (SECDED) logic on each parcel of data. Local memory has two direct memory access (DMA) ports. These DMA ports are shared by the channel adapters, HISP channels, LOSP channels, and the buffer board channel to read and write local memory.

The I/O section controls the 29 I/O channels.

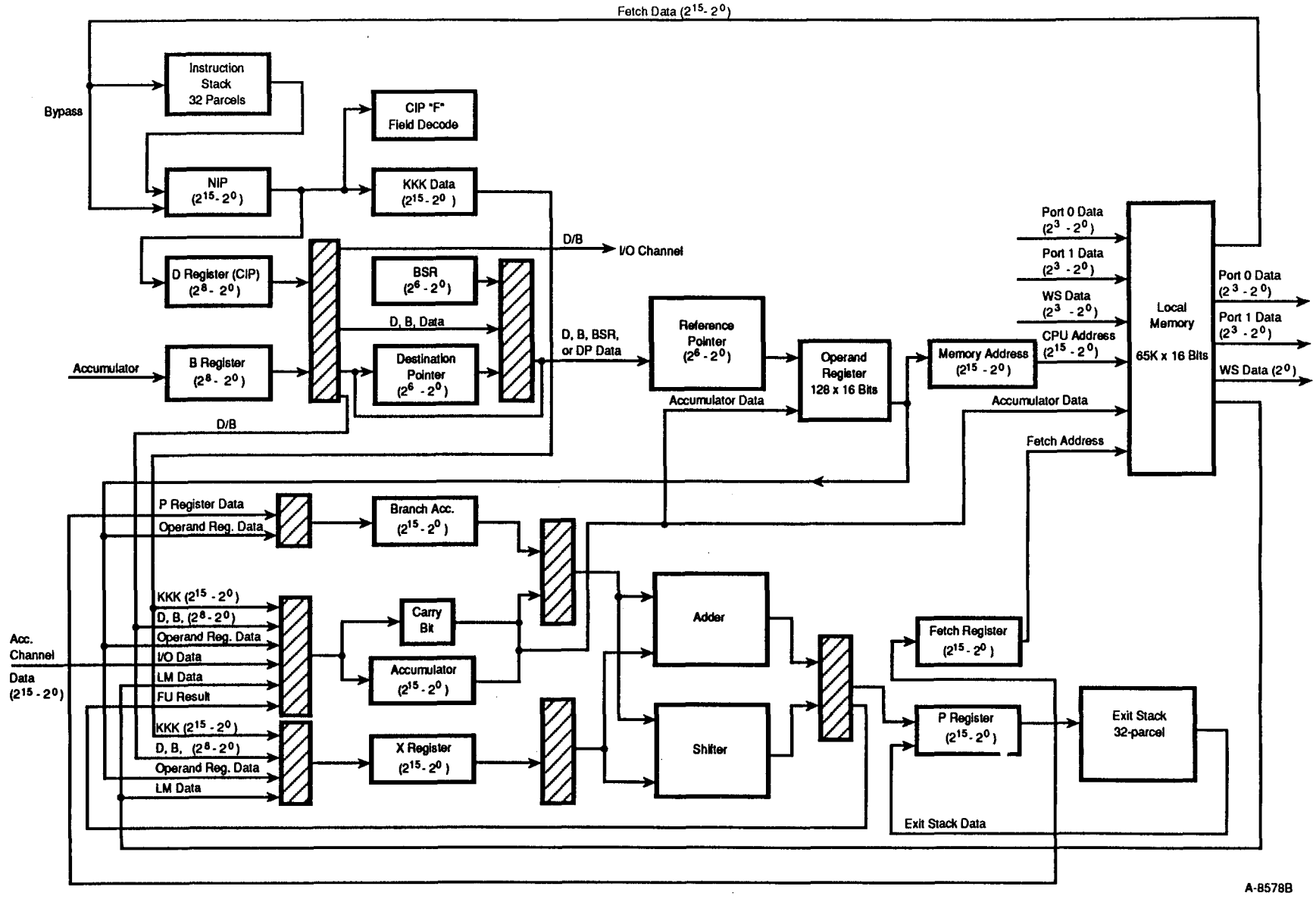


Figure 1-3. I/O Processor Functional Diagram

I/O Channels

The I/O has 29 I/O channels: 5 internal channels and 24 external channels. Refer to Table 1-1 for the I/O channel assignments and Figure 1-1 for a channel block diagram.

Table 1-1. IOS-E Channels

Channel Number	IOP MUX Type	IOP MUX DMA Port	EIOPs Type	EIOPs DMA Port	Single IOP Cluster Type	Single IOP Cluster DMA Port
0	I/O request	N/A	I/O request	N/A	I/O request	N/A
2	Program exit stack	N/A	Program exit stack	N/A	Program exit stack	N/A
3	Local memory error	N/A	Local memory error	N/A	Local memory error	N/A
4	RTC	N/A	RTC	N/A	RTC	N/A
7	Base register	N/A	Base register	N/A	Base register	N/A
10 and 12	HISP 0 input	0	Not used		HISP 0 input	0
11 and 13	HISP 0 output	0	Not used		HISP 0 output	0
14 and 16	HISP 1 input	1	Not used		HISP 1 input	1
15 and 17	HISP 1 output	1	Not used		HISP 1 output	1
20 and 21	LOSP CPU	0	MIOP	0	LOSP CPU	0
22 and 23	OWS	1	OWS	1	OWS	1
24 and 25	MWS	1	MWS	1	MWS	1
26 and 27	Not used		Buffer board	0	Buffer board	0
30 and 31	EIOP0 20, 21	0	Channel adapter 0	0	Channel adapter 0	0
32 and 33	EIOP1 20, 21	1	Channel adapter 1	1	Channel adapter 1	1
34 and 35	EIOP2 20, 21	0	Channel adapter 2	0	Channel adapter 2	0
36 and 37	EIOP3 20, 21	1	Channel adapter 3	1	Channel adapter 3	1

Channels 10 through 17

Channels 10 through 17 are HISP channels and are used by the IOP MUX. There are two sets of HISP channels: 10 through 13 and 14 through 17. There are two logical channels used for the input 10 and 12, but there is only one physical channel. There are two logical channels used for the output 11 and 13, but there is only one physical channel. The logical channels share hardware and drop cables. The logical channels stack transfers. One of the logical channels is activated and then the other channel is allowed to be programmed and activated, but if the first channel is busy the second channel must wait. The second channel is allowed to go busy when the first logical channel's done flag sets. This is true for channels 14 through 17 also. Refer to Section 4, "Low-speed and High-speed Channels," of the IOS Model E System Programmer Reference Guide (CSM-xxxx-PR1) for more information on HISP data transfers.

Channels 20 and 21

Channels 20 and 21 perform different functions in the IOP MUX and EIOPs. In the IOP MUX channels 20 and 21 are connected to the CPUs LOSP channels. They are used to deadstart the CPU and to exchange packets of information. In the EIOPs, channels 20 and 21 are connected to 30 through 37 of the IOP MUX. The EIOPs and the IOP MUX exchange information packets on these channels. Refer to Table 1-2 for channel configuration. Refer to Section 4, "Low-speed and High-speed Channels," of the IOS Model E System Programmer Reference Guide (CSM-xxxx-PR1) for more information on LOSP data transfers.

Table 1-2. EIOP Channel 20, 21

EIOP	EIOP Channel	IOP MUX Channel
0	20, 21	30, 31
1	20, 21	32, 33
2	20, 21	34, 35
3	20, 21	36, 37

Channels 22 through 25

Channels 22 through 25 in each IOP transfer data between the IOP and the workstations. Channels 22 and 23 are connected to the OWS and channels 24 and 25 are connected to the MWS. Data can be transferred across these channels under control of either the IOP or the workstation. Refer to Section 6, "Cluster Interface/Workstation Interface," of the IOS Model E System Programmer Reference Guide (CSM-xxxx-PR1) for more information on workstation data transfers.

Channels 26 and 27

Channels 26 and 27 are used only by the EIOPs. These channels transfer data between local memory and the I/O buffer and program the transfers between the I/O buffer and the channel adapters. Refer to Section 3, "I/O Buffer," of the IOS Model E System Programmer Reference Guide (CSM-xxxx-PR1) for more information on I/O buffer data transfers.

Channels 30 through 37

Channels 30 through 37 perform different functions in the IOP MUX than they do in the EIOPs. In the EIOPs, these channels transfer data between local memory and the channel adapters, and they program transfers between the channel adapters and the I/O buffer. Refer to Section 5, "Channel Adapters," of the IOS Model E System Programmer Reference Guide (CSM-xxxx-PR1) for more information on channel adapter data transfers.

Channels 30 through 37 in the IOP MUX transfer data between IOP MUX and EIOP local memory. Channels 30 through 37 are connected to channels 20 and 21 of each EIOP. Refer to Table 1-2 for a channel configuration.

Channel Adapters

Each EIOP can be connected to four channel adapters. They are channels 30 through 37. The channels work in pairs to communicate with the peripheral devices: 30/31, 32/33, 34/35, and 36/37. The channel adapters control the transfer of data between the peripheral device and the buffer board. Refer to Table 1-3 and to the individual sections in this manual for more information on the channel adapters.

Table 1-3. Channel Adapters

Name	Type	Channel	Comment
CCA1	LOSP	30 - 37	Even channel is input Odd channel is output FEIs, NSC, and Front ends Quarter board
DCA1	Disk drives	30 - 37	Both channels are input and output DD-39s, DD-49s, DD-40s, DD-41s, and DD-50s Quarter board
DCA2	Disk drives	30 - 37	Both channels are input and output IPI 9 head (DD-60s) or single head (DD-61s) disk drives Quarter board
DCA3	Disk drives	30 - 37	Both channels are input and output 9 IPI in drive in parallel Full board
TCA1	Tape drives	30 - 37	Both channels are input and output IBM type tape drives Quarter board
TCA2	Tape drives	30 - 37	Both channels are input and output IPI type tape drives Quarter board
HCA3	HIPPI in	30/31, 34/35	All channels are input Quarter board
HCA4	HIPPI out	32/33, 36/37	All channels are output Quarter board
HCA5	IPI bus	30 - 37	Both channels are input and output IPI protocol Half board

2 I/O PROCESSOR

The CPU options consist of the 3AA, 3AH, 3AI, 3AJ, 3ARs, and 3AT, which are described in Table 2-1. The local memory and channel options are 3AL, 3AM, 3AN, 3AO, 3AP, 3AQ, and 3AS, and six 64K x 4-bit memory arrays which are described in Table 2-2. The 3AK and 3AW options provide I/O control for the channels and workstation and are described in Table 2-3. Refer to Figure 2-1 for functional block diagram of CPU. Refer to Figure 2-12 for IOP quarter board option layout.

Table 2-1. CPU Options and Descriptions

Option	Functional Description
3AA	Functional units, accumulator fanin/fanout
3AH	32-parcel exit stack
3AI	Instruction stack, next instruction parcel (NIP), k data, D/B/RP/DP register, base register (BSR)
3AJ	CPU local memory control, P register, branch control, and the instruction stack address
3AR (two)	128-operand register, MA/fetch registers, accumulator, branch accumulator, X register 3AR0 bits 2^7 - 2^0, 3AR1 bits 2^{15} - 2^8
3AT	Current instruction parcel (CIP), decode, and the carry bit

Table 2-2. Local Memory and Channel Options and Descriptions

Option	Functional Description
3AL	Local memory address and parcel counter registers
3AM	Write data in – port 0, port 1, workstation, and CPU I/O fanin
3AN	Read data out – port 0, port 1, workstation, and CPU real-time clock (RTC)
3AO	Data out port 1 – channels 14 - 17, 32 - 33 and 36 - 37 Workstation data out Error logger Direct memory access busy and done flags port 1
3AP	Data in port 1 – channels 14 - 17, 32 - 33 and 36 - 37
3AQ	Data out port 0 – channels 10 - 13, 20 - 21, 26 - 27, 30 - 31, and 34 - 35 Direct memory access (DMA) busy and done flags port 0
3AS	Data in port 0 – channels 10 - 13, 20 - 21, 26 - 27, 30 - 31, and 34 - 35

Table 2-3. I/O Control Options and Descriptions

Option	Functional Description
3AK	I/O control
3AW	Workstation control channel 22 - 25

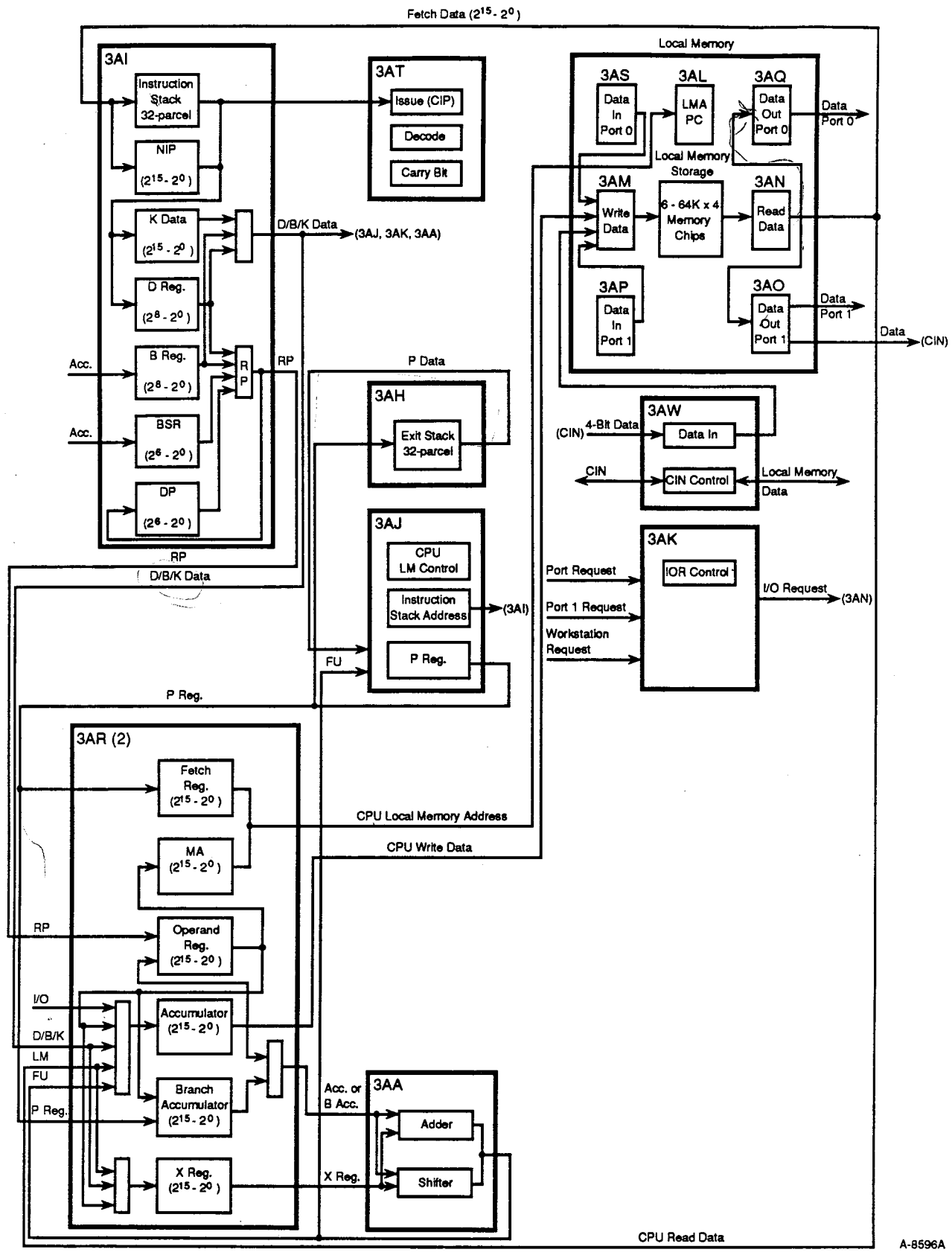


Figure 2-1. IOP Complete Block Diagram

CPU Control Signals

The CPU control is provided by the 3AT, 3AJ, 3AK, and 3AR options. An explanation of each control signal is provided. For a functional block diagram of the CPU control signals, refer to Figure 2-2.

3AT Control Signals

The 3AT decodes the instruction and then outputs the appropriate control signals. The following is an explanation of the 3AT options control signals. For a functional block diagram of the 3AT options control signals, refer to Figure 2-2.

- Advance P Branch (R0) is sent to the 3AJ to advance (+1) the P register after a branch is decoded. It is sent twice for a 2-parcel branch.

- Advance S, P (R1) increments the instruction stack read address and the P register on the 3AJ after an instruction issue. On the 3AI, it advances the next instruction into the next instruction parcel (NIP). It is not sent if a branch is issued.

- Exit or Interrupt or Call (R3 - 4) work together to read or write the exit stack and load the P register. After an exit instruction (001) has been decoded, the 3AH reads out the exit stack to the P register and then decrements the exit stack pointer (EP). The P register then sends the address to the fetch registers. After a return jump issues, the 3AH increments the EP and then writes the P register into the exit stack. After an interrupt is received, the 3AH increments the EP and writes the P register into the exit stack. The 3AH then reads out exit stack location 0 to the P and fetch registers. Refer to Table 2-4 for the proper levels of R3 and R4 during an exit, return jump, and interrupt.

Table 2-4. Exit, Interrupt, and Return Jump

R4	R3	Comment
0	1	Exit (001)
1	0	Return jump
1	1	Interrupts

- Enter B Register (R5) loads the accumulator into the B register.

- DP to RP (R6) loads the destination pointer (DP) into the reference pointer (RP). The DP to RP signal is sent for instructions that read and write operand registers. It is sent prior to the writing of the operand registers.

- Enter P from Adder (R7) loads the P register with the functional unit value (branch address) after a branch instruction.

- -d Branch or +d Branch (R8 or R9) if set, informs the 3AJ that a relative branch has issued and is sent with Go Branch (R17). If R8 is set, it is a backward jump and if R9 is set, it is a forward jump. The 3AJ determines if it is an in-stack branch by comparing the offset (D field). If it is an in-stack branch, the instruction stack read address is offset by the value of the D field. If it is an out of stack branch, the instruction stack read and write addresses are cleared. Whether it is an in-stack or out-of-stack branch, the P register is loaded with the functional unit value.

- Enter DP Register (R10) loads the reference pointer into the DP register on the 3AI. The Enter DP signal is sent for instructions that read and write the operand registers. It is sent prior to the reading of the operand registers.

- Go Read Busy/Done (R11) is sent to the 3AK after a *040 - 043* instruction has issued. It informs the 3AK to read the busy or done flag of the requested channel (I4 - 8) to the carry bit (3AT).

- Go Function I/O (R12) signals the 3AA and 3AK that a *140 - 177* instruction has issued.

- Function Code 2^0 - 2^3 (R13 - 16) are bits 2^{12} - 2^9 of the instruction if sent with Go Function I/O (R12). If sent with Go Read Busy/Done (R11), bit 2^0 differentiates between the busy and the done flag. The Function Code is also used to inform the 3AA of a functional unit operation.

- Go Branch (R17) is sent to the 3AJ when a branch is decoded. If R8 or R9 is set, it is a relative branch. If neither R8 or R9 is set, it is an absolute branch.

- Clear Accumulator (R18) clears the accumulator prior to the loading of the accumulator.

- Gate Local Memory to A/X (R20) is sent to the 3ARs to load the local memory data into the accumulator or the X register. If R24 is set, the data is loaded into the X register.

- Enter Constant (R21) sets bit 2^0 of the X register on 3AR0 after an increment or decrement instruction has been decoded.

- Gate d/b/k to a/x (R23) loads the D, B, or K register into the accumulator or X register. If R24 is set, the data is loaded into the X register.

- Steer to X (R24) is sent with R19, R20, and R23 if the X register is to be loaded instead of the accumulator.

- Gate Register to Branch (R25) loads the operand register value into the branch accumulator on the 3AR options. The Gate Register to Branch signal is sent for branch instructions that use an operand register value for the displacement value.

- Enter P to Branch A (R26) loads the P register (I60 - 67) into the branch accumulator on the 3AR after the 3AT decodes a branch instruction.

- Enter AA Data (R27) loads the functional unit value into the accumulator.

- Enter Memory Address (MA) (R28) is sent to the 3AJ requesting a local memory reference. It latches the operand register value into the memory address register on the 3ARs.

- Local Memory Write Reference (R29) is sent to the 3AJ when the 3AT decodes a CPU write (034). It is sent with Enter MA (R28).

- Write Register (R30) enables a write to the operand registers on the 3ARs.

3AJ Control Signals

The 3AJ controls the CPU local memory references, the instruction stack read and write addresses, and the P register. The following is an explanation of the 3AJ options control signals. For a functional block diagram of the 3AJ options control signals, refer to Figure 2-2.

- Instruction Stack Write (R25) is sent to the 3AI after the 3AJ has completed the fetch sequence. It writes the fetched parcel into the instruction stack.

- Instruction Stack Write (R25) is sent to the 3AI after the 3AJ has completed the fetch sequence. It writes the fetched parcel into the instruction stack.

- Enter NIP (R26) is sent after Input to NIP Valid sets and NIP is not valid. It allows the 3AI to load the NIP without an Advance S. The 3AT receives Enter NIP and sets NIP Valid on the 3AT.

- Input to NIP Valid (R27) means the instruction stack address is a valid read address or the bypass is valid. If the instruction stack is being written to and the load pointer is equal to the stack pointer, the input to NIP valid is cleared. The 3AI loads the NIP when it receives an Advance S or Enter NIP, and the input to NIP valid is set. The 3AT uses Input to NIP Valid and Advance S to keep NIP Valid on the 3AT.

- Bypass Stack (R28) is sent to the 3AI when the load pointer is equal to the stack pointer and NIP is not valid. The instruction is loaded directly into the NIP and written into the instruction stack.

- MA/Fetch Request (R29) is sent to the 3AN if there is a CPU read, write, or fetch request for local memory.

- Write Request (R30) is sent with MA/Fetch Request (R29) if the reference is a CPU write (034).

- Gate MA (R31) gates the accumulator data to the 3AM, selects the MA register on the 3ARs, and informs the 3AT that the operand registers and accumulator are free on CPU write and that the operand registers are free on CPU read.

- Enter Fetch Pointer (R32) loads the P register address into the fetch register on the 3ARs after an out-of-stack branch has issued or an interrupt has been received. The exit stack value or functional unit value is loaded into P register. The P register then loads the fetch register.

- Enter Instruction Stack Address (R33) latches the instruction stack address onto the 3AI.

- NIP Valid (R34) is sent to the 3AT when the NIP has valid data. If NIP Valid is set and an Advance S is received, the 3AT sets or holds CIP valid on the 3AT.

3AK Control Signals

The 3AK provides I/O control. The following is an explanation of the 3AK options control signals. For a functional block diagram of the 3AK options control signals, refer to Figure 2-2.

- Go Function (R15) is sent from the 3AK to the I/O channel options after a channel function is decoded.
- Channel Designator (R10 - 14) are bits 2^4 - 2^0 of the B or D registers and are only used on the IOP board. The channel designators are sent with Go Function (R15) or Go Busy/Done(R17/18).
- Go Busy/Done (R17/18) fans in the busy or done flag of the requested channel.
- Enter LMA/PC(R31/32) enters the local memory address (LMA) and parcel on the 3AL.

3AR Control Signals

The following is an explanation of the 3ARs options control signals. For a functional block diagram of the 3AR options control signals, refer to Figure 2-2.

- A = 0 (R25) is sent from 3ARs to the 3AT and is used for conditional jumps.
- Fetch Pointer Carry (R27) is sent from 3AR0 to 3AR1 when the fetch address bits 2^7 - 2^0 has a carry for bits 2^{15} - 2^8. The 3AR0 has bits 2^7 - 2^0 and 3AR1 has bits 2^{15} - 2^8.

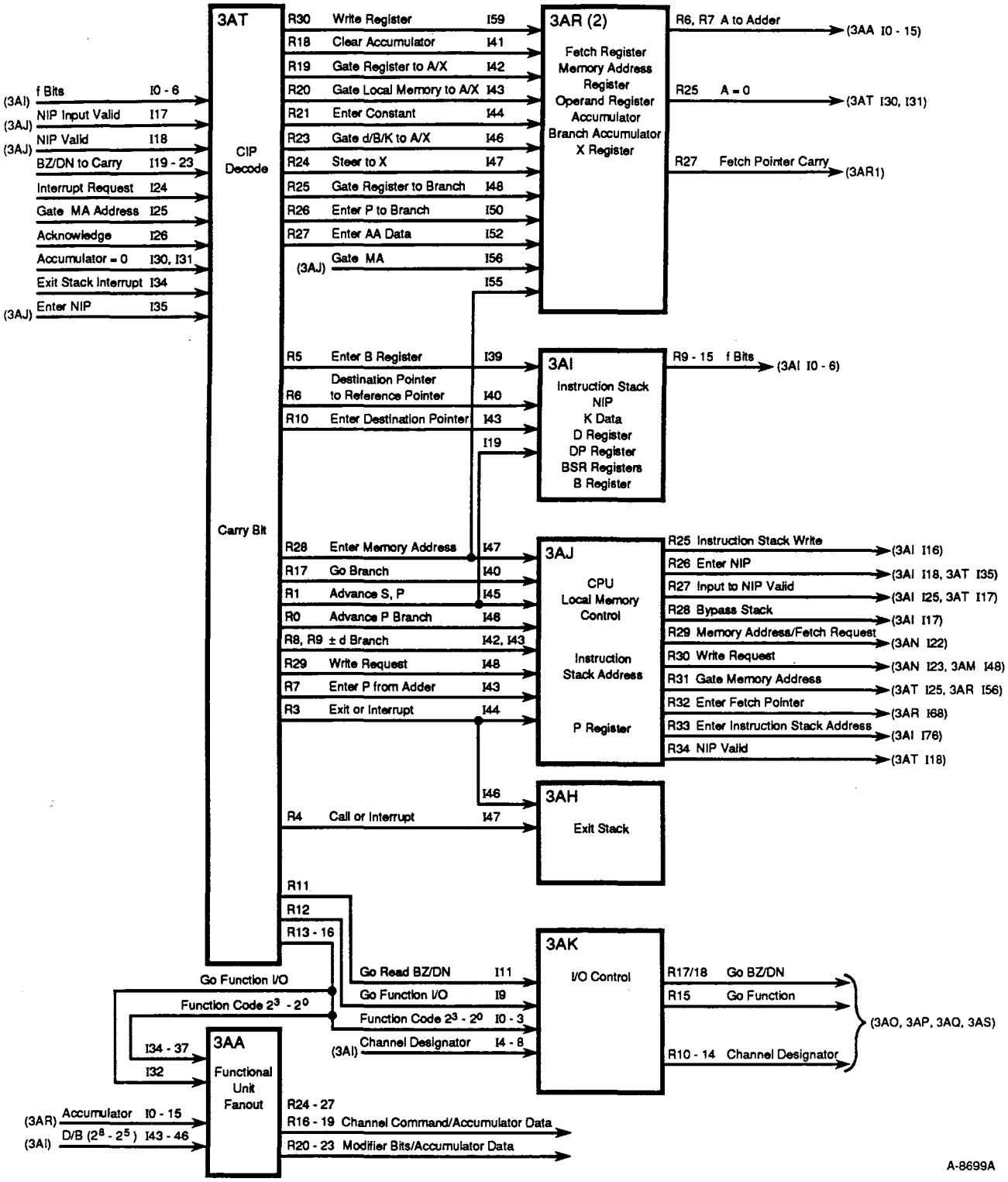


Figure 2-2. Issue and Control

CPU Local Memory References

There are three types of CPU local memory references: write, read, and fetch. The following is a sequential explanation of each reference. For a functional block diagram of the CPU references, refer to Figure 2-3.

CPU Local Memory Write Reference Sequence

The following is a sequential explanation of a CPU write reference. For a functional block diagram of the CPU write reference, refer to Figure 2-3.

1. Enter MA and Write Reference Request. When the 3AT decodes a central processing unit (CPU) Write (034), it sends an Enter MA to the 3AJ and 3ARs and a Write Reference Request to the 3AJ.

   3AJ - The Enter MA (I47) informs the 3AJ that the CPU is requesting a local memory reference and if Write Reference Request (I48) is set, it is a write request.

   3AI - The 3AI pre-decodes the NIP (2^{15} - 2^{9}) to see if the B or D register is loaded into RP (R20 -26).

   3AR - The 3ARs read out the operand register after receiving the RP (I24 - 30) and then latch the operand register value into the MA register when it receives Enter MA (I55).

2. MA/Fetch and Write Requests. The 3AJ sends MA/Fetch Request to the 3AN and MA Write Request to the 3AN and 3AM.

   3AJ - After receiving the Enter MA (I47) and Write Reference Request (I48), the 3AJ checks for a fetch request. If there is no fetch request, the 3AJ sends MA/Fetch Request (R29) to the 3AN, and a MA Write Reference (R30) to the 3AN and 3AM, and Gate MA (R31) to 3AR and 3AT.

   3AN - The 3AN checks for conflicts and priorities before sending a MA/Fetch Acknowledge (R16).

3. Gate MA. The Gate MA reads out the accumulator data, selects MA registers on the 3ARs, and frees the accumulator and the operand register on the 3AT.

   3AR - The 3ARs send the accumulator data (R16 - 19) to the 3AM and selects the MA register instead of the fetch register after receiving Gate MA.

3AM - The 3AM receives the MA Write Request (I48) and saves the parcel of data (I40 - 43) from the 3ARs. The 3AM generates single-error correction, double-error detection (SECDED) on for each parcel of data.

3AT - The 3AT frees the accumulator and operand registers after receiving Gate MA (I25) from the 3AJ.

4. MA/Fetch Acknowledge. When local memory is free, the 3AN sends a MA/Fetch Acknowledge to the 3AJ, 3AR, 3AT, and 3AL.

3AJ - After receiving the MA/Fetch Acknowledge (I49), the 3AJ clears the request.

3AR - The 3ARs read out the local memory address to the 3AL the next 2 clock periods (CPs).

3AT - The 3AT clears the CPU write reference (034) after receiving MA/Fetch Acknowledge.

3AL - The 3AL receives a copy of the MA/Fetch Acknowledge (I26) from the 3AN and latches the CPU address (I8 - 15). Address bits 2^3 - 2^0 and 2^{11} - 2^8 are latched on the first clock period, and bits 2^7 - 2^4 and 2^{15} - 2^{12} on the next clock period. On the following clock period, 3AL passes the CPU address to local memory storage arrays.

3AM - The 3AM sends the data and check bits (R0 - 21) with a Write Enable (R33 -34) to the local memory storage arrays after the MA Write Request (I48) is cleared.

CPU Local Memory Read Reference Sequence

The following is a sequential explanation of a CPU read reference. For a functional block diagram of the CPU read reference, refer to Figure 2-3.

1. Enter MA. When the CPU decodes a CPU read (030), it sends an Enter MA to the 3AJ and 3ARs.

3AJ - The Enter MA (I47) informs the 3AJ that the CPU is requesting a local memory reference. Since the Write Reference Request (I48) is cleared, the reference is a read.

3AI - The 3AI pre-decodes the NIP (2^{15} - 2^9) to see if the B or D register is loaded into the RP (R20 -26).

3AR - The 3ARs read out the operand register after receiving the RP (I24 - 30) and then latches the operand register value into the MA register when it receives Enter MA (I55).

2. MA/Fetch Request. The 3AJ sends a MA/fetch request to the 3AN when the CPU is requesting a local memory read.

   3AJ - After receiving Enter MA, the 3AJ checks for a fetch request; if there is no request, the 3AJ sends a MA/Fetch Request (R29) to the 3AN and Gate MA (R31) to the 3ARs and 3AT.

   3AN - The 3AN checks for conflicts and priorities and then sends a MA/Fetch Acknowledge (R16).

3. Gate MA. The gate MA selects the MA register on the 3ARs and frees the operand register on the 3AT.

   3AR - When the 3AJ sends a request to the 3AN, it also sends Gate MA to the 3ARs, so the 3ARs select the MA register instead of the fetch register.

   3AT - The 3AT frees the operand registers after receiving Gate MA (I25) from the 3AJ.

4. MA/Fetch Acknowledge. When local memory is free, the 3AN sends a MA/Fetch Acknowledge to the 3AJ, 3AR, 3AL, and 3AT.

   3AN - The 3AN sends the MA/Fetch Acknowledge (R16) and waits for the data to arrive from local memory (I0 - 21). The 3AN checks the data for errors and then outputs the data to the accumulator on the 3ARs.

   3AJ - After receiving the MA/Fetch Acknowledge (I49), the 3AJ clears the request.

   3AR - The 3ARs read out the local memory address to the 3AL and wait for the local memory data from the 3AN.

   3AL - The 3AL receives a copy of the MA/Fetch Acknowledge (I26) from the 3AN and latches the CPU address (I8 - 5). Address bits 2^3 - 2^0 and 2^{11} - 2^8 are latched on the first clock period, and bits 2^7 - 2^4 and 2^{15} - 2^{12} on the next clock period. On the following clock period, 3AL passes the CPU address to local memory storage arrays.

   3AT - The 3AT clears the CPU read reference (030), and sends Gate Local Memory to A/X (R20) to the 3ARs.

CPU Local Memory Fetch Reference Sequence

The following is a sequential explanation of a CPU fetch reference. For a functional block diagram of the CPU fetch reference, refer to Figure 2-3.

1. MA/Fetch Request. The 3AJ sends a MA/Fetch Request to the 3AN when the load pointer minus the stack pointer is less than 12.

   3AN - The 3AN checks for conflicts and priorities and then sends a MA/Fetch Acknowledge (R16).

2. MA/Fetch Acknowledge. When local memory is free, the 3AN sends MA/Fetch Acknowledge to the 3AJ, 3AR, and 3AL.

   3AN - The 3AN sends the MA/Fetch Acknowledge (R16) and waits for the data to arrive from local memory (I0 - 21). The 3AN checks the data for errors and then outputs the data to the instruction stack on the 3AI option.

   3AJ - After receiving the MA/Fetch Acknowledge (I49), the 3AJ clears the request if the load pointer minus the stack pointer is greater than or equal to 12.

   3AR - The 3ARs read out the fetch address to the 3AL the next 2 CPs.

   3AL - The 3AL receives a copy of the MA/Fetch Acknowledge (I26) from the 3AN and latches the fetch address (I8 -15). Address bits 2^3 - 2^0 and 2^{11} - 2^8 are latched on the first clock period, and bits 2^7 - 2^4 and 2^{15} - 2^{12} on the next clock period. On the following clock period, 3AL passes the CPU address to local memory storage arrays.

3. Stack Write. The 3AJ sends a Stack Write to enable a write to the instruction stack.

   3AJ - The 3AJ receives the MA/Fetch Acknowledge and sends an Enter Stack Address (R33), a Stack Address (R20 - 24), and a Stack Write (R25) to the 3AI.

   3AI - The 3AI addresses the stack and writes the parcel of data into the instruction stack. If bypass (I17) is set, NIP is not valid; the parcel of data is also loaded into the NIP register.

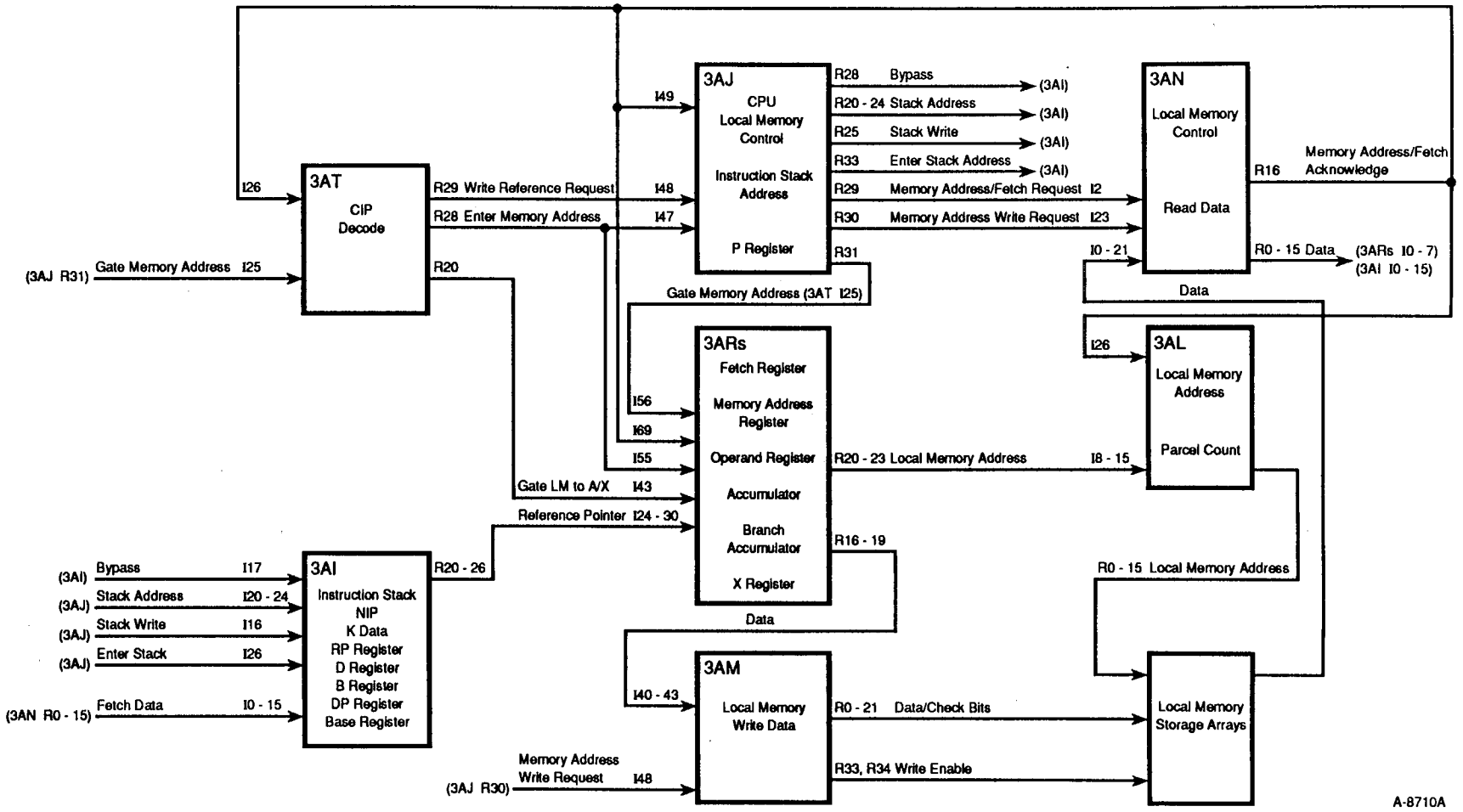


Figure 2-3. CPU Local Memory Write, Read, and Fetch Reference

Direct Memory Access Local Memory References

There are two types of DMA local memory references: DMA write and DMA read. The following is a sequential explanation of a DMA write and a DMA read. For a functional block diagram, refer to Figure 2-4.

Local Memory Write Reference

The following is a sequential explanation of a DMA write. For a functional block diagram of the DMA local memory write reference, refer to Figure 2-4.

The Command 1 sets the busy flag, clears the done flag, and activates the input channel.

1. 3AS or 3AP - The 3AS or 3AP receives the Input Control (ready at sync +0 or 3) and the data from the channel. The Input Control is passed to the 3AQ or 3AO as Channel Request (R20 - 23) with a Write Request (R28). The data is held until a reference is received. Refer to Table 2-4 for input control timing.

Table 2-5. Input and Output Control Timing

Sync	Name	Comment
sync +0 or 3	Ready	Data arriving
sync +1 or 4	Acknowledge	Data received
sync +2 or 5	Disconnect	Transfer done

2. 3AQ or 3AO - If the port is free, a Port Reference Request (R0 - 3) is passed to the 3AS or 3AP and the 3AK. The Write Request (R4) is sent to the 3AS or 3AP, 3AM, and 3AK.

3. 3AS or 3AP - The 3AS or 3AP sends the parcel of data (R0 - 7) to the 3AM after receiving the Port Reference Request (3lAS I90 - 93) or (3AP I72 - 73) and the Input Request (I14) from the 3AQ or 3AO.

4. 3AM - The 3AM receives the data from the 3AS or 3AP and a Port Write Request (I58 or I68) from the 3AQ or 3AO. The 3AM generates SECDED for each parcel of data.

5. 3AK - The 3AK checks the other port and the workstation for a request. If there is no request, the 3AK sends an I/O Request (R25) to the 3AN and Port 1 Request (R29) to the 3AM.

6. 3AN - If there is no MA/Fetch Request, an I/O Acknowledge (R17) is sent to the 3AK, 3AL, and 3AM. The I/O and MA/Fetch Request alternate priority.

7. 3AK - The 3AK clears the request after receiving the I/O Acknowledge (I60), sends a Port 0 or 1 Acknowledge (R27 or R28) to the 3AS and 3AQ or 3AQ and 3AO, and I/O Reference Channel (R20 - 24) to the 3AL.

8. 3AL - The 3AL sends the LMA (R0 - 15) to the memory arrays and then increments the LMA and decrements the parcel count. The 3AL checks the LMA and parcel count for parity errors each time they are read out. If there is an error (R25), it is reported to the 3AN and 3AO.

9. 3AM - The 3AM outputs the parcel data and check bits (R0 - 21) to the memory storage arrays and then sends a Write Enable (R33 - 34) after receiving I/O Reference Acknowledge (I83). If I84 is set, the 3AM selects port 1 data.

10. 3AS or 3AP - After a Port Acknowledge (I15) is received, the 3AS or 3AP clear the request.

11. 3AQ or 3AO - After a Port Acknowledge (I16) is received from the 3AK, the 3AQ or 3AO sends an Output Control at sync + 1 or 4. Refer to Table 2-4 for output control timing.

12. 3AQ or 3AO - The DMA done flag sets and the busy flag clears when the parcel count equals zero and ready or disconnect is received. If a ready is received, the parcel of data is saved and held on the 3AS or 3AP until the channel is activated again. Refer to Table 2-4 for ready and disconnect timing.

Local Memory Read Reference

The following is a sequential explanation of a DMA read. For a functional block diagram of the DMA local memory read reference, refer to Figure 2-4.

The Command 1 sets the busy flag, clears the done flag, and activates the channel's read request.

1. 3AQ or 3AO - If the port is free, a Port Reference Request (R0 - 3) is sent to the 3AK, and 3AS or 3AP. The next request is set after an input control (Acknowledge I40 - 43) is received.

2. 3AK - The 3AK checks the other port and workstation for a request. If there is no request, the 3AK sends an I/O Request (R25) to 3AN.

3. 3AN - If there is no MA/Fetch Request, an I/O Acknowledge (R17) is sent to the 3AK and 3AL. The MA/Fetch and I/O Request alternate priority.

4. 3AK - The 3AK clears the request and sends a Port 0 or 1 Acknowledge (R27 or R28) to the 3AS and 3AQ or 3AP and 3AO and I/O Reference Channel (R20 - 24) to the 3AL.

5. 3AL - The 3AL sends the LMA (R0 -15) to the memory arrays, and then increments the LMA and decrements the parcel count. The 3AL checks the LMA and parcel count for parity errors each time they are read out. If there is an error (R25), it is reported to the 3AO and 3AN.

6. 3AN - The 3AN receives the parcel of data from local memory storage arrays, checks for errors, and then sends it to the 3AQ or 3AO.

7. 3AQ or 3AO - After an I/O Acknowledge is received, the 3AQ or 3AO receives the parcel of data from 3AN and sends it to the channel with an output control at sync +0 or 3. Refer to Table 2-4 for output control timing.

8. 3AS or 3AP -.The 3AS or 3AP receives Input Control from the channel at sync +1 or 4. The Input Control is sent to the 3AQ or 3AO (R24 - 27) enabling the next parcel of data. Refer to Table 2-4 for input control timing.

9. 3AQ or 3AO - The DMA done flag sets and the busy flag clears when the parcel count equals zero or an input control is received at sync +2 or 5 (disconnect). The 3AQ or 3AO sends a disconnect at sync +2 or 5 if the parcel count equals zero.

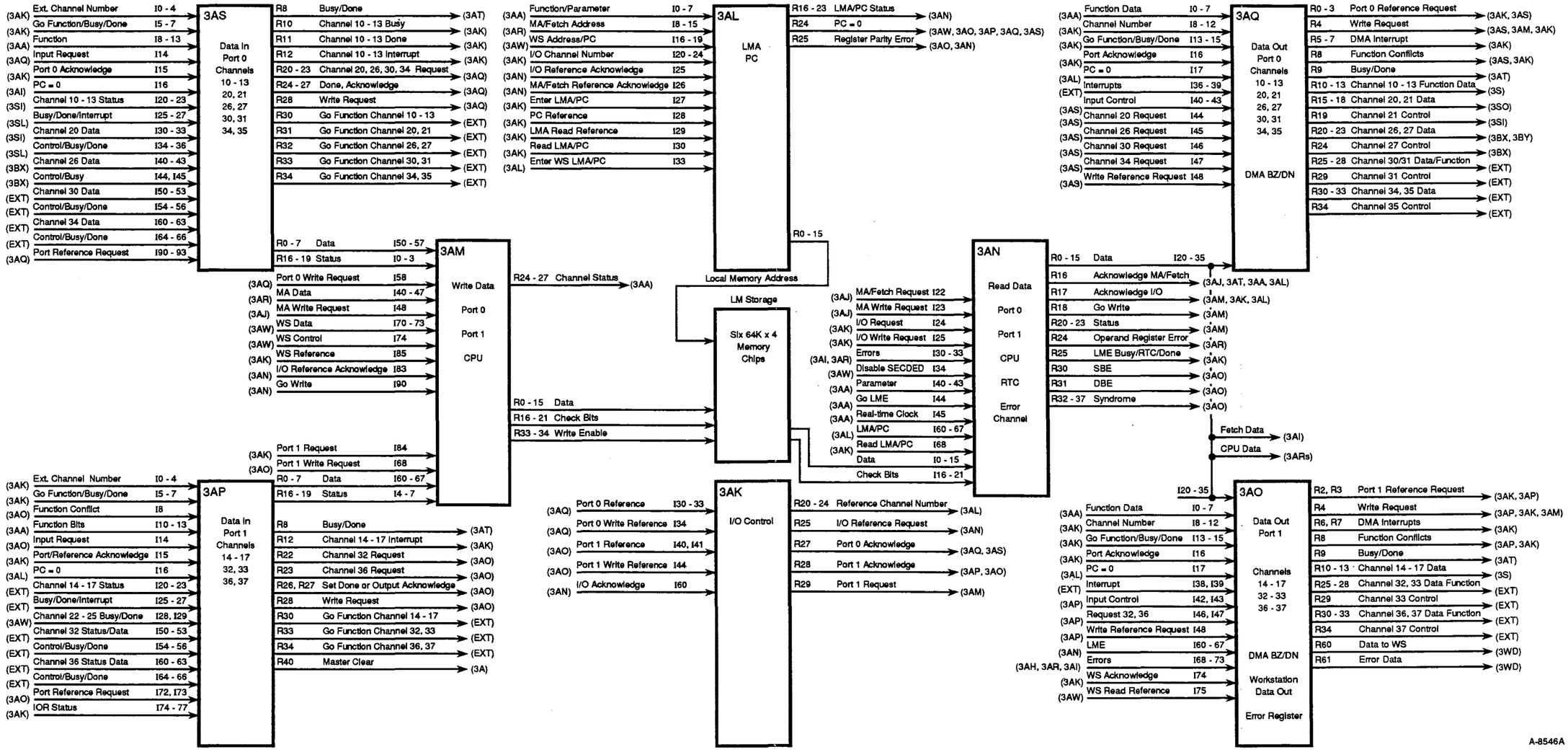


Figure 2-4. Local Memory Block Diagram and Control

Direct Memory Access I/O Function Sequence

The following is a sequential explanation of a DMA I/O function fanout. For a functional block diagram of the DMA I/O function sequence, refer to Figure 2-5.

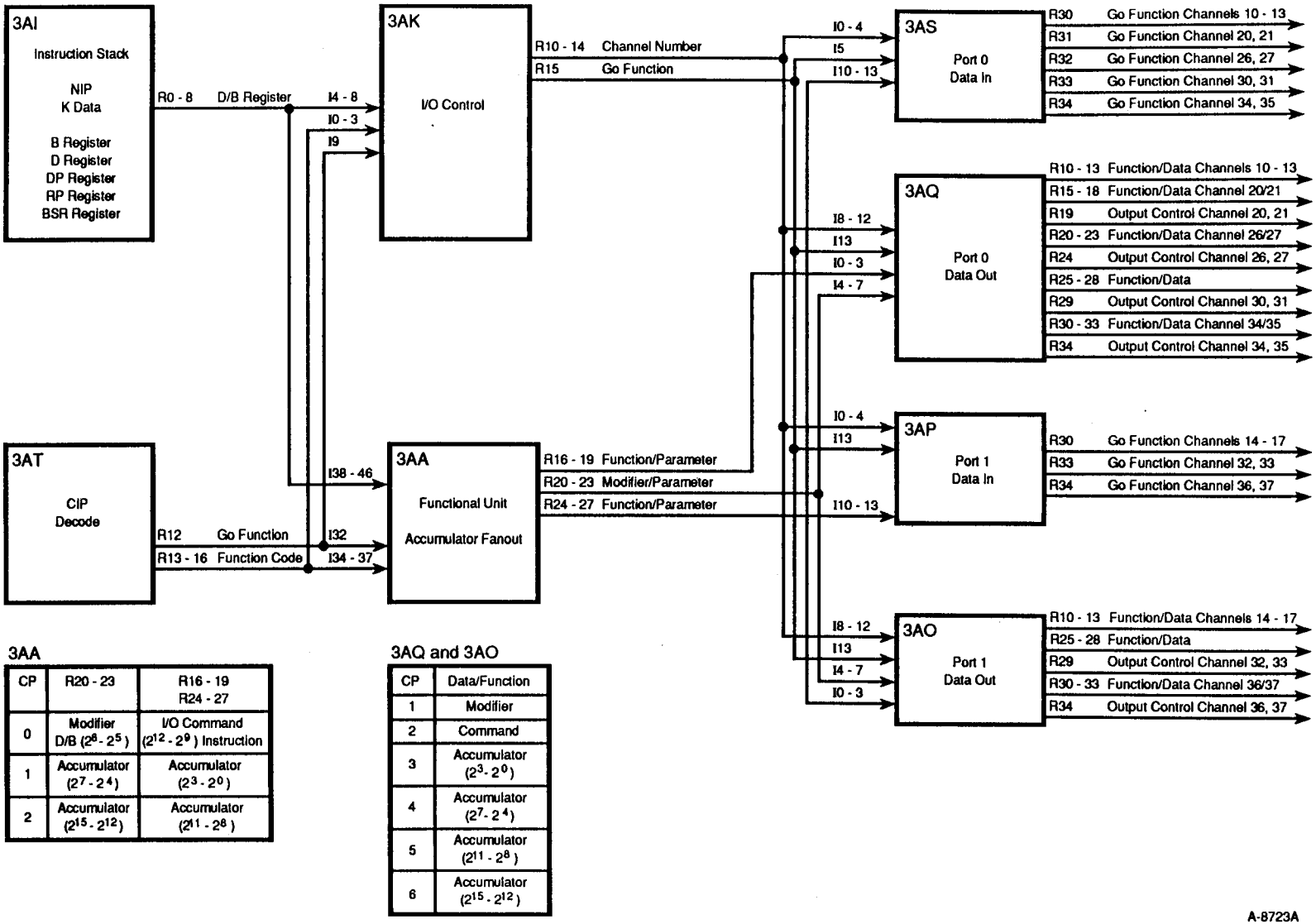
The 3AT sends Go Function to the 3AK and 3AA after a channel function is decoded.

1. 3AK - The 3AK receives the Go Function (I9) and the Function Code (I0 - 3) (2^{12} - 2^{9} of the instruction) from the 3AT. It receives the channel number (I4 - 8) (2^{4} - 2^{0} D or B register) from the 3AI. The 3AK decodes the channel and function, and then sends Go Function (R15) and the channel number (R10 - 14) to the 3AS, 3AQ, 3AP, and 3AO. Functions 10, 11, 14, and 15 on channels 10 - 37 are exceptions to this. These functions read and write the LMA and parcel count, so the 3AK sends R31 - 34 to the 3AL.

2. 3AA - The 3AA also receives the Go Function (I32) and Function Code (I34 - 37) (2^{12}- 2^{9} of the instruction) from the 3AT and the modifier bits (2^{8} - 2^{5} of the D/B registers) from the 3AI and the accumulator data from the 3ARs. The 3AA fans out the modifier bits, function code, and accumulator data to the 3AS, 3AQ, 3AP, and 3AO.

3. 3AS or 3AP - After the 3AS and 3AP receive Go Function (I5) from the 3AK, the 3AS and 3AP decode the channel designator (I0 - 4) and send a Go Function (R30 - 34) to the proper channel.

4. 3AQ or 3AO - The 3AQ or 3AO sends Function/Data to the channel after receiving Go Function (I13) and the channel number from the 3AK. The Function/Data is sent to the quarter boards and the buffer board 4 bits at a time. The modifier bits are sent first and then the command. The accumulator data is sent the next 4 CPs.



3AA

CP	R20 - 23	R16 - 19 R24 - 27
0	Modifier D/B (2^8 - 2^5)	I/O Command (2^{12} - 2^9) Instruction
1	Accumulator (2^7 - 2^4)	Accumulator (2^3 - 2^0)
2	Accumulator (2^{15} - 2^{12})	Accumulator (2^{11} - 2^8)

3AQ and 3AO

CP	Data/Function
1	Modifier
2	Command
3	Accumulator (2^3 - 2^0)
4	Accumulator (2^7 - 2^4)
5	Accumulator (2^{11} - 2^8)
6	Accumulator (2^{15} - 2^{12})

Figure 2-5. Go Function Channel and Parameter Fanout

Accumulator Fanin/Fanout and Busy/Done Fanin

The accumulator is located on the 3AR options. The 3AA option receives the accumulator fanin data from the 3AM option. The 3AM option receives the fanin data from the 3AH, 3AN, 3AP, 3AS, and 3AW options. The 3AP and the 3AS options receive the accumulator data from the buffer board, CCA1, DCA1, DCA2, HCM, HCA3/4, and TCA1 quarter boards. Refer to Figure 2-6 for accumulator fanin. The quarter board can fan in various information: status, parcel count, and errors. Refer to Figures 2-7 and 2-8 for quarter board fanin.

The 3AA option receives the accumulator data from the 3AR options and the modifier bits from the 3AI option. The 3AA option fans out this data to the 3AH, 3AI, 3AL, 3AN, 3AO, 3AP, 3AQ, 3AS, and 3AW options. The 3AO and 3AQ options fan out the command, modifier bits, and accumulator data to the buffer board, CCA1, DCA1, DCA2, HCM, HCA3/4, and TCA1 quarter boards. Refer to Figure 2-9 for accumulator fanout. One option on each quarter board receives this information and then fans it out to the entire quarter board. Refer to Figure 2-11 for accumulator on the quarter boards.

The busy and done flags are fanned in to the carry bit on the 3AT option via the 3AK, 3AO, 3AQ, 3AR, and 3AS options. The 3AP and 3AS options receive the busy and done flags for channels 10 - 17, 20 - 21, and 30 - 37. Refer to Figure 2-11 for busy and done flag fanin.

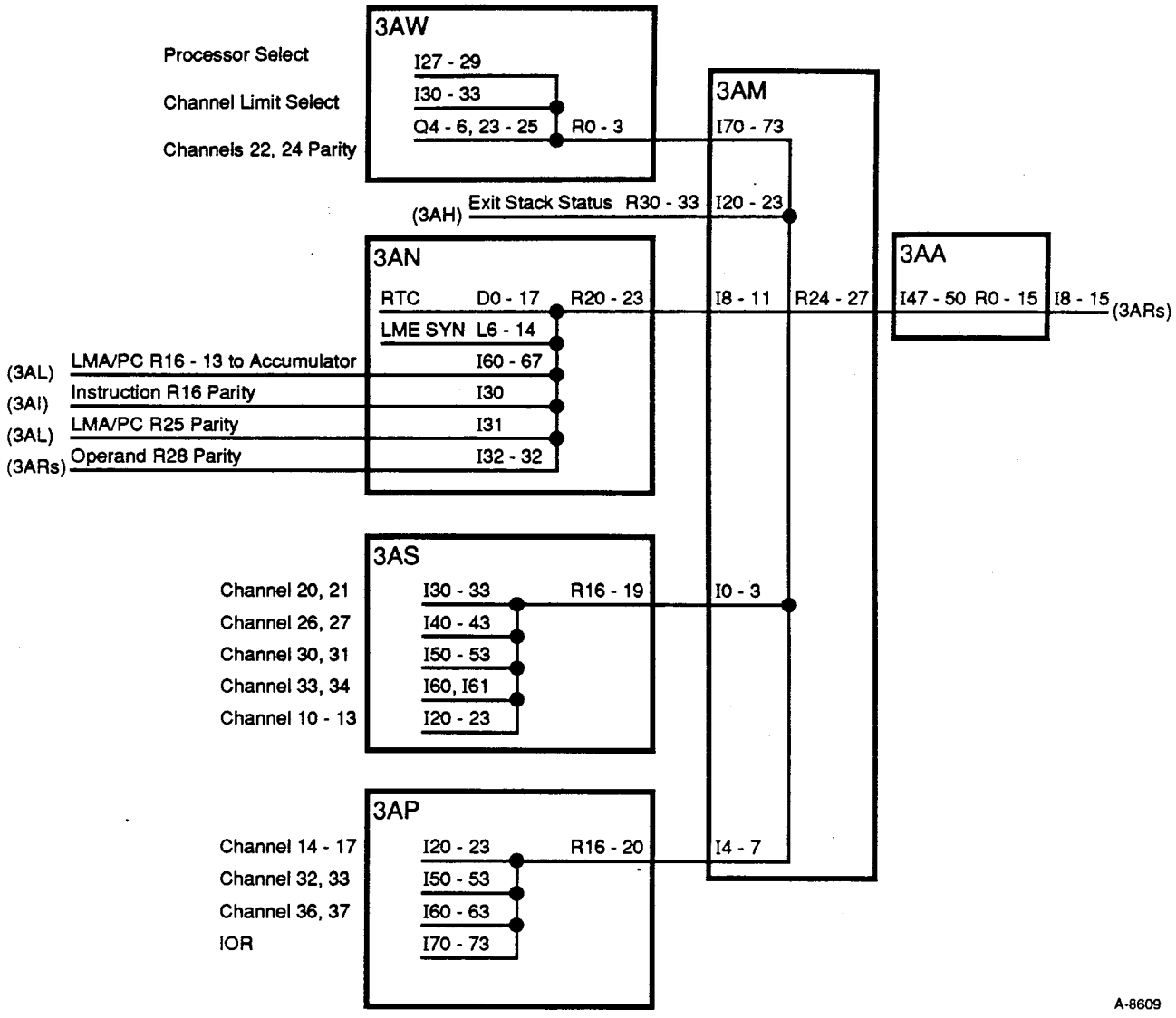


Figure 2-6. Accumulator Fanin

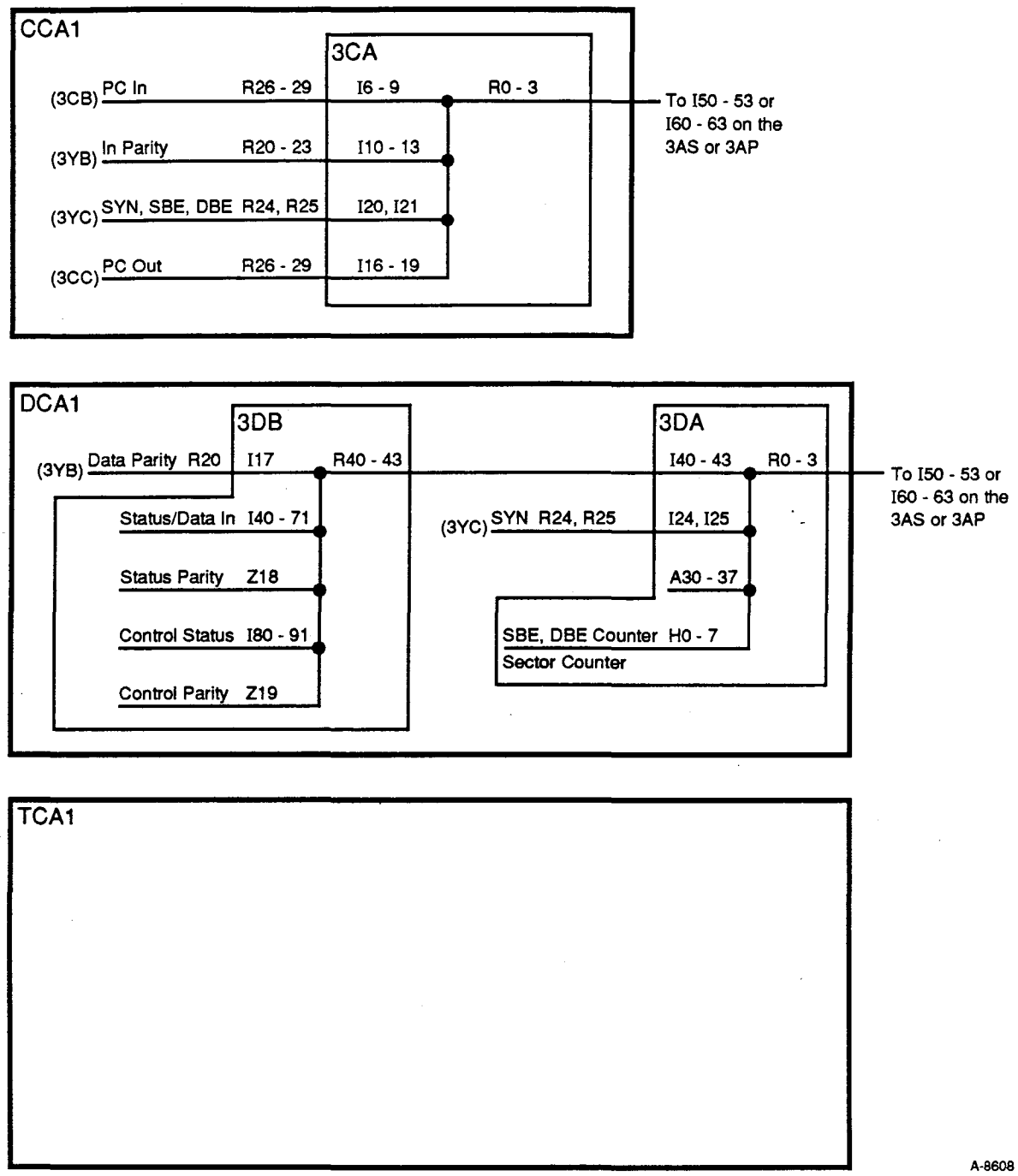


Figure 2-7. CCA1, DCA1, and TCA1 Fanin

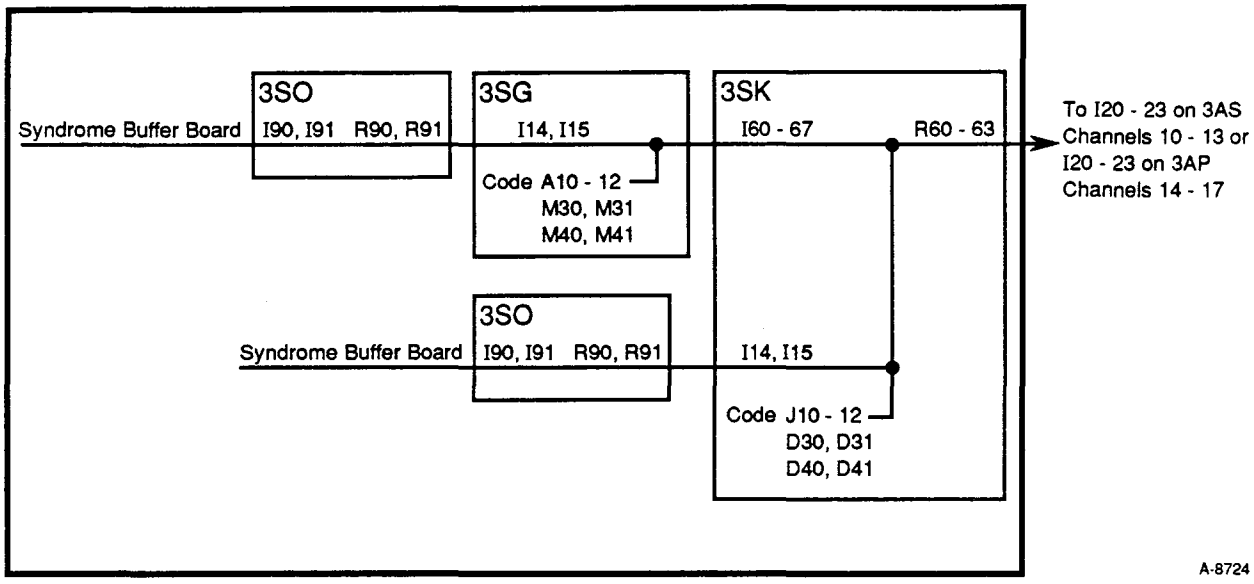


Figure 2-8. HISP/LOSP Fanin

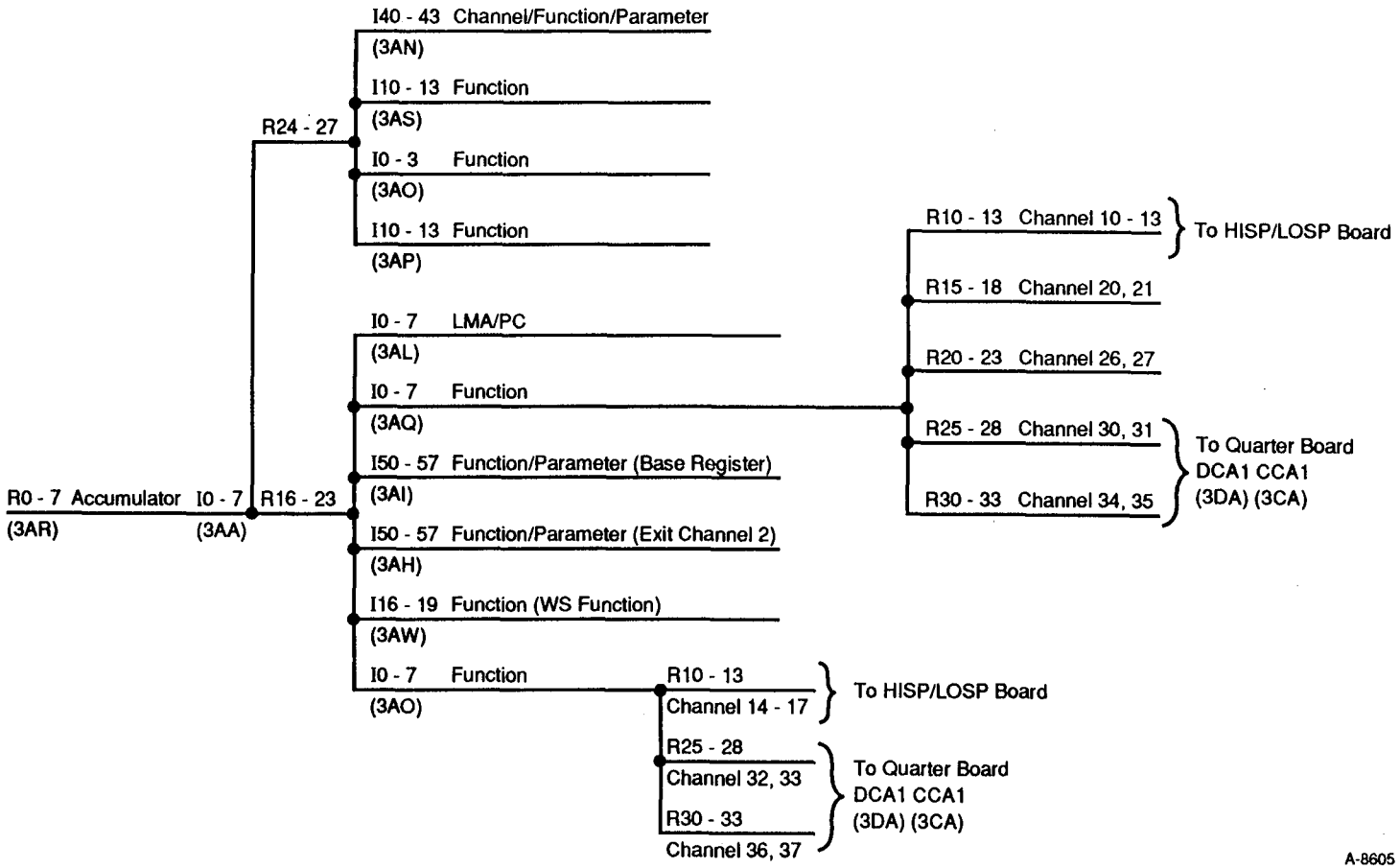


Figure 2-9. Accumulator Fanout

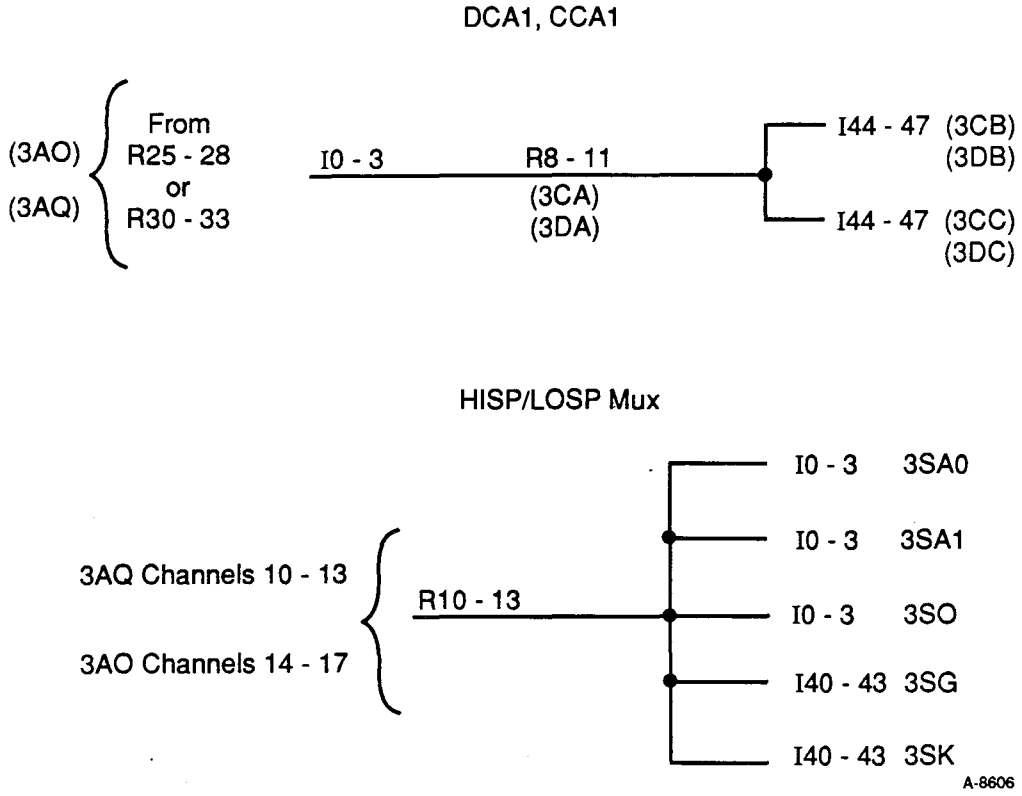


Figure 2-10. Quarter Board Fanout

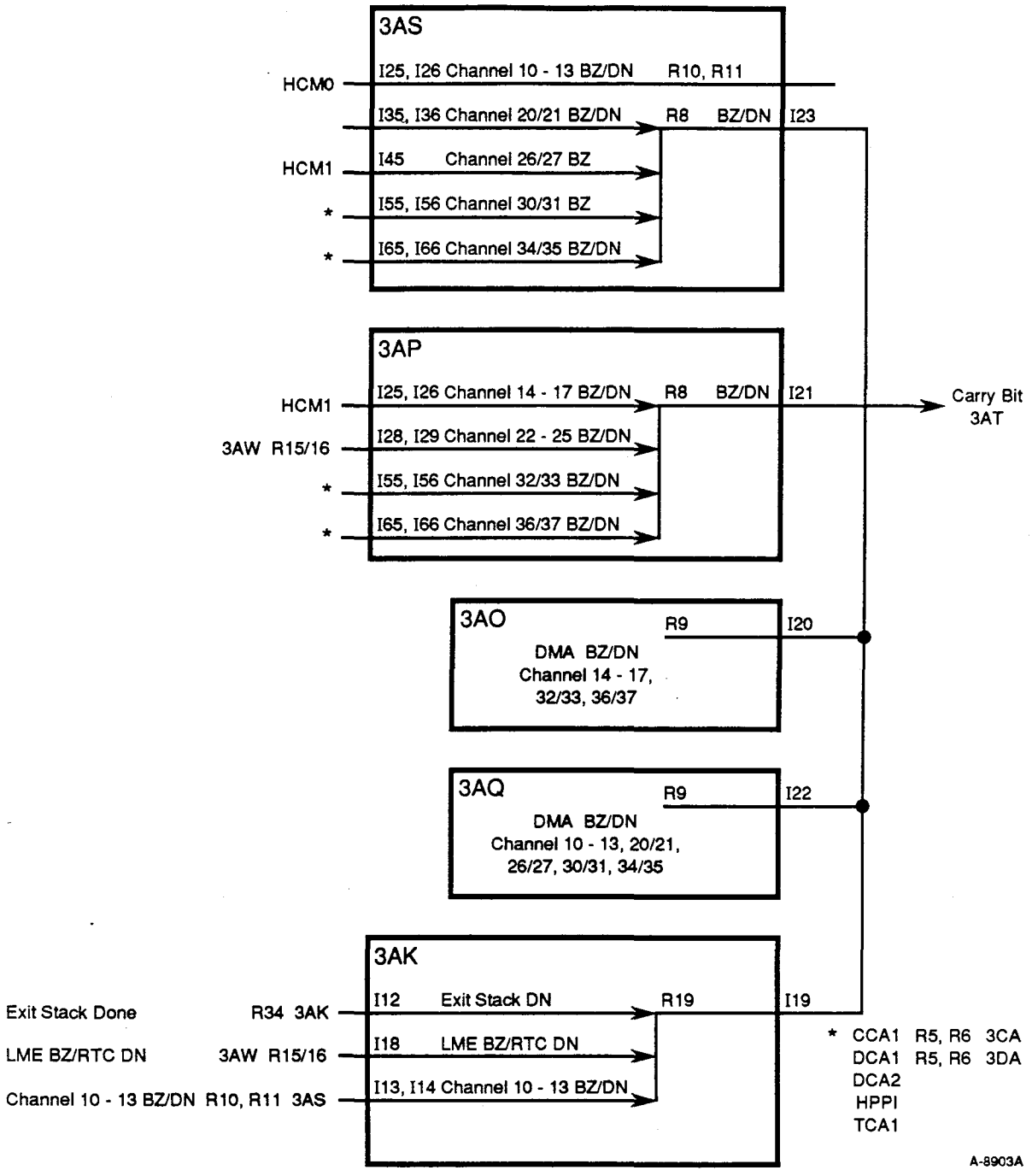


Figure 2-11. Busy/Done Fanin

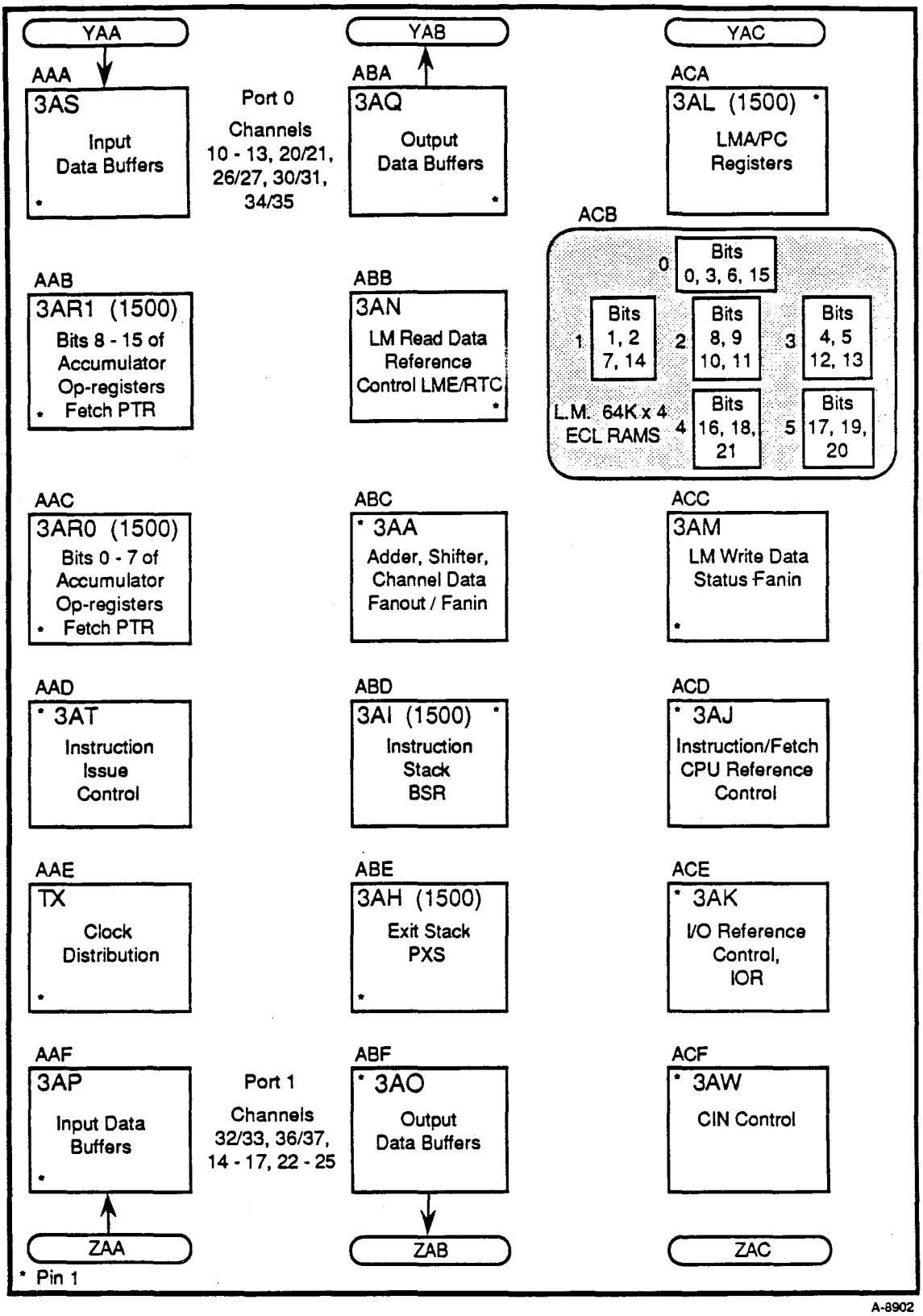


Figure 2-12. IOP Quarter Board IC Layout

3 CLUSTER INTERFACE AND WORKSTATION INTERFACE

The cluster interface (CIN) and workstation interface (WIN) control the communication between the I/O processors (IOP) and the workstations. There are two WINs, one for the operator workstation (OWS) and one for the maintenance workstation (MWS). There are eight CINs, one for each I/O cluster. Each CIN is connected to five IOPs. Both WINs are connected to the eight CINs. Data between the workstation and the WIN is parallel (16 bits per clock period), while data between the WIN and CIN is serial. Data from the IOP to the CIN is serial data, but the data from the CIN to the IOP are 4-bit transfers. The interface between the WIN and workstation is standard 6-Mbyte low-speed (LOSP) protocol. The OWS connects to channels 22/23 and the MWS connects to channels 24/25. There are five WIN commands that can be sent from the workstations to the WIN to control the IOS. Refer to Figure 3-1 for a block diagram of CIN, WIN, and workstation configurations.

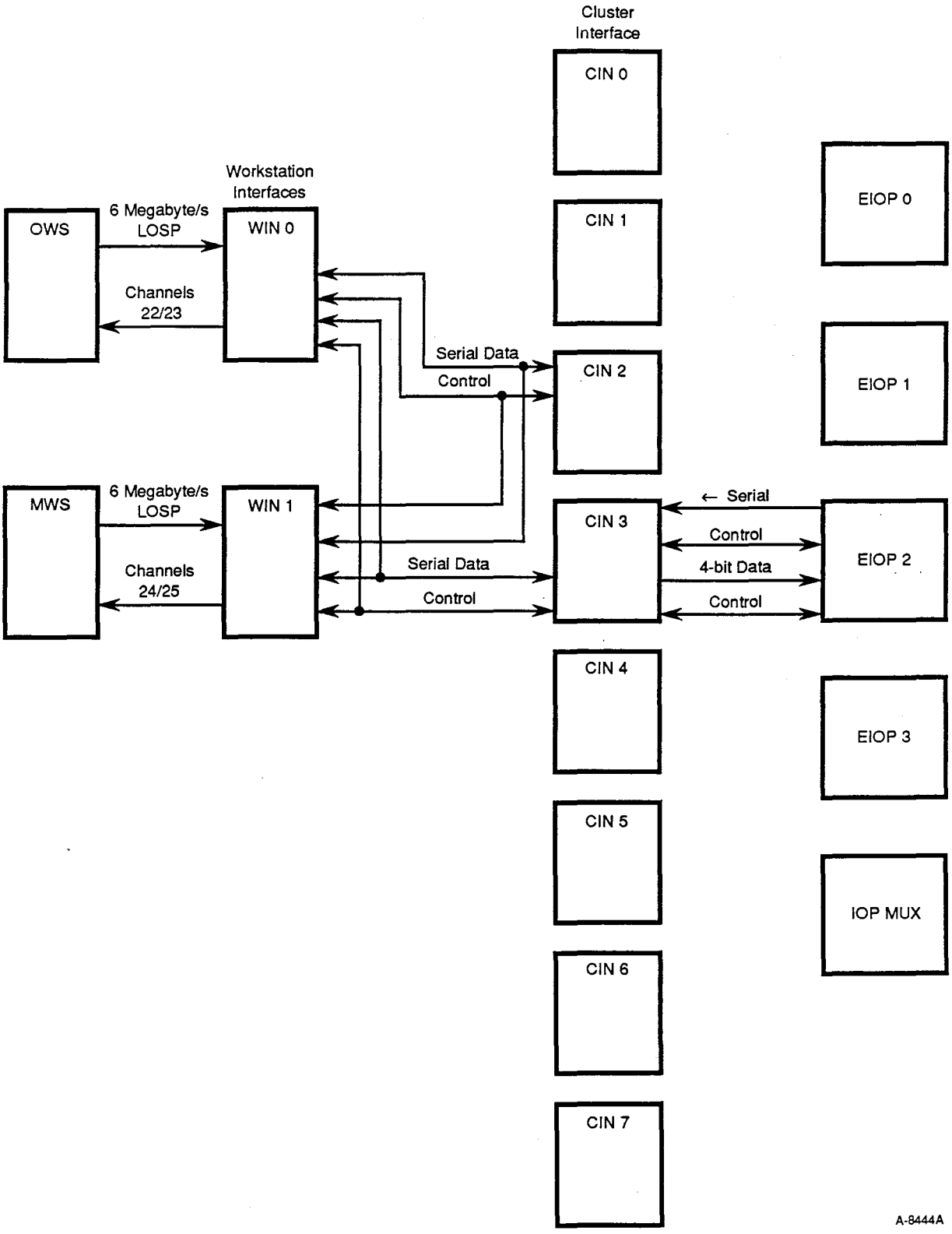


Figure 3-1. CIN/WIN Block Diagram

Cluster Interface/Workstation Interface Quarter Boards

The CIN quarter board consists of five 3WB options and two 3WD options. The WIN quarter board consists of the 3WI, 3WO, 3WA, and 3WS options. Refer to Table 3-1 for a functional description of each option. Refer to Figure 3-9 for the CIN option layout and Figure 3-10 for the WIN option layout.

Table 3-1. CIN/WIN Options and Functional Descriptions

Options	Functional Description
3WDs (two) CIN	Workstation control and interface
3WBs (five) CIN	Data into the IOP
3WA WIN	Data in (parallel to serial)
3WI WIN	Control for WIN
3WO WIN	Data out (serial to parallel) External LOSP-Out control
3WS WIN	Serial data and control out

Cluster Interface/Workstation Interface Data Flow

The input data from the OWS or MWS is sent to the WINs 3WA option. Refer to Figure 3-2 for a CIN/WIN input block diagram. The data arrives 16 bits at a time, but the 3WA sends the data serially to the CIN under control of the 3WI option. The 3WD option sends the data to the 3WB options. One 3WB is enabled to send the data to its IOP 4 bits at a time.

The IOP output data to the workstation is sent from local memory to the CIN and then to the WIN. Refer to Figure 3-3 for a CIN/WIN output block diagram. Local memory (LM) data is sent serially to the 3WD options on the CIN board. The 3WD options direct the data to the proper WIN. The 3WI option on the WIN receives the serial data and sends it to the 3WS option and then it is sent to the 3WO option. The 3WO switches the data from serial to parallel and sends 1-parcel per reference to the OWS or MWS.

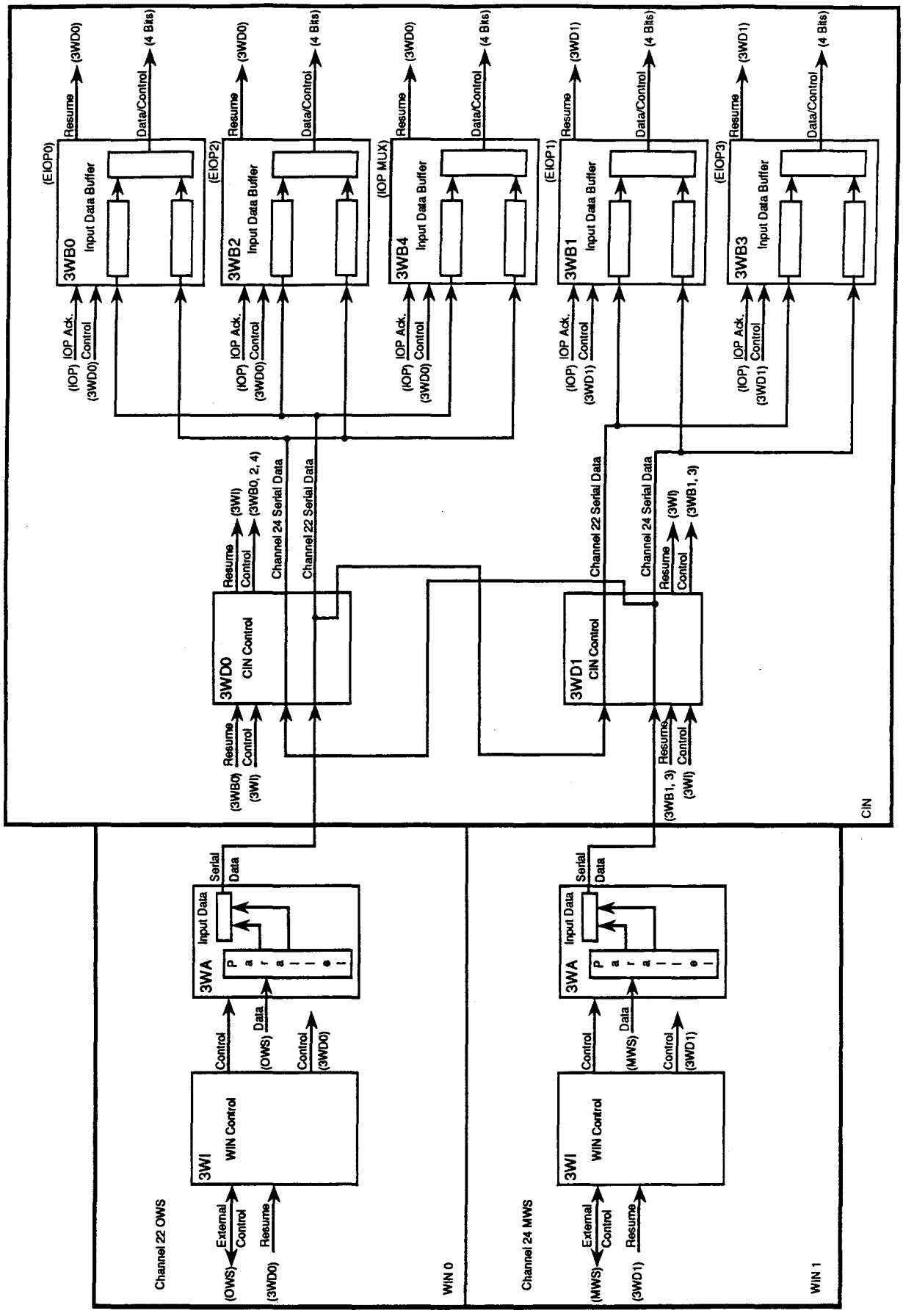


Figure 3-2. CIN/WIN Input Block Diagram

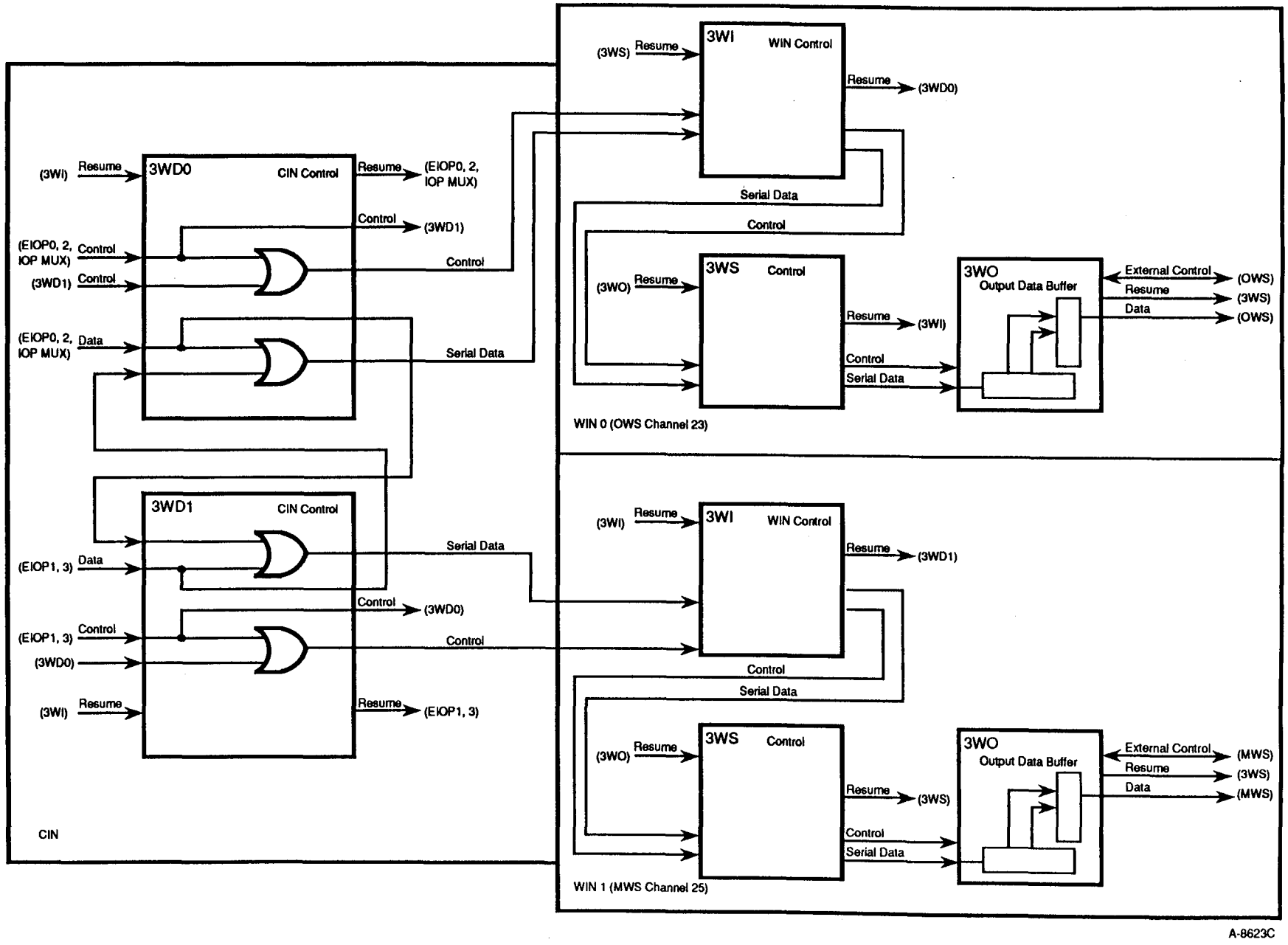


Figure 3-3. CIN/WIN Output Block Diagram

Six Mbyte Low-speed Protocol

The following is a description of the 6-Mbyte LOSP protocol that is used between the WIN quarter boards and the workstations. Refer to Figure 3-4 for a LOSP protocol block diagram.

- Ready. The Ready signal is sent by the sender with each parcel of data. The Ready is a 50 ns pulse.
- Resume. The Resume signal is sent by the receiver to acknowledge Ready and to enable the next Ready. The Resume is a 50 ns pulse.
- Disconnect. The Disconnect signal is sent by the sender to terminate the transfer.

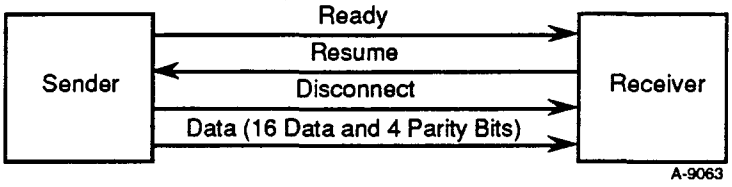


Figure 3-4. 6-Mbyte LOSP Protocol

Cluster Interface/Workstation Interface Input Sequence

The following is a sequential description of an IOP being deadstarted. The header is sent from the workstation to the WIN then to one of eight CINs. The CIN directs the header and the data to the selected IOP. There are two block diagrams to use with this sequence:
Figure 3-5, CIN/WIN Input Block Diagram and Control, is used with steps 1 through 10 and step 15, and Figure 3-6, Workstation Local Memory Write Block Diagram, is used with steps 8, 9, and 11 through 16.

1. Ready Pulse. The workstation sends a Ready Pulse with each parcel of data it sends to the WIN.

Workstation - The workstation sends a WIN 0 with a function 3 that deadstarts the selected IOP, but it must be preceded by a system, cluster, or IOP Master Clear (MC).

3WI - The 3WI option receives the Ready Pulse (I0 - 1) and then sends a Capture LOSP Data (R42) to the 3WA option; if this is a header parcel, the 3WI also sends a Capture Header to the 3WA.

2. Capture LOSP Data. A Capture LOSP Data is sent to the 3WA option to latch the input data into the parallel register.

   3WA - The 3WA option latches the data and parity (I0 - 39) in the parallel register after it receives Capture LOSP Data (I42). The 3WA can hold two data parcels or four header parcels. The 3WA checks the parity and reports the parity errors to the 3WS (R32) option.

3. Capture Header. The 3WI option sends the Capture Header to the 3WA option to latch the header parcels from the workstation.

   3WI - The Capture Header (R45) is enabled by IOP Master Clear or by the previous transfer's Disconnect and remains enabled until a Ready Pulse is received. The 3WI option receives the Ready Pulse (I0 - 1) and then sends Capture Header (R45) to the 3WA option if this is the first parcel of the transfer. After the second and third Ready Pulses, the 3WI sends Capture Header (R44) to the 3WA to save Parcels 1 and 2 of the header. The Capture Header (R41) is sent after the 3WI receives the fourth Ready Pulse, and it captures Parcel 3 of the header which is the cyclic redundancy check (CRC).

   3WA - The 3WA option latches the header parcels after receiving a Capture Header (I41, 44, 45). The header is sent from the workstation to inform the WIN of the command, the function, the cluster select, the IOP select, the local memory address (LMA), and the parcel count. It is always the first word of each transfer. Parcel 0 bits 2^{15} - 2^{12} is the command, 2^{11} - 2^{8} is the function, 2^{7} - 2^{4} is the cluster select, and 2^{3} - 2^{0} is the IOP select. Parcels 1 and 2 of the header are the LMA and parcel count. These parcels, along with parcel 0, are first sent to the CIN and then to the IOP when the workstation sends a WIN 0 command. Parcel 3 is used to check the integrity of the header.

4. Resume. The 3WI option acknowledges receiving each parcel and enables the next parcel by sending a Resume to the workstation.

   3WI - The Resume (R38) is a 50 ns pulse to the workstation and is sent if the serial register on the 3WA option is empty. Steps 2 and 4 are performed until the workstation sends a Disconnect (refer to step 15).

5. Send Header. The 3WI option sends the Send Header to inform the 3WA option to output the Cluster Select to the 3WI.

   3WA - The 3WA option checks the integrity of the header with the use of CRC, which is parcel 3 of the header. If the header is good, the 3WA responds with Send Header (R30), Cluster Select (R16 - 19), Function Decode (R22), and data bit 14 (R24). If the header is bad, the 3WA sends Bad Header (R29) to 3WI option and Header Error (R32 - 33) to the 3WS option.

   3WI - The 3WI option uses the Cluster Select (I4 - 7) to direct the data to the correct CIN. If the Function Decode (I12) is set, the 3WA option received a WIN command 0 or 4. If data bit 14 (I14) (2^{14} of the header parcel 0) is set, do a WIN command 4; but if it is clear, do a WIN command 0. A WIN command 4 is a loopback test. The header parcels are sent back to the workstation via the 3WA and 3WO options if a WIN command 4 is decoded.

6. Go Serial Data. The 3WA option loads the parallel register into the serial register after receiving Go Serial Data from the 3WI option.

   3WA - After receiving the Go Serial Data (I40), the 3WA loads the serial register with the parallel register and outputs the parcel of data serially (R0 - 7) to the correct CIN (3WD I1). All received parcels are loaded into the serial register except parcel 3 of the header.

7. Serial Control. The Serial Control informs the 3WD option there is serial data being sent from the 3WA option.

   3WI - The 3WI option generates the correct Serial Control (R0 - 7) after decoding the Cluster Select (I4 - 7). If I4 - 7 are zeroes, the 3WI sends R0 to CIN 0. If the Serial Control is a 1 clock period (CP) pulse, data is being sent; if it is a 2 CP pulse, it is a disconnect; and if it is a 3 CP pulse, it is a I/O Master Clear.

   3WD - The 3WD option receives Input Control (I0) when the WIN is sending a serial parcel of data and parity to the CIN. The data is sent from the 3WA to the 3WD. The 3WD passes the Input Control (R30 or R32) and Data (R31 or R33) to the 3WB options or Input Control (R10) and Data (R11) to the other 3WD.

3WB - After receiving Input Control (I0 or I2), the 3WB options accept the serial data and parity bits (I1 or I3) from the 3WD options (R31 or R33). After receiving all 16 bits of data, the 3WB option sends a Control (R10 - 13) to 3AW option (I37 - 40). Each 3WB has a force IOP Select (I30 - 32) and this force select is exclusive ORed with the IOP Select from the WIN (header parcel 0, bits 2^3 - 2^0), so only one 3WB is able to send control to its 3AW.

8. Control. The Control is sent to the IOP informing it of a WIN function or data.

3WB - There are four Control bits (R10 - 13) that are also used to send Function and data to the IOP (3AW). The 3AW option then latches the Control bits (I37 - 40) along with the Function bits or data parity bits and data 2^3 - 2^0 (header parcel 0 does not send bits 2^3 - 2^0). Refer to Table 3-2 for the control bit functions and Table 3-3 for the proper sync time of the control and data bits.

Table 3-2. Control Signals to the IOP

R13	R12	R11	R10	Comments
—	—	0	0	No-op
—	—	1	1	IOP Master Clear
0	0	0	1	Function to the IOP (header parcel 0 bits 2^{11} - 2^8)
0	1	0	1	Local memory address to the IOP (header parcel 1)
1	0	0	1	Parcel count to the IOP (header parcel 2)
1	1	0	1	Write data to local memory
1	0	1	0	Disconnect for local memory write WIN 0 function 2
1	1	1	0	Disconnect

Table 3-3. Control and Data Sync Time to the IOP for Channels 22 and 24

Sync	Channel 22	Channel 24
Sync 0	Control time R10 - 13	Data bits 2^7 - 2^4 if Go Input Data (I10) was received at sync 5
Sync 1	Function bits 2^{11} - 2^8 of header parcel 0 or data parity	Data bits 2^{11} - 2^8 if Go Input Data (I10) was received at sync 5
Sync 2	Data bits 2^3 - 2^0	Data bits 2^{15} - 2^{12} if Go Input Data (I10) was received at sync 5
Sync 3	Data bits 2^7 - 2^4 if Go Input Data (I10) was received at sync 2	Control time R10 - 13
Sync 4	Data bits 2^{11} - 2^7 if Go Input Data (I10) was received at sync 2	Function bits 2^{11} - 2^8 of header parcel 0 or data parity
Sync 5	Data bits 2^{15} - 2^{12} if Go Input Data (I10) was received at sync 2	Data bits 2^3 - 2^0

9. Go Input Data. The 3AW option acknowledges 3WB options Control signal with Go Input Data when it can accept bits 2^{15} - 2^4.

   3AW - If this is parcel 0 of the header, the 3AW option decodes the function 3 (2^{11} - 2^8 header parcel 0), sets the Busy Flag, and enables the Channel Interrupt. The next two parcels are the LMA and parcel count and they are sent to the 3AL option. The following parcels are local memory data. The 3AW sends Enter Data (R4) to the 3AM along with a parcel of data and a Write Request (R5) to the 3AK.

   3AL - The 3AL option receives the LMA and parcel count from the 3AW option and writes it into the workstation LMA and parcel count registers.

   3AM - The 3AM option latches the parcel of data from the 3AW option after receiving Enter Data (I74).

10. Input Resume. The 3WB option sends an Input Resume to the 3WD option requesting the next parcel.

    3WB - The 3WB option sends Input Resume (R0 - 1) to the 3WD option after receiving Go Input Data (I10). Header parcel 0 is an exception. The 3WB receives Header parcel 0 and immediately sends an Input Resume.

    3WD - The 3WD option passes Input Resume (R0) to the WIN (3WI).

    3WI - The 3WI option receives Input Resume (I20 - 27) and sends a Go Serial Data (R40) to the 3WA option if the parallel register is full. Steps 6 through 10 are performed until a Disconnect is received.

11. Write Request. The Write Request to the 3AK option is requesting to write a parcel of data to local memory.

    3AW - After receiving the control (I37 - 40) from the 3WB option, the 3AW (R5) option sends a Write Request to the 3AK (I50) option.

12. I/O Reference Request. The 3AK option sends a request to the 3AN option for each parcel of data.

    3AK - The 3AK option is local memory reference control for the workstation, port 0, and port 1. When there is no reference in progress, the 3AK sends an I/O Reference Request (R25) and I/O Write Request (R20) to the 3AN option and Workstation Request (R26) to the 3AM option after receiving LM Write Request (I50) from the 3AW option.

    3AN - The 3AN option is local memory control, so it receives the I/O Reference Request (I24), and sends back I/O Acknowledge (R17) when local memory is free. The 3AN controls LM conflicts between the CPU and I/O channels.

13. I/O Acknowledge. When local memory is free, the 3AN option sends an I/O Acknowledge to the 3AK, 3AL, and 3AM options and a Go Write signal to the 3AM option.

    3AK - The 3AK option clears the I/O Reference Request after receiving the I/O Acknowledge (I60) and sends workstation Acknowledge (R30) to the 3AW option.

3AL - The 3AL option reads out the LMA to the memory arrays and increments the LMA and decrements the parcel count after receiving I/O Acknowledge (I25). The 3AL checks the LMA and parcel count for parity errors each time they are read out.

3AM - The 3AM option gates the workstation data (R0 - 21) and a Write Enable (R33 - 34) to the memory arrays after receiving I/O Acknowledge (I83) and Go Write (I90) with workstation Request (I85) set.

3AW - After receiving workstation Acknowledge (I25) from the 3AK option, the 3AW option sends Write Reference Acknowledge (R22) to the 3WB options.

14. Write Reference Acknowledge. The IOP sends a Write Reference Acknowledge to the CIN.

3WB - After receiving the Write Reference Acknowledge (I12), the 3WB option checks for disconnect from the 3WD option.

15. Disconnect. The workstation sends a Disconnect to the 3WI option to terminate the transfer.

3WI - The 3WI option receives the Disconnect (I2 - 3) and then sends a Disconnect (R46) to the 3WA option (I46) and a 2 CP Serial Control pulse to the 3WD option, which means disconnect.

3WA - After receiving Disconnect (I46), the 3WA option is enabled to receive the next transfer.

3WD - The 3WD option passes the 2 CP Serial Control (R30 or R32) to the 3WB option.

3WB - The 3WB option receives the 2 CP Input Control (I0 or I2) and clears R10 and sets R11 - 13 which means Disconnect after receiving I/O Acknowledge. Refer to Table 3-2 for control bits R10 - 13.

3AW - After receiving Control (I37 - 40) from the 3WB option, the 3AW option sets the Done Flag.

16. Done Flag. When a Disconnect is received, the Done Flag is set.

3AW - The 3AW option sets the Done Flag and sends an Interrupt (R17) to the 3AK option. The System Interrupt is enabled by MC.

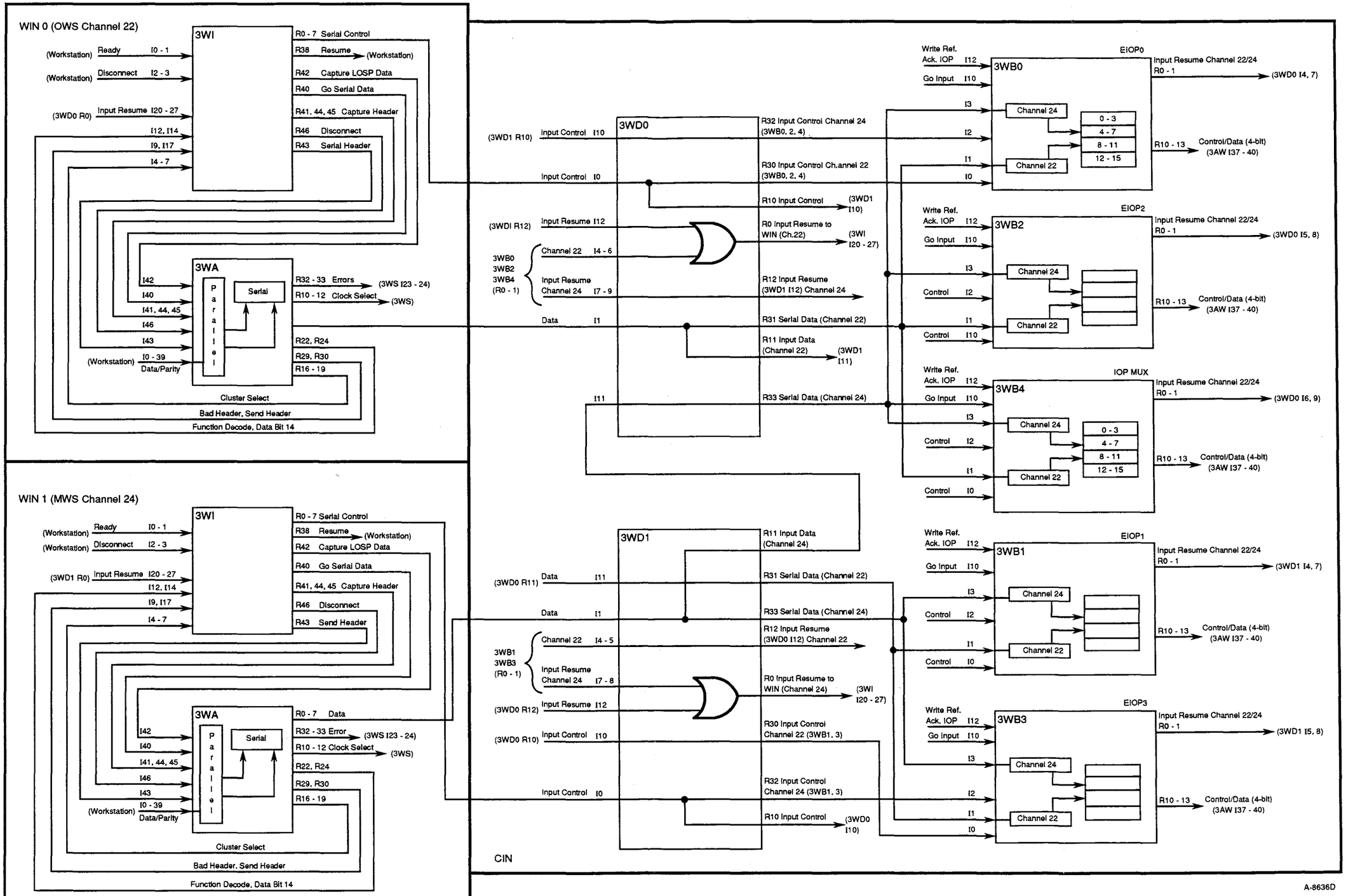


Figure 3-5. CIN/WIN Input Block Diagram and Control

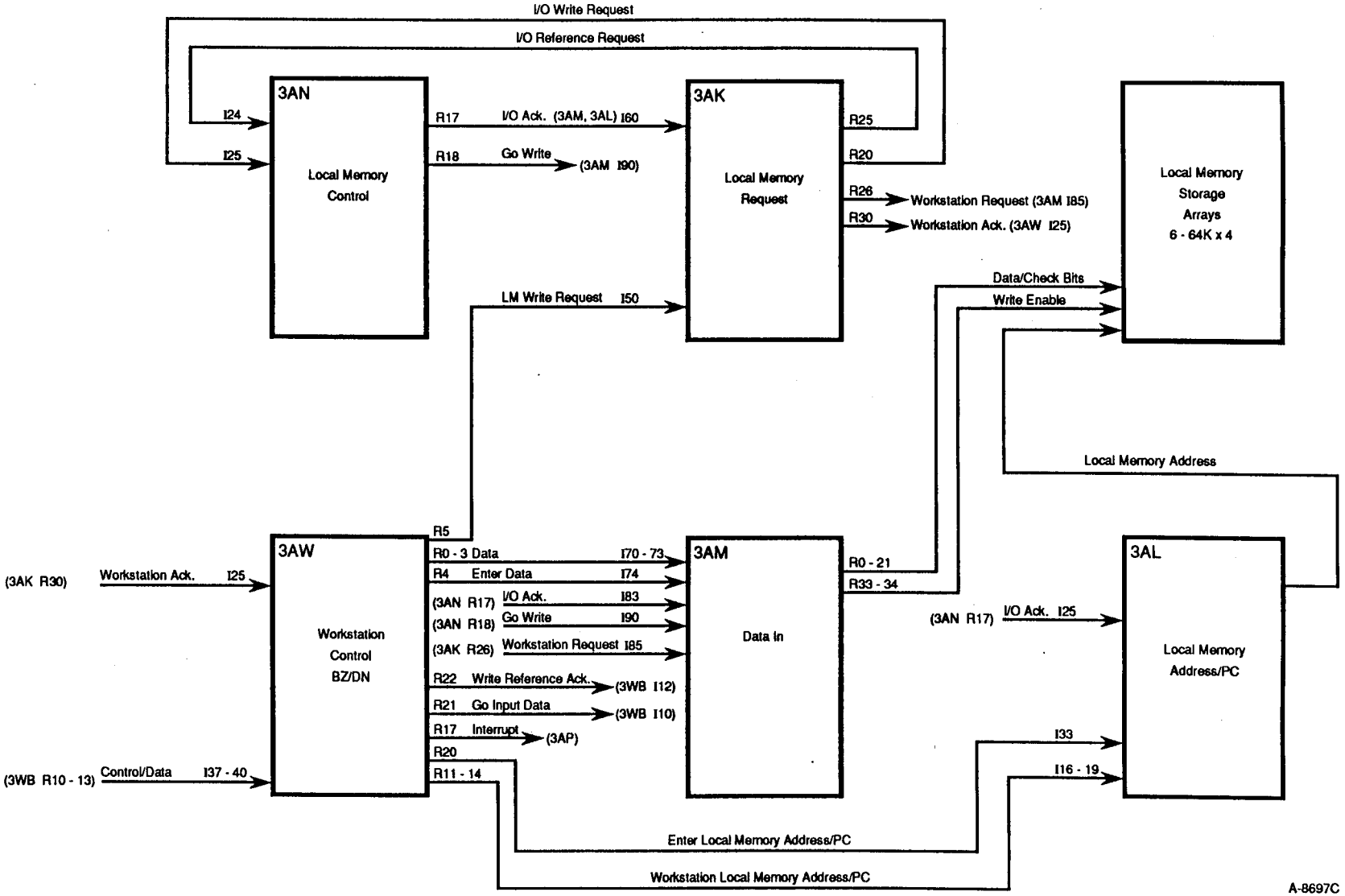


Figure 3-6. Workstation Local Memory Write Block Diagram

Cluster Interface/Workstation Interface Output Sequence

The following is a sequential description of a workstation reading an IOPs local memory. The Header is sent from the workstation to the WIN then to one of eight CINs. The CIN directs the header to the selected IOP. There are two block diagrams to use with this sequence: Figure 3-7, CIN/WIN Output Block Diagram and Control, is used with steps 1 through 4 and steps 8 and 12, and Figure 3-8, Workstation Local Memory Read Block Diagram, is used with steps 4 through 11.

1. Read Reference Request. The 3AW option sends a Read Request to the 3AK and 3AO options.

Workstation - A WIN 0 with a function of six reads the local memory to the workstation. Perform steps 1 through 10 and step 15 of the CIN/WIN input sequence to input the header parcels to the IOP.

3AW - The 3AW option sends a Read Request (R6) to the 3AK option after decoding a WIN 0 with a function of six or receiving a Output Resume from the 3WD option.

2. I/O Reference Request. The 3AK option sends a I/O Reference Request to the 3AN option for a parcel of data.

3AK - The 3AK option is local memory reference control for the workstation, port 0, and port 1. If there is no other request in progress, the 3AK sends an I/O Reference Request (R25) to the 3AN option.

3AN - The 3AN option is local memory control, so it receives the I/O Reference Request (I24), and sends the I/O Acknowledge (R17). The 3AN controls LM conflicts between the CPU and the I/O channels.

3. I/O Acknowledge. When local memory is free, the 3AN option sends an I/O Acknowledge to the 3AK and 3AL options.

3AK - The 3AK option clears the I/O Reference Request after it receives the I/O Acknowledge (I60) and then sends a Workstation Acknowledge (R30) to the 3AO and 3AW options.

3AL - The 3AL option reads the LMA to local memory, increments the LMA, and decrements the parcel count after receiving I/O Acknowledge (I25). The 3AL checks the LMA and parcel count for parity errors each time they are read out. The 3AL reports parity to the 3AN and 3AO options.

3AN - The data and check bits (CBs) (I0 - 21) are sent to the 3AN option. The data is checked for errors and then sent to 3AO option (I20 - 35). The 3AN reports errors to the 3AO.

3AO - The 3AO option receives a Workstation Acknowledge (I74) from the 3AK option and latches the data (I20 - 35). The Data (R60) is sent serially to the CIN board (3WD).

3AW - After receiving Workstation Acknowledge (I25) from the 3AK option, the 3AW option sends Output Control (R23 Channel 23 and R24 Channel 25) to the CIN (3WD).

4. Output Control. The Output Control is sent from the 3AW option to the 3WD option along with a serial parcel of data.

   3WD - The 3WD0 option or 3WD1 option receives the Output Control (I30 - 32 Channel 23, I36 - 38 Channel 25) and Data (I33 - 35) from the 3AW option. The 3WD0 receives data and control directly from the EIOP0, EIOP2, and IOP MUX, while the 3WD1 receives data and control from EIOP1 and EIOP3. The 3WD0 option outputs data to the operator workstation WIN and the 3WD1 outputs data to the maintenance workstation WIN. If the EIOP0 sends data and control to the MWS, the data and control pass through 3WD0, 3WD1, and then to the WIN for the MWS.

5. Output Control to Workstation. Each parcel of serial data transferred from the CIN (3WD) to the WIN (3WI) is proceeded by Output Control to Workstation.

   3WD - The Output Control to Workstation (R1) is sent from one of eight CINs to the 3WI option (I30 - 37) if that cluster is outputting data (R2) to the WIN.

   3WI - The 3WI option passes the Serial Output Control (R18 - 19) and serial data (R20 - 21) to the 3WS option the next clock period.

   3WS - After receiving the Serial Control (I17 - 18) and Data (I19 - 20), the 3WS option sends Control (R0) and Serial Data (R1) to the 3WO option.

6. Control. The Control enters the serial parcel of data into the serial register.

3WO - The 3WO option waits for all 16 bits of serial data (I10) and then loads the serial register into the parallel register if the parallel register is empty. The 3WO send a Ready Pulse to the workstation and Serial Resume to the 3WS option after it loads the parallel register.

7. Serial Resume. If the serial register is empty, the 3WO option sends Serial Resume to the 3WS option.

   3WO - After all 16 bits of the serial data have been received, the serial register is loaded into the parallel register if the parallel register is empty. Then a Serial Resume (R25) is sent to the 3WS (I21) option requesting the next parcel of data.

   3WS - The 3WS option receives Serial Resume (I21) and passes it (R2) to the 3WI (I16) option.

   3WI - The 3WI option sends a Serial Output Resume to Cluster 0 - 7 (R10 - 17) to the 3WD (I2) option after receiving Serial Resume (I16) from the 3WS option.

8. Output Resume. The WIN sends an Output Resume to the CIN requesting the next parcel of data.

   3WD - The Output Resume (R34 - 39) is passed to the IOP or to the other 3WD (R15) option then to the IOP. Refer to Table 3-4 for the proper output resume.

Table 3-4. Output Resume

Term	Channel	3WD0	3WD1
R15	23	3WD1 I15	—
R15	25	—	3WD0 I15
R34	23	EIOP0	EIOP1
R35	25	EIOP0	EIOP1
R36	23	EIOP2	EIOP3
R37	25	EIOP2	EIOP3
R38	23	IOP MUX	—
R39	25	IOP MUX	—

3AW - The 3AW option receives Output Resume (I41 - 42) and sends a Read Reference Request (R6) to local memory (3AK). Steps 1 through 8 are performed until the parcel count equals zero.

9. Ready Pulse. A Ready Pulse is sent to the workstation when there is a parcel of data and parity to be transferred to the workstation.

   3WO - A 50 ns Ready Pulse (R20) is sent to the workstation when the the parallel register is loaded.

10. Resume. The workstation responds back with a Resume if it can accept the next parcel of data.

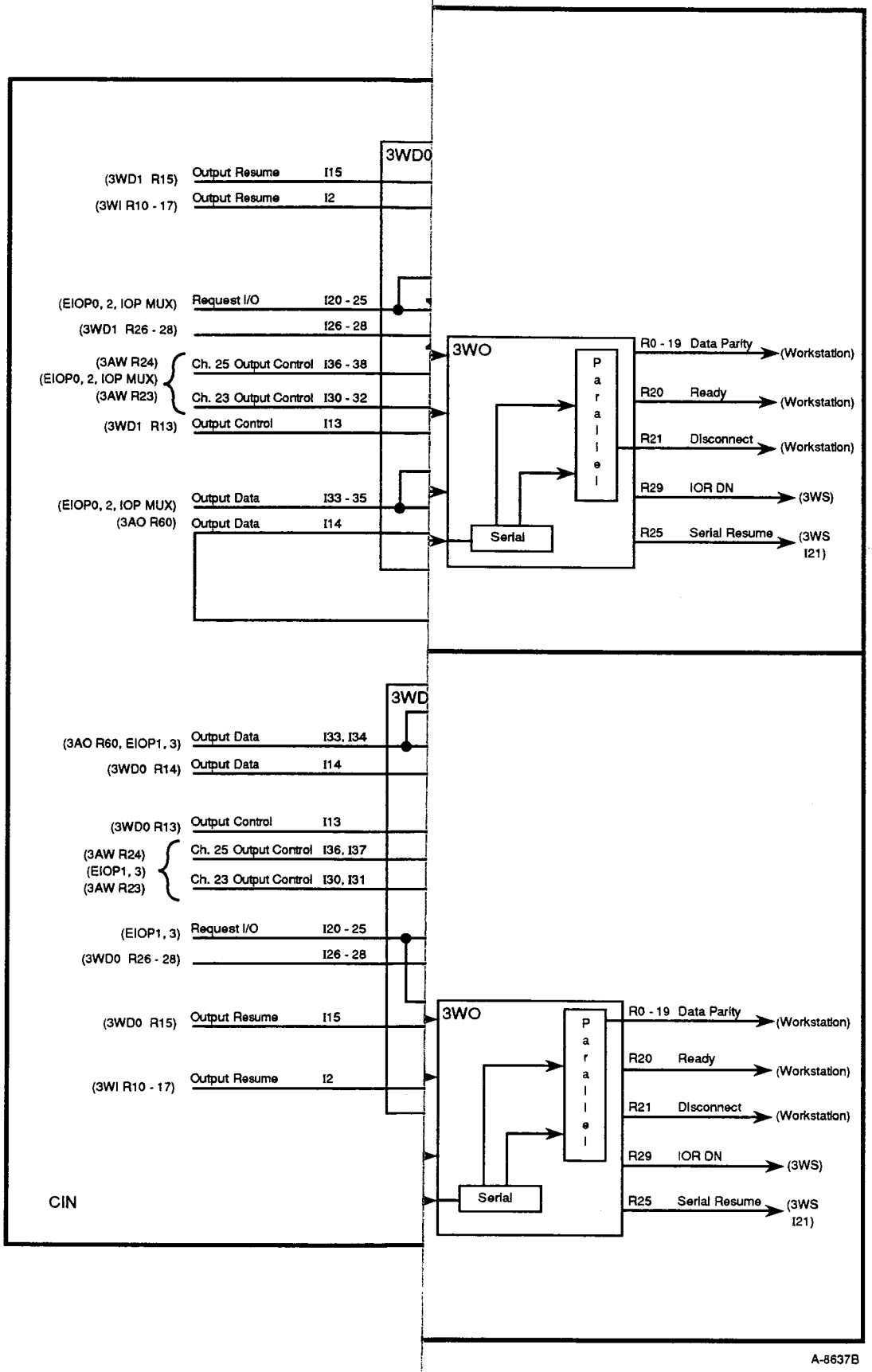
    3WO - After receiving a Resume (I0 - 1), the 3WO option loads the serial register into the parallel register if the serial register is full. Go to step 9 if the serial register is full.

11. Disconnect. The Disconnect is sent to the workstation when the IOP wants to terminate the transfer.

    3WO - The Disconnect is sent to the workstation after the 3WO option receives a Resume (I0 - 1) and IOR Not Active (I6) (parcel count = 0).

12. Done Flag. The transfer is complete when the parcel count equals zero.

    3AW - The 3AW option waits for the workstation parcel count until the 3AL option equals zero and then clears I/O Active on the 3WI option.


3WD0
(3WD1 R15)
Output Resume
I15
(3WI R10 - 17)
Output Resume
I2
(EIOP0, 2, IOP MUX)
Request I/O
I20 - 25
(3WD1 R26 - 28)
I26 - 28
(3AW R24)
(EIOP0, 2, IOP MUX)
(3AW R23)
Ch. 25 Output Control
I36 - 38
Ch. 23 Output Control
I30 - 32
(3WD1 R13)
Output Control
I13
(EIOP0, 2, IOP MUX)
(3AO R60)
Output Data
I33 - 35
Output Data
I14
3WO
Parallel
Serial
R0 - 19 Data Parity
(Workstation)
R20 Ready
(Workstation)
R21 Disconnect
(Workstation)
R29 IOR DN
(3WS)
R25 Serial Resume
(3WS I21)
3WD
(3AO R60, EIOP1, 3)
Output Data
I33, I34
(3WD0 R14)
Output Data
I14
(3WD0 R13)
Output Control
I13
(3AW R24)
(EIOP1, 3)
(3AW R23)
Ch. 25 Output Control
I36, I37
Ch. 23 Output Control
I30, I31
(EIOP1, 3)
Request I/O
I20 - 25
(3WD0 R26 - 28)
I26 - 28
(3WD0 R15)
Output Resume
I15
(3WI R10 - 17)
Output Resume
I2
3WO
Parallel
Serial
R0 - 19 Data Parity
(Workstation)
R20 Ready
(Workstation)
R21 Disconnect
(Workstation)
R29 IOR DN
(3WS)
R25 Serial Resume
(3WS I21)
CIN
A-8637B

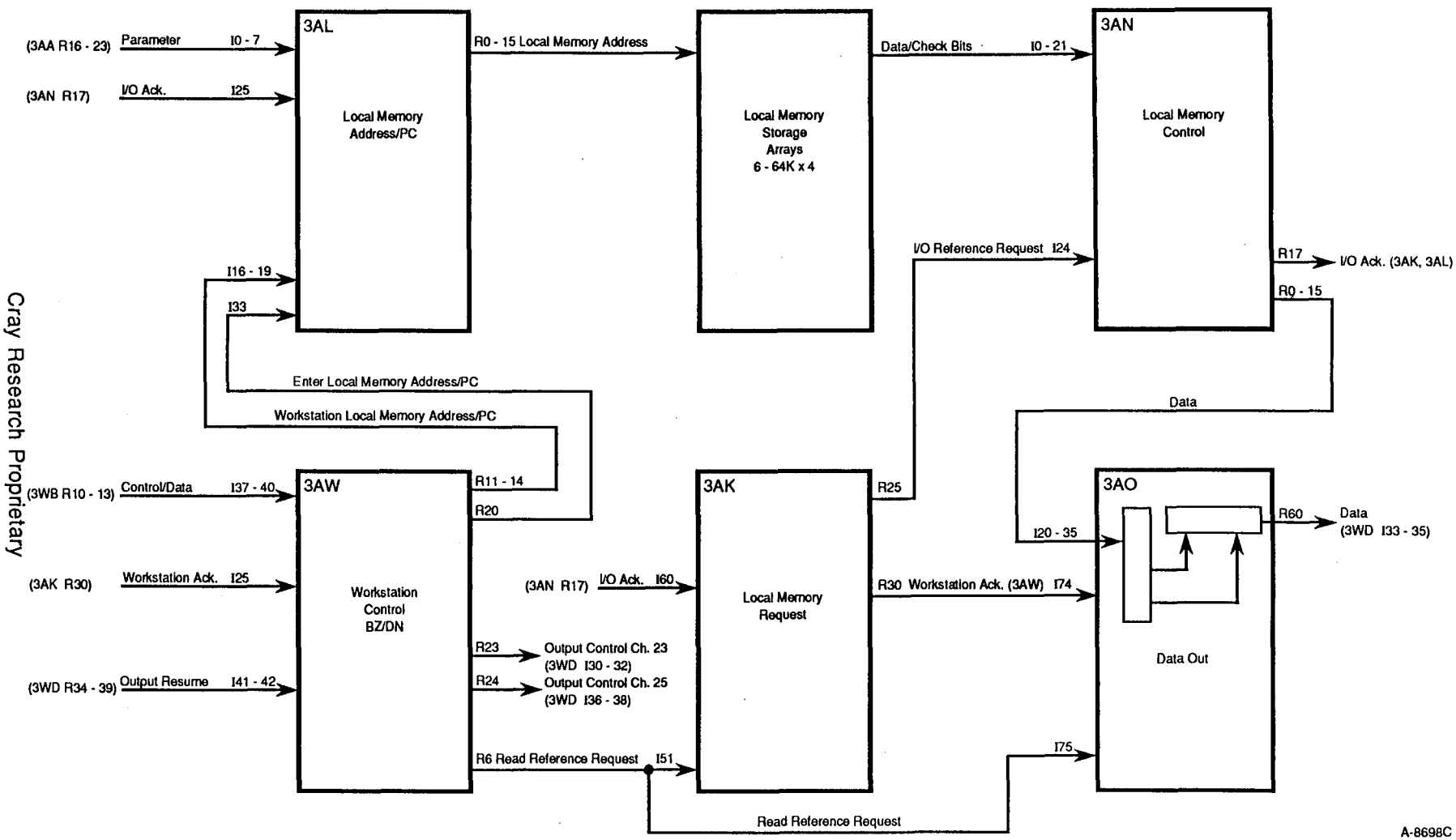


Figure 3-8. Workstation Local Memory Read Block Diagram

WIN 2 Return I/O Status Request Sequence

The following is a sequential description of a WIN command 2 returning I/O status. The I/O status is returned after all WIN commands input their header parcels. Perform steps 1 through 5 of the CIN/WIN Input Sequence to input the header parcels. Refer to Figure 3-9 for a WIN block diagram.

1. 3WI - The 3WI option sends a Go IOR Status (R22) to the 3WS option and the 3WO option after receiving the fourth Ready from the workstation.

2. 3WA - If there is an error on the header parcels the 3WA option sends the errors (R32 - 33) to the 3WS option.

3. 3WS - The 3WS option logs header errors (I23 - 24) and flags IOP errors (I0 - 7). The errors are sent to the workstation as a response header. After receiving Go IOR Function (I16), the 3WS outputs the Control (R0) and a response header parcel (R1) to the 3WO option. The response header is a 4-parcel packet.

4. 3WO - The 3WO option loads the response parcel into the serial register and then into the parallel register. Then the 3WO sends a Ready (R20) and a parcel of data with parity (R0 - 19) to the workstation. The 3WO waits for a Resume (I0) from the workstation after sending a Ready. The 3WO sends a Serial Resume (R25) to the 3WS option for the next parcel of the response header.

5. 3WS - The 3WS option outputs the Control (R0) and the next parcel of the response header (R1) to the 3WO option after receiving Serial Resume (R25).

WIN 3 Select Clock Margins Sequence

The following is a sequential description of a WIN command 3 selecting clock margins. Only WIN 1 (MWS WIN) is capable of selecting the clock margins. Perform steps 1 through 5 of CIN/WIN Input Sequence to input the header parcels. Refer to Figure 3-9 for a WIN block diagram.

1. 3WA - The 3WA option decodes the WIN command 3 and sends the clock select (R10 - 12) to the 3WS option. The clock select is 2^2 - 2^0 of header parcel 0.

2. 3WS - The 3WS option passes the clock select (R12 - 14) to the clock module.

WIN 4 Workstation Interface Loopback Sequence

The following is a sequential description of a WIN command 4 loopback mode. In loopback mode the WIN receives the header parcels and then sends the header parcels back to the workstation. Perform steps 1 through 5 of the CIN/WIN Input Sequence to input the header parcels. Refer to Figure 3-9 for a WIN block diagram.

1. 3WA - The 3WA option receives the header parcel 0 and then decodes bits 2^{15} - 2^{12} of parcel 0. After decoding a WIN 4 command, the 3WA outputs Function Decode (R22) and Data Bit 14 (R24) to the 3WI option. The Function Decode informs the 3WI that a WIN command 0 or 4 has been decoded and if Data Bit 14 is set it is a WIN command 4 loopback. The 3WA outputs the serial loopback data (R9) to the 3WO.

2. 3WI - The 3WI option sends Select Loopback Mode (R39) to the 3WO optionafter receiving Function Decode (I12) and Data Bit 14 (I14). Then the 3WI outputs a Loopback control (R9) to the 3WO and a Go Serial Data (R40) to the 3WA option for each parcel of the header.

3. 3WO - The 3WO option receives Loopback Control (I7) from the 3WI option and the loopback data (I8) from the 3WA option. Then the 3WO outputs a Ready (R20) and a parcel of data and parity (R0 - 19) to the workstation. The 3WO outputs a Loopback Serial Resume (R24) to the 3WI if the serial register is empty after receiving a Resume (I0) from the workstation.

4. 3WI - The 3WI option receives the Serial Loopback Resume (I29) and then sends a Go Serial Data (R40) to the 3WA option and a Loopback Control (R9) to the 3WO option.

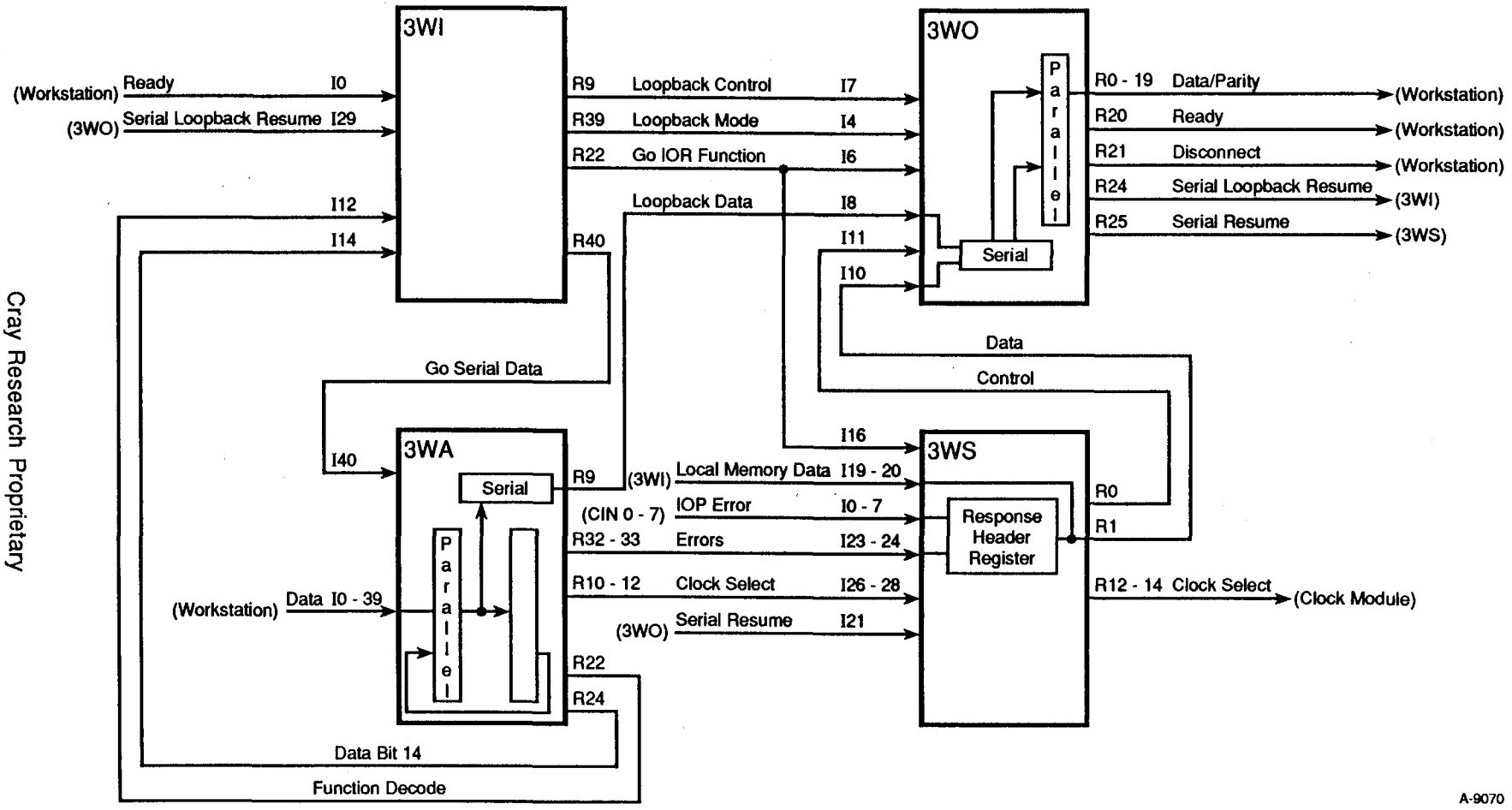


Figure 3-9. WIN Status, Clock Select, and Loopback Block Diagram

Master Clear Fanout

The workstation sends I/O Master Clear to Master Clear the WIN quarter board. The IOS-E has three types of Master Clears: System, Cluster, and IOP. A System Master Clear includes Cluster and IOP Master Clears and master clears all IOS-E hardware. A Cluster Master Clear includes an IOP Master Clear and master clears all IOPs and channel adapters belonging to that Cluster. An IOP Master Clear master clears a specific IOP and its channel adapters. A WIN 5 command is a System Master Clear, a WIN 0 with a function 11 is a Cluster Master Clear, and a WIN 0 with a function 10 is an IOP Master Clear. Both the OWS and the MWS are capable of sending these functions.

I/O Master Clear

The 3WO option receives the I/O Master Clear (I2 - 3) from the workstation and fans it out (R27 - 28) to the 3WS (I22) option. The 3WS fans out I/O Master Clear (R3) to the 3WA (I47) option and 3WI (I11) option. The 3WI passes the I/O Master Clear to the CIN in the form of a 2 CP wide Serial Control (R0 - 7). The 3WD option receives the 2 CP Serial Control and passes it to the 3WB options. The 3WB options send I/O Master Clear (R10 - 13) to the IOP.

WIN 5 System Master Clear

The 3WA options on the WINs decodes System Master Clear. The System Master Clear is passed to the 3WO and 3WS options. The 3WS (R4 - 11) fanout the System Master Clear to the 3WB1 (OWS Master Clear) option and 3WB4 (MWS Master Clear) option. The 3WB1 (R27 - 28) fans out the OWS System Master Clear to all five 3WB options, and the 3WB4 (R27 - 28) fans out the MWS System Master Clear to all five 3WB options. Refer to Table 3-5 for the System Master Clear fanout. Each 3WB then fans out System Master Clear (R20 - 26) to all the IOS-E hardware.

WIN 0 Function 11 Cluster Master Clear and Function 10 IOP Master Clear

The 3WB options also decode cluster and IOP Master Clears. R20 - R24 also fans out cluster and IOP Master Clears. Table 3-5 shows the quarter boards and the buffer board that each 3WB fans out Master Clear to. Each quarter board and the buffer board receives Master Clear and fans it out to its options.

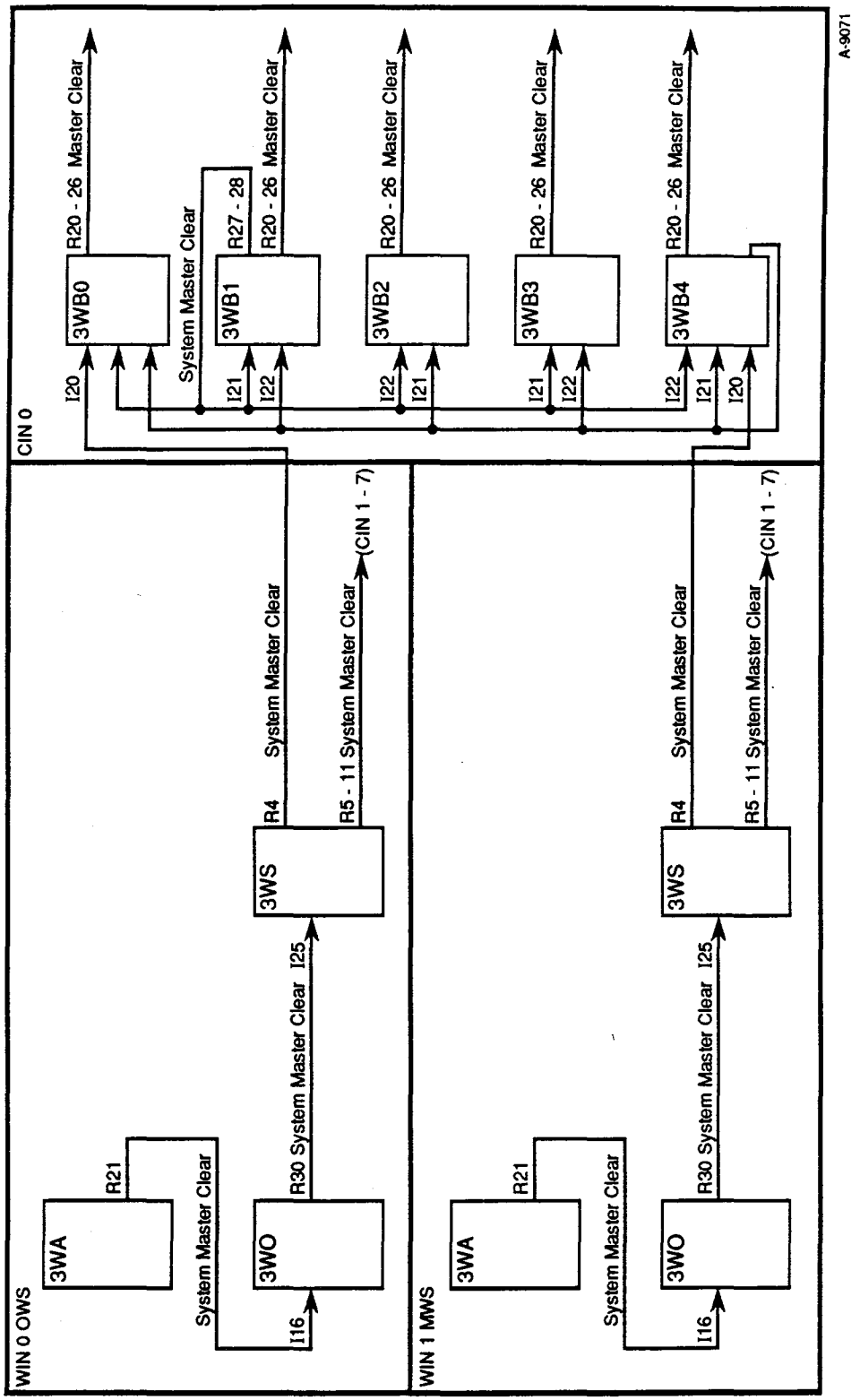


Figure 3-10. Master Clear Fanout

Table 3-5. System, Cluster, and IOP Master Clear Fanout

Boolean Term	3WB0	3WB1	3WB2	3WB3	3WB4
R20	EIOP0 3AP I69	EIOP1 3AP I69	EIOP2 3AP I69	EIOP3 3AP I69	IOP MUX 3AP I69
R21	EIOP0 CA 1	EIOP1 CA 5	EIOP2 CA 11	EIOP3 CA 15	Not used
R22	EIOP0 CA 3	EIOP1 CA 7	EIOP2 CA 13	EIOP3 CA 17	Not used
R23	EIOP1 CA 4	EIOP0 CA 0	EIOP3 CA 14	EIOP2 CA 10	Not used
R24	EIOP1 CA 6	EIOP0 CA 2	EIOP3 CA 16	EIOP2 CA 12	Not used
R25	HCM0 3SO I9	Not used	Not used	HCM1 3SO I9	Not used
R26	Not used	Buffer 3BM0 I70 3BM0 I71	Not used	Not used	Buffer 3BM20 I70 3BM20 I71

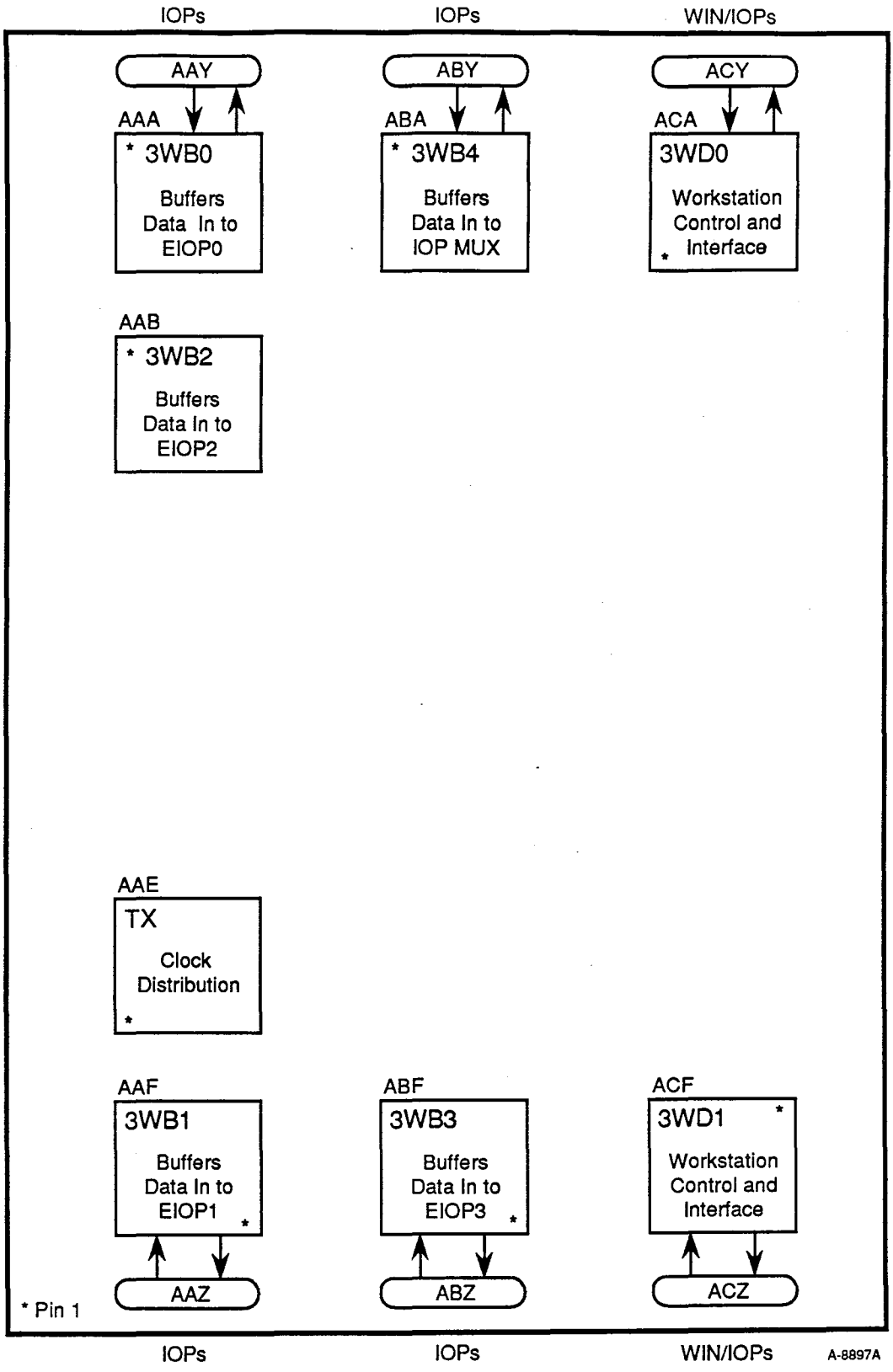


Figure 3-11. CIN Quarter Board Integrated Circuit Layout

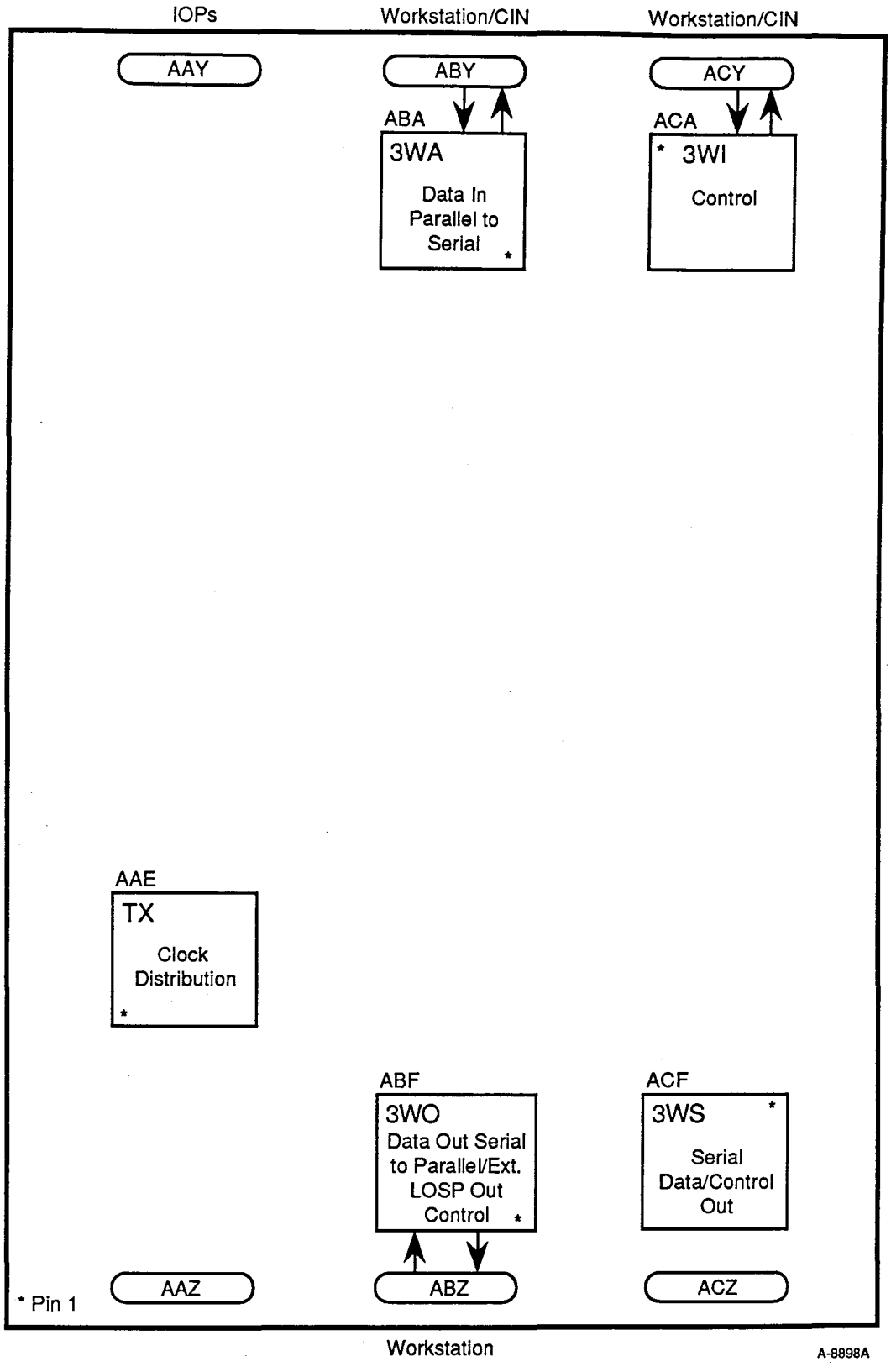


Figure 3-12. WIN Quarter Board Integrated Circuit Layout

4 BUFFER BOARD

Each I/O Cluster (IOC) has a buffer board specific to that cluster. The buffer board is a single cold plate module the same size as a CRAY Y-MP module with a full sized printed circuit (PC) board on each side, as opposed to quarter boards. Each PC board contains the logic for two EIOPs, one high-speed (HISP) channel and eight channel adapter channels. Side A handles EIOP0 and EIOP2, HISP channel 1, and channel adapter channels 0 to 3 and 10 to 13. Side B handles EIOP1 and EIOP3, HISP channel 0 and channel adapter channels 4 to 7 and 14 to 17. Each channel adapter is connected to its own buffer which will hold 65,536 72-bit words. No other channel adapter can access this buffer of memory.

An EIOP controls four channel adapters and can access the buffers associated with those four channels. EIOP0 controls channels 0 to 3, EIOP1 controls channels 4 to 7, EIOP2 controls channels 10 to 13, and EIOP3 controls channels 14 to 17. EIOPs cannot send data to or receive data from a buffer controlled by another EIOP.

Each HISP channel can access any one of the 16 buffers on a buffer board. HISP 1 is considered onboard HISP data to channels 0 to 3 and 10 to 13 and offboard HISP data to channels 4 to 7 and 14 to 17. HISP 0 is considered onboard HISP data to channels 4 to 7 and 14 to 17 and offboard HISP data to channels 0 to 3 and 10 to 13.

Two sets of pointers are used for addressing transfers in to or out of a buffer. Pointers a and b are used for channel adapter data transfers while pointers A and B are used for HISP and EIOP transfers. Each set of pointers is allowed to access memory on consecutive memory cycles, which allows for a 200 megabyte per second transfer rate on both. The a and b pointers can be incremented or decremented to support backward tape reads. HISP transfers have priority over EIOP transfers when using the A and B pointers.

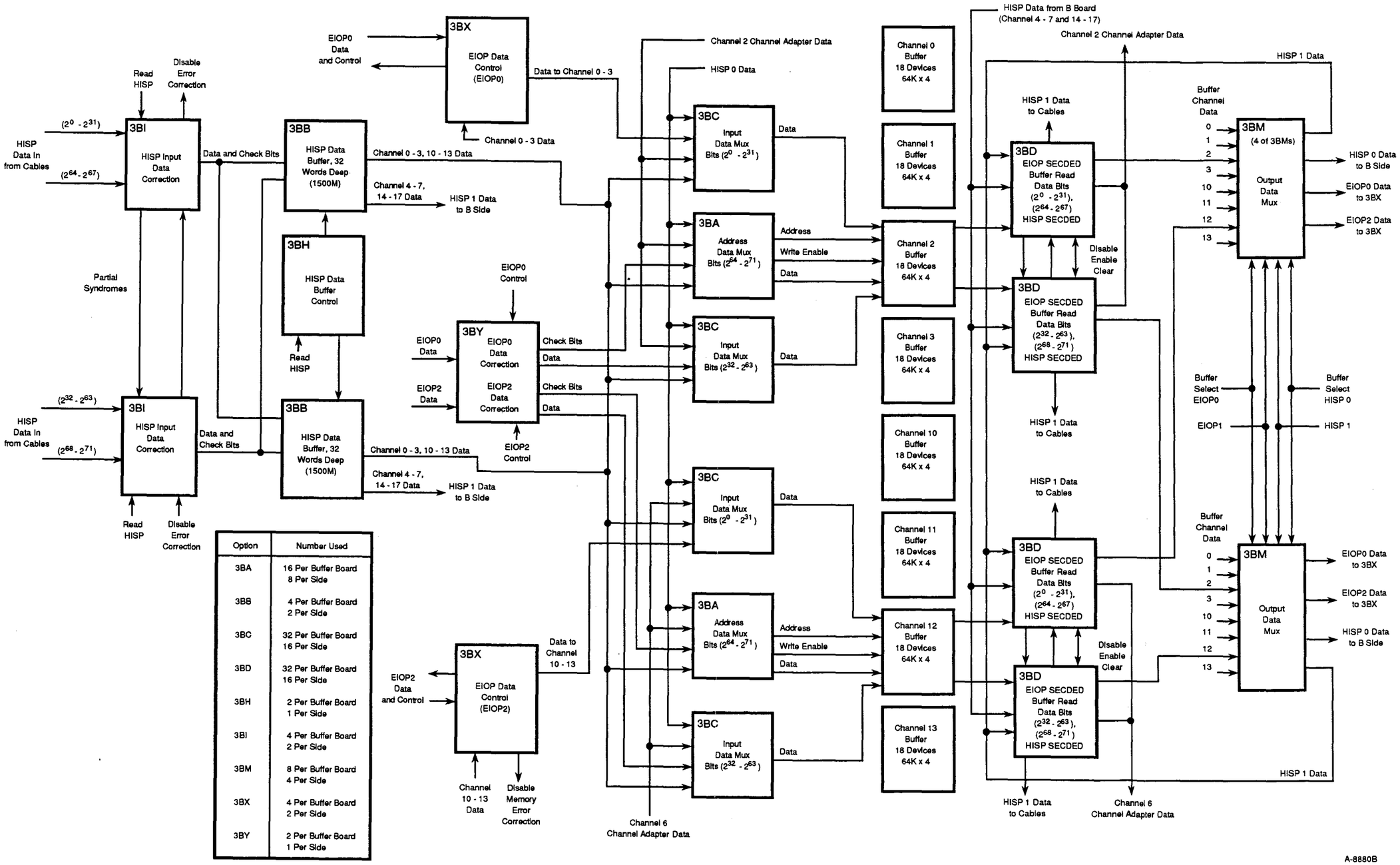
The buffer board generates a sync pulse every 37.5 nanoseconds, or once every 6 clock periods (CPs), which is fanned out to the entire cluster. This sync pulse is used to sync up the data coming to or going from the buffer board. Sync + 0 - 2 is the memory cycle when channel data is written in to or read out of memory and sync + 3 - 5 is when HISP or EIOP data is written in to or read out of memory (refer to Figure 4-2).

Check bits are generated on the EIOP data that comes onto the buffer board and single-error correction, double-error detection (SECDED) is performed on the EIOP data that leaves the buffer board.

HISP data is checked and corrected as it enters the buffer board and checked and corrected as it leaves the buffer board. Channel data has no error correction performed on it while it is on the buffer board.

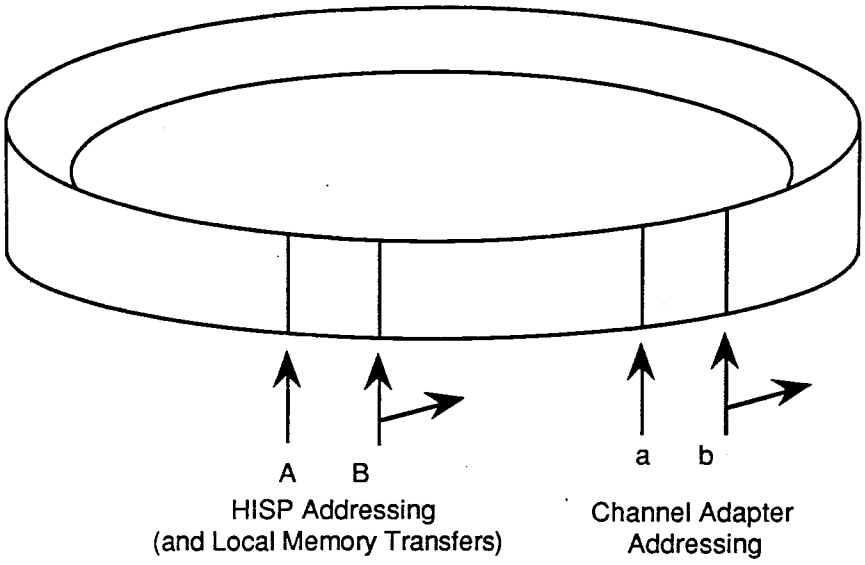
Table 4-1. Buffer Board Option Descriptions

Option	Description
3BA	1. Send check bits for EIOP, HISP, or channel data to memory 2. Load pointer a, b, A, B encode 3. Select EIOP data, onboard or offboard HISP data, or channel data to go to memory 4. Write Enable clock developed 5. Address for read or write sent to memory 6. Read Control sent to the 3BD option 7. HISP write data fanout
3BB	1. 32 bits of HISP data and 4 check bits to the 3BA and 3BC options through fanout 2. Offboard and onboard channel select to the 3BA and 3BC options
3BC	1. 32 bits of data to memory 2. HISP write data fanout
3BD	1. 32 bits of data and 4 check bits from memory to a HISP Channel, an EIOP, or a channel adapter 2. Error correction on the EIOP or HISP data 3. Rebuild and fanout of HISP data that will be leaving the buffer board 4. HISP write data fanout
3BH	1. HISP control for a read or write 2. Priority control for EIOP and HISP data
3BI	1. Receives 32 bits of HISP data and 4 check bits from the HISP MUX 2. SECDED performed 3. Sends 32 data bits and 4 check bits to the 3BB options
3BM	1. Receives EIOP and HISP read data from the 3BD options 2. Fan out HISP data to the 3BD options 3. Fan out EIOP data to the 3BX options 4. Send EIOP and HISP status to the 3BX and 3BD options respectively
3BX	1. Receive EIOP data onto the buffer board and forward it to the 3BC options 2. Control for EIOP data transfers to and from memory 3. Send data from memory back to the EIOP
3BY	1. Receive EIOP data onto the buffer board and forward it to the 3BC options 2. Generate check bits on EIOP data 3. Send check bits to the 3BA options



Option	Number Used
3BA	16 Per Buffer Board 8 Per Side
3BB	4 Per Buffer Board 2 Per Side
3BC	32 Per Buffer Board 16 Per Side
3BD	32 Per Buffer Board 16 Per Side
3BH	2 Per Buffer Board 1 Per Side
3BI	4 Per Buffer Board 2 Per Side
3BM	8 Per Buffer Board 4 Per Side
3BX	4 Per Buffer Board 2 Per Side
3BY	2 Per Buffer Board 1 Per Side

Figure 4-1. I/O Buffer Module (A Board)
(B Board has Data Buffers Channel 4 - 7 and 14 - 17)



1. Buffer size is 65536 words (72 bits).
2. A and B pointers for HISP and local memory transfers.
3. a and b pointers for channel adapter transfers.
4. Pointers can be set to any beginning word address.
5. The maximum transfer size is 65536 words.
6. Channel adapter pointers (a, b) can be both incremented and decremented for support of tape read backwards commands.

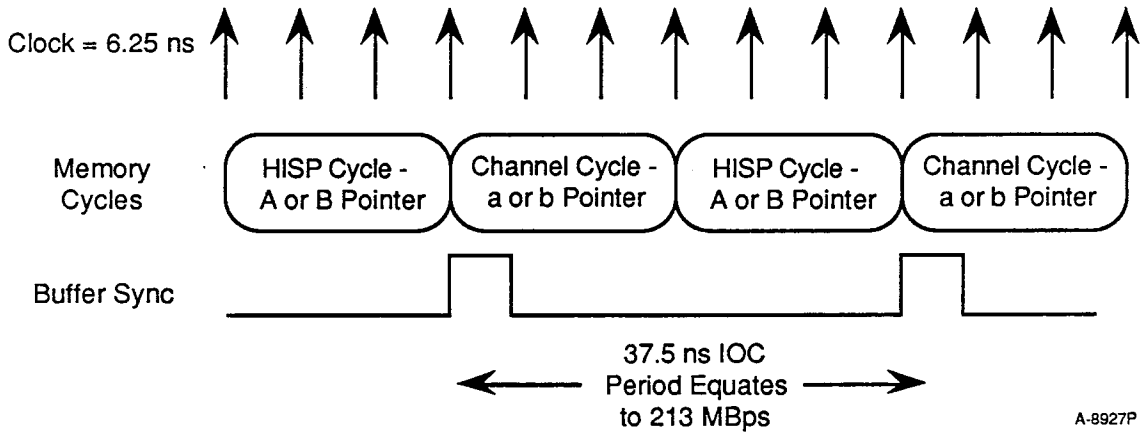


Figure 4-2. I/O Buffer

EIOP Write Data Sequence

The following is the sequence which describes a write from local memory to the buffer board.

1. Issue BOA : 0 with the accumulator equal to a 1, the mode bits are not used.

   A. I0 - 3, function bits, and I5, go function come to the 3BX. The next transfer sends the lower accumulator bits, which causes channel 27 to receive the clear channel. The ready counter and the reference signals are cleared.

   B. R33, input clear channel, goes to the 3BY as I7 and clears the ready counter and check bits.

2. Issue BOA : 16 with the accumulator set to zero. The mode bits are not used.

   A. This function loads the upper bits of the buffer address, which are not used, or it enables the writing of alternate check bits (refer to Figure 4-4).

3. Issue BOA : 17 with accumulator set to the starting address and the mode bits set for the correct pointer and buffer (refer to Figure 4-5).

   A. The modifier bits come on the first transfer.

      1) M0 - 1 make (R14 - 15) Load Pointer a, b, A, B Encode, which is sent to all the 3BA options controlled by the EIOP.

      2) M2 - 3 are decoded to make one of the four terms, (R10 - 13) Go Channel N+x Load Pointer (refer to Figure 4-5). This R term then gates R14 - 15 onto the correct 3BA option.

   B. The function bits are the next transfer and are used to gate the channel decode bits into R10 - 13.

   C. The accumulator bits come next in four 4-bit transfers. Each 4-bit transfer is sent off the 3BX as R16 - 19 to all four of the 3BA options and R10 - 13 gates the bits onto the correct 3BA option.

4. Issue the commands to load the starting local memory address (LMA) and the starting parcel count.

5. Issue BOA : 1 with the accumulator set to a 1 and the modifier bits set for the correct pointer and buffer (refer to Figure 4-5).

A. The modifier bits are sent first.

1. M2 - 3 are decoded to pick one of four buffers, (refer to Figure 4-5) and make one of four R terms, R20 - 23. Data will be presented to all of the 3BC and 3BA options, and one of these R terms will gate the data onto the correct options for the correct channel.

   R20 - 23 make I60 on the 3BA options, and based on what sync time they arrive will mean different things. I60 at sync + 5 means an EIOP reference, at sync + 4 means B select, and at sync + 5 with term H00 set to a one means read memory.

   One of the R terms, based on the decode, will be sent to the 3BH option. The 3BH option will use this term to check for HISP and EIOP conflicts. If there is a conflict, the 3BH option will send an Abort signal back to the 3BX option which will stop the EIOP reference.

2. M0 - 1 are decoded to determine which pointer will be used for the transfer.

B. The function bits, followed by the accumulator bits are used to determine the direction of the transfer. For this transfer, bit 0 of the accumulator is set to a one to indicate a transfer on channel 27.

C. This function starts the transfer.

6. Data transfer

A. Data is sent from the EIOP in parcel format and is stored on the buffer board in word format.

B. Each parcel is sent in four 4-bit transfers, with a Ready coming with each parcel. The data comes onto the 3BX and 3BY options at the same time. The 3BX option forwards the lower 32 bits and the 3BY forwards the upper 32 bits. The 3BY option also generates check bits and sends them on.

   The ready counters on each of these options keep track of which parcel is being transferred. Parcels 2 and 3 are held on the 3BX and forwarded while parcels 0 and 1 are held on the 3BY and forwarded. All four parcels of data are used on the 3BY to generate the check bits.

C. Data leaves the 3BX option as R24 - 27 and is sent to all of the even 3BC options controlled by the EIOP. Whichever R term from R20 - 23 that was generated from the decode of the modifier bits latches this data onto the correct 3BC option.

D. Data leaves the 3BY option as R0 - 3 and is sent to all the odd 3BC options controlled by the EIOP. The same R term from R20 - 23 that latched data on the even 3BC latches data on the odd 3BC.

E. Data enters the 3BC option as I0 - 3. Each 4-bit transfer is latched into a 32-bit buffer by a timing chain started by one of the R terms R20 - 23. Data is loaded into R0 - 31 to be presented to the memory chips at sync + 3 - 5.

F. Check bits leave the 3BY option as R4 - 5 and are sent to all of the 3BA options controlled by the EIOP. The same R term as above latches the check bits on the correct 3BA option.

G. Check bits enter the 3BA option as I0 - 1 and are loaded into B terms by a signal made from one of the R terms R20 - 23. These check bits are loaded into R0 - 7 and are sent to memory at the same time as the data word from above.

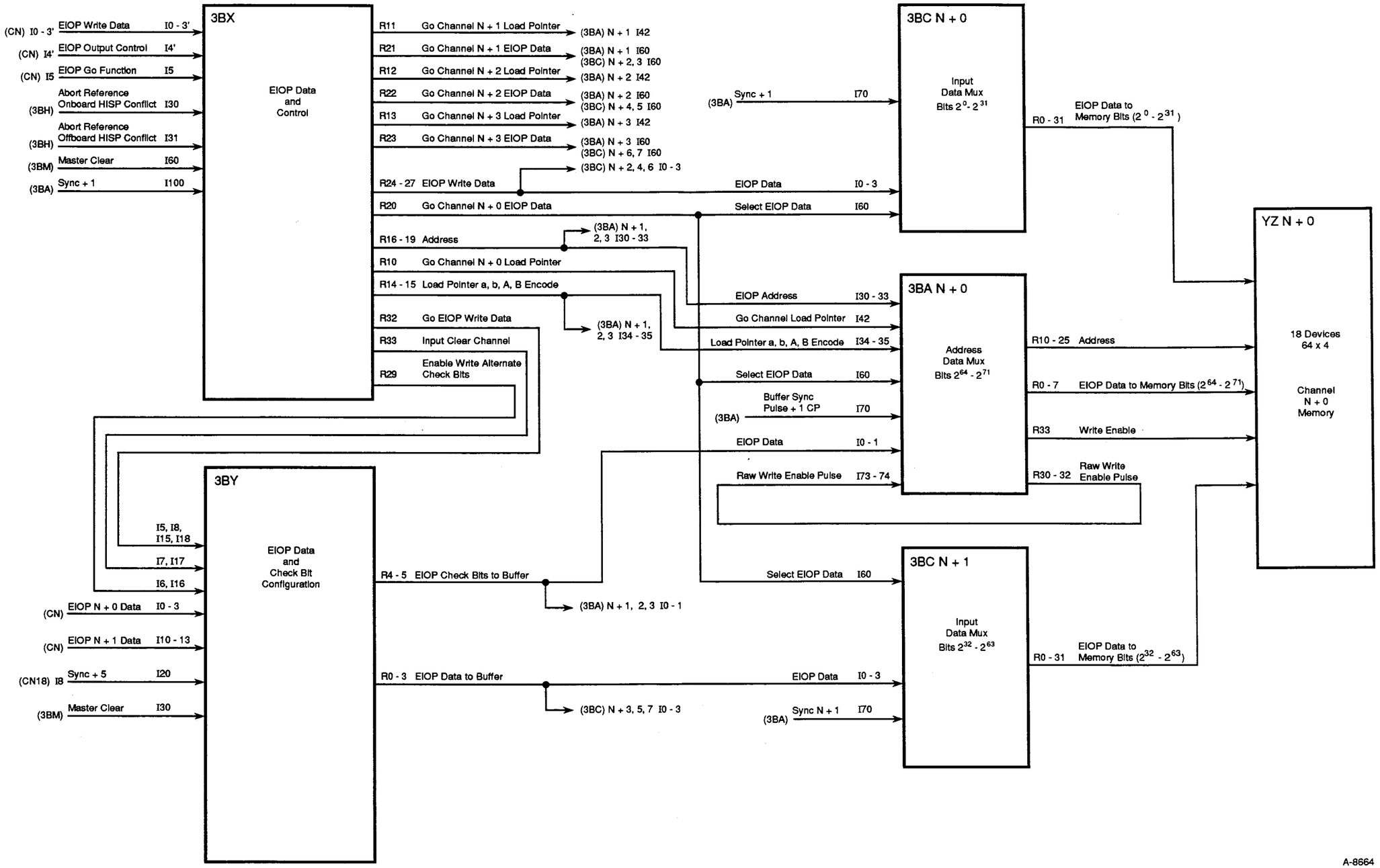


Figure 4-3. IOS Model E EIOP Write to Memory

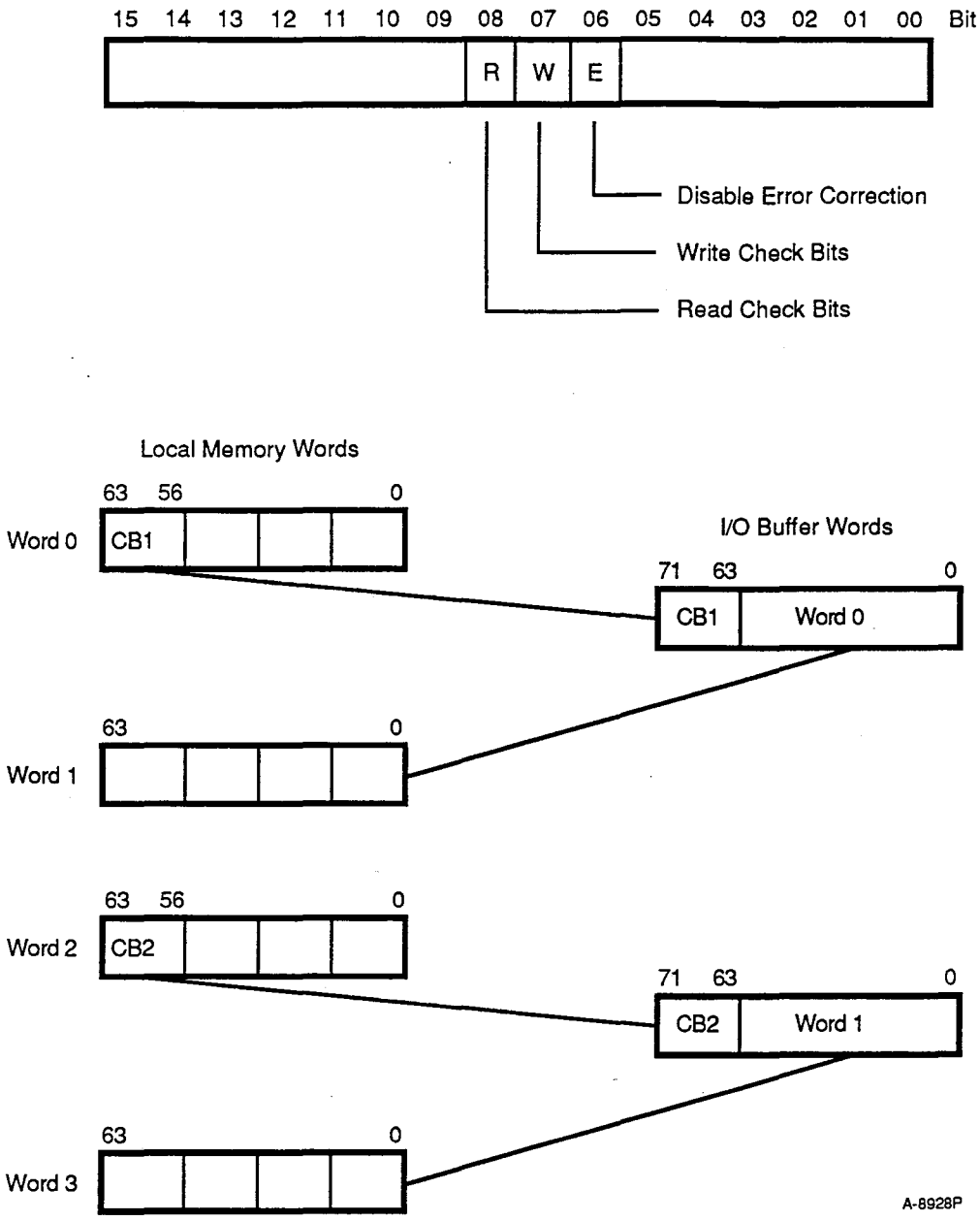
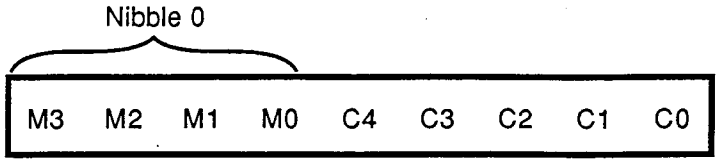


Figure 4-4. I/O Buffer Write Check Bits Diagnostic Mode

B Register or D field

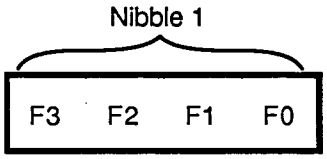


C0 - C4 = Channel number
M0 - M3 = Function modifier as needed or a and b selects

M3	M2	I/O Buffer Channel Selection
0	0	Buffer 0
0	1	Buffer 1
1	0	Buffer 2
1	1	Buffer 3

M1	M0	I/O Buffer Pointer Selection
0	0	a
0	1	b
1	0	A
1	1	B

Function Code



F0 - F3 = Function code (example: the 17 in BIA: 17 comes from instruction 157 or 177)

Accumulator

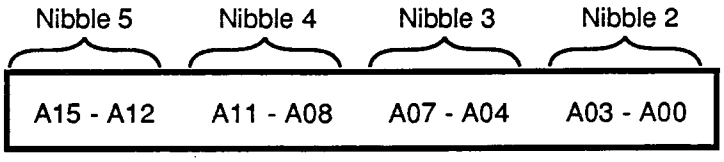


Figure 4-5. Accumulator and Modifier Bits

EIOP Read Data Sequence

This sequence used with Figure 4-6 describes a read from the buffer board to local memory of an EIOP.

1. Issue BIA: 0 with the accumulator equal to a 0. The mode bits are not used.

   A. I0 - 3, function bits, and I4, Go Function, come to the 3BX. The next transfer sends the lower accumulator bits, which when set to a zero, cause channel 26 to receive the clear channel.

      This function clears the channel 26 Ready Counter and the channel 26 Input Acknowledge. The Input Acknowledge signal is used to increment the ready counter bits.

      This function also makes Read EIOP SECDED status (R34), which causes the error information held on the 3BMs to be read out. The information read out is not used, but each time the data is read out, the terms that hold the data are cleared.

2. Issue BIA: 16 enter upper address bits and mode bits. The accumulator will be set to zero for this instruction.

   The lower six bits of the accumulator are used as upper buffer address bits in this instruction, but these bits are not used at this time. Mode bits will be explained later.

3. Issue BIA: 17 enter lower buffer pointer address. The mode bits are set for the correct pointer and buffer, (refer to Figure 4-5), and the accumulator is set for the starting channel buffer address.

   A. The modifier bits come on the first 4-bit transfer.

      1) M0 - 1 makes Load Pointer a, b, A, B Encode (R14 - 15) on the 3BX option, which is sent to all of the 3BA options controlled by the EIOP.

      2) M2 - 3 are decoded to make one of the four terms (R10 - 13) Go Channel N + x Load Pointer. Refer to Figure 4-5. This R term then gates R14 - 15 onto the correct 3BA option.

   B. The function bits are the next transfer and are used to gate the channel decode bits into R10 - 13.

   C. The accumulator bits come next in four 4-bit transfers. Each 4-bit transfer is sent off the 3BX as R16 - 19 to all four of the 3BA options, and R10 - 13 gates the bits onto the correct 3BA option.

4. Issue the commands to load the starting local memory address (LMA) and the starting parcel count.

5. Issue BOA: 1 with the accumulator set to a 0 and the modifier bits set for the correct pointer and buffer. Refer to Figure 4-5.

   A. The modifier bits are sent first.

      1) M2 - 3 are decoded to pick one of four buffers, (refer to Figure 4-5) and make one of four R terms, R20 - 23. These terms, R20 -23, make I60 on the 3BA options and based on what sync time they arrive, will determine the type of reference. This is a direction specific instruction because the accumulator set to a zero indicates a transfer from the buffer board to local memory. The R terms will arrive on the 3BA at sync + 5 with term H00 set to a one which indicates a read from the buffer board.

         R20 - 23 will also be sent to the 3BH option to be used to determine if there is a HISP conflict. If there is a conflict with Onboard HISP Data, then I30 Abort Reference Onboard HISP Conflict is received from the 3BH. If there is a conflict with Offboard HISP Data, then I31 Abort Reference Offboard HISP Conflict is received from the 3BH. These signals hold the EIOP reference until the HISP conflict is done.

      2) A decode of M2 - 3 is used to make EIOP Read Channel Encode (R30 - 31) which is sent to the 3BM options. This signal indicates to the 3BM options which 3BD options the data will be arriving from.

      3) M0 -1 are decoded to determine which pointer will be used for the transfer.

   C. This function starts the transfer.

6. Data transfer.

   A. Because I60 is sent at sync + 5 and term H00 = 1, the write enable signal is not generated on the 3BA option. This means that when the address is applied to the memory chips in the channel buffer, data is read out of the memory chips. The data is read from memory at sync + 3 - 5.

   B. EIOP data leaving the buffers arrives on two 3BD options as I0 -31, buffer read data bits N + 0 - N + 31, and I32 - 35, checkbits N + 0 - N + 3, and is latched into these options at sync + 5. Partial syndrome bits are generated on each 3BD option, then leave the option as R20 - 27, and arrive on the other

3BD option as I40 - 47. New syndromes are generated and the word of data is checked and corrected, if possible, and the corrected data leaves the 3BD option as R0 - 5. The first bits leave the 3BD option at sync + 3.

The data bits leave the 3BD options as indicated in Table 4-2.

Table 4-2. EIOP Read Data from the 3BD Options

Sync Time	Bits
sync + 3	Bits N + 5, 11, 17, 23, 29, 67
sync + 4	Bits N + 4, 10, 16, 22, 28, 66
sync + 5	Bits N + 3, 9, 15, 21, 27, 65
sync + 0	Bits N + 2, 8, 14, 20, 26, 64
sync + 1	Bits N + 1, 7, 13, 19, 25, 31
sync + 2	Bits N + 0, 6, 12, 18, 24, 30

This data is sent to the four 3BM options. The EIOP Read Data Fanout chart, Figure 4-3, shows which 3BM option the data arrives at and which I term this data arrives on. The I terms vary based on which channel buffer is being read from. This data that comes from the 3BD options is corrected EIOP data.

C. Data is clocked onto the correct terms on the 3BM option based on the decode of I32 and I33 or I34 and I35. These terms are made from EIOP Read Channel Encode (R30 and R31) from the 3BX options. I32 and I33 comes from 3BX N + 0 and I34 and I35 comes from 3BX N + 1. (Example: I32 and I33 comes from 3BX0 on the A side of the buffer board and from 3BX20 on the B side of the board.)

D. The data is passed directly to R terms on the 3BM options and back to the correct 3BX option. The data is on the 3BM options for less than 1 CP. Table 4-3, EIOP Data A and B Board Fanout from 3BM Option, shows which R terms the data leaves the 3BM options on, which 3BX option the data is sent to, and on which I terms the data arrives at the 3BX option.

E. Twelve bits (I10 - 21) EIOP Read Data arrive on the 3BX option, 3 bits from each of four 3BM options, starting at sync + 4. The entire 72-bit word is buffered on the 3BX options, broken into parcels based on the ready counter, and then broken into 4-bit groups to be sent out (R0 - 3) EIOP Data/Status, back to local memory of the EIOP.

7. Syndrome Data.

A. Each 3BD option generates a partial syndrome on the data bits that arrive on the option. This partial syndrome is sent to the other 3BD option, leaving as R20 - 27 and arriving as I40 - 47. This partial syndrome is used to develop the final syndrome for the bits handled on the option. If a byte error is detected on one of the 3BD options, No On Chip Error Byte Decode (R40) is set to a zero. This makes No Off Chip Error Byte Decode (I60) on the other 3BD option for this channel. This will be sent as R30, Syndrome, to the 3BM option, which will make SECDED Status (R42), which makes I51 on the 3BX option. This will cause the error flag to set and indicate that a data error has occurred.

B. Syndrome information developed on the 3BD option leaves that option as Syndrome (R30), and is sent to the 3BM options. The information below shows which 3BM options receive the information 3BM0 and 3BM1 handles syndrome data for channel buffers 0 - 3 and 3BM2 and 3 handles syndrome information for channel buffers 10 - 13, on the A side of the buffer board. 3BM20 and 21 handle syndrome data for channel buffers 4 - 7 and 3BM22 and 23 handle syndrome data for channel buffers 14 - 17 on the B side of the buffer board.

3BM0	3BM1	3BM2	3BM3
I40 from 3BD0	I40 from 3BD1	I40 from 3BD8	I40 from 3BD9
I41 from 3BD2	I41 from 3BD3	I41 from 3BD10	I41 from 3BD11
I42 from 3BD4	I42 from 3BD5	I42 from 3BD12	I42 from 3BD13
I43 from 3BD6	I43 from 3BD7	I43 from 3BD15*	I43 from 3BD14*

3BM20	3BM21	3BM22	3BM23
I40 from 3BD20	I40 from 3BD21	I40 from 3BD28	I40 from 3BD29
I41 from 3BD22	I41 from 3BD23	I41 from 3BD30	I41 from 3BD31
I42 from 3BD24	I42 from 3BD25	I42 from 3BD32	I42 from 3BD33
I43 from 3BD26	I43 from 3BD27	I43 from 3BD35*	I43 from 3BD34*

NOTE: *This is different from the order in the rest of the chart.

C. The error information is held on the 3BM options until a command 12 is issued to read it back to the EIOP. The error will cause the busy flag to stay set which will indicate the need to read this information. The programmer will be responsible to have code that will check for this condition.

A command 12, Read SECDED Status, causes Read EIOP SECDED Status (R34) to be sent to I81 of the 3BM. This starts a timing chain that reads the data into terms that feed SECDED Status.(R41 - 42) These terms from 3BM0 make I50 - 51, and from 3BM1 make EIOP Read Syndrome Data (I52 - 53) on 3BX0. These same I terms from 3BM2 and 3 would make I50 - 53 on 3BX1.

I81 on the 3BM made from R34 also makes Read EIOP Status In Progress (R43), which makes I54, called the same thing, on the 3BX. This starts a timing chain that latches I50 - 53 onto the 3BX option.

D. A single-bit error will be held over a double-bit error and it will overwrite a double-bit error that is being held on the 3BM options. The error will be the first error that occurred. Once a single-bit error is in the 3BM option, it will be held until it is written to the 3BX options.

8. Disabling Error Correction.

A. If a command 16 is issued with bit 2^6 set, error correction will be disabled. This will cause Enable Error Correction (R28) to be set to a zero. This signal is fanned out through the 3BA N + 0 and 1 options for this EIOP, and sent to the 3BD options as I37, Enable Error Correction. With this term a zero, the checkbits are not loaded into terms on the 3BD option which would be used to correct the data.

B. This command will also prevent the correction of HISP data on the 3BD option, so the command must be cleared after it is used. This can be done with a Master Clear or by issuing another command 16 with bit 2^6 set to a zero.

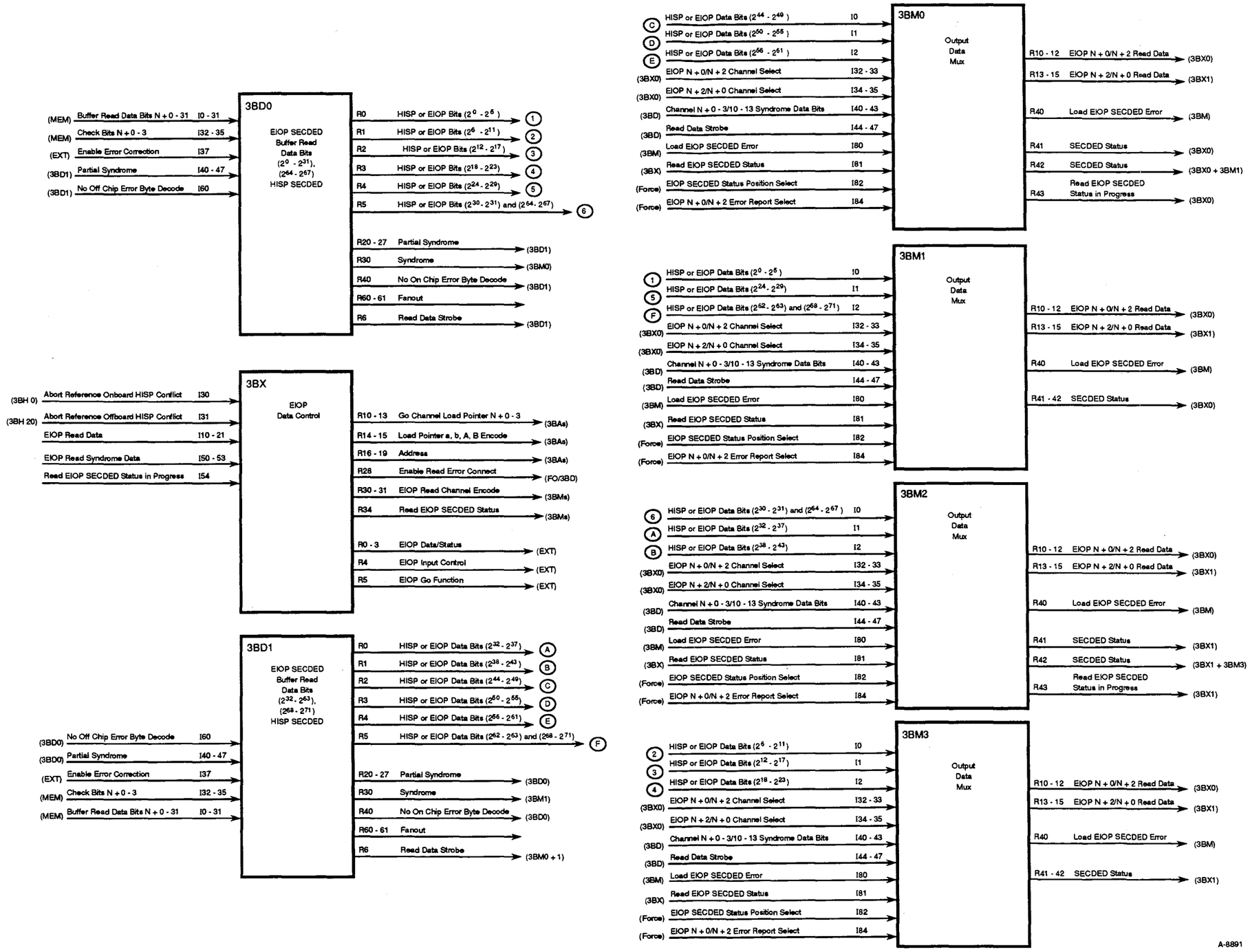


Figure 4-6. EIOP Output from Channel 0

EIOP Read Data Fanout

EIOP data fanout from the 3BD options to the 3BM options

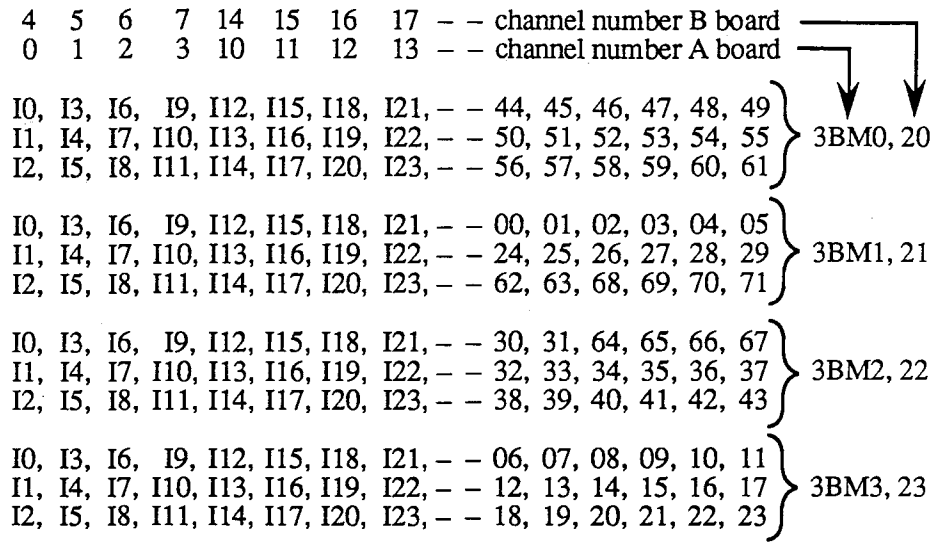


Table 4-3. EIOP Data A and B Board Fanout from 3BM Option

	EIOP Data A Board						EIOP Data B Board				
	Term	To	Option	Term	Bits		Term	To	Option	Term	Bits
3BM0	R10	to	3BX0	I18	44 - 49	3BM20	R10	to	3BX20	I18	44 - 49
	R11	to	3BX0	I19	50 - 55		R11	to	3BX20	I19	50 - 55
	R12	to	3BX0	I20	56 - 61		R12	to	3BX20	I20	56 - 61
	R13	to	3BX1	I18	44 - 49		R13	to	3BX21	I18	44 - 49
	R14	to	3BX1	I19	50 - 55		R14	to	3BX21	I19	50 - 55
	R15	to	3BX1	I20	56 - 61		R15	to	3BX21	I20	56 - 61
3BM1	R10	to	3BX0	I10	00 - 05	3BM21	R10	to	3BX20	I10	00 - 05
	R11	to	3BX0	I14	24 - 29		R11	to	3BX20	I14	24 - 29
	R12	to	3BX0	I21	62, 63, 68 - 71		R12	to	3BX20	I21	62, 63, 68 - 71
	R13	to	3BX1	I10	00 - 05		R13	to	3BX21	I10	00 - 05
	R14	to	3BX1	I14	24 - 29		R14	to	3BX21	I14	24 - 29
	R15	to	3BX1	I21	62, 63, 68 -71		R15	to	3BX21	I21	62, 63, 68 - 71
3BM2	R10	to	3BX0	I15	30, 31, 64 - 67	3BM22	R10	to	3BX20	I15	30, 31, 64 - 67
	R11	to	3BX0	I16	32 - 37		R11	to	3BX20	I16	32 - 37
	R12	to	3BX0	I17	38 - 43		R12	to	3BX20	I17	38 - 43
	R13	to	3BX1	I15	30, 31, 64 - 67		R13	to	3BX21	I15	30, 31, 64 - 67
	R14	to	3BX1	I16	32 - 37		R14	to	3BX21	I16	32 - 37
	R15	to	3BX1	I17	38 - 43		R15	to	3BX21	I17	38 - 43
3BM3	R10	to	3BX0	I11	06 - 11	3BM23	R10	to	3BX20	I11	06 - 11
	R11	to	3BX0	I12	12 - 17		R11	to	3BX20	I12	12 - 17
	R12	to	3BX0	I13	18 - 23		R12	to	3BX20	I13	18 - 23
	R13	to	3BX1	I11	06 - 11		R13	to	3BX21	I11	06 - 11
	R14	to	3BX1	I12	12 - 17		R14	to	3BX21	I12	12 - 17
	R15	to	3BX1	I13	18 - 23		R15	to	3BX21	I13	18 - 23

Channel Adapter Write Sequence

This sequence, used with Figure 4-7, describes a write to the buffer board from the channel adapter. The only programming commands that will be covered will be those that affect the buffer board. The commands for the channel adapters are covered in the channel adapter sections.

1. BOA:16 or BIA:16 Commands. A command 16 on channel 26 or 27 is issued with the accumulator equal to a zero. The modifier bits are not used. Either channel may be used because direction of data flow does not need to be indicated.

   EIOP Write Data. EIOP Write Data is the function bits and the accumulator bits coming from the EIOP.

   3BX - This function uses the lower six bits of the accumulator as the upper buffer address and bits 2^6, 2^7, and 2^8 to set or clear certain maintenance modes. Refer to Figure 4-4. The function code and the accumulator bits come to the 3BX option in 4-bit transfers on EIOP Write Data (I0 - 3).

2. BOA:17 or BIA:17 Commands. A command 17 on channels 26 or 27 is issued with the accumulator set to the starting channel buffer address and the modifier bits set for the correct pointer and buffer. Refer to Figure 4-5.

   EIOP Write Data. EIOP Write Data is the modifier bits, the function bits, and the buffer channel address bits coming from the EIOP. This data comes in 4-bit transfers to I0 - 3.

   3BX - The first 4-bit transfer is the modifier bits. M0 - 1 makes Load Pointer a, b, A, B, Encode (R14 - 15) which is sent to all four of the 3BA options controlled by the EIOP.

   M2 - 3 are decoded to make one of the four terms Go Channel N + x Load Pointer (R10 - 13) on the 3BX option. In Figure 4-7, Go Channel N+1 Load Pointer (R11) is made.

   The function bits are the next transfer and are used to gate the channel decode bits into R10 -13.

   The accumulator bits come in the next four, 4-bit transfers. This is the buffer channel address and is sent in four, 4-bit transfers to the inputs of all four 3BA options.

   3BA - All four 3BA options controlled by the EIOP receive Load Pointer a, b, A, B, Encode (I34 - 35) from the 3BX option. Only 3BA1 will receive Go Channel Load Pointer

(I42) from the 3BX option, which will latch I34 -35 on this 3BA option only.

The 3BX option sends the buffer channel address, R16 -19 to all of the 3BA options controlled by the EIOP. In our example, I42 latches the address onto 3BA1 only. The address arrives on the 3BA options as I30 -33.

At this point, all of the control information needed from the EIOP has been received. The control of the transfer of data from this point on is with the channel adapter.

3. Select Channel Data (Go a or b) . These are the control signals from the channel adapter that will set the pointers in the correct read/write mode and increment the buffer channel address.

   3BA - The channel adapter sends either Select Channel Data (Go a or b) (I61 or I62) to the 3BA option at sync + 2 to set the pointers in the correct mode. The information below shows how the mode is set for each term. The hardware allows either pointer to be used for a write to memory.

	Go a I61	Go b I62	
Sync +	2		Mode "a" read or "b" write
Sync +		2	Mode "a" write or "b" read

   These signals are only sent once at the beginning of the transfer.

   At sync + 3, I61 or I62 must be sent with the word of data, depending on which pointer is to be used, to write the word and increment the correct pointer. The example below demonstrates this.

   Figure 4-7 shows a channel adapter writing to channel buffer 1 of an EIOP. If the "a" pointer is going to be used, Go b (I62) would have been sent at sync + 2 to put the "a" pointer in the write mode. Go a (I61) would be sent at sync + 3 with each word to load the word onto the buffer board and increment the pointer address.

   In the case of a write from a tape that is in read backward mode, I61 would also be sent at sync + 4 to decrement the channel buffer address.

5. Write Enable. This signal is sent to the memory chips to allow the data to be written to memory.

3BA - When the Go a is sent at sync + 3, the 3BA options begin to generate the raw write pulses (R30 and R32) that are sent back to I74 and I73, respectively, on the same 3BA option. These signals then form the Write Enable (R33) that is sent to memory with the address and data.

6. Address. Address is the 16 address bits that are sent to memory with each word of data.

   3BA - This option receives the initial channel buffer address from the 3BX option and sends the address to memory at sync + 0 - 2 with each word of data. The address register on the 3BA option is incremented or decremented by the Go a or b signals as explained above.

7. Data. Data is the 72-bit word of data that is sent from the channel adapter to the buffer board. No error correction is done to this word of data on the buffer board.

   3BA - The check bits (I10 - 17) are received from the channel adapter all at once. The channel adapter sends the data in six 12-bit transfers, and the check bits come as a part of the sixth transfer. Refer to Table 4-4. Data (R0 - 7) are the check bits going to memory at sync + 0 - 2.

   3BC - Channel Data (I10 - 15) is the data coming to the two 3BC options from the channel adapter. The 12-bit transfer is split between the two options. The even 3BC option handles the lower 32 bits of the data word, and the odd 3BC option handles the upper 32 bits. The data arrives on the 3BC options as shown in Table 4-4. Data (R0 - 31) is the data leaving the 3BC options for memory at sync + 0 - 2.

Table 4-4. Channel Adapter Data

Sync Time	Even 3BC Option	Odd 3BC Option	3BA Option
0	Bits 2^{26} - 2^{31}	Bits 2^{58} - 2^{63}	None
1	Bits 2^{20} - 2^{25}	Bits 2^{52} - 2^{57}	None
2	Bits 2^{14} - 2^{19}	Bits 2^{46} - 2^{51}	None
3	Bits 2^{8} - 2^{13}	Bits 2^{40} - 2^{45}	None
4	Bits 2^{2} - 2^{7}	Bits 2^{34} - 2^{39}	None
5	Bits 2^{0} - 2^{1}	Bits 2^{32} - 2^{33}	Bits 2^{64} - 2^{71}

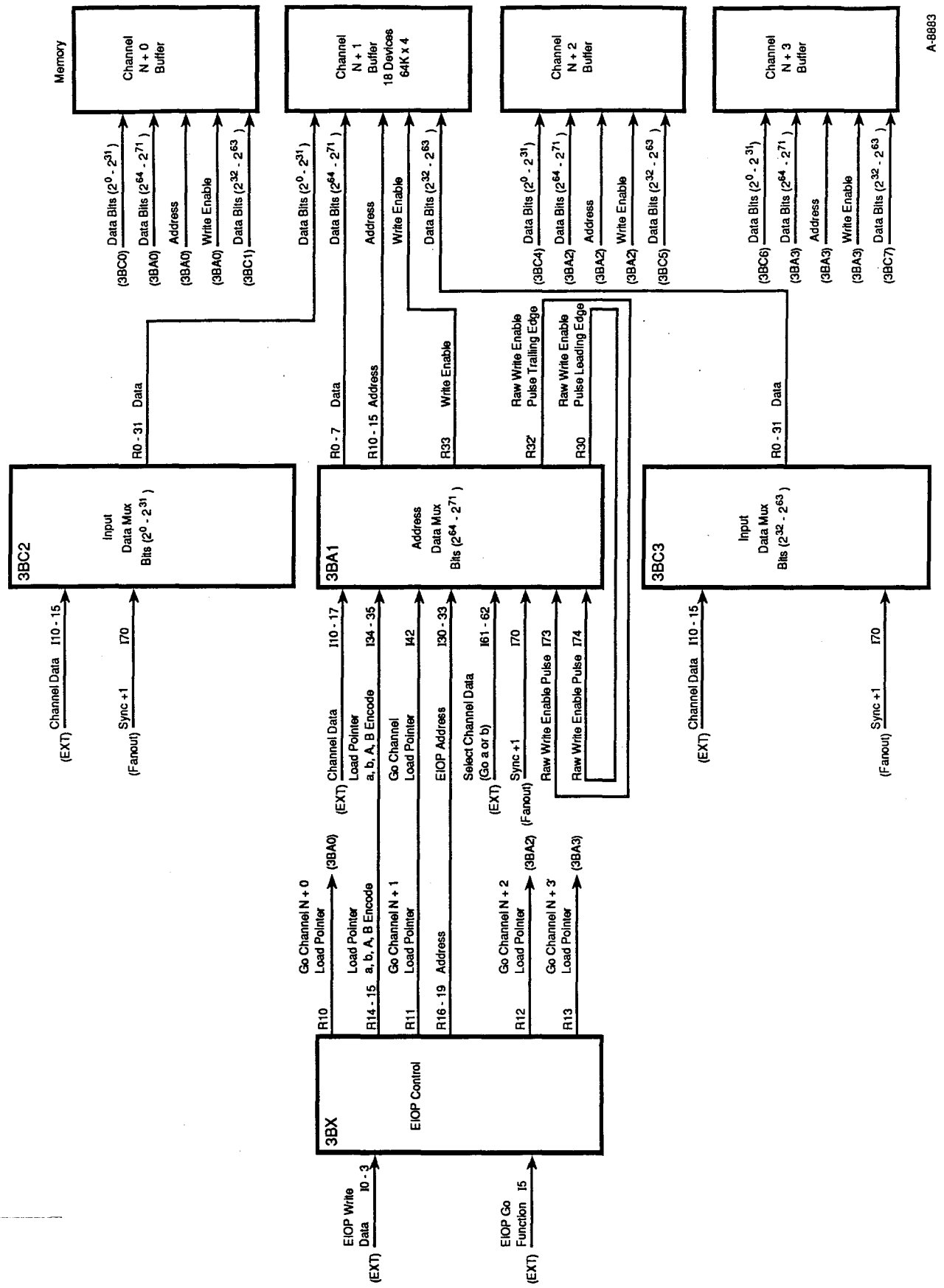


Figure 4-7. Channel Data Input

Channel Adapter Read Sequence

This sequence, shown in Figure 4-8, describes a read from the buffer board to a channel adapter. The only programming commands that will be covered will be those that affect the buffer board. The commands for the channel adapters are covered in the channel adapter sections.

1. BOA:16 or BIA:16 Commands. A command 16 on channel 26 or 27 is issued with the accumulator equal to a zero. The modifier bits are not used. Either channel may be used because direction of data flow does not need to be indicated.

   EIOP Write Data. EIOP Write Data is the function bits and the accumulator bits coming from from the EIOP.

   3BX - This function uses the lower 6 bits of the accumulator as the upper buffer address and bits 2^6, 2^7, and 2^8 to set or clear certain maintenance modes. Refer to Figure 4-4. The function code and the accumulator bits come to the 3BX option in 4-bit transfers on EIOP Write Data (I0 - 3).

2. BOA:17 or BIA:17 Commands. A command 17 on channels 26 or 27 is issued with the accumulator set to the starting channel buffer address and the modifier bits set for the correct pointer and buffer. Refer to Figure 4-5.

   EIOP Write Data. The EIOP Write Data is the modifier bits, the function bits, and the buffer channel address bits coming from the EIOP. This data comes in 4-bit transfers to I0 - 3.

   3BX - The first 4-bit transfer is the modifier bits. M0 - 1 makes Load Pointer a, b, A, B, Encode (R14 - 15) which is sent to all four of the 3BA options controlled by the EIOP.

   M2 - 3 are decoded to make one of the four terms Go Channel N + x Load Pointer (R10 - 13) on the 3BX option. In Figure 4-8, Go Channel N + 1 Load Pointer (R11) is made.

   The function bits are the next transfer and are used to gate the channel decode bits into R10 -13. The address leaves the 3BX option as R16 - 19.

   The accumulator bits come in the next four, 4-bit transfers. This is the buffer channel address and is sent in four 4-bit transfers to the inputs of all four 3BA options.

3BA - All four 3BA options controlled by the EIOP receive Load Pointer a, b, A, B, Encode (I34 - 35) from the 3BX option. Only 3BA1 will receive Go Channel Load Pointer (I42) from the 3BX option, which will latch I34 -35 on this 3BA option only.

The 3BX option sends the buffer channel address to all 3BA options controlled by the EIOP. In Figure 4-8, I42 latches the address on to 3BA1 only. The address arrives on the 3BA options as I30 -33.

At this point all of the control information needed from the EIOP has been received. From this point on, the channel adapter controls the transfer of data.

3. Select Channel Data (Go a or b). These are the control signals from the channel adapter that will set the pointers in the correct read/write mode and increment the buffer channel address.

   3BA - The channel adapter sends either I61 or I62, Select Channel Data (Go a or b), to the 3BA option at sync+2 to set the pointers in the correct mode. The information below shows how the mode is set for each term. The hardware allows either pointer to be used for a read from memory.

	Go a I61	Go b I62	
Sync +	2		Mode "a" read or "b" write
Sync +		2	Mode "a" write or "b" read

   These signals are only sent once at the beginning of the transfer.

   At sync + 3, I61 or I62 must be sent, depending on which pointer is to be used, to read the word from memory and to increment the address. The example below demonstrates this.

   Figure 4-8 shows a channel adapter reading from channel buffer 1 of an EIOP. If the "b" pointer is going to be used, Go b (I62) would have been sent at sync + 2 to put the "b" pointer in the read mode. Go b, (I62) would be sent at sync + 3 with each word to read the word from memory and increment the pointer address.

4. Address. Address is the 16 address bits that are sent to memory with each word of data.

3BA - This option receives the initial channel buffer address from the 3BX option and sends the address to memory at sync + 0 - 2 to read a word of data from memory. The address register on the 3BA option is incremented by the Go a or Go b signals as explained above.

5. Data. Data is the 72-bit word of data that is sent from the buffer board to the channel adapter. No error correction is done to this word of data on the buffer board.

3BD - The 72-bit word leaves memory and is latched onto two 3BD options at sync + 2. The even 3BD option receives data bits 2^0 - 2^{31} and check bits 2^{64} - 2^{67}, and the odd 3BD option receives data bits 2^{32} - 2^{63} and check bits 2^{68} - 2^{71}. The data arrives as I0 - 31 and the check bits arrive as I32 - 35. This data passes through the 3BD options and is sent in 12-bit transfers (6 bits from each option) to the channel adapter. Data leaves the 3BD option as shown in Table 4-5.

Table 4-5. Channel Adapter Data Leaving the 3BD Option

Sync Time	Even 3BD Option	Odd 3BD Option
4	Bits 2^{26} - 2^{31}	Bits 2^{58} - 2^{63}
5	Bits 2^{20} - 2^{25}	Bits 2^{52} - 2^{57}
0	Bits 2^{14} - 2^{19}	Bits 2^{46} - 2^{51}
1	Bits 2^{8} - 2^{13}	Bits 2^{40} - 2^{45}
2	Bits 2^{2} - 2^{7}	Bits 2^{34} - 2^{39}
3	Bits 2^{64} - 2^{67}, 2^{0}, 2^{1}	Bits 2^{68} - 2^{71}, 2^{32}, 2^{33}

Channel adapter data leaves the 3BD options as R10 - 15.

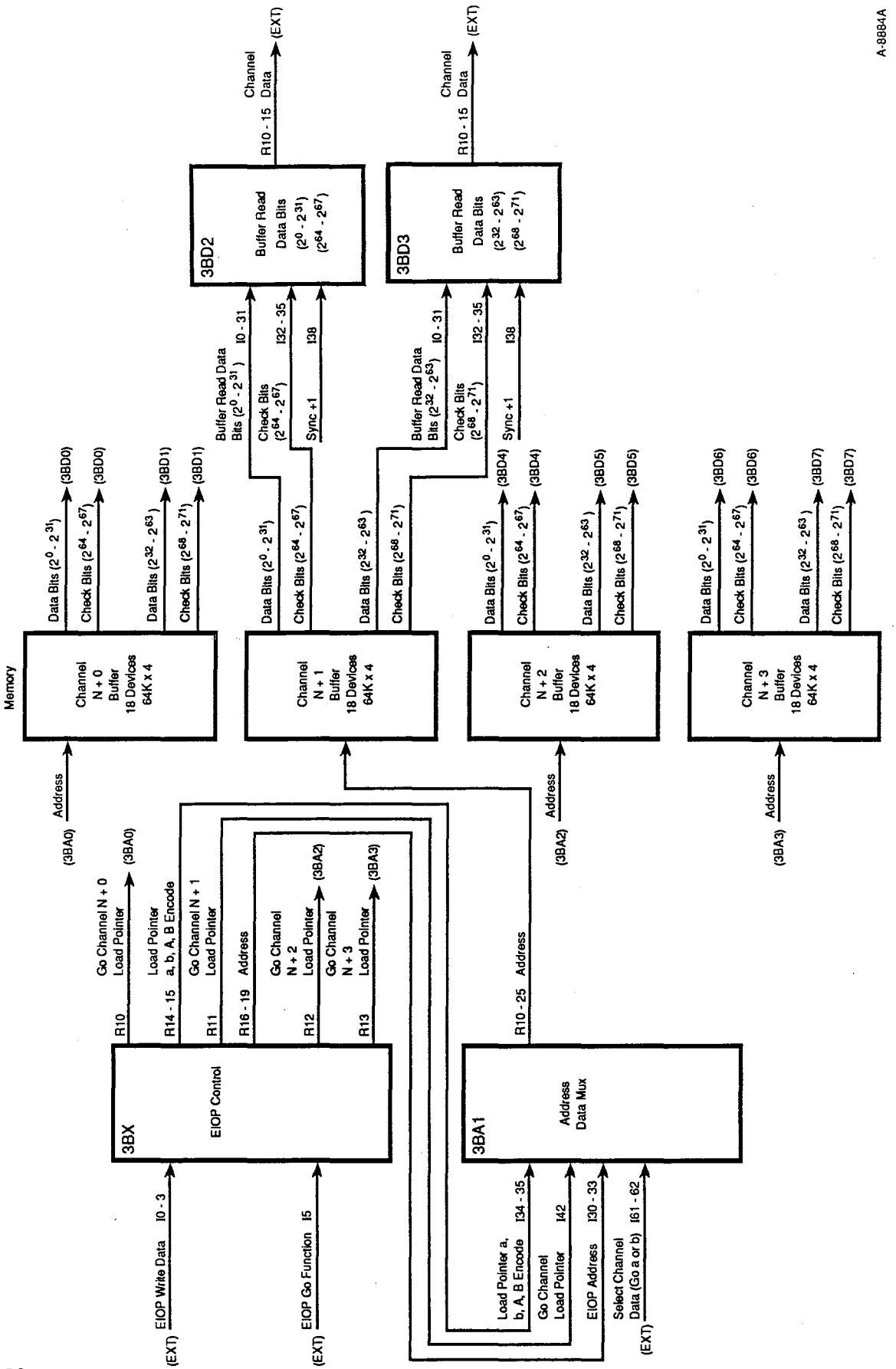


Figure 4-8. Channel Data Output

High-speed Write Data Sequence

This sequence, shown in Figure 4-9, describes a write to the buffer board from one of the HISP channels. The numbers in the options are for the A side of the buffer board.

The EIOP must program the starting address and buffer pointer for the channel buffer that is going to be used. That sequence is described in the channel adapter write sequence that is just before Figure 4-7. Items 1 and 2 of that sequence describe the commands that need to be issued. The EIOP that is used to set up the channel buffer must be the one that controls that channel buffer.

1. Clear Buffer and Parameter Select. These signals are received on the buffer board from the HCM and are used to clear the buffer board, to select the correct pointer, and to select the correct buffer.

   3BH - HISP Input Clear Channel (I11) is received and clears the channel buffer bits, the Select A or B, the Sample HISP Data Input Read and Write Buffer Addresses, and the Error Information on the 3BH option. The 3BH option sends Clear Channel (R18) to the 3BB options.

   HISP Input Parameters (I13) is the buffer channel number and the pointer A or B Select. The first 4 bits that are received are the channel number starting with the least significant bit. Four bits are needed to select one of the 16 channel buffers. The fifth bit to be transferred is the A or B Select. This data is stored on the 3BH option and passed on to the 3BB options.

   3BB - The 3BH option sends Clear Channel (R18) to the 3BB options. HISP Input Clear Channel (I30) is received on the 3BB options and clears the Channel Buffer bits and the B Select.

   HISP Input Parameter (R19) from the 3BH option, is sent to the HISP Input Channel Parameter (I31) on the 3BB options. This loads the 4 bits that are the channel number and the B Select bit onto the 3BB options.

2. Parameter Select. The Parameter Select is sent from the HCM each time that a word of HISP data is sent to the buffer board.

   3BH - HISP Input Parameters (I12) starts a 9 CP HISP Input Sample Data timing chain that is used to load syndrome codes onto the 3BH option, load the read or write buffer address into R20 - 24, make Write Buffer (R17), going to the 3BB options, increment the write and read buffer

address, and make Buffer Readout Read Ahead (R25) when it is needed. Sample HISP Data (R15) is also made from I12 and is sent to the 3BI options.

3. Sample HISP Data. Sample HISP Data is sent from the 3BH option to the 3BI options each time a word of incoming HISP data is received.

   3BH - Sample HISP Data (R15) is made from HISP Input Parameters (I12) and is sent to the I72 of the 3BI option.

   3BI - Read HISP (I72) is received from the 3BH option and latches the incoming word of data into the 3BI options. Before being latched to the options, this data passes through differential amplifiers. I0 - 63 are the 32 bits of data coming onto each 3BI option, and I64 - 71 are the 4 check bits that come to each of these options.

4. HISP Data Input Bits. These are the data bits coming to the buffer board from the HISP cables and can be either CPU or SSD data.

   3BI - HISP Data Input Bits (I0 - 63) are the data bits coming from the HISP drop cables. Thirty-two bits come to each of the 3BI options and pass through differential amplifiers before being latched onto the option. I64 - 71 are the 4 check bits coming to each 3BI option. The check bits also pass through differential amplifiers.

5. Enable Error Correct. The Enable Error Correct signal is sent to the 3BI option to allow error correction to be done on the incoming HISP data word.

   3BH - The 3BH option sends Enable Error Correction (R26) to the 3BI option. A command 17, HIA:17, with the accumulator equal to a seven, will stop this signal.

   3BI - If the 3BI options receive an Enable Error Correction (I84) from the 3BH option, SECDED is performed on the incoming word of HISP Data. Each 3BI option generates partial syndrome on the 32 data bits it receives and sends this partial syndrome to the other 3BI option. Eight bits are generated and sent off the option. The two 4-bit transfers leave the 3BI options as Partial Syndrome (R10 - 13).

   I80 - 83 is the partial syndrome coming from one 3BI option to the other one. The 8 bits of partial syndrome are used on the 3BI option to generate the final syndrome to be used to check and correct the HISP data.

6. Syndrome. A Syndrome is sent back to the 3BH option from the 3BI option.

   3BI - Syndrome (R20 - 21) from the 3BI options is sent to the 3BH option.

   3BH - Syndrome data is received from 3BI0 as I14 - 15 and from 3BI1 as I16 - 17. This data is latched to the 3BH option by the HISP Input Sample Data counter started by I12. The 3BH option then sends the error information back to the HCM through R30 - 31.

7. Buffer Address. The Buffer Address is the read and write address that is sent to the 3BB options for the 32-word buffers on these options.

   3BH - Buffer Address (R20 - 24) is sent to the 3BB options and is a MUX of the address for both the write to and read from the buffers on the 3BB options. The address on these lines is a read address except at count seven of the HISP Input Sample Data timing chain started by I12. During count seven the write address is presented to the 3BB options. The write buffer address is incremented at count seven, and the read buffer address is incremented at sync + 0 if the write and read buffer address are not equal.

   3BB - The Buffer Address comes from the 3BH option as I10 - 14. This address slides through four sets of terms to address the four buffer ranks on the 3BB options.

8. Read HISP Data (Write Buffer). This buffer is used as a write enable for the buffers on the 3BB options.

   3BH - Read HISP Data (Write Buffers) (R17) is sent to the 3BB options with the Write Buffer Address to write a word of Data into the buffers on the 3BB options. This signal is sent at count seven of the HISP Input Sample Data timing chain.

   3BB - Read HISP Data (Write Buffer) (I17) is received from the 3BH option and slides through four terms to make the write enables for the four buffer ranks on the 3BB option.

9. HISP Data to Buffers. HISP Data to Buffers is the data leaving the 3BI options going to the 3BB options.

3BI - Corrected HISP data leaves the 3BI options as R0 - 7, and check bits leave the 3BI option as R8. It takes four transfers to send each word of data.

3BB - HISP Input Data (I0 - 8) comes from the 3BI options and is written into the 32-word buffers on the 3BB options. The information below shows which R terms on the 3BI option sends data to which I terms on the 3BB options, and which bits are handled on which option.

3BI0 sends R0 - 3 to I0 - 3 on 3BB0
3BI0 sends R4 - 7 to I4 - 7 on 3BB1
3BI0 sends R8 to I8 on 3BB1
3BI1 sends R0 - 3 to I0 - 3 on 3BB1
3BI1 sends R4 - 7 to I4 - 7 on 3BB0
3BI1 sends R8 to I8 on 3BB0

3BB0 handles bits 2^0 - 2^3, 2^8 - 2^{11}, 2^{16} - 2^{19}, 2^{24} - 2^{27}, 2^{36} - 2^{39}, 2^{44} - 2^{47}, 2^{52} - 2^{55}, 2^{60} - 2^{63}, and 2^{68} - 2^{71}

3BB1 handles bits 2^4 - 2^7, 2^{12} - 2^{15}, 2^{20} - 2^{23}, 2^{28} - 2^{31}, 2^{32} - 2^{35}, 2^{40} - 2^{43}, 2^{48} - 2^{51}, 2^{56} - 2^{59}, and 2^{64} - 2^{67}

10. Go HISP Write Reference. The Go HISP Write Reference is sent from the 3BH option to the 3BB options to send data from the 3BB options on memory.

    3BH - Go HISP Write Reference (R16) is sent to the 3BB options if the write and read buffers are not equal at sync + 0.

    3BB - Go HISP Write Reference (I32 and I33) comes from the 3BH option and is used to latch the channel number and A/B Select into terms that will make the correct R terms (R20 - 27) that are sent onto the 3BA option.

11. Buffer Readout Read Ahead. The Buffer Readout Read Ahead is sent from the 3BH option to the 3BB option to resolve read and write conflicts in the buffers on the 3BB options.

    3BH - Buffer Readout Read Ahead (R25) is sent to the 3BB option if count six of the HISP Input Sample Data counter and sync + 5 happen at the same time.

    3BB - If a conflict of a read and a write from the buffers occurs, the read will be held up for 1 CP. Buffer Readout Read

Ahead (I21) causes the data to be read from the correct terms.

12. HISP Data to Buffers. The HISP Data to Buffers is the word of HISP data leaving the 3BB option and going to fanin.

    3BB - Data leaving the buffers on the 3BB options are sent to fanin based on the tinformation listed in subsection, High-speed Data Fanin into Channel Memory. R0 - 8 is the data leaving each 3BB option. It takes four transfers to send all 72 bits.

13. Select Channel N + x HISP Data. This signal is sent to the correct 3BA option to latch the data in from the fanin explained above.

    3BB - The 3BB option receives the channel number and A/B encode from the 3BH option and sends R20 - 27, Select Channel N + x HISP Data, to the correct 3BC and 3BA options. Figure 4-9 shows where each of these signals goes from the 3BB options on the A side of the buffer board.

14. Select Onboard/Offboard HISP Data. These signals come to the 3BA and 3BC options from R20 -27 on the 3BB options.

    3BA - Select Onboard HISP Data (I63) and Select Offboard HISP Data (I64) come from one of the R terms above. These terms, at sync + 3, mean there is a write reference, at sync + 4 they mean the B pointer is to be used, and at sync + 5 they mean it is a read reference. This signal latches the check bits on to the 3BA option and also begins the process to generate the write enable signal.

    3BC - Select Onboard HISP Data (I63) and Select Offboard HISP Data (I64) come from the 3BB option and starts a timing chain that latches the data coming from the fanin on to the 3BC option. The 32 bits of data are latched in four 8-bit transfers.

15. Data. The Data is the data leaving the 3BA and 3BC options going to the channel buffer memory array.

    3BA - The HISP check bits going to memory are loaded into Data (R0 - 7), and are presented to the memory chips at sync + 3 - 5.

    3BC - The HISP data going to memory is loaded into Data (R0 - 31), and is presented to the memory chips at sync + 3 - 5.

16. Address. The Address is the address that is sent to address the memory chips.

    3BA - The 16-bit address (R10 - 25) is sent to memory at sync + 3 - 5 for HISP Data, along with the data.

17. Write Enable. This signal is sent with the address and word of data to allow the data to be written into the memory chips.

    3BA - When I63 or I64 come to the 3BA option at sync + 3 they start the generation of the write enable pulse. The Raw Write Enable (R30 - 32) is fed back to the same 3BA option as I74 and I73 respectively, and these signals are used to make Write Enable (R33). This signal goes to memory and allows the memory chips to be written to.

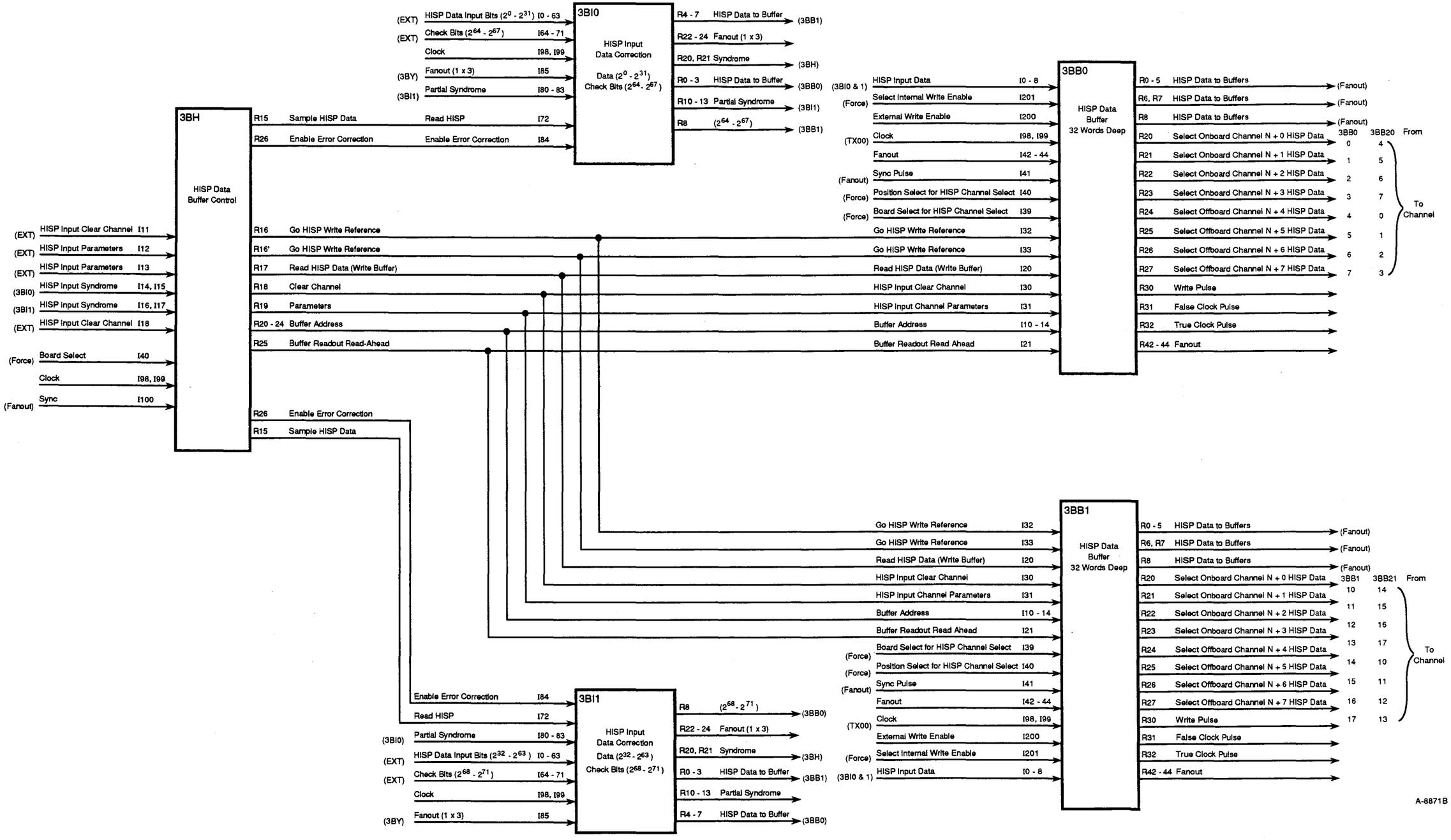


Figure 4-9. HISP Input

High-speed Data Fanin into Channel Memory

HISP data leaving the 3BB options on the A board is fanned in in the following manner:

For Channels 0, 1, 2, 3

From 3BB0					From 3BB1				
R0	BC02	I40	on	00, 08, 16, 24	R0	BC06	I40	on	04, 12, 20, 28
R1	BC02	I41	on	01, 09, 17, 25	R1	BC06	I41	on	05, 13, 21, 29
R2	BA01	I36	on	02, 10, 18, 26	R2	BA03	I36	on	06, 14, 22, 30
R3	BC03	I40	on	03, 11, 19, 27	R3	BC07	I40	on	07, 15, 23, 31
R4	BC03	I41	on	36, 44, 52, 60	R4	BC07	I41	on	64, 65, 66, 67
R5	BD02	I90	on	37, 45, 53, 61	R5	BD06	I90	on	32, 40, 48, 56
R6	BD02	I91	on	38, 46, 54, 62	R6	BD06	I91	on	33, 41, 49, 57
R7	BD03	I90	on	39, 47, 55, 63	R7	BD06	I90	on	34, 42, 50, 58
R8	BD03	I91	on	68, 69, 70, 71	R8	BD06	I91	on	35, 43, 51, 59

For Channels 10, 11, 12, 13

R0'	BC10	I40	on	00, 08, 16, 24'	R0'	BC14	I40	on	04, 12, 20, 28'
R1'	BC10	I41	on	01, 09, 17, 25'	R1'	BC14	I41	on	05, 13, 21, 29'
R2'	BA05	I36	on	02, 10, 18, 26'	R2'	BA07	I36	on	06, 14, 22, 30'
R3'	BC11	I40	on	03, 11, 19, 27'	R3'	BC15	I40	on	07, 15, 23, 31'
R4'	BC11	I41	on	36, 44, 52, 60'	R4'	BC15	I41	on	64, 65, 66, 67'
R5'	BD10	I90	on	37, 45, 53, 61'	R5'	BD14	I90	on	32, 40, 48, 56'
R6'	BD10	I91	on	38, 46, 54, 62'	R6'	BD14	I91	on	33, 41, 49, 57'
R7'	BD11	I90	on	39, 47, 55, 63'	R7'	BD15	I90	on	34, 42, 50, 58'
R8'	BD11	I91	on	68, 69, 70, 71'	R8'	BD15	I91	on	35, 43, 51, 59'

For Channels 4, 5, 6, 7

R0a	BC20	I40	off	00, 08, 16, 24	R0a	BC24	I40	off	04, 12, 20, 28
R1a	BC20	I41	off	01, 09, 17, 25	R1a	BC24	I41	off	05, 13, 21, 29
R2a	BA20	I36	off	02, 10, 18, 26	R2a	BA22	I36	off	06, 14, 22, 30
R3a	BC21	I40	off	03, 11, 19, 27	R3a	BC25	I40	off	07, 15, 23, 31
R4a	BC21	I41	off	36, 44, 52, 60	R4a	BC25	I41	off	64, 65, 66, 67
R5a	BD20	I90	off	37, 45, 53, 61	R5a	BD24	I90	off	32, 40, 48, 56
R6a	BD20	I91	off	38, 46, 54, 62	R6a	BD24	I91	off	33, 41, 49, 57
R7a	BD21	I90	off	39, 47, 55, 63	R7a	BD25	I90	off	34, 42, 50, 58
R8a	BD21	I91	off	68, 69, 70, 71	R8a	BD33	I91	off	35, 43, 51, 59

For Channels 14, 15, 16, 17

R0a'	BC28	I40	off	00, 08, 16, 24'	R0a'	BC32	I40	off	04, 12, 20, 28'
R1a'	BC28	I41	off	01, 09, 17, 25'	R1a'	BC32	I41	off	05, 13, 21, 29'
R2a'	BA20	I36	off	02, 10, 18, 26'	R2a'	BA26	I36	off	06, 14, 22, 30'
R3a'	BC29	I40	off	03, 11, 19, 27'	R3a'	BC33	I40	off	07, 15, 23, 31'
R4a'	BC29	I41	off	36, 44, 52, 60'	R4a'	BC33	I41	off	64, 65, 66, 67'
R5a'	BD28	I90	off	37, 45, 53, 61'	R5a'	BD32	I90	off	32, 40, 48, 56'
R6a'	BD28	I91	off	38, 46, 54, 62'	R6a'	BD32	I91	off	33, 41, 49, 57'
R7a'	BD29	I90	off	39, 47, 55, 63'	R7a'	BD33	I90	off	34, 42, 50, 58'
R8a'	BD29	I91	off	68, 69, 70, 71'	R8a'	BD25	I91	off	35, 43, 51, 59'

NOTE: A not sign at the end of a group of terms indicates all terms are notted (00, 08, 16, 24' = 00', 08', 16', 24'). The words "off" and "on" in the charts above indicate offboard and onboard HISP data respectively. Data continues through the above options as follows:

BC I40 - 41 makes B40 - 41 which makes R40 - 41
BA I36 makes K36 which makes R36
BD I90 - 91 makes Y0 - 1 which makes R60 - 61

The above R terms send the HISP data to the correct 3BC and 3BA options for the channel the data is intended for.

HISP data is sent to the correct channel options on the A board as follows:

Channels 00, 01, 02, 03
BC00, 02, 04, 06

Offboard HISP Data					Onboard HISP Data				
I30	from	BC00	R40	00, 08, 16, 24	I20	from	BC02	R40	00, 08, 16, 24
I31	from	BC00	R41	01, 09, 17, 25	I21	from	BC02	R41	01, 09, 17, 25
I32	from	BA00	R36	02, 10, 18, 26	I22	from	BA01	R36	02, 10, 18, 26
I33	from	BC01	R40	03, 11, 19, 27	I23	from	BC03	R40	03, 11, 19, 27
I34	from	BC04	R40	04, 12, 20, 28	I24	from	BC06	R40	04, 12, 20, 28
I35	from	BC04	R41	05, 13, 21, 29	I25	from	BC06	R41	05, 13, 21, 29
I36	from	BA02	R36	06, 14, 22, 30	I26	from	BA03	R36	06, 14, 22, 30
I37	from	BC05	R40	07, 15, 23, 31	I27	from	BC07	R40	07, 15, 23, 31

BC01, 03, 05, 07

I30	from	BD04	R60	32, 40, 48, 56	I20	from	BD06	R60	32, 40, 48, 56
I31	from	BD04	R61	33, 41, 49, 57	I21	from	BD06	R61	33, 41, 49, 57
I32	from	BD05	R60	34, 42, 50, 58	I22	from	BD07	R60	34, 42, 50, 58
I33	from	BD05	R61	35, 42, 51, 59	I23	from	BD07	R61	35, 43, 51, 59
I34	from	BC01	R41	36, 44, 52, 60	I24	from	BC03	R41	36, 44. 52, 60
I35	from	BD00	R60	37, 45, 53, 61	I25	from	BD02	R60	37, 45, 53, 61
I36	from	BD00	R61	38, 46, 54, 62	I26	from	BD02	R61	38, 46, 54, 62
I37	from	BD01	R60	39, 47, 55, 63	I27	from	BD03	R60	39, 47, 55, 63

BA00, 01, 02, 03

I22	from	BC05	R41	64, 65, 66, 67	I20	from	BC07	R41	64, 65, 66, 67
I23	from	BD01	R61	68, 69, 70, 71	I21	from	BD03	R61	68, 69, 70, 71

Channels 10, 11, 12, 13

BC08, 10, 12, 14

I30	from	BC08	R40	00, 08, 16, 24	I20	from	BC10	R40	00, 08, 16, 24
I31	from	BC08	R41	01, 09, 17, 25	I21	from	BC10	R41	01, 09, 17, 25
I32	from	BA04	R36	02, 10, 18, 26	I22	from	BA05	R36	02, 10, 18, 26
I33	from	BC09	R40	03, 11, 19, 27	I23	from	BC11	R40	03, 11, 19, 27
I34	from	BC12	R40	04, 12, 20, 28	I24	from	BC14	R40	04, 12, 20, 28
I35	from	BC12	R41	05, 13, 21, 29	I25	from	BC14	R41	05, 13, 21, 29
I36	from	BA06	R36	06, 14, 22, 30	I26	from	BA07	R36	06, 14, 22, 30
I37	from	BC13	R40	07, 15, 23, 31	I27	from	BC15	R40	07, 15, 23, 31

BC09, 11, 13, 15

I30	from	BD12	R60	32, 40, 48, 56	I20	from	BD14	R60	32, 40, 48, 56
I31	from	BD12	R61	33, 41, 49, 57	I21	from	BD14	R61	33, 41, 49, 57
I32	from	BD13	R60	34, 42, 50, 58	I22	from	BD15	R60	34, 42, 50, 58
I33	from	BD13	R61	35, 43, 51, 59	I23	from	BD15	R61	35, 43, 51, 59
I34	from	BC09	R41	36, 44, 52, 60	I24	from	BC11	R41	36, 44, 52, 60
I35	from	BD08	R60	37, 45, 53, 61	I25	from	BD10	R60	37, 45, 53, 61
I36	from	BD08	R61	38, 46, 54, 62	I26	from	BD10	R61	38, 46, 54, 62
I37	from	BD09	R60	39, 47, 55, 63	I27	from	BD11	R60	39, 47, 55, 63

BA04, 05, 06, 07

I22	from	BC13	R41	64, 65, 66, 67	I20	from	BC15	R41	64, 65, 66, 67
I23	from	BD09	R61	68, 69, 70, 71	I21	from	BD11	R61	68, 69, 70, 71

NOTE: To use this chart for the B side simply add 20 to the option number. Channel numbers would be 04, 05, 06, 07 and 14, 15, 16, 17.

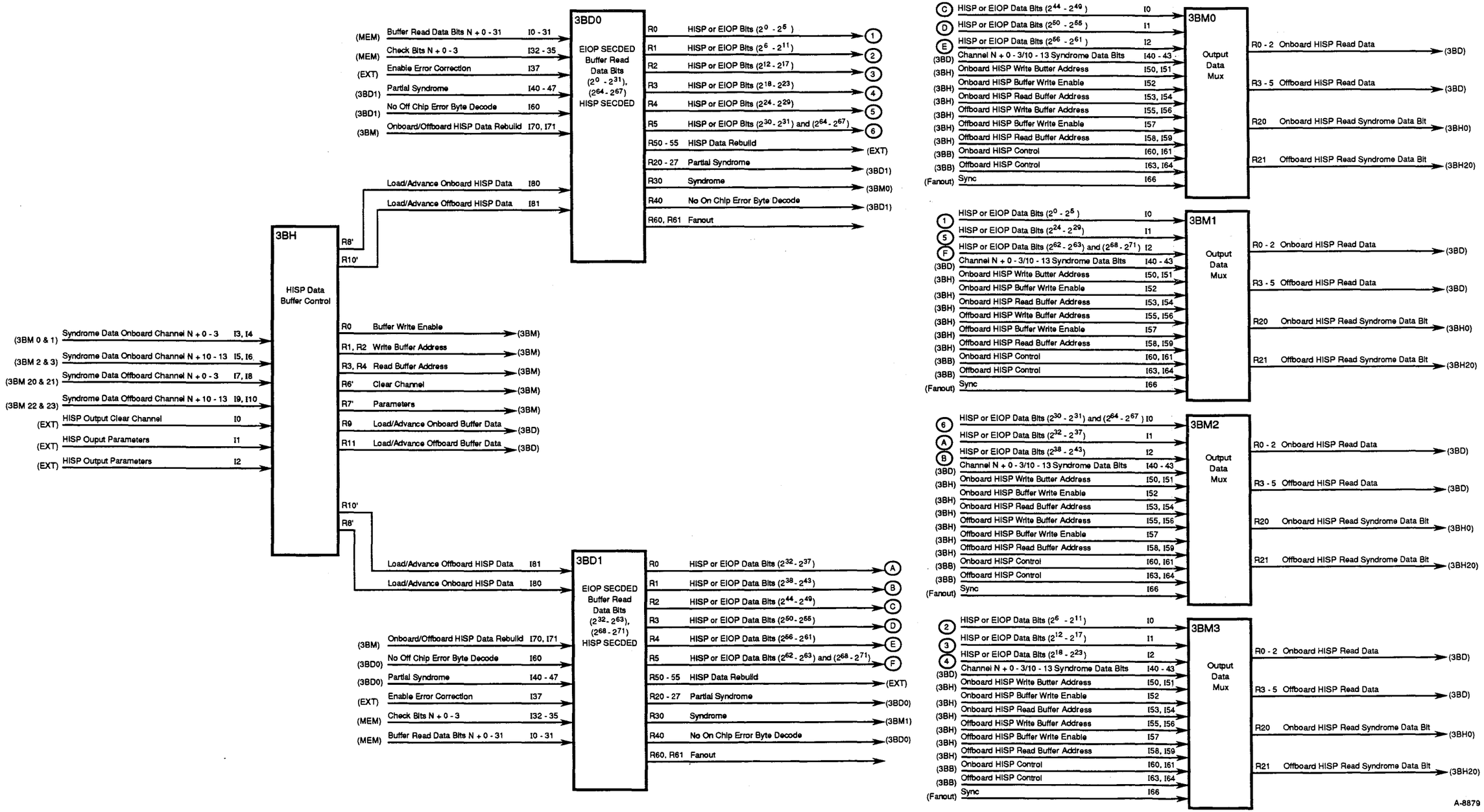


Figure 4-10. HISP Output From Channel 0

High-speed Read Data Fanout

The information below shows HISP data fanin from the 3BD options to the 3BM options.

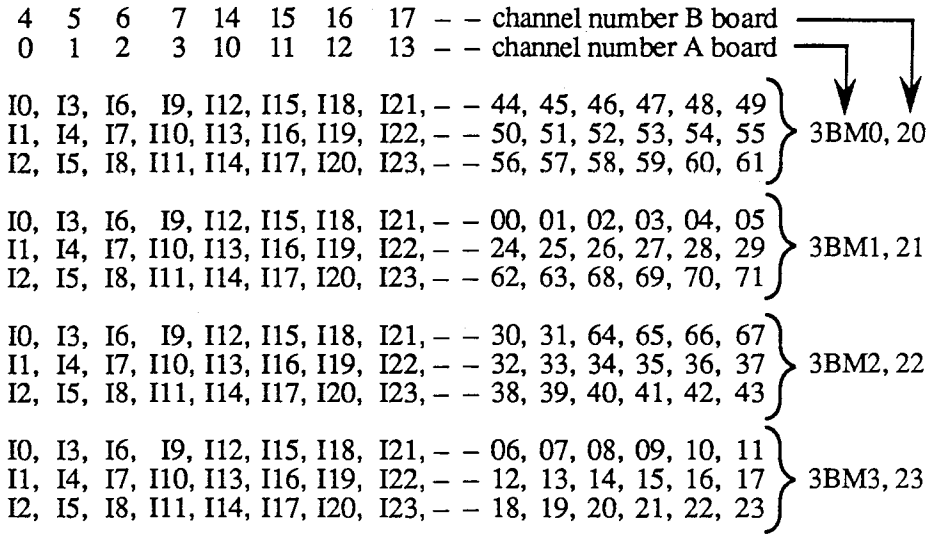


Table 4-6. HISP Data A and B Board Fanout from 3BM Options

	HISP Data A Board				
	Term	To	Option	Term	Bits
3BM0	R0	to	3BD8	I70	44 - 49
	R1	to	3BD5	I70	50 - 55
	R2	to	3BD6	I70	56 - 61
	R3	to	3BD28	I71	44 - 49
	R4	to	3BD25	I71	50 - 55
	R5	to	3BD26	I71	56 - 61
3BM1	R0	to	3BD0	I70	00 - 05
	R1	to	3BD12	I70	24 - 29
	R2	to	3BD10	I70	62, 63, 68 - 71
	R3	to	3BD20	I71	00 - 05
	R4	to	3BD32	I71	24 - 29
	R5	to	3BD30	I71	62, 63, 68 -71
3BM2	R0	to	3BD9	I70	30, 31, 64 - 67
	R1	to	3BD13	I70	32 - 37
	R2	to	3BD14	I70	38 - 43
	R3	to	3BD29	I71	30, 31, 64 - 67
	R4	to	3BD33	I71	32 - 37
	R5	to	3BD34	I71	38 - 43
3BM3	R0	to	3BD1	I70	06 - 11
	R1	to	3BD2	I70	12 - 17
	R2	to	3BD4	I70	18 - 23
	R3	to	3BD21	I71	06 - 11
	R4	to	3BD22	I71	12 - 17
	R5	to	3BD24	I71	18 - 23

	HISP Data B Board				
	Term	To	Option	Term	Bits
3BM20	R0	to	3BD28	I70	44 - 49
	R1	to	3BD25	I70	50 - 55
	R2	to	3BD26	I70	56 - 61
	R3	to	3BD8	I71	44 - 49
	R4	to	3BD5	I71	50 - 55
	R5	to	3BD6	I71	56 - 61
3BM21	R0	to	3BD20	I70	00 - 05
	R1	to	3BD32	I70	24 - 29
	R2	to	3BD30	I70	62, 63, 68 - 71
	R3	to	3BD0	I71	00 - 05
	R4	to	3BD12	I71	24 - 29
	R5	to	3BD10	I71	62, 63, 68 - 71
3BM22	R0	to	3BD29	I70	30, 31, 64 - 67
	R1	to	3BD33	I70	32 - 37
	R2	to	3BD34	I70	38 - 43
	R3	to	3BD9	I71	30, 31, 64 - 67
	R4	to	3BD13	I71	32 - 37
	R5	to	3BD14	I71	38 - 43
3BM23	R0	to	3BD21	I70	06 - 11
	R1	to	3BD22	I70	12 - 17
	R2	to	3BD24	I70	18 - 23
	R3	to	3BD1	I71	06 - 11
	R4	to	3BD2	I71	12 - 17
	R5	to	3BD4	I71	18 - 23

Table 4-7. A Side Buffer Board Chip Locator

	Buffer 0 EIOP0 30/31	Buffer 1 EIOP0 32/33	Buffer 2 EIOP0 34/35	Buffer 3 EIOP0 36/37	Buffer 10 EIOP2 30/31	Buffer 11 EIOP2 32/33	Buffer 12 EIOP2 34/35	Buffer 13 EIOP2 36/37
Chip Group → Bits ↓	AZZ0 ↓	AZZ1 ↓	AZZ2 ↓	AZZ3 ↓	AZZ4 ↓	AZZ5 ↓	AZZ6 ↓	AZZ7 ↓
0, 9, 23, 28	6	6	6	6	8	8	8	8
1, 10, 21, 30	7	7	7	7	7	7	7	7
2, 11, 22, 31	3	3	3	3	5	5	5	5
3, 8, 20, 29	4	4	4	4	4	4	4	4
4, 13, 19, 24	5	5	5	5	3	3	3	3
5, 14, 17, 26	0	0	0	0	2	2	2	2
6, 15, 18, 27	1	1	1	1	1	1	1	1
7, 12, 16, 25	2	2	2	2	0	0	0	0
32, 41, 55, 60	9	9	9	9	11	11	11	11
33, 42, 53, 62	10	10	10	10	10	10	10	10
34, 43, 54, 63	12	12	12	12	14	14	14	14
35, 40, 52, 61	13	13	13	13	13	13	13	13
36, 45, 51, 56	14	14	14	14	12	12	12	12
37, 46, 49, 58	15	15	15	15	17	17	17	17
38, 47, 50, 59	16	16	16	16	16	16	16	16
39, 44, 48, 57	17	17	17	17	15	15	15	15
64, 66, 68, 70	8	8	8	8	6	6	6	6
65, 67, 69, 71	11	11	11	11	9	9	9	9

Example: EIOP2, Buffer 10, Bit 34 would be chip AZZ4-14.

Table 4-8. B Side Buffer Board Chip Locator

	Buffer 4 EIOP1 30/31	Buffer 5 EIOP1 32/33	Buffer 6 EIOP1 34/35	Buffer 7 EIOP1 36/37	Buffer 14 EIOP3 30/31	Buffer 15 EIOP3 32/33	Buffer 16 EIOP3 34/35	Buffer 17 EIOP3 36/37
Chip Group → Bits ↓	BZZ0 ↓	BZZ1 ↓	BZZ2 ↓	BZZ3 ↓	BZZ4 ↓	BZZ5 ↓	BZZ6 ↓	BZZ7 ↓
0, 9, 23, 28	6	6	6	6	8	8	8	8
1, 10, 21, 30	7	7	7	7	7	7	7	7
2, 11, 22, 31	3	3	3	3	5	5	5	5
3, 8, 20, 29	4	4	4	4	4	4	4	4
4, 13, 19, 24	5	5	5	5	3	3	3	3
5, 14, 17, 26	0	0	0	0	2	2	2	2
6, 15, 18, 27	1	1	1	1	1	1	1	1
7, 12, 16, 25	2	2	2	2	0	0	0	0
32, 41, 55, 60	9	9	9	9	11	11	11	11
33, 42, 53, 62	10	10	10	10	10	10	10	10
34, 43, 54, 63	12	12	12	12	14	14	14	14
35, 40, 52, 61	13	13	13	13	13	13	13	13
36, 45, 51, 56	14	14	14	14	12	12	12	12
37, 46, 49, 58	15	15	15	15	17	17	17	17
38, 47, 50, 59	16	16	16	16	16	16	16	16
39, 44, 48, 57	17	17	17	17	15	15	15	15
64, 66, 68, 70	8	8	8	8	6	6	6	6
65, 67, 69, 71	11	11	11	11	9	9	9	9

Example: EIOP3, Buffer 14, Bit 34 would be chip BZZ4-14.

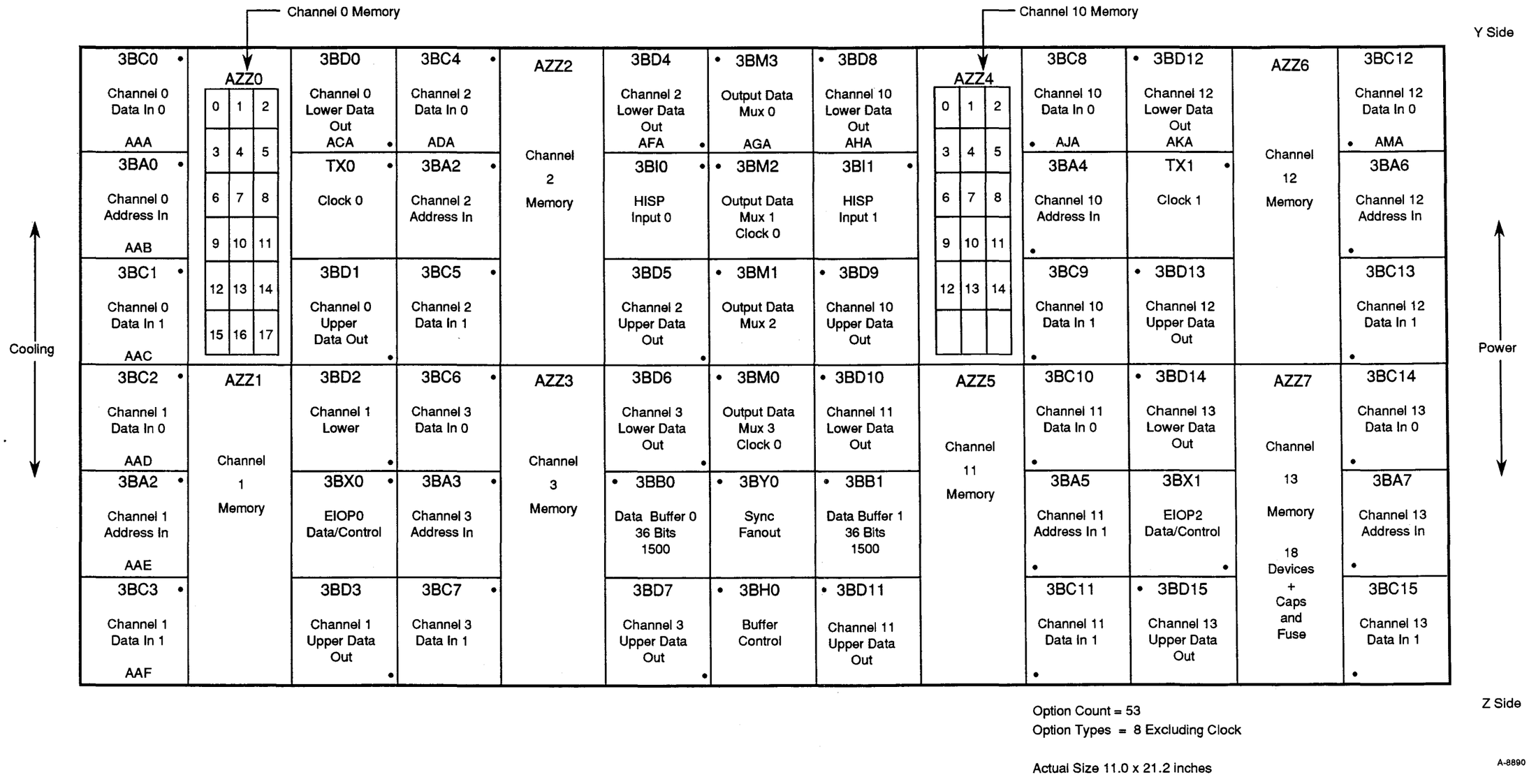


Figure 4-11. I/O Buffer Chip Map (A Board)

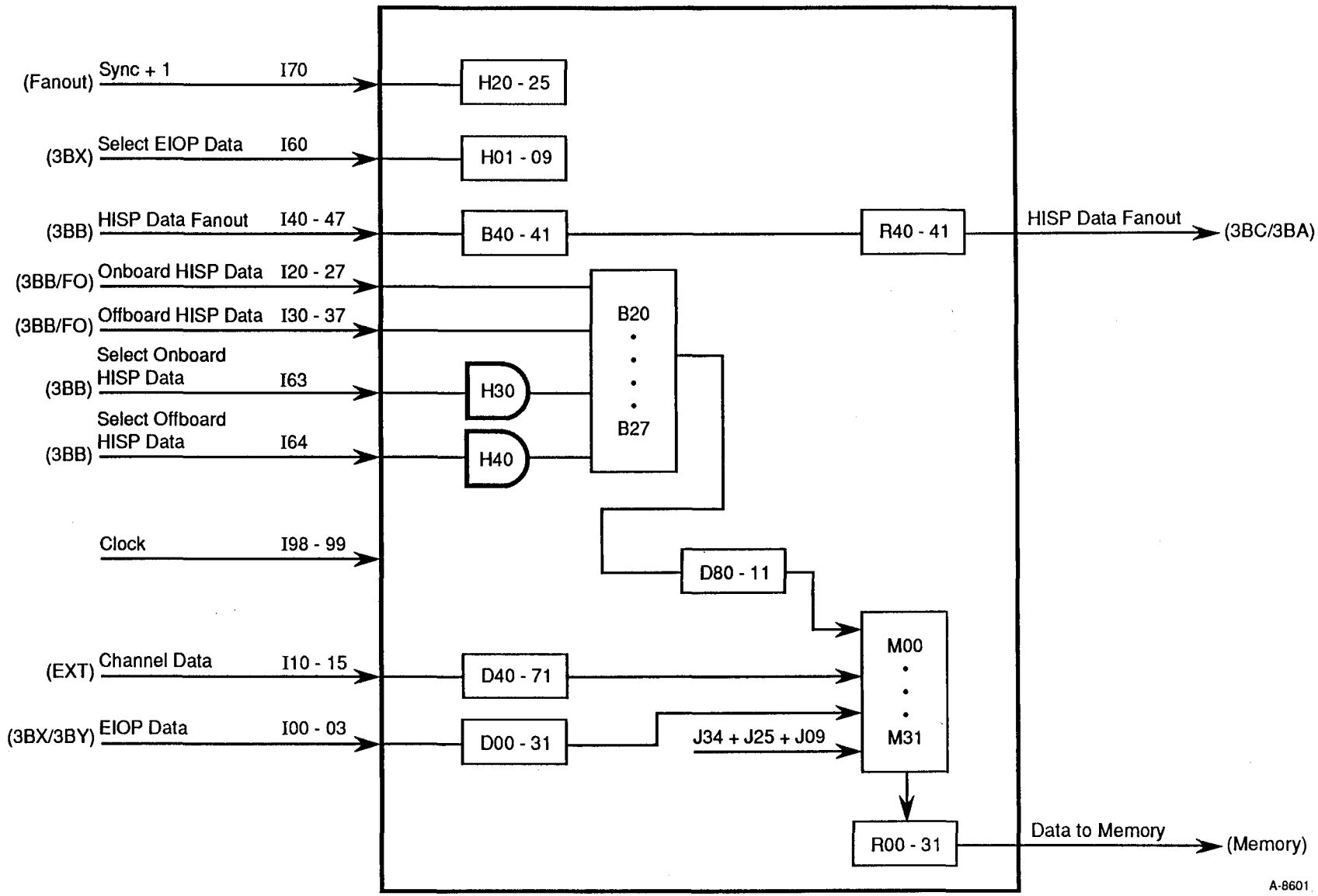


Figure 4-12. IOS Model E 3BC

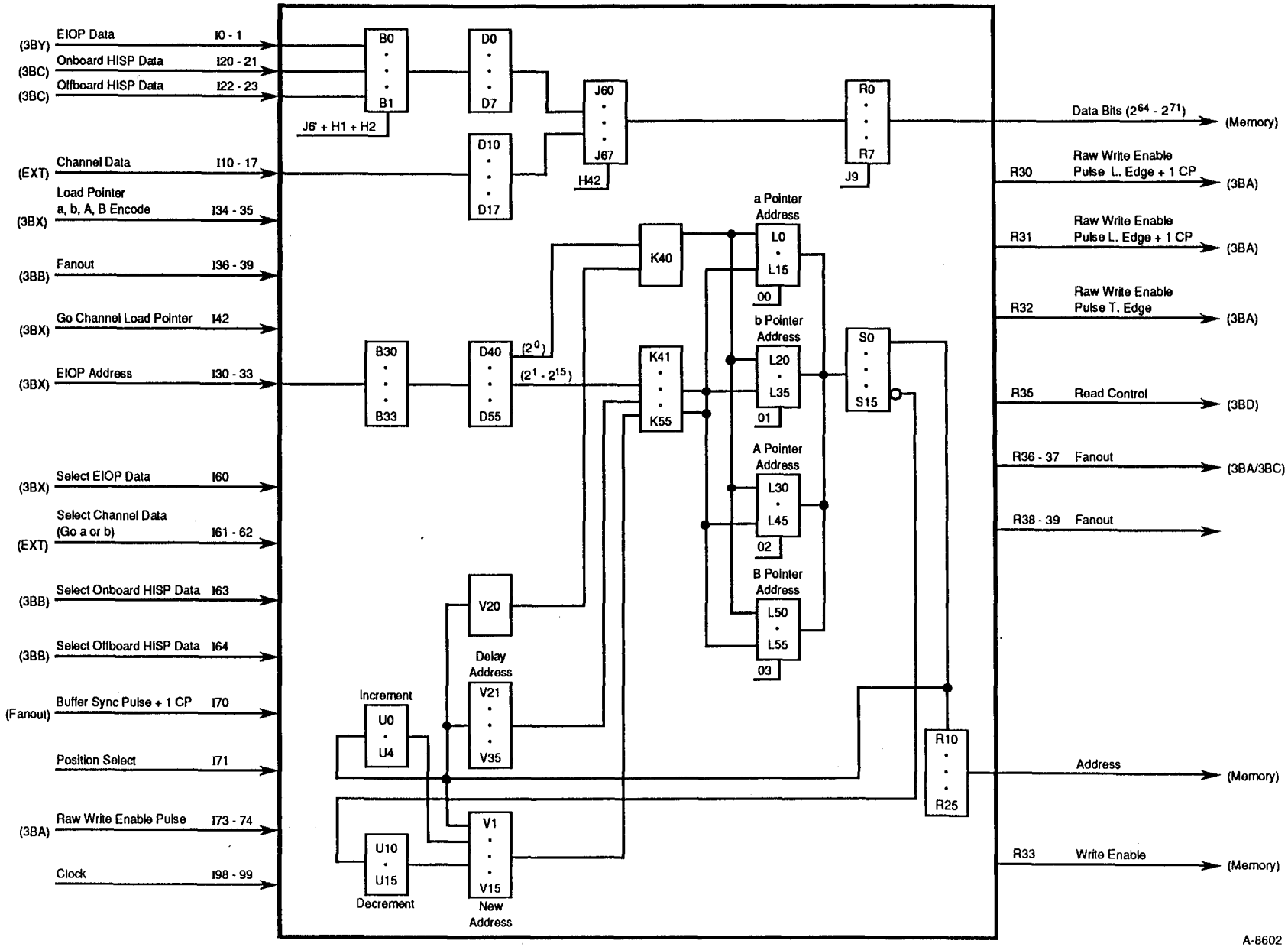


Figure 4-13. IOS Model E 3BA

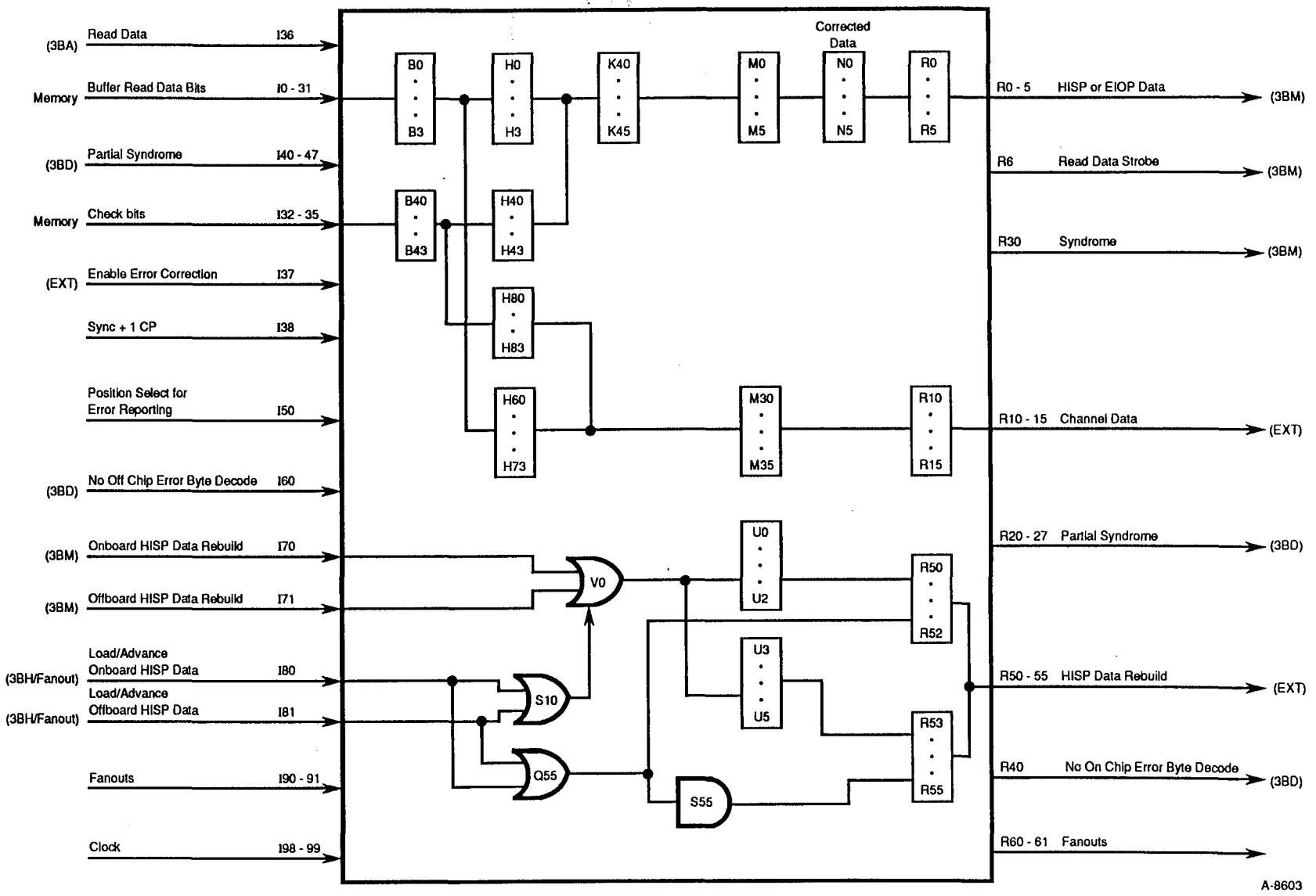


Figure 4-14. IOS Model E 3BD

5 HCM HIGH-SPEED/LOW-SPEED QUARTER BOARD

The HCM high-speed/low-speed (HISP/LOSP) multiplexer (MUX) quarter board consists of the 3SA, 3SG, 3SL, 3SI, and 3SO options. Refer to Table 5-1 for a functional description of each option. The HCM controls the LOSP transfers between the mainframe and the IOS-E, and the HISP transfers between the IOS-E and the mainframe and the SSD solid-state storage device (SSD). Each IOS-E cluster requires two HCM quarter boards. The HCM0 quarter board has HISP channels 10 - 13. The HCM1 quarter board has LOSP channels 20 - 21 and HISP channels 14 - 17. The LOSP channels 20 - 21 transfer data at 6- or 50-Mbyte rates. The HISP channels transfer data at 100- or 200-Mbyte rates. Refer to Figure 5-7 for the HCM option layout.

Table 5-1. HCM Options and Descriptions

Options	Functional Description
3SA0	HISP-In address/block length to mainframe or SSD
3SA1	HISP-Out address/block length to mainframe or SSD
3SG	HISP input control and BZ/DN HISP-In block length
3SI	LOSP data in (7-parcel buffer)
3SK	HISP output control and BZ/DN
3SL	LOSP control and BZ/DN LOSP-In parcel count
3SO	HISP-Out block length LOSP data out (7-parcel buffer)

High-speed Data Flow

The HISP-In data is sent from the mainframe or SSD to the buffer board under the control of the 3SG. Data is sent one word per reference with check bits (CBs) (64 data bits and 8 CBs). Refer to Figure 5-1 for a HISP data in block diagram.

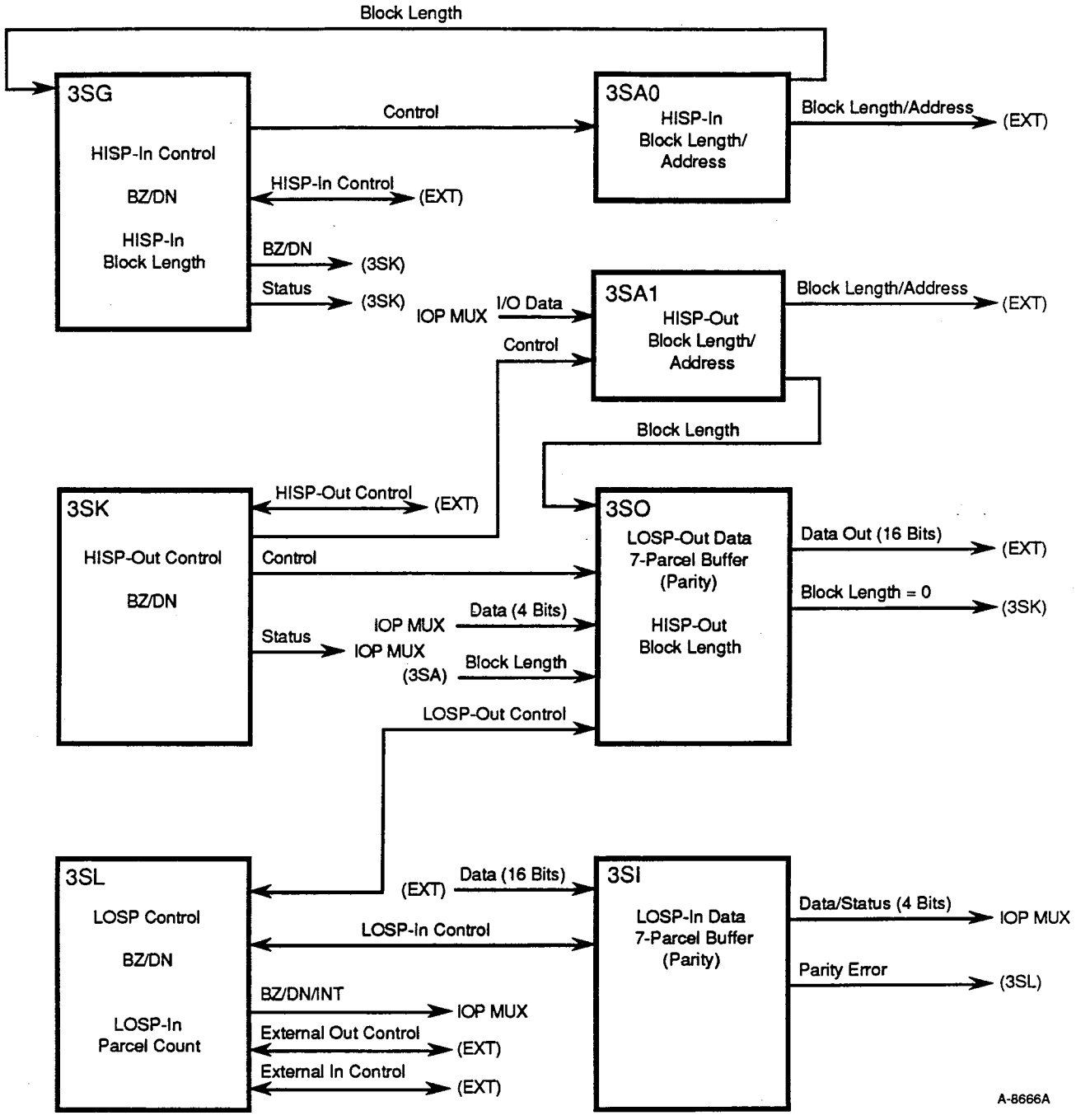


Figure 5-1. HISP/LOSP MUX Block Diagram

The HISP-Out data is sent from the buffer board to the mainframe or SSD under the control of the 3SK. Data is sent 1 word per reference with check bits (64 data bits and 8 CBs). Refer to Figure 5-1 for a HISP data out block diagram.

Low-speed Data

The LOSP data is transferred from the mainframe to the 3SI to the I/O processor (IOP) (3AS). For a LOSP data in block diagram, refer to Figure 5-1. The mainframe sends the data to the 3SI 1 parcel per reference with 4 bits of parity per parcel. The 3SI checks the parity and then sends the data to the 3AS, 4 bits at a time. The 3AS assembles the data into a parcel and then writes it into local memory. The 3SI has a 7-parcel data buffer.

The LOSP data out is transferred from the IOP (3AQ) to the 3SO and then to the mainframe. For a LOSP data out block diagram, refer to Figure 5-1. The data is sent from the 3AQ to the 3SO 1 parcel per reference, but 4 bits at a time. The 3SO assembles the data into a parcel, generates parity, and then outputs the data to the mainframe. The 3SO has a 7-parcel data buffer.

High-speed Protocol

The following is a description of the HISP protocol. Refer to Figure 5-2 for a HISP protocol block diagram.

- Clear Channel. The Clear Channel clears the device and enables it to send or receive data.

- Transmit Address. The Transmit Address enables the HCM to output the address and block length. The device deactivates Transmit Address after receiving all the Address Readies. The device activates Transmit Address at the end of the transfer if no errors occurred.

- Address Ready. The Address Ready informs the external device that the HCM is sending the address and/or block length.

  There are 16 bits of address and block length and 4 bits of parity for the CRAY Y-MP or SSD Model D. It takes three Address Readies to get the complete address and block length to the device.

  There are 12 bits of address and block length and 3 bits of parity for the CRAY Y-MP16 or SSD Model E. It takes five Address Readies to get the complete address and block length to the device.

- Transmit Data. The Transmit Data is sent by the receiver and it enables the sender to send 16 words (72 bits) of data.

- Data Ready. The Data Ready is sent by the sender with each word of data.
- Last Word Flag. The Last Word Flag is sent by the sender to signal the last word of the transfer. It is sent with the last Data Ready.
- Errors. The Errors are sent to the HCM from the device. The device error types are parity errors on the address and block length bits, SECDED errors, sequence errors, and block length errors.

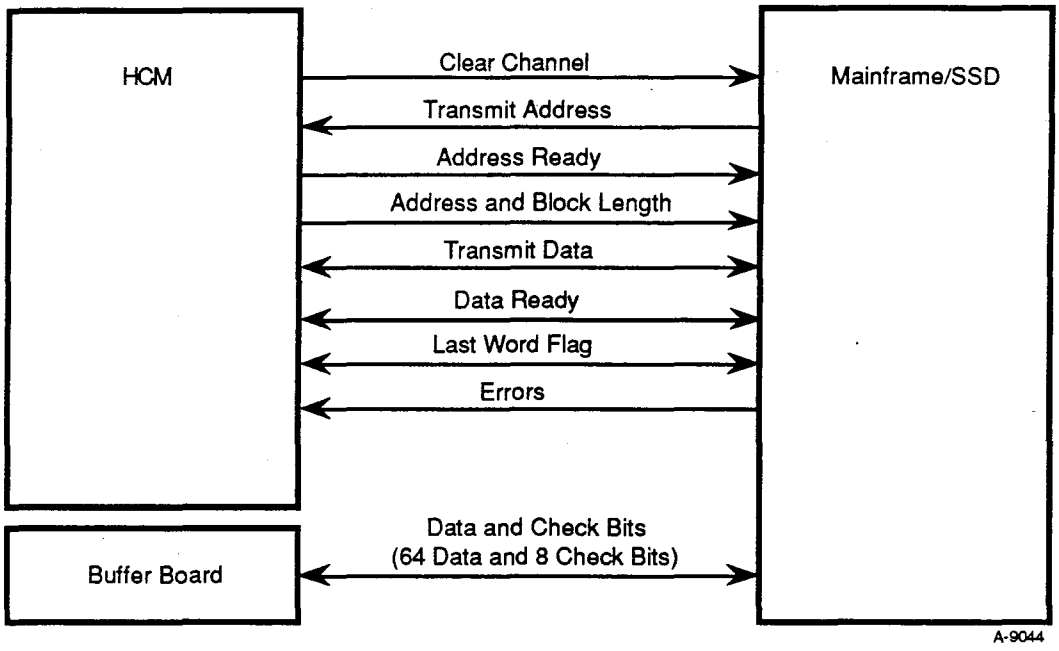


Figure 5-2. High-speed Protocol Block Diagram

High-speed Data In Sequence

The following is a sequential description of a HISP data input sequence. Refer to Figure 5-3 for a HISP block diagram.

1. Go IOP Function. The IOP sends Go IOP Function to channels 10 - 13 or 14 - 17. After Go IOP Function is received, the channel decodes the IOP Function Data. The IOP Function Data is the modifier bit that clock period (CP) and the command on the next clock period. If needed, for the next 4 CPs the IOP Function Data is the accumulator data.

   IOP - The 3AS sends Go IOP Function (R30) and the 3AQ sends IOP Function Data (R10 - 13) for channels 10 - 13. The 3AP sends Go IOP Function (R30) and the 3AO sends IOP Function Data (R10 - 13) for channels 14 - 17.

3SG - After the 3SG decodes a command 0, it initiates the Clear Channel sequence. After a command 5, the 3SG initiates the Address Ready sequence.

3SA0 - After receiving the CPU Output Control (Go IOP Function I4), the 3SA0 decodes the CPU Output Data (IOP Function Data I0 - 3). After a command 5 is decoded, the accumulator data is the block length, after a command 2 or 3 it is the CPU address, and after command 16 it is the pointer select A or B and buffer bits 2^0 - 2^3.

2. Clear Channel. The Clear Channel clears the device and enables it to send data.

   3SG - After a command 0 is decoded by the 3SG and Transmit Address is not enabled, the 3SG starts the Clear Channel sequence. If Transmit Address was already enabled, the 3SG does not initiate a Clear Channel (R0), but instead waits for a command 5 and then starts the Address Ready sequence.

3. Transmit Address. The device activates Transmit Address when it can accept the CPU address and block length, and drops it after it has received three Address Readies.

   3SG - The 3SG accepts the Transmit Address (I0 - 1) and sends a Reset Address Channel (R5) to the 3SA0 and enables Address Ready (R1) to the mainframe or SSD. If the previous transfer completed error free, Transmit Address would have already been enabled.

   3SA0 - The 3SA0 clears the address readout counter after receiving Reset Address Channel (I10) from the 3SG.

4. Address Ready. The Address Ready informs the device that the IOP is sending the address and/or block length, and it takes three Address Readies to get the address and block length to the device.

   3SG - The Address Ready sequence starts after a command 5 has been decoded and the Clear Channel sequence has completed and Transmit Address is active. The Address Ready sequence sends the Address Readies (R1) to the device. Prior to that, the 3SG sends Select Buffer A (R7), 100 MB Mode (R8), and Advance Address (R6) to the 3SA0. The 3SG option then receives the block length from the 3SA0 and holds the block length of the active transfer.

3SA0 - The 3SA0 receives Select Buffer A (I12) and 100 MB Mode (I13) and reads out the address and block length. The Advance Address (I11) shifts the address and block length to the output which is sent prior to each Address Ready. The address and block length (R0 - 15) are sent 16 bits at a time with 4 bits of parity (R16 - 19) to the mainframe or SSD. The 3SA0 reads out the block length (R20 - 27) 8 bits at a time to the 3SG. Refer to Tables 5-2 and 5-3 for the address and block length to the device.

5. Clear Buffer and Parameter Select. These signals are sent together to clear the buffer board, to select the correct pointer, and to select buffers 0 - 16.

   3SG - When the Address Ready sequence begins, the 3SG sends Clear Buffer (R3) and Parameter Select (R4) to the 3SO. The Parameter Select is serial data for the buffer board. The first 4 bits are buffers select 0 - 16 and the fifth bit is pointer select A or B.

   3SO - The 3SO passes Clear Buffer (R70) and Parameter Select (R71) to the buffer board.

6. Transmit Data. The Transmit Data is sent every time the input buffer can receive 16 words.

   3SG - After Transmit Address is dropped by the device, the 3SG sends Transmit Data to the mainframe or SSD. After the 3SG sends Transmit Data, the buffer board receives 16 words (64 bits and 8 CBs) one at a time. The 3SG then sends another Transmit Data for the next 16 words.

7. Data Ready. A Data Ready is sent with each word of data sent from the device.

   3SG - The Data Ready decrements the block length on the 3SG. It is then passed to the 3SO as Sample Data (R15) along with Parameter Select (R4).

8. Sample Data. The Sample Data is sent to the 3SO informing it that a word of data is to be written into the buffer.

   3SO - The 3SO sends Parameter Select (R71) to the buffer board after receiving Sample Data (I72) and Parameter Select (I71). The buffer board writes the word of data into the buffer and then increments the buffer address.

9. Last Word Flag. The Last Word flag is received when the device's block length equals zero.

3SO - The Last Word Flag (I4) is sent with the Data Ready when the device's block length equals zero. It is compared with the block length on the 3SG. If they do not equal zero at the same time, an unrecoverable error is flagged.

10. Done Flag. The Done flag sets when the transfer is complete.

    3SG - The Done flag is set if the block length equals zero, the 3SG has received the Last Word flag from the device, and the device has enabled Transmit Address.

11. Errors. The device reports parity errors (I47) on the address and double-bit single-error correction, double-error detection (SECDED) errors (I46).

High-speed Data Out

The following is a sequential description of a HISP data output sequence. Refer to Figure 5-3 for a HISP block diagram.

1. Go IOP Function. The IOP sends Go IOP Function to channels 10 - 13 or 14 - 17. After the Go IOP Function is received, the channel decodes the IOP Function Data. The IOP Function Data is the modifier bit that clock period and the command on the next clock period. If needed, for the next 4 CPs the IOP Function Data is the accumulator data.

    IOP - The 3AS sends Go IOP Function (R30) and the 3AQ sends IOP Function Data (R10 - 13) for channels 10 - 13. The 3AP sends Go IOP Function (R30) and the 3AO sends IOP Function Data (R10 - 13) for channels 14 - 17.

    3SK - After the 3SK decodes a command 0, it initiates the Clear Channel sequence. After a command 5, the 3SK initiates the Address Ready sequence.

    3SA1 - After receiving the CPU Output Control (Go IOP Function I4), the 3SA0 decodes the CPU Output Data (IOP Function Data I0 - 3). After a command 5 is decoded, the accumulator data is the block length, after a command 2 or 3 it is CPU address, and after a command 16 it is pointer select A or B and buffer bits 2^0 - 2^3.

2. Clear Channel. The Clear Channel clears the device and enables it to receive data.

    3SK - After command 0 is decoded on the 3SK and Transmit Address is not enabled, the 3SK starts the Clear Channel

sequence. If Transmit Address is enabled, the 3SG does not initiate Clear Channel (R0), but instead waits for a command 5 and then starts the Address Ready sequence.

3. Transmit Address. The device activates Transmit Address when it can accept the address and block length, and drops it after it has received three Address Readies.

   3SK - The 3SK accepts the Transmit Address (I20 - 21), and then sends Reset Address Channel to the 3SA1 and enables Address Ready to the device. If the previous transfer completed error free, Transmit Address would have already been enabled.

   3SA1 - The 3SA1 clears the address readout counter after receiving Reset Address Channel (I10) from the 3SK.

4. Address Ready. The Address Ready informs the device that the IOP is sending the address and/or block length, and it takes three Address Readies to get the address and block length to the device.

   3SK - The Address Ready sequence starts after a command 5 has been decoded and Transmit Address is enabled. The Address Ready sequence sends the Address Readies (R20) to the device. Prior to that, the 3SK sends Select Buffer A (R32), 100 MB Mode (R33), and Advance Address (R31) to the 3SA1. The 3SK also sends a HISP-Out Grab Block Length (R36), Clear Buffer (R25), and Parameter Select to the 3SO.

   3SA1 - The 3SA1 receives Select Buffer A (I12) and 100-Mbyte mode (I13) and reads out the address and block length (R0 - 19). The Advance Address (I11) shifts the address and block length to the output which is sent with each Address Ready. The address and block length (R0 - 15) are sent 16 bits at a time with 4 bits of parity (R16 - 19) to the device. The 3SA1 also reads out the block length (R20 - 27) 8 bits at a time to 3SO. Refer to Tables 5-2 and 5-3 for the address and block length to the device.

   3SO - The 3SO receives HISP-Out Grab Block Length (I18) and latches the block length from the 3SA1. The 3SO holds and decrements block length during the transfer.

5. Clear Buffer and Parameter Select. These signals are sent together to clear the buffer board, to select the correct pointer, and to select buffers 0 - 16.

3SK - When the Address Ready sequence begins, the 3SK sends Clear Buffer (R25) and Parameter Select (R26) to the 3SO. The Parameter Select is serial data for the buffer board. The first 4 bits are buffer select 0 - 16 and the fifth bit is buffer select A or B.

3SO - The 3SO passes Clear Buffer (R70) and Parameter Select (R71) to the buffer board.

6. Transmit Data. A Transmit Data is sent from the mainframe or SSD when it can accept 16 words of data from the IOP.

   3SK - After receiving Transmit Data (I22 - 23), the IOP is enabled to output data. The IOP continues to output data as long as the mainframe or SSD sends a Transmit Data for every 16 words.

7. Data Ready. A Data Ready is sent to the device with each word of data from the IOP.

   3SK - The 3SK sends Data Ready (R22) with each word of data, but the data is sent from the buffer board to the mainframe or SSD. The Data Ready is sent every 6 CPs in 200-Mbyte mode or every 12 CPs in 100-Mbyte mode. At the same time, the 3SK sends HISP-Out Decrement Block Length (R37), Parameter Select (R26), and Advance Data (R27) to the 3SO.

8. Parameter Select. The Parameter Select is sent to the buffer board to increment the address.

   3SO - The 3SO Parameter Select (I81) is ANDed with Advance Data (I82). It is then sent to the buffer board as Parameter Select (R81) to increment the buffer address while HISP-Out Decrement Block Length (I19) decrements the block length on the 3SO.

9. Last Word Flag. The Last Word Flag is sent when the block length on the 3SO equals zero.

   3SK - The Last Word Flag (R23) is sent to the device with the last Data Ready (R22) and the last word of data.

10. Done Flag. The Done Flag on the 3SK sets when the block length equals zero and Transmit Address is active. Transmit Address is activated by the device when all data is written into memory and no errors occurred.

11. Errors. The device reports parity errors (I47) on the address and double-bit SECDED errors (I46) on the data.

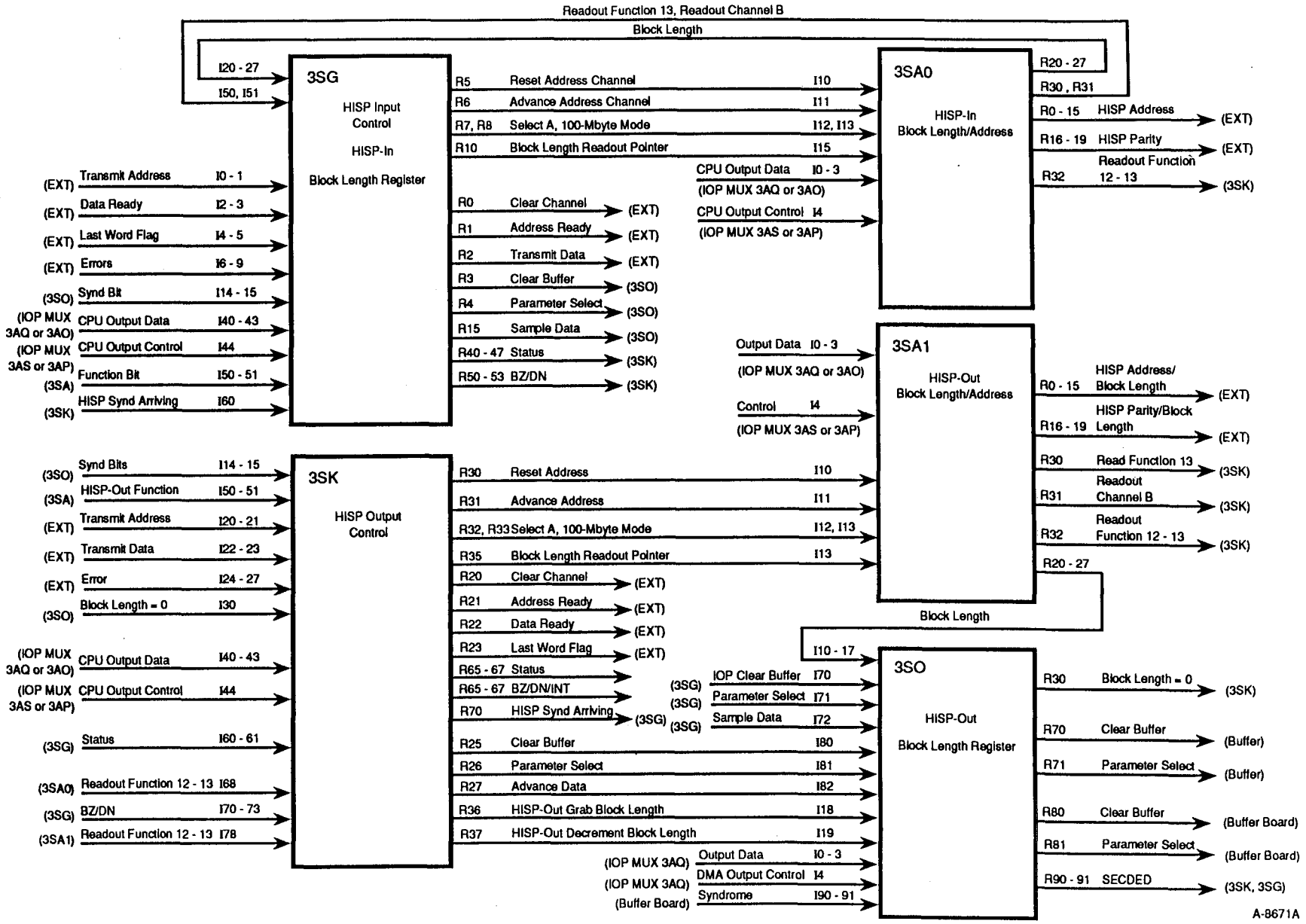


Figure 5-3. HISP MUX In/Out Block Diagram and Control

Table 5-2. CRAY Y-MP Address/Block Length

3SA	1st	2nd	3rd
R0	AD 2^{17}	BL 2^{12}	BL 2^{0}
R1	2^{18}	2^{13}	2^{1}
R2	2^{19}	AD 2^{0}	2^{2}
R3	2^{20}	2^{1}	2^{3}
R4	2^{21}	2^{2}	2^{4}
R5	2^{22}	2^{3}	2^{5}
R6	2^{23}	2^{4}	2^{6}
R7	2^{24}	2^{5}	2^{7}
R8	2^{25}	2^{6}	2^{8}
R9	2^{26}	2^{7}	2^{9}
R10	2^{27}	2^{8}	2^{10}
R11	2^{28}	2^{16}	2^{11}
R12	2^{29}	2^{10}	AD 2^{14}
R13	2^{30}	2^{11}	2^{15}
R14	2^{31}	2^{12}	——
R15	2^{9}	2^{13}	——

Table 5-3. Future Address/Block Length

3SA	1st	2nd	3rd	4th	5th
R0	AD 2^0	AD 2^4	AD 2^8	AD 2^{12}	AD 2^{16}
R1	2^1	2^5	2^9	2^{13}	2^{17}
R2	2^2	2^6	2^{10}	2^{14}	2^{18}
R3	2^3	2^7	2^{11}	2^{15}	2^{19}
R4	2^{20}	2^{24}	2^{28}	—	—
R5	2^{21}	2^{25}	2^{29}	—	—
R6	2^{22}	2^{26}	2^{30}	—	—
R7	2^{23}	2^{27}	2^{31}	—	—
R8	BL 2^0	BL 2^4	BL 2^8	BL 2^{12}	—
R9	2^1	2^5	2^9	2^{13}	—
R10	2^2	2^6	2^{10}	2^{14}	—
R11	2^3	2^7	2^{11}	2^{15}	—
R12	—	—	—	—	—
R13	—	—	—	—	—
R14	—	—	—	—	—
R15	—	—	—	—	—

Low-speed Protocol

The HCM LOSP can operate with 6-Mbyte LOSP protocol or 50-Mbyte mid-speed channel (MISP) protocol. The 6-Mbyte LOSP protocol is used with the CRAY Y-MP and the 50-Mbyte MISP protocol is used with the CRAY Y-MP16. The protocol is software selectable.

6-Mbyte Low-speed Protocol

The following is a description of 6-Mbyte LOSP protocol. Refer to Figure 5-4 for a LOSP protocol block diagram.

- Ready. The Ready is sent by the sender with each parcel of data. The Ready is a 50 ns pulse.

- Resume. The Resume is sent by the receiver to acknowledge Ready and to enable the next Ready. The Resume is a 50 ns pulse.
- Disconnect. The Disconnect is sent by the sender to terminate the transfer. The Disconnect is a 50 ns pulse.

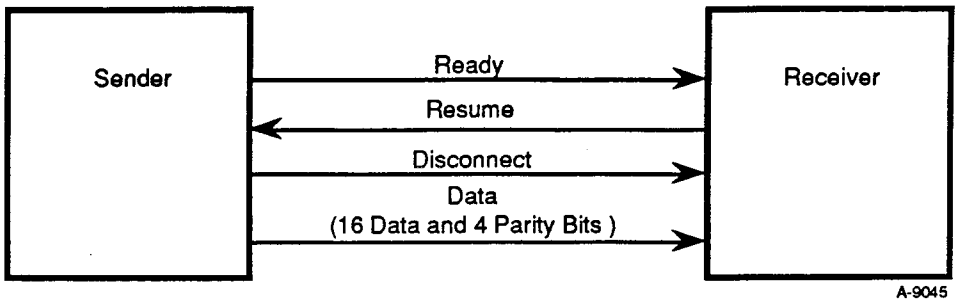


Figure 5-4. 6-Mbyte LOSP Protocol

50-Mbyte MISP Protocol

The following is a description of a 50-Mbyte MISP input and output protocol. Refer to Figure 5-5 for a MISP protocol block diagram.

- Ready. The sender sends 4 Ready pulses and 4 parcels of data. The Ready is a 18.5 ns pulse.
- Resume. A Resume is sent by the receiver to acknowledge the four Ready pulses and to enable the next four Readies. The Resume is a 18.5 ns pulse.
- Disconnect. The Disconnect is sent by the sender to terminate the transfer. The Disconnect is a 18.5 ns pulse.

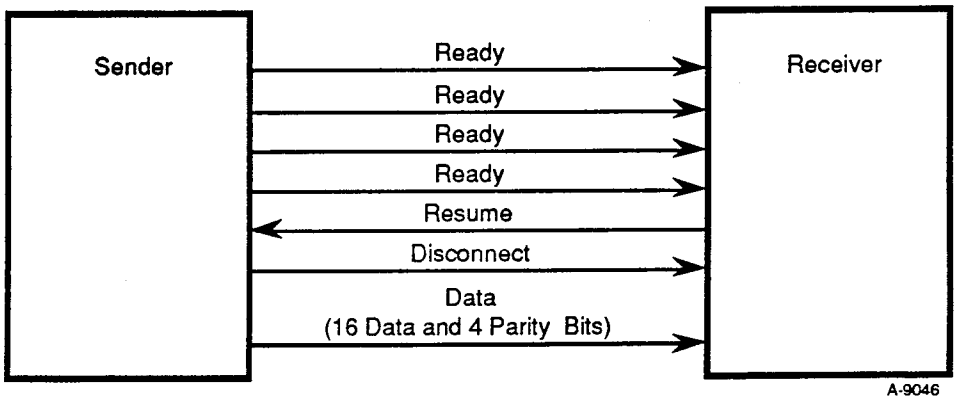


Figure 5-5. 50-Mbyte MISP Protocol

Low-speed Data In Sequence

The following is a sequential description of a LOSP data input sequence. Refer to Figure 5-5 for a LOSP block diagram.

1. Go IOP Function. The IOP sends Go IOP Function to channel 20. After Go IOP Function is received, the channel decodes the IOP Function Data. The IOP Function Data is the modifier bit that clock period and the command on the next. If needed, for the next 4 CPs the IOP Function Data is the accumulator data.

   IOP - The 3AS sends Go IOP Function (R31) and the 3AP sends IOP Function Data (R15 - 18) for channel 20.

   3SL - After receiving the CPU Output Control (Go IOP Function I44), the 3SL decodes the CPU Output Data (IOP Function Data I40 - 43). After a command 1 is decoded, the accumulator data is the parcel count. After loading the counter, the 3SL sets the busy flag and clears the done flag.

2. LOSP Ready. The mainframe sends LOSP Ready with each parcel of data.

   3SL - After 3SL receives the LOSP Ready (I0 - 1), it decrements the parcel counter, increments the buffer counter, and sends Capture LOSP-In (R1) to the 3SI. The buffer counter counts the number of parcels in the 3SI option's buffer.

3. Capture LOSP-In. The Capture LOSP-In latches the parcel of data on the 3SI.

   3SI - After the Capture LOSP-In (I41) latches the parcel of data, the 3SI shifts the data forward in the buffer and then sends Data Available to the 3SL. There is a 7-parcel input buffer on the 3SI. The 3SI checks the incoming data for parity. If a parity error (R24) is detected, it is reported to the 3SL.

4. LOSP Resume. A LOSP Resume is sent to the external device requesting the next parcel of data.

   3SL - The 3SL sends a 50 ns LOSP Resume (R0) pulse to the mainframe enabling it to send the next parcel of data. Perform steps 2 through 4 if the buffer is not full.

5. Data Available. When the 3SI has a parcel of data to output to the IOP MUX, it sends Data Available to the 3SL.

   3SL - After receiving Data Available (I5), the 3SL sends a request to the IOP MUX in the form of DMA Input Control (R40) at sync 0 or 3.

6. DMA Input Control. The 3SL sends DMA Input Control to the IOP MUX when it is requesting to write a parcel of data into local memory.

   3SL - When the 3SL sends DMA Input Control (R40) to the 3AS, it also sends Advance Out (R4) to the 3SI. The 3SL decrements the buffer counter with each DMA Input Control.

   3SI - The 3SI outputs a parcel data (R20 - 23) 4 bits at a time to the 3AS after receiving Advance Out (I44). The 3SI outputs bits 2^3 - 2^0, then bits 2^7 - 2^4, then 2^{11} - 2^8, and then bits 2^{15} - 2^{12}.

   3AS - The 3AS receives DMA Input Control (I34) from the 3SL and the data (I30 - 33) from the 3SI. (See Direct Memory Access (DMA) Local Memory Write Reference in the IOP quarter board section for a DMA write sequence.)

7. DMA Output Control. The IOP MUX acknowledges the DMA Input Control with a DMA Output Control.

   3SL - The 3SL receives DMA Output Control from the IOP MUX at sync 1 or 4. If Data Available is set, the 3SL sends another DMA Input Control to the IOP MUX. Perform steps 6 and 7 if Data Available is set.

8. Disconnect. The mainframe sends a Disconnect to the 3SL when it has completed its transfer.

   3SL - The Disconnect (I2 - 3) is how the mainframes ends the transfer, and it is sent by the mainframe when it receives a LOSP Resume with the block length equals zero.

9. Done Flag. The Done Flag sets after the 3SL receives a Disconnect or the parcel count on the 3SL equals zero.

   3SL - The 3SL sends the Busy and Done Flags to the IOP MUX (3AS or 3AP). When the parcel count equals one on the 3SL and it receives a LOSP Ready, the 3SL does not send a LOSP Resume which is the IOPs way of terminating the transfer.

10. Interrupt. An Interrupt (R43) is sent from the 3SL to the IOP MUX when the Done Flag sets and Channel Interrupt is enabled.

Low-speed Data Out Sequence

The following is a sequential description of LOSP data output sequence. Refer to Figure 5-6 for a LOSP block diagram.

1. Go IOP Function. The IOP MUX sends Go IOP Function to channel 21. After Go IOP Function is received, the channel decodes the IOP Function Data. The IOP Function Data is the modifier bit that clock period and the command on the next clock period. If needed, for the next 4 CPs the IOP Function Data is the accumulator data.

   IOP - The 3AS sends Go IOP Function (R31) and the 3AQ sends IOP Function Data (R15 -18) for channel 21.

   3SL - After receiving the CPU Output Control (Go IOP Function I4), the 3SL will decode the CPU Output Data (IOP Function Data I0 - 3). After the 3SL decodes a command 1, the 3SL sets the busy flag and clears the done flag.

2. DMA Output Control. The IOP MUX sends DMA Output Control to the 3SL and 3SO with each parcel of data.

   3SL - The 3SL receives DMA Output Control (I45) at sync 0 or 3 and then sends DMA Input Control (R40) at sync 1 or 4 if the LOSP-Out Buffer Full (I26) is not set. When channel 21 busy flag sets, the IOP MUX reads the first parcel of data out of local memory, and sends it to the 3SO along with DMA Output Control.

   3SO - The 3SO receives DMA Output Control (I4) and the parcel of data 4 bits at a time from the 3AO. Bits 2^3 - 2^0 arrives first, then bits 2^7 - 2^4, then 2^{11} - 2^8, and then 2^{15} - 2^{12}.

3. DMA Input Control. The 3SL sends a DMA Input Control to the IOP MUX requesting a parcel of data.

   3SL - If the LOSP-Out Buffer Full (I26) is not set and the output channel busy flag is set, the 3SL sends a DMA Input Control (R40) to the IOP MUX at sync 1 or 4. Perform steps 2 and 3 if the LOSP-Out Buffer Full is not set. (See DMA Read Reference in the IOP quarter board section for a DMA read sequence.)

4. Data Available. The Data Available is informing the 3SL that the 3SO has a parcel of data to output to the mainframe.

   3SL - The Data Available (I25) enables a LOSP Ready to the mainframe.

5. LOSP Ready. A LOSP Ready is sent to the mainframe with each parcel of data.

   3SL - The 3SL sends the 50 ns LOSP Ready pulse to the mainframe and a Go Output to LOSP (R24) to the 3SO.

   3SO - The 3SO outputs a parcel of data (R0 - 19) and 4 parity bits to the mainframe after receiving Go Output to LOSP (I6).

6. LOSP Resume. The mainframe sends LOSP Resume after it has saved the parcel of data and it can receive another parcel.

   3SL - After receiving the LOSP Resume (I20), the 3SL sends a LOSP Ready to the mainframe if Data Available is set. Perform steps 5 and 6 if Data Available is set.

7. Disconnect. The Disconnect is sent to the mainframe to terminate the transfer.

   3SL - The Disconnect (R21) is sent after the 3SL receives a LOSP Resume and a DMA output control at sync 2 or 5.

8. Done Flag. The Done Flag sets when the parcel count equals zero.

   3SL - When the 3SL receives a DMA Output Control (I45) at sync 2 or 5, the parcel count equals zero on the 3AL.

9. Interrupt. An Interrupt (R43) is sent from the 3SL to the IOP MUX when the Done Flag sets and the Channel Interrupt is enabled.

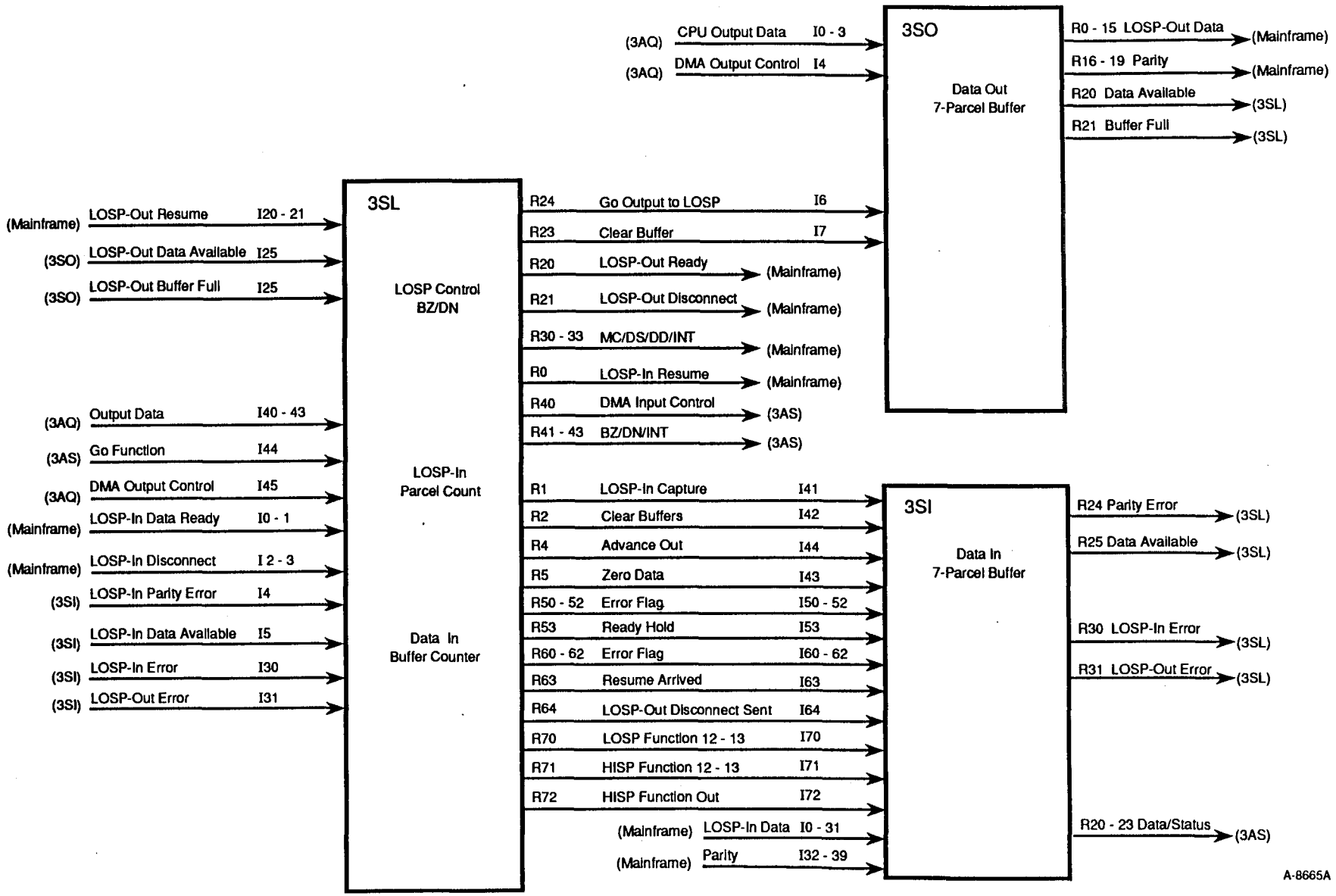


Figure 5-6. LOSP MUX In/Out Block Diagram and Control

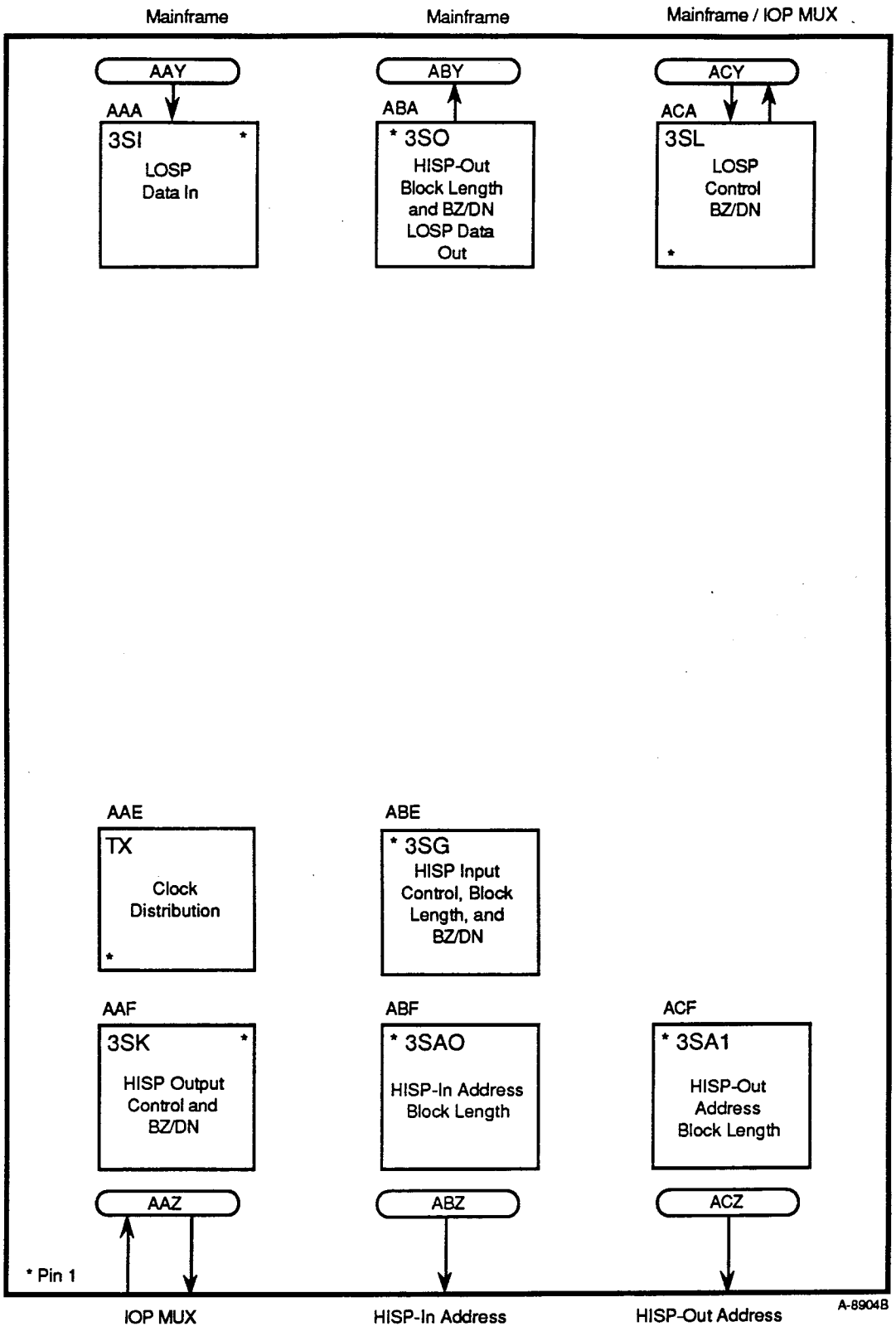


Figure 5-7. HCM Quarter Board Option Layout

6 CCA1 LOW-SPEED QUARTER BOARD

The CCA1 quarter board consists of the 3CA, 3CB, 3CC, 3YA, 3YB, and 3YC options. Refer to Table 6-1 for a functional description of CCA1 options. The CCA1 controls the data transfer between the I/O processor (IOP) and an external device with low-speed (LOSP) protocol or Networks System Corporation (NSC) protocol. Refer to Figure 6-6 for CCA1 option layout.

Table 6-1. CCA1 Options and Functional Descriptions

Option	Functional Description
3CA	Control between the IOP and the CCA1
3CB	Data in (1-parcel buffer) Data in control, busy, and done LOSP-In parcel count
3CC	Data out (1-parcel buffer) Data control, busy, and done LOSP-Out parcel count
3YA	Data interface for buffer board
3YB	Input buffer (1 word) Check parity and generate single-error correction, double-error detection (SECDED)
3YC	Output buffer (1 word) Check SECDED and generate parity

CCA1 Data Flow

Input data is transferred from the external device to the buffer board via 3CB, 3YB, and 3YA options. Refer to Figure 6-1 for a CCA1 input block diagram. Data is sent from the device one parcel per reference. The 3CB receives the parcel of data and parity bits and sends it to the 3YB. The 3YB checks the parity and generates SECDED as the parcels are assembled into a word. The word of data, along with check bits, is sent to the 3YA one parcel at a time. The 3YA outputs the data to the buffer board in a 12-bit transfer.

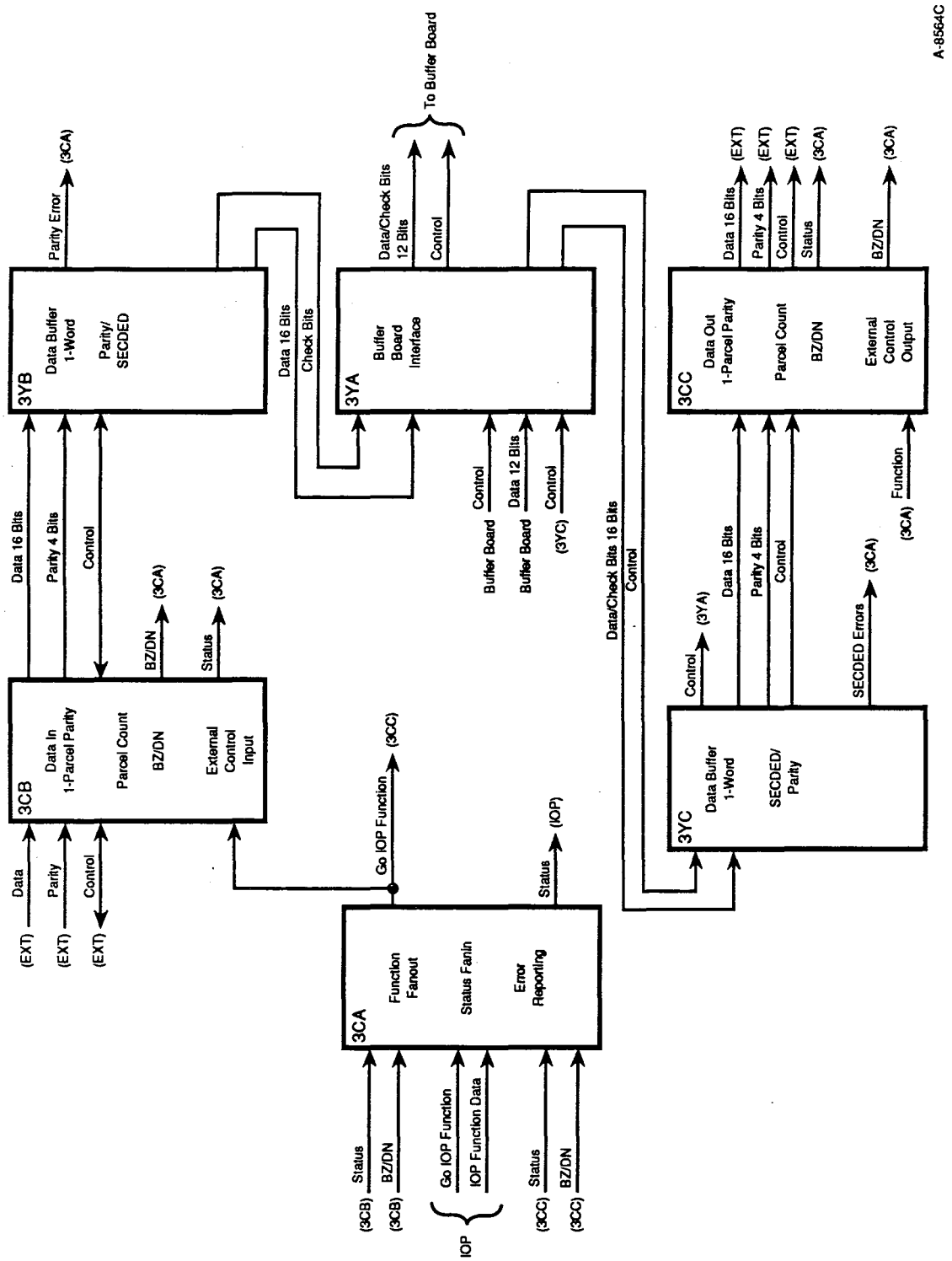


Figure 6-1. CCA1 Block Diagram

Output data is transferred from the buffer board to the 3YA, 3YC, 3CC options, and then to the external device. Refer to Figure 6-1 for an output block diagram. The buffer board outputs 1 word of data and check bits (CBs), 12 bits at a time to the 3YA. The 3YA sends the word of data to the 3YC. After the SECDED is performed and parity is generated on each parcel, the data and parity are sent to the 3CC. The 3CC sends the data to the external device one parcel per reference.

Low-speed Channel Protocol

The CCA1 can operate with 6-Mbyte LOSP channel protocol or 12-Mbyte NSC protocol. The protocol is software selectable.

6-Mbyte Low-speed Channel Protocol

The following is a description of 6-Mbyte LOSP channel protocol. Refer to Figure 6-2 for a LOSP channel protocol block diagram.

- Ready. The Ready signal is sent by the sender with each parcel of data. The Ready is a 50 ns pulse.
- Resume. The Resume signal is sent by the receiver to acknowledge the Ready and to enable the next Ready. The Resume is a 50 ns pulse.
- Disconnect. The Disconnect signal is sent by the sender to terminate the transfer. The Disconnect is a 50 ns pulse.

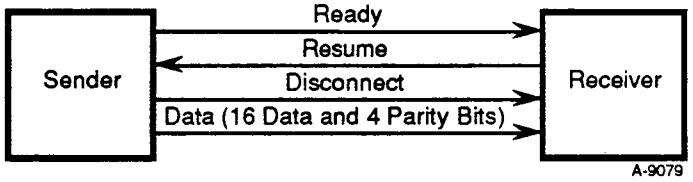


Figure 6-2. 6-Mbyte LOSP Channel Protocol

12-Mbyte Networks System Corporation Input Protocol

The following is a description of 12-Mbyte NSC input protocol. Refer to Figure 6-3 for an NSC protocol block diagram.

- Resume. The CCA1 sends four Resume signals to enable the device to send four Readies with 4 parcels of data. The Resume is a 50 ns pulse.

- Ready. The sender sends four Ready signals and 4 parcels of data. The Ready is a 50 ns pulse.
- Disconnect. The Disconnect signal is sent by the sender to terminate the transfer. The Disconnect is a 50 ns pulse.

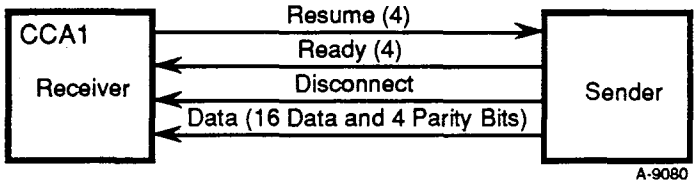


Figure 6-3. 12-Mbyte NSC Input Protocol

12-Mbyte Networks System Corporation Output Protocol

The following is a description of a 12-Mbyte NSC output protocol. Refer to Figure 6-4 for a NSC protocol block diagram.

- Ready. The CCA1 sends four Ready signals and 4 parcels of data. The Ready is a 50 ns pulse.
- Resume. A Resume signal is sent by the receiver to acknowledge the four Ready pulses and to enable the next four Readies. The Resume is a 50 ns pulse.
- Disconnect. The Disconnect signal is sent by the CCA1 to terminate the transfer. The Disconnect is a 50 ns pulse.

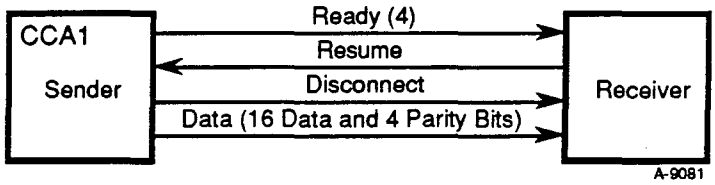


Figure 6-4. 12-Mbyte NSC Output Protocol

CCA1 Low-speed Channel Data In Sequence

The following is a sequential description of a low-speed data in transfer. Refer to Figure 6-5 for a functional block diagram of a low-speed in transfer.

1. Go IOP Function. The IOP sends Go IOP Function to a specific channel pair, and after the channel pair receives the signal, it decodes the IOP Function Data. The IOP Function Data is the modifier bits for this clock period and the command on the next

clock period. If needed, for the next 4 clock periods (CPs), the IOP Function Data is the accumulator data.

IOP - The 3AS option sends Go IOP Function (R33 or R34) and the 3AQ option sends IOP Function Data (R25 - 28 or R30 - 33) for channels 30 - 31 and 34 - 35. The 3AP option sends Go IOP Function (R33 or R34) and the 3AO option sends IOP Function Data (R25 - 28 or R30 - 33) for channels 32 - 33 and 36 - 37. The IOP Function Data is sent to the CCA1 four bits at a time. Refer to Section 5, "Direct Memory Access Function Sequence", for a complete Go IOP Function and IOP Function Data description.

3CA - The 3CA option receives Go IOP Function (I4), decodes IOP Function Data (I0 - 3), and fans out Go IOP Function (R12) and IOP Function Data (R8 - 11) to the 3CB and 3CC options.

3CB - The 3CB option receives Go IOP Function (I48) and decodes the IOP Function Data (I44 - 47). After Command 5 is decoded, the IOP Function Data is the parcel count for the next 4 CPs. The Busy Flag (R30) is set 1 CP after bits 2^{15} - 2^{12} of the parcel count are loaded.

2. Start a. The 3CA option sends a Start a to inform the 3YB option that the CCA1 is inputting data.

   3CA - The 3CA option sends Start a (R13) after it decodes a Command 5 for an even channel.

3. LOSP Ready. The external device sends a LOSP Ready with each parcel of data it sends to the 3CB option.

   3CB - A 50 ns LOSP Ready Pulse (I40 - 41) precedes each parcel of data (I0 - 31) and its 4 parity bits (I32 - 39). After the 3CB option has latched the data, it sends a Go Parcel (R21) to the 3YB option. The LOSP Ready decrements the parcel count.

4. Go Parcel. The Go Parcel informs the 3YB option that the 3CB option is sending a parcel of data.

   3YB - The 3YB option receives the Go Parcel (I16) and the parcel address (I20 - 21) and saves the parcel of data. As the parcels of data are received, parity is checked and check bits are generated as the parcels are assembled into a word (64 bits).

5. LOSP Resume. A LOSP Resume is sent to the external device requesting the next parcel of data.

   3CB - After receiving a LOSP Ready and sending a Go Parcel, the 3CB option sends a LOSP Resume (R20) to the external device. Perform steps 3 through 5 for each parcel of data received from the device.

6. Last Parcel of Word. The 3CB option sends the Last Parcel of Word to the 3YA option when it sends the fourth parcel of the word to the 3YB option.

   3CB - The Last Parcel of Word (R24) is sent when parcel address equals three. If parcel address is not equal to three when a Disconnect is received, the 3CB option zero fills the final parcel(s).

7. Go to Input Buffer. When the 3YA option can receive the word of data, it sends Go to Input Buffer to the 3YB option.

   3YA - The Go to Input Buffer (R19) is enabled by Last Parcel of Word (I36) and a sync 2 pulse.

8. Start a Write. The Start a Write selects the a pointer, and is sent with each word transferred from the 3YB option to the 3YA option.

   3YB - The 3YB option sends a Start a Write (R32) and one word of data (R0 - 15) with check bits (R16 - 19) after receiving Go to Input Buffer (I23).

9. Go a or Go b to I/O. The Go a or Go b to I/O sets the buffer board in the read or write mode and increments the address.

   3YA - After the 3YA option receives a Start a Write (I37) (the CCA1 is inputting data), it sends a Go b to I/O (R18) at sync 2. The Go b to I/O puts the buffer board in a write and b read mode and is sent once at the beginning of the transfer. The Go a to I/O (R17) at sync 3 informs the buffer board that a word of data (R20 - 31) is being sent to the a pointer and increments the address. The Go a to I/O at sync 3 is sent with each word of data. Twelve data and check bits are sent to the buffer board at a time. Perform steps 6 through 9 for each word of data. If the parcel count equals zero, go to Step 11.

10. Disconnect. The external device sends a Disconnect to the 3CB option when the transfer is complete.

    3CB - The Disconnect (I42 - 43) is the external devices way of ending the transfer.

11. Done Flag. The Done Flag is set after the 3CB option receives a Disconnect or the parcel count equals zero.

    3CA - If the IOP receives a LOSP Ready with the parcel count equal to one, it does not send a LOSP Resume, which is how the IOPs terminate the transfer. The set Done Flag on the 3CB option is detected by the 3CA (I14) option.

12. Interrupts. An Interrupt (R7) is sent from the 3CA option to the IOP when the Done Flag sets and the Channel Interrupt is enabled.

CCA1 Low-speed Channel Data Out Sequence

The following is a sequential description of a low-speed data out transfer. Refer to Figure 6-5 for a functional block diagram of a low-speed out transfer.

1. Go IOP Function. The IOP sends Go IOP Function to a specific channel pair, and after the channel pair receives the signal, it decodes the IOP Function Data. The IOP Function Data is the modifier bits this clock period, and the command on the next clock period. If needed, the next 4 CPs of the IOP Function Data is the accumulator data.

   IOP - The 3AS option sends Go IOP Function (R33 or R34) and the 3AQ option sends IOP Function Data (R25 - 28 or R30 - 33) for channels 30 - 31 and 34 - 35. The 3AP option sends Go IOP Function (R33 or R34) and the 3AO option sends IOP Function Data (R25 - 28 or R30 - 33) for channels 32 - 33 and 36 - 37. The IOP Function Data is sent to the CCA1 four bits at a time. Refer to Section 5, "Direct Memory Access Function Sequence", for a complete Go IOP Function and IOP Function Data description.

   3CA - The 3CA option receives Go IOP Function (I4), decodes IOP Function Data (I0 - 3), and fans out Go IOP Function (R12) and IOP Function Data (R8 - 11) to the 3CB and 3CC option.

3CC - The 3CC option receives Go IOP Function (I48) and decodes the IOP Function Data (I44 - 47). After a Command 5 is decoded on an odd channel, the IOP Function Data (I44 - 47) is the parcel count for the next 4 CPs. The Busy Flag (R30) sets 1 CP after bits 2^{15} - 2^{12} of the parcel count are loaded.

2. Clear and Start b Read. The Clear signal clears the pointer and Start b Read signal selects b pointer.

   3CA - The 3CA option sends Clear and Start b Read (R14) after it decodes a Command 5 for the odd channel.

3. Go a or Go b to I/O. The Go a or Go b to I/O sets the buffer board in read or write mode and increments the address.

   3YA - The 3YA option sends a Go b to I/O at sync 2 to the buffer board after receiving Start b Read (I15). The Go b to I/O at sync 2 sets the buffer board in a write and b read mode. The buffer board is now reading out the correct b pointer word. The 3YA saves it at the proper sync time. The data and CBs are received 12 bits (I0 - 11) at a time. Then a Go b to I/O at sync 3 is sent to the buffer board to increment the b pointer address. From now on when the 3YA receives a Read Data Empty (I12) from the 3YC option, it saves the next word of data and then sends a Go b to I/O at sync 3 to increment the b pointer address.

4. Go to Output Buffer. The 3YA option outputs a word of data and Go to Output Buffer to the 3YC option.

   3YC - The 3YC option receives Go to Output Buffer (I16) with four parcels of data and CBs. The data and CBs are sent 16 bits (I0 - 15) at a time for the next 5 CPs. The 3YC performs SECDED and then generates parity for each parcel. If there is a SECDED error (R24 - 25), it is reported to the 3CA (I20 - 21) option.

5. Output Data Available. The Output Data Available is informing the 3CC option that the 3YC option has a parcel of data ready.

   3CC - The 3CC option saves the parcel (I0 - 15) and its 4 parity bits (I16 - 19) after receiving Output Data Available (I43).

6. Ready. When the 3CC option has a parcel of data to output, it sends Ready to the external device.

   3CC - The 3CC option sends a 50 ns Ready to the external device along with a parcel of data (R0 - 15) and 4 parity bits (R16 - 19).

7. Resume. The external device sends a Resume after it has saved the parcel of data and can receive another parcel.

   3CC - After receiving the Resume (I20), the 3CC option decrements the parcel count and sends Go Parcel to Output Buffer (R24) to the 3YC option.

8. Go Parcel to Output Buffer. The 3CC option sends Go Parcel to the 3YC option requesting the next parcel.

   3YC - The Go Parcel to Output Buffer (I20) acknowledges Data Available and enables the next parcel. Perform steps 5 through 8 until the parcel count equals zero.

9. Data Request. When the 3YC option buffer is empty it sends a Data Request to the 3YA option for the next word.

   3YA - The 3YA option sends a Go to Output Buffer (R16) and 4 parcels of data to the 3CC option after receiving a Data Request (I12). Perform steps 3 through 9 until the parcel count equals zero.

10. Disconnect. The Disconnect is sent to the external device when the the IOP wants to terminate the transfer.

    3CC - The Disconnect (R21) is sent after the 3CC option receives a Resume with the parcel count equal to zero.

11. Done Flag. The Done Flag sets when the parcel count equals zero on the 3CC option.

    3CA - The Done Flag on the 3CC option is detected by the 3CA (I14) option.

12. Interrupts. An Interrupt (R7) is sent from the 3CA option to the IOP when the Done Flag sets and the Channel Interrupt is enabled.

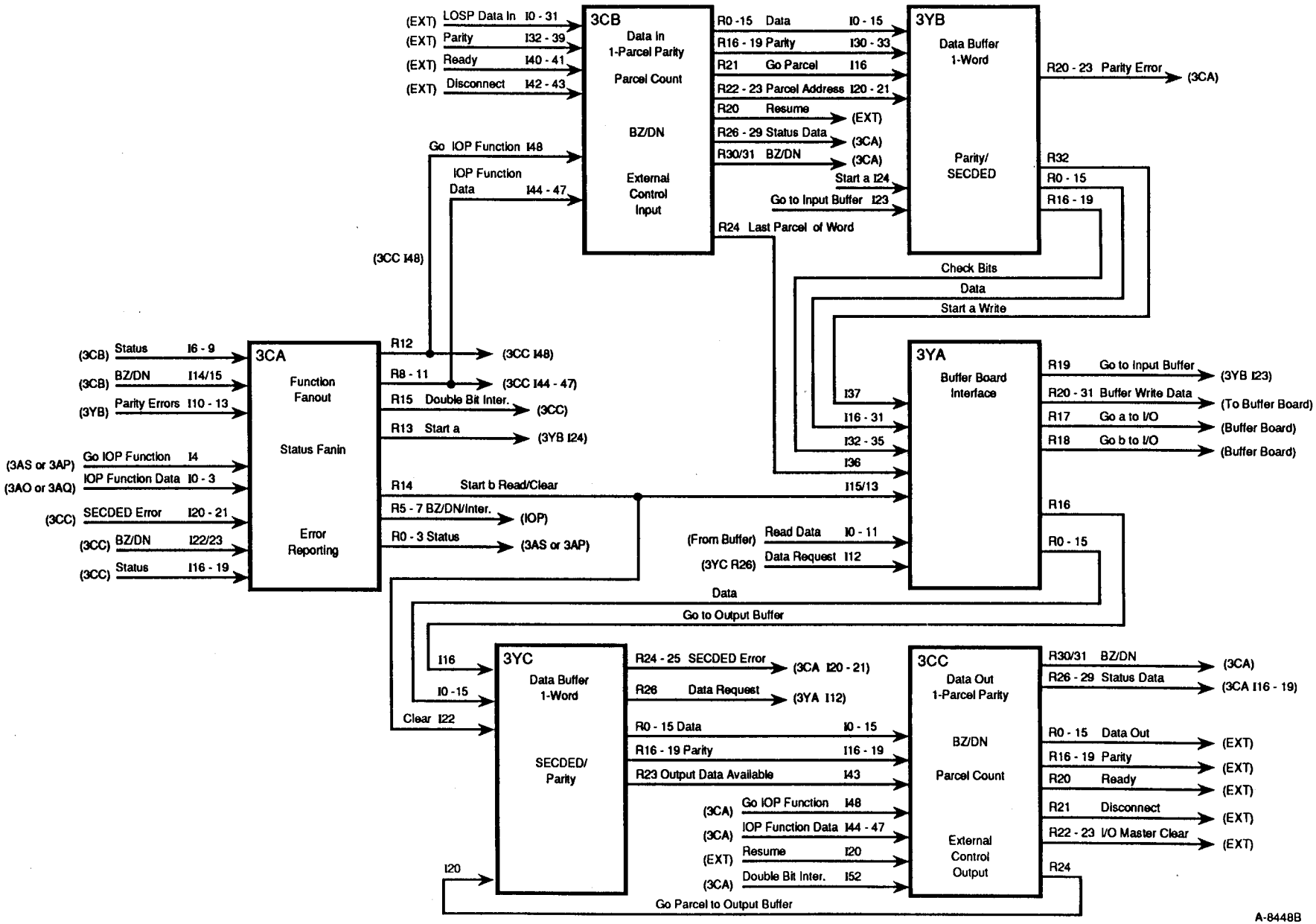


Figure 6-5. CCA1 Block Diagram and Control

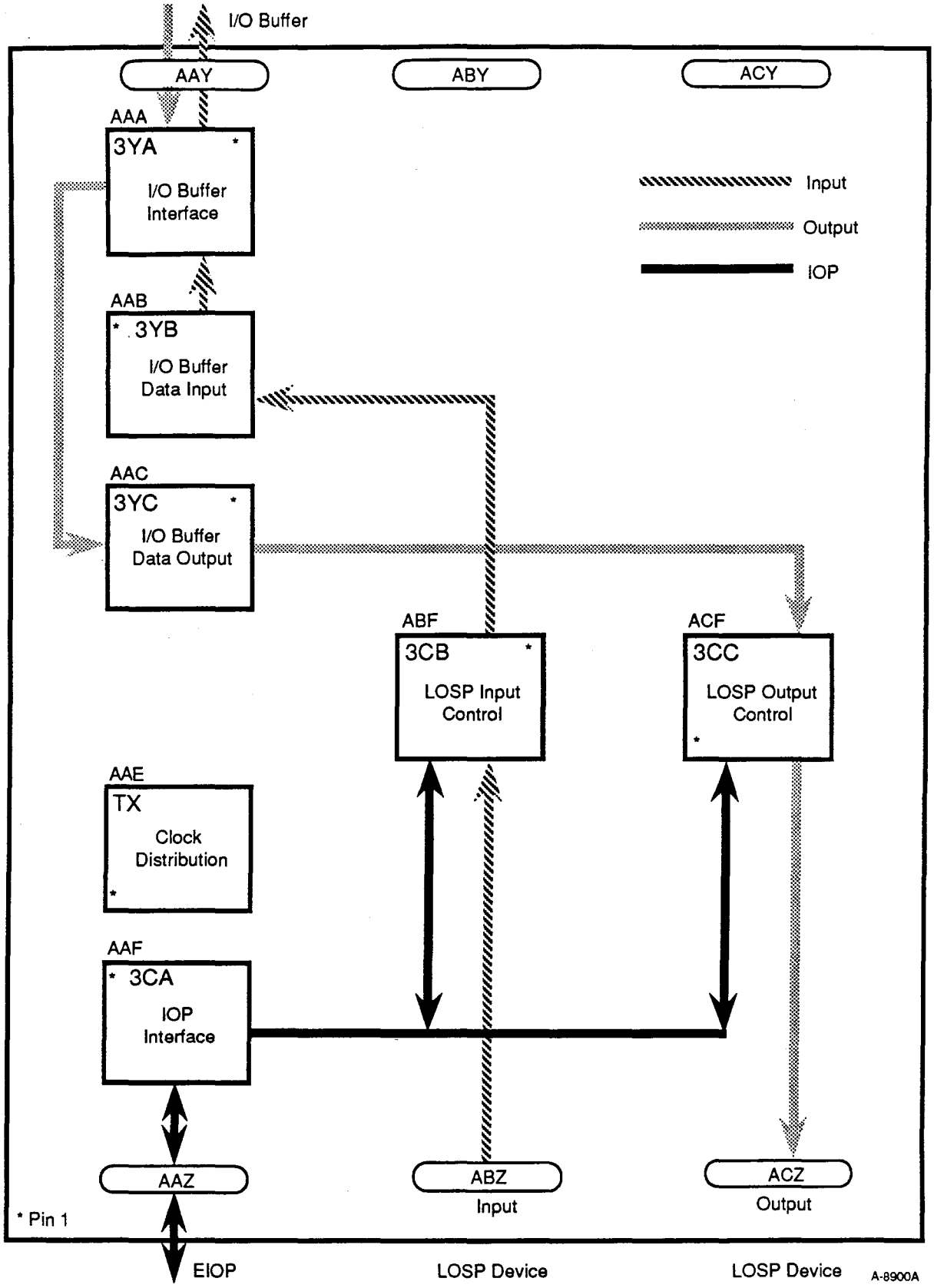


Figure 6-6. CCA1 Quarter Board Integrated Circuit Layout

7 DCA1 DISK DRIVE QUARTER BOARD

The DCA1 controls data transfers between the I/O processor (IOP) and the DD-49, DD-39, or DD-40. The DCA1 quarter board consists of the 3DA, 3DB, 3DC, 3YA, 3YB, and 3YC options. Refer to Table 7-1 for a functional description of DCA1 options. Refer to Figure 7-3 for DCA1 quarter board layout.

Table 7-1. DCA1 Options and Functional Descriptions

Option	Functional Description
3DA	Control between the IOP and the DCA1 Sector counter
3DB	External input control Bus In Parcel count register Status registers
3DC	External output control Bus Out Parcel count register Parameter register
3YA	Data and control interface for buffer board
3YB	Input buffer (1 word) single-error correction, double-error detection (SECDED) generation
3YC	Output buffer (1 word) error correction

DCA1 Data Flow

The input data flows as follows: from the disk drive, to the 3DB, 3YB, 3YA options, to the buffer board. The data is received from the disk drive in 16-parcel bursts. The 3DB receives the parcel of data and the parity bit, and sends it to the 3YB. The 3YB checks the parity and assembles the parcels into a word. SECDED is generated on each word of data. The word of data and check bits (CBs) are then sent to the 3YA a parcel at a time. The 3YA sends the data and CBs to the buffer board in 12-bit transfers. Refer to Figure 7-1 for DCA1 Input block diagram.

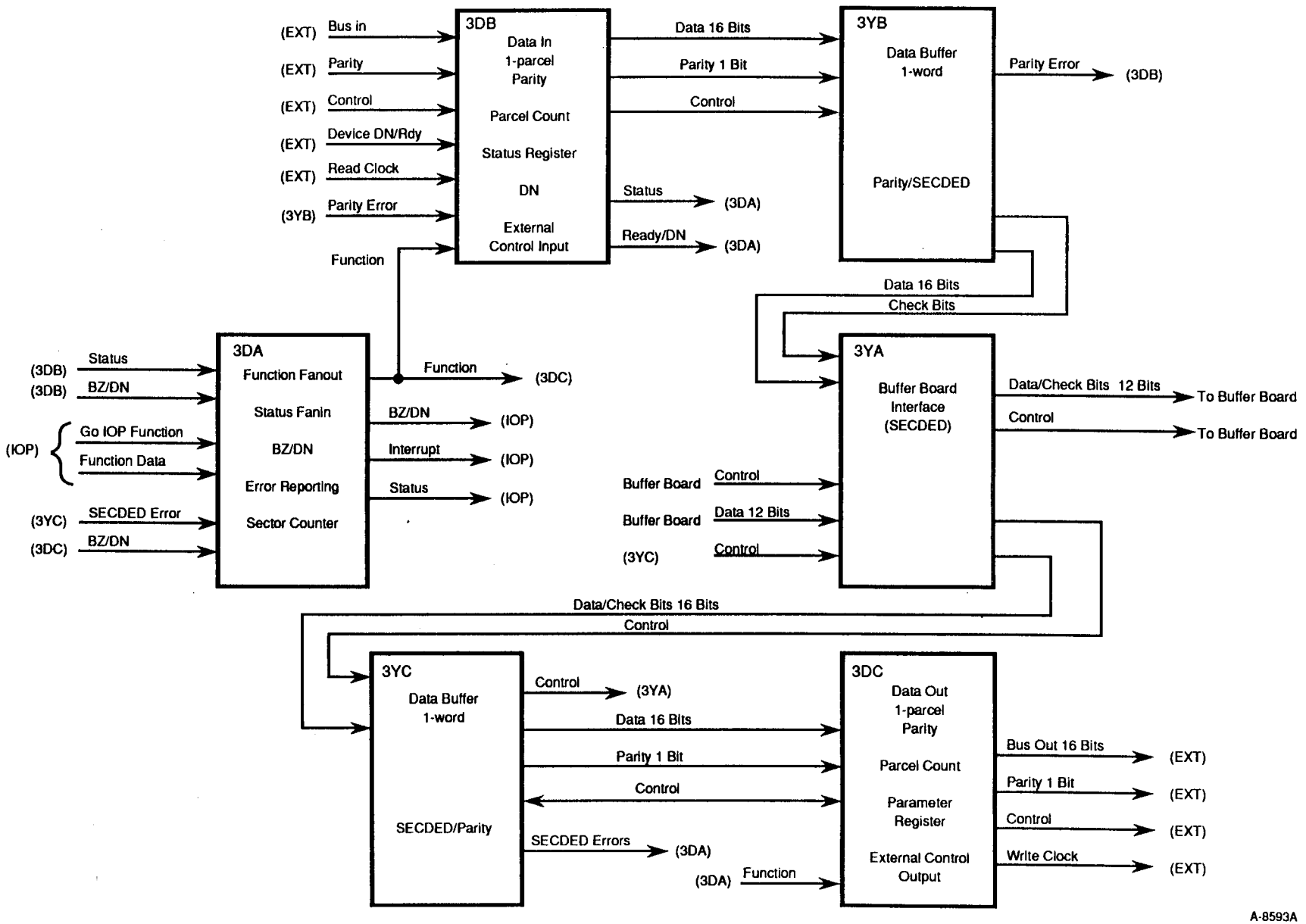


Figure 7-1. DCA1 Block Diagram

The output data flows from the buffer board to the 3YA, 3YC, and 3DC options, and then to the disk drive. The buffer board outputs 1 word of data 12 bits at a time to the 3YA. The 3YA sends the word of data to the 3YC where SECDED is performed, and parity is generated on each parcel. The 3YC sends the data to the 3DC. The 3DC sends the data to the disk drive one parcel at a time in a 16-parcel burst. Refer to Figure 7-1 for DCA1 output block diagram.

DCA1 Data In Sequence (Disk Drive Read)

The following is a sequential description of a DCA1 data in transfer. Refer to Figure 7-1 for a functional block diagram of a DCA1 data in transfer.

1. Go IOP Function. The IOP sends Go IOP Function to a specific channel pair, and after the channel receives the signal, it decodes the IOP Function Data. The IOP Function Data is the modifier bits this clock period and the command on the next clock period (CP). If needed, the next 4 CPs of the IOP Function Data is the accumulator data.

   IOP - The 3AS sends Go IOP Function (R33 or R34) and the 3AQ sends IOP Function Data (R25 - 28 or R30 - 33) for Channels 30 - 31 and 34 - 35. The 3AP sends Go Function (R33 or R34) and the 3AO sends IOP Function Data (R25 - 28 or R30 - 33) for Channels 32 - 33 and 36 - 37. The IOP Function Data is sent to the DCA1 four bits at a time. Refer to Section 5, Direct Memory Access Function Sequence, for a complete Go IOP Function and IOP Function Data description.

   3DA - The 3DA receives Go IOP Function (I5) and decode IOP Function Data (I0 - 4). The 3DA also fans out Go IOP Function (R24) and IOP Function Data (R20 - 23) to the 3DB and 3DC.

   3DC - The 3DC decodes IOP Function Data (I20 - 23) after receiving Go IOP Function (I24). After an IOP Command 5 is decoded, the 3DC sends a Function/Data Ready (R25) to the drive. The 3DC holds the drive parameter in the parameter register and sends it to the drive with Function/Data Ready. The parameter register must be loaded before a Command 5 is issued.

   3DB - The 3DB receives Go IOP Function (I24) and the IOP Function Data (I20 - 23) and decodes the modifier bits and command.

2. Start a or Start b. The 3DB sends a Start a or Start b to initialize the 3YB after an IOP Command 5 with a drive code of 2.

   3DB - A Start a (R30) or Start b (R31) is sent from the 3DB to the 3YB (I24 - 25). Start a is sent for an even channel and Start b is sent for an odd channel. On the DCA1, the channels can be both input and output.

3. Function/Data Ready. The 3DC sends a Function/Data Ready to the disk drive to inform the drive of data or function on the Bus Out.

   3DC - The drive detects whether it's a data or a function on the Bus Out (R0 - 15) by decoding Code Out (R20 - 24). A IOP Command 5 with a drive code of two is a read from the disk drive. The IOP hardware changes the Code Out to a six for the next Function/Data Ready signal.

4. Status/Data Ready. The disk drive sends Status/Data Ready for every 16 parcels it sends to the IOP.

   3DB - The 3DB receives Status/Data Ready (I90 - 91) with a Read Clock (I92 - 93). Each pulse of the Read Clock latches 1-parcel of data on the 3DB, and the data is sent in 16-parcel bursts. The Bus In (I40 - 71) has 1-bit of parity (I72 - 73) for each parcel of data.

5. Go Parcel. The Go Parcel precedes each parcel of data to the 3YB from the 3DB.

   3DB - The 3DB sends Go Parcel (R28), the parcel address (R20 - 21), the parcel of data (R0 - 15), and 1-bit of parity (R16) every time it receives a Read Clock (I92 - 93) and a disk read is being performed.

   3YB - The 3YB receives the Go Parcel (I16), the parcel address (I20 - 21), and a parcel of data. As the parcels of data are received, parity is checked and check bits are generated as the parcels are assembled into a word (64 bits).

6. Last Parcel of Word. When the parcel address equals three, the 3DB sends the Last Parcel of Word to the 3YA.

   3YA - The 3YA receives Last Parcel of Word (I36) and waits for sync +2, at which time it sends Go to Input Buffer (R19) to the 3YB.

7. Go Input Buffer. After the 3YA can receive a word of data, it sends Go Input Buffer to the 3YB.

   3YB - The 3YB outputs a word of data with a Start a or Start b Write after receiving Go Input Buffer (I23).

8. Start a or b Write. The 3YB responds back with Start a or Start b Write after receiving Go Input Buffer.

   3YB - The 3YB sends a Start a (R32) or Start b (R33) Write and 4 parcels of data (R0 - 15) along with check bits (R16 - 19). Start a Write is sent for the even channel and Start b Write is sent for the odd channel.

9. Go a or b to Input Buffer. The Go a or Go b to Input Buffer informs the buffer board which pointer to use, a or b, and if it is a read or a write.

   3YA - The 3YA sends Go a and/or b to Input Buffer (R17 and/or 18) and a word of data with check bits (R20 - 31) to the buffer board. The data is sent from the 3YA to the buffer board 12 bits at a time.

	Go a	Go b	
Sync+	2		Mode "a" read or "b" write
Sync+		2	Mode "a" write or "b" read

   One of the above is sent once at the beginning of the transfer to select the proper mode.

	Go a	Go b	
Sync+	3		Disk read ("a" write) even channel "a"
Sync+		3	Disk read ("b" write) odd channel "b"

   One of the above is sent with each word to the buffer board, writes data into the buffer, and increments the address.

10. Read/Write Resume. A Read/Write Resume is sent to the 3DC from the 3DB requesting the next 16 parcels of data.

    3DB - After a Status/Data Ready is received, the 3DB waits for the parcel count to equal 16 and sends a Read/Write Resume (R32) to the 3DC. The parcel count is incremented by the Read Clock pulse.

3DC - The 3DC sends Function/Data Ready (R25) to the disk drive after receiving the Read/Write Resume (I32). Perform steps 3 through 10 until a sector of data is transferred.

11. Done Flag. The Done Flag sets at the end of a sector of data and a Drive Done is received.

    3DA - The 3DB sends Done Flag (R44) to the 3DA and a Channel Adapter Done a or b to the 3DC and an Interrupt.

12. Interrupts. The 3DA sends an Interrupt to the 3AK when the Done Flag is set and if Channel Interrupt is enabled.

DCA1 Data Out Sequence (Disk Drive Write)

The following is a sequential description of a DCA1 data out transfer. Refer to Figure 7-1 for a functional block diagram of a DCA1 data out transfer.

1. Go IOP Function. The IOP sends Go IOP Function to a specific channel pair, and after the channel receives it, it decodes the IOP Function Data. The IOP Function Data is the modifier bits this clock period, and the command on the next clock period. If needed, the next 4 CPs of the IOP Function Data is the accumulator data.

    IOP - The 3AS sends Go Function (R33 or R34) and the 3AQ sends IOP Function Data (R25 - 28 or R30 - 33) for Channels 30 - 31 and 34 - 35. The 3AP sends Go Function (R33 or R34) and the 3AO sends IOP Function Data (R25 - 28 or R30 - 33) for Channels 32 - 33 and 36 - 37. The IOP Function Data is sent to the DCA1 four bits at a time. Refer to Section 5, Direct Memory Access Function Sequence, for a complete Go IOP Function and IOP Function Data description.

    3DA - The 3DA receives Go IOP Function (I5) and decode IOP Function Data (I0 - 4). The 3DA also fans out Go IOP Function (R12) and IOP Function Data (R20 - 23) to the 3DB and 3DC.

    3DC - The 3DC decodes IOP Function Data (I20 - 23) after receiving the Go IOP Function (I24). After the 3DC decodes IOP Command 5 it sends Function/Data Ready to the drive. The 3DC holds the drive parameters in the parameter register, and sends it to the drive with the Function/Data Ready. The parameter register must be loaded prior to a Command 5.

3DB - The 3DB also decodes IOP Function Data (I20 - 23), because it must know even or odd channels and if it is a read or a write.

2. Start a or Start b. The 3DC sends a Start a or Start b so the 3YA selects pointer a or b.

   3DC - After the 3DC decodes IOP Command 5 with a drive code of three, it sends a Start a or Start b Write (R30 or R31) to the 3YA and a Clear (R29) to the 3YA and 3YC. Start a Write is sent if an even channel was selected or Start b Write is sent if an odd channel was selected.

3. Go a or b to I/O. The Go a or Go b to I/O sets the buffer board in read or write mode and increment the address.

   3YA - The buffer board is always reading the present address of the selected pointer. The 3YA saves the first word of data from the buffer board at proper sync time after sending Go a or Go b to I/O at sync +2. The data is sent from the buffer board 12 bits at a time for the next 6 CPs.

	Go a	Go b	
Sync+	2		Mode "a" read or "b" write
Sync+		2	Mode "a" write or "b" read

One of the above is sent once at the beginning of the transfer to select the proper mode.

	Go a	Go b	
Sync+	3		Disk write (buffer read), even channel "a"
Sync+		3	Disk write (buffer read), odd channel "b"

One of the above is sent to the buffer board to increment the address.

4. Function/Data Ready. The Function/Data Ready informs the disk drive there is parameter or data on Bus Out.

   3DC - The Function/Data Ready (R25) is sent after the 3DC decodes an IOP Command 5. The drive decodes at Code Out (R20 - 24) to determine the request. After an IOP Command 5 with a drive code of 3 is decoded, a Function/Data Ready is sent and informs the disk drive there is function on the Bus Out followed by 16 parcels of data. The edge of the Write Clock (R26) latches the data or the parameter into the disk drive's data buffer. The Function/Data Ready is sent to the drive with each 16

parcels of data transfer. The drive responds back with Status/Data Ready when it can receive the next 16 parcels. After the Function/Data Ready with a code of 3, the 3DC forces the Code Out to 6 for the next Function/Data which means the data transfer will continue.

5. Go to Output Buffer. One word of data is transferred from the 3YA to the 3YC with each Go to Output Buffer.

   3YA - A Read Data Empty (I12) is sent from the 3YC to the 3YA. The 3YA sends Go to Output Buffer (R16) and 1 word of data to the 3YC after receiving Data Request. The first Go to Output Buffer is made by Start a or Start b Write from the 3DC.

   3YC - Four parcels of data and check bits are sent 16 bits (I0 - 15) at a time for the next 5 CPs after a Go to Output Buffer (I16) is received. The 3YC checks for SECDED errors and then generate parity on each parcel. If there is a SECDED error (R24 - 25) it is reported to the 3DA (I24 - 25).

6. Data Available. The 3YC sends Data Available to the 3DC with each parcel of data.

   3DC - The 3DC saves the parcel (I0 - 15) and its parity bit (I16) after receiving Data Available (I43).

7. Go Parcel. The 3YC receives a Go Parcel from the 3DC when the 3DC can accept the next parcel.

   3YC - The Go Parcel to Output Buffer (I20) and Output Data Available (R23) handshake each parcel until the parcel count equals zero. A Go Parcel to Output Buffer is sent to the 3YC for every pulse of the write clock.

8. Data Request. A Data Request is sent to the 3YA requesting the next word of the transfer.

   3YC - After 4 parcels have been transferred to the 3DC, the 3YC sends Data Request (R26) to the 3YA requesting the next word.

   3YA - The 3YA saves the next word from the buffer board and outputs it to the 3YC after receiving Read Data Empty The Read Data Empty (I12) and Go to Output Buffer (R16) handshake for each word transferred.

9. Status/Data Ready. The disk drive sends Status/Data Ready (I90 - 91) when it can accept the next 16 parcels of data.

   3DB - After the 3DB receives a Status/Data Ready on a disk write, it sends a Read/Write Resume (R32) to the 3DC.

10. Read/Write Resume. The Read/Write Resume is informing the 3DC that the drive has requested the next 16 parcels of data.

    3DC - After the 3DC receives a Read/Write Resume (I32), it sends a Function/Data Ready (R25) along with the Write Clock (R26) and 16 more parcels of data to the drive. Perform on steps 3 through 10 until a sector of data has been transferred.

11. Done Flag. The Done Flag on the 3DA sets after receiving Transfer Incomplete a or b and Done from the 3DB.

    3DB - The disk drive sends Drive Done (I82) to the 3DB and the 3DB passes it to the 3DA.

    3DA - The done signals sent from the 3DC and the 3DB are detected by the 3DA, and the Done Flag sets. The 3DA sends Channel Adapter a or b Done (R30 - 31) to the 3DC to acknowledge the Transfer Incomplete.

12. Interrupts. If the Channel Interrupt is enabled when the Done Flag sets, the 3DA sends an Interrupt to the IOP (3AK).

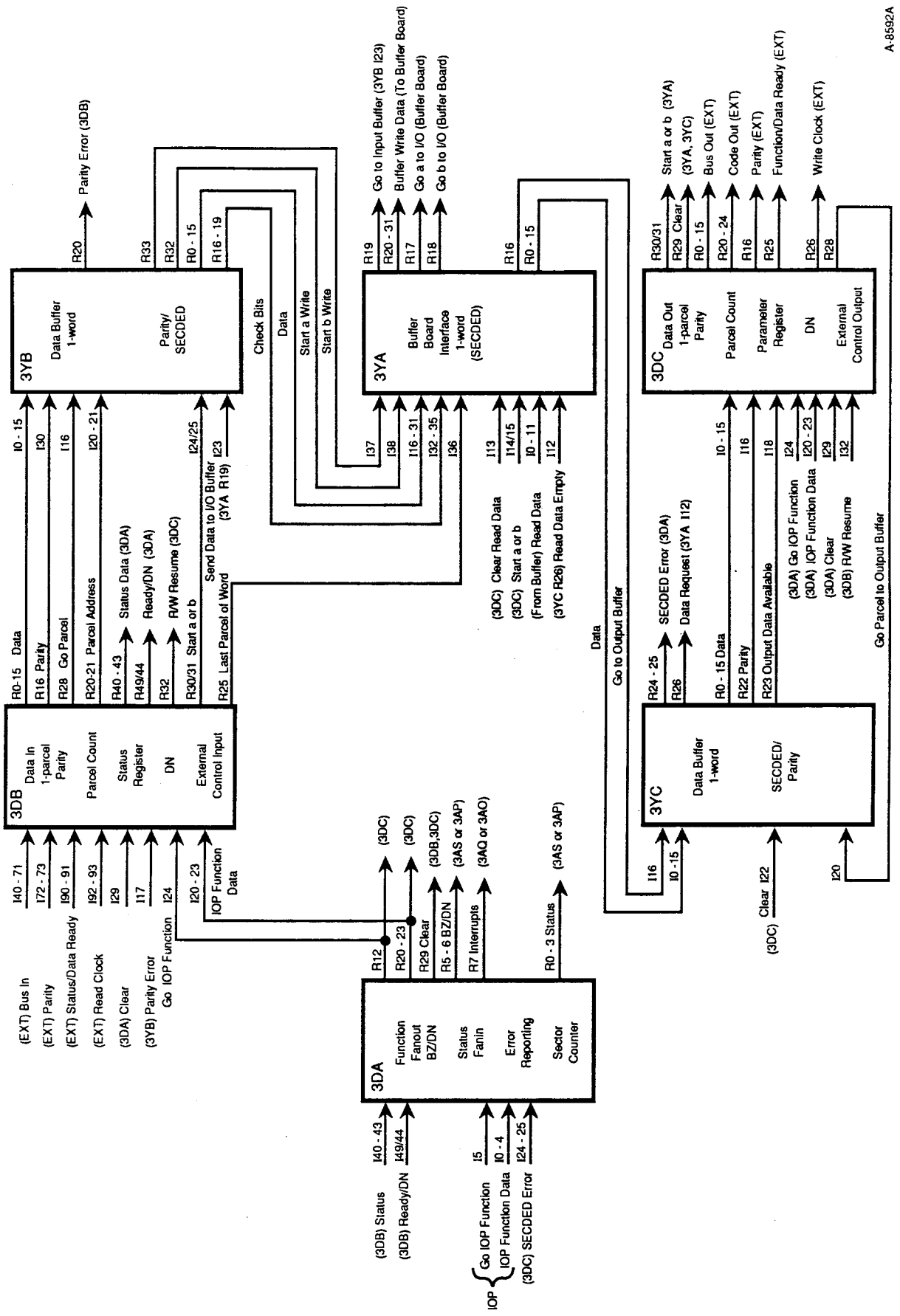


Figure 7-2. DCA1 Block Diagram and Control

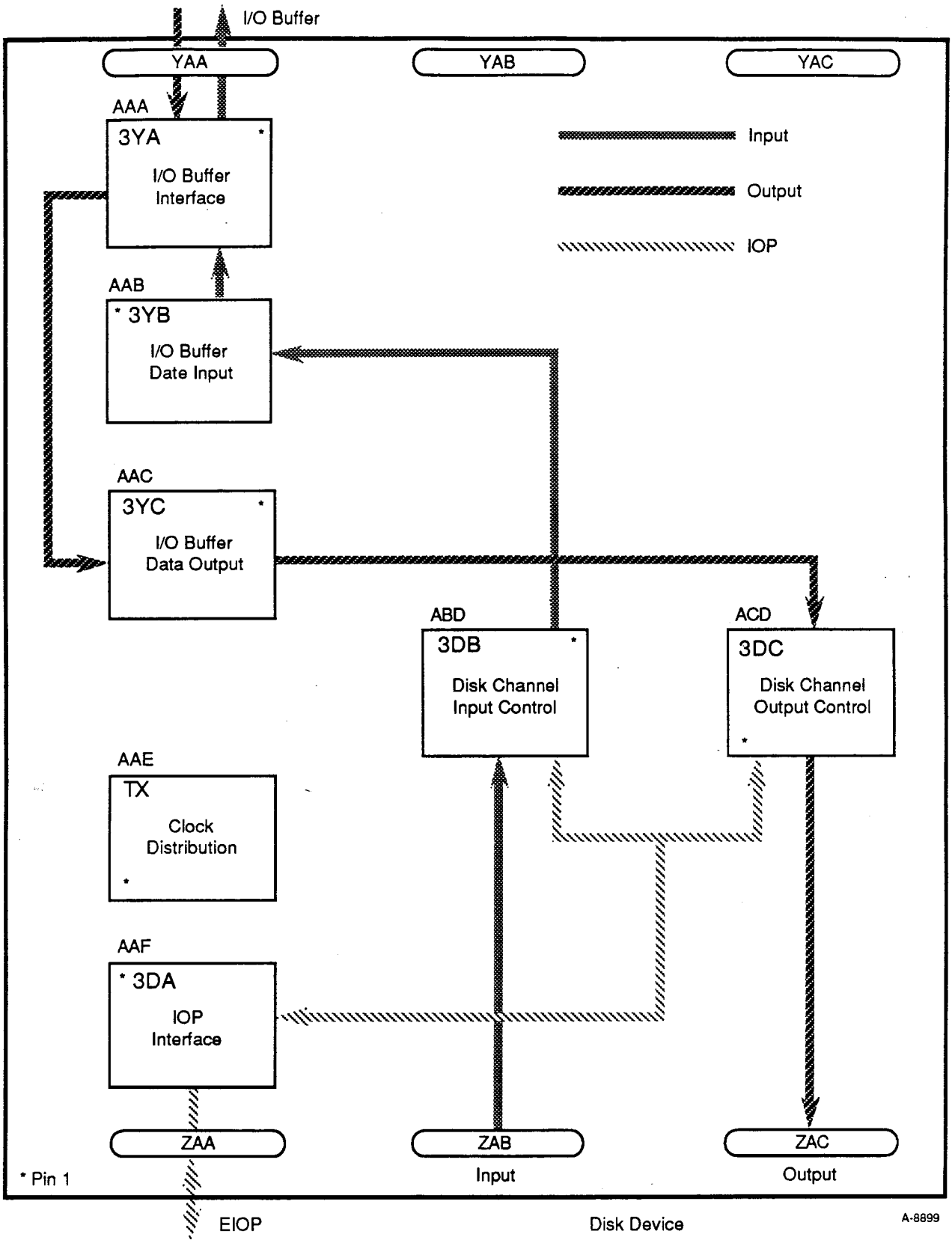


Figure 7-3. DCA1 Quarter Board IC Layout

8 DCA2 IPI DISK DRIVE CONTROLLER QUARTER BOARD

The DCA2 quarter board interfaces between the I/O processor (IOP) and an intelligent peripheral interface (IPI) type disk drive. The DCA2 simulates the IPI protocol with the use of the micro sequencer code. The micro sequencer code is stored on nine 761K x 4-bit random access memory (RAM) chips and is loaded via local memory. The IPI drives are nine head parallel or one head serial. The drives are dual ported and can be daisy chained. The DCA2 quarter board consists of the 3DD, 3DE, 3DF, 3DG, 3DH, 3DI, 3DJ, 3YA, 3YB, and 3YC options. Refer to Table 8-1 for a functional description of the DCA2 options. Refer to Fgure 8-4 for the DCA2 quarter board option layout.

Table 8-1. DCA2 Options and Functional Description

Option	Functional Description
3DD	IOP contol Error register Internal status register
3DE	External input control Bus in A and B
3DF	External output control Bus out A and B i, j, and k registers
3DG	ID compare Parcel and defect counters Parameter registers Cylinder register
3DH0	Data out 2^{11} - 2^{8}, 2^{3} - 2^{0} ECC generation and check
3DH1	Data out 2^{15} - 2^{12}, 2^{7} - 2^{4} ECC generation and check
3DI	Sequencer control Transfer counter Status register (initial and ending)
3DJ	Sequencer address
3YA	Buffer board interface
3YB	Input data buffer
3YC	Output data buffer

DCA2 Data Flow

The DCA2 inputs data to the buffer board via 3DE, 3YB, and 3YA. Refer to Figure 8-1 for a DCA2 block diagram. The 3DE receives data on the A and B buses. Each bus is 8 bits of data and 1 bit of parity. The 3DE checks for bus parity errors and then outputs the data and parity to the 3DG, 3DH and 3YB options. The 3DG option receives the ID parcels. The 3DH options use the data to generate the new Error Correction Code (ECC). The 3YB option checks the parity and assembles the data in a 64-bit word. The 3YB outputs the word of data and check bits to the 3YA option. The 3YA option outputs the data and check bits to the buffer board 12 bits per clock period (CP).

The DCA2 outputs data to the disk drive via the 3YA, 3YC, 3DH, and 3DF options. Refer to Figure 8-1 for a DCA2 block diagram. The 3YA receives the data and check bits from the buffer board 12 bits per clock

period. The data and check bits are then sent to the 3YC option. The 3YC performs single-error correction, double-error detection (SECDED) and then generates 1 bit of parity for each byte of data. The 3YC outputs a byte of data to each 3DH option. The 3DH options generate the ECC and then outputs the data to the 3DF option. The 3DF loads the data on the A and B buses and then outputs the data to the disk drive.

The micro sequencer code is written to the RAM via the 3DD and 3DI options. Refer to Figure 8-1 for a DCA2 block diagram. The 3DD receives the data from local memory (3AO or 3AQ options) 4 bits at a time. The 3DD then outputs the data to the 3DI. The 3DI generates a write enable and then sends the data to the RAM. The 3DJ option outputs the sequencer address.

For diagnostic purposes the micro sequencer code is read back to local memory via the 3DI and 3DD options. Refer to Figure 8-1 for a DCA2 block diagram. The 3DJ addresses the RAM. The RAM outputs the data to the 3DI. The 3DI sends the data to the 3DD 4 bits at time. The 3DD option sends the data to local memory (3AS or 3AP).

The DCA2 writes and reads the ID via the buffer board. Refer to Figure 8-1 for a DCA2 block diagram. The EIOP must write the ID to the buffer and then issue a write ID command to the DCA2. The buffer board outputs the ID to the 3YA. The ID is passed to the 3YC, 3DH, and 3DF options. The 3DF loads the ID on to the A and B buses. The disk drive reads the buses and writes the ID to the appropriate location.

The DCA2 reads the ID to the buffer board via the 3DE, 3YB, and 3YA options. Refer to Figure 8-1 for a DCA2 block diagram. The DCA2 issues a read ID command and then receives the ID on the A and B buses. The 3DE outputs the ID to the 3YB option. The 3YB passes the ID to the 3YA one word at a time. The 3YA option then passes the data to the buffer board. The EIOP reads the ID from the buffer board via channel 26.

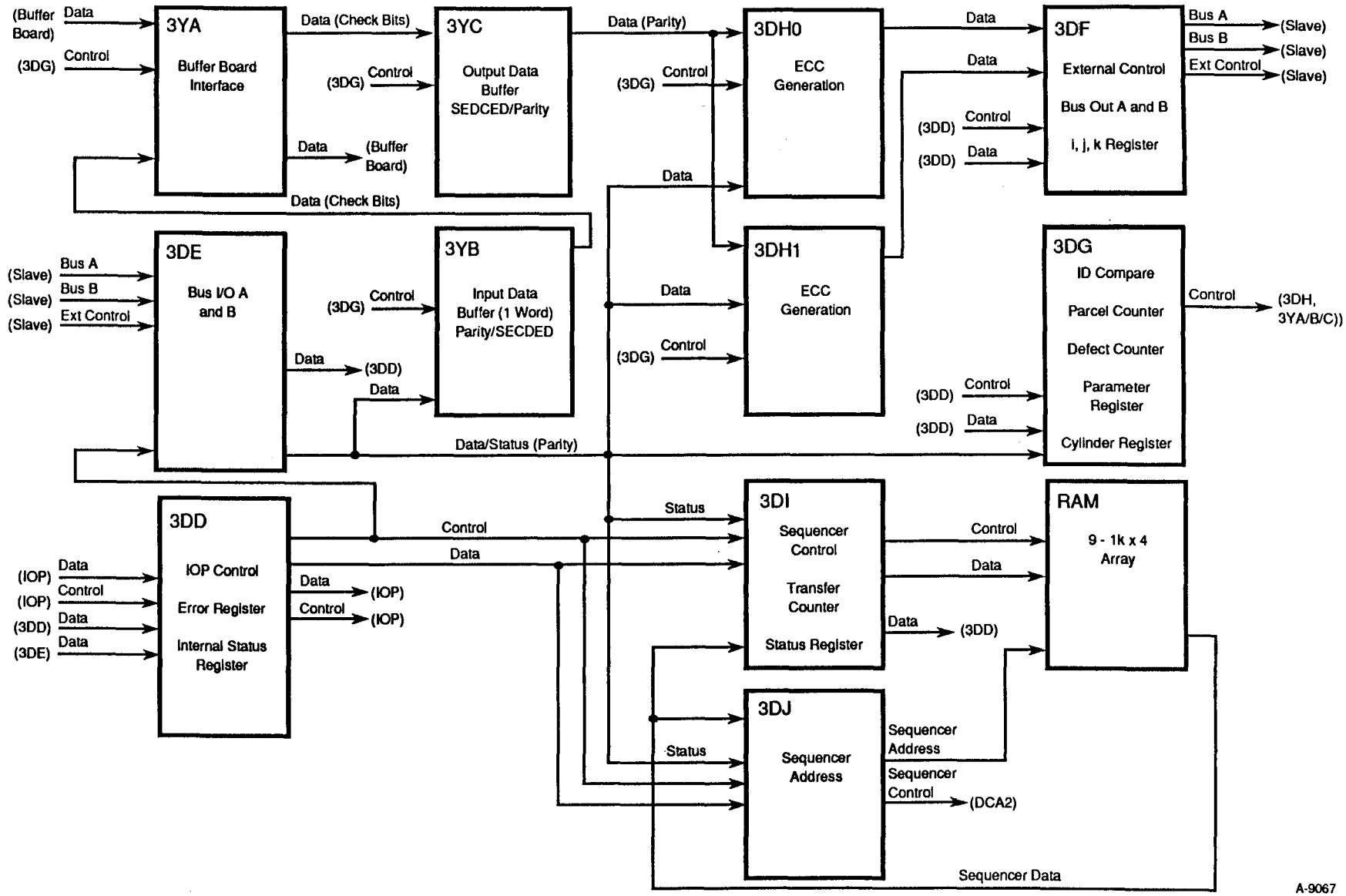


Figure 8-1. DCA2 Block Diagram

IPI Protocol

The following is a description of the DCA2 IPI protocol signals. Refer to Figure 8-2 for IPI block diagram.

- Select Out. The Select Out is asserted by the master to the slave (disk drives). It selects the disk drive with the use of the device address.
- Slave In. The Slave In is asserted by the slave to enable the master to output control or status. It is negated to terminate the transfer.
- Master Out. The Master Out is asserted by master to initiate the transfer, and negated to terminate the transfer.
- Sync In. The Sync In is asserted by the slave for data and control. On a disk write, the slave asserts Sync In when it can accept the data. On disk read, the slaves assert Sync In when there is valid data on the buses.
- Sync Out. The Sync Out is asserted by the master for data and control. On a disk write, the master asserts Sync Out when the master has valid data on the bus and Sync In is asserted. On a disk read, the master asserts Sync Out when the master can accept the next parcel of data.
- A and B Bus. The A and B buses are each 8-bit data buses with 1 bit of odd parity.
- Attention In. The Attention In is asserted by the slave when the slave needs service.

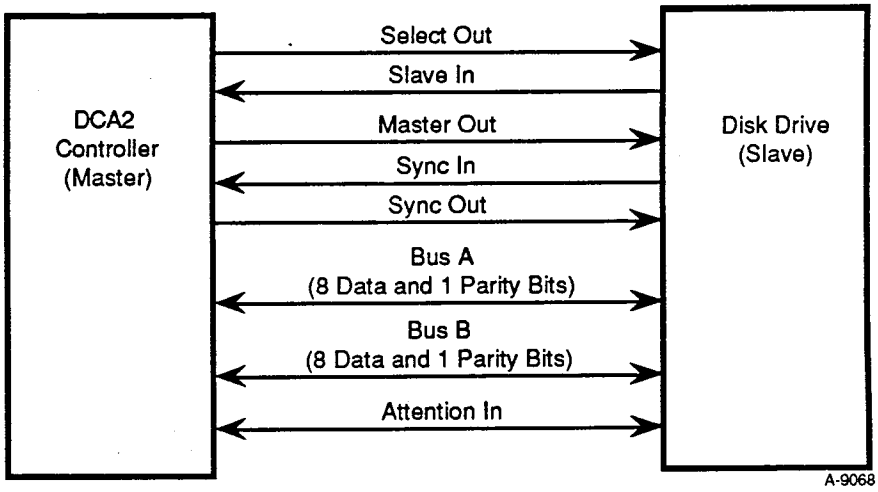


Figure 8-2. IPI Block Diagram

DCA2 Autoload Sequence

The following is a sequential description of a DCA2 micro sequencer code autoload. The DCA2 quarter board has nine 1K x 4 bit RAM arrays to hold the micro sequencer code. The micro sequencer code simulates IPI protocol for the DCA2. Refer to Figure 8-3 for a DCA2 block diagram.

1. Go IOP Function. The IOP sends Go IOP Function to a specific channel pair. When the channel receives the signal, it decodes the IOP Function Data. The IOP Function Data is the modifier bit this clock period and the command on the next clock period. If needed for the next 4 CPs, the IOP Function Data is the accumulator data.

   IOP - The 3AS option sends Go IOP Function (R33 or R34) and the 3AQ option sends IOP Function Data (R25 - 28 or R30 - 33) for channels 30, 31 and 34, 35. The 3AP option sends Go IOP Function (R33 or R34) and the 3AO option sends IOP Function Data (R25 - 28 or R30 - 33) for channels 32, 33 and 36, 37. The IOP Function Data is sent to the DCA2 4 bits at a time. The IOP sets the appropriate DMA busy flag and clears DMA done flag for the odd channel after decoding a command 1. When programming the DCA2 for an autoload (command 1), use the even channel on the DCA2 quarter board and the odd channel on the IOP board. Refer to Table 8-2 for the correct autoload instruction.

Table 8-2. DCA2 Autoload Instruction

Function	Channel	Instruction
Autoload	30, 31	141131
Autoload	32, 33	141133
Autoload	34, 35	141135
Autoload	36, 37	141137

3DD - The 3DD option receives the Go IOP Function (I4) and decodes the IOP Function Data (I0 - 3). After decoding a command 1 for the even channel, the DCA2 sets the busy flag and clears the done flag for the even channel and then waits for the local memory data. The 3DD sends the Go IOP Function (R14) and the Function Data (R10 - 13) to the 3DJ and 3DI options.

3DI - The 3DI option decodes a command 1 and sends a Reset Address (R80) to the 3DJ.

3DJ - The 3DJ option clears the sequencer address after receiving Reset Address (I80) from the 3DI and then outputs the address (R0 - 9) to the RAM.

2. DMA Output Control. The IOP sends a DMA Output Control with each parcel of local memory data.

IOP - After setting the busy flag, the IOP generates a local memory read request. The IOP outputs the DMA Output Control at sync 0 or 3 to the DCA2 after reading the parcel of data from local memory. The IOP generates the next local memory read request after receiving DMA Input Control at sync 1 or 4. When the parcel counter on the 3AL option equals zero, the IOP then sends a DMA Output Control at sync 2 or 5 to the 3DD option with the last parcel of data. Refer to Section 5, "DMA Local Memory Read Reference Sequence," for a complete local memory read reference sequence.

3DD - The 3DD option receives DMA Output Control (I5) and IOP Function Data (I0 - 3) from the IOP. The 3DD passes the DMA Control (R14) and IOP Function Data (R10 - 13) to the 3DI and 3DJ options.

3DI - The 3DI option generates the Write Enable (R0 - 8) and outputs 4 bits of Sequencer Data (R10 - 13) to the RAM. The 3DI sends an Advance Sequencer Address (R82) to the 3DJ after writing the 2 parcels of data into the RAM. Refer to Table 8-3 for the write data sequence.

Table 8-3. Sequencer Data

Parcel/Parity	Nibble	Sequence Bits	Write Enable
Parcel N	0	$2^{31} - 2^{28}$	R0
	1	$2^{27} - 2^{24}$	R1
	2	$2^{23} - 2^{20}$	R2
	3	$2^{19} - 2^{16}$	R3
Parcel N+1	4	$2^{15} - 2^{12}$	R4
	5	$2^{11} - 2^{8}$	R5
	6	$2^{7} - 2^{4}$	R6
	7	$2^{3} - 2^{0}$	R7
Parity	8	$2^{35} - 2^{32}$	R8

3DJ - The 3DJ option increments the address each time it receives an Advance Sequencer address (I80).

3. DMA Control. The 3DI sends a DMA Control (R44) to the 3DD requesting the next parcel of data.

4. DMA Input Control. The 3DD sends a DMA Input Control to the IOP requesting the next parcel of data.

   3DD - The 3DD option outputs a DMA Input Control (R4) to the IOP at sync 1 or 4 requesting the next parcel. If the 3DD received the previous DMA Output Control at sync 2 or 5 (disconnect), the 3DD sets the done flag. Perform steps 2 through 4 for each parcel of data.

5. Interrupt. The 3DD sends an Interrupt (R7) to the IOP when the done flag sets and the Channel Interrupt is enabled.

   IOP - When the parcel counter on the 3AL option equals zero, the IOP outputs a DMA Output Control at sync 2 or 5 to the 3DD option with the last parcel of data. Then the IOP sets the appropriate DMA done flag and clears the DMA busy flag.

   3DD - The 3DD sets the done flag and clears the busy flag after receiving the DMA Control (I5 - 4) from the 3DI if the 3DD received a DMA Output Control at sync 2 or 5 from the IOP.

DCA2 Autodump Sequence

The following is a sequential description of a DCA2 autodump. The DCA2 quarter board has nine 1K x 4-bit RAM arrays to hold micro sequencer code. The micro sequencer code simulates IPI protocol for the DCA2. For diagnostic purposes, the micro sequencer code is read to local memory (autodump). Refer to Figure 8-3 for a DCA2 block diagram.

1. Go IOP Function. The IOP sends Go IOP Function to a specific channel pair. When the channel receives the signal, it decodes the IOP Function Data. The IOP Function Data is the modifier bits that clock period and the command on the next clock period. If needed for the next 4 CPs, the IOP Function Data is the accumulator data.

   IOP - The 3AS option sends Go IOP Function (R33 or R34) and the 3AQ option sends IOP Function Data (R25 - 28 or R30 - 33) for channels 30, 31 and 34, 35. The 3AP option sends Go IOP Function (R33 or R34) and the 3AO option sends IOP Function Data (R25 - 28 or R30 - 33) for channels 32, 33 and 36, 37. The IOP Function Data

is sent to the DCA2 four bits at a time. The IOP sets the appropriate DMA busy flag and clears DMA done flag for the even channel after decoding a command 1. When programming the DCA2 for an autodump (command 1), use the odd channel on the DCA2 quarter board and the even channel on the IOP board. Refer to Table 8-4 for the correct autodump instruction.

Table 8-4. DCA2 Autodump Instruction

Function	Channel	Instruction
Autodump	30, 31	141170
Autodump	32, 33	141172
Autodump	34, 35	141174
Autodump	36, 37	141176

3DD - The 3DD option receives the Go IOP Function (I4) and decodes the IOP Function Data (I0 - 3). After decoding a command 1 for the odd channel, the 3DD sets the busy flag and clears the done flag for the odd channel. The 3DD sends the Go IOP Function (R14) and the IOP Function Data (R10 - 13) to the 3DJ and 3DI options.

3DI - After the 3DI option decodes a command 1, it sends a Reset Address (R80) to the 3DJ and a DMA Control (R44) to the 3DD.

3DJ - The 3DJ option clears the sequencer address after receiving Reset Address (I80) from the 3DI and then outputs the sequencer address (R0 - 9) to the RAM.

RAM - The RAM outputs 32 bits of sequencer data to the 3DI and 3DJ options.

2. DMA Control. The 3DI sends a DMA Control to the 3DD after receiving the data from the RAM.

3DI - The 3DI option receives the sequencer data (I0 - 31) from the RAM, then sends a DMA Control (R44) and a parcel of data (R40 - 43) to the 3DD. Then the 3DI sends Advance Sequencer Address to the 3DJ.

3. DMA Input Control. The 3DD sends an DMA Input Control to the IOP with each parcel of data.

   3DD - The 3DD sends a DMA Input Control (R4) at sync 0 or 3 and the parcel of data.

4. DMA Output Control. The IOP sends a DMA Output Control to acknowledge the parcel of data and to request the next parcel.

   IOP - After setting the busy flag, the IOP waits for a DMA Input Control at sync 0 or 3. The IOP generates a local write request after receiving the DMA Input Control. Then the IOP outputs the DMA Output Control at sync 1 or 4 to the DCA2 after writing the parcel of data into local memory. When the parcel counter on the 3AL option equals zero, the IOP sends the DMA Output Control at sync 2 or 5 to the 3DD. Refer to Section 5, "DMA Local Memory Write Reference Sequence," for complete local memory write reference sequence.

   3DD - The 3DD option receives DMA Output Control (I5) from the IOP. The 3DD passes the DMA Control (R14) to the 3DI. Perform steps 2 through 4 for each parcel.

5. Interrupt. The 3DD sends an Interrupt (R7) to the IOP when the done flag sets and the channel Interrupt is enabled.

   IOP - When the parcel counter on the 3AL equals zero, the IOP sets the appropriate DMA done flag and clears the DMA busy flag. The IOP then sends DMA Output Control at sync 2 or 5 with the last parcel of data.

   3DD - The 3DD sets the done flag and clears the busy flag after receiving a DMA Output Control at sync 2 or 5 from the IOP.

DCA2 Disk Drive Read Sequence

The following is a sequential read from an IPI disk drive with a DCA2 controller. The IPI protocol is simulated by micro sequencer code located on the DCA2 quarter board. Refer to Figure 8-3 for DCA2 block diagram.

1. Go IOP Function. The IOP outputs Go IOP Function to a specific channel pair. When the channel receives the signal, it decodes the IOP Function Data. The IOP Function Data is the modifier bits that clock period, and the command on the next clock period. If needed for the next 4 CPs, the IOP Function Data is the accumulator data.

IOP - The 3AS option sends Go IOP Function (R33 or R34) and the 3AQ option sends IOP Function Data (R25 - 28 or R30 - 33) for channels 30, 31 and 34, 35. The 3AP option sends Go IOP Function (R33 or R34) and the 3AO option sends IOP Function Data (R25 - 28 or R30 - 33) for channels 32, 33 and 36, 37. The IOP Function Data is sent to the DCA2 four bits at a time.

3DD - The 3DD option receives the Go IOP Function (I4) and IOP Function Data (I0 - 3). The DCA2 sets the busy flag and clears the done flag for the selected channel after decoding a command 5. The 3DD sends the Go IOP Function (R14) and the Function Data (R10 - 13) to the 3DJ and 3DI options. It also sends Go IOP Function (R24) and IOP Function Data (R20 - 23) to the 3DE, 3DF and 3DG options.

3DF - The 3DF option loads the device address after decoding a command 5.

3DI - The 3DI option loads the transfer counter after decoding a command 4. The transfer length is 20,154 parcels. There are 24 ID, 20,000 data, 20 ECC, and 110 defect parcels.

3DJ - The 3DJ option loads the sequencer address after decoding a command 5.

RAM - The RAM outputs the Sequencer Data addressed by the 3DJ. The 3DJ option latches the Sequencer Data (I0 - 35). The sequencer data bits are as follows: 2^{35} - 2^{32} parity, 2^{31} - 2^{20} parameter, 2^{19} - 2^{16} function, 2^{15} - 2^{10} branch select, and 2^{9} - 2^{0} next address.

2. Sequence Data. The Sequence Data is used to control the DCA2 quarter board and to simulate the IPI protocol.

   3DJ - Each time the 3DJ option outputs a new address to the RAM, the 3DJ receives 32 bits of sequencer data. The sequencer data is decoded for the next address, branch control, functions, and parameters. The sequencer data is parity protected. The 3DJ reports parity errors (R32 - 35) to the 3DD and halts the sequence. The 3DJ outputs Sequencer Parameter and Function (R80 - 87) to the 3DD, 3DE, 3DF, 3DG, 3DHs, and 3DI options with each new sequencer address.

3. Select Out. The master asserts a Select Out to select the slave (Select state).

3DF - The 3DF option asserts Select Out (R20) after decoding the Sequencer Parameter and Function (I80 - 87). The device address is on the A bus (R0 - 8) when Select Out is asserted.

4. Slave In. The slave asserts Slave In in response to Select Out (Slavack state).

   3DE - The 3DE option receives Slave In (I21) and then outputs the Input Tag Status (R50 - 53) to the 3DJ.

   3DF - The 3DF option enables the loading of the A and B buses after receiving Slave In (I21).

   3DJ - After receiving Input Tag Status (I50 - 53), the 3DJ selects the next sequencer address. The 3DJ then receives the sequencer data and fans out the Sequencer Parameter and Function (R80 - 87).

5. Sync Out. The master asserts Sync Out to inform the slave there is control on the A bus (Busctl).

   3DE - Sync Out is generated by Sequencer Parameter and Function (I80 - 87) from the 3DJ option. The Master negates Sync Out after receiving Sync In (Mastend state).

   3DF - The 3DF option loads the A bus (R0 - 8) with the control and then asserts Sync Out (R22) after receiving Send Sync Out (I46).

6. Sync In. The slave asserts Sync In to acknowledge Sync Out and to transfer status to DCA2 on the B bus (Busack).

   3DE - The 3DE receives Sync In (I22) and the status. Then the 3DE outputs Sync In (R22) to the 3DF and Input Tag Status (R50 - 53) to the 3DJ. The Slave negates Sync In after the master negates Sync Out (Slavack state).

7. Master Out. The Master asserts Master Out to initiate the transfer after the slave negates Sync In (Xfrrdy state).

   3DF - The 3DF asserts Master Out (R21) after decoding Sequence Parameter (I80 - 83) and Function (I84 - 88) from the 3DJ option.

8. Sync In. The slave asserts Sync In for each parcel of information (Xfrst state).

3DE - The 3DE receives Sync In (I22) and latches the parcel. The A and B buses are 8 bits of data and 1 bit of parity each. The 3DE sends Sync In (R22) to the 3DF and Input Tag Status (R50 - 53) to the 3DJ. The Slave negates Sync In after the master asserts Sync Out (Xfrend state).

9. Sync Out. The master asserts Sync Out after latching the data (Xfrres state).

   3DE - Sync Out is generated by Sequencer Parameter (I80 - 83) and Function (I84 - 88) from the 3DJ option. The Master negates Sync Out after receiving Sync In (Xfrrdy state).

   3DF - The 3DF option asserts Sync Out (R22) after receiving Send Sync Out (I46). The 3DF negates Sync Out after the slave negates Sync In. Perform steps 8 and 9 for each parcel information from the slave.

10. Go Parcel. The 3DE sends a Go Parcel to increment the parcel counter on the 3DG and to decrement the transfer counter on the 3DI each time Sync In is asserted.

    3DE - The 3DE option outputs the data to the 3DG, 3DH, and 3YB options. The data is sent a parcel at a time with 2 parity bits.

    3DG - The 3DG option increments the parcel counter after receiving Go Parcel (I42). The first 24 parcels are the ID parcels. The 3DG receives the 24 ID parcels and compares it to the selected ID and then clears the parcel counter. Since the next 20,000 parcel are data, the 3DG increments the parcels counter and then sends a Go Read (R8) and parcel address (R20 - 22) to the 3YB. It also sends a Go Read (R9) to the 3DH options. When the parcel counter equals 20,000 the data is transferred. The next 20 parcels are ECC parcels. The 3DG sends a Go Read ECC (R12) to the 3DH options. If there is a defect pad located on this cylinder, the defect counter counts the 110 parcels of defect. The parcel counter counts ID, Data, and ECC parcels.

    3DI - The 3DI option decrements the transfer counter after receiving Go Parcel (I50). The transfer counter counts ID, data, defect, and ECC parcels.

11. Start a or Start b. The 3DE sends a Start a or Start b to the 3YB option to select the proper pointer.

3DD - The 3DD outputs an a Active (R36) or b Active (R38) to the 3DJ for the select channel. If stacking sector, the 3DD outputs a Hold (R37) or b Hold (R39) for the waiting channel.

3DJ - The 3DJ receives a Active (I36) or b Active (I38) and outputs the proper Sequencer Parameter and Function (R80 - 87).

3DE - The 3DE sends Start a (R21) for the even channel or Start b (R22) for the odd channel. The even channel uses the a pointer and the odd channel uses the b pointer. The Start a and Start b are determined by the Sequencer Parameter and Function (I80 - 87).

12. Go Read. The 3DG option sends a Go Read to latch the data parcels on the 3YB and 3DH options. The 3DG also sends the parcel address to the 3YB.

    3YB - The 3YB option checks the parity and assembles the data into a word. As the data is assembled, the 3YB generates SECDED.

    3DHs- The 3HD options generate the ECC. After the a sector of data is received, the 3DH options compare the new ECC to the old ECC. The ECC errors (R10 - 13) are reported to the 3DG option. If an ECC error occurred, the ECC is read to the IOP with a command 1.

13. Last Parcel. The 3DG sends Last Parcel to the 3YA requesting to send a word of data to the buffer board.

    3DG - When the parcel address (R20 - 22) equals three, the 3YB has received the last parcel of the word.

14. Go to Input Buffer. The 3YA option sends Go to Input Buffer to request a word of data from the 3YB option.

    3YA - After receiving Last Parcel (I36), the 3YA sends Go to Input Buffer to the 3YB (R19) at sync 2.

15. Start a or Start b. The Start a or Start b signals inform the 3YA which pointer to use.

    3YB - The 3YB sends a Start a (R32) for the even channel and Start b (R33) for the odd channel and a word of data with check bits (R0 - 19).

16. Go a To I/O or Go b To I/O. These signals select the proper mode and increment the address on the buffer board.

3YA - The 3YA sends Go a To I/O (R17) or Go b To I/O (R18) designated by Start a (I37) or Start b (I38). The 3YA outputs the data (R20 - 31) 12 bits at a time to the buffer board. Perform steps 8 through 16 until Slave In is negated.

The Go a To I/O and Go b To I/O at sync 2 selects the mode. A Go a To I/O at sync 2 selects "a" read and "b" write mode. A Go b To I/O at sync 2 selects "a" write and "b" read mode.

The Go a To I/O and Go b To I/O at sync 3 writes the word into the buffer and increments the "a" or "b" pointer's address. The Go a To I/O at sync 3 increment "a" pointer's address and writes word to the buffer board. A Go b To I/O at sync 3 increments the "b" pointer's address and writes the word to the buffer board. Refer to Table 8-5 for correct sync time for Go a To I/O and Go b To I/O.

Table 8-5. Go a to I/O and Go b to I/O Sync Time

Channel/Function	Pointer	Mode	Increment Address
Even/Input	a	Go b sync 2	Go a sync 3
Odd/Input	b	Go a sync 2	Go b sync 3
Even/Output	a	Go a sync 2	Go a sync 3
Odd/Output	b	Go b sync 2	Go b sync 3

17. Go Read ECC. The 3DG option outputs Go Read ECC to the 3DH option to stop the ECC generation.

    3DG - If the ECC is enabled, the 3DG outputs Go Read ECC (R12) when the parcel counter is greater than 20,000. If ECC is not enabled, the 3DG continues to send Go Read (R8 - 9).

    3DH - The 3DH options compare the old ECC to the new ECC after receiving Go Read ECC (I9).

    3YB - The 3YB passes the ECC parcels to the buffer board if ECC is not enabled.

18. Slave In. The slave negates Slave In to end the transfer (Slavend state).

3DE - The 3DE option receives Slave In (I21) and then outputs the Input Tag Status (R50 - 53) to the 3DJ option.

19. Master Out. The master negates Master Out acknowledging Slave In (Select state).

    3DF - When Slave In is negated, the transfer counter equals zero and the 3DF has received Sequencer Parameter and Function. The 3DF negates Master Out (R14).

20. Slave In. The slave asserts Slave In in response to Master Out and to exchange ending status (Slavack state).

    3DE - The 3DE receives Slave In (I21) and then outputs the Input Tag Status (R50 - 53) to the 3DJ.

21. Sync Out. The master asserts Sync Out to inform the slave of ending status on the A bus (Busctl).

    3DE - Sync Out is generated by Sequencer Parameter (I80 - 83) and Function (I84 - 88) from the 3DJ option. The Master negates Sync Out after receiving Sync In (Mastend state).

    3DF - The 3DF option loads the A bus (R0 - 8) with the ending status and then asserts Sync Out. The Master negates Sync Out after receiving Sync In.

22. Sync In. The slave asserts Sync In to acknowledge Sync Out and to transfer the response status to DCA2 on the B bus (Busack state).

    3DE - The 3DE option receives Sync In (I22) and then sends Sync In (R22) to the 3DF and Input Tag Status (R50 - 53) to the 3DJ. The Slave negates Sync In after the master negates Sync Out (Slavack state).

23. Interrupts. An Interrupt is sent to the IOP when the done flag sets and the channel Interrupt is enabled.

    3DD - The 3DD option sets the done flag and clears the busy flag after receiving the proper Sequence Parameter and Function (I80 - 87).

DCA2 Disk Drive Write Sequence

The following is a sequential write to an IPI type disk drive with a DCA2 controller. The IPI protocol is simulated by the micro sequencer code located on the DCA2 quarter board. Refer to Figure 8-3 for DCA2 block diagram.

1. Go IOP Function. The IOP sends Go IOP Function to a specific channel pair. When the channel receives the signal, it decodes the IOP Function Data. The IOP Function Data is the modifier bits that clock period and the command on the next clock period. If needed for the next 4 CPs, the IOP Function Data is the accumulator data. Perform steps 1 through 7 of the DCA2 Read Sequence to select and enable the disk drive and read the ID field.

2. Start a or Start b. The Start a or Start b signal informs the 3YA option which pointer to use.

   3DF - The 3DF option sends a Start a (R50) for the even channel or Start b (R51) for the odd channel. The even channel uses the a pointer and the odd channel uses the b pointer. The Start a and Start b are determined by the Sequencer Parameter and Function (I80 - 87).

   3YA - The 3YA option selects the proper pointer and then sends Go a To I/O or Go b To I/O (R17 or R18) to the buffer board to select the mode.

3. Go a To I/O or Go b To I/O. These signals select the proper mode and increment the address on the buffer board.

   3YA - The 3YA option sends Go a To I/O (R17) or Go b To I/O (R18) designated by Start a (I14) or Start b (I15). The 3YA then latches the data (I0 -11) that is being sent 12 bits at a time from the buffer board.

   The Go a To I/O and Go b To I/O at sync 2 selects the mode. The Go a To I/O at sync 2 selects a read and b write mode. The Go b To I/O at sync 2 selects a write and b read mode.

   The Go a To I/O and Go b To I/O at sync 3 increments the a or b pointer's address. The Go a To I/O at sync 3 increments a pointer's address. The Go b To I/O at sync 3 increments the b pointer's address. Refer to Table 8-5 for correct sync time for Go a To I/O and Go b To I/O.

4. Go to Output Buffer. The 3YA option sends Go to Output Buffer with each word of data to the 3YC option.

   3YC - The 3YC option receives the Go to Output Buffer and one word of data with check bits. The data and check bits are sent 16 bits (I0 -15) at a time for 5 CPs. The 3YC performs SECDED and then generates 2 bits of parity for each parcel. If there is a SECDED error (R24 - 25), it is reported to the 3DD option.

5. Data Available. The 3YC sends a Data Available to the 3DF for each parcel of data it sends to the 3DH options.

   3DF - The 3DF option sends Go Parcel (R60 - 61) to the 3DG and 3DI options and then waits for the data from the 3DH options after receiving Data Available (I19).

6. Go Parcel. The 3DF sends a Go Parcel to decrement the transfer counter on the 3DI option and increment the parcel counter on the 3DG option.

   3DI - The 3DI option decrements the transfer counter after receiving Go Parcel (I50). The transfer counter counts ID, data, and ECC parcels.

   3DG - The 3DG option increments the parcel counter and sends a Go Write (R10 -11) to the 3YC and 3DH options after receiving Go Parcel (I43). The parcel counter counts the data parcels. When the parcel counter equals 20,000 the data transfer is complete. The next 20 parcels are ECC parcels, so the 3DG outputs Go Write ECC (R13) and Gate Out ECC (R16). If there is a defect, the 3DG counts the 110 defect parcels with the defect counter. The 3DG does not send Go Write (R10 - 11) if the defect counter is counting, so the 3DF outputs the same parcel of data to each parcel of the defect pad.

7. Go Write. The 3DG sends a Go Write to latch the data on the 3DH options.

   3DHs- The 3DH options output the data to the 3DF option and generate the ECC code. The ECC is read to the IOP with a command 1.

   3YC - The 3YC option outputs the next data available after receiving Go Write (I20).

8. Sync In. The slave asserts Sync In requesting a parcel of data (Xfrst state).

   3DE - The 3DE option receives the Sync In (I22). The 3DE sends Sync In (R22) to the 3DF and Input Tag Status (R50 - 53) to the 3DJ. The Slave negates Sync In after the master asserts Sync Out (Xfrend state).

9. Sync Out. The master asserts Sync Out with each parcel of data (Xfres state).

3DE - Sync Out is generated by Sequencer Parameter and Function (I80 - 87) from the 3DJ option. The Master negates Sync Out after receiving Sync In (Xfrrdy state).

3DF - The 3DF option asserts Sync Out (R22) after receiving Send Sync Out (I46). The 3DF loads the A and B buses with 8 bits of data and 1 bit of parity each. The 3DF negates Sync Out after the slave negates Sync In. Perform steps 8 and 9 for each parcel data or ECC to the slave.

10. Data Request. The 3YC option sends a Data Request to request the next word of data from the 3YA option.

    3YA - The 3YA option receives the Data Request and latches the next word from the buffer board at the proper sync time. The buffer board is always reading out the selected address.

11. Go Write ECC and Gate Out ECC. The 3DG option sends the Go Write ECC and Gate Out ECC to enable the 3DH options to output the ECC. Perform steps 18 through 23 of the DCA2 Read Sequence to terminate the transfer.

    3DG - When the parcel counter equals 20,000, the 3DG sends Go Write ECC (R12) and Gate Out ECC (R16) to the 3DH options.

    3DHs- The 3DH options gate the inverted ECC (R0 - 7) to the 3DF after receiving Go Write ECC (I9) and Gate Out ECC (I28).

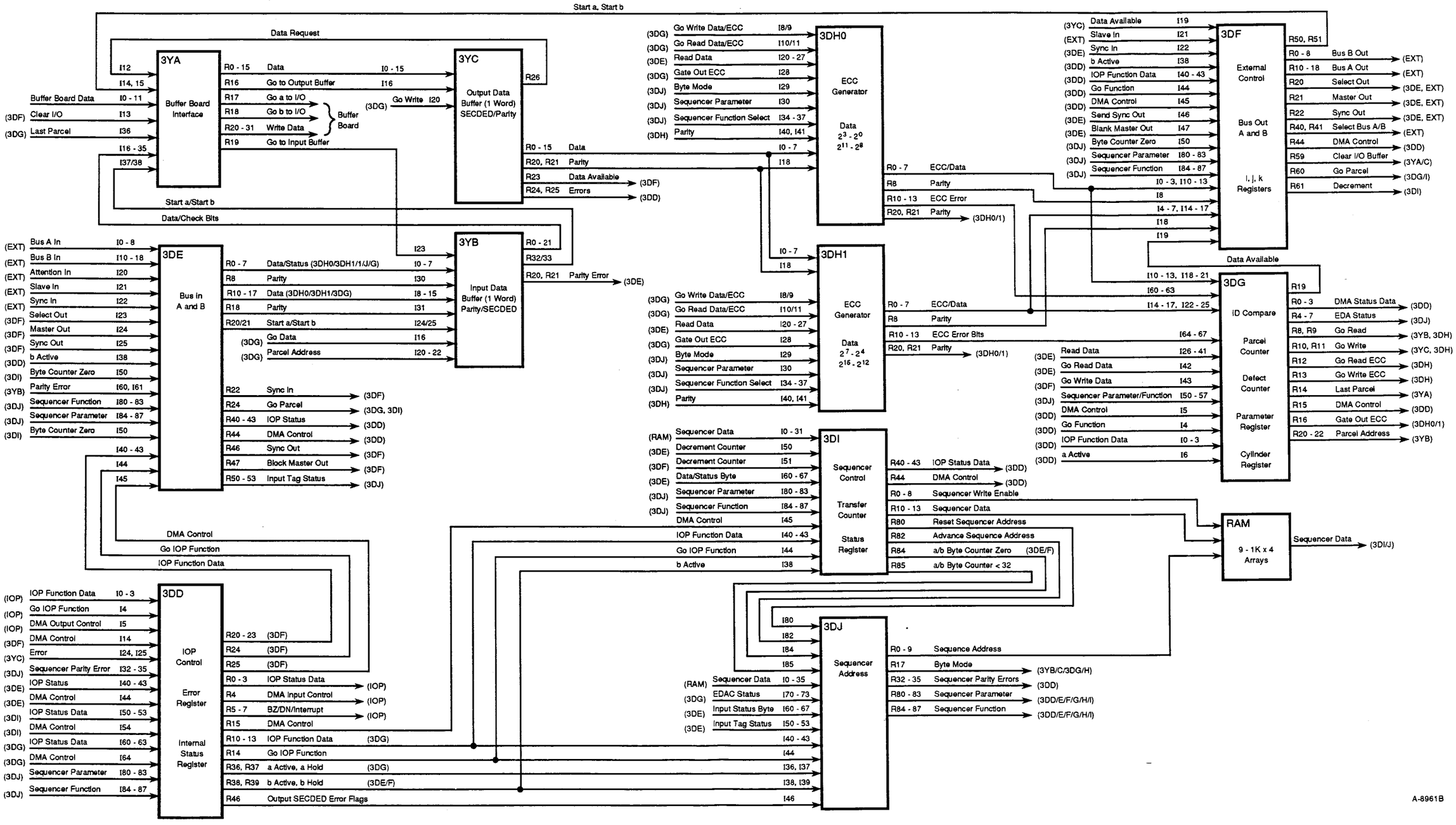


Figure 8-3. DCA2 Block Diagram and Control Signals

9 TCA1 TAPE CONTROLLER QUARTER BOARD

The TCA1 quarter board interfaces between the IOP and IBM tape drives. The TCA1 simulates the IBM protocol with the use of the micro-sequencer code. The micro-sequencer code is stored on nine 1K x 4-bit random access memory (RAM) chips and is loaded via local memory. The TCA1 quarter board consists of the 3DD, 3DG, 3DH, 3DI, 3DJ, 3TA, 3TB, 3YA, 3YB, and 3YC options. Refer to Table 9-1 for a functional description of TCA1 options. Refer to Figure 9-6 for the TCA1 quarter board option layout.

Table 9-1. TCA1 Options and Functional Description

Option	Functional Description
3DD	IOP control Error register Internal status register
3DG	Byte counter
3DH0	Data out 2^3 - 2^0
3DH1	Data out 2^7 - 2^4
3DI	Sequencer control Transfer counter Status register
3DJ	Sequencer address
3TA	External input control Bus 0 in
3TB	External output control Bus 0 out i, j, and k registers
3YA	Buffer board interface
3YB	Input data buffer
3YC	Output data buffer

TCA1 Data Flow

The TCA1 inputs data to the buffer board via 3TA, 3YB, and 3YA options. Refer to Figure 9-1 for a TCA1 block diagram. The 3TA receives data from the tape drive. The bus has 8 bits of data and 1 bit of parity. The 3TA checks the data for bus parity errors. Then the 3TA outputs the data and parity to the 3YB. The 3YB checks the parity and assembles the data in a 64-bit word and generates check bits. The 3YB outputs the word of data and check bits to the 3YA. The 3YA outputs the data and check bits to the buffer board 12 bits per clock period (CP).

The TCA1 outputs data to the tape drive via the 3YA, 3YC, 3DH, and 3TB options. Refer to Figure 9-1 for a TCA1 block diagram. The 3YA receives the data and checks bits from the buffer board 12 bits per CP. The data and check bits are then sent to the 3YC. The 3YC performs single-error correction, double-error correction (SECDED[†]) and then generates 1 bit of parity for each byte of data. The 3YC outputs the data to 3DH options. Then each 3DH outputs 4 bits of data to the 3TB option. The 3DH0 option also outputs the parity bit. The 3TB loads the data and parity on the bus and then outputs it to the tape drive.

The micro-sequencer code is written to the RAM via the 3DD and 3DI options. Refer to Figure 9-1 for a TCA1 block diagram. The 3DD receives the data from local memory (3AO or 3AQ options) 4 bits at a time. The 3DD then outputs the data to the 3DI. The 3DI generates a written enable and then passes the data to the RAM. The 3DJ option outputs the sequencer address.

For diagnostic purposes the micro-sequencer code is read back to local memory via the 3DI and 3DD options. Refer to Figure 9-1 for a TCA1 block diagram. The 3DJ option addresses the RAM. The RAM then outputs the data to the 3DI. The 3DI passes the data to the 3DD 4 bits at time. The 3DD outputs the data to local memory (3AS or 3AP options).

IBM Protocol

The following is a description of the TCA1s IBM protocol: data bus, tag lines, and select lines.

[†] Hamming, R. W. "Error Detection and Correcting Codes." *Bell System Technical Journal.* 29.2 (1950): 147 - 160.

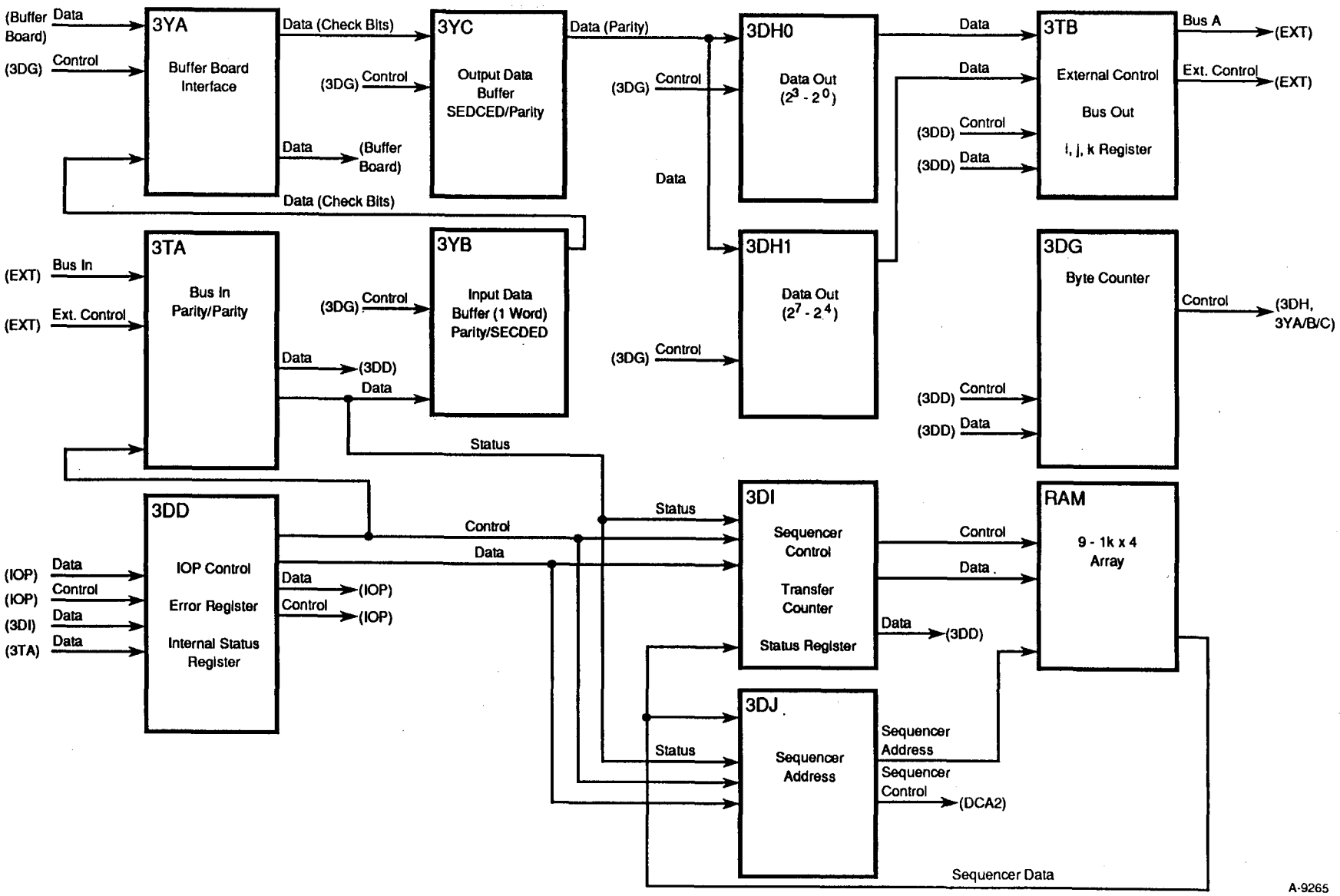


Figure 9-1. TCA1 Block Diagram

NOTE: The TCA1 has meter and mark lines but they are not used at the present time.

Data Bus

The following is a description of the TCA1 data bus signals. Refer to Figure 9-2 for a data bus block diagram.

- Bus. The Bus 0 has 8 bits of data and 1 bit of parity. The Bus is used to pass the address, data, commands, and status between the TCA1 and the tape drive.

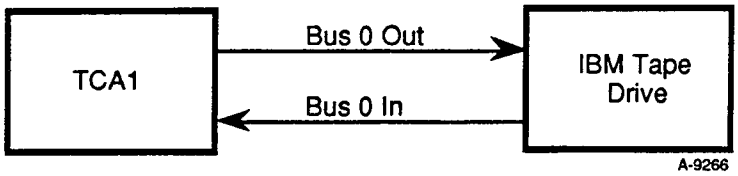


Figure 9-2. Data Bus Block Diagram

Tag Lines

The following is a description of the TCA1 tag line signals. Refer to Figure 9-3 for a tag line block diagram.

- Address Out. The Address Out is raised by the TCA1 when there is an address on the bus out.
- Address In. The Address In is raised by the drive when it returns the address to the TCA1. The address is returned by the selected drive.
- Command Out. The Command Out is raised by the TCA1 when there is a command on the bus out or the byte count equals zero.
- Status In. The Status In is raised by the drive when it is inputing status to the TCA1. The tape drives send a byte of initial status and a byte of ending status.
- Service Out. The Service Out is raised by the TCA1 for each byte of data or in response to Status In.
- Service In. The tape drive raises Service In when it is sending or receiving a byte of data. Service In and Service Out handshake each byte of data.

- Data Out. The TCA1 raises Data Out when it is accepting or sending a byte of data.
- Data In. The tape drive raises Data In when it is accepting or sending a byte of data. The Data In and Data Out signals handshake every other byte of data in 1.5, 3.0, and 4.5 Mbyte modes. The Service In and Service Out signals handshake the other byte of data.

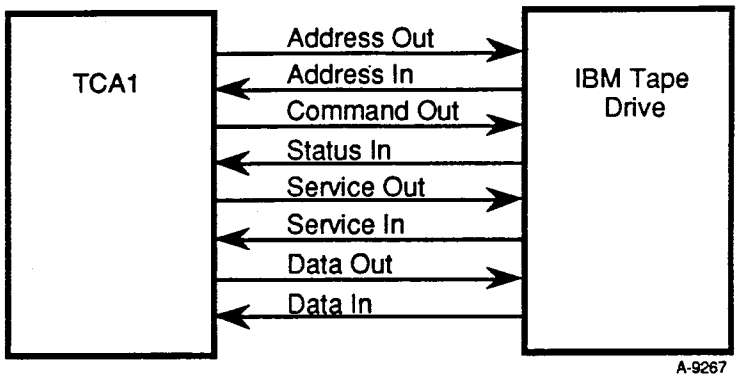


Figure 9-3. TCA1 Tag Lines

Select Lines

The following is a description of the TCA1 select line signals. Refer to Figure 9-4 for a select line block diagram.

- Operational Out. The Operational Out enables the control signals for the TCA1 and tape drive.
- Hold Out. The Hold Out is used with Select Out to select the tape drive.
- Select Out. The Select Out is used with Hold Out to select the tape drive.
- Operational In. Operational In states the tape drive is selected and active.
- Suppress Out. The Suppress Out suppresses the data, status, chaining command, and selective reset.
- Select In. The Select In is asserted if no tape drive selects the address.

- Request In. The Request In indicates the tape drive needs service.
- Disconnect In. The Disconnect In is raised by the selected tape drive if an error occurred.

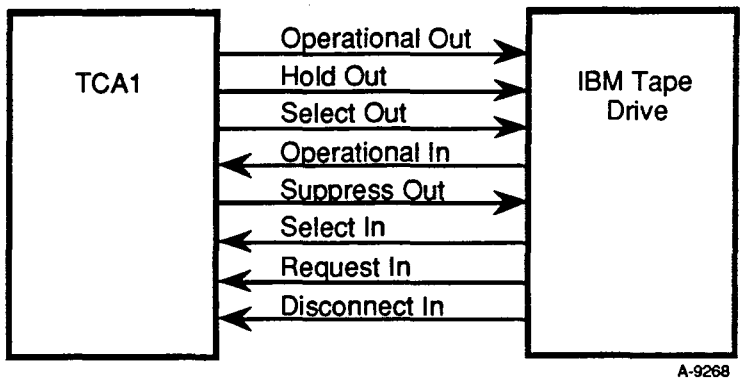


Figure 9-4. Select Line Block Diagram

TCA1 Autoload Sequence

For a sequential description of a TCA1 micro-sequencer code autoload, refer to the DCA2 autoload sequence in the DCA2 section. The TCA1 quarter board has nine 1K by 4-bit RAM arrays to hold the micro-sequencer code. The micro-sequencer code simulates IBM protocol for the TCA1. Refer to Figure 9-5 for a TCA1 block diagram.

TCA1 Autodump Sequence

For a sequential description of a TCA1 micro-sequencer code autodump, refer to the DCA2 autodump sequence in the DCA2 section. The TCA1 quarter board has nine 1K by 4-bit RAM arrays to hold micro-sequencer code. The micro-sequencer code simulates IBM protocol for the TCA1. For diagnostic purposes, the micro-sequencer code is read to local memory (autodump). Refer to Figure 9-5 for a TCA1 block diagram.

TCA1 Tape Drive Select and Read Sequence

The following is a sequential read from an IBM-type tape drive with a TCA1 controller. The IBM protocol is simulated by the micro-sequencer code located on the TCA1 quarter board. Refer to Figure 9-5 for a TCA1 block diagram.

1. Go IOP Function. The IOP outputs Go IOP Function to a specific channel pair. When the channel receives the signal, it decodes the IOP Function Data. The IOP Function Data is the modifier bits that clock period and the command on the next clock period; if needed the next 4 CPs, the IOP Function Data is the accumulator data.

   IOP - The 3AS option sends Go IOP Function (R33 or R34) and the 3AQ option sends IOP Function Data (R25 - 28 or R30 - 33) for channels 30, 31 and 34, 35. The 3AP option sends Go IOP Function (R33 or R34) and the 3AO option sends IOP Function Data (R25 - 28 or R30 - 33) for channels 32, 33 and 36, 37. The IOP Function Data is sent to the TCA1 4 bits at a time.

   3DD - The 3DD option receives the Go IOP Function (I4) and IOP Function Data (I0 - 3). The 3DD sets the busy flag and clears the done flag for the selected channel after decoding a command 5. The 3DD sends the Go IOP Function (R14) and the Function Data (R10 - 13) to the 3DG, 3DJ and 3DI options. It also sends Go IOP Function (R24) and IOP Function Data (R20 - 23) to the 3TA and 3TB options. The 3DD option outputs an a Active (R36) or a b Active (R38) to the 3DJ option for the selected channel. If stacking channels, the 3DD outputs a Hold (R37) or b Hold (R39) for the waiting channel.

   3DI - The 3DI option loads the transfer counter after decoding a command 4.

   3DJ - The 3DJ option loads the sequencer address after decoding a command 5.

   3TB - The 3TB option loads the i register after decoding a command 5 and the j and k registers after decoding a command 16.

   RAM - The RAM outputs the sequencer data addressed by the 3DJ option. The 3DJ latches the sequencer data (I0 - 35). The sequencer data bits are as follows: 2^{35} - 2^{32} parity, 2^{31} - 2^{20} parameter, 2^{19} - 2^{16} function, 2^{15} - 2^{10} branch select, and 2^{9} - 2^{0} next address.

2. Sequence Data. The sequencer data is used to control the TCA1 quarter board and to simulate the IBM protocol.

   3DJ - Each time the 3DJ option outputs a new address to the RAM, the 3DJ receives 32 bits of sequencer data. The sequencer data is decoded for the next address, branch

control, functions, and parameters. The sequencer data is parity protected. The 3DJ reports parity errors (R32 - 35) to the 3DD option and halts the sequence. The 3DJ outputs sequencer parameter (R80 - 83) and function (R84 - 87) to the 3DD, 3DG, 3DH, 3DI, 3TA, and 3TB options with each new sequencer address. The sequencer address can be changed every 3 CPs (the access time of RAM is 18.75 ns).

3. Operational Out. The TCA1 raises Operational Out to activate the controller and enable the tag and select lines.

   3TA - The 3TA option outputs Operational Out (R24) after receiving the sequencer parameter and function (I80 - 87). The 3TA passes the input tag 7 status (R50 - 53) to the 3DJ option every clock period.

4. Address Out. The TCA1 raises Address Out with the device address on the bus out.

   3TA - The 3TA option raises Address Out (R24) after receiving the sequencer parameter and function (I80 - 87). The 3TA drops Address Out after receiving Operational In (I24).

   3TB - The 3TB option loads the device address on the bus out (R0 - 8).

5. Hold Out and Select Out. The TCA1 raises a Hold Out and Select Out to select the drive.

   3TA - The 3TA option raises Hold Out (R26) and Select Out (R27) after decoding the sequencer parameter and function (I80 - 87). Since Address Out is raised, the devices reads the address on the bus out.

6. Operational In. The drive raises Operational In after accepting the address. The 3TA and 3TB options receive Operational In.

7. Address In. The selected tape drive raises Address In response to Select Out with the address on the bus in.

   3TA - The 3TA option receives Address In (I21) and then latches the bus in (I0 - 8) and then outputs the input tag status (R50 - 53) to the 3DI and 3DJ options. The bus holds the address of the selected drive. If no drive accepts the address, the termination block sends back a Select In (I27).

8. Command Out. The TCA1 raises Command Out to inform the tape drive there is control on the bus out.

   3TB - The Command Out is generated by sequencer parameter and function (I80 - 87) from the 3DJ option. The 3TB option loads the bus out (R0 - 8) with the command (j register) and then sends Command Out (R22) to the 3TA option.

   3TA - The 3TA option outputs the Command Out (R22). The 3TA drops Command Out after receiving Status In.

9. Status In. The tape drive raises Status In to indicate there is a byte of status on the bus in.

   3TA - The 3TA option receives Status In (I22) and the byte status. Then the 3TA outputs input status (R0 - 7) to the 3DI and 3DJ options.

10. Service Out. The TCA1 raises Service Out to acknowledge Status In.

    3TB - The 3TB option sends Service Out (R20) to the 3TA option. The Service Out is generated by sequencer parameter and function (I80 - 87) from the 3DJ option.

    3TA - The 3TA option outputs Service Out to the tape drive.

11. Data In. The tape drive raises Data In for each byte of information.

    3TA - The 3TA option receives Data In (I22) and latches the byte of data. The tape drive drops Data In after the TCA1 raises Data Out. Data In and Data Out are not used in .75 Mbyte mode. If in 1.5 Mbyte mode, Data In and Data Out handshake every other byte starting with the second byte of data. If in 3.0 or 4.5 Mbyte modes, Data In and Data Out handshake every other byte of data starting with the first byte.

12. Data Out. The TCA1 raises Data Out after latching the data.

    3TB - The 3TB option sends Data Out (R20) to the the 3TA option. The Data In and Data Out signals operate in interlock and nonlock modes.

3TA - The 3TA option outputs Data Out to the tape drive. The TCA1 drops Data Out after receiving Data In. Perform steps 11 and 12 for every other byte of data from the tape drive.

13. Service In. The tape drive raises Service In for each byte of information.

    3TA - The 3TA option receives Service In (I22) and latches the byte of data. The tape drive drops Service In after the TCA1 raises Service Out. Perform steps 13 and 14 for each byte information from the tape drive in .75 Mbyte mode. If in 1.5, 3.0, or 4.5 Mbyte modes, Service In and Service Out handshake every other byte of data with Data In and Data Out.

14. Service Out. The TCA1 raises Service Out after latching the data.

    3TB - The 3TB option sends Service Out (R20) to the the 3TA option. The Service In and Service Out signals operate in interlock and noninterlock mode.

    3TA - The 3TA option outputs Service Out to the tape drive. The TCA1 drops Service Out after receiving Service In.

15. Go Byte. The 3TA option sends a Go Byte to increment the parcel counter on the 3DG option and decrement the transfer counter on the 3DI option each time Data In and Service In are raised.

    3TA - The 3TA option outputs the data to the 3YB option. The data is sent one byte at a time with 1 parity bit.

    3DG - The 3DG option increments the parcel counter after receiving Go Byte (I42). The 3DG then sends a Go Read (R8) and the byte address (R20 - 22) to the 3YB option.

    3DI - The 3DI option decrements the transfer counter after receiving Go Byte (I50).

16. Start a or Start b. The 3TA option sends a Start a or Start b to the 3YB option to select the proper pointer.

    3TA - The 3TA option sends a Start a (R21) for the even channel or Start b (R22) for the odd channel. The Start a and Start b are determined by the sequencer parameter and function (I80 - 87).

17. Go Read. The 3DG option sends a Go Read and the byte address to latch the byte of data on the 3YB option.

3YB - The 3YB option checks the parity and assembles the data into a word. As the data is assembled, the 3YB generates SECDED. The 3YB reports parity errors (R20 - 21) to the 3TA option.

18. Last Byte. The 3DG option sends Last Byte to the 3YA option requesting to send a word of data to the buffer board.

    3DG - When the byte address (R20 - 22) equals seven, the 3YB option has received the last byte of the word.

19. Go to Input Buffer. The 3YA option sends Go to Input Buffer to request the word of data from the 3YB option.

    3YA - After receiving Last Byte (I36), the 3YA option sends Go to Input Buffer to the 3YB option (R19) at sync 2.

20. Start a or Start b. The Start a or Start b signal informs the 3YA option which pointer to use.

    3YB - The 3YB option sends a Start a (R32) for the even channel or Start b (R33) for the odd channel and a word of data with check bits (R0 - 19).

21. Go a to I/O or Go b to I/O - These signals select the proper mode and increment the address on the buffer board.

    3YA - The 3YA option sends Go a to I/O (R17) or Go b to I/O (R18) designated by Start a (I37) or Start b (I38). The 3YA outputs the data (R20 - 31) 12 bits at a time to the buffer board. Perform steps 11 through 22 until Command Out raised is dropped.

    The Go a to I/O and Go b to I/O at sync 2 selects the mode. A Go a to I/O at sync 2 selects a read and b write mode. A Go b to I/O at sync 2 selects a write and b read mode.

    The Go a to I/O and Go b to I/O at sync 3 writes the word into the buffer and increments the a or b pointer's address. The Go a to I/O at sync 3 increments a pointer's address and writes the word to the buffer board. A Go b to I/O at sync 3 increments the b pointer's address and writes the word to the buffer board. Refer to Table 9-1 for correct sync time for Go a to I/O and Go b to I/O.

    The Go a to I/O and Go b to I/O at sync 4 writes the word into the buffer and decrements the a or b pointer's address.

Table 9-2. Go a to I/O and Go b to I/O Sync Time

Channel/Function	Pointer	Mode	Increment Address	Decrement Address
Even/Input	a	Go b sync 2	Go a sync 3	Go a sync 4
Odd/Input	b	Go a sync 2	Go b sync 3	Go b sync 4
Even/Output	a	Go a sync 2	Go a sync 3	N/A
Odd/Output	b	Go b sync 2	Go b sync 3	N/A

22. Command Out. The TCA1 raises Command Out when the byte count equals zero and Service In is raised.

    3DI - The 3DI option sends byte counter zero (R82) to the 3DJ and 3TA options.

    3TA - The 3TA option receives Byte Count Zero (I50) from the 3DI and then raises Command Out (R22).

23. Status In. The tape drive raises Status In to end the transfer.

    3TA - The 3TA option receives Status In (I21) and a byte of status on the bus in and then outputs the byte of status (R0 - 8) to the 3DI and 3DJ options.

24. Hold Out and Select Out. The TCA1 drops Hold Out and Select Out after latching the status.

25. Service Out. The TCA1 raises Service Out in response to Status In.

    3TA - The 3TA option receives Service Out (I21) from the 3TB option and then raises Service Out. The TCA1 drops Service Out after receiving Status In.

26. Status In and Operational In. The tape drive drops Status In and Operational In after receiving Service Out.

27. Interrupts. An Interrupt is sent to the IOP when the done flag sets and the channel Interrupt is enabled.

    3DD - The 3DD option sets the done flag and clears the busy flag after receiving the proper sequence parameter (I80 - 83) and function (I84 - 88).

TCA1 Tape Drive Write Sequence

The following is a sequential write to an IBM-type tape drive with a TCA1 controller. The IBM protocol is simulated by the micro-sequencer code located on the TCA1 quarter board. Refer to Figure 9-5 for a TCA1 block diagram.

1. Go IOP Function. The IOP sends Go IOP Function to a specific channel pair. When the channel receives the signal, it decodes the IO Function Data. The IOP Function Data is the modifier bits that clock period and the command on the next clock period; if needed the next 4 CPs, the IOP Function Data is the accumulator data. Perform steps 1 through 10 of the TCA1 read sequence to select the tape drive.

2. Start a or Start b. The Start a and Start b signals inform the 3YA option which pointer to use.

    3TB - The 3TB option sends a Start a (R50) for the even channel or Start b (R51) for the odd channel. The Start a and Start b are determined by the sequencer parameter and function (I80 - 88).

    3YA - The 3YA option selects the proper pointer and then sends Go a to I/O or Go b to I/O (R17 or R18) to the buffer board to select the mode.

3. Go a to I/O or Go b to I/O - These signals select the proper mode and increment the address on the buffer board.

    3YA - The 3YA option sends Go a to I/O (R17) or Go b to I/O (R18) designated by Start a (I14) or Start b (I15). The 3YA then latches the data (I0 -11) that is being sent 12 bits at a time from the buffer board.

    The Go a to I/O and Go b to I/O at sync 2 selects the mode. The Go a to I/O at sync 2 selects a read and b write mode. The Go b to I/O at sync 2 selects a write and b read mode.

The Go a to I/O and Go b to I/O at sync 3 increments the a or b pointer's address. The Go a to I/O at sync 3 increments a pointer's address. The Go b to I/O at sync 3 increments the b pointer's address. Refer to Table 9-1 for correct sync time for Go a to I/O and Go b to I/O.

4. Go to Output Buffer. The 3YA option sends Go to Output Buffer with each word of data to the 3YC option.

   3YC - The 3YC option receives the Go to Output Buffer and 1 word of data with check bits. The data and check bits are sent 16 bits (I0 -15) at a time for 5 CPs. The 3YC performs SECDED and then generates 1 bit of parity for each byte of data. If there is a SECDED error (R24 - 25), it is reported to the 3DD option.

5. Data Available. The 3YC option sends a Data Available to the 3TB option for each byte of data it sends to the 3DH options.

   3TB - The 3TB option sends Go Byte (R60) to the 3DG option and Decrement Counter (R61) to the 3DI option. Then the 3TB waits for the data and parity from the 3DH options after receiving Data Available (I19).

6. Go Byte and Decrement Counter. The 3TB option sends a Go Byte to decrement the transfer counter on the 3DI option and increment the byte counter on the 3DG option.

   3DI - The 3DI option decrements the transfer counter after receiving Go Byte (I51).

   3DG - The 3DG option increments the byte counter and sends a Go Write (R10 -11) to the 3YC and 3DH options after receiving Go Byte (I43).

7. Go Write. The 3DG option sends a Go Write to latch the data on the 3DH options.

   3DHs - The 3DH options latch the output and the data to 3TB option. The 3DH0 option outputs bits 2^3 - 2^0 and the parity bit. The 3DH1 option outputs bit 2^7 - 2^4.

   3YC - The 3YC option outputs the next Data Available after receiving Go Write (I20).

8. Data In. The tape drive raises Data In for each byte of data.

   3TA - The 3TA option receives Data In (I22). The tape drive drops Data In after the TCA1 raises Data Out. The Data In and Data Out are not used in .75 Mbyte mode. If in 1.5 Mbyte mode, Data In and Data Out handshake every other byte starting with the second byte of data. If in 3.0 or 4.5 Mbyte modes, Data In and Data Out handshake every other byte of data starting with the first byte.

   3TB - The 3TB option also receives Data In (I21) and then loads the bus out with a byte of data.

9. Data Out. The TCA1 raises Data Out after loading the bus out.

   3TB - The 3TB option sends Data Out (R20) to the the 3TA. The Data In and Data Out signals operate in interlock and noninterlock mode.

   3TA - The 3TA option outputs Data Out to the tape drive. The TCA1 drops Data Out after the tape drive drops Data In. Perform steps 8 and 9 for each byte of information from the tape drive.

10. Service In. The tape drive raises Service In for each byte of information.

    3TA - The 3TA option receives the Service In (I22). The tape drive drops Service In after the TCA1 raises Service Out. If in 1.5, 3.0, or 4.5 Mbyte modes, Service In and Service Out handshake every other byte of data with Data In and Data Out.

    3TB - The 3TB option also receives Service In (I20) and loads a byte of data on the bus out.

11. Service Out. The TCA1 raises Service Out after loading the data on the bus out.

    3TB - The 3TB option sends Service Out (R20) to the the 3TA option.

    3TA - The 3TA option outputs Service Out to the tape drive. The TCA1 drops Service Out after receiving Service In. The Service In and Service Out operate in interlock or noninterlock mode.

12. Data Request. The 3YC option sends a Data Request to request the next word of data from the 3YA option. Perform steps 22 through 27 of the TCA1 read sequence to terminate the transfer.

    3YA - The 3YA option receives the Data Request and latches the next word from the buffer board at the proper sync time. The buffer board is always reading out the selected address.

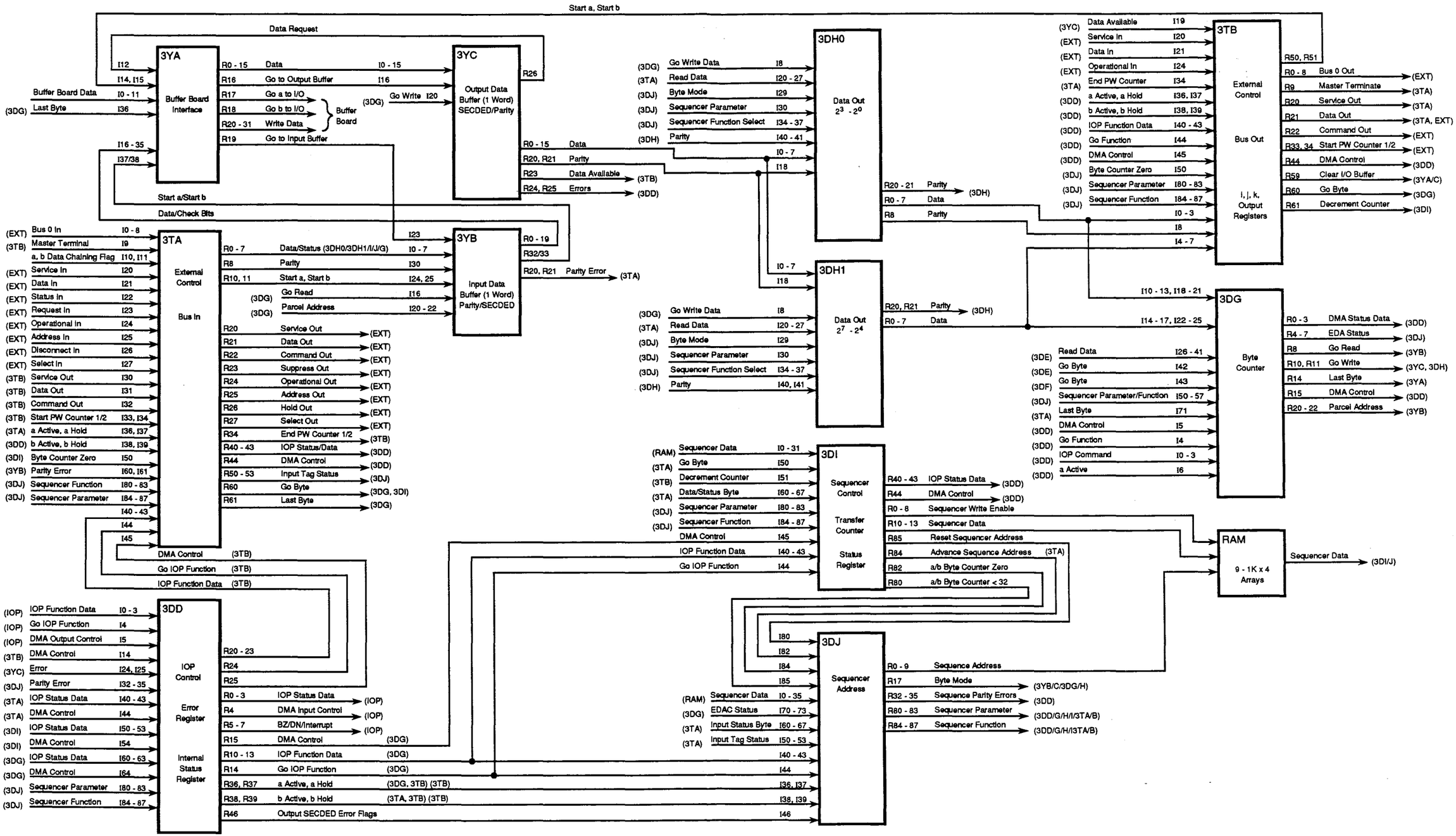


Figure 9-5. TCA1 Block Diagram and Control Signals

10 HCA3/HCA4 HIPPI QUARTER BOARDS

The HCA3 quarter board controls High Performance Parallel Interface (HIPPI) input transfers and consists of the 3HA, 3HB, 3HC, 3HD, 3YA, and 3YD options. Refer to Table 10-1 for a functional description of the HCA3 options. The HCA4 quarter board controls HIPPI output transfers and consists of the 3HE, 3HF, 3HG, 3YA, and 3YE options. Refer to Table 10-2 for a functional description of the HCA4 options. For a complete HIPPI channel there must be HCA3 and HCA4 quarter boards. The HCA3 channels are 30, 31 and 34, 35, and the HCA4 channels are 32, 33 and 36, 37. The HIPPI input channel is called the destination and the output channel is termed the source. The HIPPI operates in 100-Mbyte (32-bit halfwords) or 200-Mbyte (64-bit words) mode. Refer to Figures 10-7 and 10-8 for HCA3 and HCA4 option layout.

Table 10-1. HCA3 Options and Functional Description

Option	Functional Description
3HA	Input control Halfword count register
3HB	Transfer length register
3HC	Input status register Ready counter Max ready counter
3HD0	HIPPI input data, bus A Burst length counter
3HD1	HIPPI input data, bus A HIPPI input external countrol
3HD2/3	HIPPI input data, bus B
3YA	Buffer board interface
3YD	Input data buffer

Table 10-2. HCA4 Options and Functional Description

Option	Functional Description
3HE	HIPPI external output control Transfer length counter Burst length counter
3HF0/1	Output data buffer, bus A
3HF2/3	Output data buffer, bus B
3HG0	HIPPI output data, bus A
3HG1	HIPPI output data, bus A HIPPI external control
3HG2/3	HIPPI output data, bus B
3YA	Buffer board interface
3YE	Output data buffer

HIPPI Channel Data Flow

The HIPPI channel inputs data from the source to the buffer board via the 3HD, 3YD, and 3YA options. Refer to Figure 10-1 for an HCA3 block diagram. The 3HD options receive the data from the source. If in 32-bit mode, the 3HD0 and 3HD1 options both receive 16 bits of data and 2 bits of parity. If in 64-bit mode, each 3HD option receives 16 bits of data and 2 bits of parity. The 3HD option checks the parity as the data arrives. If there is a parity error, the 3HD options report the error to the 3HA. The 3HD1 and 3HD3 options send the data and parity bits to the 3YD. The 3HD0 option sends its data and parity bits to the 3HD1 option and then to the 3YD option. The 3HD2 option sends its data and parity bits to the 3HD3 option and then to the 3YD. The 3YD checks the data for parity errors and then assembles the data into a 64-bit word and generates SECDED. If a parity error occurs, it is reported to the 3HA option. The data and check bits are sent to the 3YA option and then to the buffer board in 12-bit transfers.

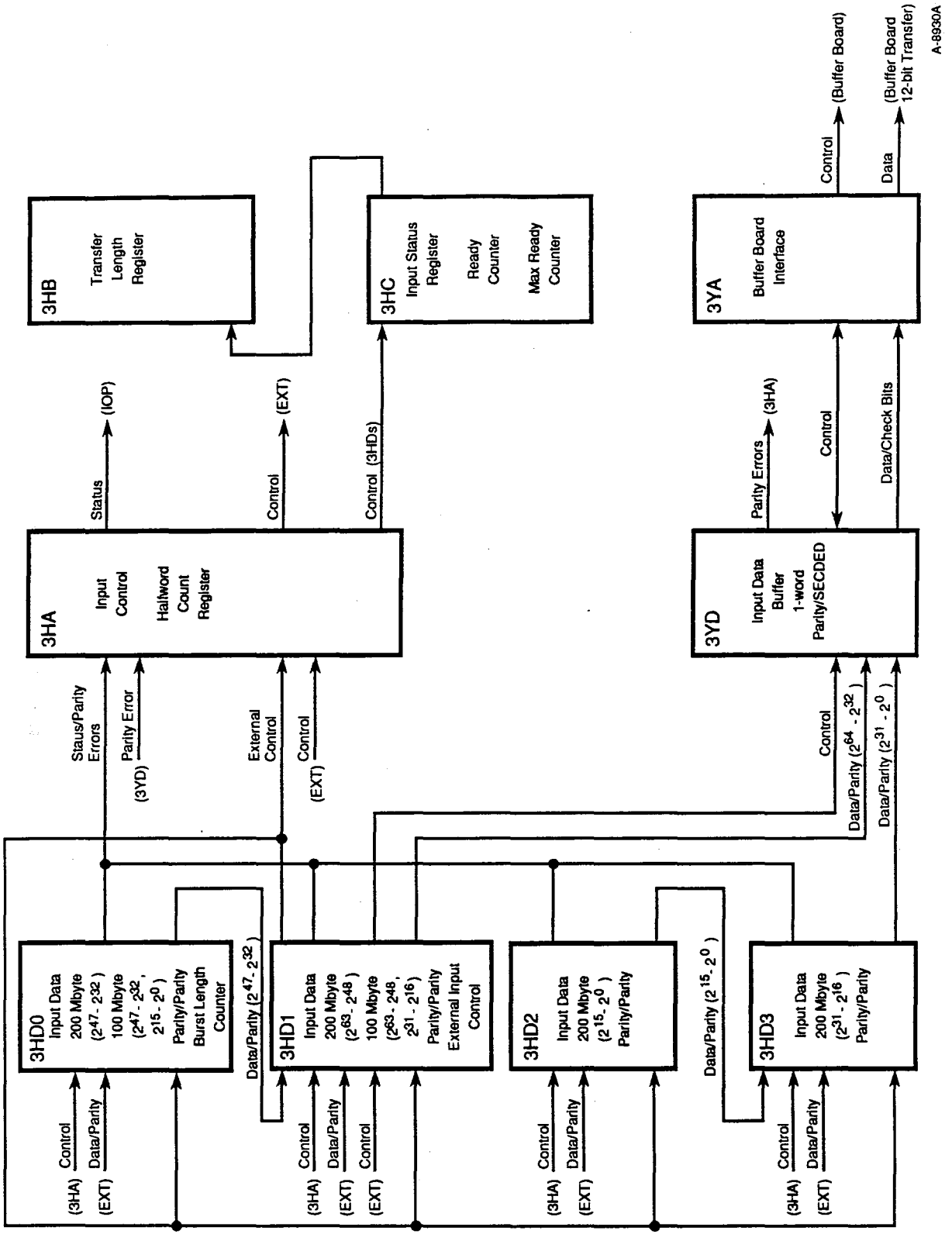


Figure 10-1. HCA3 Block Diagram

The HIPPI outputs data from the buffer board to the destination via the 3YA, 3YE, 3HF, and 3HG options. Refer to Figure 10-2 for a HCA4 block diagram. The buffer board outputs the data and check bits to the 3YA option 12 bits at a time. The 3YA outputs the data to the 3YD. The 3YD performs SECDED and then generates 1 bit of parity for each byte of data. If a SECDED error occurs, the 3YE reports the error to the 3HE. The 3HF options receive the data from the 3YD option and then output the data to the 3HG options. The 3HG options send the data to the destination. If in 32-bit mode only, 3HF0, 3HF1, 3HG0, and 3HG1 options are used.

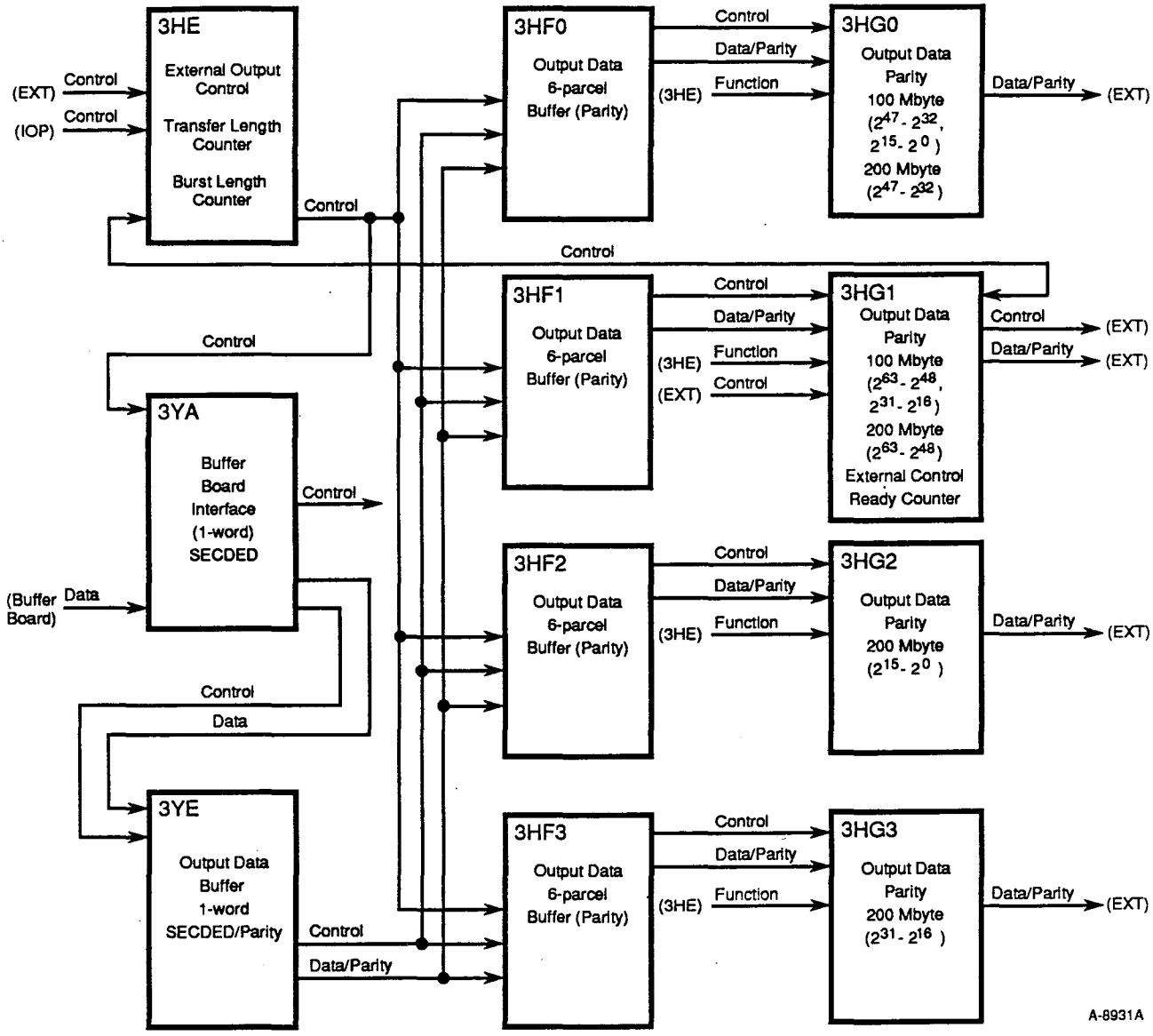


Figure 10-2. HCA4 Block Diagram

HIPPI Channel Protocol

Below are the signals associated with the HIPPI protocol. Refer to Figure 10-3 for a HIPPI protocol block diagram and Figure 10-4 for a HIPPI control and data sequence.

- Interconnect signal. Both the source and the destination have an Interconnect signal. It ensures that the other device is powered on and the cables are connected.

- Request signal. The Request signal is asserted by the source and requests to send data to destination. The I field is sent with the Request and contains information about the transfer.

- Connect signal. The Connect signal is asserted by the destination to indicate to the source that it is operational and can accept data. When the Connect is sent, the destination latches the I field.

- Packet signal. The Packet signal is asserted by the source in response to the Connect sent by the destination. Packet states that the source has one or more bursts to send.

- Ready signal. The Ready signal is asserted by the destination to indicate that one Burst can be sent. It must be negated before the end of the Burst.

- Burst signal. The Burst signal is asserted with the first word of the burst and negated following the last word of the Burst. If the source received another Ready, it can immediately send the next Burst. A Burst is 256 64-bit word. There can be one short Burst with each Packet signal. The Burst is usually the first or last signal. Refer to Table 10-3 for IOS-E and HIPPI data bits.

- Clock signal. The Clock signal is sent by the source to latch the data to the destination. The data is latched on the falling edge. The Packet, Burst, and data change states on the rising edge. The Clock is a symmetrical 25 MHz pulse.

Table 10-3. IOS-E and HIPPI Data Bits

Byte	IOS-E	HIPPI (100)	HIPPI (200)	Cable 100/200
0	$2^{63} - 2^{56}$	$2^{31} - 2^{24}$	$2^{31} - 2^{24}$	A/A
1	$2^{55} - 2^{48}$	$2^{23} - 2^{16}$	$2^{23} - 2^{16}$	A/A
2	$2^{47} - 2^{40}$	$2^{15} - 2^{8}$	$2^{15} - 2^{8}$	A/A
3	$2^{39} - 2^{32}$	$2^{7} - 2^{0}$	$2^{7} - 2^{0}$	A/A
4	$2^{31} - 2^{24}$	$2^{31} - 2^{24}$	$2^{63} - 2^{56}$	NU/B
5	$2^{23} - 2^{16}$	$2^{23} - 2^{16}$	$2^{55} - 2^{48}$	NU/B
6	$2^{15} - 2^{8}$	$2^{15} - 2^{8}$	$2^{47} - 2^{40}$	NU/B
7	$2^{7} - 2^{0}$	$2^{7} - 2^{0}$	$2^{39} - 2^{32}$	NU/B

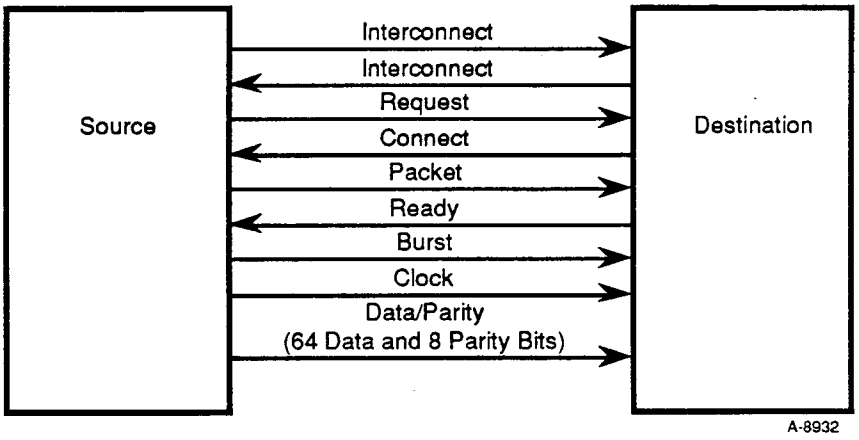
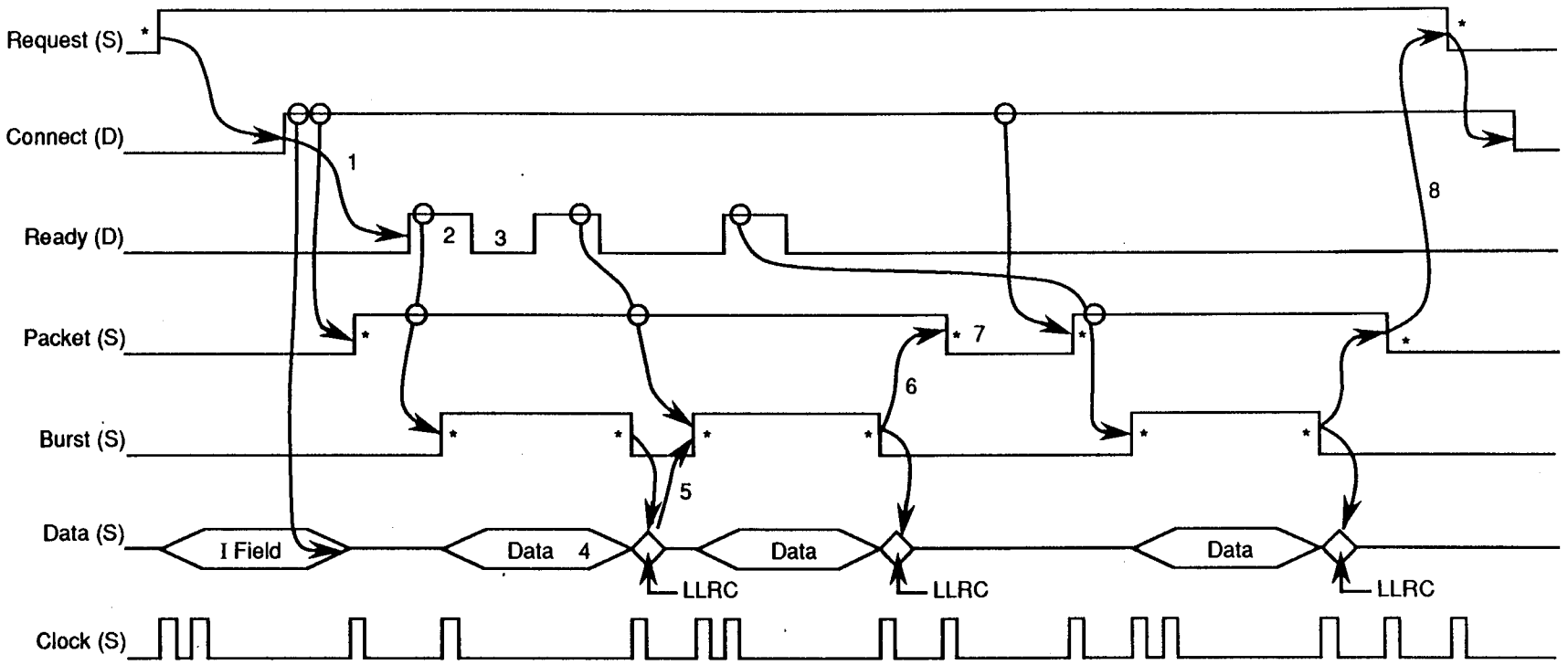


Figure 10-3. HIPPI Protocol



1. 4 CP Minimum — Connect - Ready
2. 4 CP Minimum — Ready Asserted
3. 4 CP Minimum — Ready Negated
4. 1 CP Minimum — 1 Word (Maximum Burst 256)
5. 2 CP Minimum — LLRC - Next Burst
6. 1 CP Minimum — End Burst - End Packet
7. 2 CP Minimum — End Packet
8. 1 CP Minimum — End Packet - End Request

* The source changes state on the rising edge, but the destination samples it on the falling edge.

A-8933

Figure 10-4. HIPPI Control and Data Sequence

HCA3 HIPPI Data In Sequence

The following is a description of HIPPI data input sequence. The HIPPI input transfer uses the HCA3 quarter board. Refer to Figure 10-5 for a HIPPI block diagram.

1. Go IOP Function. The IOP sends Go IOP Function to a specific channel pair. When the channel receives the signal, it decodes the IOP Function Data. The IOP Function Data is the modifier bits this clock period (CP) and the command on the next CP. If needed, for the next 4 CPs the IOP Function Data is the accumulator data.

   IOP - The 3AS sends Go IOP Function (R33 or R34) and the 3AQ sends IOP Function data (R25 - 28 or R30 - 33) for channels 30, 31 and 34, 35. The IOP Function Data is sent to the HCA3 4 bits at a time.

   3HA - The 3HA receives the Go IOP Function (I4) and decodes the IOP Function Data (I0 - 3). After decoding a command 5, the 3HA loads the halfword count register and then sets the busy flag and clears the done flag.

2. Request. The Request (3HA I18) is asserted by the source and is requesting to send data to the destination. The I field is received with the Request and contains information about the transfer. The Request is detected with a command 12.

3. Connect. The Connect is asserted by the destination to indicate to the source that it is operational and can accept data. When the Connect is sent, the destination latches the I field.

   3HA - The 3HA sends a Connect (R13) to the 3HD and 3HC options and a Connect (R10) to the source after decoding a command 4 with accumulator bit 2^0 set and the Request (I18) asserted.

   3HDs- The 3HD options latch the I field after receiving Connect (I47) and hold it until a Read I Field (I46) is received from the 3HA. The 3HD options output the I field (R26 - 29) to the 3HA. Refer to Table 10-4 for data and I field bits.

   3HC - The Connect (I18) clears the ready counter and the max ready counter on the 3HC.

Table 10-4. Data and I Field Bits

Option	Mode	IOP Data or I Field Bits	Cable
3HB0	100/200	$2^{47} - 2^{32}, 2^{15} - 2^{0}/2^{47} - 2^{32}$	A/A
3HD1	100/200	$2^{63} - 2^{48}, 2^{31} - 2^{16}/2^{63} - 2^{48}$	A/A
3HD2	NU/200	Not used $/2^{31} - 2^{16}$	NU/B
3HD3	NU/200	Not used $/2^{15} - 2^{0}$	NU/B

4. Ready. The Ready is asserted by the destination to indicate that one burst can be sent. It must be negated before the end of the burst.

   3HC - The 3HC option sends Enable Ready (R20) if the max ready count is greater than the ready count. The ready counter is incremented with each Ready and decremented with each Burst signal. The max ready count is equal to 77_8 minus the unserviced packet interrupts.

   3HA - The 3HA option sends a Ready (R11) to the source when the HCA3 can accept data and to Increment Ready Count (R28) to the 3HC.

5. Packet. The Packet is asserted by the source in response to the Connect sent by the destination. The Packet signal states that the source has one or more Bursts to send.

   3HD1- The 3HD1 option receives the Packet (I38) from the source and then fans it out (R18) to 3HB and 3HD0-3.

   3HB - The 3HB option enables the transfer length counter after receiving Packet (I3).

   3HDs- The 3HD options receive Packet (I44) at the same time and wait for Burst (I43).

6. Burst. The Burst is asserted with the first word of the Burst and negated following the last word of the Burst. If the source received another Ready it can immediately send the next Burst. A Burst is 400_8 32-bit halfwords in 100-Mbyte mode or 400_8 64-bit words in 200-Mbyte mode. There can be one short Burst with each Packet signal. It is usually the first or last Burst.

   3HD1- The 3HD1 option receives the Burst (I36) from the source and fans it out (R17) to 3HB and 3HD0-3. For the next CP the 3HD1 sends a Start Burst (R30) to the 3HA and 3HC.

3HB - The Burst (I2) enables the incrementing of the transfer length counter.

3HA - After receiving Start Burst (I57), the 3HA sends Start a or Start b to the 3YD and decrements the halfword count by 400_8 in 100-Mbyte mode or 1000_8 in 200-Mbyte mode.

3HC - The Start Burst (I0) signal decrements the ready counter on the 3HC.

7. HIPPI Clock. The HIPPI Clock is a 25 MHz clock which syncs the data and control with the destination.

3HD1- The 3HD1 option receives the HIPPI Clock (I40) and fans it out to all 3HDs.

3HDs- The 3HD options latch a halfword or a word of data with each falling edge of the HIPPI Clock (I298) if Packet (I44) and Burst (I43) are enabled.

8. Data Valid. The Data Valid signal syncs the HIPPI data to the IOS clock.

3HD1- The 3HD1 option uses the HIPPI and IOS clocks to generate Data Valid (R16), and then fans out Data Valid to all 3HDs. The Data Valid syncs the data to the IOS clock on each of the 3HD options.

3HB - The 3HB option increments the transfer length count with each Data Valid (I0) if Packet (I3) and Burst (I2) are set. The transfer length counter is used for determining final transfer length.

3HD0- The 3HD0 option clears burst length counter after receiving the first Data Valid and then increments the burst length with each Data Valid (I42). When the burst length equals 400_8, the 3HD0 option sets Full Burst (R16).

9. Start a or Start b. The 3HA option sends a Start a or Start b to select the proper pointer.

3HA - The 3HA sends a Start a (R8) for the even channel or Start b (R9) for the odd channel if the channel is active and Start Burst (I57) is received. The even channel uses the a pointer and the odd channel uses the b pointer.

10. Go Data. The 3HD0 sends a Go Data to the 3YD to inform it that there is a word of data being sent.

3HD0- The Go Data signal (R9) is enabled by Packet (I44), Connect (I47), Burst (I43), and HIPPI Clock (I298). It is sent once in 200-Mbyte mode and twice in 100-Mbyte mode for each word.

3HDs- The 3HD1 and 3HD3 options send the data and parity bits to the 3YD after receiving Data Valid (I42). The 3HD0 and 3HD2 options send their data and parity bits to the 3HD1 and 3HD3 options. Refer to Table 10-4 for input data bits. The 3HD options check the input data for parity errors. If there is a parity error (R19) on the input data, the error is reported to the 3HA.

3YD - The 3YD checks the parity and then generates SECDED as the data is assembled into a word. The 3YD reports the parity errors (R20 - 21) to the 3HC.

11. Input Data Buffer Full. The 3YD sends a Input Data Buffer Full to the 3YA requesting to send a word of data.

    3YA - The 3YA receives Input Data Buffer Full (I36) and waits for sync 2. The 3YA then sends a Go Input (R19) to the 3YD.

12. Go Input. The Go Input (I23) enables the 3YD to send a word of data.

13. Start a or Start b. The Start a or Start b signal informs the 3YA which pointer to use.

    3YD - The 3YD sends a Start a (R32) for the even channel or Start b (R33) for the odd channel and a word of data with check bits (R0 - 19).

14. Go a To I/O or Go b To I/O. These signals select the proper mode and increment the address on the buffer board.

    3YA - The 3YA sends Go a To I/O (R17) or Go b To I/O (R18) designated by Start a (I37) or Start b (I38). The 3YA outputs the data (R20 - 31) 12 bits at a time to the buffer board. Perform steps 7 through 14 for each word of data until the Burst is negated.

    The Go a To I/O and Go b To I/O at sync 2 selects the mode. A Go a To I/O at sync 2 selects "a" read and "b" write mode. A Go b To I/O at sync 2 selects "a" write and "b" read mode.

The Go a To I/O and Go b To I/O at sync 3 writes the word into the buffer and increments the "a" or "b" pointer's address. The Go a To I/O at sync 3 increments the "a" pointer's address and writes word to the buffer board. A Go b To I/O at sync 3 increments the "b" pointer's address and writes the word to the buffer board. Refer to Table 10-5 for correct sync time for Go a To I/O and Go b To I/O.

Table 10-5. Go a To I/O and Go b To I/O Sync Time

Channel/Function	Pointer	Mode	Increment Address
Even/Input	a	Go b sync 2	Go a sync 3
Odd/Input	b	Go a sync 2	Go b sync 3
Even/Output	a	Go a sync 2	Go a sync 3
Odd/Output	b	Go b sync 2	Go b sync 3

15. End Burst. The 3HD1 sends the End Burst 1 CP after the source negates Burst.

    3HD - The 3HD options latch the longitudinal length redundancy check (LLRC). Then the 3HD1 option outputs an End Burst (R31) 1 CP after the source negates Burst (I36). The 3HD options report LLRC parity errors (R20) and LLRC checksum errors (R21) to the 3HC.

    3HA - When the halfword count equals zero and End Burst (I47) is received, the 3HA sends a Transfer Length End a or b (R16 or R17) to the 3HC.

    3HB - The 3HB checks for proper burst length after receiving End Burst (I7). If Full Burst (I9) is set when End Burst is received, it is a full burst. If Full Burst (I9) is not set when End Burst is received, the burst is a short burst. If Full Burst (I9) is set before End Burst is received, the burst is too long.

16. End Packet. The 3HD1 sends an End Packet to the 3HC and 3HB 1 CP after the source negates Packet (I38).

    3HC - The 3HC receives End Packet, then writes the status into the status register and decrements the maximum ready count. It also sends Write Enable (R16) and (Random

Access Memory) RAM Address (R10 - 15) to the 3HB. The status (R0 - 5) is read out with a command 12 and accumulator bit 2^0 cleared. After the status is readout, the 3HC increments the max ready counter.

17. Write Register. The Write Register writes the transfer length count into the proper register.

    3HC - When End Packet (I1) is received or Transfer Length Done a (16) or b (I3) is received, the 3HC sends Write Register to the 3HB.

    3HB - The 3HB writes the transfer length count into the register after receiving Write Enable (I16) and Ram Address (I10 - 15). A command 12 with accumulator bit 2^0 set reads this value to the accumulator via the 3HA.

18. Interrupt. The 3HE sends an Interrupt (R7) to the IOP when the halfword count equals zero or a packet interrupt is received and the Channel Interrupt is enabled.

    3HA - The HCA3 will interrupt the IOP if a Packet End is received or the halfword count equals zero and the Channel Interrupt is enabled. The done flag does not have to set. The Packet Interrupt is cleared when a command 12 is received with bit 2^0 of the accumulator cleared. To clear an interrupt caused by a halfword count equal to zero, both command 12s must be issued.

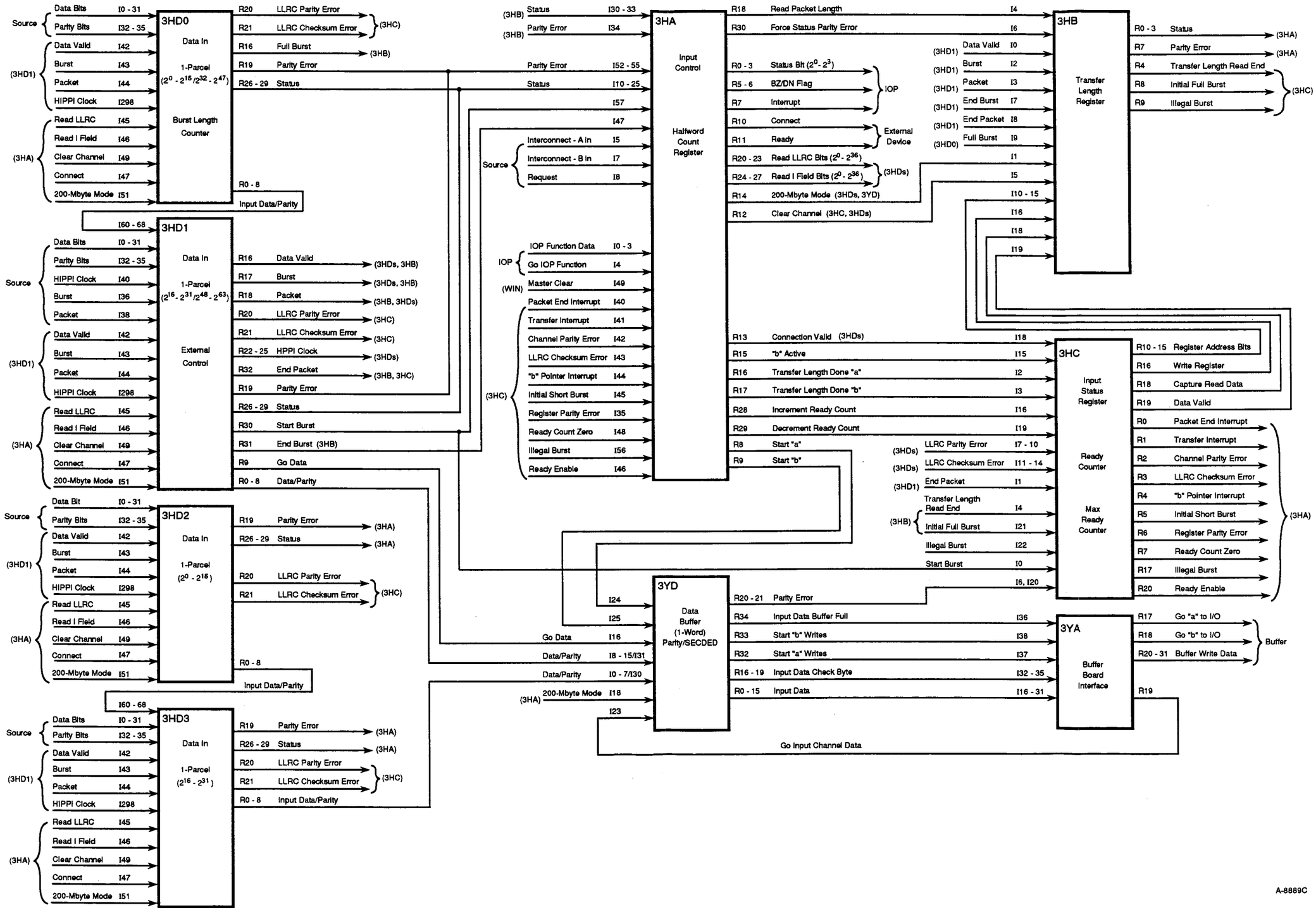


Figure 10-5. HCA3 HIPPI Input Channel Block Diagram and Control

HCA4 HIPPI Data Out Sequence

The following is a sequential description of a HIPPI data out transfer. The HIPPI output transfer uses the HCA4 quarter board. Refer to Figure 10-6 for a HIPPI block diagram.

1. Go IOP Function. The IOP sends Go IOP Function to a specific channel pair. When the channel receives Go IOP Function, it decodes the IOP Function Data. The IOP Function Data is the modifier bits this clock period and the command on the next clock period. If needed, for the next 4 CPs the IOP Function Data is the accumulator data.

   IOP - The 3AP sends the Go IOP Function (R33 or R34) and the 3AO sends IOP Function Data (R25 - 28 or R30 - 33) for channels 32, 33 and 36, 37. The IOP Function Data is sent to the HCA4, 4 bits per clock period.

   3HE - The 3HE receives Go IOP Function (I4), decodes the IOP Function Data (I0 - 3), and fans out Go IOP Function (R30) and IOP Function Data (R26 - 29) to the 3HGs. After decoding a command 5, the 3HE loads the accumulator data into the transfer length register and activates the channel.

   3HGs- The 3HG options receive the Go IOP Function and decode the IOP Function Data. After decoding a command 2 and 3, the 3HG0 and 3HG1 options load the I field register with the accumulator data.

2. Request. The Request is asserted by the source and is requesting a connection with the destination. The 3HE decodes a command 4 with 2^0 accumulator bit set and asserts a Request to the destination.

   3HE - The 3HE sends the Request (R13) to the 3HG1 after decoding a command 4. The Request is sent once to establish a connection with the destination. The I field is sent with the Request.

   3HG1- The 3HG1 passes the Request (R23) to the destination.

3. Connect. The Connect (3HE I8) is asserted by the destination to indicate to the source that it is operational. The I field is latched by the destination when the Connect is asserted. The connection is detected with a command 12, and accumulator bit 2^0 is cleared.

4. Ready. The Ready is asserted by the destination to enable a burst data from the source.

3HG1- After the 3HG1 receives Ready (I8), the 3HG1 increments the Ready counter and sends a Ready Received (R34) to the 3HE.

3HE - The Ready Received signal (I10) enables the 3HE to send a Start Burst (R21).

5. Clear, Start a, and Start b. The Clear signal clears the read pointer and the Start a and Start b signals select the proper pointer.

   3HE - The 3HE sends a Start a (R9) for the even channel or a Start b (R10) for the odd channel. The Start a or Start b and Clear are sent to the 3YA after command 5 is decoded. The Start a or Start b is also sent when a channel finishes, and the HCA4 is a stacking pointer.

   3YA - The 3YA selects the proper pointer and then sends Go a To I/O or Go b To I/O (R17 - 18) to the buffer board to select the mode.

6. Go a To I/O or Go b To I/O. These signals are sent to the buffer board to select the mode and increment the address.

   3YA - The 3YA sends Go a To I/O (R17) or Go b To I/O (R18) designated by Start a (I37) or Start b (I38). The 3YA receives the data and check bits (I0 - 11) 12 bits at a time from the buffer board.

   The Go a To I/O and Go b To I/O at sync 2 selects the mode. A Go a To I/O at sync 2 selects "a" read and "b" write mode. A Go b To I/O at sync 2 selects "a" write and "b" read mode.

   The Go a To I/O and Go b To I/O at sync 3 increments the "a" or "b" pointer's address. The Go a To I/O at sync 3 increments "a" pointer's address. A Go b To I/O at sync 3 increments the "b" pointer's address. Refer to Table 10-5 for the correct sync time for Go a To I/O and Go b To I/O.

7. Buffer Full. The 3HF1 sends Buffer Full enabling the next word of data.

   3HE - If Buffer Full (I12) is not set, the 3HF1 is requesting the next word of data from the 3YA. The 3HE responds with a Data On Its Way signal (R12) and a Go signal (R11).

8. Data On Its Way. The 3HE sends Data On Its Way to inform the 3HF and 3YE options that a word of data is on its the way.

3HE - The 3HE sends Data On Its Way (R12) every 6 CPs if Buffer Full is not set. The burst counter is incremented and transfer length counter is decremented at this time.

9. Go. The 3HE sends a Go signal to the 3YA to enable a word of data from the Buffer Board.

   3HE - The 3HE sends a Go signal if Buffer Full is not set and the word count is not equal to zero.

   3YA - The buffer board is always outputting the next word. The 3YA passes the word of data to the 3YE at proper sync time after receiving Go (I12). The 3YA then sends Go a To I/O (R17) or Go b To I/O (R18) to increment the pointer address.

10. Go Output Data. The Go Output Data is sent to 3YE with each word of data from the 3YA.

    3YE - The 3YE receives Go Output Data (I16) at sync 0 followed by a word of data (I0 - 15). The 3YE performs SECDED on the data and then generates parity for each byte. If a SECDED error occurs, it is reported to the 3HE.

11. Data Available. The 3YE sends Data Available with each word of data sent to the 3HF.

    3HFs- Each 3HF receives Data Available (I6) followed by two 8-bit data transfers with 2 bits of parity. Each 3HF has a 6-parcel data buffer.

12. Start Burst - The 3HE sends Start Burst to the 3HF options with the first word.

    3HFs- The 3HF1 passes the Start Burst (R40) to the 3HG1. At the same time, all 3HFs output the first word of data and parity (R20 - 37) to the 3HGs.

    3HG1 - The 3HG1 decrements the ready counter and fans out Start Burst (R22) to all the 3HG options. Then the 3HG options output the data after receiving Start Burst (I42) and 100-MHz sync (I41).

13. Packet. The Packet is asserted by the source. The Packet states that the source has one or more bursts to send to the destination.

    3HG1- The 3HG1 sends Packet (R36) to the 3HE and Packet (R20) to the destination after receiving Start Burst.

3HE - The 3HE sets the packet status bit after receiving Packet (I5).

14. Burst. The Burst is asserted by source with the first word and negated following the last word of the burst.

3HG1- The 3HG1 asserts the Burst (R19) and then sends a 25-MHz HIPPI Clock and the data to the destination. The 3HG options continue to output data until an End Burst (I38) is received. The LLRC is generated by 3HG options as the data is sent to the destination. Refer to Table 10-6 for output data bits.

Table 10-6. 3HG Options Data and I Field Bits

Option	Mode	IOP Data or I Field Bits	Cable
3HG0	100/200	$2^{47} - 2^{32}, 2^{15} - 2^{0}/2^{47} - 2^{32}$	A/A
3HG1	100/200	$2^{63} - 2^{48}, 2^{31} - 2^{16}/2^{63} - 2^{48}$	A/A
3HG2	100/200	Not used $/2^{31} - 2^{16}$	NU/B
3HG3	100/200	Not used $/2^{15} - 2^{0}$	NU/B

15. Data Taken. The Data Taken signal informs the 3HF1 that a word has been sent to the destination.

3HG1- The 3HG1 sends Data Taken (R33) to the 3HF1, and all the 3HG options send Data Pointers (R30 - 32) to the 3HF options. The 3HG options increment the Data Pointers with each word transferred to the destination. Perform steps 6 through 15 until the end of the burst.

3HF1- The 3HF1 checks the Buffer Full signal when it receives Data Taken (I4).

16. End Burst. The 3HE sends an End Burst with the last word.

3HF1 - The 3HF1 passes the End Burst (R38) to the 3HG1.

3HG1 - The 3HG1 negates the Burst (R40) after receiving End Burst (I38) and outputs the LLRC.

17. End Packet. The 3HE sends End Packet to the 3HF1 to terminate the transfer.

3HF1 - The 3HF1 passes the End Packet (R39) to the 3HG1.

3HG1 - The 3HG1 negates Packet (R20) after receiving End Packet (I39).

18. Interrupt. The 3HE sends an Interrupt (R7) to the IOP when the done flag sets and the Channel Interrupt is enabled. The done flag sets and the busy flag clears when the word count equals zero.

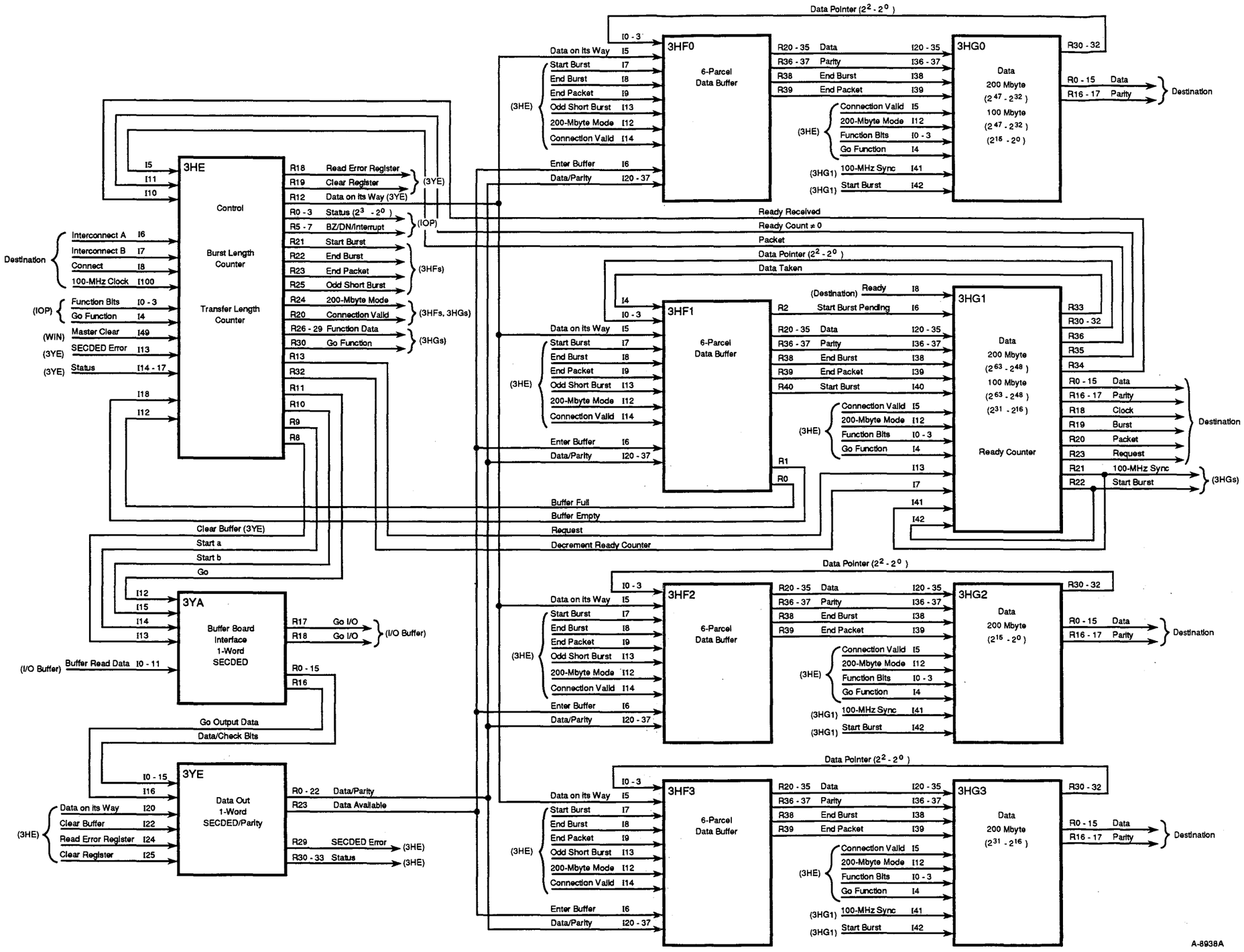


Figure 10-6. HCA4 Block Diagram (HIPPI Output Channel Adapter)

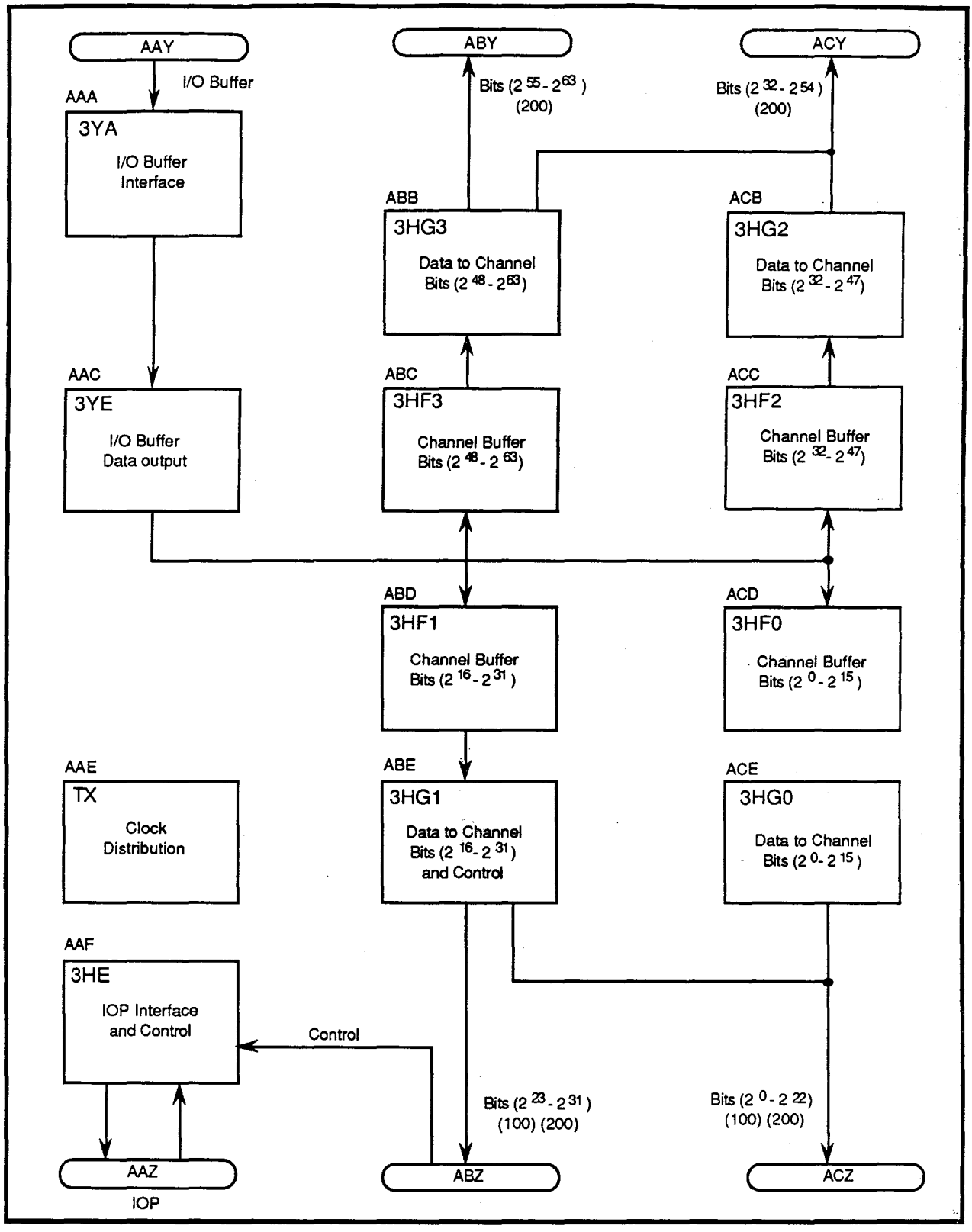


Figure 10-7. HCA4 Quarter Board Option Layout

Cray Research, Inc.
Hardware Publications and Training
770 Industrial Boulevard
Chippewa Falls, WI 54729