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CRAY® COMPUTER SYSTEMS

(PRE- DC/DD-40) ~~MA~~INTENANCE MANUAL

CMM1103000

RECORD OF REVISION

PUBLICATION NUMBER CMM1103000

Each time this manual is revised and reprinted, all changes issued against the previous version are incorporated into the new version and the new version is assigned an alphabetic level.

Every page changed by a reprint with revision has the revision level in the lower righthand corner. Changes to part of a page are noted by a change bar in the margin directly opposite the change. A change bar in the margin opposite the page number indicates that the entire page is new. If the manual is rewritten, the revision level changes but the manual does not contain change bars.

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Revision	Description

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This manual is intended to help Cray Research, Inc. (CRI) field engineers (FEs) maintain the DC-40 disk controller and the DD-40 disk storage device. The DC-40 has been designed and manufactured by CRI to control the DD-40, which consists of XMD spindles. This is a CRI company private document and should not leave the site.

This manual consists of seven sections. The following is a description of each section:

Section	Description
1	Overview - introduces the DC-40 and DD-40
2	DD-40 Drives - describes the XMD-III drives of the DD-40
3	Cabling - describes the cabling for the DC-40 and DD-40
4	Theory of Operations - describes the DC-40 modules
5	DC-40 Cooling System - describes the cooling system of the DC-40
6	DC-40 Maintenance - describes how to maintain the DC-40
7	Trouble shooting - provides trouble shooting procedures for the DC-40 and the DD-40

The following publications are relevant to this manual:

- HR - 0077 Disk Systems Hardware Reference Manual
- HR - 0080 Cray Peripheral Equipment Site Planning Reference Manual

Complete details of the DD-40 are contained in the following vendor manuals:

- CDC Publication Volume 1 - 83325090 (CRI Publication Number xxxxxxxxxx)
- CDC Publication Volume 2 - 83325100 (CRI Publication Number xxxxxxxxxx)
- CDC Publication Volume 3 - 83325110 (CRI Publication Number xxxxxxxxxx)

CONTENTS

FIGURES

TABLES

TABLES (continued)

The following devices are components of the I/O Subsystem (IOS) of a Cray computer system:

- I/O Processor (IOP)
- Disk Controller Unit-5 (DCU-5)
- DC-40 disk controller (DC-40)
- DD-40 disk storage device (DD-40)

The DD-40 stores information from a Cray computer system. The DC-40 is the interface between the DCU-5 and the DD-40. The DCU-5 is the interface between the IOP and the DC-40.

When the IOP executes a write request, the DC-40 receives the data from the channel, buffers it, and passes it to the DD-40. On a read request, the DC-40 retrieves the data requested from the DD-40, buffers it, and passes it to the channel. The DC-40 does error checking on the data that is read or written and relays status messages to the IOP.

//

WARNING

This device operates in accordance with FCC Part 15, Subpart J Rules.

//

1.1 COMPONENTS OF THE DC-40

The DC-40 is designed and manufactured by CRI. It occupies a separate cabinet and consists of the following components:

- Four controllers
- Four power supplies
- One cooling system

Each controller is functionally independent and can control up to two DD-40's. When there are two DD-40's on a controller, one is called the primary DD-40 and the other the shadow DD-40. Each DD-40 consists of four XMD spindles. Because a controller in the DC-40 can control two DD-40's, it can control eight spindles. A DC-40, consisting of four controllers, can control 32 spindles.

Each controller in the DC-40 consists of the following five types of modules:

- 2EI channel interface module
- 2EM disk multiplexer module
- 2EB full-track buffer module
- 2EK disk-data and error-correction module
- 2EJ disk controller module (four per controller)

There are four 2EJ disk controller modules and one of each of the other modules in each controller in the DC-40. Each 2EJ module controls read and write exchanges for a single spindle in the DD-40. The 2EJ module has a single cold plate; all the other modules have a double cold plate.

Figure 1-1 shows the interrelationship of the modules of the DC-40. This figure shows the modules of a single controller of the DC-40.

The DC-40 is cooled by a vapor compression type of cooling system. This system consists of a compressor, a condenser, two evaporators, an accumulator, valves, filters, piping, guages, and controls. The refrigerant used in the cooling system is R-22. Heat is absorbed by the liquid refrigerant from the modules and passed from the refrigerant to a water supply.

1.2 IOS CONFIGURATION

Figure 1-2 shows an IOS with a single DC-40 and a primary and a shadow DD-40 connected to DC-40 controller 0. There are four controllers in the DC-40 and each of these can control a primary and a shadow DD-40. Each DD-40 has four spindles (A, B, C, and D).

One IOP can control up to four DCU-5's. Each DCU-5 can control up to four controllers in the DC-40. Thus one IOP can control up to 16 controllers (that is, up to four DC-40's). A full IOS configuration is as shown in figure 1-3. A single controller in the DC-40 can control up to 8 spindles, a DC-40 can control up to 32 spindles, and an IOP can control up to 128 spindles.

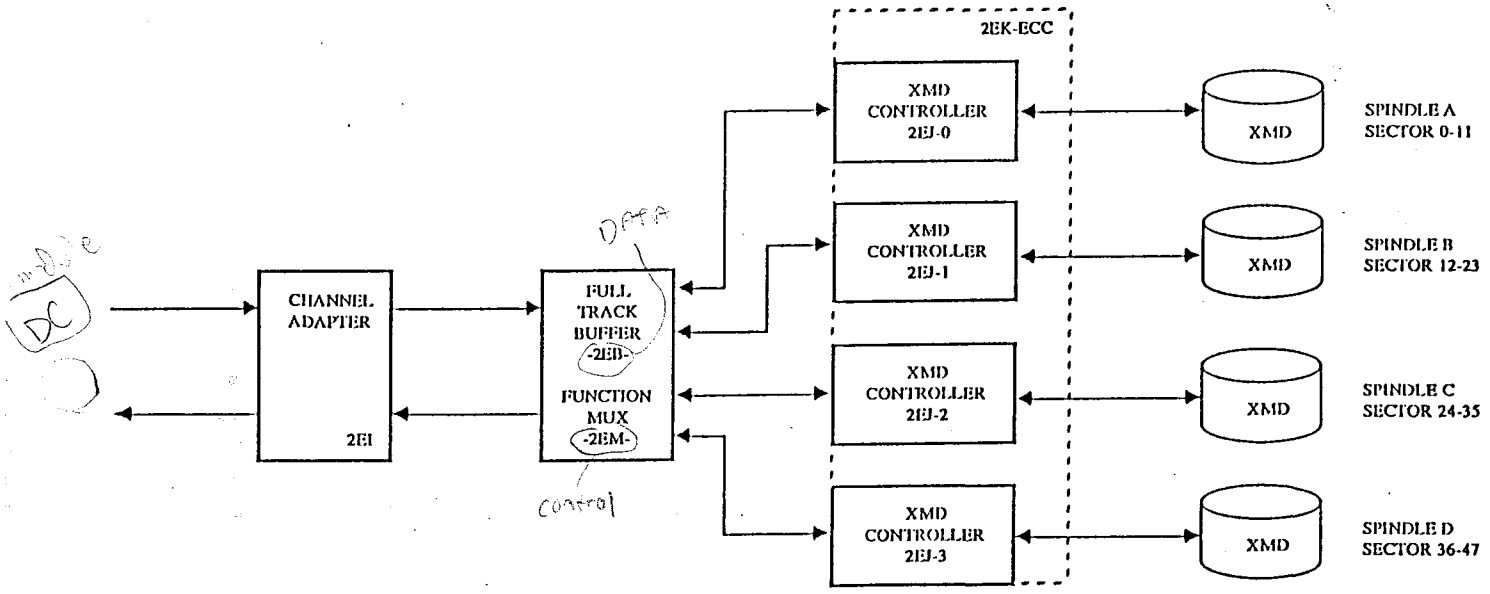

Figure 1-1. DC-40/DD-40 Block Diagram

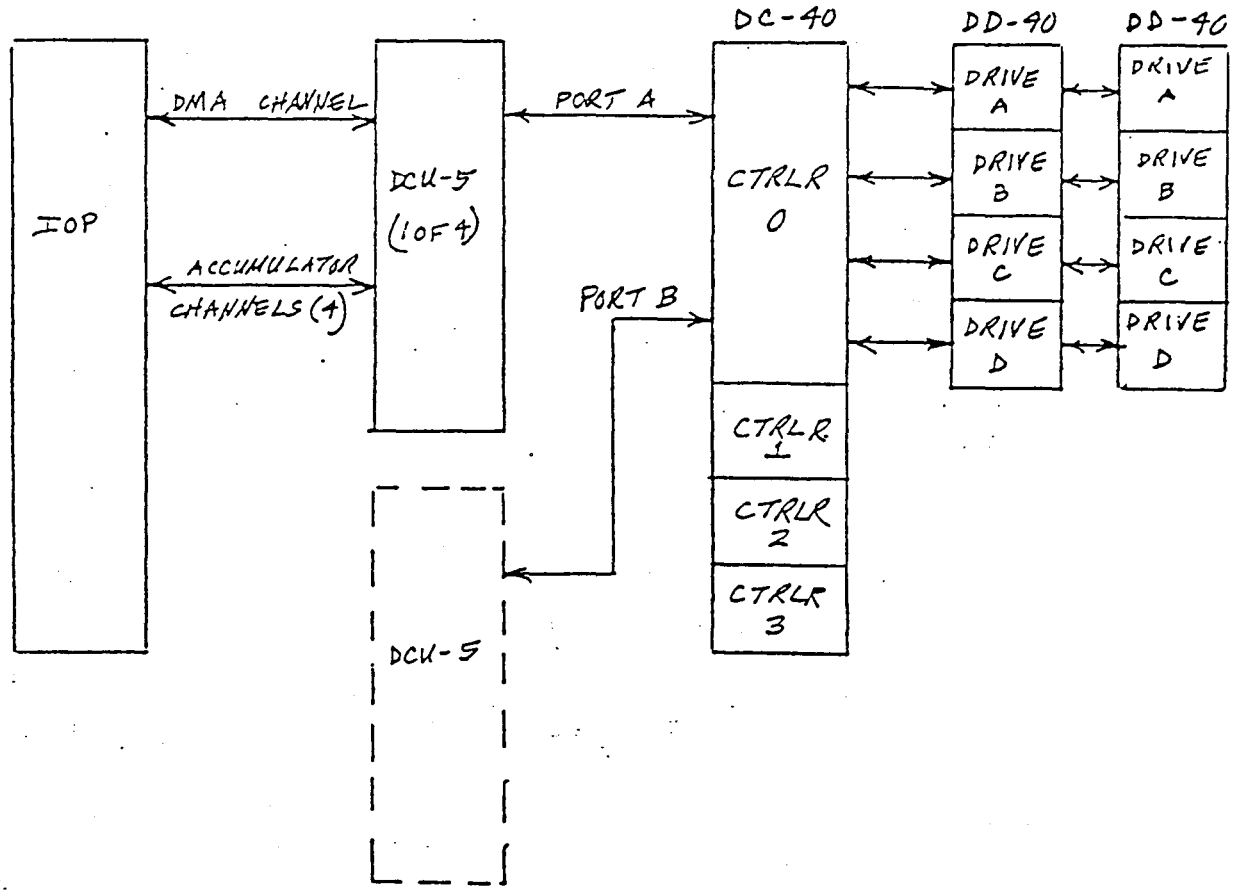

Figure 1-2. IOS Configuration

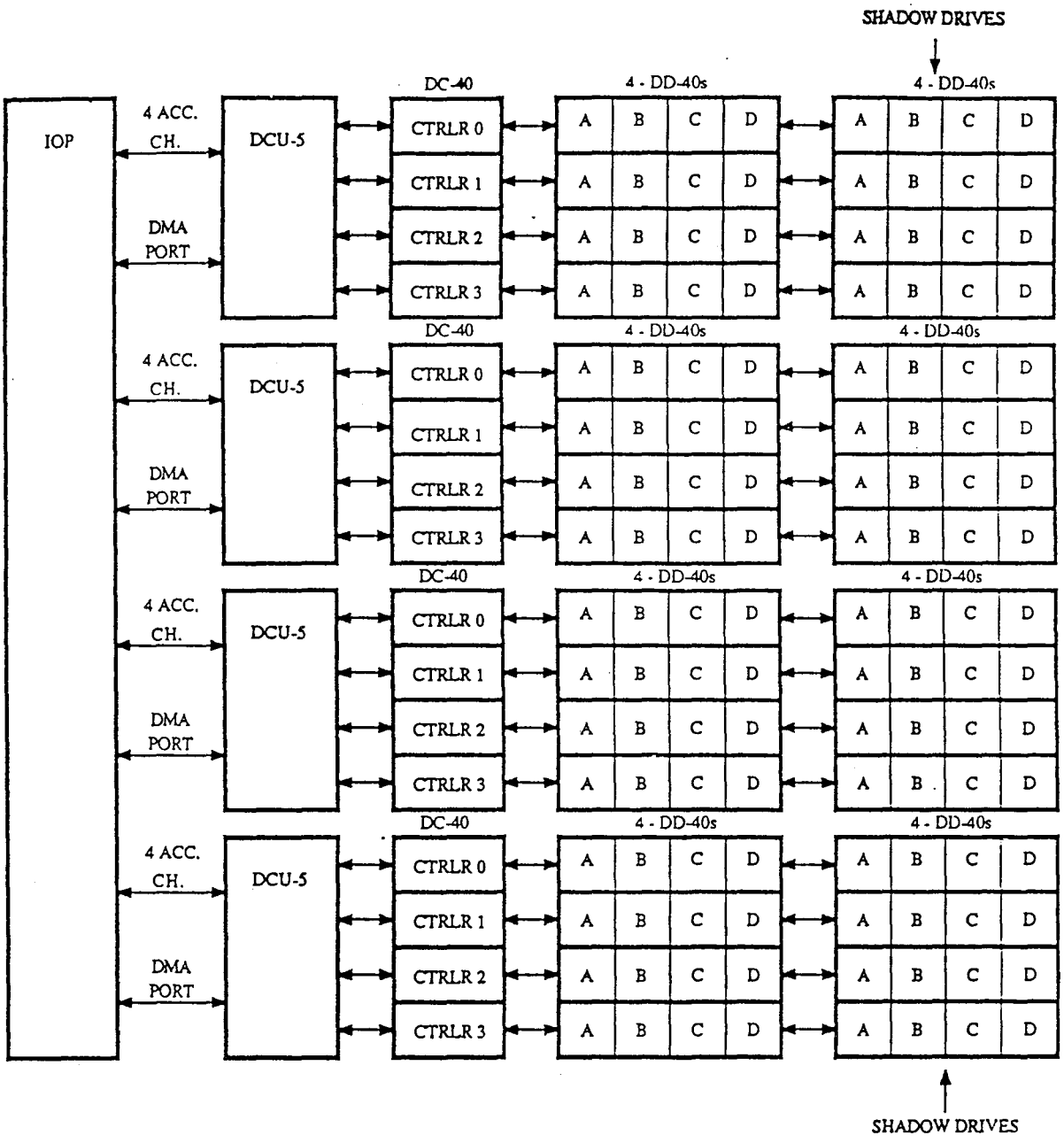

Figure 1-3. Maximum IOS Configuration

1.3 DC-40/DD-40 SPECIFICATIONS

This section discusses the following specifications of the DC-40 and DD-40:

- Floor loading
- Heat rejection
- Power requirements
- DD-40 XMD spindle specifications

1.3.1 FLOOR LOADING

The DC-40 cabinet weighs 1100 lbs (500 Kg) and takes up 7.3 sq ft (.68 sq m) of floor space. The DC-40 average floor loading is 150 lbs per sq ft (735 Kg per sq m). Figure 1-4 shows the DC-40 cabinet.

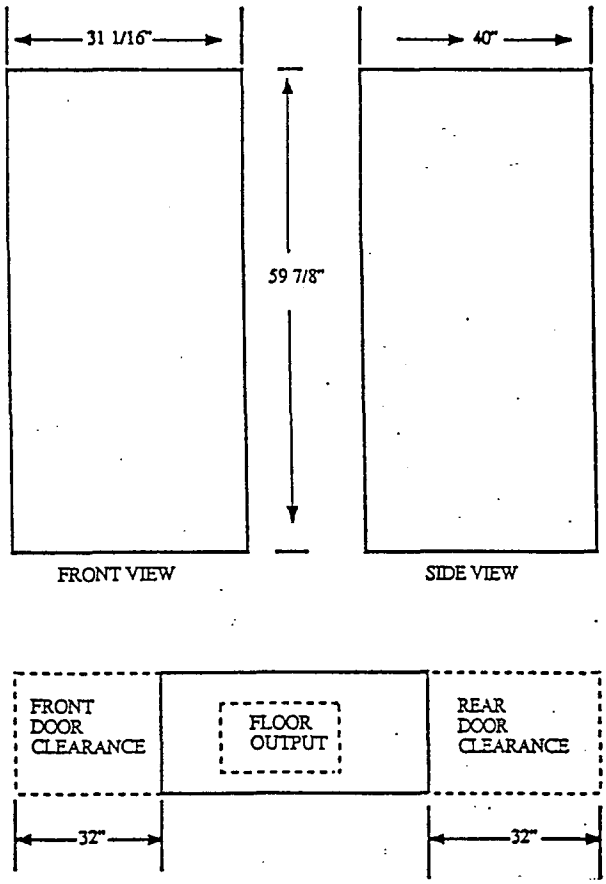

Figure 1-4. Dimensions of the DC-40 Cabinet

The DD-40 cabinet weighs 800 lbs (364 Kg) and takes up 8.7 sq ft (.81 sq m) of floor space. The DD-40 average floor loading is 92 lbs per sq ft (449 Kg per sq m). Figure 1-5 shows the DD-40 cabinet.

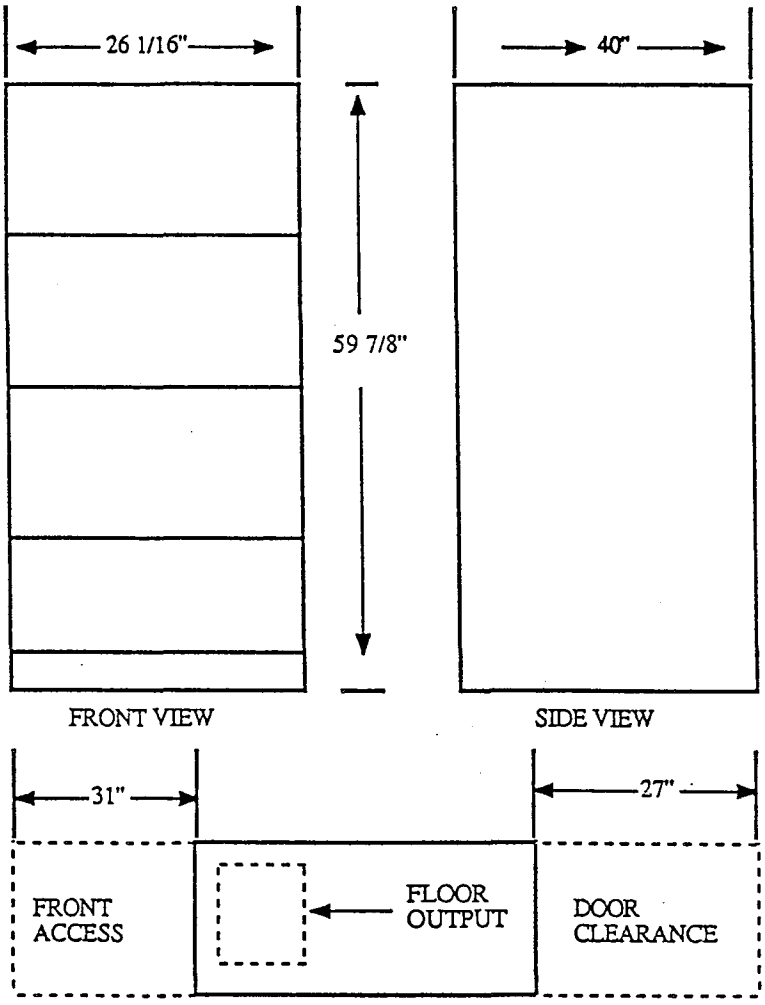

Figure 1-5. Dimensions of the DD-40 Cabinet

1.3.2 HEAT REJECTION

The DC-40 generates approximately 28,000 BTUs per hour. It is freon-cooled by a self-contained refrigeration unit. The refrigeration condenser unit is cooled by an external water supply.

The DD-40 generates approximately 8,000 BTUs per hour. The heat generated by the DD-40 must be handled by the equipment room air conditioning.

1.3.3 DC-40/DD-40 POWER REQUIREMENTS

The following are the electrical power requirements for the DC-40 and the DD-40:

DC-40:

40A/phase, 120/208, 3 phase Y, 5-pin power plug: IEC 309

DD-40:

208 VAC, 3 phase, 5-pin power plug: NEMA L21 through 20P

The nominal operating current for the DD-40 is:

Phase A-B 2.8A
Phase B-C 2.8A
Phase C-A 5.6A

The nominal startup current for the DD-40 is:

21.4 A/phase for 3.5 seconds

Spindles A, B, and C start simultaneously, presenting a balanced load to the 3-phase line. Spindle D is started after spindles A, B, and C are up to speed.

1.3.4 DD-40 XMD SPINDLE SPECIFICATIONS

Table 1-1 lists the specifications for the XMD spindles of the DD-40.

Table 1-1. Specifications for the XMD Spindles

Characteristic	Specification
Number of spindles per DD-40	4
Cylinders per spindle	1418 + 2 maintenance 2611_8 +2
Cylinders per DD-40	1418 + 2 maintenance
Data heads per spindle	19
Buffer capacity	48 sectors
Sectors per track	48
Sectors per cylinder	912
Data bytes per sector	4096
Bytes per spindle, formatted	1,324 Mbytes
Bytes per DD-40, formatted	5,297 Mbytes
Transfer rate	86 Mbits/s
Ports per DD-40	1
Drives active at one time	4
Minimum number of operational drives required per cabinet	4

1.4 DC-40 CONTROLS AND INDICATORS

This section describes the controls and indicators for the DC-40.

Figure 1-6 identifies the controls and indicators of the power supply and refrigeration system control panel. Table 1-2 describes the function of the controls and indicators.

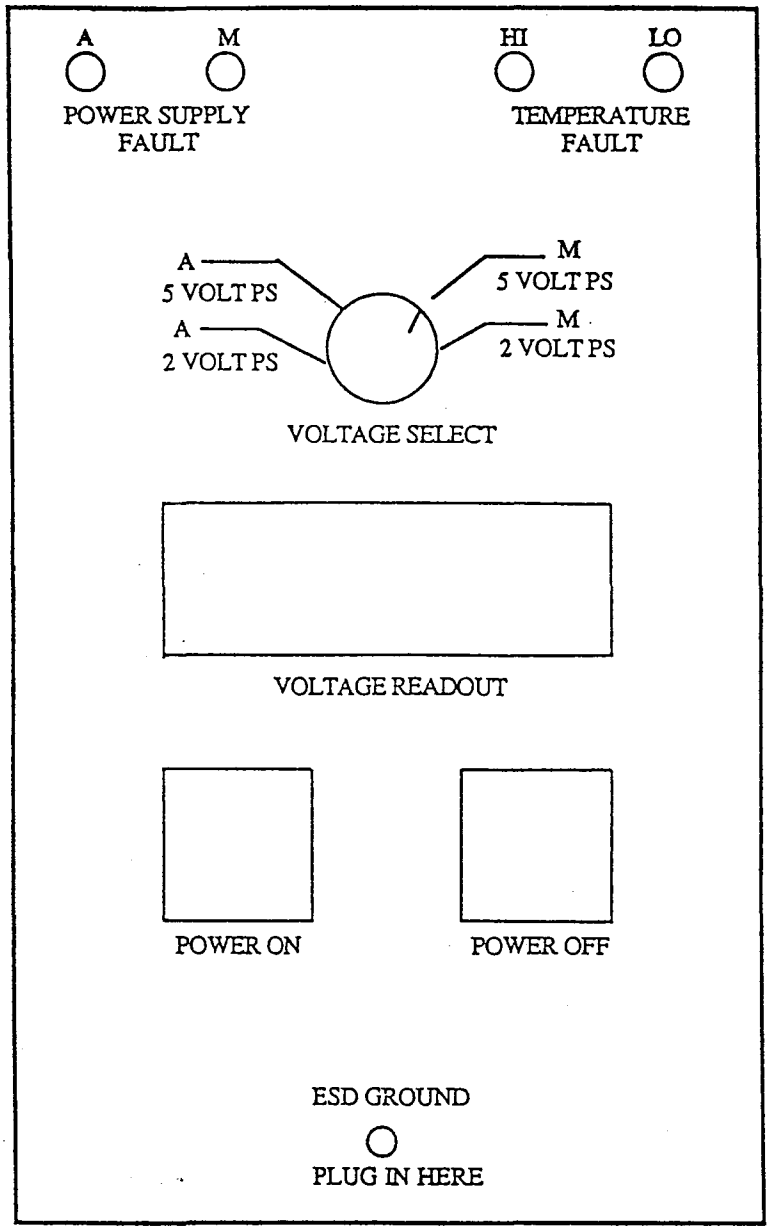

Figure 1-6. Power Supplies and Refrigeration System Control Panel

Table 1-2. Power Supplies and Refrigeration System Control Panel Functions

Name	Function
POWER SUPPLY FAULT A,M indicator	Indicate out-of-range fault in power supplies A and M. A is the lower power supply. M is the upper power supply.
TEMPERATURE FAULT, HI, LO indicator	Indicate out-of-range temperatures within the DC-40.
VOLTAGE SELECT switch	Selects one of four power supply outputs to be displayed at the VOLTAGE READOUT METER.
VOLTAGE READOUT meter	Indicates the value of the selected power supply on the digital voltmeter.
POWER ON switch	Enables power supplies to provide power to the modules and opens the cooling system solenoid.
POWER OFF switch	Disconnects the power supplies from modules and puts the refrigeration system into the pump-down cycle. After about three seconds of pump-down, the compressor is automatically shut off.
ESD GROUND receptacle	Provides ground connection for draining off electrostatic discharge (ESD).

Figure 1-7 identifies the controls and indicators of the control panel for a single DC-40 controller. Table 1-3 describes the function of the controls and indicators. The controls and indicators shown for controller 0 are the same for controllers 1, 2, and 3.

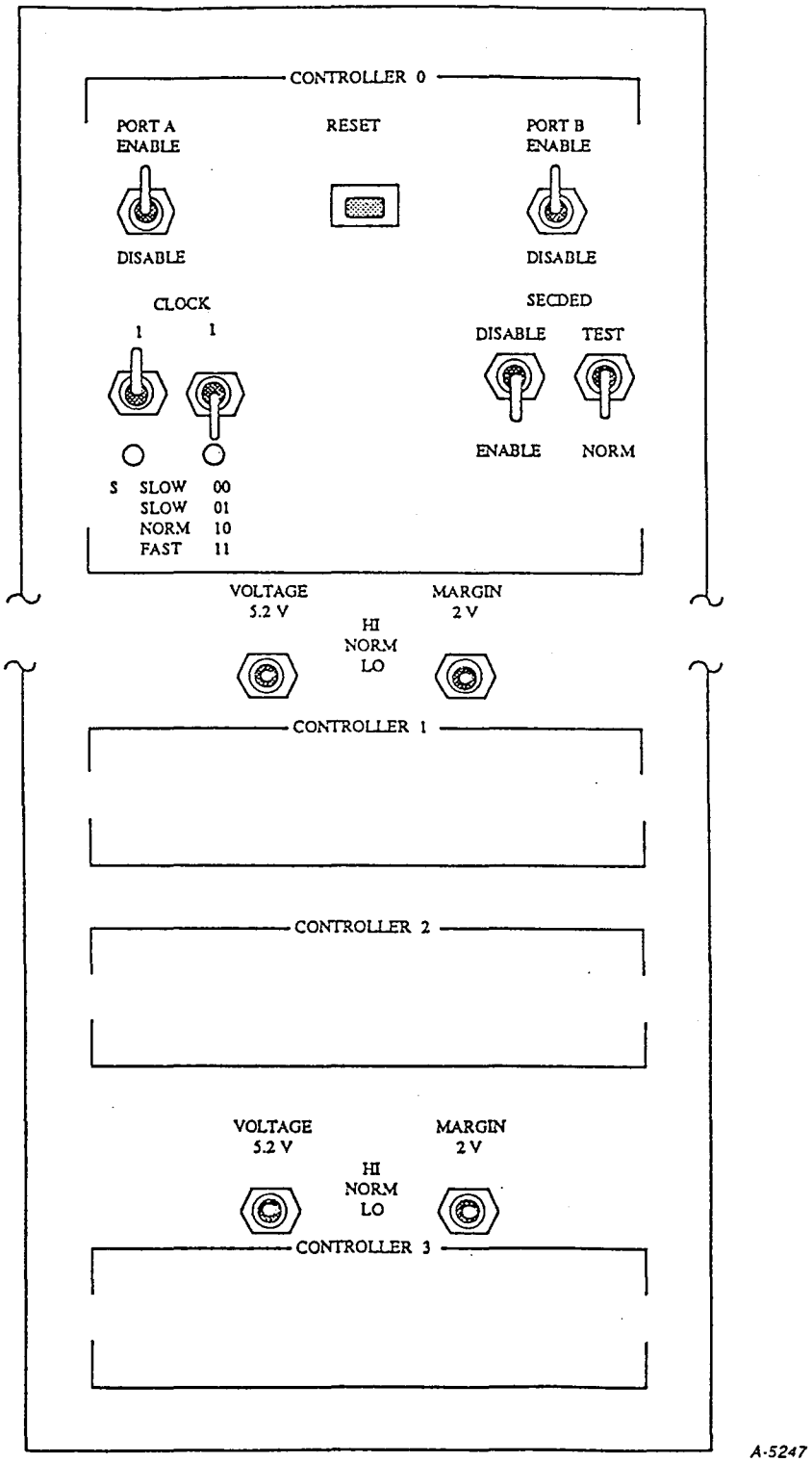

Figure 1-7. DC-40 Control Panel

Table 1-3. DC-40 Control Panel Functions

Name	Function
Port A Enable/ Disable switch	Allows port A to use the DC-40 when in the ENABLE position. Prevents port A from using the DC-40 when in the DISABLE position.
Port B Enable/ Disable switch	Allows port B to use the DC-40 when when in the ENABLE position. Prevents port B from using the DC-40 when in the DISABLE position. Both port A and port B may be enabled at the same time.
Clock 1,0 switch	Selects the logic clock speed.
Margin -5.2V -2.0V switch	Selects the voltage levels of the logic power supply outputs.
SECDED Enable/ Disable switch	Activates single error correction double error detection (SECDED) when in the ENABLE position. Inactivates SECDED when in the DISABLE position.
SECDED Test/ Norm switch	Allows testing of SECDED by forcing 0's to be written into check bits.

Figure 1-8 identifies the controls of the DC-40 power panel. Table 1-4 describes the function of the controls. (This panel is located inside the rear of the DC-40 cabinet.)

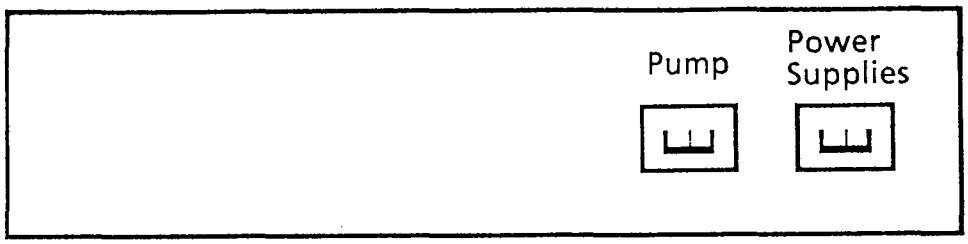

Figure 1-8. DC-40 Power Panel

Table 1-4. DC-40 Power Panel Functions

Name	Function
COMPRESSOR circuit breaker	Applies primary power to the compressor and control circuitry.
POWER SUPPLIES circuit breaker	Applies primary power to the power supplies. Observe the warning below.

//

WARNING

When powering off the DC-40, before turning off the COMPRESSOR and POWER SUPPLY circuit breakers on the DC-40 power panel, you must first press the POWER OFF switch on the power supply and refrigeration system control panel. The refrigeration system must be allowed to power down (about 3 seconds) before removing all power in order to prevent damage to the compressor at start up.

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DD-40 DISK DRIVE

DD-40 DISK DRIVE

Hardware Training Aid

HTA-0859

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PUBLICATION NUMBER
HTA-0859

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Revision	Description
	August 1988 - Original printing.
A	September 1988. Page 7 added.

This device is exempt from the technical requirements of the FCC's Part 15 Subpart J Rules pursuant to Section 15.801(c).

OBJECTIVES - Overview

Upon completion of this section, the student will be able to:

- Describe each disk channel with respect to DCU-5 modules, DC-40 modules, and DD-40 drives
- Give specifications on the DC/DD-40 configuration
- Briefly describe each of the DC/DD-40 commands and functions

OBJECTIVES - DD-40

Upon completion of this section, the student will be able to:

- Describe the functions of the DD-40, (seek, load, RTZ, write and read)
- Follow the flow charts and diagrams and know which part of the drive is involved with each step
- Explain errors that can occur with each of the drive functions
- Interpret the drive's selected status. (Refer to troubleshooting section)
- Explain the purpose of each part of the Sector Format
- Demonstrate the switch settings for the sector count and I/O Board switch settings

DC4004W103M

OBJECTIVES - Cabling

Upon completion of this section, the student will be able to:

- Correctly cable the DCU-5, DC-40 and DD-40 together
- Identify and describe each signal on the A and B cables between the DC-40 and DD-40
- Locate the part numbers that identify different cables for the DC-40 and DD-40
- Re-cable DD-40 spindles for fault isolation

OBJECTIVES - DC-40

Upon completion of this section, the student will be able to:

- With the aid of the Boolean and diagrams, describe the major functions of the modules
- Follow the read and write paths through the DC-40 and give a description of what each module does during a read and write
- Determine the bad buffer chip, given the syndrome bits
- Interpret the error bits that are in General Status and Buffer Status and know the module where the bits originate
- Explain the function of each of the fields in the PROM sequencer
- Follow a sequence through the PROM Micro Code
- Explain how defect detection works

OBJECTIVES - Lab

Upon completion of this section, the student will be able to:

- Load and run the DC-40 diagnostics and give an explanation of what each test section does
- Set up diagnostics to check out a given number of cylinders and heads
- Execute diagnostic tests from the Fault Display panel
- Use the micro tester to write test and execute diagnostics to the DC-40 and DD-40
- Take refrigeration readings and know how to make adjustments
- Demonstrate adding a flaw to the user flaw table with a defect and moving a defect pad
- Demonstrate writing and reading the O.S. flaw table

DS-40 Commands

A REGISTER		B REGISTER		DESCRIPTION
1DD000	Int. Addr.	000000	00000U	Release
1DD001	Int. Addr.	000000	00000U	Release Opposite and Select
1DD010	Int. Addr.	000000	00000U	Reserve
1DD020	Int. Addr.	000000	000000	Clear Faults
1DD021	Int. Addr.	000000	000000	Reset
1DD030	Int. Addr.	000000	000000	Return to Zero
1DD040	Int. Addr.	000000	Status	Select Status
1DD050	Int. Addr.	000000	000000	General Status
1DD070	Int. Addr.	000000	Diag. mode	Diagnostic Select
1DD100	Int. Addr.	000000	Offsets Cyl. Addr.	Select Cylinder
1DD101	Int. Addr.	000000	Head Addr.	Select Head
	READ			
1DD200	Int. Addr.	000000	RRRRRR	Read disk data (with Read Ahead Enabled)
1DD201	Int. Addr.	000000	RRRRRR	Read ID
1DD202	Int. Addr.	000000	RRRRRR	Read Absolute
1DD203	Int. Addr.	000000	RRRRRR	Read Buffer (16 parcels)
1DD204	Int. Addr.	000000	RRRRRR	Read Syndrome Block
1DD205	Int. Addr.	000000	RRRRRR	Compute Correction Vector
1DD206	Int. Addr.	000000	RRRRRR	Track Header
1DD210	Int. Addr.	000000	RRRRRR	Read disk data (with Read Ahead Enabled
1DD212	Int. Addr.	000000	RRRRRR	Read Buffer (2048 parcels)
	WRITE			
1DD300	Int. Addr.	000000	WWWWWW	Write disk data (Write Behind Enabled)
1DD301	Int. Addr.	000000	WWWWWW	Write ID
1DD302	Int. Addr.	000000	WWWWWW	Write Defective ID
1DD303	Int. Addr.	000000	WWWWWW	Write Buffer (16 parcels)
1DD304	Int. Addr.	000000	WWWWWW	Write Zero ECC
1DD310	Int. Addr.	000000	WWWWWW	Write disk data (Write Behind Disabled)
1DD314	Int. Addr.	000000	WWWWWW	Write Buffer (2048 parcels)
1DD370	Int. Addr.	000000	PPPPPP	Echo Parameter

DC4004/117

DD-40 COMMANDS

		ACCUMULATOR BITS	FUNCTION
*	DIA:1	Drive Control Functions	
		01000U	Unit select
		010007	Port select
		04hh00	Head select
		07SSSS	Status select (5 status words available)
		100000	General status
		11000d	Diagnostic select (2 options available to perfom Bus-In Parity errors and Status Parity errors)
		130000	Reset drive
		140000	Clear faults on drive
		150000	Return to zero
		16000U	Release opposite and select
		17000U	Release
*	DIA:2	Read	
		00xxxx	Read data record with read ahead
		01xxxx	Read ID
		02xxxx	Read absolute
		03xxxx	Read track buffer (16 parcels)
		04xxxx	Read ECC parameter block
		05xxxx	Compute and transfer correction vectors
		06xxxx	Read track header
		10xxxx	Read data record with no read ahead
		12xxxx	Read track buffer (1 sector)
*	DIA:3	Write	
		00xxxx	Write data record with write behind
		01xxxx	Write ID
		02xxxx	Write defective ID
		03xxxx	Write track buffer (16 parcels)
		04xxxx	Write data with zero ECC
		10xxxx	Write data record with no write behind
		14xxxx	Write track buffer (1 sector)
*	DIA:4	Diagnostic Echo/Enter Defect Parameter	
		xxxxxx	Echoes xxxxxx out to the 2EI and back, and enters Defect Parameter into latches on the 2EK
*	DIA:5	Select Cylinder (Seek)	

* Accumulator value accompanies these commands and must be set up before issuing the command.

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DC4004/116 S.J.M.

Bit

$2^0 - 2^3$ **Sector #**

$2^4 - 2^5$ **Drive #**

2^6 **Command Error** - Command Error will set if a new FNX is received with a FNX in progress. Also if a FNX 12 is decoded, since a FNX 12 is not used in the DC40.

2^7 **Channel Diagnostic Mode** - This bit is set when only the port is selected. The port is selected without selecting a drive when a Unit Select FNX is issued with the lower three bits set. This condition is held until a Unit Select is sent to select the drive, a Reset or a Release Opposite and Select will also clear the bit.

2^8 **Unit Ready** - Unit Ready indicates that the drive is up to speed, that the first seek was successful, and that no fault condition exists.

2^9 **On Cylinder** - This signal indicates that the servo head is positioned at a track. This line goes inactive if the positioner drifts off cylinder.

2^{10} **Seek Error** - This signal indicates that the drive took too long to complete a seek, that the positioner has moved outside the recording field, or that the drive was commanded to seek beyond cylinder 1063. The seek error can be cleared by an RTZ command.

2^{11} **Fault** - When this line is active, it indicates that one or more of the following faults exists:

- Read and Write Fault
- Write or Read attempted while Off Cylinder
- First Seek Fault
- Write Fault
- Write and Write Protected Fault
- Head Select Fault
- Voltage Fault

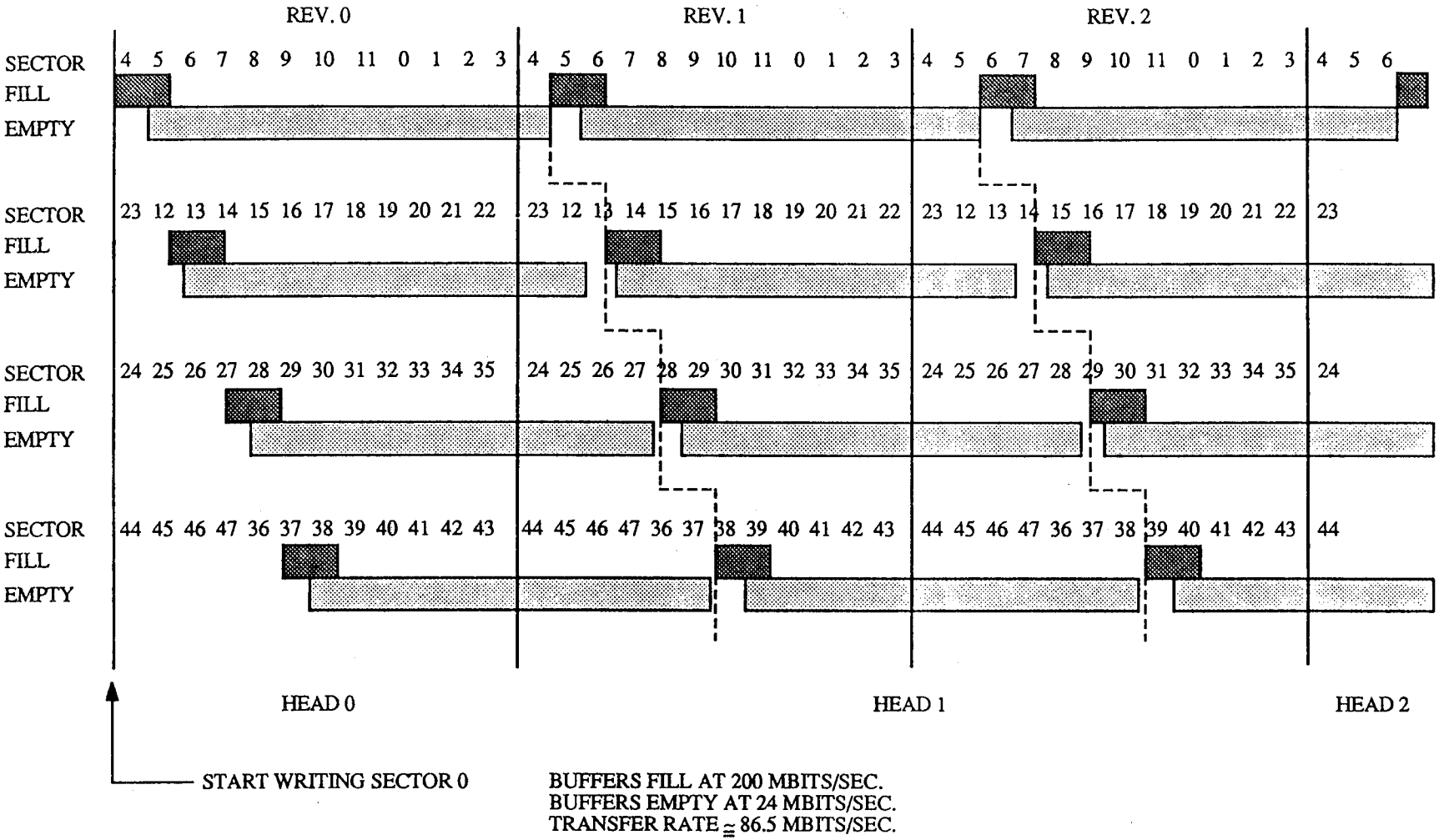
2^{12} **Write Protect** - This signal indicates that the drive write circuits are disabled. The write protect mode is enabled by a jumper plug on the control board, by a switch on the operator panel, by a fault condition, or by a loss of motor speed. Attempting to write while the write protect mode is active results in a fault condition.

2^{13} **Address Mark** - When an address mark has been found during an address mark search operation, this line goes high (refer to Tag 3 description).

2^{14} **Index Mark** - This signal is derived from the servo tracks. It occurs once per revolution of the disk, and its leading edge is the leading edge of sector zero. Note: This signal may be disabled by a switch selection on the I/O board.

2^{15} **Sector Mark** - This signal is derived from the servo tracks. The number of sector signals that occur for each revolution of the disk is selected by switches on the control board. Note: This signal may be disabled by a switch selection on the I/O board.

DC4004W107M



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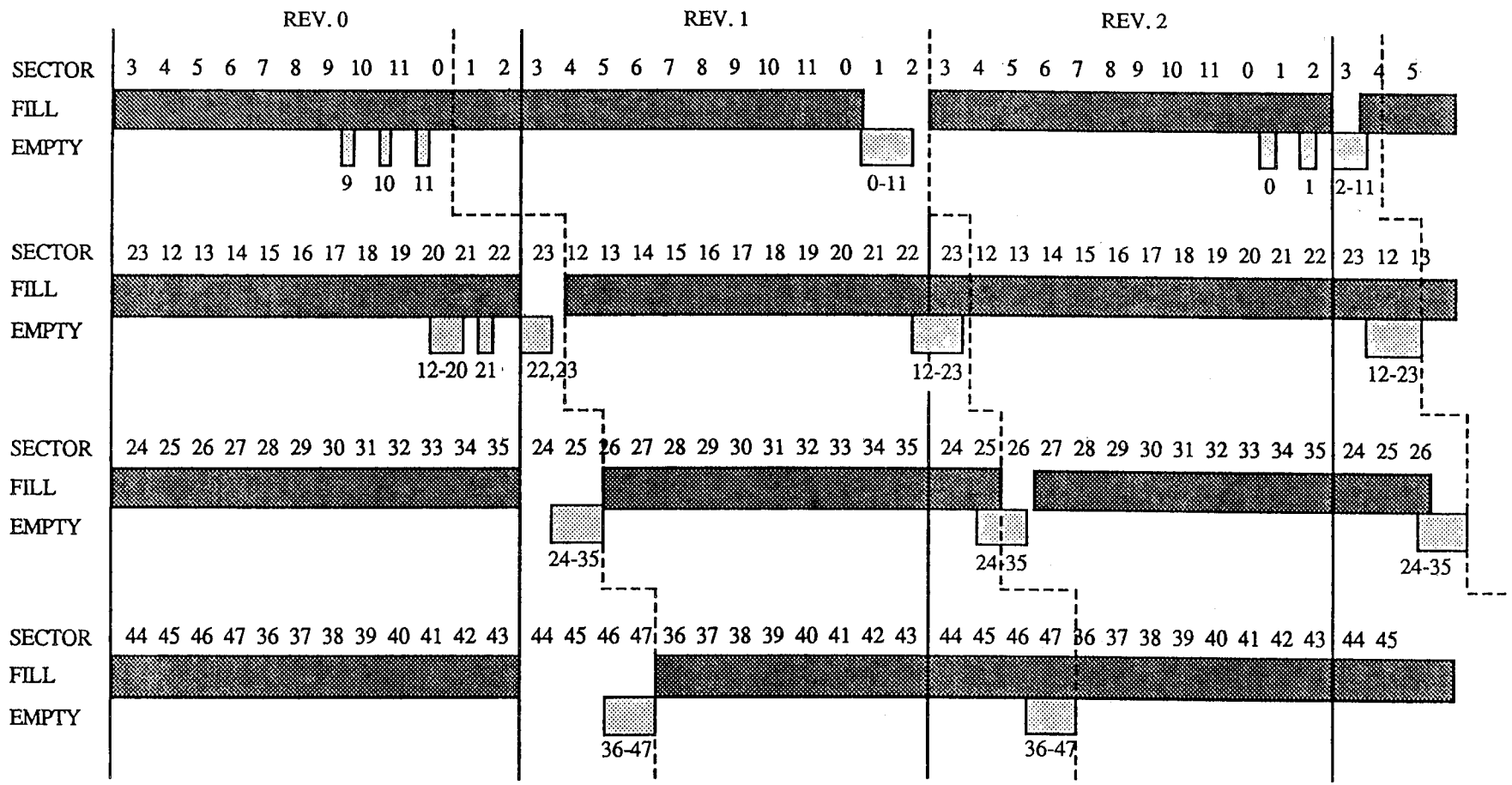
A-5199A S.J.M.

DD40 - WRITE TRANSFER



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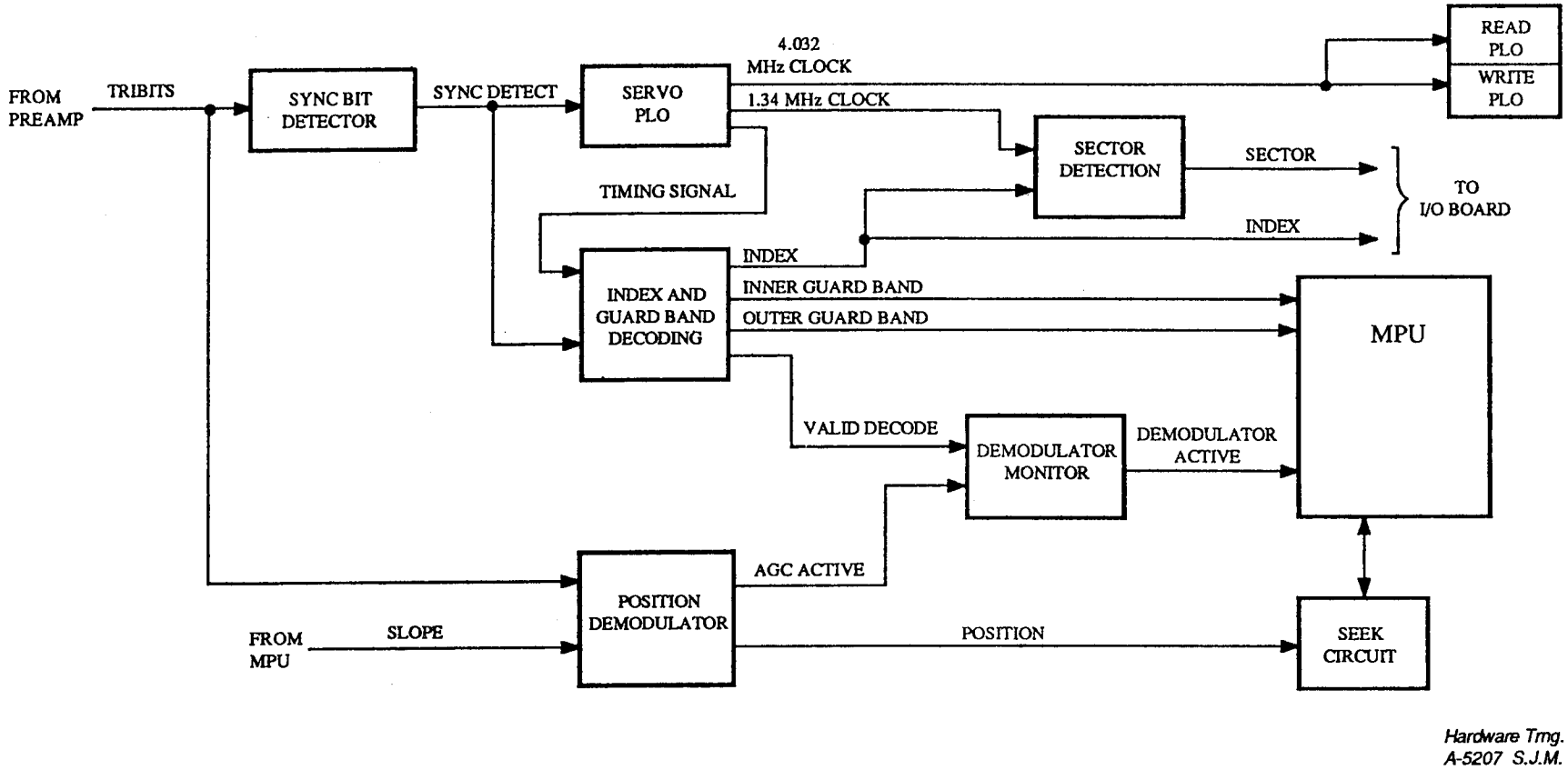
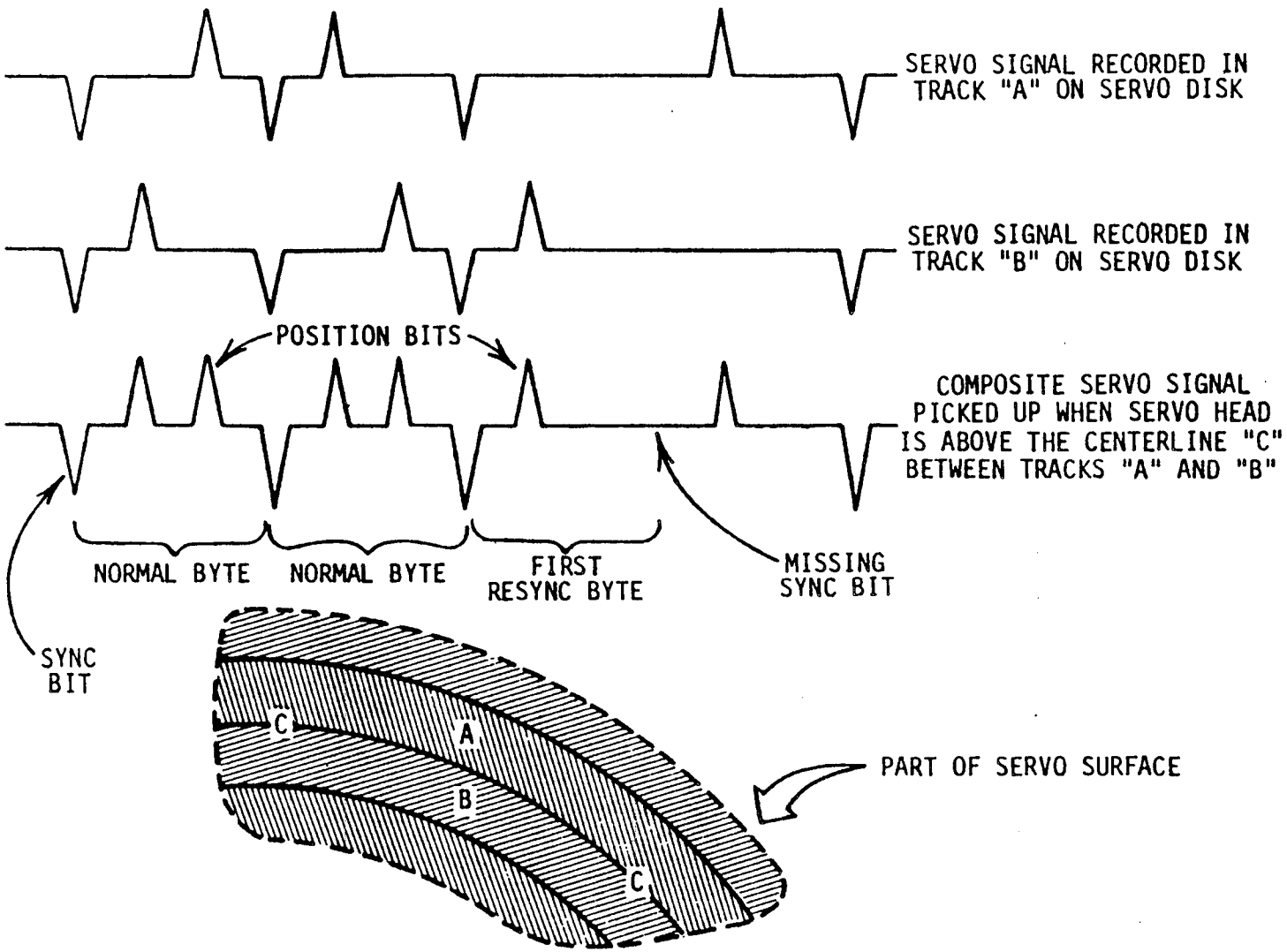
A-5200A S.J.M.

DD40 - READ TRANSFER



DD40 SERVO CIRCUIT



ibit Pattern

CALCULATING DEFECT PARAMETER FROM CORRECTION VECTOR

The offset and mask obtained from the CRAYLOG after an ECC error on a DD-40 can be used to calculate a defect pad. The drive can then be reformatted to hide this defect. This should be done only for errors which are corrected in error recovery and repeat after being rewritten. The following algorithm should be used:

$$\text{DEFPAD} + R = \frac{100040_8 - \text{OFFSET}}{200_8}$$

if $R \geq 170_8$, the defect is unhideable

Example:

OFFSET = 75366
MASK = 003400

$$\frac{100040_8 - 75366_8}{200_8} = \frac{2452_8}{200_8} = 12 + R\ 52$$

The defect pad entered in the diagnostic flaw table would be 12. The flaw should be added using format mode 2.

Hardware Trng.
DC4004/122 S.J.M.

DD-40 EXTRACT ERROR REPORT 1

17:46:06.3159 Disk error packet Error type: Read Final Status: Corrected
Reason recovery invoked: DN and BZ both set
IOP/Chan: 1/27 Device type: DD-40 Unit: 00 Retry count: 3
Expected cylinder: 000567 Expected head group: 000004 Expected sector: 000006
Controller status: 003211 Drive general status: 011406 Function: Read
Buffer status: 011406 Drive status: 001406 Final buffer status: 001406 Final drive status: 001406
Offset: Disabled
Correction mask: 003400 Offset: 051312 Previous correction mask: 003400 Previous offset: 051312

17:46:06.3467 * Corrected data error Read IOP device: 40-1-27A Local dataset: DD-40 JSQ/Job name: 8/40127
Cylinder: 0567 Head: 0004 Sector: 0000

$$\frac{(\#\text{Data bits}_8 + \text{ECC bits}_8) - \text{Offset}_8}{\text{bits in a defect pad}}$$

$$\frac{100040_8 - 51312_8}{200_8} = \frac{26526_8}{200_8} = 132 \quad R126_8 = 86_{10}$$

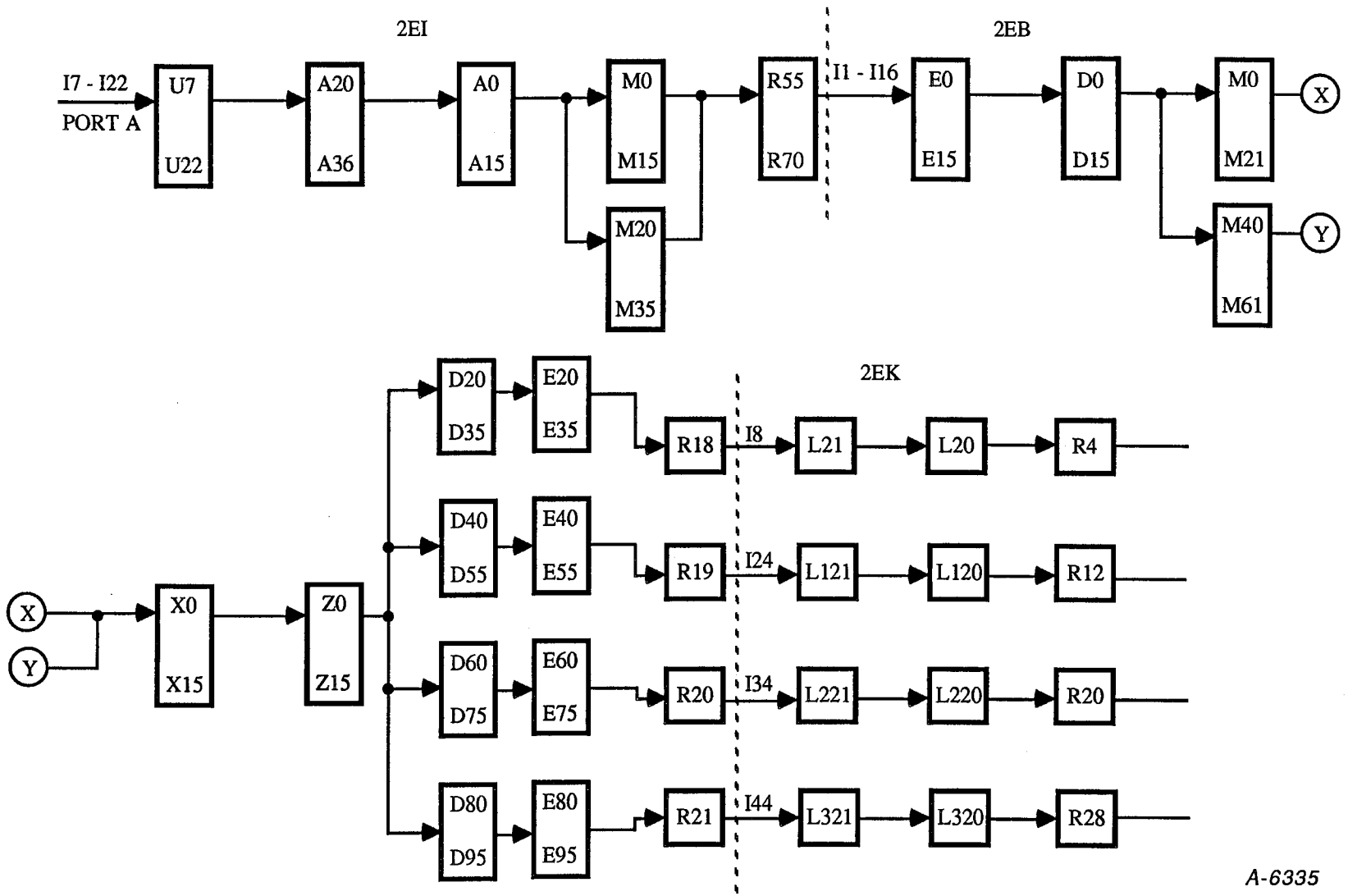
DD-40 EXTRACT ERROR REPORT 2

17:59:21.1634 Disk error packet Error type: Read Final Status: Corrected
Reason recovery invoked: DN and BZ both set
IOP/Chan: 1/25 Device type: DD-40 Unit: 00 Retry count: 3
Expected cylinder: 000004 Expected head group: 000013 Expected sector: 000024
Controller status: 114211 Drive general status: 011430 Function: Read
Buffer status: 011430 Drive status: 001430 Final buffer status: 001430 Final drive status: 001430
Offset: Disabled
Correction mask: 001400 Offset: 074674 Previous correction mask: 001400 Previous offset: 074674

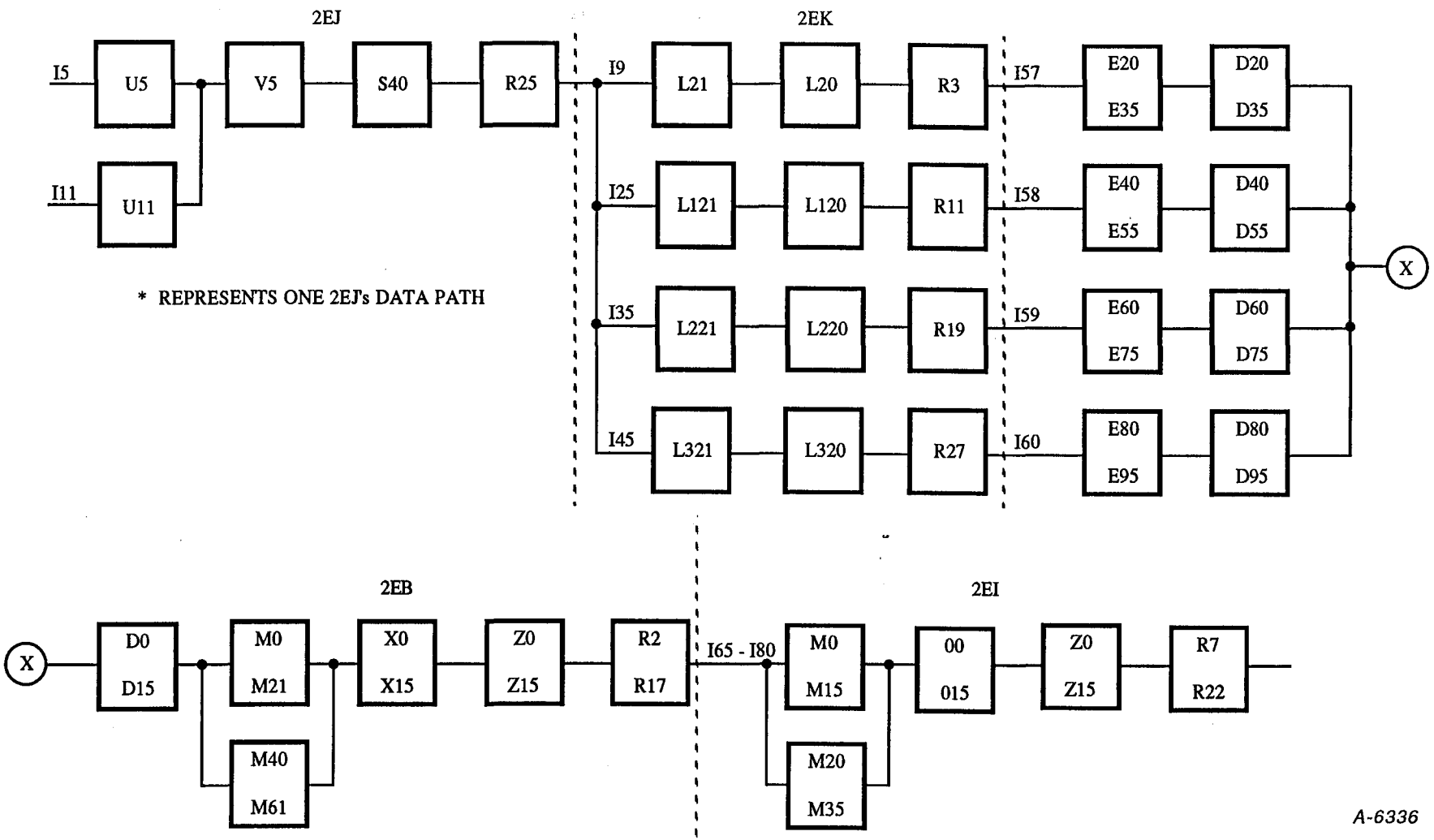
17:59:21.1898 * Corrected data error Read IOP device: 40-1-25A Local dataset: ZZZ25A JSQ/Job name: 6/DD125A
Cylinder: 0004 Head: 0013 Sector: 0000

$$\frac{\text{(\#Data bits + ECC bits) - Offset}}{\text{bits in a defect pad}}$$

$$\frac{100040_8 - 74674}{200} = \frac{3144}{200} = 14 \quad R = 144_8 \text{ or } 100_{10}$$



DATA PATH WRITE MODE 0



DATA PATH READ MODE 0

COMMAND LIST

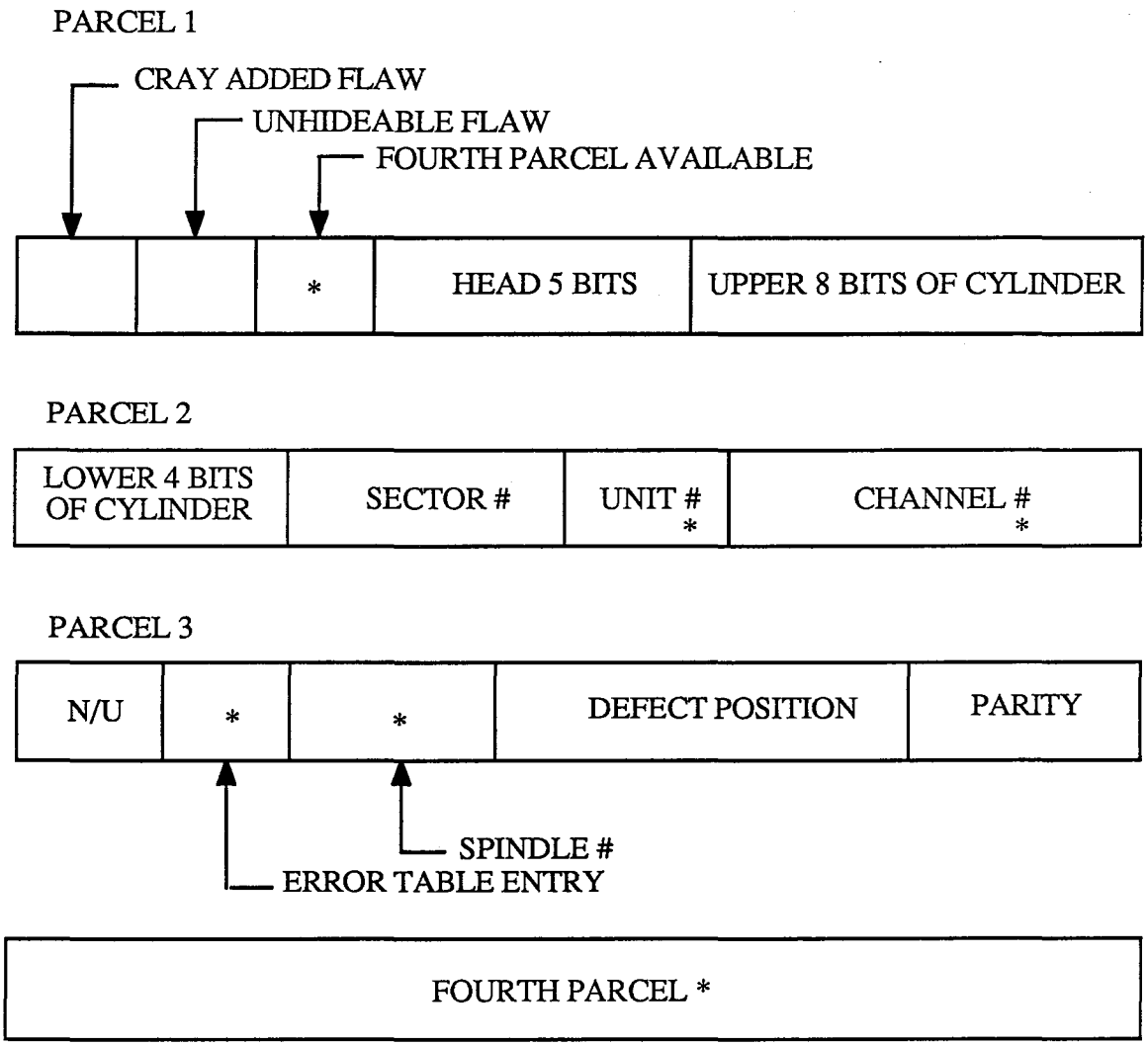
COMMAND	DESCRIPTION	
DS	(Diagnostic start ; Run the selected diagnostics)	
EX	(Exit ; Prepare spindles for power down)	
MC	(Master clear ; Software reset)	
RC	(Reset all selected disk controllers)	
RD	(Reset all selected disk cabinets)	
RG X	(Display the contents of an operand register) X = Register number to display	
D XXXX	(Display memory)	XXXX = Memory Address
DL XXX	(Display memory left)	XXXX = Memory Address
DR XXX	(Display memory right)	XXXX = Memory Address
DF	(Display Forward)	
DE	(Display the error table)	
DC	(Display counts for flaw tables) (First load the tables)	
S XXXX YYYY	(Store a value to memory)	
S+XXXX YYYY	(Store consecutive memory locations) XXXX = Memory Address YYYY = Value to be stored	
ST ZZ Y X	(Save a flaw table on the expander disk)	
RT ZZ Y X	(Restore a flaw table from the expander disk)	
VF ZZ Y X	(Display a active flaw table)	
LF ZZ Y X	(Load an active flaw table from a DC40 disk)	
CF ZZ Y X	(Clear an active flaw table) ZZ = Channel number of DD40 cabinet Y = Unit number X = Spindle number	
CFA	(Clear all active flaw tables)	

AF ZZ Y X WWWW VV UU TTT S R (Add a flaw to the active flaw table)
RF ZZ Y X WWWW VV UU TTT S R (Remove a flaw to the active flaw table)

ZZ = Channel number of the DD40 cabinet
Y = Unit number
X = Spindle number
WWWW = Cylinder
VV = Head number
UU = Sector number
TTT = Defect position
S = CRI added
R = Unhidable defect

DC4003C26M

DD-40 FLAW TABLE FORMAT UNDER XMD



The fourth parcel will be either the logical difference if a data error or Status register 1 if the error was other than a data error.

* This information is only available in Local Memory.

Hardware Trng.
DC4004/113A S.J.M.

PARAMETERS

220 = Section selects (Lower)

1 -	Section 0	2EI data echo through save bus out
2 -	Section 1	Force a parity error
4 -	Section 2	Full track buffer data bus
10 -	Section 3	Full track buffer drive secded
20 -	Section 4	Full track buffer spindle addressing
30 -	Section 5	Full track buffer sector addressing
100 -	Section 6	Track buffer memory
200 -	Section 7	Header Reads - Seek Timing - Head Address
400 -	Section 10	Correction vector analysis
1000 -	Section 11	Disk data bus - scratch cylinder
2000 -	Section 12	Disk spindle addressing - scratch cylinder
4000 -	Section 13	Disk sector addressing - scratch cylinder
10000 -	Section 14	Defect pad writeability
20000 -	Section 15	Chaining - write ahead / read ahead
40000 -	Section 16	Disk system exerciser
100000 -	Section 17	Seek distance / data verification

221 = Section selects (Upper)

1 -	Section 21	Flaw table generation from factory headers
2 -	Section 22	Disk formatting
4 -	Section 23	Write the O.S. flaw table on O.S. cylinder
10 -	Section 24	Surface analysis

222 = Number of passes to run - 177777 means infinite
223 = Type of disk to test
0 = DD40
1 = DD10
226 = Flaw table reference enable
0 = Disable
1 = Enable (default)
230 = Spindle number to test (starting)
231 = Spindle number to test (ending)
232 = Head number to test (starting)
233 = Head number to test (ending)
234 = Cylinder number to test (starting)
235 = Cylinder number to test (ending)

240 = IOP channel number for the display
241 = IOP channel number for the keyboard
242 = Timeout delay used in wait for done (lower)
243 = Timeout delay used in wait for done (upper)
244 = Number of sectors in each track buffer drive (148 normally)
245 = Number of cylinders in one spindle
246 = Number of heads in one spindle

250 = Retry count (used in formatting)
251 = Scratch cylinder address
252 = Flaw table cylinder address
253 = Flaw table head number
254 = O.S. flaw table sector number
255 = O.S. flaw table drive number
256 = O.S. flaw table head number
257 = O.S. flaw table track number
260 = Channel number and unit number for the drive under test. Example:

LOC.	ENTRY	MEANING
260	000025	Chan 25, unit 0
261	100026	Chan 26, unit 1
262	177777	No more
263	177777	
264	177777	
265	177777	
266	177777	
267	177777	

NOTE: These entries must be in ascending order by channel number.

ERROR INFORMATION

12 = Current test section
13 = Current test condition
14 = Error code

1 - Timeout - channel never got done (done = 0 after delay)
2 - Channel error (busy = 1, done = 1)
3 - Channel took longer to finish than expected
4 - Hardware error - check status registers
5 - Unexpected interrupt
6 - Channel not busy too soon
7 - Channel done too soon
10 - Status registers error
11 - Data compare error
12 - Software error - contact Engineering
13 - Exit stack under run
14 - Track header defect position past end of track
15 - Could'nt find any UD's
16 - Unexpected interrupt on DC40 channel
17 - Chaining broken
20 - Hardware error during chaining - check status registers
21 - Did'nt get an expected ECC error
22 - Timeout on waiting for a DC40 interrupt
23 - Did'nt get an expected sync time out
24 - Got an ECC error but data compare did'nt fail
25 - No writeable sectors, found only defective sectors
26 - O.S. flaw table buffer overflow
27 - Out of memory for the active flaw table buffer
30 - Could'nt find the end of the flaw table
31 - Incorrect flaw table on the current spindle

32 - Could'nt find the flaw table in active memory
33 - Out of temporary buffer space
34 - Could'nt find the flaw table entry
35 - Flaw table is too big; it won't fit in buffer memory image
36 - Incomplete flaw table (missing hideables or unhideables)
37 - Empty disk flaw table
40 - The real-time clock is defective
41 - Not enough space on the current spindle trace
42 - Could'nt find a clean track on the selected cylinder
43 - Seek distance exceeded the last entry of the seek time chart

20 = Logical difference
21 = Actual data
22 = Expected data
23 = Error count
24 = Pass count
25 = Location in listing where error occurred (E)
26 = Stop on error flag
0 - continue after error and update error count
1 - stop on error

STATUS INFORMATION

320 = STAT0 (Status register 0)
Bit 0 = Drive ready
Bit 1 = Drive Status available
Bit 2 = Drive Busy/invalid drive command
Bit 3 = Drive error
Bit 4 = Status parity error
Bit 5 = Bus-in parity error
Bit 6 = Read data parity error
Bit 7 = Error flag
Bit 8-15 = Parameter register

321 = STAT1 (General status)
Bit 0-3 = Sector number of last error
Bit 4-5 = Drive number of last error
Bit 6 = Channel error
Bit 7 = Buffer error
Bit 8 = Unit ready (all four spindles)
Bit 9 = On cylinder (all four spindles)
Bit 10 = Seek error (on any of the four spindles)
Bit 11 = Drive fault (on any of the four spindles)
Bit 12 = ECC error (sector status of last error)
Bit 13 = ID not found (sector status of last error)
Bit 14 = Sync time out (sector status of last error)
Bit 15 = Defect parity error (sector status of last error)

322 = STAT2 (Track buffer status)
Bit 0-3 = Sector number
Bit 4-5 = Drive number
Bit 6 = Uncorrectable buffer error
Bit 7 = Buffer error
Bit 8 = Unit ready (on specified drive)
Bit 9 = On cylinder (on specified drive)
Bit 10 = Seek error (on specified drive)
Bit 11 = Drive fault (on specified drive)
Bit 12 = ECC error (on specified sector)
Bit 13 = ID not found (on specified sector)
Bit 14 = Sync time out (on specified sector)
Bit 15 = Defect field parity error (on specified sector)

323 = STAT3 (Drive status)
Bit 0-3 = Sector number
Bit 4-5 = Drive number
Bit 6 = Command error
Bit 7 = Drive in channel diagnostic mode
Bit 8-15 = SMD disk bus in bits specified by tags 4 and 5 and SMD disk bus bits 0-2

DEFINE SPECIAL ERROR LOCATIONS

300	177777	ERRPRC	177777	• Sector address the error occurred in
301	000000	CHERCT	0	• Channel error count
302	000000		0	
303	000000		0	
304	000000	ERROR1	0	• General purpose error location
305	000000	ERROR2	0	• General purpose error location
306	000000	ERROR3	0	• General purpose error location
307	000000	ERROR4	0	• General purpose error location
310	000000	ERRCH	0	• Current channel number after error
311	000000	ERRCI	0	• Current cylinder number after error
312	000000	ERRHN	0	• Current head number after error
313	000000	ERRSP	0	• Current spindle number after error
314	000000	ERRSN	0	• Current sector number after error
315	000000	LSTCI	0	• Last cylinder number
316	000000	ERLNXT	0	• Next previous error location (E - 1)
317	000000	ERLNX2	0	• Next previous error location (E - 2)
320	000000	STAT0	0	• Status register 0
321	000000	STAT1	0	• Status register 1 (general - reg. 1)
322	000000	STAT2	0	• Status register 2 (track buffer - reg. 1)
323	000000	STAT3	0	• Status register 3 (spindle - reg. 1)
324	000000	ADREG0	0	• Local Memory Address register 0
325	000000	ADREG1	0	• Local Memory Address register 1
326	000000		0	
327	000000		0	

USER TEST MODES UNIQUE TO TEST SECTIONS
(See the individual test sections for more detail)

		* ******	SECTION 6	(Track Buffer Memory)
330	125252	BFPT1	125252	• Test data pattern
331	052525	BFPT2	52525	• Test data pattern
		* ******	SECTION 7	(Header reads - seek timing - head address)
332	000044	CDSL7	44	• Condition selector starting / ending
333	000001	FACCRA	1	• Factory track headers or Cray formatted sector IDS • 0 - Factory track headers • 1 - Cray formatted sector IDS (default) • 2 - Seek timing only (no reads)
334	000400	BSCIST	400	• Base cylinder number step
335	002000	RDCT7	2000	• Number of random seeks in condition 4
336	000000	DSPTRA	0	• Display cylinder number
		* ******	SECTION 10	(Connection vector analysis)
337	000044	CDSL10	44	• Condition selector starting / ending
340	000001	WLKINT	1	• Walking one interval (1/16)

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341	000777	UCDTPT	777	• Uncorrectable data pattern (default = 777)
342	002000	RDCVP	2000	• Random correction vector pass count (177777=infinity)
		* ******	SECTION 15	(Chaining - write ahead / read ahead)
343	046000	WTSCTM	46000	• Write sector time in RTC count (220 US)
344	041000	RDSCTM	41000	• Read sector time in RTC count (200 US)
345	000023	RDFSTM	23	• First sector read time (19 MS)
346	000015	WTFLTM	15	• Full 48 sector write time in milliseconds (10560 US)
347	000035	RDFLTM	35	• Full 48 sector read time in milliseconds (9600 US)
350	000550	WTCYTM	550	• Full cylinder write time in milliseconds
351	000570	RDCYTM	570	• Full cylinder read time in milliseconds
		* ******	SECTION 16	(Disk system exerciser)
352	000000	DSEMD	0	• Disk sys. exer. mode (0=I.D. labels , 1=random data)
353	000000	RLOUT	0	• Code rollout - see section 16 for details
		* ******	SECTION 17	(Seek distance / data verification)
354	000013	CDSL17	13	• Condition selector starting / ending
355	000000	ACCSEL	0	• Cylinder access selector scratch / both
356	000040	CYLSKP	40	• Number of cylinders to skip within the selected range
357	000000	DATSEL	0	• Data selector random / user specified
360	125252	OPDAPT	125252	• User specified data pattern
361	000001	PSS17	1	• Number of passes to run this test section
		* ******	SECTION 20	(Flaw table generation)
362	000000	FLAMOD	0	• Flaw table generation mode (factory / Cray)
		* ******	SECTION 21	(Disk formatting)
363	000004	FMTMDE	4	• Format mode (see the formatter section for more detail) • 0 = All IDS are written - replaces flaw table • 2 = Only Cray added IDS are written, merges new flaws • 4 = ID verify only - no writes to the disk
364	000001	VERIFY	1	• Format mode 0 verify Enable; 0 = disable, 1 = Enable
		* ******	SECTION 22	(O.S. flaw table generation)
365	000001	OSFLMD	1	• Mode of operation (seperate / combined)
366	000002	SECNUM	2	• Number of sectors allowed for O.S. table
		* ******	SECTION 23	(Surface analysis)
367	000001	SFAMOD	1	• Surface analysis mode (whole / incremental)
370	000001	PASMOD	1	• Passmode 0 = multiple pass shift counts on all sectors • 1 = multiple pass shift counts on error only
371	000000	HCPRND	0	• Test patterns (test patterns / random numbers)
372	000100	RNDPAS	100	• Number of passes in random number mode
373	000040	PASSHF	40	• Number of shifts to cinsitute one pass
374	000100	SHFCNT	100	• Multiple pass shift count (2 passes - 40 shifts per pass)
375	000002	PATNUM	2	• Number of data pat. par. (to change, double or halve)
376	021225		21225	• Data Pattern

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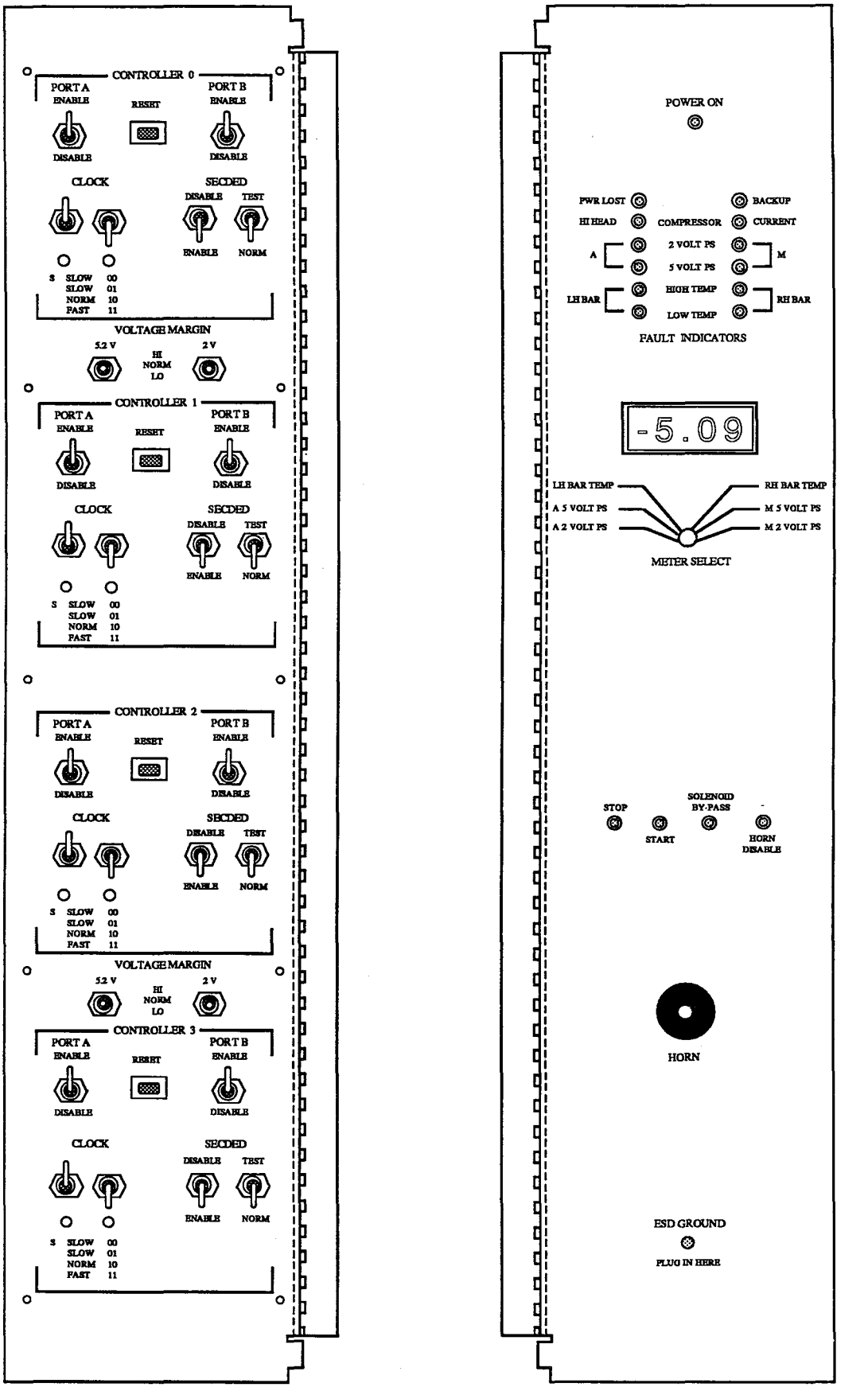
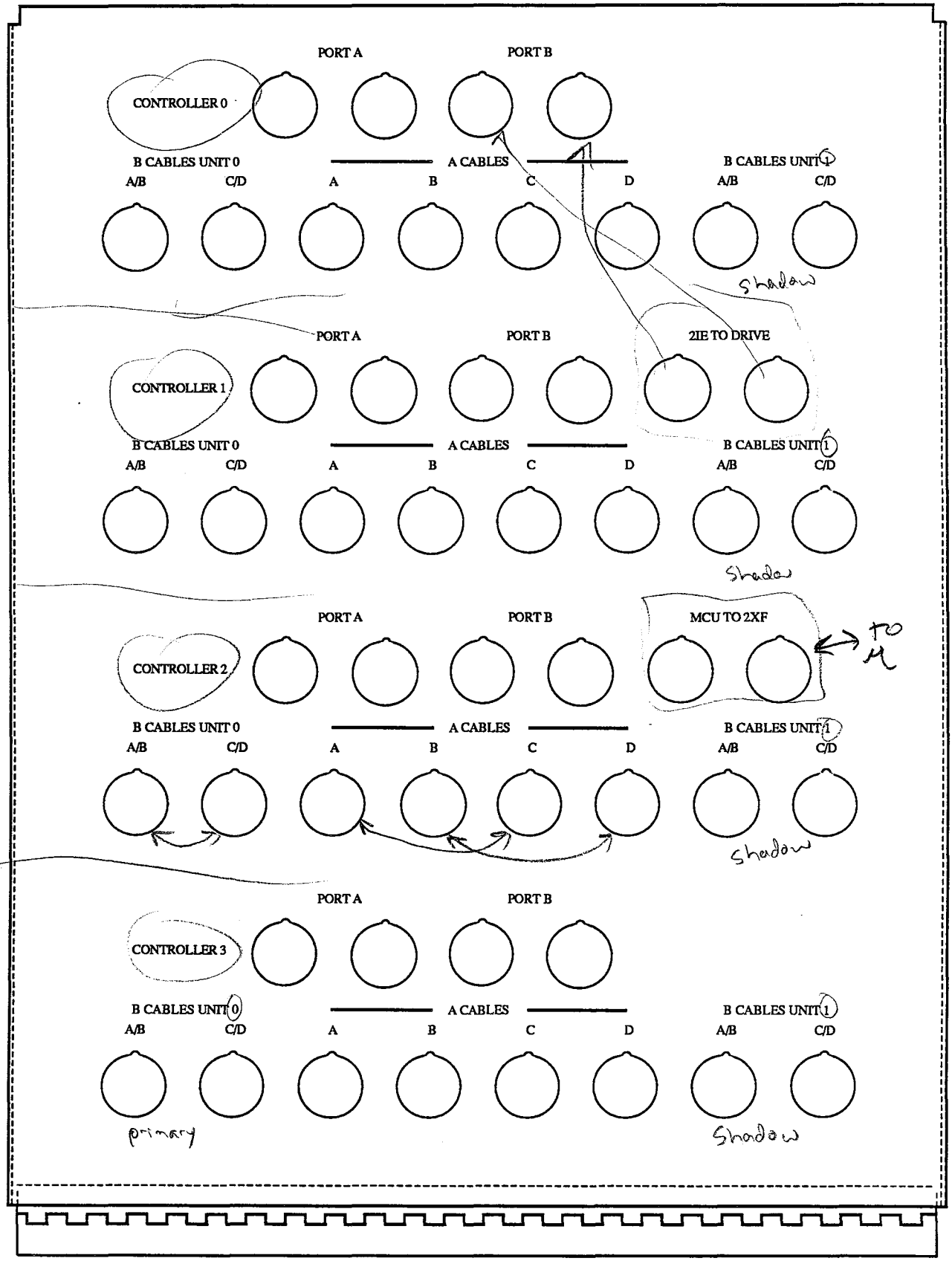
377	014714	14714	• Data pattern
400	000000	0	• Spare data pattern location
401	000000	0	• Spare data pattern location
402	000000	0	• Spare data pattern location
403	000000	0	• Spare data pattern location
404	000000	0	• Spare data pattern location
405	000000	0	• Spare data pattern location



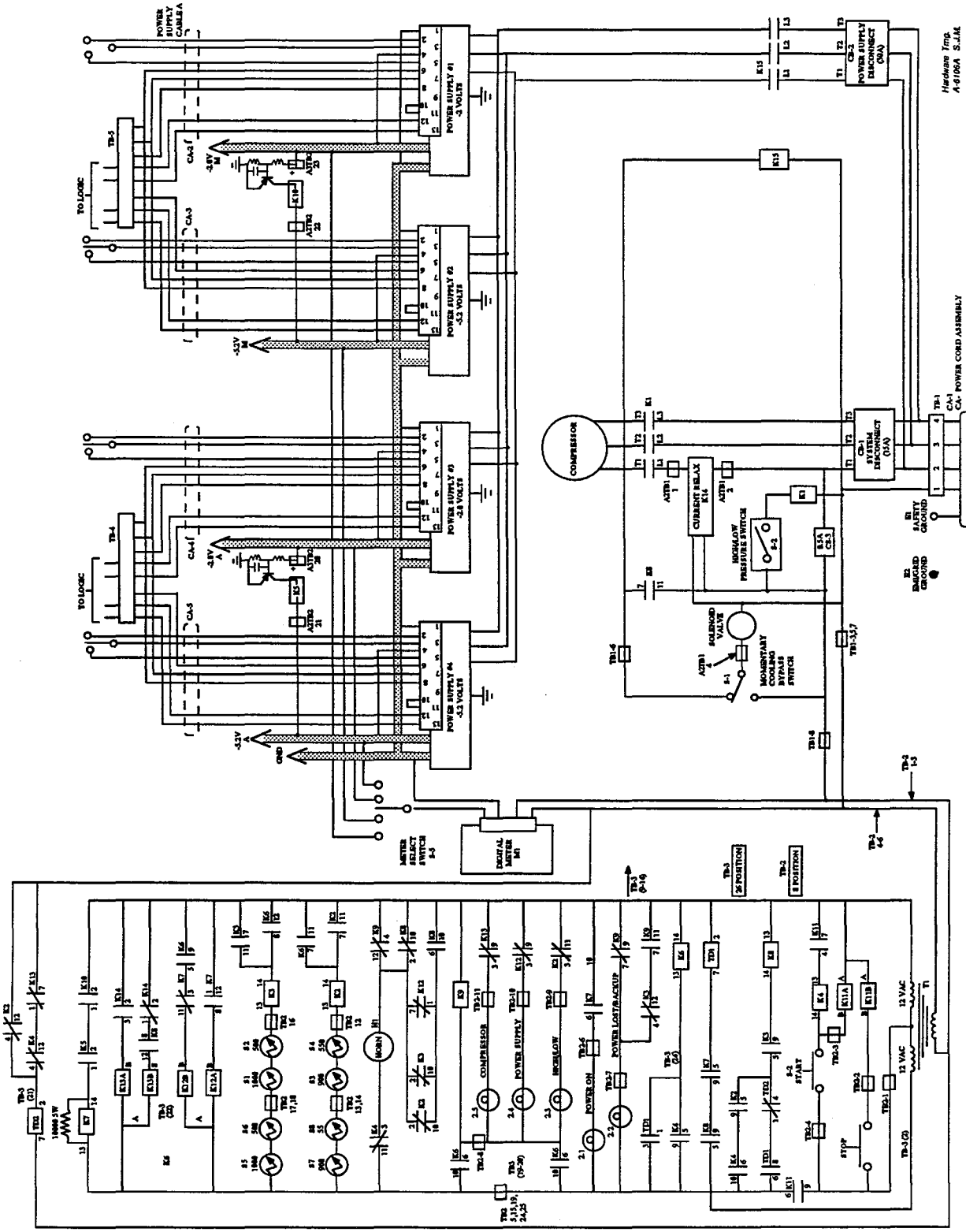
Hardware Trng.
A-8408 S.J.M.

DC-40 MAINTENANCE PANEL



Hardware Tmg.
A-6407 S.J.M.

DC-40 CABLE CONTROL PANEL



DC-40 CONTROL SYSTEM (SERIAL NO. 1 - 9)

DC-40 CONTROL CIRCUIT OPERATION (SERIAL NO. 1 - 9)

Start Sequence

Start switch (S2) latches K11 which then allows 12 volt power to flow to the control circuit. S2 and K11 pull K4.

K4 pulls K6, opens the alarm circuit and opens the condensing unit fault circuit.

K6 pulls K2, K3, and K9 (K2 primary thermostat relay) (K3 back-up thermostat relay) (K9 power lost relay).

K2, K3, and K4 pull K8.

K8 pulls K15 and energizes the refrigeration solenoid and hour meter. Activation of the refrigeration solenoid causes a pressure differential in the refrigeration system which causes the condensing unit to turn on, thus pulling K14.

K14 pulls K13 (condensing unit fault relay).

K15 enables the power supplies which pull K5 and K10.

K5 and K10 pull K7.

K7 activates power on light, latches K12 (power supply fault relay) and K7 and K8 pull TD1.

TD1 holds K6 and K8 and also provides a .5 second ride through for line voltage variations.

After the system starts operation S2 can be released and K4 dropped. K4 then enables the condensing unit fault circuit and the alarm circuit.

Fault Sequence

Power Lost Fault

In the event of a power line sag TD1 provides a .5 second ride through to ensure system stability and prevent nuisance faults.

In the event the power loss lasts longer than .5 seconds TD1 will time out. When power is restored K6, K8, and K9 will be unable to pull, the system will remain shutdown and the power lost lamp will be lit and the alarm will sound.

Condensing Unit Fault

If the current through K14 (condensing unit current sense relay) drops below the holding threshold this will cause K13 (condensing unit fault relay) to drop. K13 will pull TD2 and light the condensing unit fault lamp. After TD2 times out (one minute) K8 drops causing the system to power down and the alarm to sound.

Power Supply Fault

Failure of a power supply will drop K7. K7 then drops TD1, K12 and the power on light. K12 then lights the power supply fault lamp and sounds the alarm. After a .5 second wait K6 and K8 drop causing the system to shut down, but the alarm remains.

Thermostat Fault

A primary thernostat fault drops K2 which will cause TD2 to time out, the temperature fault lamp to illuminate and the alarm to sound. After one minute TD2 drops K8, the system powers down and the alarm remains.

A back-up thermostat fault will drop K3 which lights the back-up temperature light, sounds the alarm, and drops K8 which causes system power down.

Stop Sequence

When stop switch (S1) is pushed K11 unlatches and all 12 volt power is removed from the control circuit.

DC40 REFRIGERATION SYSTEM
WEEKLY CHECKOFF SHEET

Site Name _____
Site S/N _____
DC40 S/N _____

Return completed copy monthly to
Hardware Tech Support, Chippewa Falls.

Properties of Saturated Refrigerant, R-22

Temp.	Press.
10	33
17	40
20	43
23	46
26	50

Temp.	Press.
34	60
41	70
48	81
57	95
65	111

Temp.	Press.
90	168
95	182
100	186
105	211
110	226

	DISCHARGE					SUCTION				MISCELLANEOUS					
Date Checked DD/MM/YY	Pressure	Saturation Temp.	Liquid Line Temp.	Sub-cooling	Hot Gas Temp.	Pressure	Saturation Temp.	Temp.	Super-heat	Water Temp. In	Water Temp. Out	ΔT	Oil Level	LL Glass	Initials
Nominal	170-210	97-110°	See Inst.	5-10°	170-215°	30-60	See Inst.	50-60°	15-20°				1/2	Green	

TEMPERATURE PRESSURE CHART

Vacuum - Inches of Mercury - *Italic Figures*

Pressure - Pounds Per Square Inch Gage Bold Figures

TEMPERATURE °F.	REFRIGERANT 12	22	500	502	717
-60	*19.0*	*12.0*	*17.0*	*7.2*	*18.6*
-55	*17.3*	*9.2*	*15.0*	*3.8*	*16.6*
-50	*15.4*	*6.2*	*12.8*	*0.2*	*14.3*
-45	*13.3*	*2.7*	*10.4*	1.9	*11.7*
-40	*11.0*	0.5	*7.6*	4.1	*8.7*
-35	*8.4*	2.6	*4.6*	6.5	*5.4*
-30	*5.5*	4.9	*1.2*	9.2	*1.6*
-25	*2.3*	7.4	1.2	12.1	1.3
-20	0.6	10.1	3.2	15.3	3.6
-18	1.3	11.3	4.1	16.7	4.6
-16	2.0	12.5	5.0	18.1	5.6
-14	2.8	13.8	5.9	19.5	6.7
-12	3.6	15.1	6.8	21.0	7.9
-10	4.5	16.5	7.8	22.6	9.0
- 8	5.4	17.9	8.8	24.2	10.3
- 6	6.3	19.3	9.9	25.8	11.6
- 4	7.2	20.8	11.0	27.5	12.9
- 2	8.2	22.4	12.1	29.3	14.3
0	9.2	24.0	13.3	31.1	15.7
1	9.7	24.8	13.9	32.0	16.5
2	10.2	25.6	14.5	32.9	17.2
3	10.7	26.4	15.1	33.9	18.0
4	11.2	27.3	15.7	34.9	18.8
5	11.8	28.2	16.4	35.8	19.6
6	12.3	29.1	17.0	36.8	20.4
7	12.9	30.0	17.7	37.9	21.2
8	13.5	30.9	18.4	38.9	22.1
9	14.0	31.8	19.0	39.9	22.9
10	14.6	32.8	19.7	41.0	23.8
11	15.2	33.7	20.4	42.1	24.7
12	15.8	34.7	21.2	43.2	25.6
13	16.4	35.7	21.9	44.3	26.5
14	17.1	36.7	22.6	45.4	27.5
15	17.7	37.7	23.4	46.5	28.4
16	18.4	38.7	24.1	47.7	29.4
17	19.0	39.8	24.9	48.8	30.4
18	19.7	40.8	25.7	50.0	31.4
19	20.4	41.9	26.5	51.2	32.5
20	21.0	43.0	27.3	52.4	33.5
21	21.7	44.1	28.1	53.7	34.6
22	22.4	45.3	28.9	54.9	35.7
23	23.2	46.4	29.8	56.2	36.8
24	23.9	47.6	30.6	57.5	37.9
25	24.6	48.8	31.5	58.8	39.0
26	25.4	49.9	32.4	60.1	40.2
27	26.1	51.2	33.2	61.5	41.4
28	26.9	52.4	34.2	62.8	42.6
29	27.7	53.6	35.1	64.2	43.8
30	28.4	54.9	36.0	65.6	45.0
31	29.2	56.2	36.9	67.0	46.3
32	30.1	57.5	37.9	68.4	47.6
33	30.9	58.8	38.9	69.9	48.9
34	31.7	60.1	39.9	71.3	50.2
35	32.6	61.5	40.9	72.8	51.6
36	33.4	62.8	41.9	74.3	52.9
37	34.3	64.2	42.9	75.8	54.3
38	35.2	65.6	43.9	77.4	55.7
39	36.1	67.1	45.0	79.0	57.2
40	37.0	68.5	46.1	80.5	58.6
41	37.9	70.0	47.1	82.1	60.1
42	38.8	71.4	48.2	83.8	61.6
43	39.8	73.0	49.4	85.4	63.1
44	40.7	74.5	50.5	87.0	64.7
45	41.7	76.0	51.6	88.7	66.3
46	42.6	77.6	52.8	90.4	67.9
47	43.6	79.2	54.0	92.1	69.5
48	44.6	80.8	55.1	93.9	71.1
49	45.7	82.4	56.3	95.6	72.8
50	46.7	84.0	57.6	97.4	74.5
55	52.0	92.6	63.9	106.6	83.4
60	57.7	101.6	70.6	116.4	92.9
65	63.8	111.2	77.8	126.7	103.1
70	70.2	121.4	85.4	137.6	114.1
75	77.0	132.2	93.5	149.1	125.8
80	84.2	143.6	102.0	161.2	138.3
85	91.8	155.7	111.0	174.0	151.7
90	99.8	168.4	120.6	187.4	165.9
95	108.2	181.8	130.6	201.4	181.1
100	117.2	195.9	141.2	216.2	197.2
105	126.6	210.8	152.4	231.7	214.2
110	136.4	226.4	164.1	247.9	232.3
115	146.8	242.7	176.5	264.9	251.5
120	157.6	259.9	189.4	282.7	271.7
125	169.1	277.9	203.0	301.4	293.1
130	181.0	296.8	217.2	320.8	——
135	193.5	316.6	232.1	341.2	——
140	206.6	337.2	247.7	362.6	——
145	220.3	358.9	264.0	385.0	——
150	234.6	381.5	281.1	408.4	——
155	249.5	405.1	298.9	432.9	——

DC/DD-40 LAB SKILLS LIST

NAME: _____ DATE: _____

HOW A	HOW B	HOW C	*COMPONENT REPLACEMENT*	LEVEL
			MODULE (HDA)	
			POWER SUPPLY	
			I/O CARD (VJX)	
			R/W CARD (WNX)	
			DRIVE	
			DRIVE BELT	
			BRAKE	
			CONTROL CARD VDX	
			POWER AMP UCX	
			OPERATOR PANEL PBX	
			FAULT DISPLAY UQX	
			FILTER REPLACEMENT	
			FAN	
			MOTOR	
			HDA INTERFACE	
			RELAY BOARD	
			MOTHER BOARD	
			REGULATOR BOARD	

DC-40 DIAGNOSTIC

Circle test sections used during lab. 0 1 2 3 4 5 6 7 10 11 12 13 14 15 16 17 21 22 23 24

			FORMATTER	
			SURFACE ANALYSIS	
			WRITE O.S. FLAW TABLE	

OTHER

			ADD/REMOVE FREON FROM THE REFRIG. SYSTEM	
			READY FOR SHIPPING/INSTALLATION	
			VOLTAGE MEASUREMENT	
			RUN DIAGNOSTICS FROM CE PANEL	
			MAINTENANCE PANEL	
			REFRIGERATION ADJUSTMENTS	
			CONNECT OFFLINE TESTER	
			REPLACE A MODULE POWER SUPPLY	
			PERFORM ADJUSTMENTS ON POWER SUPPLY	
			SCOPE SECTOR	
			XMD VOLTAGE MEASUREMENT	
			VOLTAGE ADJUSTMENT	
			CHECK OUT DRIVE FROM OFFLINE TESTER	
			WRITE A PROGRAM USING MICRO DOTS	

COMMENTS: _____

_____

KEY:

	A	B	C
HOW	Shown or Video	Lecture or Theory	Performed

LEVEL Excellent - 5 Above Average - 4 Average - 3 Below Average - 2 Unsatisfactory - 1 Not Apply - N/A

Student's Signature _____

Instructor's Signature _____

If you sign this sheet, you are responsible on site for this task.

MF02W09A

HOW TO INSTALL AND USE THE MIX EDITOR

The following information can be used to set up your version of the MIX editor for your terminal type along with a few steps to get you started using the MIX editor.

The first thing that must be done is to have the file "SETUP.EDT" built for your terminal characteristics. If you happen to have either a Dialog-80, Dialog-150 and/or an Ampex 230 (emulating a D-150) the steps below should work. First, place the MIX diskette into one of the floppy drives and select that drive.

1. Type SETEDIT <cr> - A menu will be displayed

2. Type T <cr> - A new menu will be displayed on which will be several terminal types

3. Type 7 <cr> - This will select terminal type D-80 which is the closest to correct as any others. It will return to the main menu

4. Type R <cr> and at the message asking for the filename type MACRO.TXT <cr> - This will add the macro file to the terminal characteristics already there

5. Type O <cr> - The letter, not the number. At the filename request type TEMP.TXT - This will write the text file you have just built out to diskette.

6. Type E <cr> to exit SETEDIT. A message will ask if you want to create an edit file, type N <cr>

Now comes the tricky part. Go back to drive A: and

7. PIP TEMP.TXT to the A drive of the hard disk

8. With the use of some other text editor (ED or whatever), the eigth line must be modified. As it stands now, it reads "CURSOR COLROW". It must be changed to read "CURSOR ROWCOL"

9. Now that the text file has been corrected and resaved, it must be converted to binary and renamed. To do this:

10. PIP TEMP.TXT back to the MIX diskette and select the floppy drive

11. Type SETEDIT (cr) - This will get the main menu

12. Type R <cr> and at the filename request type TEMP.TXT - It will read in the corrected text file

13. Type W <cr> and at the filename request type SETUP.EDT - This will save it as a binary file useable by the editor

14. Type E <cr> - To exit

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Now that you have a correct version of the terminal information on the diskette, you can begin to edit. There are three files on the diskette that need to be present on the hard disk as you edit. They are EDIT.COM, EDIT.OVY, and SETUP.EDT. You can start to edit by simply typing:

EDIT (filename)

If you are creating a new file there is no need for the filename.

A message will appear saying "Reading setup file...". When it is finished an EOB* will appear, this is the end of block marker. You are now in the insert mode and ready to start typing. The keyboard is set up to be WordStar compatable; but as you learn more about this you will find it can be modified to be any way you want it.

If you are not familiar with this type of editor, on the following pages is a partial list of the command with a very brief description (kind of a ready reference) to help you get started. It is in no way complete.

To save your file and exit the editor hit the escape key and then an E. The prompt will appear requesting a filename. If the file already has a name simply hit return or else give the file a name. Then a prompt requesting a backup will appear. If you want a backup hit return. If you don't, type N and return. If you want to quit the editor without saving the file type ESCAPE followed by a Q. It will ask for a confirmation.

Again, if you have any questions or problems, contact the Diagnostics Department at (715) 723-2206. (Technical Operations Building, Chippewa Falls, WI)

A^ is the control key, it should be held down while typing the other specified key(s).

A^[is the escape key. By depressing the escape key you enter the command mode. The cursor will drop to the bottom left corner and display a < >. Command mode's full usage is explained in the book beginning on page 31.

COMMAND	DESCRIPTION
^S	Moves the cursor left one position
^A	Moves the cursor left one word
^QS	Moves the cursor to the beginning of the line
^D	Moves the cursor right one position
^F	Moves the cursor right one word
^QD	Moves the cursor to the end of the line
^E	Moves the cursor up one position
^QE	Moves the cursor to the top of the page
^R	Moves the cursor up one page
^X	Moves the cursor down one position
^QX	Moves the cursor to the bottom of the page
^C	Moves the cursor down one page
^W	Scrolls the screen up one line (does not move the cursor)
^Z	Scrolls the screen down one line (does not move the cursor)
^G	Deletes a character under the cursor
DEL key	Deletes the character to the left of the cursor
^T	Deletes word
^QY	Deletes from the cursor to the end of line
^Y	Deletes line
^U	Undoes the line deleted by ^Y (can be used to move a line)
^QT	Undoes the word deleted by ^T
^QL	Undo whatever changes were made to this line
^QJ	Joins the following line with this line
^V	Toggles insert mode on and off
^QI	Toggles auto indent on and off
^N	Insert one new line
^QN #	Inserts # number of lines
^KB	Marks the beginning of the block
^KK	Marks the end of the block
^KV or KM	Moves the block
^KC	Copies the block
^KY	Deletes the block
^KW	Writes the block to file
^KR	Reads the block from file
^KL	Makes all characters in the block lower case
^KU	Makes all characters in the block upper case
^KP	Prints block

^KO	Outputs the block to temporary file
^KI	Inputs the block from temporary file
^[SS	Split screen - it will ask for row to split horizontally, if no # is specified, it will ask for column
^O	Other screen - toggles between the split screens
^I or TAB key	Tabs right four spaces
^B	Tabs left four spaces
^[DT	Deletes tabs
^[TS	Sets tab at cursor position
^[TC	Clears tab at cursor position
^[TB #	Sets tabs at # intervals
^[TABS = #, #, #	Sets tabs at colums #, #, and #
^[LN	Toggles line numbers (do not become part of file)
^[AL	Auto line numbers that stay in file (useful for BASIC)
^KX	Saves the present file and exits the editor
^KS	Saves the present file but continues editing it
^KD	Saves the present file and creates a new file in the editor
^KQ	Quits with no save and stays in the editor
^KF	Lists the directory specified as directory path
^KJ	Deletes the file specified by filename
^KE	Writes lines to file filename
^QF	Find string - a prompt will ask for the string to find
^L	Finds the next occurance of the previously defined string
^QA	Find and replace - a prompt will ask for the string to find, then the string to replace it. When it finds a match, it will ask Replace? y/n/q. A y will replace, a n will not replace, and the search will continue until a q is typed.
^QV	Will return the cursor to the position it had prior to any of these instructions

CONTROL RELAY FUNCTIONS (SERIAL NO. 1 - 9)

K1 - Condensing unit contactor, controlled by high/low pressure switch.

K2 - Pulled by K6, self-latching, controlled by primary "T" stats, 4 sets of contacts.
A = Self-latch and temperature light B = Alarm circuit C = K8 pull D = TD2 pull

K3 - Pulled by K6, self-latching controlled by secondary "T" stats, 4 sets of contacts.
A = Self-latch B = Alarm circuit C = K8 pull and latch circuit
D = Power lost light circuit

K4 - Momentary, controlled by start switch and K11, 4 sets of contacts.
A = TD2 pull circuit B = K6 pull C = K8 pull D = Alarm power

K5 - Pulled by "A" power supplies, 1 set of contacts in K7 pull.

K6 - Pulled by K4, latched by TD1, 4 sets of contacts.
A = K9 pull B = K13B pull C = K3 pull D = K2 pull

K7 - Pulled by K5 and K10, 4 sets of contacts.
A = TD1 pull B = K12A pull C = K12B pull D = Power on light

K8 - Pulled by K4, K2, and K3, latched by TD1, TD2, and K3, 4 sets of contacts
A = Pull K15, energize solenoid and H.M. B = Pull TD1 C = Pull K12B
D = Alarm circuit

K9 - Pulled by K6, self-latching, 4 sets of contacts.
A = Self-latch B = Alarm circuit C = Power lost light D = Power lost light

K10 - Pulled by "M" power supplies, 1 set of contacts in K7 pull.

K11 - Latched by start switch, unlatched by stop switch, 2 sets of contacts.
A = K4 pull B = Passes power for all other circuit components

K12 - Latched by K7, unlatched by K7 and K6, 2 sets of contacts.
A = Alarm circuit B = Power supply light

K13 - Latched by K14, unlatched by K8 and K14, 2 sets of contacts.
A = Pull TD2 B = Condensing unit light

K14 - Latched and unlatched by flow of current to condensing unit. 1 set of contacts.
A = Latch K13 B = Unlatch K13

K15 - Pulled by K8, 3 sets of contacts used to supply power to power supplies.

TDR1 - Pulled by K8 and K7, 2 sets of contacts, delay on drop.
A = Holds K6 B = Part of hold for K8

TDR2 - Pulled by K2 or K13 and K4, 2 sets of contacts, delay on pull.
A = Part of K8 hold B = Not used

2. DD-40 DRIVES

The DD-40 disk storage unit (sometimes called a drive) contains 4 XMD spindles (sometimes called spindles). This section provides the following information on the XMD spindles:

- A description of the XMD spindles
- The XMD switches and indicators
- XMD power-on and power-off procedures
- Drive address selection
- Drive head selection

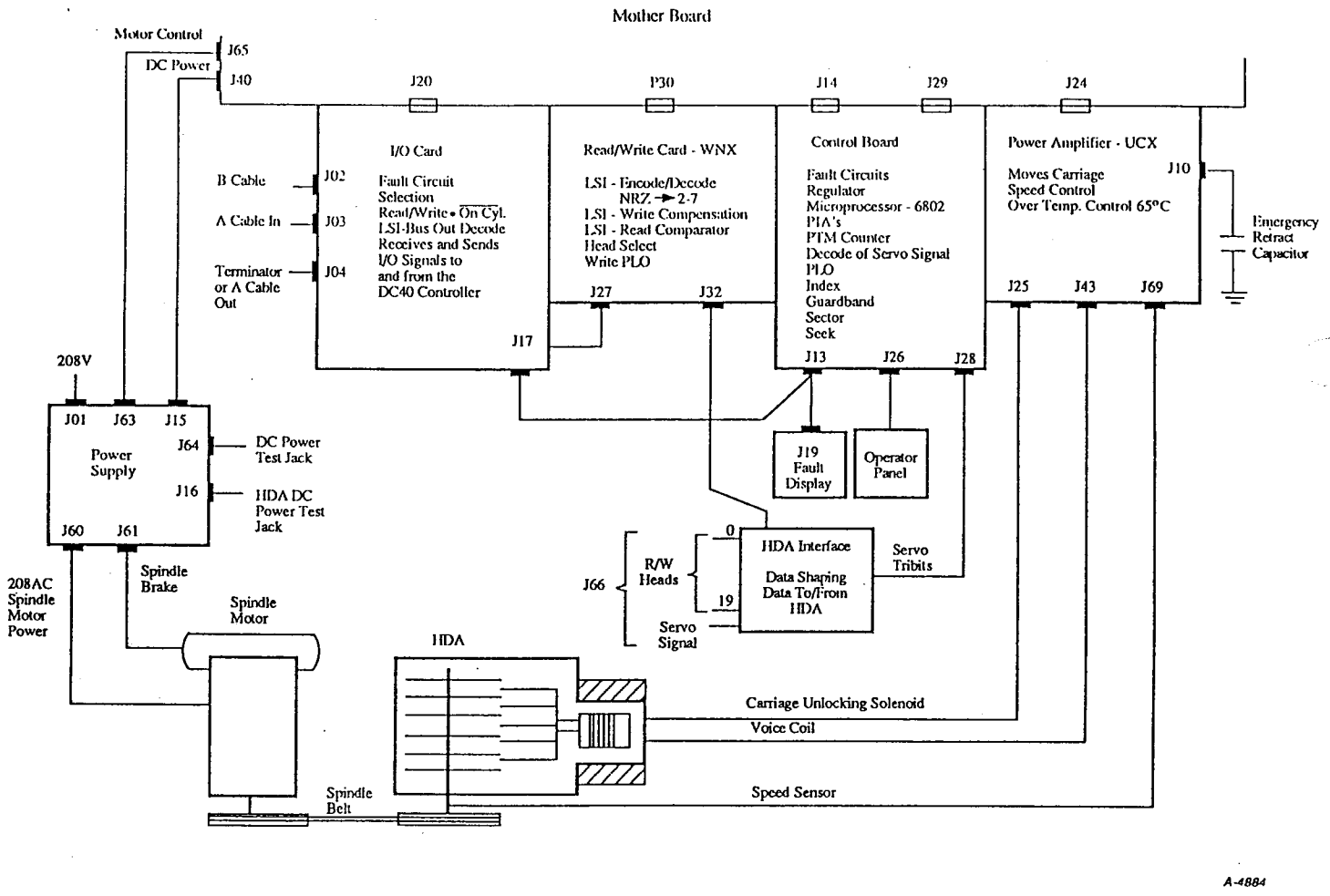
2.1 DESCRIPTION

Each XMD spindle controls reading and writing of data to 6 disks. Data is read and written across 19 heads which ride on the surface of the disks. The DD-40 drive has an internal power supply, which receives its input power from the site's main power source.

Figure 2-1 is a block diagram of an XMD spindle.

The DD-40 drives operates under direction of the DC-40 disk controller. The DC-40 communicates with the DD-40 drive by way of an interface consisting of a number of I/O lines. Some of the interface lines (e.g., those that carry commands to the drive) are not enabled if the drive is not selected by the DC-40. Unit selection enables the DC-40, which can be connected to more than one drive, to initiate and direct an operation on a specific drive.

All operations performed by the drive are related to reading and writing data. Writing and reading data is performed by heads, which are positioned over the recording surfaces of the rotating disks. There are 2 heads for each disk surface. The heads are positioned in such a way that data is written in concentric tracks around the disk surfaces. Before any read or write operation can be performed, the DC-40 must instruct the drive to position the heads over the desired tracks (called seeking) and use the head located over the surface where the operation



2-1. XMD Block Diagram

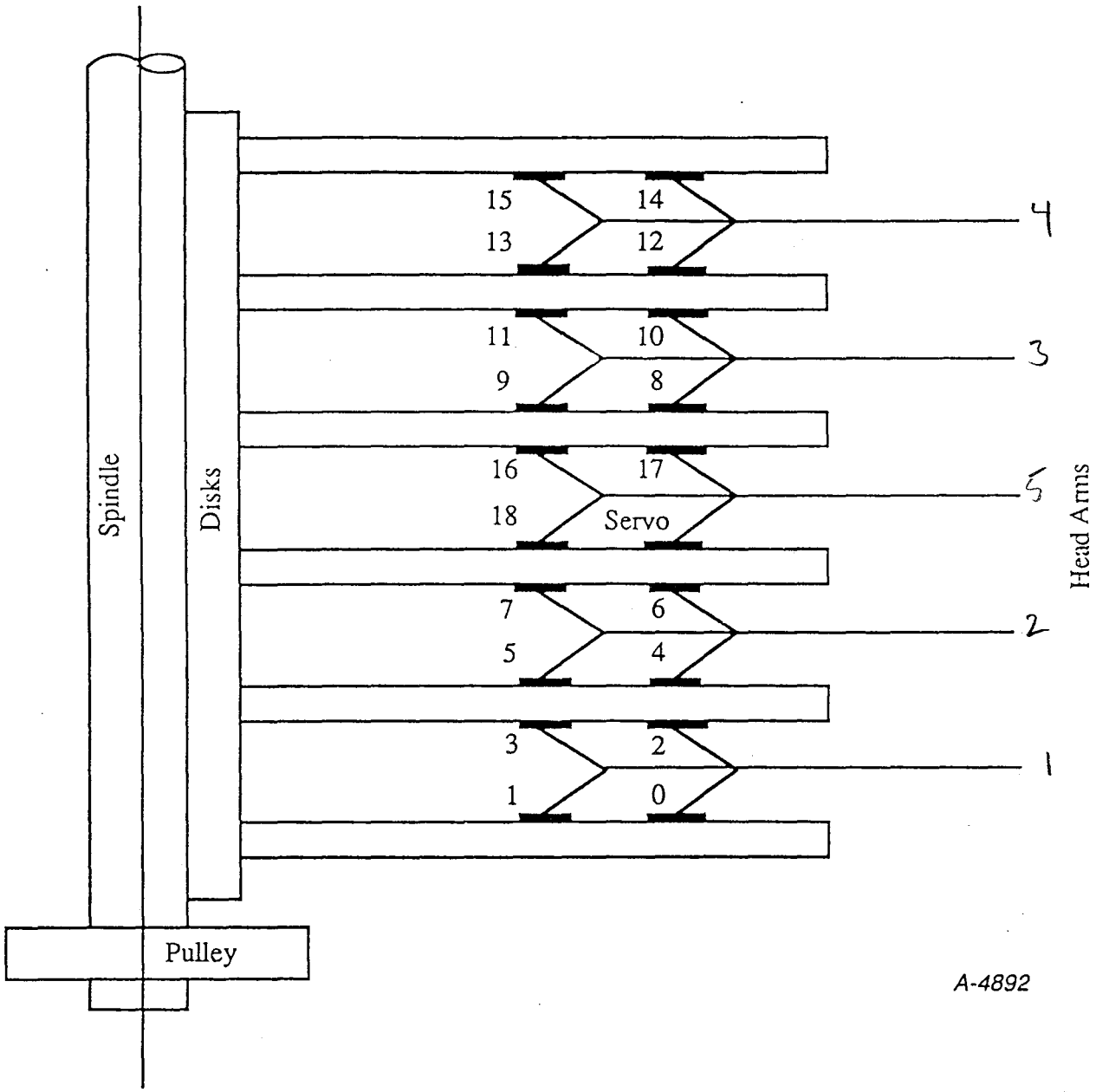


Figure 2-2. XMD Drive Head/Disk Relationship

will be performed (called head selection). An XMD spindle has 19 data heads and one servo head. Figure 2-2 shows the relationship of the heads to the disks for an XMD spindle.

After selecting a head and arriving at the correct data track, the portion of the track where the data will be written or read must be located. This is called track orientation and is done by using the Index and Sector signals generated by the spindle. The Index signal indicates the logical beginning of each track. The Sector signal indicates the position of the head on the track with respect to the index.

When the desired location is reached, the DC-40 commands the spindle to read or write data. During a read operation, the spindle recovers data from the disks and transmits it to the controller. During a write operation, the spindle receives data from the controller, processes it, and writes it on the disks.

The spindle is capable of recognizing fault conditions that may occur during its operation. When a fault condition is detected, it is indicated by a fault signal to the DC-40 and by a maintenance indicator on the XMD spindle itself.

Table 2-1 lists the specifications of the XMD spindles.

Table 2-1. XMD Spindle Specifications.

Characteristic	Specification
Size	
Height	26.4 cm (10.3 in)
Width	48.0 cm (18.9 in)
Length	76.5 cm (30.1 in)
Weight	80.1 kg (176 lbs)
Interface	
SMD-O/SMD-E	
Recording	
Total Capacity (unformatted)	
PA1A4/1A5 xmd2	858 Mbytes
PA1A6/1A7 xmd3	1359 Mbytes
Bytes per track	50,400 bytes

Table 2-1. XMD Spindle Specifications (continued)

Characteristic	Specification
Number of disks:	
850 Mbytes	5
1350 Mbytes	6
Movable data heads:	
850 Mbytes	16
1350 Mbytes	19
Servo heads	1
Tracks per inch:	
850 Mbytes	960
1350 Mbytes	1280
Physical heads per surface	2
Logical cylinders per head/disk assembly:	
850 Mbytes	1064 (0 through 1063)
1350 Mbytes	1420 (0 through 1419)
Transfer rate	
Disk speed at 3600 rpm	24.2 MHz (3,025,000 bytes/s)
Latency	
Average	8.33 ms (disk rotation speed at 3600 rpm)
Maximum	17.3 ms (disk rotation speed at 3474 rpm)
Recording	
Mode	2 through 7 code
Density	15,400 bpi (inner track)
Seek Time	
Full	30 ms

Table 2-1. XMD Spindle Specifications (continued)

Characteristic	Specification
Average	16 ms
Single track	5 ms maximum
Start Time	3 minutes 30 seconds maximum (not including power sequence delay determined by unit address in string)
Stop time	
Start switch OFF	30 seconds maximum
Power loss	30 seconds maximum

2.2 XMD SPINDLE SWITCHES AND INDICATORS

Table 2-2 lists the XMD spindle switches and indicators. Figure 2-3 shows where the switches and indicators are located on an XMD spindle.

Table 2-2. XMD Spindle Switches and Indicators Functions

Switch/Indicator	Function
	POWER SUPPLY REAR PANEL
CB1 (ON/OFF) circuit breaker	Applies site AC power to the fan and the internal power supply, which supplies the DC operating voltages to the spindle electronics.

Table 2-2. XMD Spindle Switches and Indicators Functions (continued)

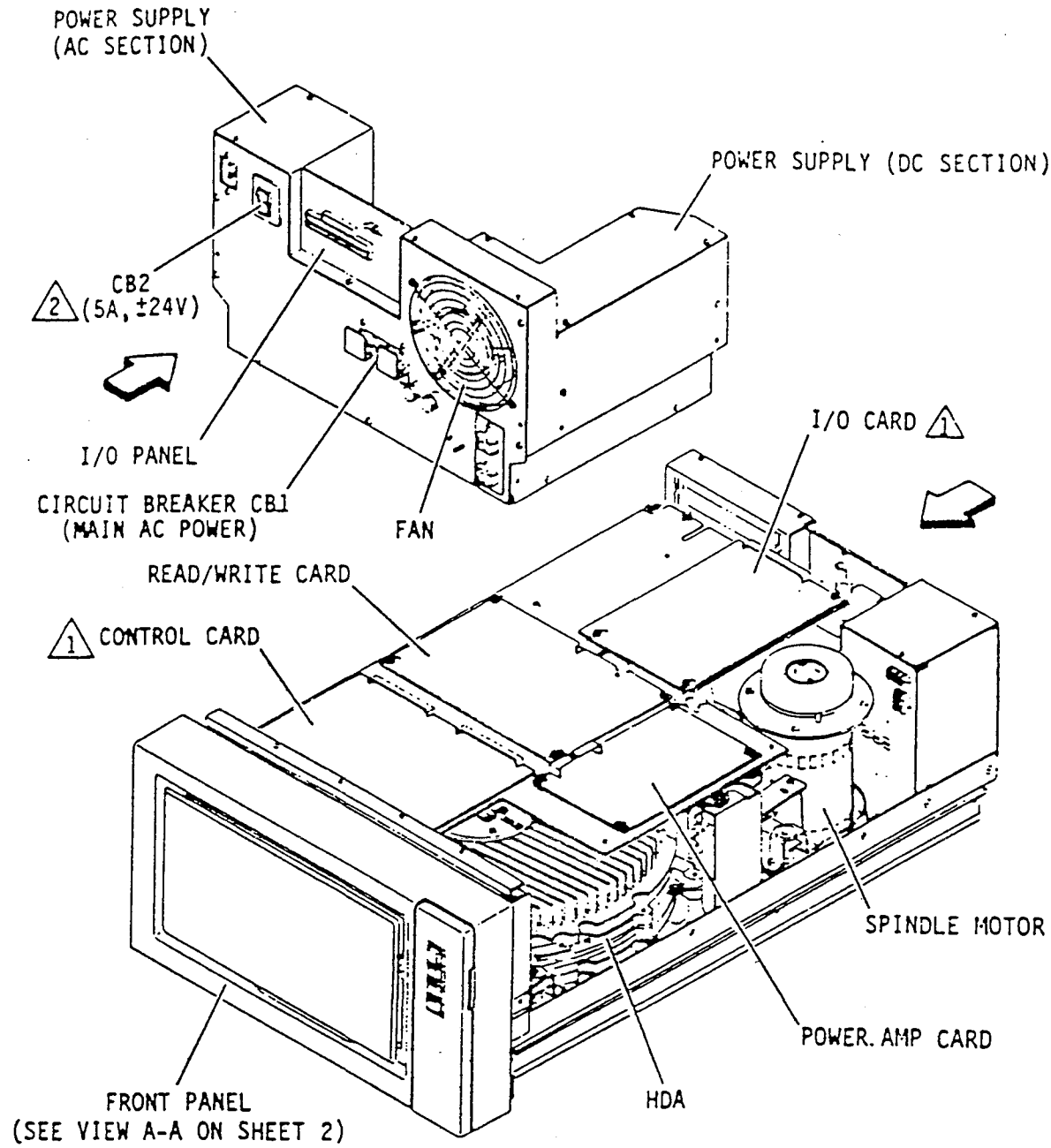
Switch/Indicator	Function
	The ±5 V supplies are protected by current limiting circuitry in the power supply.
CB2 (±24 V) circuit breaker	Protects the voice coil in the module from overheating caused by failure of the power amplifier board.
	FRONT PANEL
Logic plug/unit selected indicator	The logic plug activates switches that establish the logical address of the device. A logic plug, numbered 0, is included with each unit, and logic plugs, numbered 1 through 15, are available as options. The unit selected indicator is lit if the spindle is selected.
START switch/ready indicator	The START switch has alternate action, in for start and out for stop, and it contains the ready indicator. Pressing the START switch to the start position activates the power-up sequence, and the ready indicator flashes until the disks are up to speed, the heads are loaded, a stabilization period has elapsed, and there are no fault conditions. The ready indicator is on steady with power up complete. Pressing the START switch to release it from the start position causes the ready indicator to flash for 30 seconds.
FAULT indicator/fault clear switch	The FAULT indicator is inside the fault clear switch, and it lights if a fault exists within the spindle. It is turned off by any of the following (provided that the error condition or conditions no longer exist):

Table 2-2. XMD Spindle Switches and Indicators Functions (continued).

Switch/Indicator	Function
	• Pressing the fault clear switch • Fault clear command from the controller • Reapplying ac power to the spindle
WRITE PROTECT switch/ indicator	The operation of the WRITE PROTECT switch, or installing the write protect plug on the control board, places the spindle in the write protected mode (preventing write operations) and lights the WRITE PROTECT indicator.
	CONTROL BOARD
Sector select switches	Allows the disk to be divided into segments or sectors. The switch settings determine the number of sectors per track.
	FAULT/STATUS DISPLAY BOARD
First seek indicator	Indicates that the spindle failed the first seek/load attempt.
R/W•OC indicator	Indicates a read or write condition occurred during a seek operation (an off-cylinder condition).
WRT indicator	Indicates that a write fault occurred.
RD•WRT indicator	Indicates that a read and a write command existed simultaneously.
VOLT indicator	Indicates a below normal voltage existed.
HD SEL indicator	Indicates a multiple head selected fault has occurred.
Diagnostic mode indicator	Indicates that the spindle is in diagnostic mode (green LED).

Table 2-2. XMD Spindle Switches and Indicators Functions (continued).

Switch/Indicator	Function
Diagnostic mode switch	Places the spindle in diagnostic mode and disables the I/O.
Diagnostic execute switch	Starts and stops diagnostic tests.
Diagnostic step switch	Selects individual diagnostic tests.
Diagnostic/servo fault display	When a spindle is in diagnostic mode, the display indicates which diagnostic test is being initiated. If a failure occurs, the status code display indicates which major assembly or assemblies are the most likely cause of the problem. When a spindle is not in diagnostic mode, the display indicates error status code generated by the microprocessor.
	I/O BOARD
DEVICE ID switches	Provide a device type status code. Switch settings determine a device ID code that conforms to individual customer requirements.
I/O OPTIONS switches	Allow selection of specific I/O options. Switch settings determine which options are enabled.



NOTES:

1. SWITCHES LOCATED ON CIRCUIT BOARDS ARE ILLUSTRATED IN SECTION 3.
2. PROTECTS VOICE COIL IN MODULE.

Figure 2-3. XMD Spindle Switches and Indicators (Sheet 1 of 2)

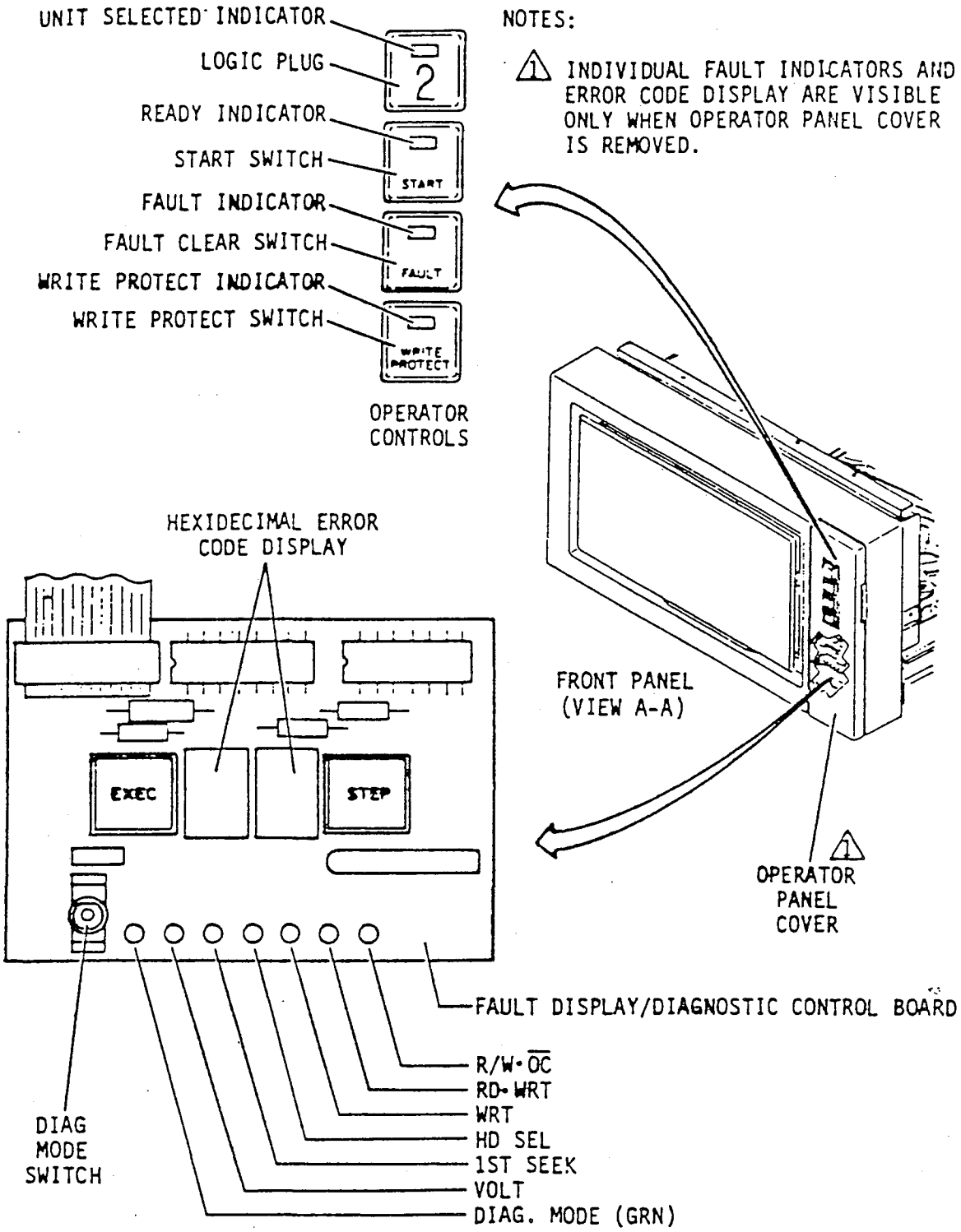


Figure 2-3. XMD Spindle Switches and Indicators (Sheet 2 of 2)

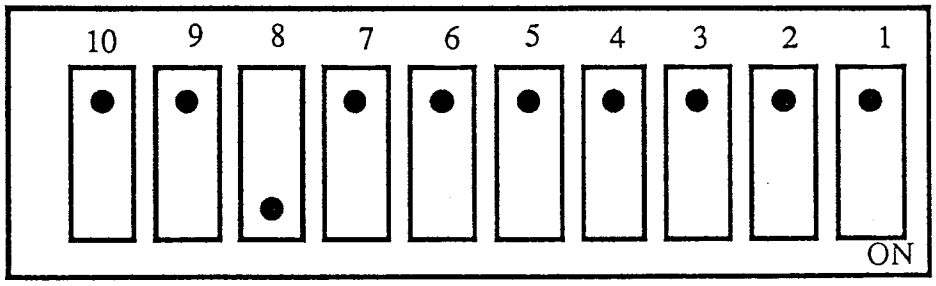
I/O BOARD SWITCH SETTINGS

On the NO board, there are two sets of switches. The set of switches at location E103 is for setting a device I.D. but is unused for drives in the DD40. The other set of switches located at C503 is used to select the I/O options. The following table gives the switch numbers (1-10) along with the switch I.D., the position of each switch and a description of the option used in the DD40. All switches are in the "OFF" position except switch number 8 which is "ON" to select the extended cylinder addressing.

SWITCH SETTINGS FOR I/O OPTIONS

Switch Number	Switch I.D.	Description of I/O Options used in the DD40
1	1A	OFF - Index & Sector in Channel 1, A Cable
2	1B	OFF - Index & Sector in Channel 1, B Cable
3	2A	OFF - Index & Sector in Channel 2, A Cable (Not Used)
4	2B	OFF - Index & Sector in Channel 2, B Cable (Not Used)
5	1D	OFF - Channel 1 Enabled
6	2D	OFF - Channel 2 Enabled (Not Used)
7	SO	OFF - Extended SMD Mode
8	XA	ON - Extended Cylinder Addressing
9	AR	OFF - Absolute Reserve Mode
10	RL	OFF - Remote Power Up

Located at C503



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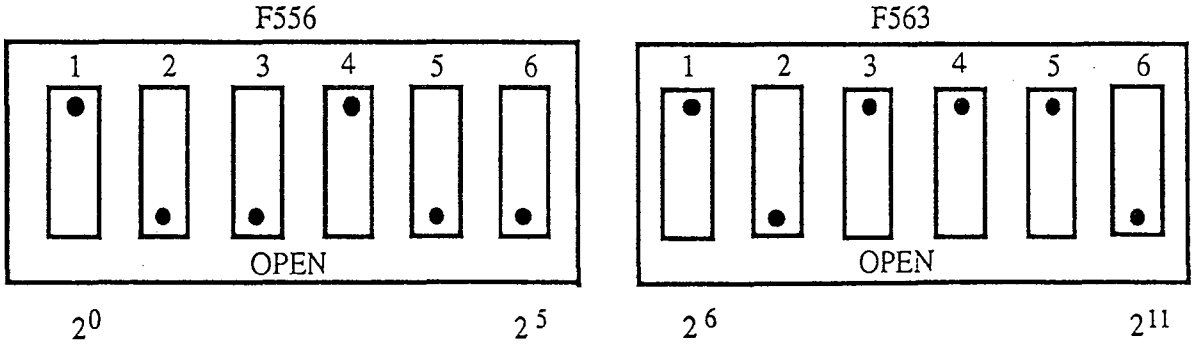
DC4004W100M S.J.M .

The sector switches are located on the control board and are set to predetermined value to provide 12 sectors per revolution. The following table shows the location of the two switch packages on the control board, F556 and F563. It also gives the desired number of sectors in the left most column followed by the setting for each of the individual switches. Each switch is represented by either a C for closed or an O for open.

The switches preset a byte counter. The counter is incremented by each servo byte until it reaches a value of 4095 when it is preset again. Each servo byte is equal to 2.25 data bytes. The switches are shown in the following figure. Bit 2^0 is the left most switch and bit 2^{11} is the right most switch.

SECTOR SELECT SWITCH SETTINGS

Number of Sectors	Location F556 Switch Number						Location F563 Switch Number					
	1	2	3	4	5	6	1	2	3	4	5	6
6	O	O	C	O	C	O	O	C	O	C	C	C
7	C	C	C	C	C	C	C	O	O	O	C	C
8	C	C	C	C	O	C	C	C	O	C	O	C
9	C	C	C	O	C	C	O	C	C	O	O	C
10	C	C	C	C	C	C	O	C	O	O	O	C
11	C	C	O	O	C	C	C	C	C	C	C	O
12	C	O	O	C	O	O	C	O	C	C	C	O
13	O	C	O	C	C	C	O	C	O	C	C	O
14	C	C	C	C	C	C	O	O	O	C	C	O
15	O	O	C	O	C	O	C	C	C	O	C	O



SECTOR SWITCHES

POWER ON INITIALIZATION

The power on initialization is the process the drive goes through from the time power is applied until the drive is waiting for start conditions.

For power on initialization to occur, both CB1 and CB2 must be on to provide AC and DC power to the drive. Until the +5V reaches 4.9V, the drive Master clear signal is active which resets the sector count and disables the Interface Card.

When drive power reaches its desired level there is a 3 ms. delay, after which the MPU starts three self tests. These tests are:

-A check of the MPU firmware instructions.

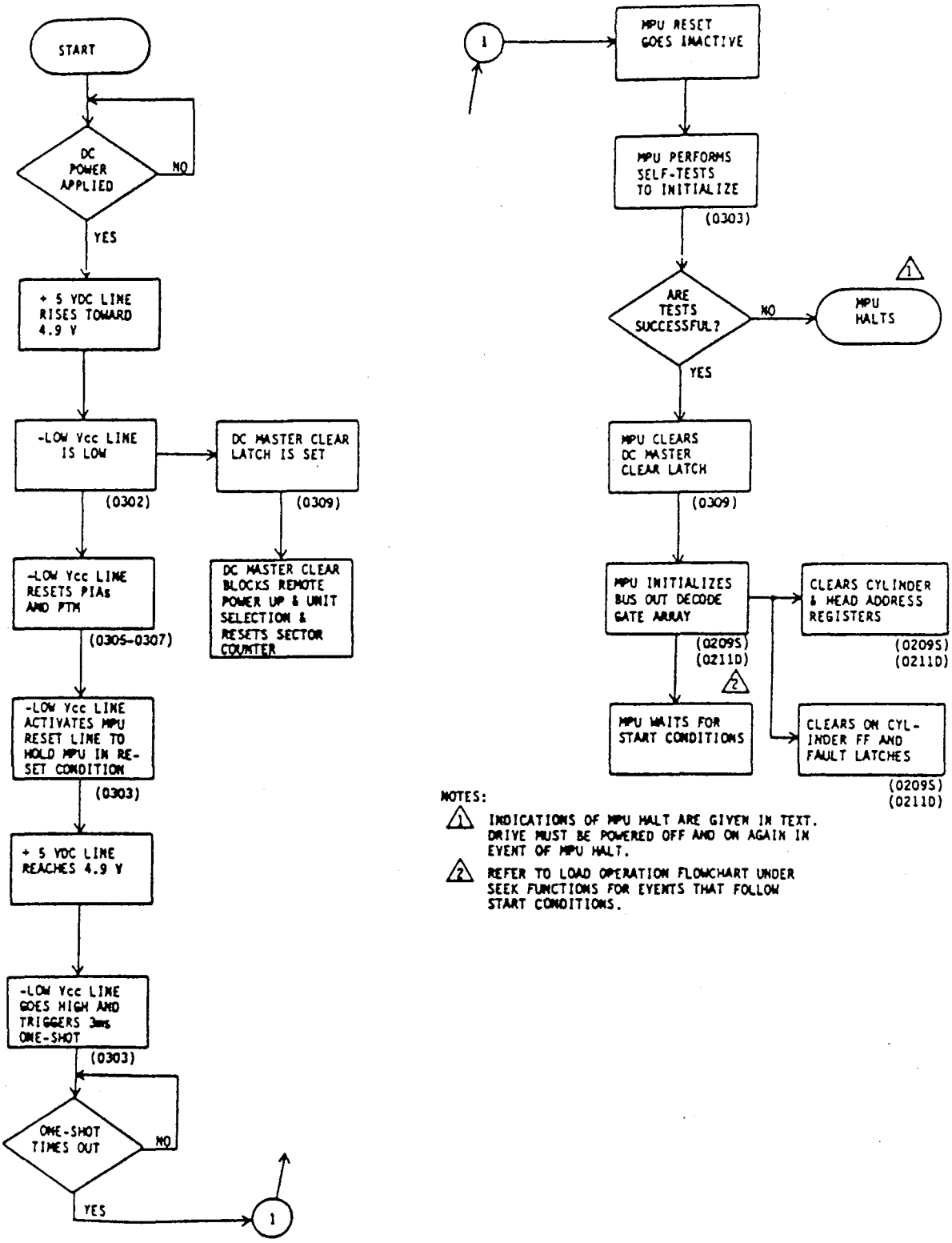
-Writing to and reading from the RAM.

-The MPU sends data to the peripheral interface adapters (PIA) and reads it back to initialize them.

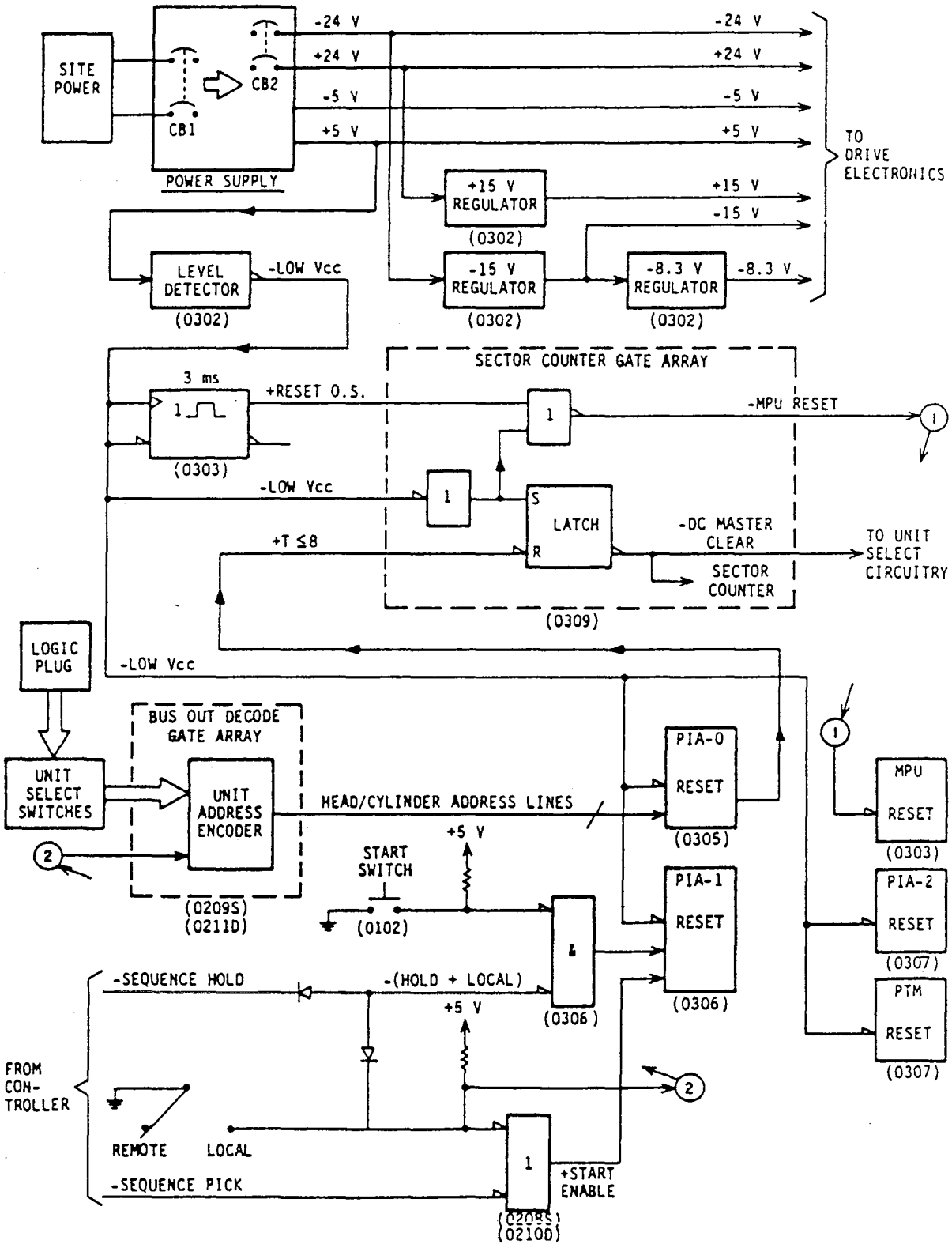
If one of the first two tests fail, the MPU stops and turns on all fault LEDs on Fault panel. If the third test fails, the MPU attempts to turn on the First Seek LED. Any fault on the power on initialization must be cleared by a power cycle.

After the self tests have been successfully completed, the Master Clear becomes inactive and the MPU clears the cylinder address register, head address register, on-cylinder FF, and the fault latches. The MPU now waits for the start conditions before starting the load operation.

Figure 2-5 shows the power on circuitry and Figure 2-6 shows the power on initialization flowchart. Both figures can be used as an aid in troubleshooting problems that occur during a power on initialization.



Power On Initialization Flowchart



Power On Circuitry

2.3 XMD POWER-ON AND POWER-OFF PROCEDURES

The power supply circuit breaker (CB1) on the power supply rear panel is usually left on, so that dc power is available to the drive.

The following procedure describes how to power-up the DD-40.

1. Press the START switch. If the LOCAL/REMOTE switch was set in the REMOTE position during drive installation, the power up sequence continues when power sequence ground is available from the controller. If the LOCAL/REMOTE switch was set in the LOCAL position, the power-up sequence begins immediately. When set to the REMOTE position, the power-up sequence of each spindle (except spindle 0) is delayed. The length of the delay is determined by the number of the unit logic plug used in increments of $\frac{1}{10}$ seconds. Delay = 10 sec X Unit plug #
2. Observe that the ready indicator (located in the START switch) flashes, indicating that power-up is in progress.
3. Observe that the ready indicator lights steadily within 3 minutes and 30 seconds, indicating that the disks are up to speed, the heads are loaded, and a stabilization period has elapsed.
4. Ensure that the FAULT indicator is off.

The power-up sequence is now complete, and the drive is ready to write data.

The following procedure describes how to power-down the DD-40.

1. Press the START switch to release it from the start position.
2. Observe that the ready indicator (located in the START switch) flashes, indicating that power-up is in progress.
3. Observe that the READY indicator goes off after approximately 30 seconds.

When power-down is complete, the heads are positioned in the landing zone and the disks are not rotating. Normally, the power supply circuit breaker (CB1) is left on to continue supplying power to the drive.

LOAD OPERATION

When the power on initialization is complete, the MPU checks the Over Temperature on the Power Amp board to make sure it is inactive and waits for the start conditions. The MPU will wait for the start switch to be depressed. When this happens, provided the remote/local switch is in the remote position and that the DD40 has its A cables connected to the DC40 to provide the correct signal on the sequence Pick and Hold lines, the MPU will start the load operation. Once these conditions are met, a delay is started. This delay is:

Unit Address X 10 sec = Delay (in Seconds)

When the delay ends the MPU unlocks the actuator, pulls the heads against the carriage stop, and the motor starts to spin. The Ready light on the operator's panel will start to flash. The MPU checks for the signal Speed OK within three to seven seconds. If Speed OK is not detected in three attempts, the MPU will stop trying and wait for CB1 to be turned off and back on again to allow another three attempts.

When Speed OK is detected by the MPU, it checks and rechecks the speed until the drive is spinning at the rated speed. This is done by counting Speed pulses.

The MPU enables the Power Amplifier, checks for any faults, and starts a 200 ms. timer. The MPU starts pulsing the voice coil to move the actuator inward. This continues until a servo signal is detected. The actuator is now moving inward. After 40 ms. the MPU checks for 32 cylinder crossing pulses. When the 32 pulses are detected, the MPU checks that the 200 ms. timer has not timed out. At this point, heads are over the data area. The actuator direction is reversed and starts moving outward under coarse control. The actuator moves in the outward direction until the outer guardband is detected. Once the outer guardband is detected the MPU checks for two cylinder pulses. The actuator is turned around and moves toward Cylinder 0. The MPU must detect at least one cyclinder pulse for the outer guardband. There is one additional cylinder pulse detected before the heads reach Cylinder 0. With one third track to go, fine control is enabled and coarse control is disabled.

The MPU checks that on-cylinder stays active for 2.1 ms. If it does not, the MPU will wait for up to 11 ms. for on-cylinder to go active and check it again. When on-cylinder stays active for 2.1 ms. and the servo signal is still present and three or more cylinder crossing pulses were not detected after on-cylinder, the MPU starts the scan cycle.

The scan cycle consists of two cycles of single track seeks from Cylinder 0 to 1419 and back to 0. (See Figure 2-7). The scan cycle is followed by the velocity calibration cycle which executes a series of 128 track seeks to calibrate the velocity measurement circuit.

At the end of the load operation, the heads are positioned to Cylinder 0. A successful load operation will take 3 minutes and 30 seconds. A successful load operation is indicated by a steady unit ready light and unit ready and seek end being sent to the controller. The DD40 is ready to receive commands from the DC40.

During the load operation, the MPU periodically checks the fault line to make sure there is no fault present. It also checks for other conditions that must be present to allow the load operation to continue. The following is a list that will cause a first seek fault.

-A fault is detected during the load operation.

-The servo signal is present before the actuator starts to move forward.

-It takes longer that 200 ms. to detect 32 cylinder pulses.

-The servo signal is lost during the reverse motion of the actuator.

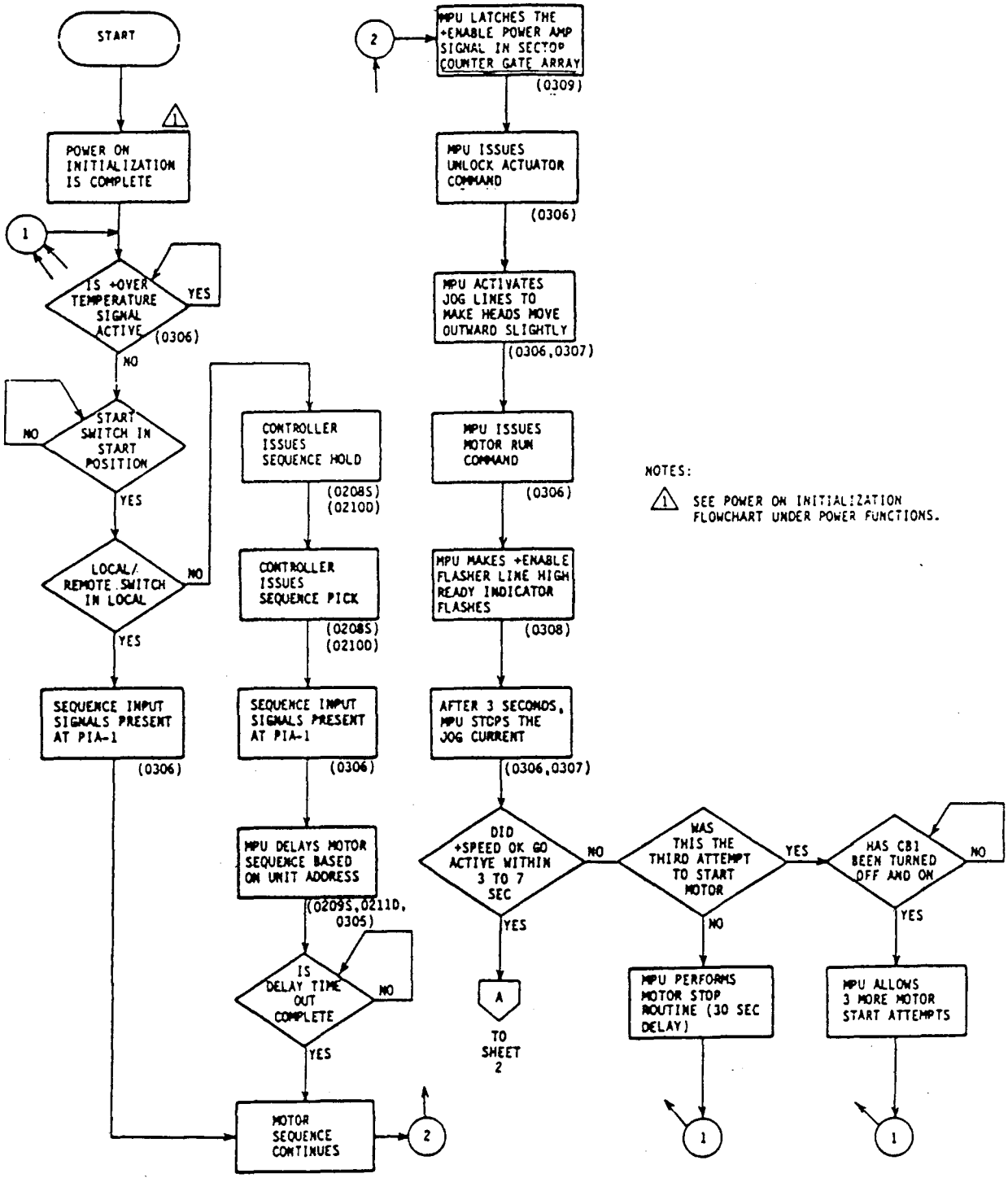
-At least one cylinder pulse of the outer guardband was not detected before Cylinder 0 was found.

-Three or more cylinder pulses are detected after Cylinder 0 has been detected.

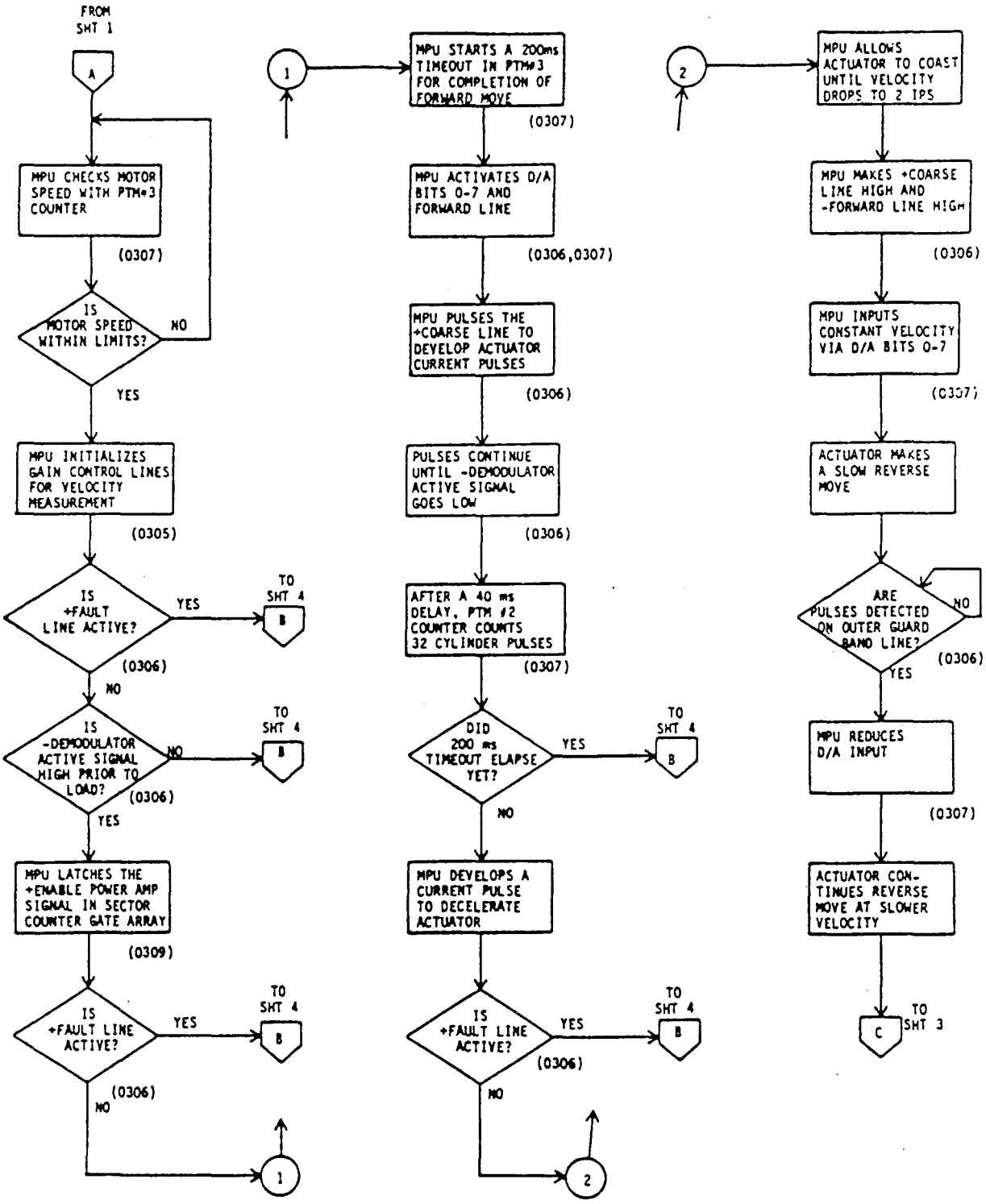
-When Cylinder 0 has been detected and on-cylinder is active, if on-cylinder goes inactive before 2.1 ms. and does not return to the active state in 11ms.

Any of the above occurances will cause the MPU to set fault first seek fault, retract and lock the actuator, and send servo status to the fault display board. When the fault is cleared, the MPU will attempt another load operation.

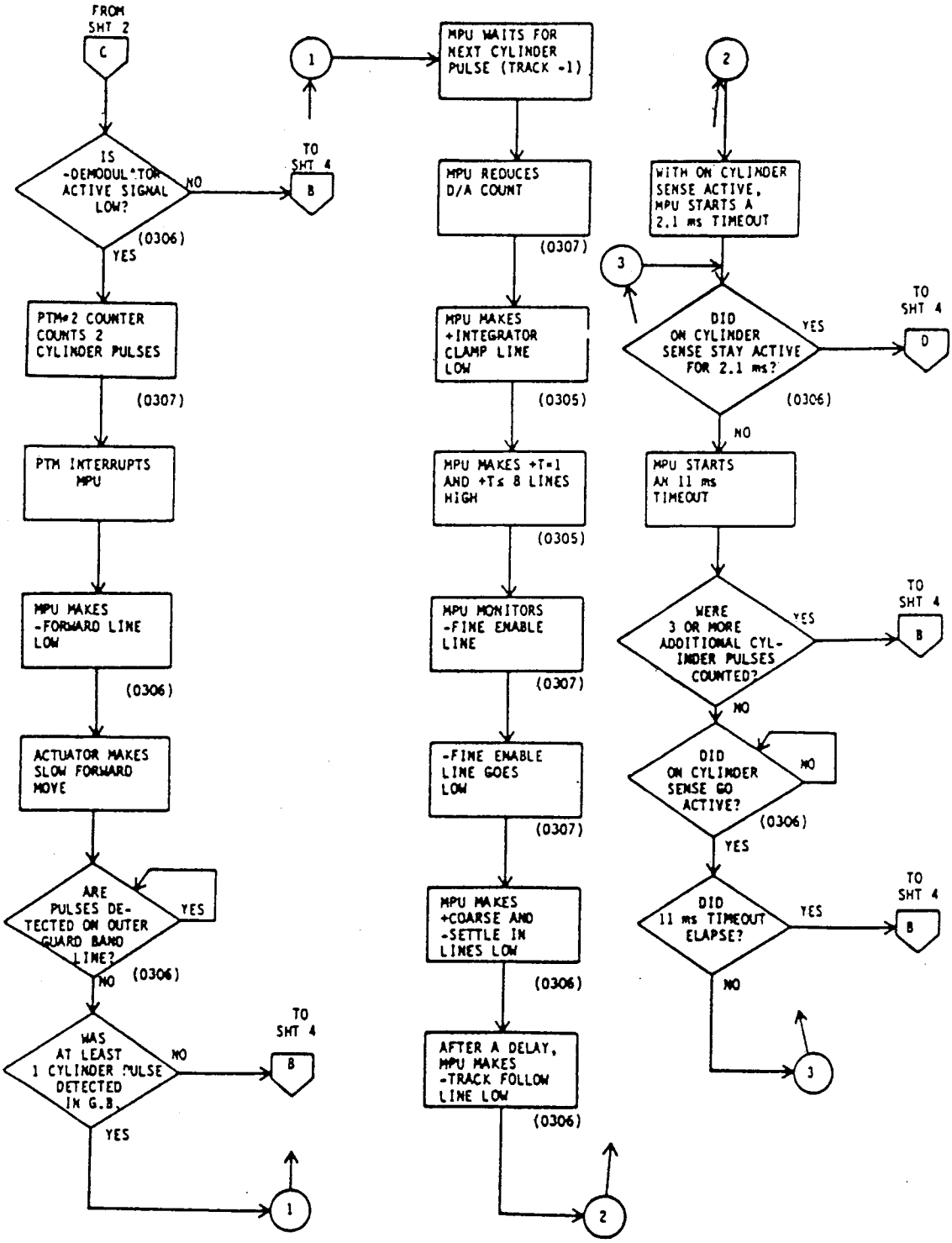
The Load Operation Flowchart gives a step by step flow of this operation. The Load Trajectory shows the movement of the actuator during the load operation.



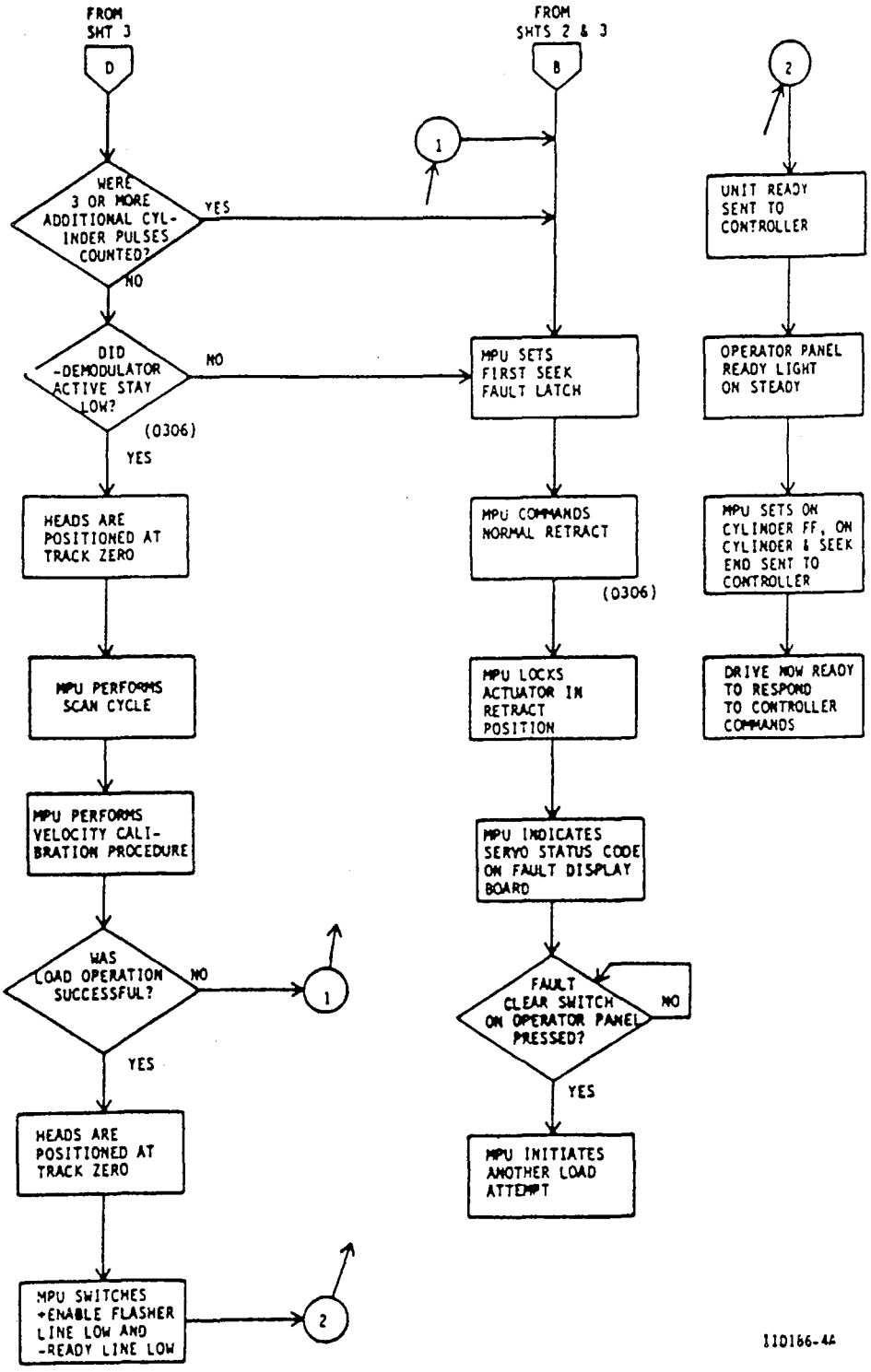
Load Operation Flowchart (Sheet 1 of 4)



Load Operation Flowchart (Sheet 2)

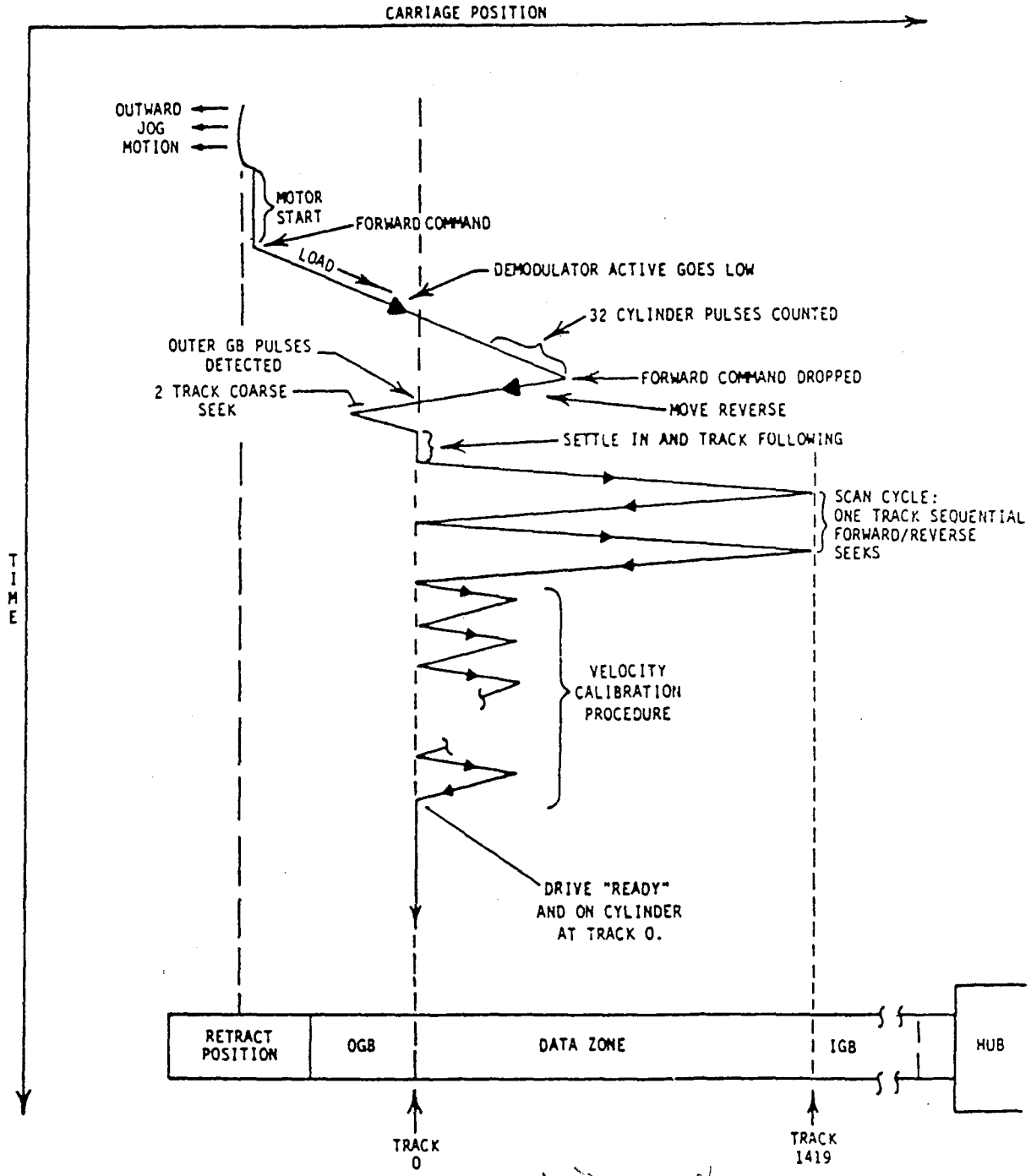


Load Operation Flowchart (Sheet 3)



Load Operation Flowchart (Sheet 4)

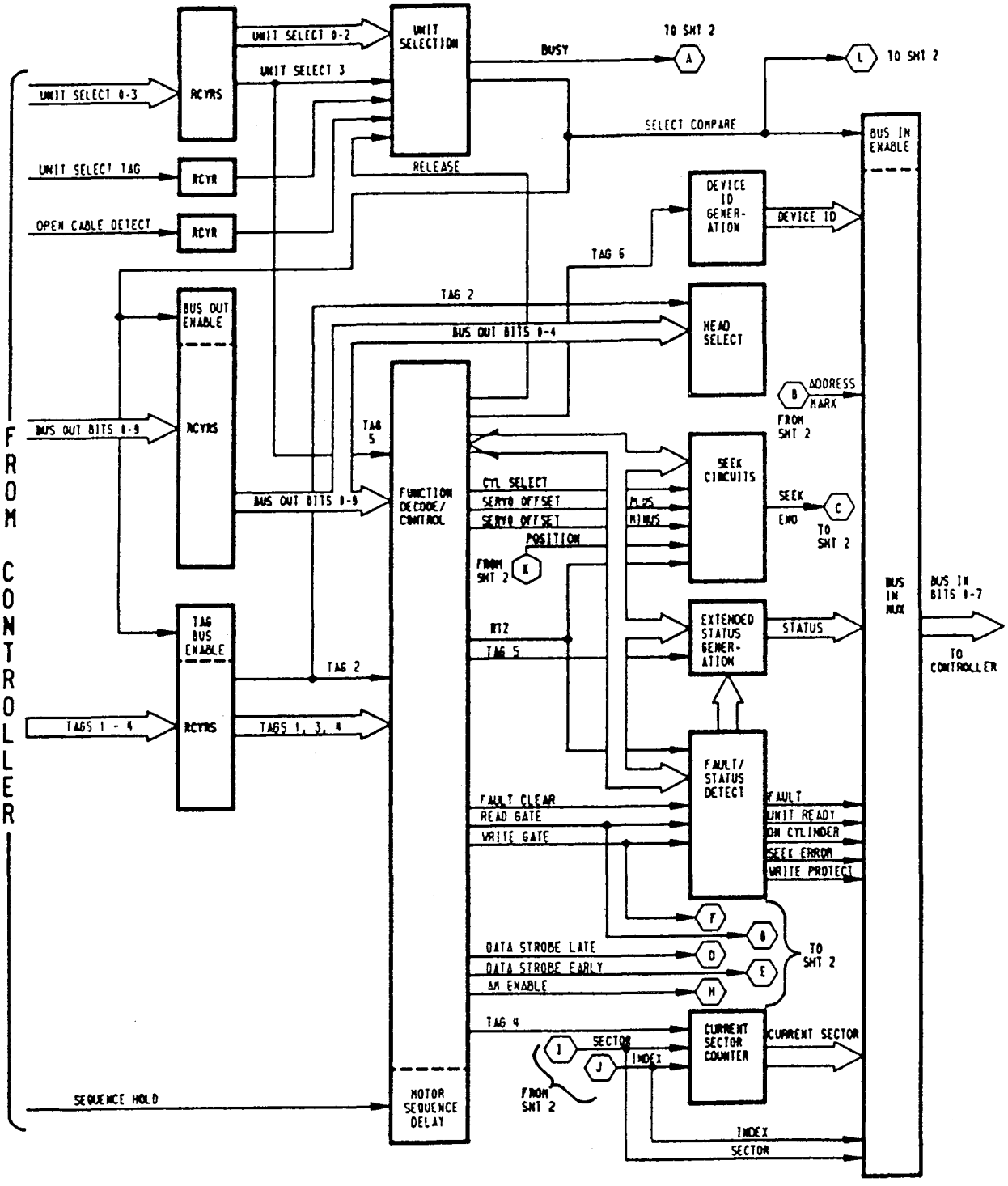
The Load Seek Trajectory summarizes what happens during the load operation. It also shows the movement of the heads with respect to the guardbands and the data zones.



if this stuff don't work "first seek fault"

Load Seek Trajectory

The I/O signals for the A cable are shown on page 2-10N, I/O Signal Processing (Sheet 1 of 2). The signals on the A cable are listed in the table on page 2-10O and a brief discription is given on the page 2-10P. The I/O signals for the B cable are shown on page 2-10Q, Sheet 2 of I/O Signal Processing figure. The signals for the B cable are listed on page 2-10R. A brief description of the B cable signals is given on page 2-10S.



I/O Signal Processing (Sheet 1 of 2)

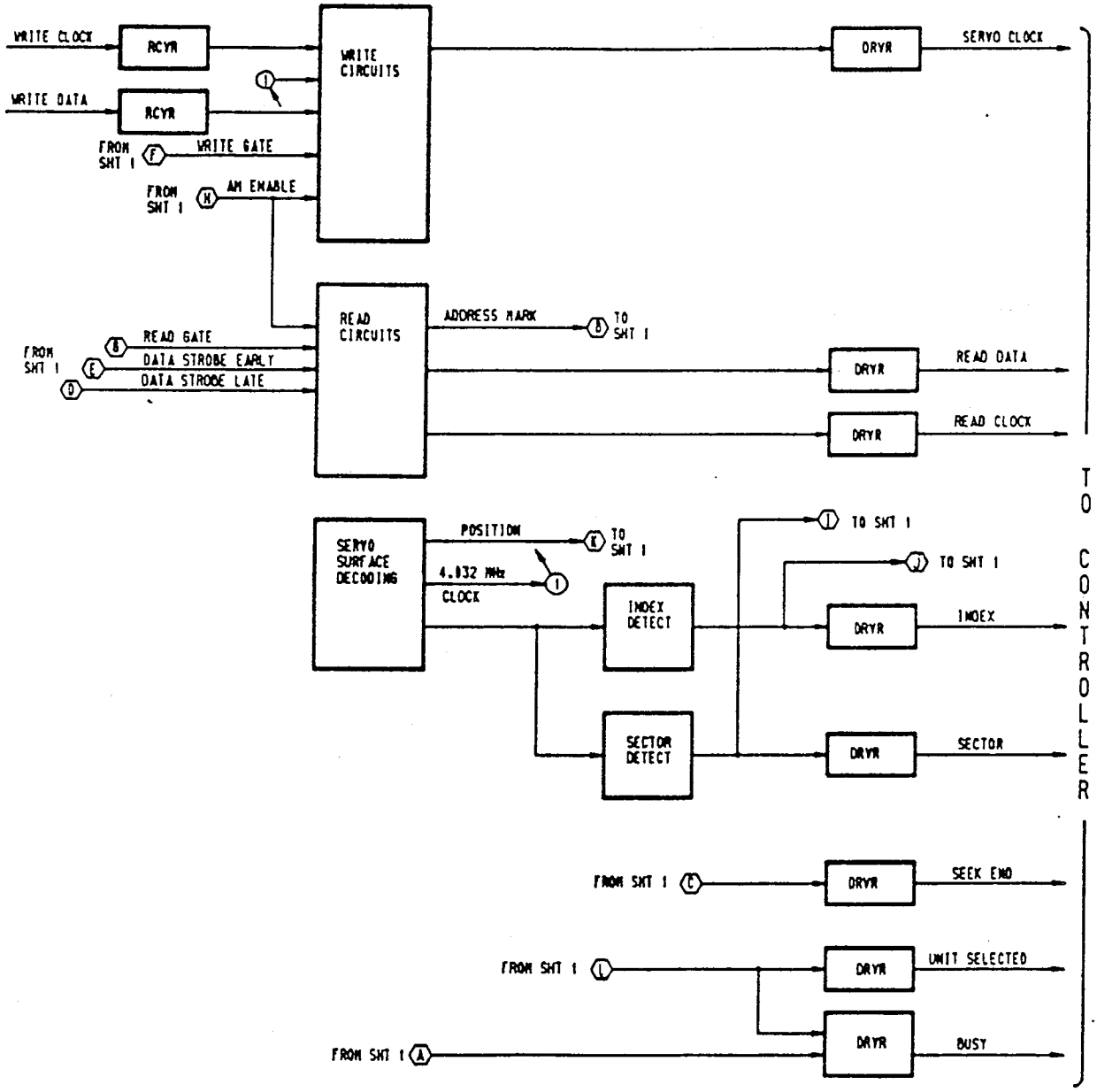
I/O BOARD - VJX

A CABLE - J03/J04

SIGNAL	DC40 - I/O	XMD - LO/HI
Unit Select Tag	R0 - 2EJ	22/52
Unit Select bit 0	R1 - 2EJ	23/53
Unit Select bit 1	R2 - 2EJ	24/54
Unit Select bit 2	R3 - 2EJ	26/56
Tag 1	R4 - 2EJ	1/31
Tag 2	R5 - 2EJ	2/32
Tag 3	R6 - 2EJ	3/33
Tag 4	R7 - 2EJ	30/60
Tag 5	R8 - 2EJ	27/57
Bus 0	R9 - 2EJ	4/34
Bus 1	R10 - 2EJ	5/35
Bus 2	R11 - 2EJ	6/36
Bus 3	R12 - 2EJ	7/37
Bus 4	R13 - 2EJ	8/38
Bus 5	R14 - 2EJ	9/39
Bus 6	R15 - 2EJ	10/40
Bus 7	R16 - 2EJ	11/41
Bus 8	R17 - 2EJ	12/42
Bus 9	R18 - 2EJ	13/43
Status 0	I18, I26, I34, I42 - 2EM	19/49
Status 1	I19, I27, I35, I43 - 2EM	17/47
Status 2	I20, I28, I36, I44 - 2EM	16/46
Status 3	I21, I29, I37, I45 - 2EM	15/45
Status 4	I22, I30, I38, I46 - 2EM	28/58
Status 5	I23, I31, I39, I47 - 2EM	20/50
Status 6	I24, I32, I40, I48 - 2EM	18/48
Status 7	I25, I33, I41, I49 - 2EM	25/45
Open Cable Detect	R34 - 2EJ	14/44
Busy	N/U	21/51
Spindle Sequence Pick	Controller GND	29
Spindle Sequence Hold	Controller GND	59

XMD A Cable Signals

Signal	Description
Unit Select Tag	This signal is sent to the drive along with the Unit Select Bits 0-2 to select the desired unit.
Unit Select Bits 0-2	These signals must be active at least 200 ns before the Unit Select Tag becomes active. Only Unit Select bit 0 is used by the DC40 to select either the Primary ($2^0 = 0$) or Shadow ($2^0 = 1$) DD40. (Unit Select Bit 3 is used on Tag 5.)
Tag 1	Lower cylinder select, bits 2^0-2^9. (When doing a cylinder select the higher bits must be sent first.)
Tag 2	Head Select/Higher Cylinder Bits. Head select bits are represented in Bus Out Bits 2^0-2^4. The upper cylinder bits (2^{10} and 2^{11}) are represented by Bus Out Bits 2^7 and 2^8. (The upper cylinder bits must be sent before the lower cylinder bits.)
Tag 3	Enable the Control bits to be sent out on the bus. When the Bus Out Bit is active it controls the following in the XMD. 2^0 - Write Gate 2^1 - Read Gate 2^2 - Offset + Offsets positioner toward the spindle for 2.75 ns. 2^3 - Offset - Offsets positioner away from the spindle for 2.75 ns. 2^4 - Clear Fault 2^5 - Not used 2^6 - RTZ 2^7 - Data Strobe Early 2^8 - Data Strobes Late 2^9 - Not Used
Tag 4 and 5 (See individual status words for bit by bit discription in Troubleshooting section of this manual.)	Selected Status Tag 4 - Sector Status Tag 5 - Extended Status B0B0=0 B0B1=0 Tag 5 - Operating Status B0B0=1 B0B1=0 Tag 5 - Diagnostic Status B0B0=0 B0B1-1 Tag 5 - Diagnostic Execute Status B0B0=1 B0B1=1
Open Call Detect	Detects loss of power in DC40
Pick	DC40 Ground
Hold	DC40 Ground
Bus In Bits 0-7	Drive Status or Selected Status



I/O Signal Processing (Sheet 2)

I/O BOARD - VJX

B CABLE - J02

SIGNAL	PRIMARY DC40 - I/O	XMD - LO/HI
Write Data	R4, R12, R20, R28 - 2EK	8/20
Ground		7
Write Clock	R5, R13, R21, R29 - 2EK	6/19
Ground		18
Servo Clock	I6, I22, I32, I42 - 2EK	2/14
Ground		1
Read Data	I5 - 2EJ	3/16
Ground		15
Read Clock	I6 - 2EJ	5/17
Ground		4
Seek End	I10 - 2EJ	10/23
Ground		11
Unit Selected	I9 - 2EJ	22/9
Ground		21
Index	I7 - 2EJ	12/24
Ground		25
Sector	I8 - 2EJ	13/26

SIGNAL	SHADOW DC40 - I/O	
Write Data	R4, R12, R20, R28 - 2EK	8/20
Write Clock	R5, R13, R21, R29 - 2EK	6/19
Servo Clock	I7, I23, I33, I43 - 2EK	2/14
Read Data	I11 - 2EJ	3/16
Read Clock	I12 - 2EJ	5/17
Seek End	I16 - 2EJ	10/23
Unit Selected	I15 - 2EJ	22/9
Index	I13 - 2EJ	12/24
Sector	I14 - 2EJ	13/26

XMD B Cable Signals

The B cable signal for spindle A and B share one 55 pin cable between the DC40 and DD40. The B cable signals for spindle C and D are shared by another cable.

Signal	Description
Write Data	NRZ Data to XMD
Write Clock	24 MHz/41.3ns
Servo Clock	24.192 MHz/41.3ns
Read Data	NRZ Data from XMD
Read Clock	24 MHz/41.3ns
Seek End	Seek End with On cylinder indicates the seek was completed as expected. Seek End without On cylinder indicates a Seek Error. When a Diagnostic Execute Status is performed, Seek End indicates test execution is complete.
Unit Selected	This is the response to a Unit Select Tag and a match between the Unit Select Bits and Drive Address.
Index	Decoded from servo tracks once per resolution.
Sector	12 Sector pulses per revolution. This is determined by the setting on the sector switches.

2.4 DD-40 ADDRESS SELECTION

The XMD spindles within the DD-40 cabinet are not individually addressable from the IOP. A spindle is selected with 3 bits of the unit select bus. The logic plug supplied with the DD-40 is inserted in the top of the operator panel. When inserted, it activates switches that establish the logical address of the DD-40. The logic plug also determines the delay before startup.

In each DD-40 cabinet, three of the four spindles are given the same number. The bottom spindle is one number higher than the other three if the DD-40 is the primary DD-40 and one number lower if it is the shadow DD-40. The top three spindles in the shadow DD-40 are one number higher than the same three spindles in the primary DD-40. Figure 2-4 shows how the addresses of the XMD spindles are specified.

The DD-40's connected to DC-40 disk controller unit 0 use numbers 0 and 1 and the DD-40's connected to disk controller unit 1 use numbers 2 and 3, and so on.

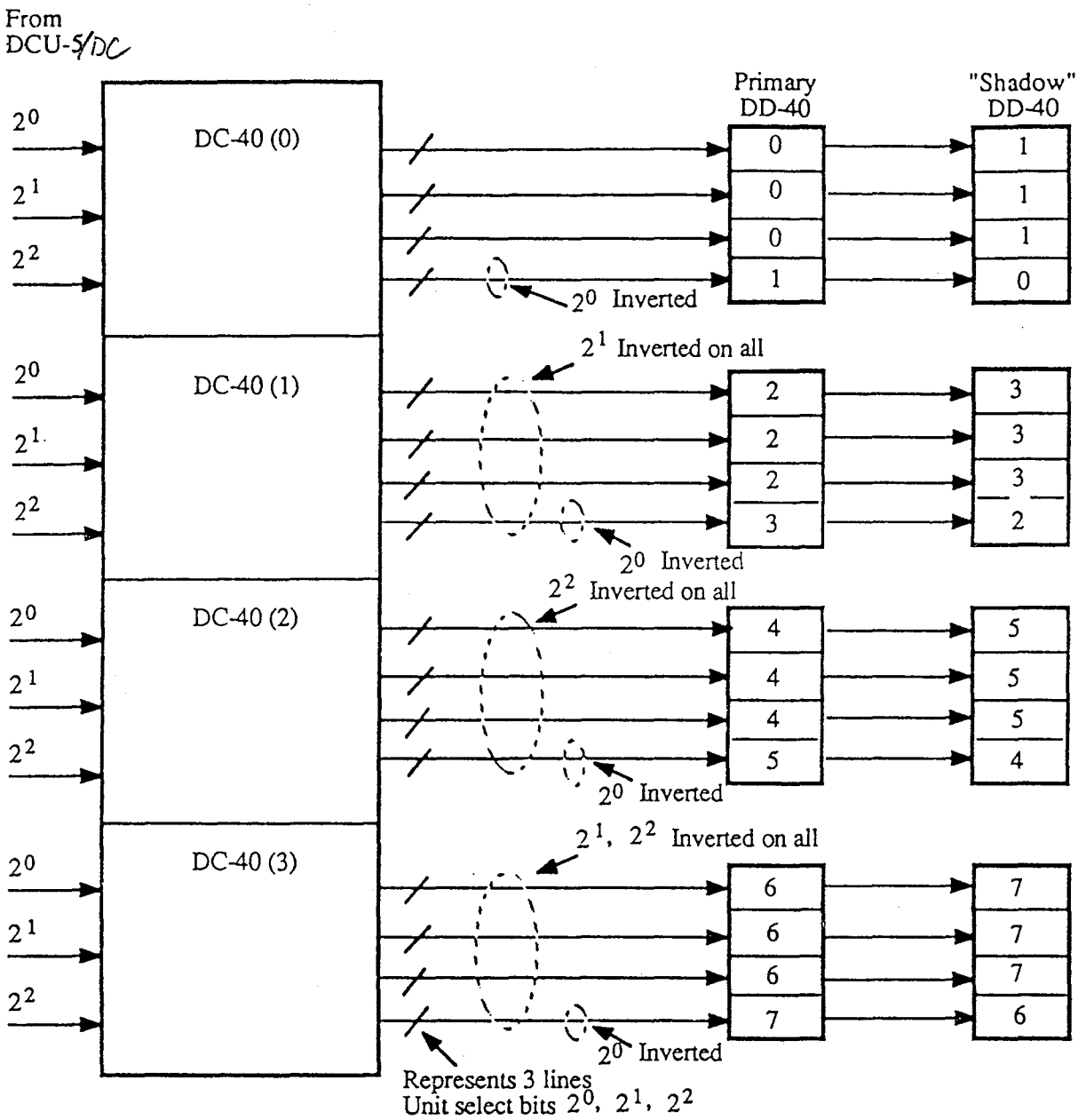
When the primary DD-40 is selected, the unit select command is issued with the lower 3 bits of the accumulator equal to 0's. The unit select tag and the lower 3 bits of the accumulator are sent to the DD-40 from the disk controller unit. Some of the bits are inverted in the drop cables to make the 3 unit select bits match the unit number when they reach the DD-40. When the shadow unit is selected, 2^0 is set in the accumulator. When the logical address of the DD-40 matches the address that is sent by the disk controller, the select compare signal is enabled if open cable detect signal is active. The select compare signal enables the transmitter and receivers. Select compare is also the unit selected signal returned to the DC-40.

When the DD-40 cabinet circuit breaker is turned on, the top three spindles of the primary DD-40 start to spin up first and the bottom spindle starts spinning 10 seconds later. For the shadow DD-40, the bottom spindle starts spinning first and the top three spindles 10 seconds later. The startup delay is the unit number times 10 seconds.

2.5 XMD SPINDLE HEAD SELECTION

The XMD spindle has 19 data heads and 1 servo head. There are 2 heads on a disk surface and 4 heads on a head/arm assembly. The heads must be positioned at the cylinder from which the data is to be read or written before a head can be selected. Only one data head can be selected at a time. Figure 2-5 shows the head select circuits of the XMD-III spindle.

The cylinder address and head address are held in registers in the bus out decode gate array. The spindle's Micro Processor Unit (MPU) uses a series of pulses on I/O control lines 1 and 2 to transfer the cylinder address to the MPU. The MPU sends another series of pulses on I/O control lines 1 and 2 that cause the bus-out gate array to output the head address. Until the spindle is commanded to do another seek, the head address is held on the head/cylinder address lines. The head/cylinder lines go to the read/write board when they address a ROM, which outputs the correct signals on arm select lines 1 through 5.



Note: 000 from DCU-5 selects all Primary drives
001 from DCU-5/DC selects all "Shadow" drives

A-4433

Figure 2-4. XMD Spindle Address Selection

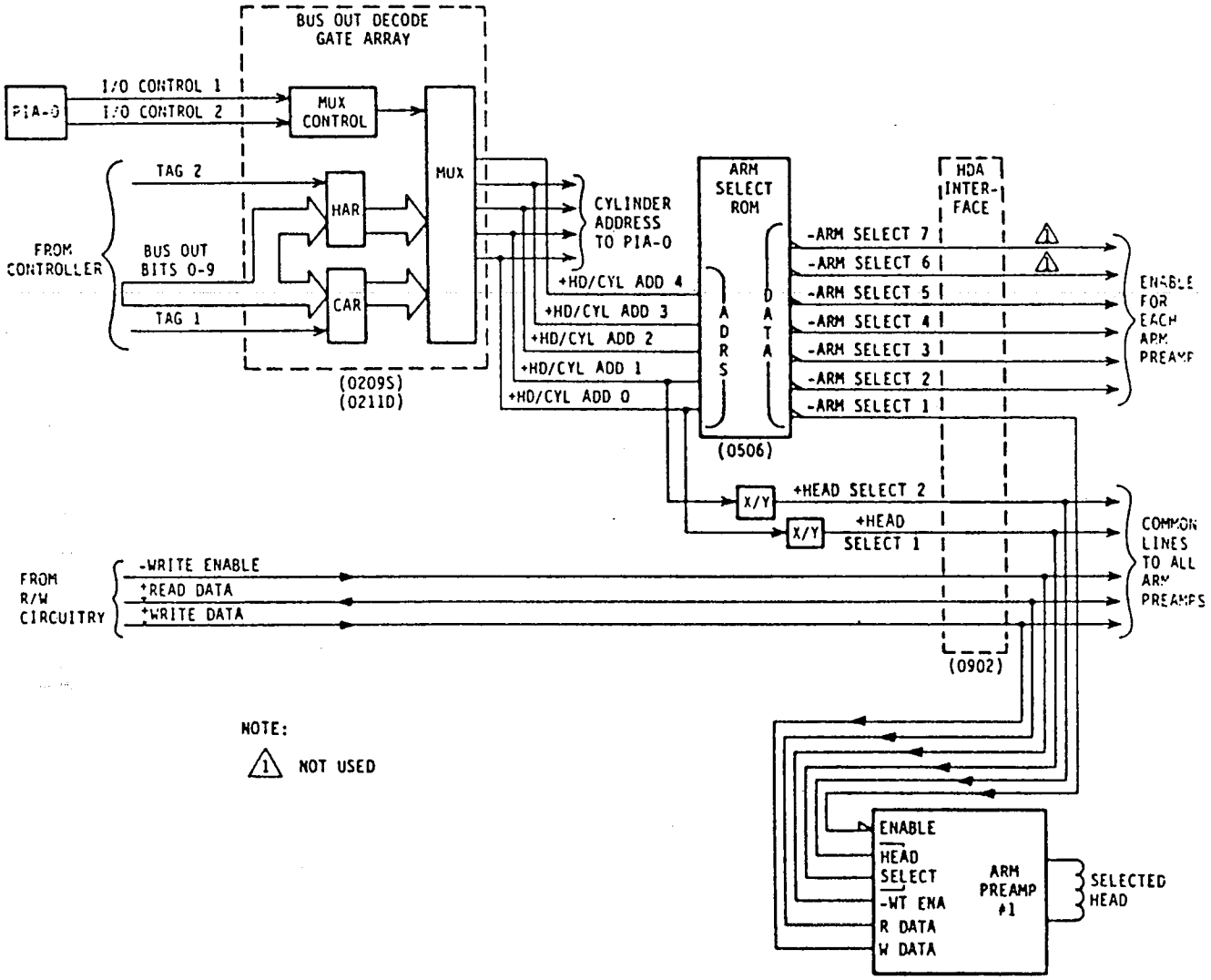


Figure 2-5. XMD Head Select Circuits

If a head address greater than 18 is received, no head is selected. If a write is attempted with no head selected, a write fault occurs.

Table 2-3 lists the head select addressing for the XMD spindles.

Table 2-3. XMD Spindle Head Select Addressing

Head (decimal)	Head (hex)	Arm	Head/Cylinder Address Lines 0	1	2	3	4
0	0	1	0	0	0	0	0
1	1	1	1	0	0	0	0
2	2	1	0	1	0	0	0
3	3	1	1	1	0	0	0
4	4	2	0	0	1	0	0
5	5	2	1	0	1	0	0
6	6	2	0	1	1	0	0
7	7	2	1	1	1	0	0
8	8	3	0	0	0	1	0
9	9	3	1	0	0	1	0
10	A	3	0	1	0	1	0
11	B	3	1	1	0	1	0
12	C	4	0	0	1	1	0
13	D	4	1	0	1	1	0
14	E	4	0	1	1	1	0
15	F	4	1	1	1	1	0
16	10	5	0	0	0	0	1
17	11	5	1	0	0	0	1
18	12	5	0	1	0	0	1

NORMAL SEEK

When the DD40 is ready and selected the controller can send it a command to do a seek. The controller sends the cylinder address to the DD40 in two parts. First, the drive receives the upper two cylinder address bits as bus out bits 2^7 & 2^8 along with the head address and Tag 2. The lower ten cylinder address bits are sent next, along with Tag 1. The maximum cylinder address is 1419. On-cylinder goes low and the MPU is interrupted via PIA-1.

The MPU pulses the Bus Out Decode array and it transfers the cylinder address 4 bits at a time to the MPU RAM where it is stored. After the cylinder address is stored, the head address is ready from the Bus Out Decode array. (See Head Selection). The MPU compares the new cylinder address to the present cylinder address to determine two things, the direction of the seek, and the distance of the seek in tracks.

Before the MPU starts the seek it checks that there is no fault, the servo signal is being detected and the speed is O.K. If no errors are detected, the MPU starts a 60 ms. timer and starts the seek.

If it is a one track seek, the MPU sets T=1 and T≤8 and starts to move the actuator. The actuator accelerates until it reaches the maximum speed for a one track seek. The actuator will coast for a period then decelerate and eventually settle on the cylinder under fine control.

If it is a seek of two or more tracks, the actuator starts moving and the MPU loads the tracks to go into a counter. The actuator continues to accelerate. Each time the servo head crosses a cylinder, a pulse is generated which decrements the counter. The actual speed of the actuator is compared to the expected speed, which is held in a table in the ROM to see if the actuator has reached the desired speed. This will be repeated until the actual speed exceeds the expected speed. When this happens, the counter for tracks to go is checked to see if it is less than 256 tracks to go. If the counter is less than 256 tracks, the actuator begins to decelerate. If the counter is at 256 or more tracks the actuator continues at a constant velocity until the tracks to go is less than 256.

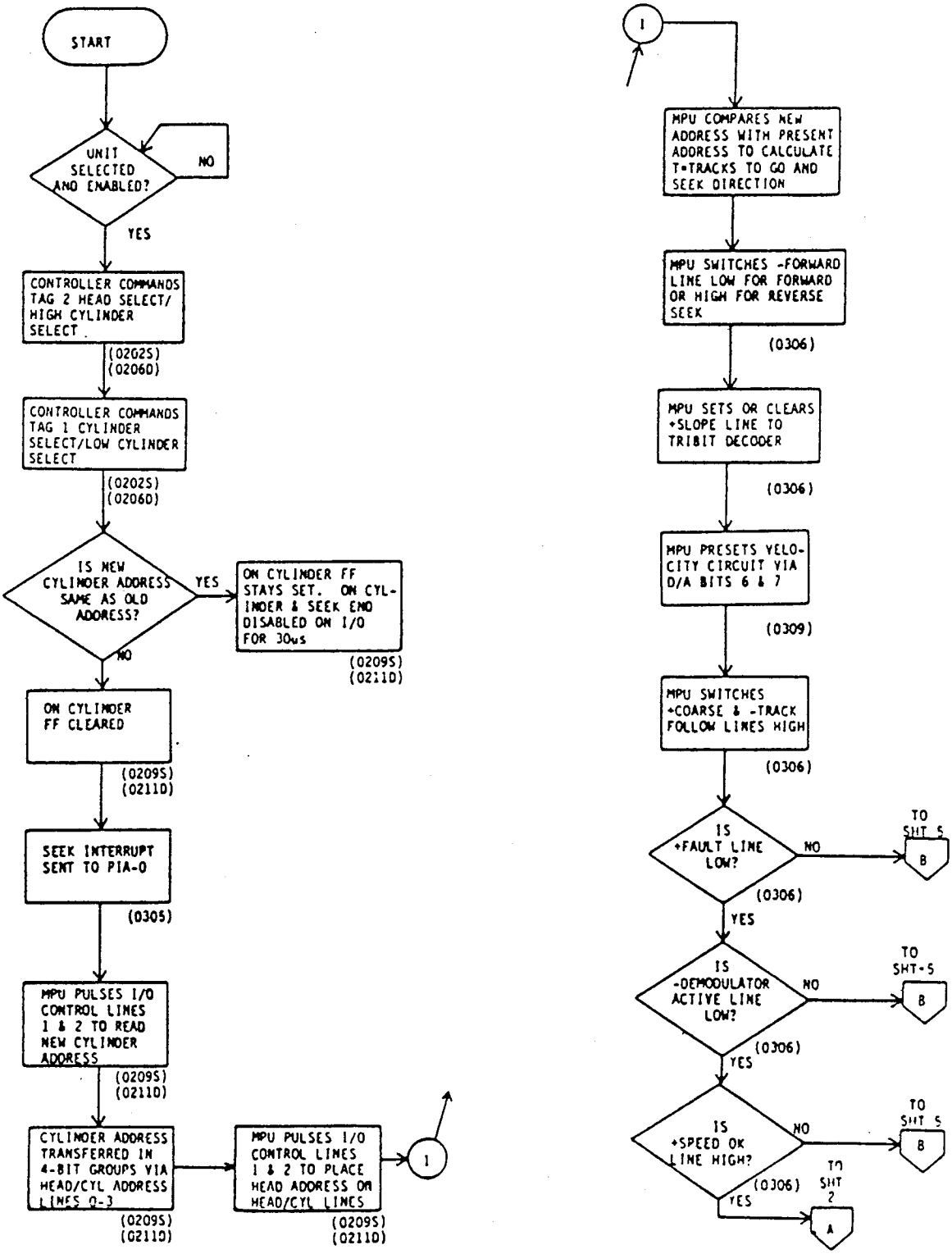
When the tracks to go is less than 256, the actuator begins to decelerate. The MPU starts to compare the actual speed to the next lower desired speed in the ROM table. When the tracks to go are less than or equal to 40, the actuator decelerates again. The MPU begins to compare to the next lower desired speed until the tracks to go are less than or equal to 8. When the last cylinder pulse is detected, the MPU sets T=1 and with 1/3 track to, go the MPU enables the fine control.

After a delay, the servo enters track follow mode. On-cylinder will become active and the MPU will check on-cylinder until it remains active for 2.1 ms. If on-cylinder does not stay active for 2.1 ms., it must return to the active state within 11 ms. so the MPU can check it again. This cycle will repeat until either the on-cylinder signal stays active for 2.1 ms. or the 11 ms. timer expires before on-cylinder returns to the active state.

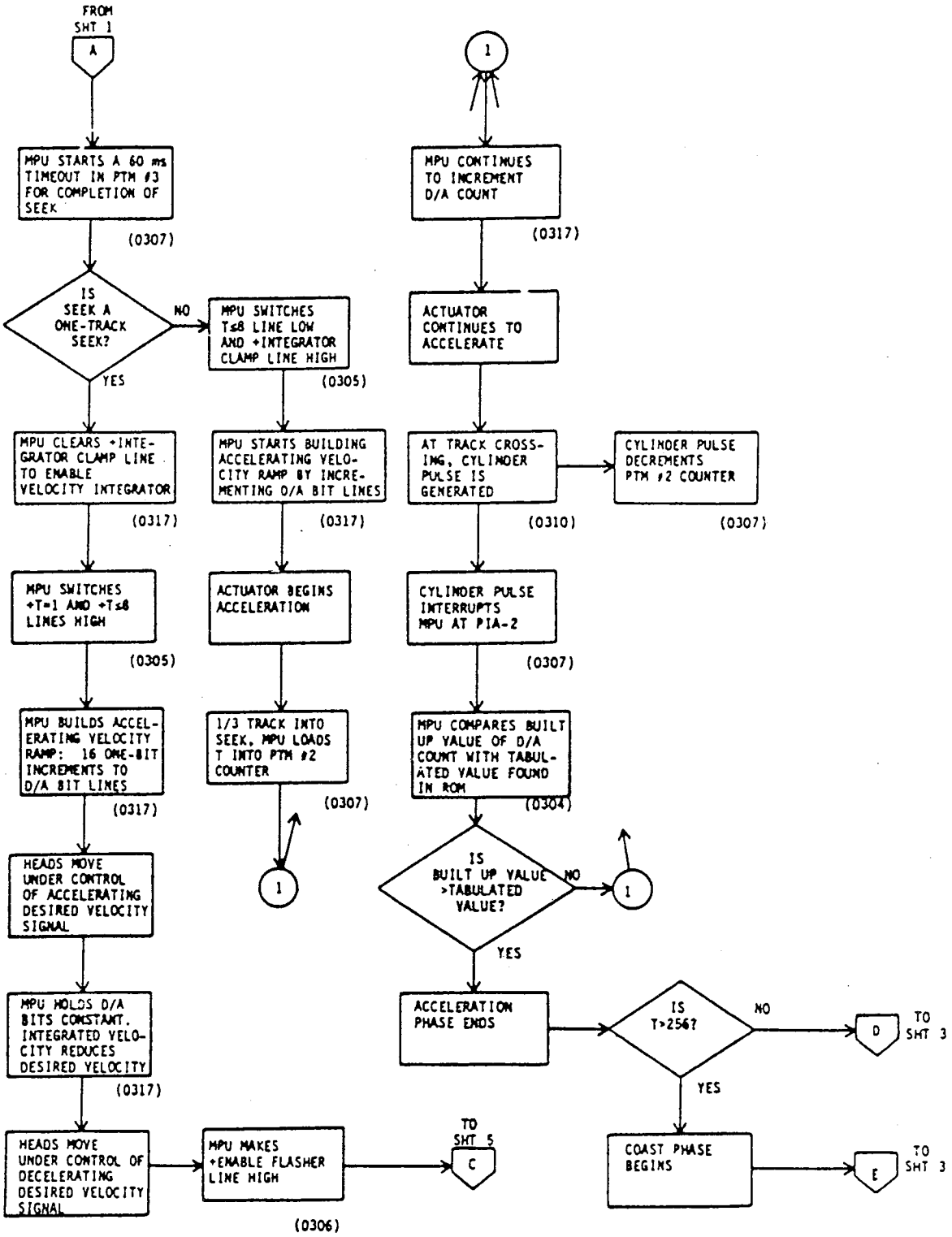
If the seek was successful, the drive will send seek end to the controller.

At the beginning of the seek, the MPU checks the fault signal, the servo signal, and the speed O.K. signal to make sure that it is safe to proceed with the seek operation. At the end of the seek, the MPU checks the servo signal, that no guardband is being detected and that the seek was completed within 60 ms. The 11 ms. timer cannot expire before on-cylinder returns to the active state. If the MPU detects an error in any of the above conditions, it drops all servo commands, stops the actuator, sends seek error to the controller, and waits for a return to zero command from the controller.

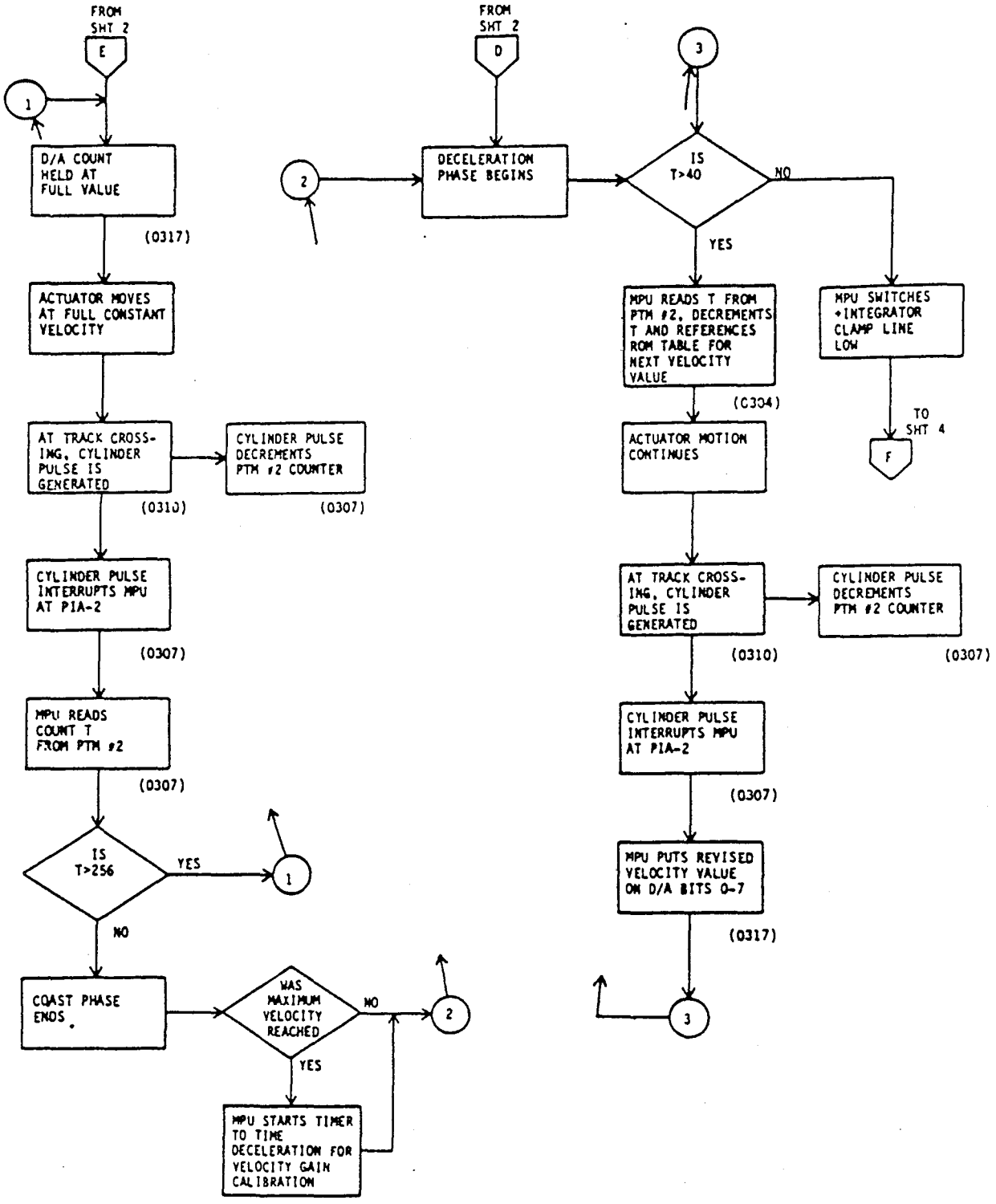
When the actuator reaches the maximum speed for any given seek, the MPU will check the deceleration time and adjust the velocity gain if necessary.



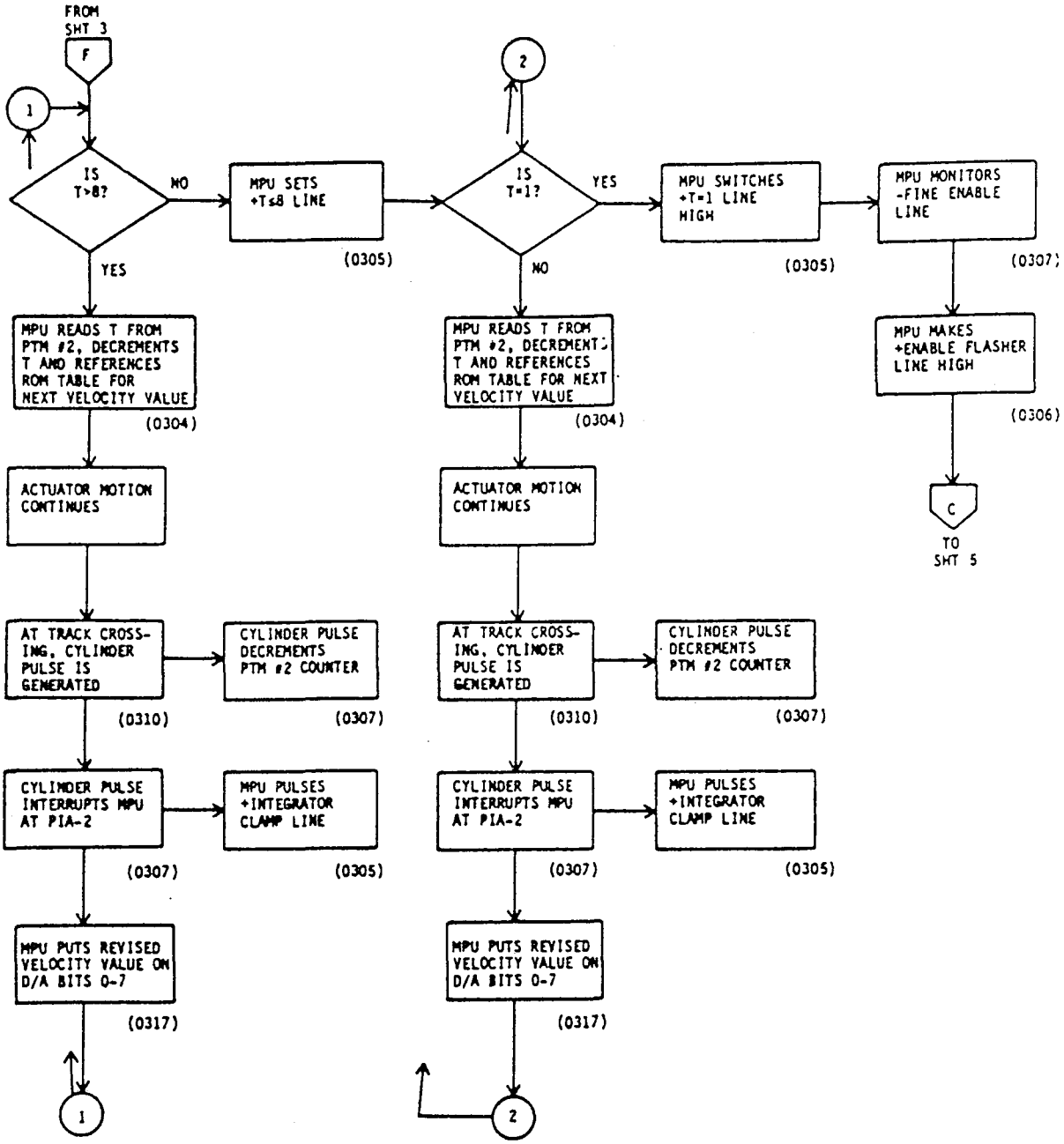
Normal Seek Flowchart (Sheet 1 of 5)



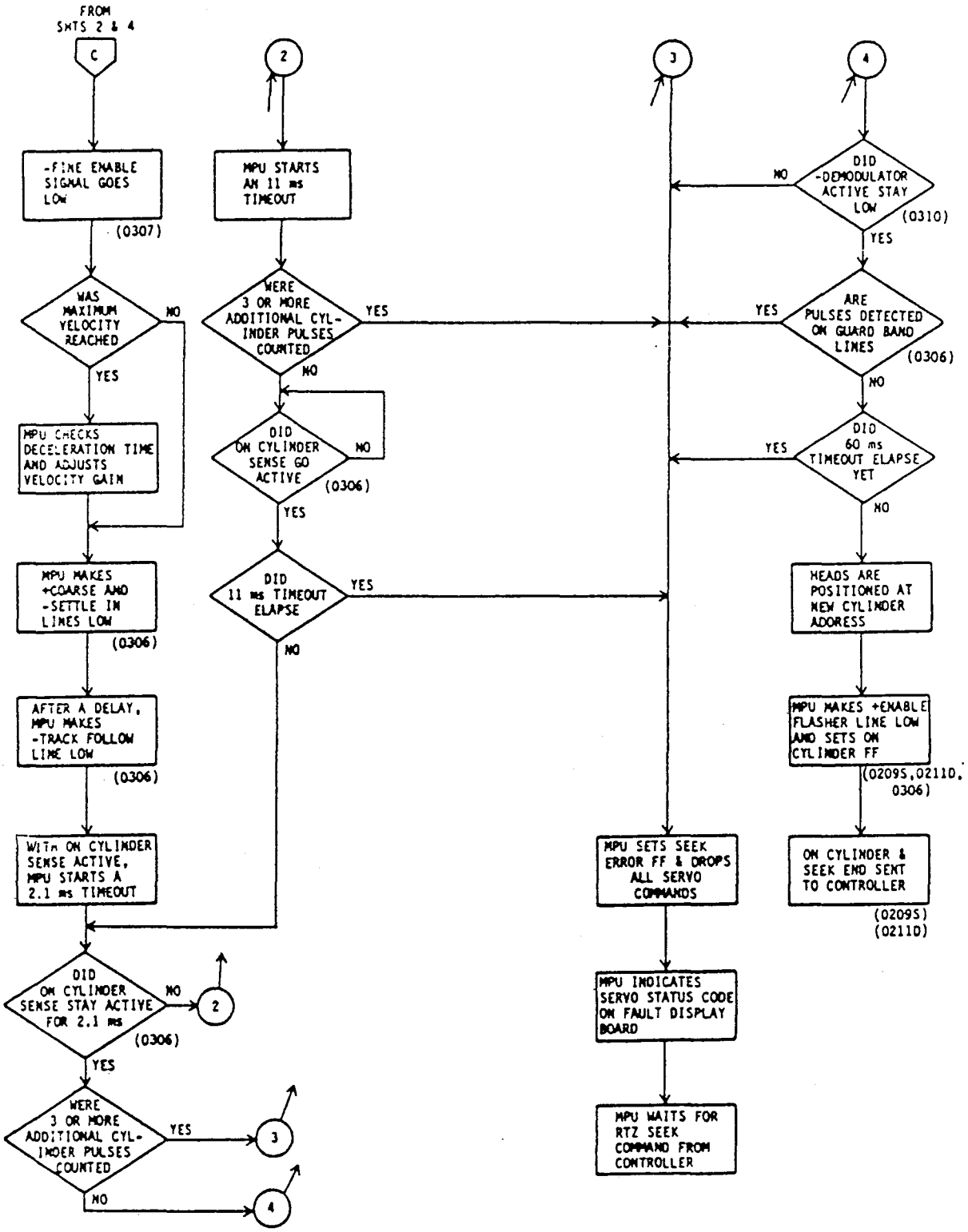
Normal Seek Flowchart (Sheet 2)



Normal Seek Flowchart (Sheet 3)



Normal Seek Flowchart (Sheet 4)



Normal Seek Flowchart (Sheet 5)

RETURN TO ZERO SEEK

During a normal seek operation, if a seek error occurs the only method of clearing it is to issue a return to zero command from the controller. (A seek error does not set the fault signal and therefore cannot be cleared by depressing the fault switch.) To do this the controller sets bit six true on the bus out and sends Tag 3 to the interface board.

When the bus out decode gate array on the interface board decode the return to zero it clears the cylinder register, the head register, on-cylinder FF and the seek error FF, all contained in the bus out gate array. The MPU receives a return to zero interrupt from the bus out gate array.

The return to zero interrupt will cause the MPU to stop the actuator motion and start moving it in an outward direction under coarse control. The acutator continues to move outward until the outer guardband is detected. Once the outer guardband is detected, the MPU checks for two cylinder pulses before reversing the direction of the actuator. The actuator begins to move toward Cylinder 0. The MPU must see at least one cylinder pulse for the outer guardband. There is one additional cylinder pulse detected before the heads reach Cylinder 0. With one third track to go fine control is enabled and course control is disabled.

The MPU checks that on-cylinder stays active for 2.1 ms. If it does not, the MPU will wait for up to 11 ms. for on-cylinder to go active and check it again. When on-cylinder stays active for 2.1 ms., the MPU checks other conditions that would indicate an error occurred before proceeding. These conditions are that there were not three or more cylinder pulses detected after on-cylinder was detected, that the servo signal is present and that no guardband is being detected. The MPU will continue if no error condition is found.

If the return to zero seek was completed in less than 60 ms. the MPU performs a velocity gain calibration. The ready light will be on steady and seek end and drive ready will be sent to the controller. The DD40 is now ready to receive commands from the DC40.

During the return to zero seek the MPU periodically checks condition that will determine if the operation should be continued. The following list shows the conditions that will cause the return to zero operation to be stopped.

-A fault is detected at the beginning of the return to zero.

-The servo signal is not present at the beginning of the return to zero.

-The servo signal is lost after the outer guardband is detected.

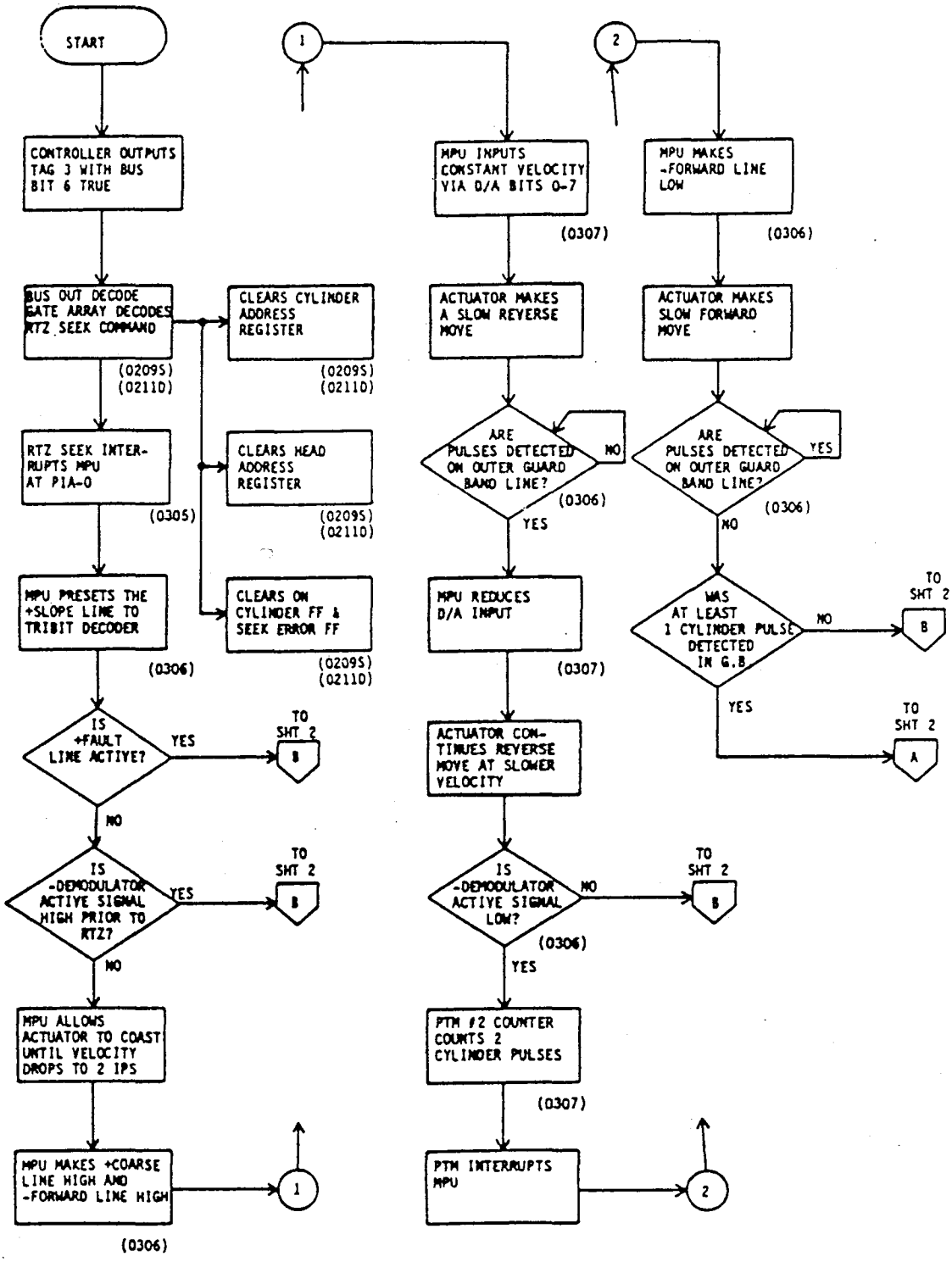
-One or more cylinder pulses from the outer guardband was not detected before Cylinder 0 was found.

-Three or more cylinder pulses are detected after Cylinder 0 has been detected.

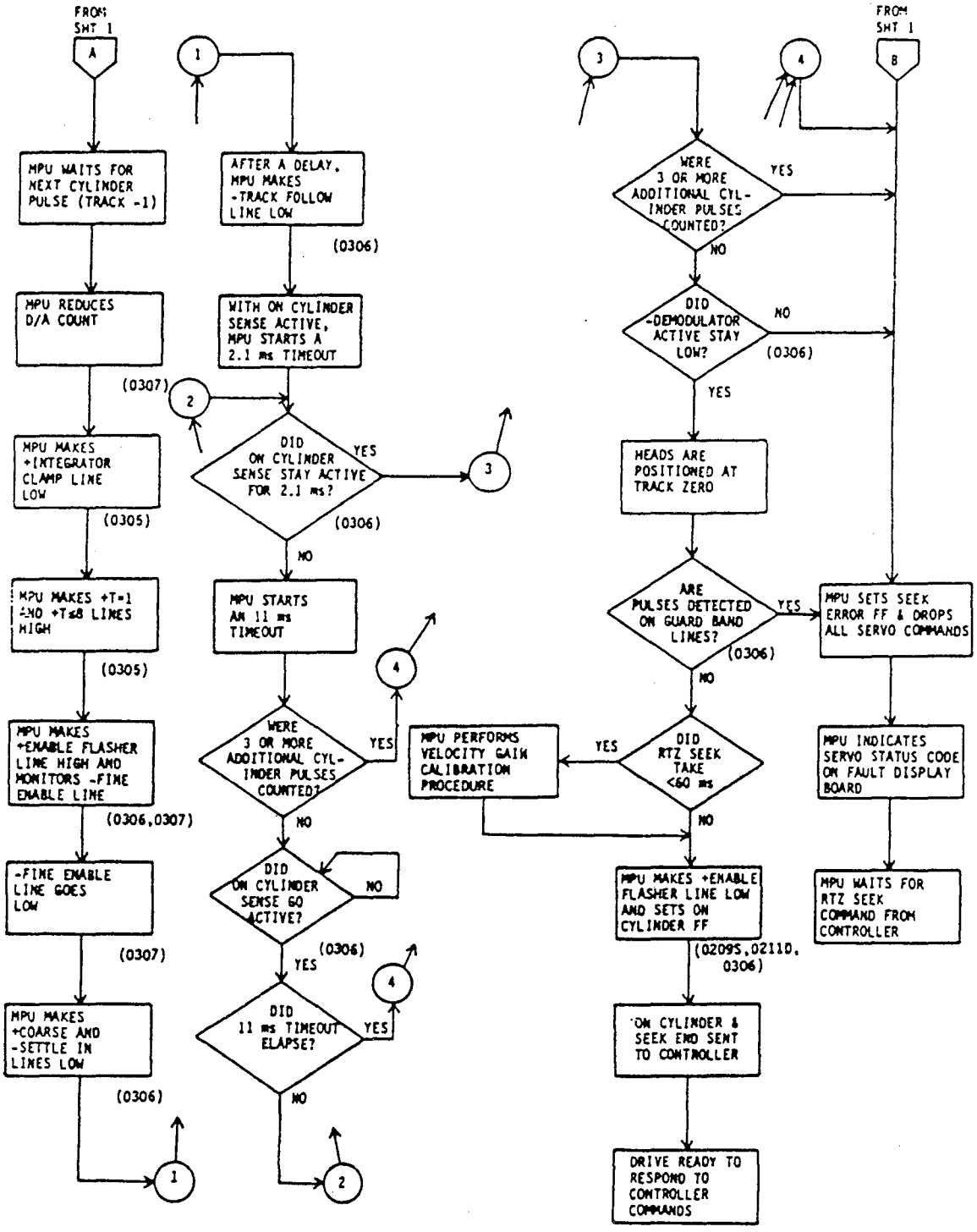
-When Cylinder 0 has been detected and on-cylinder is active, if on-cylinder goes inactive before 2.1 ms. and does not return to the active status in 11 ms.

Any of the above occurances will cause the MPU to set the fault light, flash the ready light, send servo status code to the fault display board and send seek error to the controller. The operating status select can be used by the controller to read the servo status code.

The return to zero flowchart gives a step by step flow of this operation.



Return to Zero (RTZ) Seek (Sheet 1 of 2)



Return to Zero (RTZ) Seek (Sheet 2)

2.6 WRITE CIRCUIT

Figure 2-6 is a block diagram of the write circuit. This circuit has four main parts: the write PLO, the 2 through 7 encoder, write compensation, and arm preamp. The write operation begins when the DC-40 controller sends tag 3 and bus-out bit 0 is true. The NRZ data starts coming from the controller at this time, synchronized by the 24.2 MHz clock. The servo clock is sent to the DC-40 controller and returned to the spindle as the write clock.

The write PLO generates the following:

- 24.2 MHz servo clock, which is sent to the controller by way of the I/O board.
- 12.096 MHz clock used in the read comparator
- 48.8 MHz 2F clock used in the 2 through 7 data encoder. The 2F clock is also used as an input to the frequency dividing circuit.

The 4.032 output from the divider is used for comparison with the 4.032 MHz reference frequency 4.032 MHz). This comparison keeps the 48.4 MHz 2F clock stable.

The encoder gate array changes NRZ data to 2 through 7 data. Table 2-4 shows the relationship between NRZ and 2 through 7 code words.

Table 2-4. Relationship Between NRZ and 2 Through 7 Codes

NRZ Code Words	2 Through 7 Code Words
00	1000
01	0100
100	001000
101	100100
111	000100
1100	00001000
1101	00100100

The NRZ data is broken down into seven NRZ code words. For each NRZ code word, there is a there is a corresponding 2 through 7 code word. The 2 through 7 encoder receives from the I/O board the following signals: write clock, write gate and write data. The encoder chip looks for one of the seven NRZ words. When a word is recognized, the 2 through 7 equivalent word is sent to the write compensate circuit. In the write compensate circuit, 2 through 7 data goes through a pulse shaping circuit, a shift register, and a patten decode. The purpose of this circuit is to compensate for peak shift in the data on the drive. The part of the circuit that compensates for peak shift is divided into two parts. One part is for tracks less than 768 (outer zone tracks) and one part is for tracks greater than 768 (inner zone tracks). The data is sent out on one of the four data lines early, late, normal, or block

R/W CARD

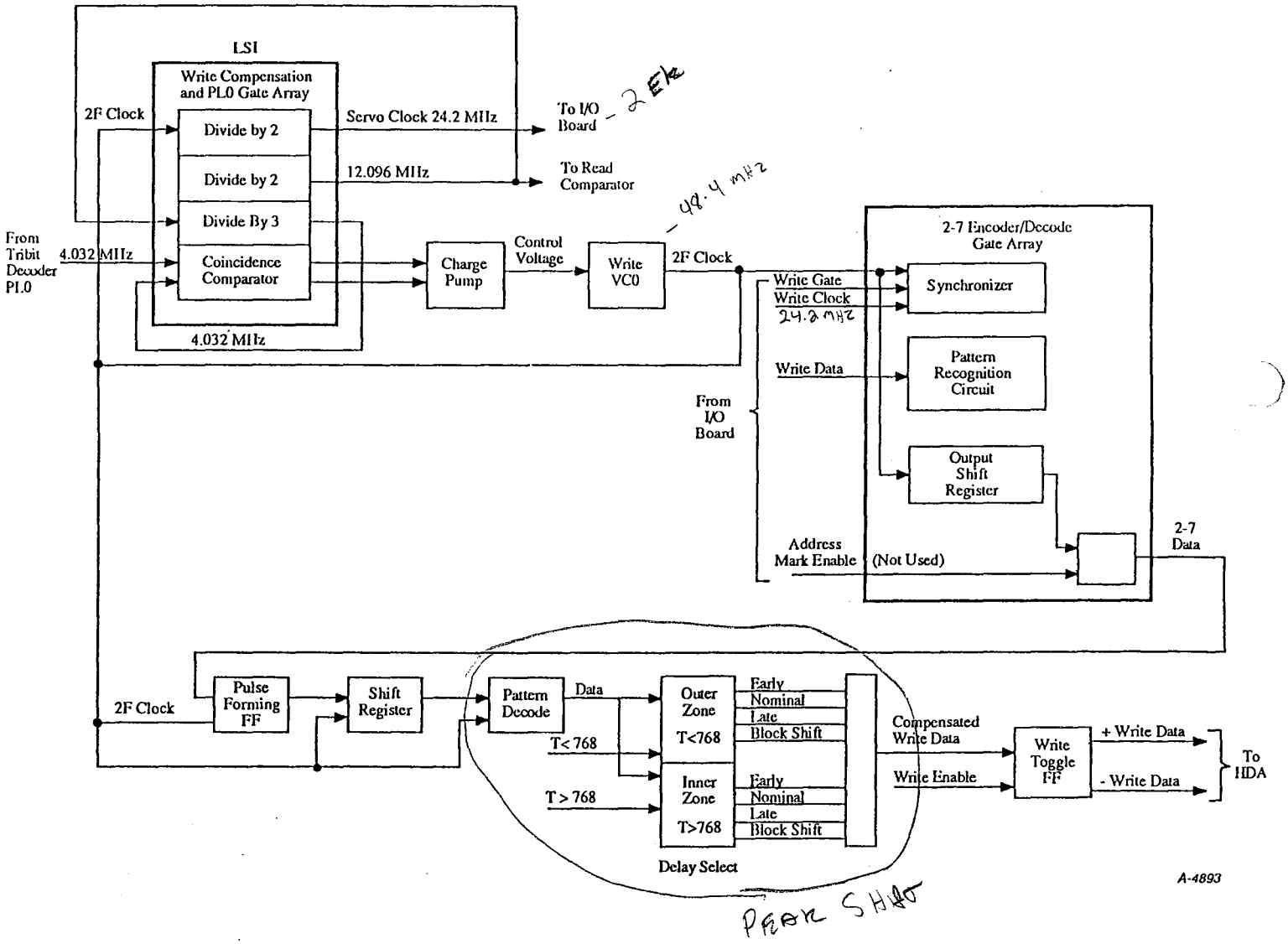


Figure 2-6. Write Circuit Block Diagram

shift. The write enable signal is used as an enable for the write toggle flip-flop (F/F). As a bit arrives on a data input line, the write toggle F/F toggles. If the F/F starts at 0, the first 1 bit sets it, the next clears it, and so on. From the write toggle F/F the data goes to the selected preamp inside the module and to the selected head.

The write enable allows the operation to continue as long as 1) write protect is off, 2) there are no faults, 3) the drive is at the correct speed, 4) the power amp is enables, and 5) the write gate is on.

2.7 READ CIRCUIT

Figure 2-7 is a block diagram of the read circuit. Data is read by the selected head and sent to the read buffer amplifier by way of the preamp. The data is split into low resolution data and high resolution data. Each kind of data is sent through a waveshaping network. When the data is changed from analog to digital data, it enters the data latch chip, which reduces the high frequency noise. From the data latch, the 2 through 7 data is sent to the read comparator and the PLO circuit, where the data is synchronized to the 48.4 MHz clock.

The data is sent to the 2 through 7 decode gate array, which looks for one of the 2 through 7 data words and sends out the corresponding NRZ data word. The NRZ data is synchronized to the 24.2 MHz read clock and sent to the controller by way of the I/O board.

2.8 FAULT AND ERROR CIRCUITS

Figure 2-8 shows the fault and error detection circuitry. There are two kinds of errors: those erros that are indicated by a fault and those that are not. When a fault is indicated, the XMD spindle sends the DC-40 controller fault and write protected. The MPU drops the ready signal and tries to identify the fault. The MPU reads the seven fault latches from the bus-out decode gate array and lights the corresponding LED on the fault display board.

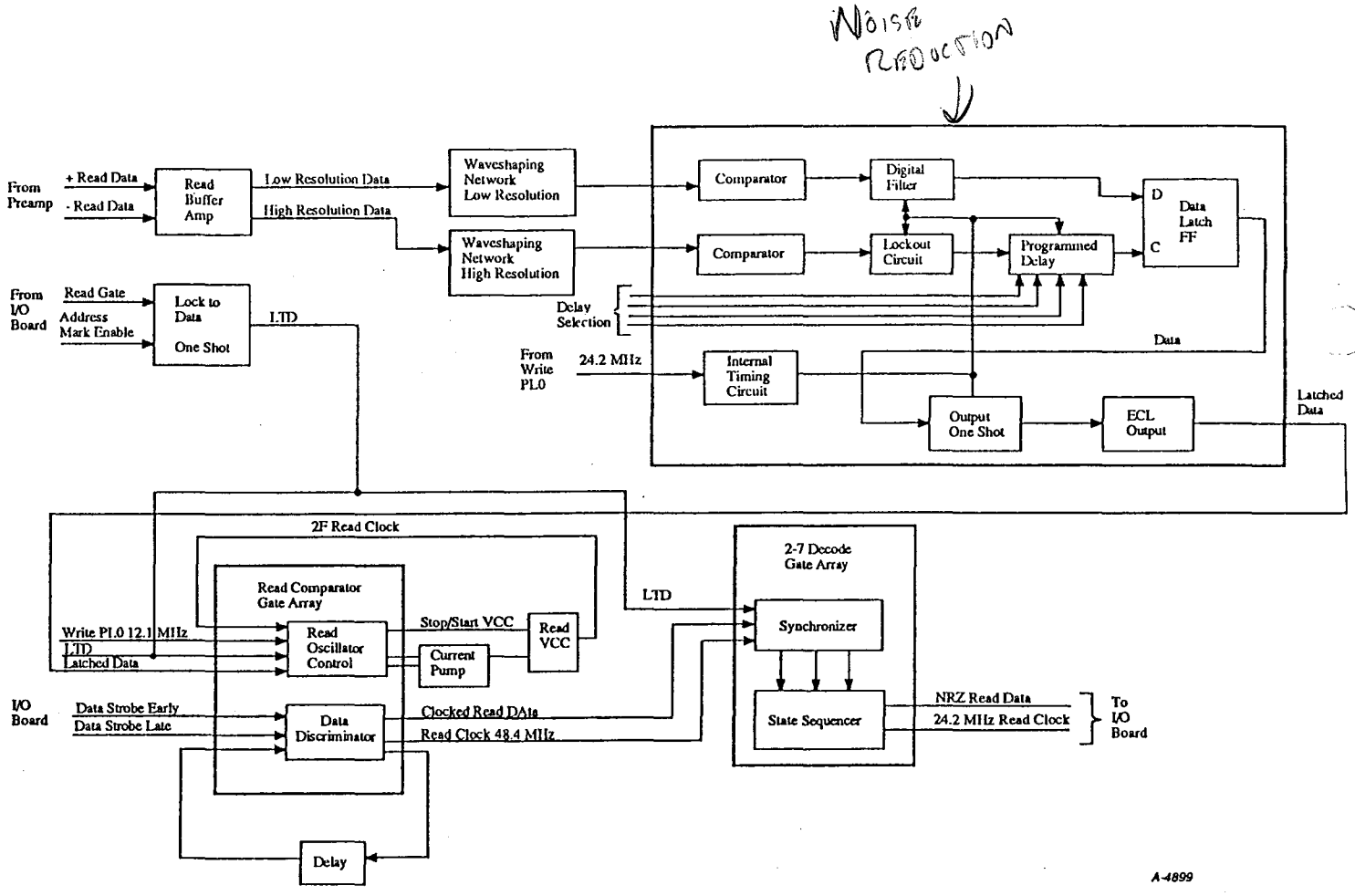


Figure 2-7. Read Circuit Block Diagram

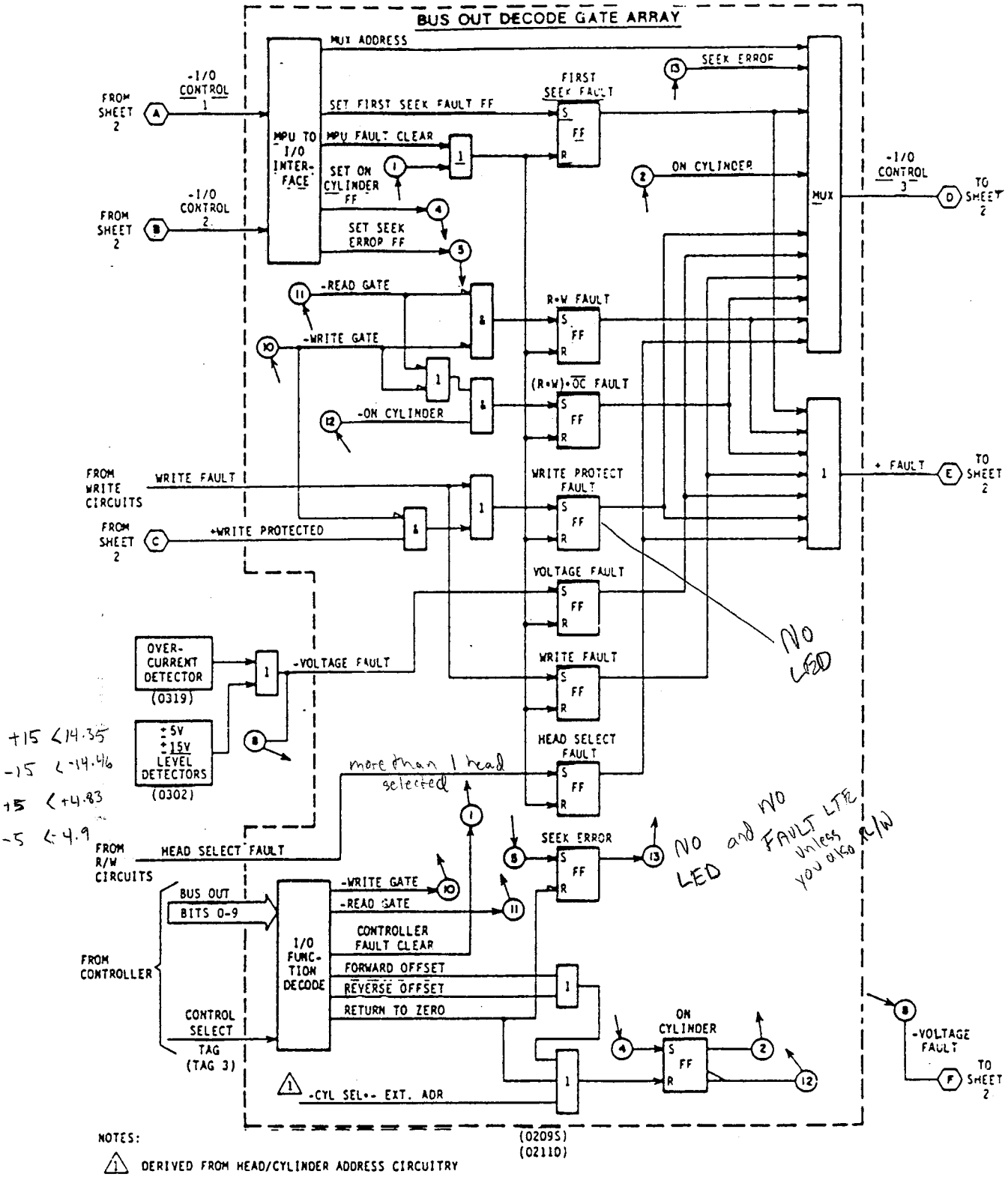


Figure 2-8. Fault and Error Detection Circuitry (page 1 of 2)

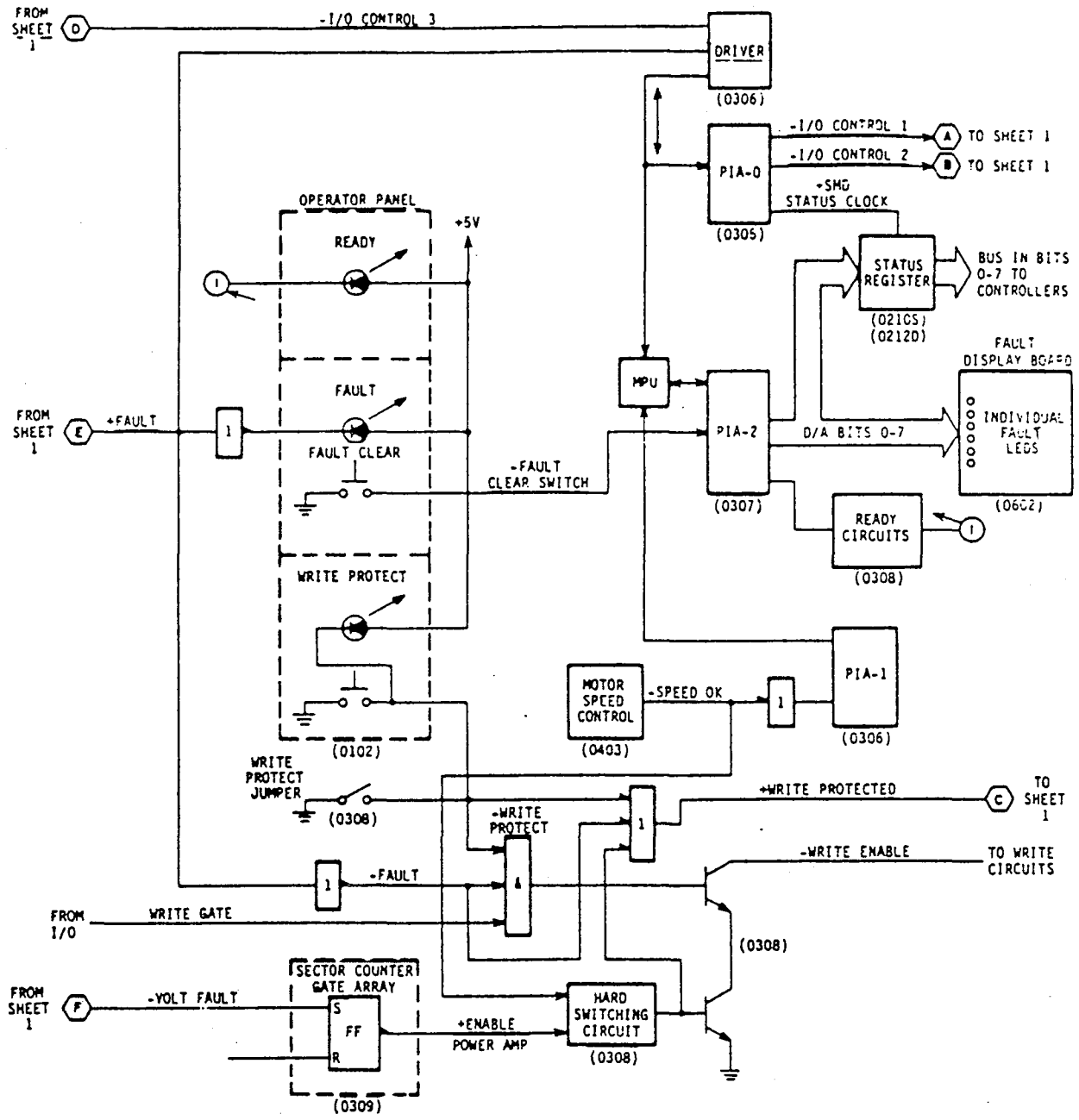


Figure 2-8. Fault and Error Detection Circuitry (page 2 of 2)

The fault light indicates the following faults:

- Voltage fault
- Read or write and off cylinder
- Write fault
- Head select fault
- Read and write fault
- Write and write protected fault*
- First seek fault

  * This signal does not have a corresponding LED on the fault display board.

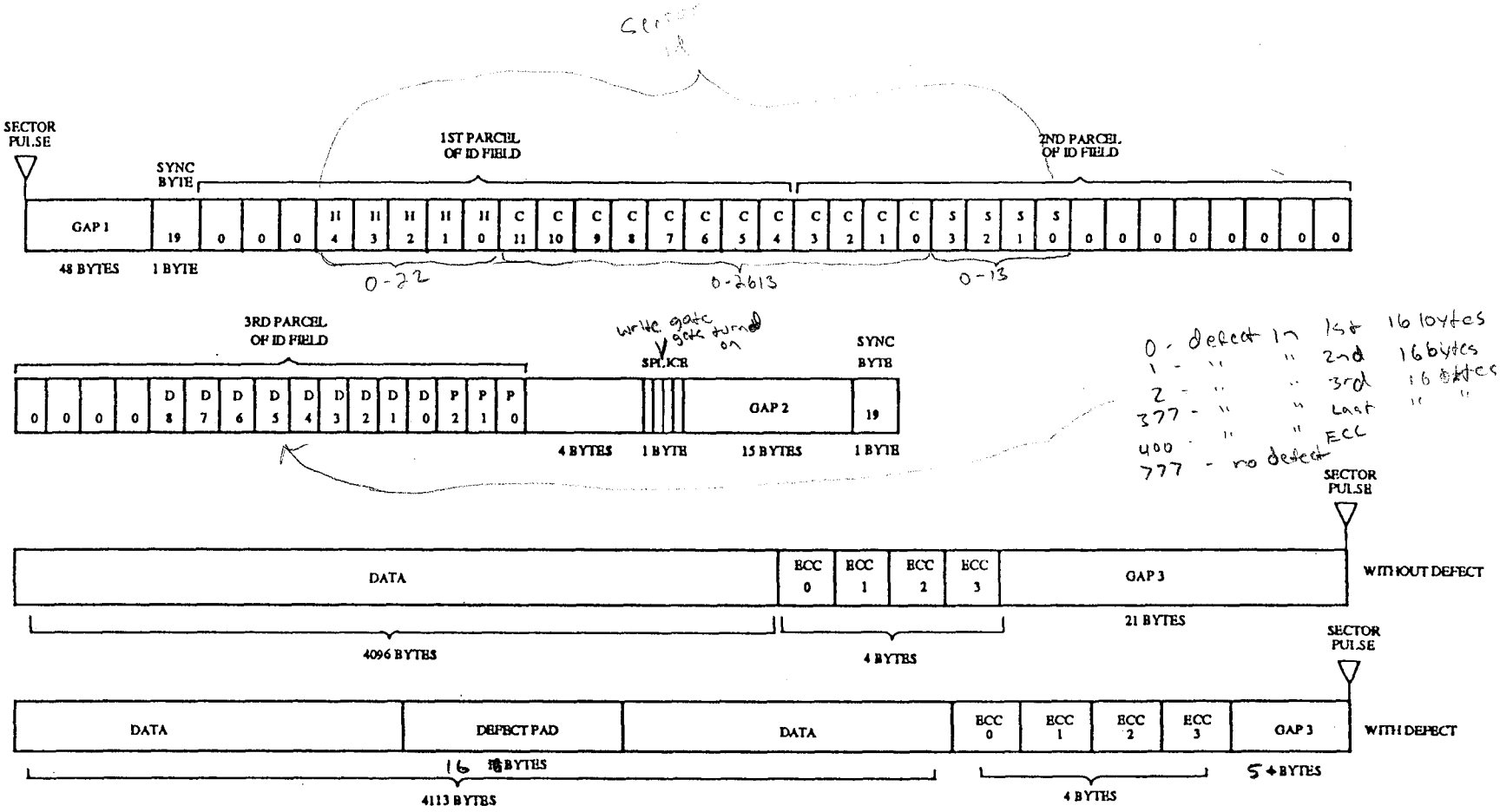
There are two error conditions that do not cause a fault: motor speed error (less than 2100 RPM) and seek error (cleared by RTZ).

For more information on the fault signals and errors, see pages 1-142 through 1-150 in Control Data manual 83325100.

DD40 SECTOR FORMAT

Each track in the 3340 is divided into 48 sectors, twelve sectors on each of the four spindles. The following figure shows the format of one sector. The length of one sector is 4198 bytes or 1866 servo bytes. The sector I.D. is six bytes in length. The first three bytes contain the actual I.D. of head, cylinder and sector. These three bytes are used on the 2EJ to detect when the correct sector is under the heads. The fourth byte is all zeros. The last two bytes contain the defect parameter which is protected by three bits of parity. The defect parameter is used on the 2EK to point to where within the data field the defect appears. When the head reaches the defect in the data field, the defect parameter is used to disable the read or write logic until the 17 byte defect pad has passed under the data head.

The bottom half of the diagram shows a data field without a defect and one with a defect. Notice that the last gap (Gap 3) is 17 bytes shorter when there is a defect than when there is no defect. The same amount of data is written in the data field and the sector has the same number of total bytes whether or not there is a defect. The data field is followed by four bytes of Error Correction Code (ECC) which is generated by the 2EK on the data field. Gap 3 is normally 21 bytes if there is no defect present in the data field or 4 bytes if a defect exists in the data field. There are two sync bytes in each sector, one prior to the I.D. and the other prior to the data field.



A-4427

H0-4 = Head 1-19 decimal, 0-22 Octal

C0-11 = Cylinder 0-1420 decimal, 0-2614 Octal

S0-3 = Sector 1-12 decimal, 0-13 Octal

D0-8 = Defect parameter If there is no defect in the sector, the parameter equals all 1's

P0-2 = Defect Parity Bits

XMD SECTOR FORMAT

Unhiddable flaw
1) id field = all one's
2) flaw entry defect parameter = 7777

cyl 2612 User Flaw table

unhiddable flaws ->

hidable flaws

7777 — —
— 7777 — —
7777 — — 7777
— — 7777 —

3. CABLING

Figure 3-1 shows the cable connections between a DCU-5 in the IOS and a DC-40. Each controller in the DC-40 is connected to a DCU-5 by a bus-in and bus-out cable. Two DCU-5's can be connected to each controller (one through the A port and one through the B port). One DCU-5 can access a controller at a time.

The cable between the DCU-5 and the DC-40 is normally 50 ft long, but it can be up to 80 ft long.

Figure 3-2 shows the DD-40 drive configuration and bulkhead cable ports. Figure 3-3 shows the cable connections of a DC-40 controller to primary and shadow DD-40's.

Each controller can be cabled to a primary and a shadow DD-40. A controller has eight cables, four A cables and four B cables. The four A cables are connected to four IN ports, one for each drive, in the primary DD-40. If there is a shadow DD-40 on the controller, A cables are connected from OUT ports on the primary DD-40 to IN ports on the shadow DD-40.

Two B cables are connected from the controller to the primary DD-40 and two to the shadow DD-40. Each B cable contains identical sets of signals. One B cable contains the signals for spindles A and B and the other contains the signals for spindles C and D. Each B cable separates into two cables, one for each spindle, when it goes from the bulkhead to the back of the DD-40. Unlike the A cables, the B cables are not daisy-chained from the primary to the shadow DD-40. Separate B cables carry the B cable signals from the DC-40 to the shadow DD-40.

The A and B cables are connected from the bulkhead to the back of the spindles. The cables that make this connection are 10 in. longer for a given spindle than for the spindle below it. If a shadow DD-40 is not connected to the controller, a terminator on the primary DD-40 terminates the A cable signals. If a shadow DD-40 is connected, A cables take the signals from the spindles to the OUT ports on the bulkhead, from which they can be linked to the shadow DD-40. The A cables are terminated on the shadow DD-40.

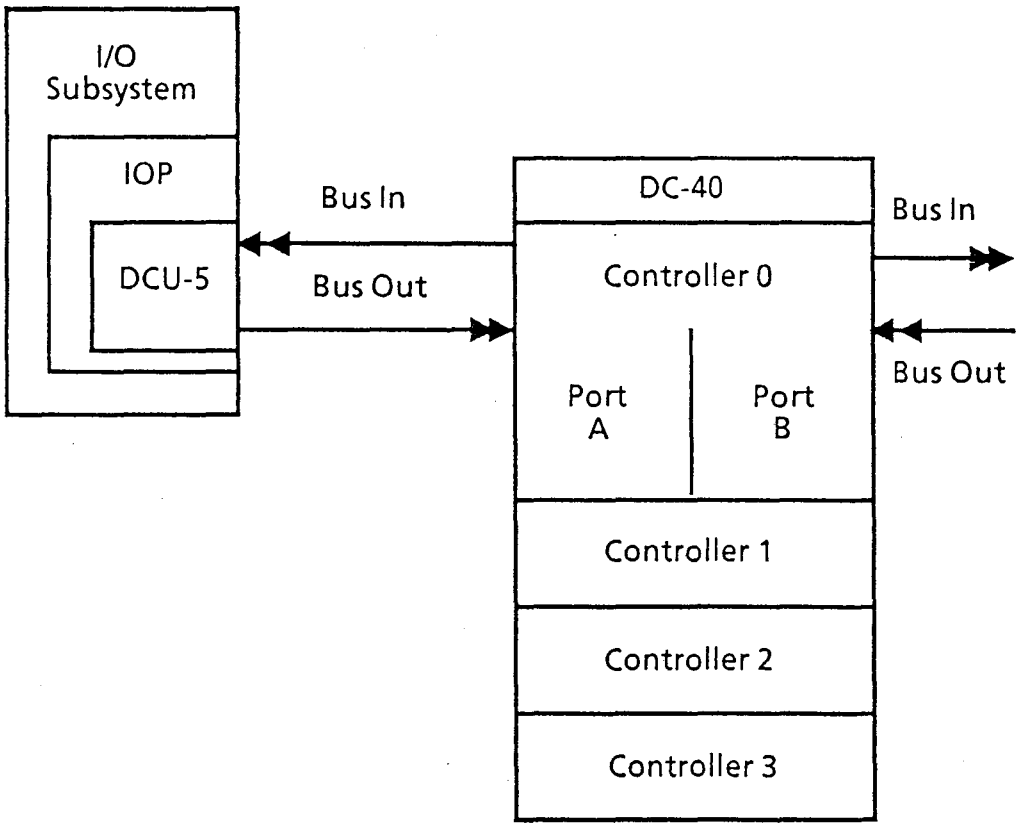


Figure 3-1. DC-40 to IOS Communication

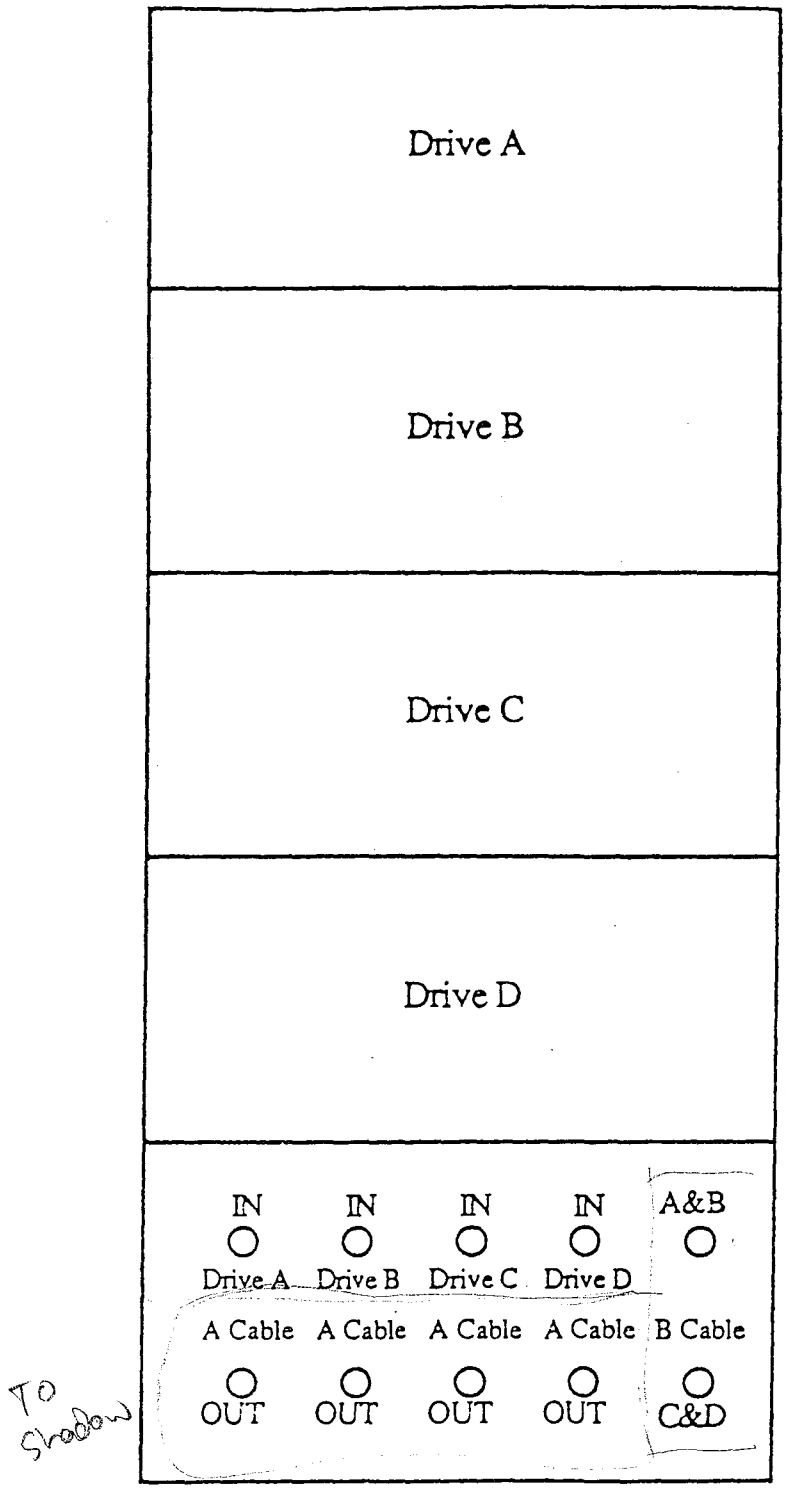


Figure 3-2. DD-40 Drive Configuration and Bulkhead

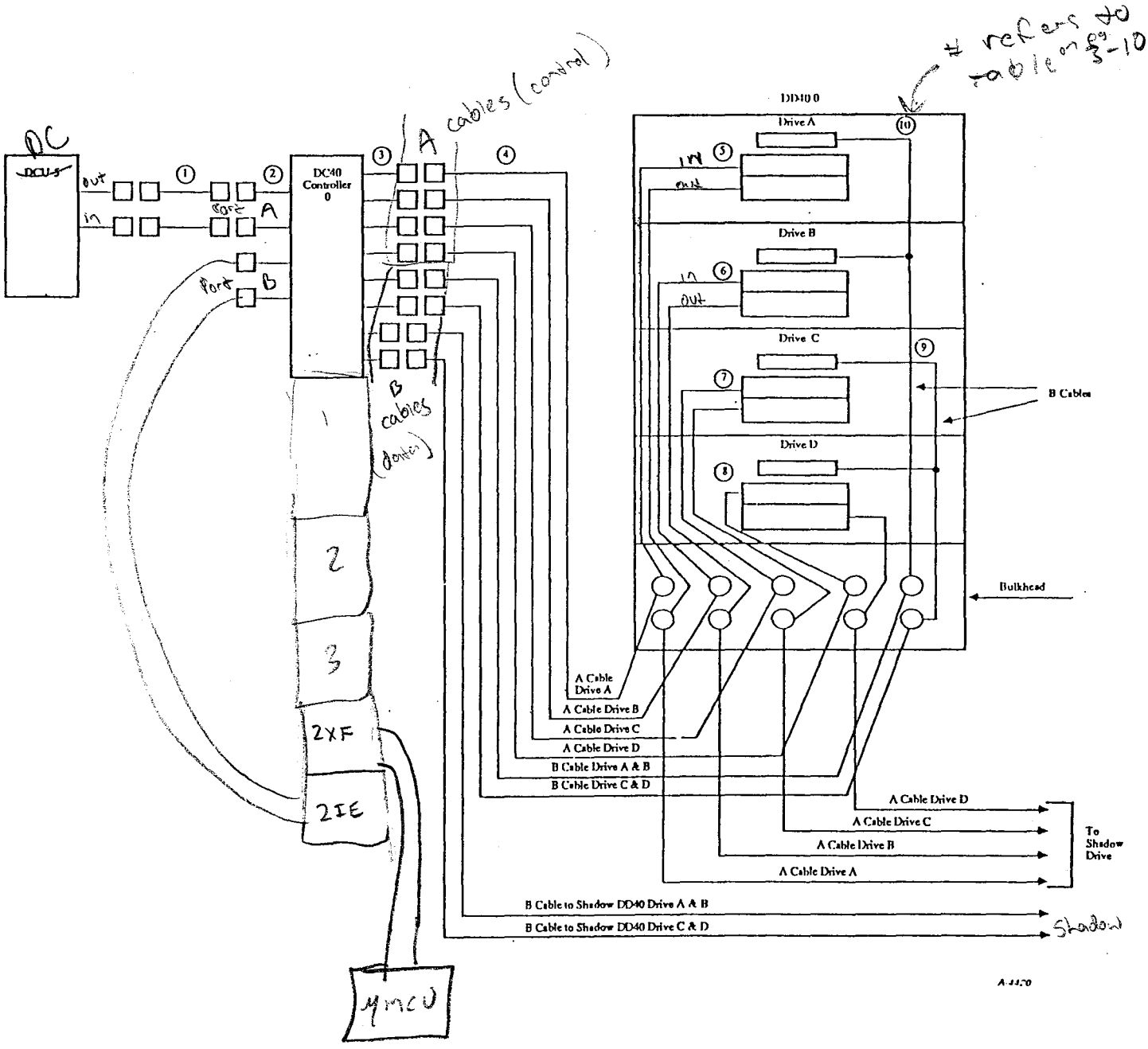


Figure 3-3. DC-40/DD-40 Cabling Diagram

Table 3-1 lists the pin assignments for the A cable that connects the DC-40 controllers to the primary and shadow DD-40s. Table 3-2 describes the A cable signals.

Table 3-1. A Cable Pin Assignments

Signal Name	Inverted Pin	Normal Pin
Unit select Tag	22	52
Unit select 1 (Bit 0)	23	53
Unit select 2 (Bit 1)	24	54
Unit select 3 (Bit 2)	26	56
Tag 1	1	31
Tag 2	2	32
Tag 3	3	33
Tag 4	30	60
Tag 5	27	57
Bus 0	4	34
Bus 1	5	35
Bus 2	6	36
Bus 3	7	37
Bus 4	8	38
Bus 5	9	39
Bus 6	10	40
Bus 7	11	41
Bus 8	12	42
Bus 9	13	43
Status 0	19	49
Status 1	17	47
Status 2	16	46
Status 3	15	45
Status 4	28	58
Status 5	20	50
Status 6	18	48
Status 7	25	55
Open cable detect	14	44
Busy	21	51
Spindle sequence pick		29
Spindle sequence hold		59

Table 3-2. XMD A Cable Signals

Signal	Description
Unit select tag	This signal is sent to the drive along with unit select bits 0 through 2 to select the desired unit.
Unit select bits 0 through 2	These signals must be active at least 200 ns before the unit select tag becomes active. Only unit select bit 0 is used by the DC-40 to select either the primary (2^0 = 0) or shadow (2^0 = 1) DD-40. (Unit select bit 3 is used on tag 5.)
Tag 1	Lower cylinder select, bits 2^0 through 2^9. (When doing a cylinder select, the higher bits must be sent first.)
Tag 2	Head select/higher cylinder bits. Head select bits are represented in bus-out bits 2^0 through 2^4. The upper cylinder bits (2^{10} and 2^{11}) are represented by bus-out bits 2^7 and 2^8. (The upper cylinder bits must be sent before the lower cylinder bits.)
Tag 3	Enable the control bits to be sent out on the bus. When the bus-out bit is active, it controls the following in the XMD: • 2^0 - Write gate • 2^1 - Read gate • 2^2 - Offset - offsets positioner toward the spindle. • 2^3 - Offset - offsets positioner away from the spindle. • 2^4 - Clear fault • 2^5 - Not used • 2^6 - RTZ • 2^7 - Data strobe early • 2^8 - Data strobe late • 2^9 - Not used
Tags 4 and 5	Selected status

Table 3-2. XMD A Cable Signals (continued)

Signal	Description
(See the trouble shooting section for a description of the individual status words.)	Tag 4 - Sector status Tag 5 - Extended status B0B0 = 0 B0B1 = 0 Tag 5 - Operating status B0B0 = 1 B0B1 = 0
Tags 4 and 5	Selected status Tag 5 - Diagnostic status B0B0 = 0 B0B1 = 1 Tag 5 - Diagnostic execute status B0B0 = 1 B0B1 = 1
Open cable detect	Disables the DD-40 when a loss of power in the DC-40 occurs.
Pick	DC-40 ground
Hold	DC-40 ground
Bus-in bits 0-7	Drive status or selected status

Table 3-3 lists the pin assignments for the B cable that connects the DC-40 controllers to the primary and shadow DD-40s. Table 3-4 describes the B cable signals.

Table 3-3. B Cable Pin Assignments

Signal Name	Inverted Pin	Normal Pin
Ground	A	B
Servo Clock 24.2 mHz	b	c
Read Data	a	V
Ground	D	E
Read Clock 24.2 mHz	d	e

Table 3-3. B Cable Pin Assignments (continued)

Signal Name	Inverted Pin	Normal Pin
Write Clock	w	x
Ground	F	G
Write Data	f	g
Unit Selected	J	H
Seek End	h	i
Ground	y	z
Index	JJ	KK
Sector	GG	HH
Ground	NN	PP
Ground	AA	BB
Ground	MM	LL
Servo Clock	DD	CC
Read Data	FF	EE
Ground	j	k
Read Clock	K	L
Write Clock	m	n
Ground	N	P
Write Data	p	q
Unit Selected	S	R
Seek End	r	s
Ground	T	U
Index	t	u
Sector	V	W
Ground	C	X
Ground	Y	Z

The B cable signal for spindles A and B share one 55-pin cable between the DC-40 and the DD-40. The B cable signals for spindles C and D are shared by another cable.

Table 3-4. XMD B Cable Signals

Signal	Description
Write data	NRZ data to XMD

Table 3-4. XMD B Cable Signals (continued)

Signal	Description
Write clock	Clocks write data into the drive (24 MHz/41.3 ns)
Servo clock	Used by the DC-40 to synchronize the transfer of write data to the servo clock (24.192 MHz/41.3 ns)
Read data	NRZ data from XMD
Read clock	24 MHz/41.3 ns
Seek end	Seek end with on-cylinder indicates the seek was completed as expected. Seek end without on-cylinder indicates a seek error. When a diagnostic execute status is performed, seek end indicates test execution is complete.
Unit selected	This is the response to a unit select tag and a match between the unit select bits and drive address.
Index	Decoded from servo tracks once per revolution.
Sector	Twelve sector pulses per revolution. This is determined by the setting on the sector switches.

Table 3-5 gives the part numbers of the drop and interconnect cables for the DCU-5, DC-40, and DD-40. The reference numbers correspond to the numbers on Figure 3-3.

Table 3-5. Part Numbers of the Drop Cables and Interconnect Cables

Cable	Number
DC-40 to DCU-5 Interconnect Cables	① Cable PN 10559201 Socket PN 01106500 Plug PN 01106600
DC-40 Drop Cables (to DCU-5)	② Bus In Cable PN 02203500 Bus Out Cable PN 02203501 55 Pin Socket PN 01106500 55 Pin Plug PN 01106600
DC-40 Drop Cables (to DD-40)	③ A and B Cables PN 12021000 61 Pin Plug PN 01110400
DD-40 to DC-40 and DD-40 to DD-40 Interconnect Cables	④ A and B Cables PN 01110500
DD-40 Bulkhead to Disk Drive Cables	⑧ A Cable - 70" - PN 12019700 ⑦ - 80" - PN 12019701 ⑥ - 90" - PN 12019702 ⑤ -100" - PN 12019703 ⑨ B Cable - 70/80" - PN 12019800 ⑩ -90/100" - PN 12019801
A and B Cable 61-Pin Bulkhead Connector	PN 01234600
A Cable 60-Pin Flat-Cable-Type Connector	PN 01311300
B Cable 26-Pin Flat-Cable-Type Connector	PN 01311200

4. THEORY OF OPERATIONS

This section is a theory of operations for the modules of the DC-40. The DC-40 has the following modules:

- 2EI channel interface module - receives data from the DCU-5 on a write and passes data to the DCU-5 on a read.
- 2EB full-track buffer module - buffers read and write data.
- 2EM disk multiplexer module - provides control for reads and writes.
- 2EJ disk controller module - controls an XMD spindle in the DD-40.
- 2EK disk-data and error-correction module - performs error correction and defect detection on data read from the disk.

A DC-40 has four controllers. Each controller has four 2EJ modules and one of each of the other modules. A controller can control one primary and one shadow DD-40, each of which has four XMD spindles.

The DC-40 adapts the signals and protocol of the DCU-5 to the spindles in the DD-40. The DC-40 performs the following functions:

- Controls up to 32 DD-40s.
- Buffers read and write data transfers between the DCU-5 and the DD-40s.
- Passes control functions to the selected spindles.
- Generates error-correction codes for write data.
- Checks read-correction codes and and computes a correction vector for correcting read data.
- Controls the distribution of read/write data over 48 sectors per cylinder using 12 sectors from each of the four spindles.
- Passes status from the spindles to the DCU-5.

Figure 4-1 is a chassis map of the DC-40. Figure 4-2 is a block diagram of the DC-40.

4.1 2EI MODULE

The 2EI module (see figure 4-3) receives write data from the DCU-5 and sends it to the 2EB module's full-track buffer. The 2EI module also receives read data from the full track buffer and sends it to the DCU-5. There are two ports on the 2EI module, so that data can be received from or sent to different locations on each port. Port A or B must be selected before data can be sent through the port. The port is selected with either a select the port function (010007) or a select the DD-40 drive function. A 010001 select code specifies the shadow DD-40 and a 010000 select code specifies the primary DD-40.

4.1.1 2EI MODULE - FUNCTION DECODE

When the DC-40/DD-40 receives a function code from the DCU-5, a 4-bit function code is latched into the F terms and a corresponding 16-bit function parameter is latched into the A terms. (Port A or B must be selected.) The same clock is used to clock in the function code, the function parameter, and data when doing a write. Once the function code and function parameter are latched, the function code is sent to the function decode. At the same time, the function code and function parameter go to the parity checking circuit.

The following three conditions block the go function (term QO) from going to the 2EM module: command error (term B12), parity error (term F41), and diagnostic mode (term F30). Two clock periods (CPs) pass after the function is latched before go function (term R48) and the function code (terms R49 through R52) are sent to the 2EM module. They are followed by the function parameter in the next 4 CPs, 4 bits each CP.

4.1.2 2EI MODULE - WRITE

When data is received from the DCU-5, it passes through the U terms and is latched in terms A20 through A36 for port A or terms A40 through A56 for port B (terms A36 and A56 are parity bits.) The data and the parity bit are sent to the parity checking circuit. If a parity error is detected on a data transfer, it is flagged in the general status. From the A terms, the data enters terms A0 through A15 and is latched in the M terms. Terms M0 through M15 receive the even parcels and terms M20 through M35 receive the odd parcels. The odd parcels go to bank A and the even parcels go to bank B on the 2EB module.

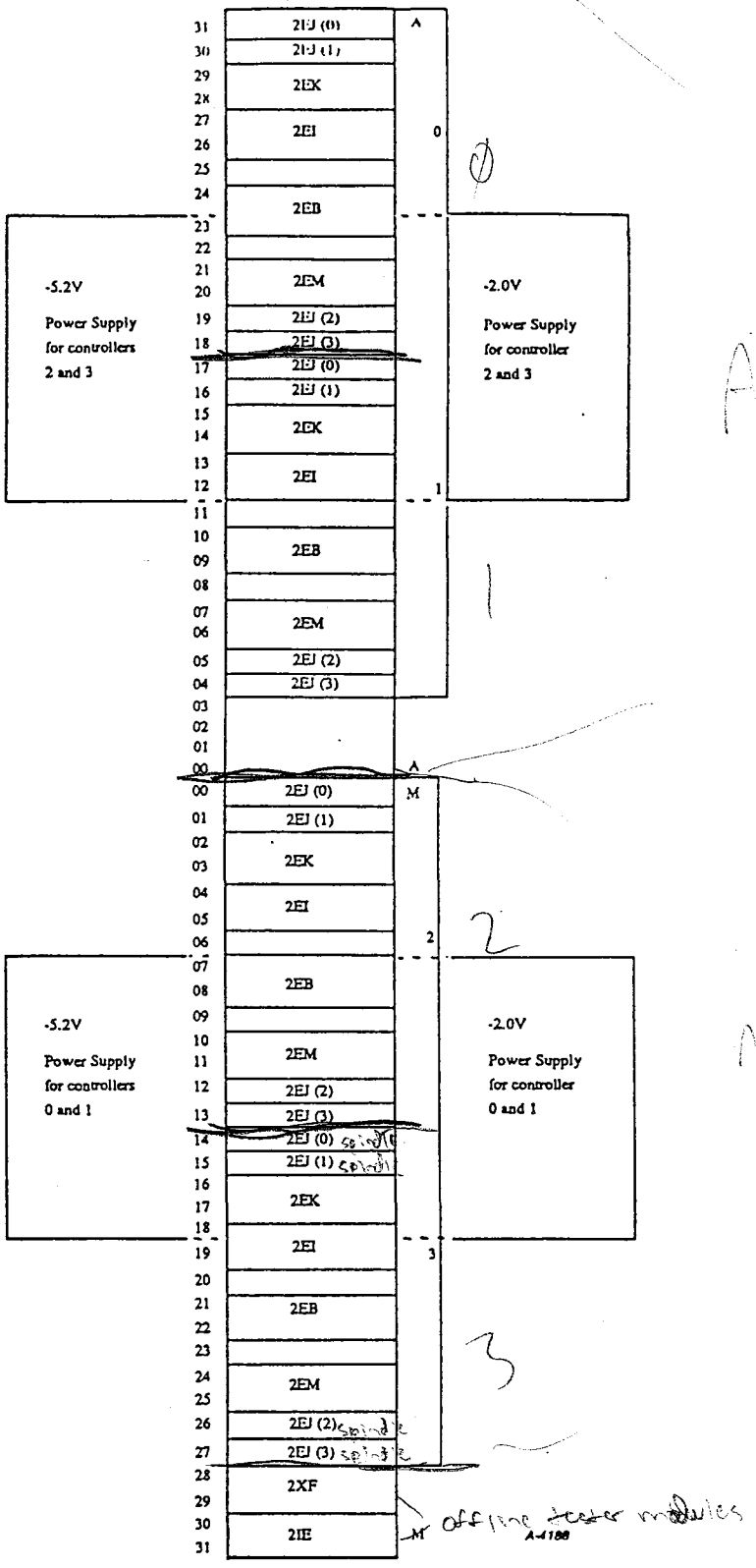


Figure 4-1. DC-40 Chassis Map

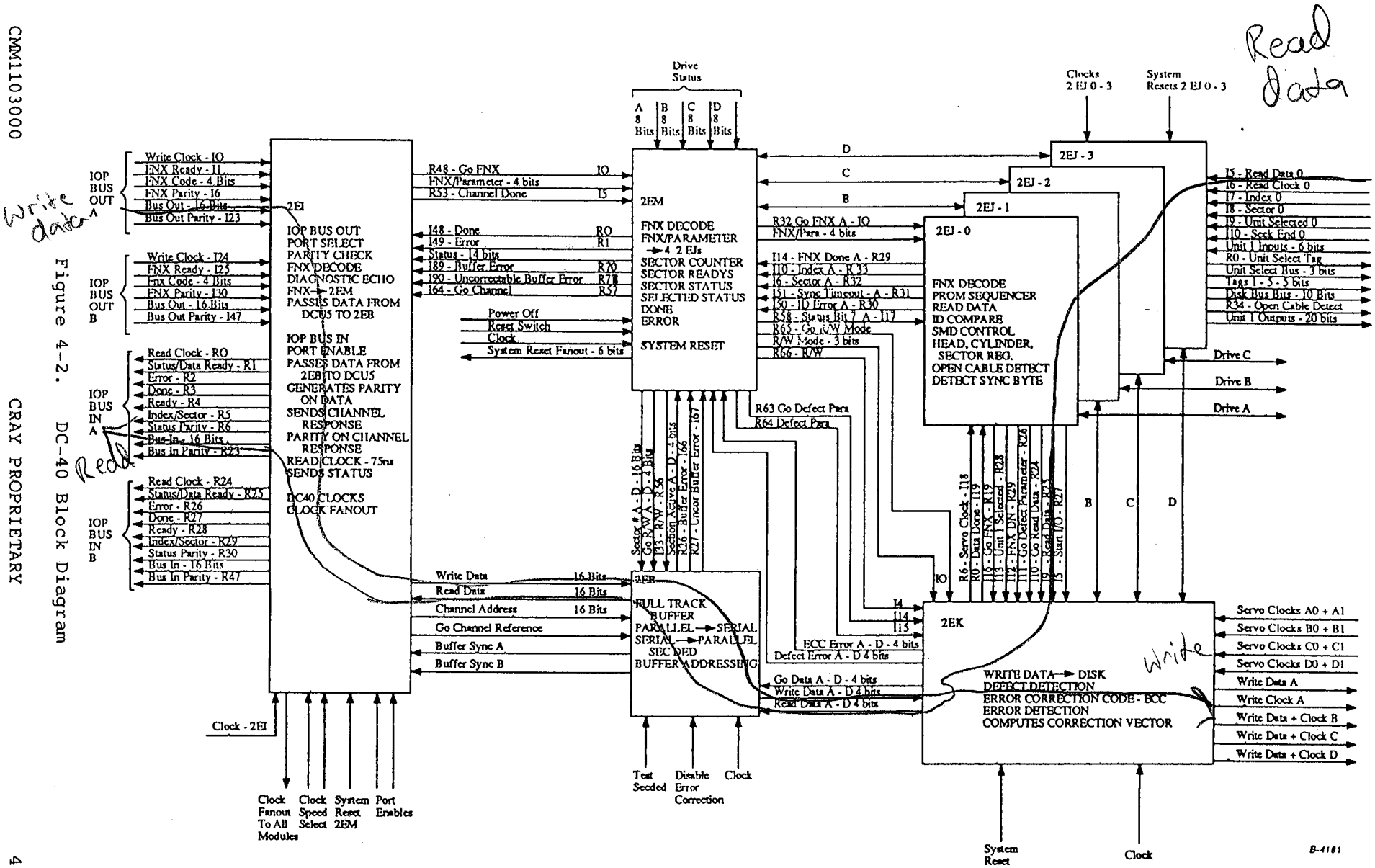
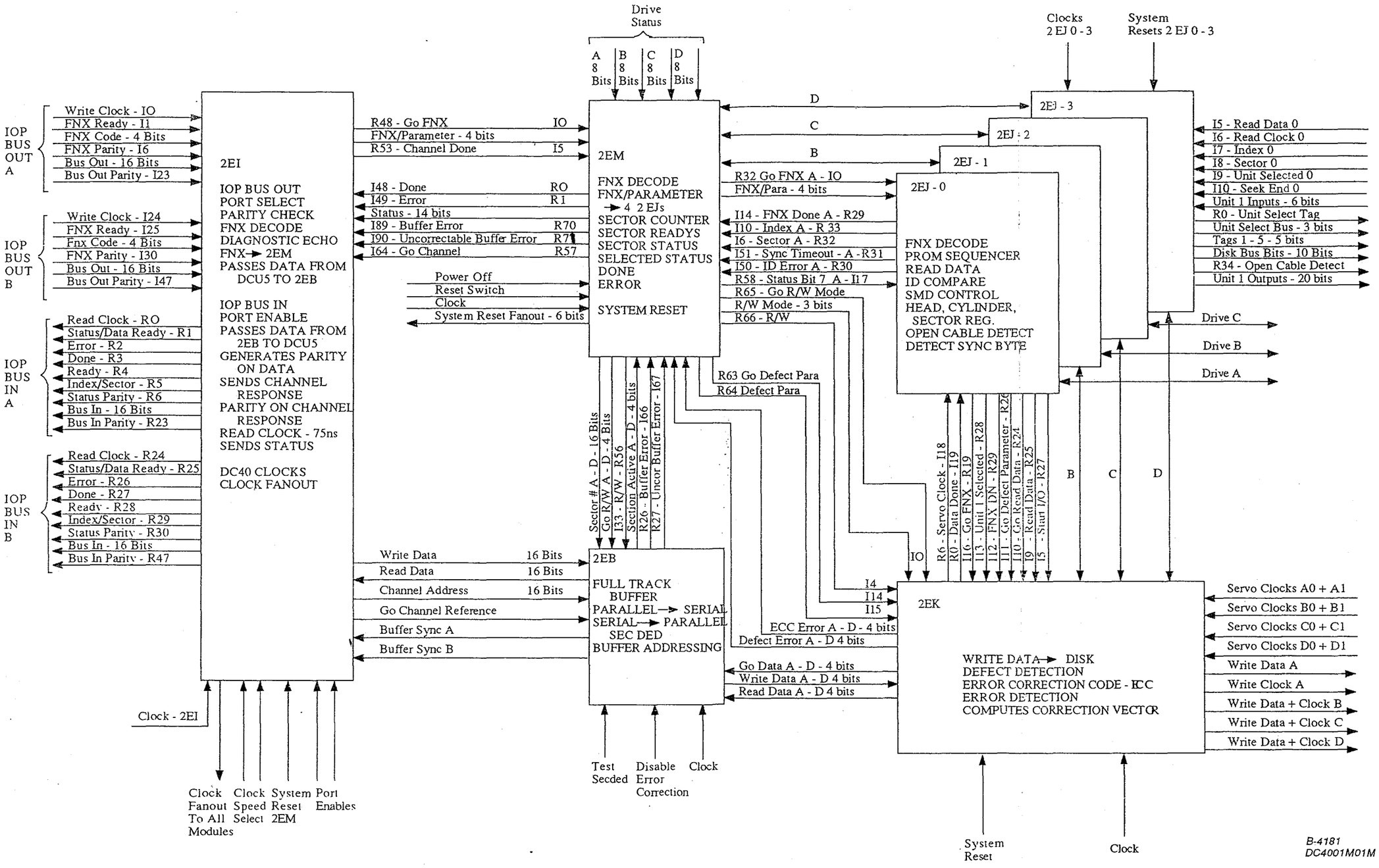


Figure 4-2. DC-40 Block Diagram



DC-40 BLOCK DIAGRAM

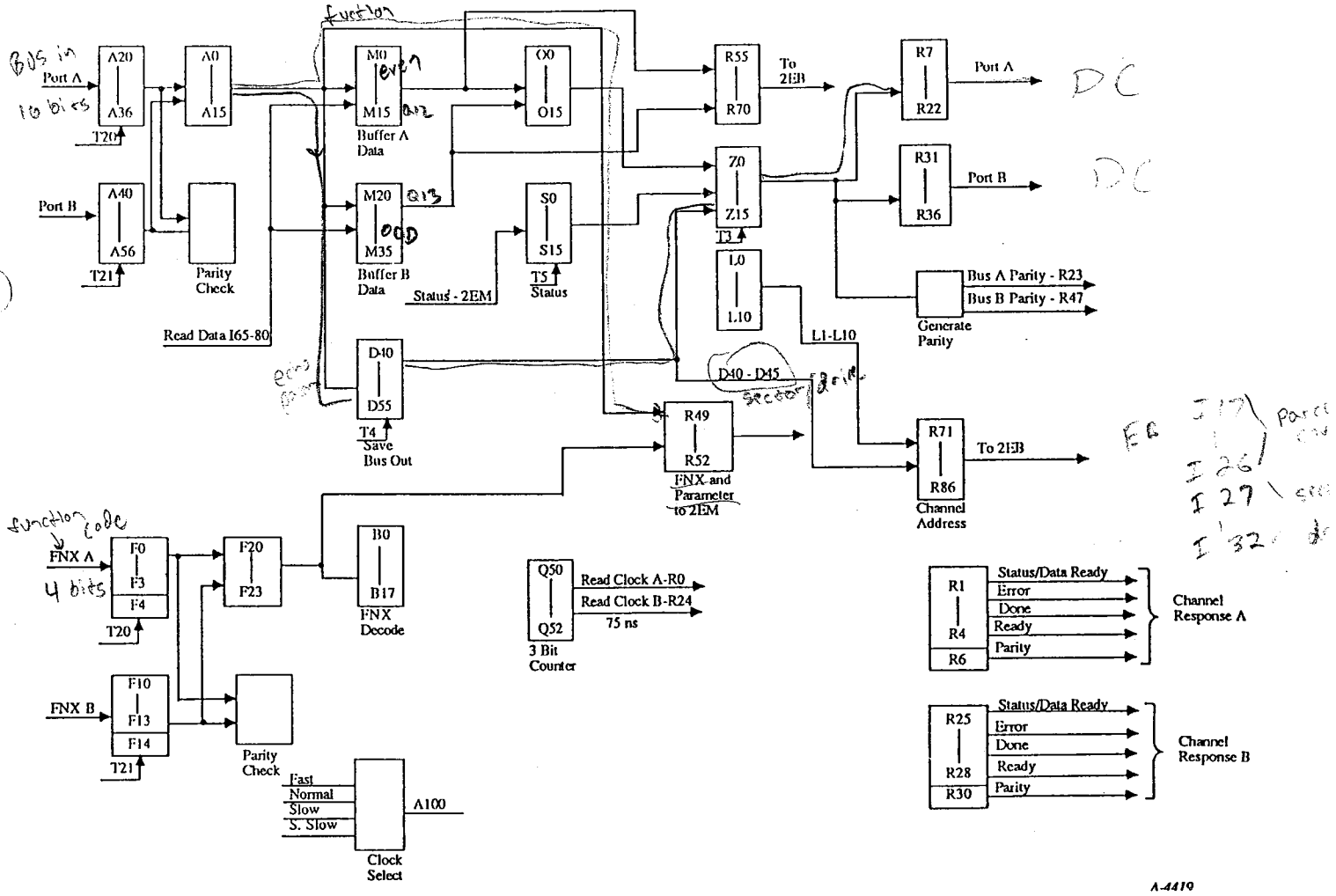


Figure 4-3. 2EI Module Block Diagram

The data is held in the M terms until the buffer sync signals are received from the 2EB module. The Buffer Sync A signal enables the data in terms M0 through M15 to pass through terms R55 through R70 and go to the 2EB module. The buffer sync B signal enables the data in terms M20 through M35 to pass through terms R55 through R70 and go to the 2EB module. The buffer sync signals synchronize data transfer to the desred bank in the 2EB module's full-
track buffer.

4.1.3 2EI MODULE - READ

During a read operation, the data comes to the 2EI module from the full track buffer. The data enters terms M0 through M15 for even parcels and terms M20 through M35 for odd parcels. The data is allowed to pass through O0 through O15 by term L20 (the low bit of the parcel counter) and is latched in terms Z0 through Z15. The data then goes to the DCU-5 by way of terms R7 through R22 for port A and terms R31 through R36 for port B. As the data leaves the 2EI module, a parity bit is generated for each parcel and is sent to the DCU-5 along with the parcel.

4.1.4 2EI MODULE - DIAGNOSTIC ECHO

During a diagnostic echo function, a function code is latched in the F terms and 1 parcel of data is latched in the A terms. The parcel enters terms A0 through A15 and is latched in terms D40 through D55 by term T4. It is then latched into the Z0 through Z15 bus-in terms and is returned to the DCU-5 through the R terms.

4.1.5 2EI MODULE - STATUS

When a status is requested, it is sent to the 2EI module from the 2EM module. When a function is completed, a general status code is latched into terms S0 through S15 by term T5. During the next CP, the general status code is latched into terms Z0 through Z15 bus-in terms and returned to the DCU-5 through the R terms.

4.1.6 2EI MODULE - CHANNEL RESPONSE

After receiving each function code, the DC-40 sends a done signal to the DCU-5 if the function has completed correctly. If the DCU-5 receives an error along with the done signal, an error has occurred and the status must be evaluated. If the DCU-5 does not receive a ready signal, this also indicates an error has occurred. If the DCU-5 does not receive a done signal after a function code is issued, a timeout occurs.

If a function is sent to the DC-40 and a port is not selected, a busy response signal is sent to the DCU-5. The busy response signal is made up of the following: status/data ready, error, and done signals.

4.1.7 2EI MODULE - CLOCKS

The 2EI module provides logic clocks for all the DC-40 modules. It uses four vextron oscillator cells for the clocks. The logic clock speeds are as follows:

- Fast = 81.600 MHZ
- Normal = 80.000 MHZ
- Slow = 78.400 MHZ
- Super Slow = 71.400 MHZ

A read clock is used to synchronize data and status signals to the DCU-5 clock. The read clock is a 3-bit counter (Q50 through Q52) that counts from 1 to 6. The resulting output has a 75ns clock rate.

4.2 2EB MODULE

On a write transfer, the 2EB module (see figure 4-4) receives parallel data from the channel and sends it to the disks as serial data. On a read transfer, the 2EB module receives serial data from the disks and sends it to the channel as parallel data.

4.2.1 2EB MODULE - BUFFER SECTIONING

Figure 4-5 illustrates the buffer partitioning in the 2EB module.

The 2EB module buffer has two banks, A and B. Each bank is partitioned in the same manner with respect to the spindles. Every other parcel is loaded into A and B, so that one bank contains the even parcels and the other contains the odd parcels. Each bank holds 1024 parcels or half of each sector for an entire track. As data comes from the DD-40, the first parcel enters bank A and the second parcel for the same sector enters bank B in the same locations as bank A. The cycle is repeated for the rest of the sector. The buffer is laid out so that each spindle uses a specified part of the buffer. Spindle A has the first 16K, spindle B has the second 16K, and so on. The last 4K of each section is unused.

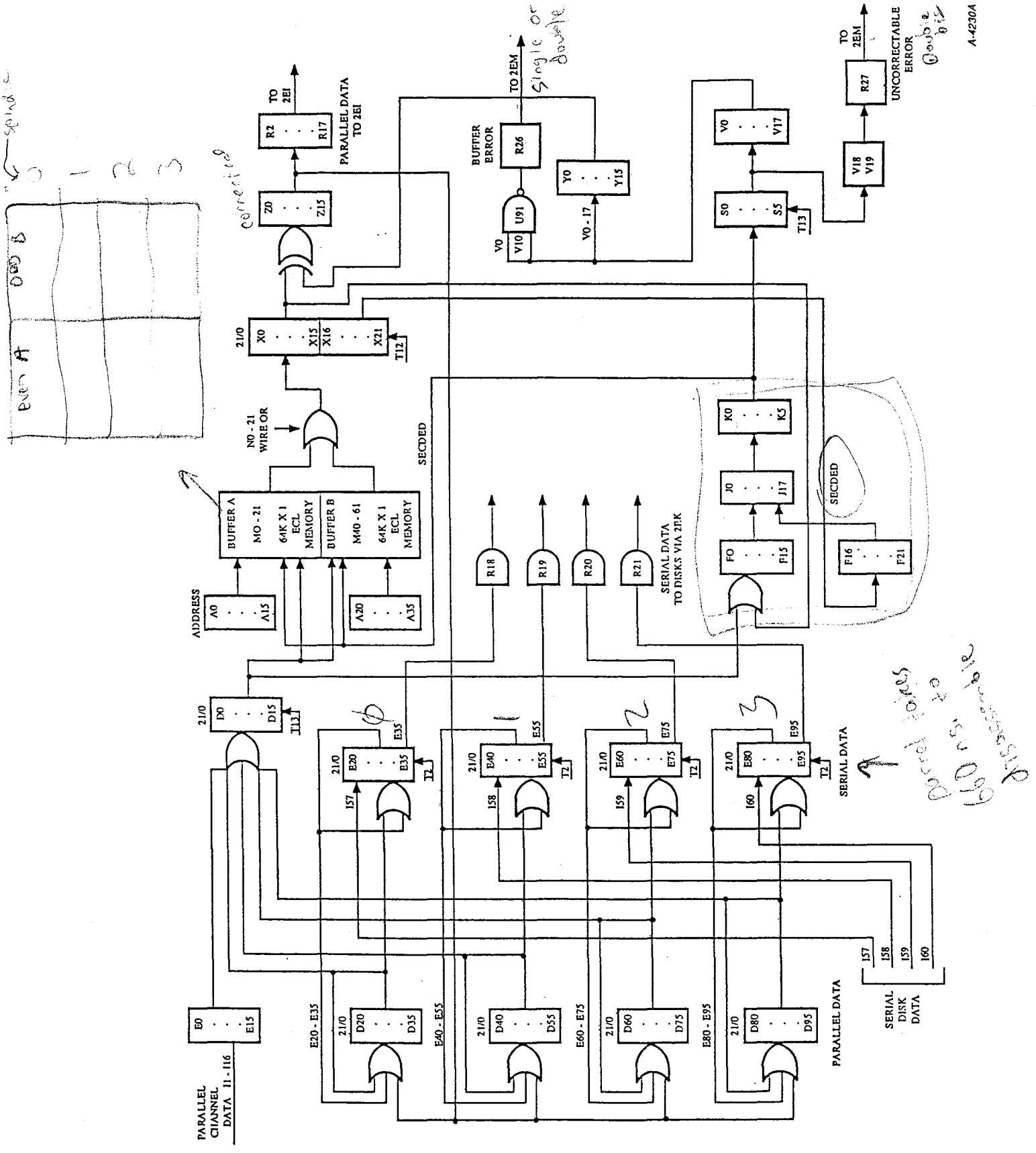


Figure 4-4. 2EB Module Block Diagram

4.2.2 2EB MODULE - WRITE

When a 16-bit parcel of data is received on the channel with the correct buffer sync, the 2EI module sends it to the 2EB module. The data enters terms E0 through E15 and is latched in terms D0 through D15. From here, the data enters the single-error correction double-error detection (SECDED) circuit where check bits are generated. The data, along with 6 check bits for each parcel, is then written into the buffer. When one complete sector is written to the buffer, it can be transferred to the drive. Data is read from the buffer and enters the read-out latches X0 through X21. The read out latches send the data along with the check bits to the SECDED circuitry. The data also goes to terms Z0 through Z15. If a single-bit error is detected, the data is corrected in the Z terms. The data is held in the X terms for 4 CPs. This gives the SECDED circuitry time to perform corrections.

When the corrected data is going to drive A, it enters terms D20 through D35. The Boolean terms correspond to the data channels as follows:

- Terms 20 through 37 are for the spindle A data channel.
- Terms 40 through 57 are for the spindle B data channel.
- Terms 60 through 77 are for the spindle C data channel.
- Terms 80 through 97 are for the spindle D data channel.

From terms D20-D35, data is latched into terms E20 through E35. Data in the E terms is shifted into a serial stream. Each bit of the spindle A data leaves through term E35 and goes out through term R18. The data now goes to the spindle through the 2EK module which generates the error correction code (ECC).

4.2.3 2EB MODULE - READ

The 2EB module receives the data from the spindles in a serial stream. The data enters the E terms (E20 through E35 for spindle A) through terms E20, E40, E60 or E80. As the data enters the E terms, it is shifted until a parcel is assembled. The parcel is loaded into the D terms and the next parcel starts entering the E terms. Once the parcel is through the D terms (D20 through D80, depending on the spindle), it enter terms D0 through D15. The data enters the buffer and is presented to the SECDED circuitry to generate the check bits.

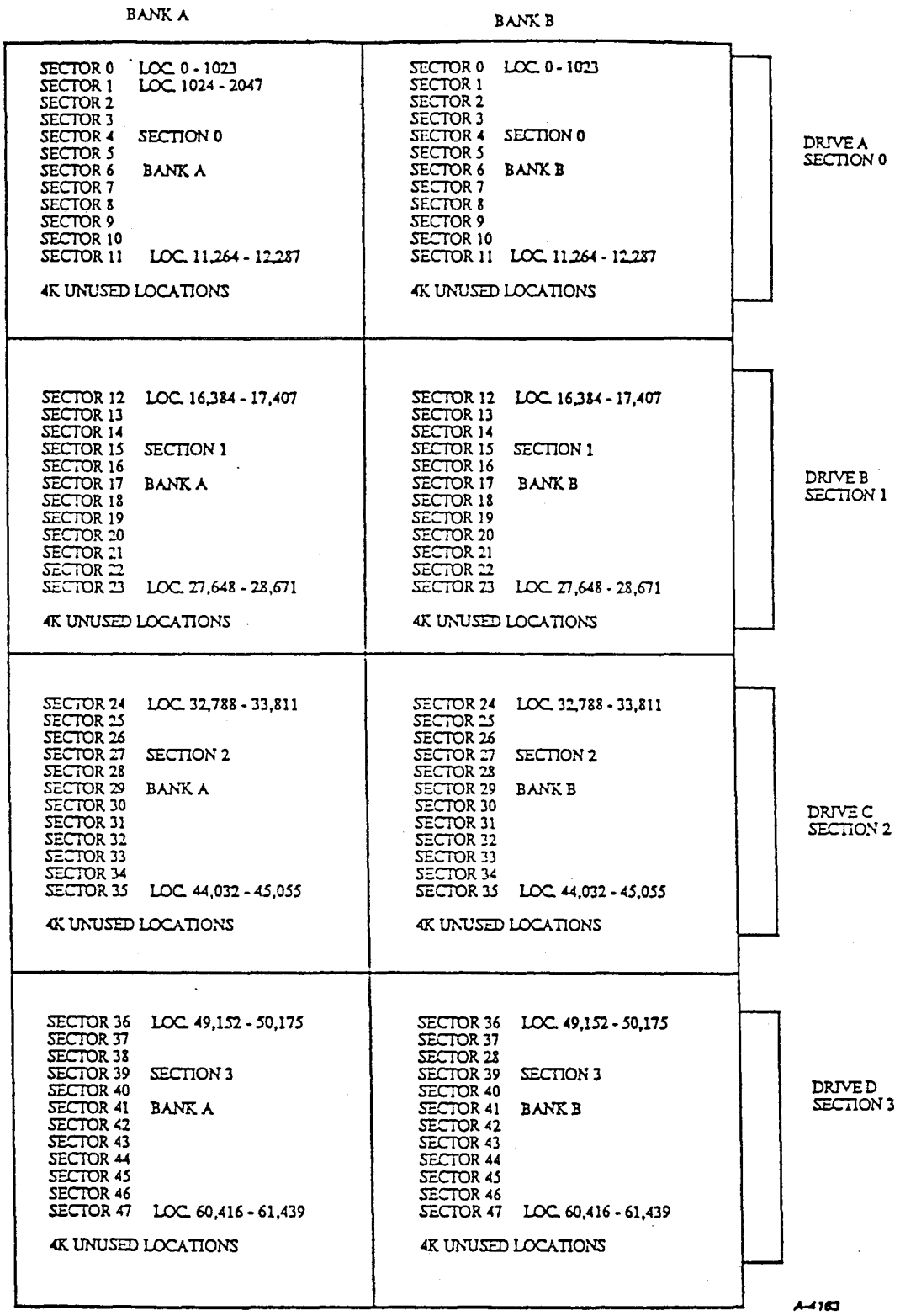


Figure 4-5. 2EB Buffer Partitioning

The data parcel, along with its check bits, is entered into bank A if it is an even numbered parcel or bank B if it is an odd numbered parcel. Once a full sector of data is assembled, it can start transferring to the channel.

When data is read out of the buffer, it enters the readout latches. The data passes through the SECDED circuitry to check for data errors and then enters terms Z0 through Z15. If a single-bit error is detected, the data is corrected and term R26 (buffer error) is sent to the 2EM module. If an uncorrectable error is detected, terms R26 and R27 are sent to the 2EM module which sends them to the 2EI module, where they become part of the error status.

4.2.4 2EB MODULE - SECDED

The SECDED circuitry generates check bits, which are used to check the integrity of data that leaves the buffer. When a single-bit error occurs, a syndrome code is formed. This code identifies and corrects the bit in error before the data leaves the 2EB module. When no error is detected, the syndrome code is all 0's. If there is a single-bit error, 3 bits of the 6 bits in the syndrome code are set. The following figure is a matrix that shows the check bits which are set for parcel bits in error. For example, if bit 12 in the data parcel is in error, check bits 18, 19, and 20 are set.

	Check Bits						Data Bits																
	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
K0						X	X		X		X		X		X		X		X		X		
K1					X			X			X	X			X	X			X	X		X	
K2	Syndrome			X			X	X	X	X					X	X	X	X					
K3	Bits		X					X	X	X	X	X	X	X								X	
K4		X					X			X		X	X	X				X		X	X		
K5	X													X		X	X	X	X	X	X	X	
																							Syndrome
	40	20	10	04	02	01	25	16	15	34	13	32	31	70	07	46	45	64	43	62	61	52	octal
	20	10	08	04	02	01	15	0E	0D	1C	0B	1A	19	38	07	26	25	34	23	32	31	2A	hex

Figure 4-6. Syndrome Bits Matrix

The SECDED circuitry has the capability of correcting single bit errors and detecting double bit errors. A single bit in error is corrected in the Z terms and R26 (buffer error) is sent to the 2EM module.

When a single-bit error occurs (if the syndrome code is written in hexadecimal), the lower digit points to the data bit in error, unless it is data bit 2^{15} or 2^{0}.

The SECDED circuitry detects double-bit errors by checking for an even number of syndrome bits being set. When a double-bit error is detected, the SECDED circuitry is unable to correct it and terms R27 (uncorrectable error) and R26 (buffer error) are sent to the 2EM module, and sent back to the controller.

4.2.5 2EB BUFFER ADDRESSING

The 2EB buffer has two banks. The banks together hold 48 sectors plus syndrome bits for each parcel. Each bank can hold 48k parcels. (16k or 1/4 of each bank is unused).

There are two sets of addressing terms, A0 through A15 for bank A and A20 through A35 for bank B. The address terms can be loaded with either the channel address from the 2EI module or the incremented address from the C terms (C0 through C15). The state of term Q2 (which comes from term G2) dtermines which addressing scheme is used by banks A and B. When term Q2 is cleared, bank A uses the incremental address from the C terms and bank B uses the channel address from the 2EI module. When term Q2 is set, bank A uses the channel address and bank B uses the incremental address. The free running count in terms Q0 through Q2 selects the bank. Two terms (H2 and H12) are sent to the 2EI module, so it knows which bank is being used for channel data and can send the channel address at the correct time.

Figure 4-7 is a simplified diagram of the buffer addressing for spindle A. Figure 4-8 shows the buffer addressing for all the spindles.

The 2EB module uses 16 bits of address (terms C0 through C15) to access the banks of the buffer. The lower 10 address bits (terms C0 through C9) come from a set of B terms. The set of B terms used depends on the spindle that is accessing the buffer. The next 4 address bits (terms C10 through C13) come from the sector that is being read or written. The sector number is sent from the 2EM module. Table 4-1 shows how the upper 2 bits (terms C14 and C15) designate the spindle that is accessing the buffer.

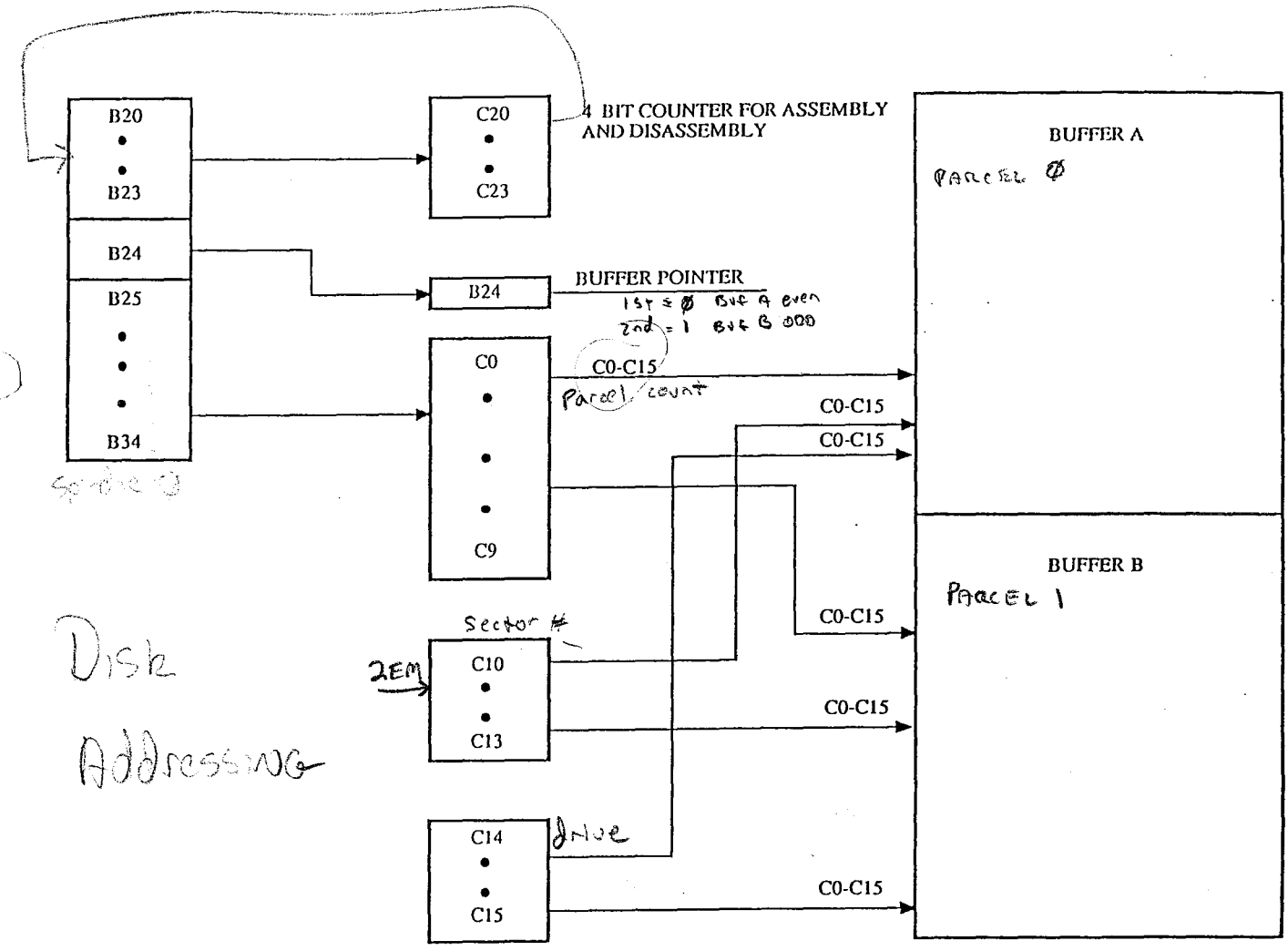


Figure 4-7. 2EB Buffer Addressing - Simplified Diagram

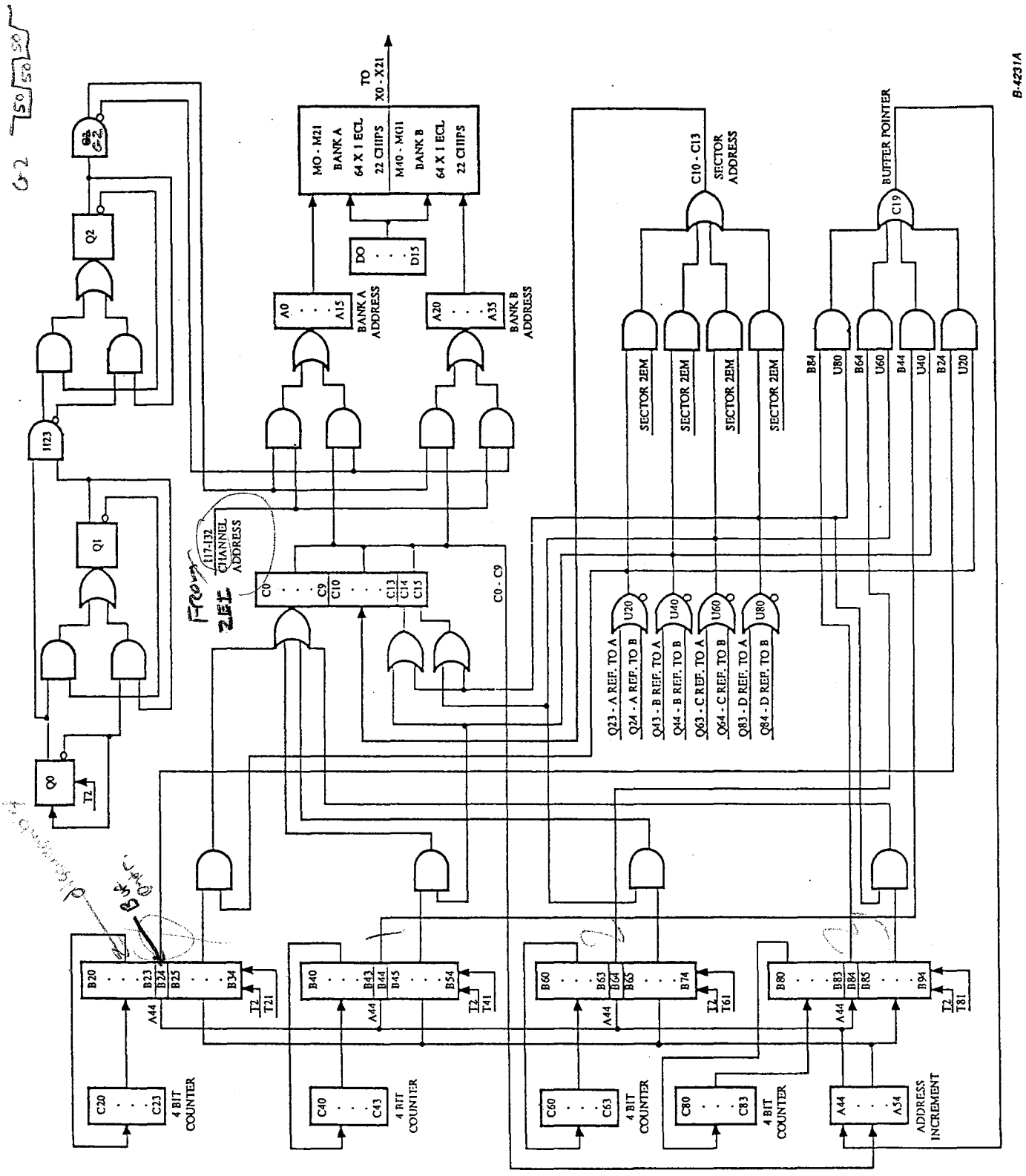


Figure 4-8. 2EB Buffer Addressing

Table 4-1. 2EB Module Spindle Address Bits

Spindle	C15	C14
A	0	0
B	0	1
C	1	0
D	1	1

Term C19 points to the buffer being used, but C19 is not presented to the buffer as part of the address. Terms C20 through C23 count the number of CPs needed to assemble a 16-bit parcel.

Figure 4-9 illustrates the address field.

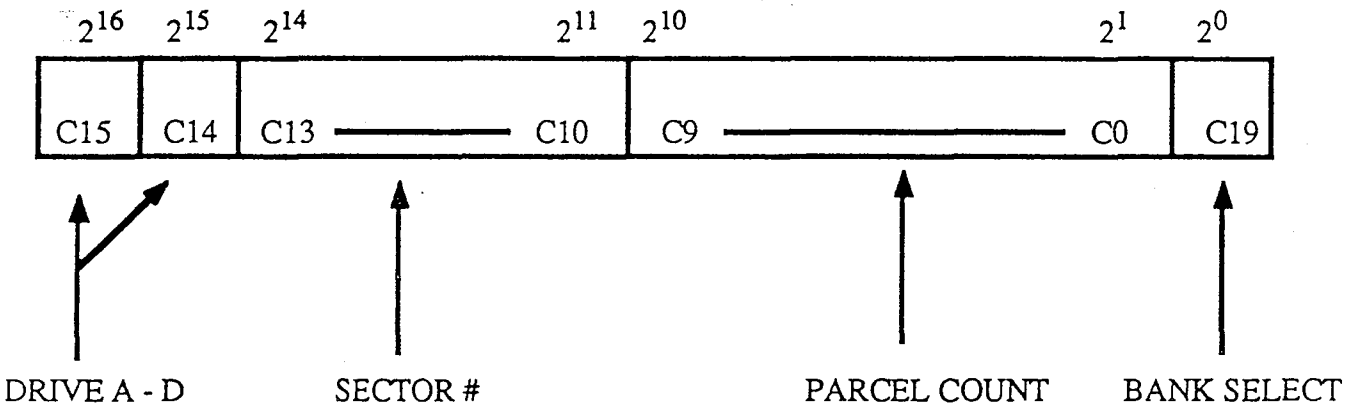


Figure 4-9. Address Field

4.2.6 2EB PRIORITY SCHEME

Each disk has a predetermined priority assigned to it. Because each spindle can have a parcel ready for the buffer every 660 ns and the buffer can accept a parcel every 100 ns, spindle priority is not a problem. Table 4-2 shows the priorities assigned to the spindles.

Table 4-2. 2EB Module Priority Scheme

Spindle	U Term	Q Term	Enable	Buffer A	Buffer B
A	U12	Q23	U20	First	
A	U13	Q24	U20		Last
B	U14	Q43	U40	Second	
B	U15	Q44	U40		Third
C	U16	Q63	U60	Third	
C	U17	Q64	U60		Second
D	U18	Q83	U80	Last	
D	U19	Q84	U80		First

The U terms (U12 through U19) are made up of a buffer pointer and a disk reference pending. When the enable conditions are met, the enable term will enable the buffer pointer, the address, the sector, the disk, and the clock signals.

For example, the spindle A enable term is U20. It enables the following:

Clock - T21 by way of V22
Address - C0 through C9; B25 through B34 path
Buffer pointer - C19; B24 path
Sector from 2EM - C10 through C13; I35 through I38 path
Disk - C15 and C14
Parallel Load - D20 through D35 by G25
Reference A - R22 to the 2EM module

The buffer pointer term (C19) looks at the fifth bit (that is, terms B24, B44, B64, and B84) of each set of B terms and the drive enable signal. The spindle accesses the same address in both buffers before the address for the spindle is incremented. The buffer pointer and the lower 10 bits of the address (terms C0 through C9) are fed back into A44 through A54 (address increment terms). After the address is incremented, it is fed back to the B terms for the disk that has been accessing the buffer. Each spindle has a 4-bit counter that keeps track of the assembly and disassembly of the parcels.

4.3 2EM Module

The 2EM module controls read and write data transfers. However, data does not pass through the 2EM module. Figure 4-10 is a block diagram of the 2EM module for spindle A.

The 2EM module receives the function code and go function signal from the 2EI module. The 4-bit function code is followed by the 16-bit function parameter, 4 bits in each of the next 4 CPs, which is latched in terms A0 through A15. The function code and read/write mode bits are decoded to determine what kind of function is being executed.

The function code and parameter codes are sent to the appropriate 2EJ module in 4-bit nibbles (except on diagnostic echo and buffer echo, for which this is blocked).

The 2EM module receives the channel done signal from the 2EI module and the function done signal from the four 2EJ modules. When the function has been completed, the 2EM module sends the done signal to the 2EI module. The 2EM module also sends error and status signals to the 2EI module. As sectors of data are read from the buffer, the sector status signal is checked for errors on each sector.

The 2EM module has 48 G terms, each of which is a sector ready corresponding to a specified sector for each track. That is, G term G0 is for sector 0, G term G1 is for sector 1, and so on. When reading a sector, the G term corresponding to the sector is set, indicating that the sector is in the buffer and is ready to be transferred to the DCU-5.

When writing a sector, the G terms are set before data is sent across the channel. As a sector of data is written into the buffer, the corresponding G term clears. When the data is written to the disk, the G term sets again.

2.3.1 2EM MODULE - DONE CIRCUITRY

Figure 4-11 shows the done circuitry for the 2EM module. The done term (Q20) sets through one of three paths and is passed to the 2EI module on term R0. When the done term sets, it is sent to the 2EI module for 1 CP. The first of the three paths that sets the done term is term P13, which checks that all spindles are complete on functions that do not use the buffer.

The second path for setting the done term is through terms P15 and Q7. This is the path used to set the done term on read and write ahead commands. On a read ahead and a write ahead, the done term is set when data is in the buffer ready to be written to the channel or the disk. This allows the transfers into the buffer to be independent of the transfers from the buffer to the channel or the disk. On a read ahead, the done term is also set when the data transfer completes because the data transfer does not start until the entire requested sector is in the buffer. The 2EI module sends the channel done signal when it has counted the correct number of parcels for a read or write. The channel done signal from the 2EI module is latched in term Q40. When there is no done term from the 2EJ modules and no write synchronize signal, done is latched in term Q7 (sector done). Once term Q7 sets, a read or write ahead allows the done term to be set and sent to the 2EI module.

If an error is detected on a write ahead, term Q29 (write synchronize) sets and blocks the done term from being sent to the 2EI module. The write synchronize term allows all data to be written from the buffer to the disk before the done and error terms are sent to the DCU-5. The write synchronize term also sets on the following conditions: 1) if the next function code is not a write mode 0, 2) if the next function code is a write ahead with a new head, or 3) any one of the functions listed under term D15 (read immediate) are set.

The write synchronize term is cleared when a write ahead completes and all sector readies are set, indicating all data has been transferred to the disk from the buffer. When a read or write ahead is being executed, term P15 enables the next read/write parameter to be sent to the appropriate 2EJ module, provided a sector pulse is received, indicating the correct sector has been read or written.

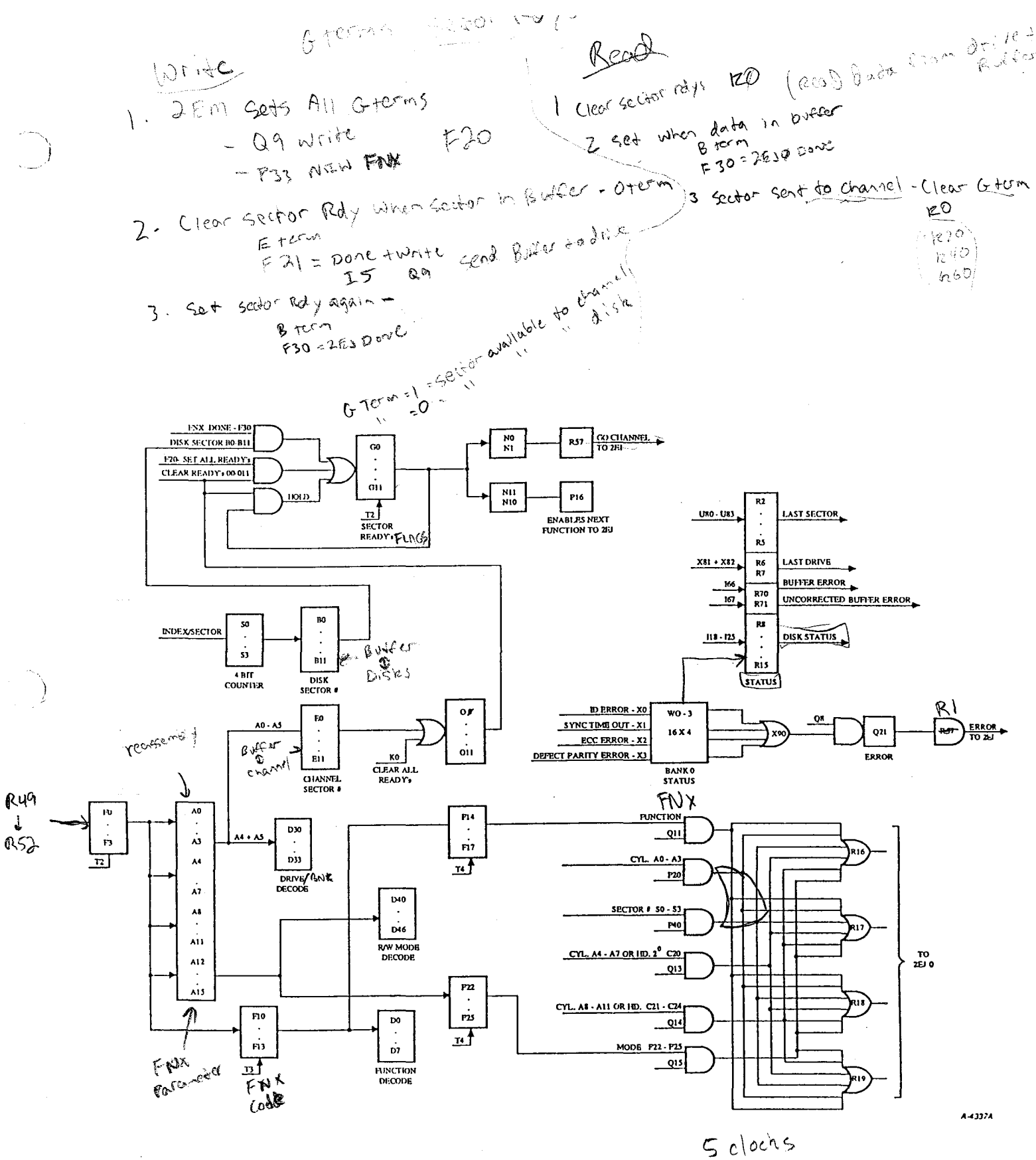


Figure 4-10. 2EM Module Block Diagram for Spindle A

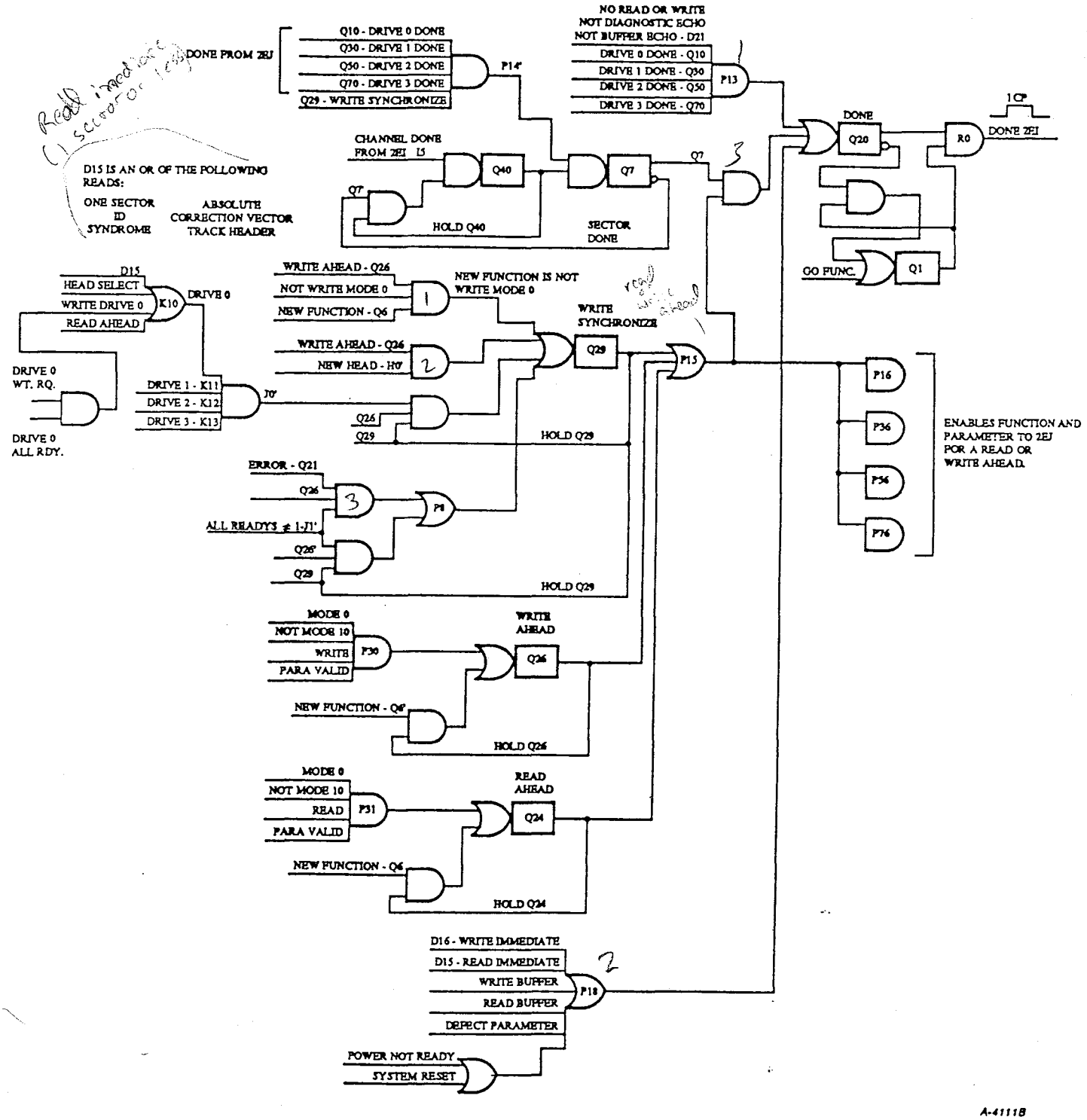


Figure 4-11. DONE Circuitry - 2EM Module

The last path that can set the done term is term P18. The done term sets through term P18 for read immediate, write immediate, read buffer, write buffer, transfer defect parameter, or not ready terms. A read and write immediate is any read or write of a single sector or less. Table 4-3 lists the read and write immediate modes

Table 4-3. Read and Write Immediate Modes

Done	Read Immediate (D15)	Write Immediate (D16)
1	Read ID	Write ID
2	Read Absolute	Write Defective
4	Read Syndrome Block	Write Data with 0 ECC
5	Read Correction Vector	N/U
6	Read Track Header	N/U
10	Read 1 Sector	Write One Sector

4.3.2 2EM MODULE - ERROR TERM

Figure 4-12 shows the error circuitry for the 2EM module.

When the error term (Q21) sets, it is sent to the 2EI module. Term Q21 is not latched on the 2EI module, however, until the done term (Q20) sets. The error term sets when a status is not being requested and there is a buffer error, a seek error, or a drive fault term (Y5). When doing a read operation, a defect parameter parity error, an ID error, an ECC error, or a sync timeout error is sent to the 2EI module when the go channel term (Q22) is set. On a write operation, the previous four error signals are checked in addition to the the buffer error from the 2EB module. When the error signal is set, it remains set until the done term sets.

A write error always causes the error signal to be flagged on the channel immediately. A read error is latched into the status buffer and only causes a channel error if the sector is requested from the track buffer.

4.3.3 2EM MODULE - PARAMETER/FUNCTION TO 2EJ MODULE

The 2EM module sends the parameter and function to the 2EJ module. (There are four 2EJ modules, 2EJ-0 through 2EJ-4.) The function code is sent to the 2EJ-0 module when term Q11 sets or to the 2EJ-1 module when term Q31 sets. Once the function code is sent by term Q11, term Q12 sets on the next clock period, enabling bits 2^0 through 2^3 of the function parameter code to go to the 2EJ module. Term Q13 sets on the next CP, enabling bits 2^4 through 2^7 to go to the 2EJ module, and so on. Function codes going to the other 2EJ modules are handled the same way, except a different set of Q terms is used. Table 4-4 gives the terms used for each of the 2EJ modules.

The following relationships between control terms apply here:

```
Q11 = D21 P33 + P16 + P17
Q31 = D21 P33 + P36 + P37
Q51 = D21 P33 + P56 + P57
Q71 = D21 P33 + P76 + P77

P17 = P0 Z4 P9 + D30 D15 P33
P37 = P1 Z5 P9 + D31 D15 P33
P57 = P2 Z6 P9 + D32 D15 P33
P77 = P3 Z7 P9 + D33 D15 P33
```

The control term that sends the function parameter code to the 2EJ module (Q11, Q31, Q51 and Q71) can be set in the following four ways:

- If the function code is not a read or write term (D21), or a read or write ahead function and the previous write ahead has (term P33) finished. This applies to function codes for all four banks.

- If term P16 is set. Term P16 checks if the buffer is ready to receive data (terms P0 through P3) on either a read ahead or a write ahead (term P15) and there is a sector pulse from the drive (terms Y6 through Y13).

- If a write immediate (terms D16 or P9) is set with the buffer available.

- If a read immediate (term D15) is set with the right bank selected (terms D30 through D33) with a new function code (term P33).

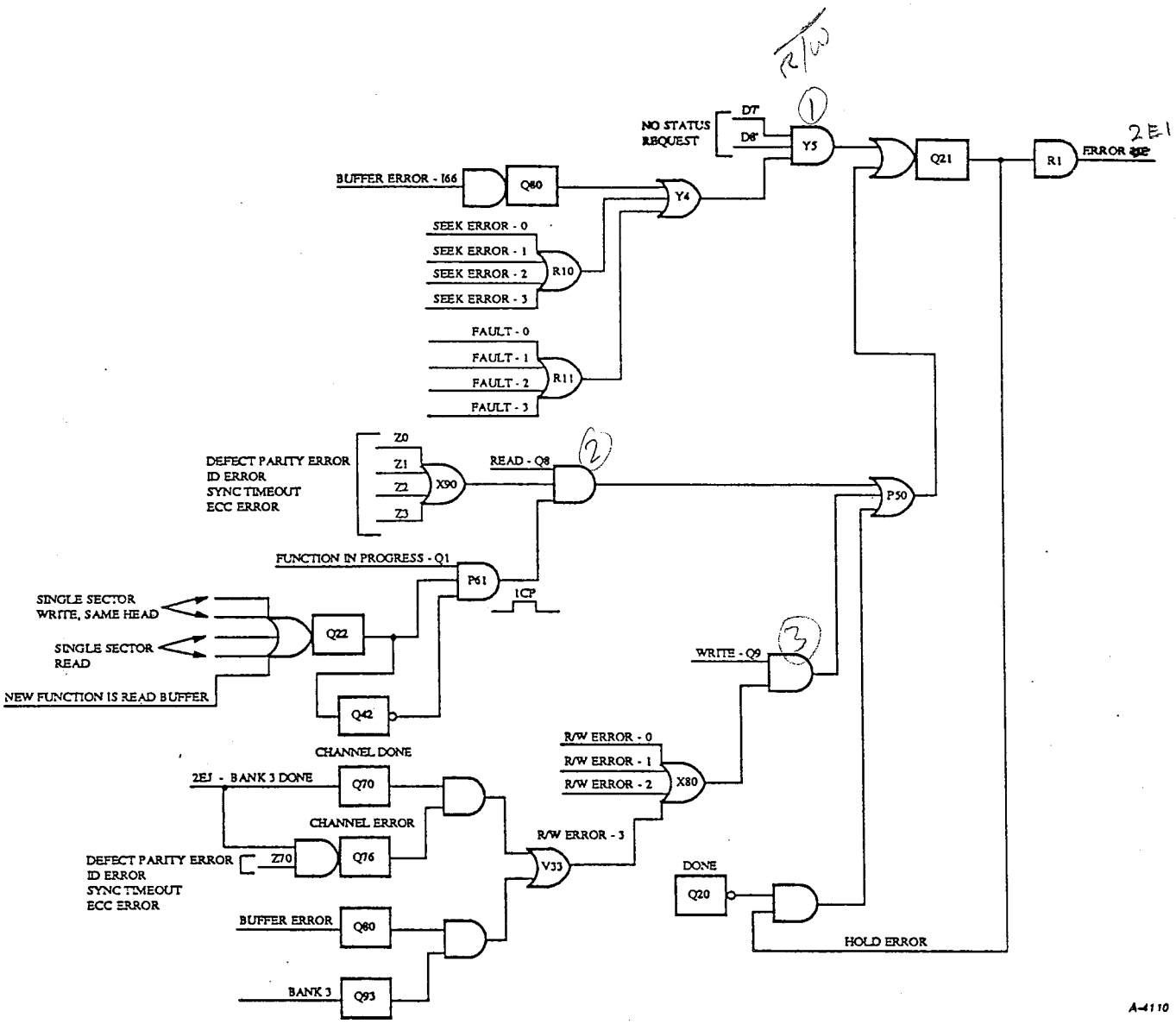
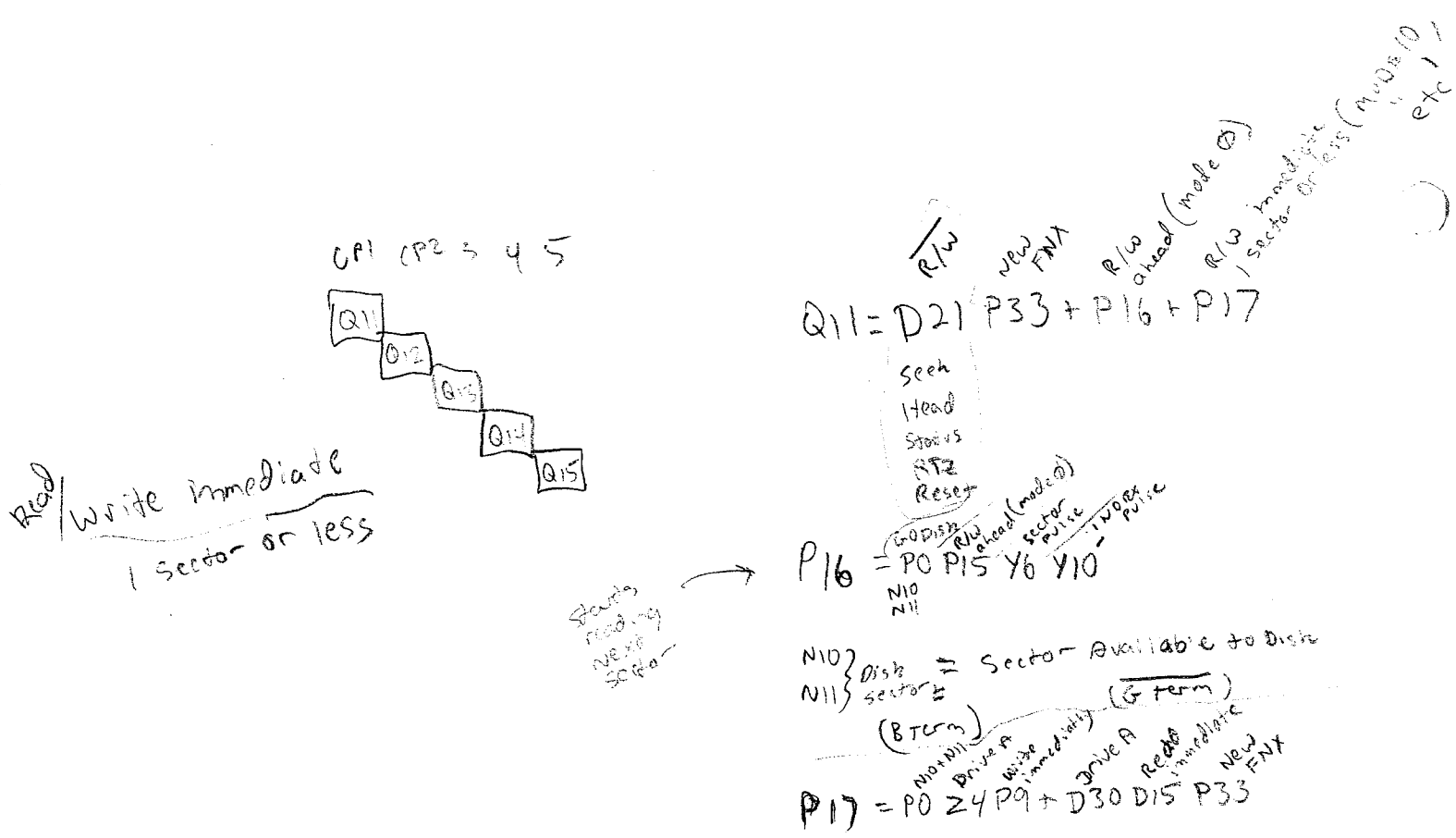


Figure 4-12. ERROR Circuitry - 2EM Module



READ OR WRITE MODE	CYLINDER NO. OR HEAD NO.	CYLINDER NO. OR HEAD BIT 2 0	SECTOR NO. ON READ OR WRITE AHEAD	CYLINDER NO. WITH NO READ OR WRITE AHEAD	FUNCTION CODE	OUTPUTS
Q15 F22 Q15 F23 Q15 F24 Q15 F25	Q14 P26 Q14 P27 Q14 P28 Q14 P29	Q13 A4 Q13 A5 Q13 A6 Q13 P25	P40 S0 P40 S1 P40 S2 P40 S3	P20 A0 P20 A1 P20 A2 P20 A3	Q11 F14 Q11 F15 Q11 F16 Q11 F17	R16 R17 R18 R19 — PARAMETER/FNX TO 2EJ-0
Q35 F22 Q35 F23 Q35 F24 Q35 F25	Q34 P26 Q34 P27 Q34 P28 Q34 P29	Q33 A4 Q33 A5 Q33 A6 Q33 P25	P41 S20 P41 S21 P41 S22 P41 S23	P21 A0 P21 A1 P21 A2 P21 A3	Q31 F14 Q31 F15 Q31 F16 Q31 F17	R20 R21 R22 R23 — PARAMETER/FNX TO 2EJ-1
Q55 F22 Q55 F23 Q55 F24 Q55 F25	Q54 P26 Q54 P27 Q54 P28 Q54 P29	Q53 A4 Q53 A5 Q53 A6 Q53 P25	P42 S40 P42 S41 P42 S42 P42 S43	P22 A0 P22 A1 P22 A2 P22 A3	Q51 F14 Q51 F15 Q51 F16 Q51 F17	R24 R25 R26 R27 — PARAMETER/FNX TO 2EJ-2
Q75 F22 Q75 F23 Q75 F24 Q75 F25	Q74 P26 Q74 P27 Q74 P28 Q74 P29	Q73 A4 Q73 A5 Q73 A6 Q73 P25	P43 S60 P43 S62 P43 S62 P43 S63	P23 A0 P23 A1 P23 A2 P23 A3	Q71 F14 Q71 F15 Q71 F15 Q71 F17	R28 R29 R30 R31 — PARAMETER/FNX TO 2EJ-3

A-4101

Table 4-4. Parameter/Function to the 2EJ Module

4.4 2EJ MODULE

There are four 2EJ modules in each DC-40 controller. Each 2EJ module controls a spindle in a DD-40. The 2EJ module has a prom sequencer consisting of a series of instructions for each disk function. Each 2EJ module receives read data from a spindle and passes it to the 2EK module. Figure 4-13 is a block diagram of the prom sequencer.

4.4.1 2EJ MODULE - FUNCTION AND PARAMETERS

The 2EJ module receives the function code and go function from the 2EM module. The function code is followed by 16 parameter bits. These bits specify the mode, head, cylinder, sector, and so on. As the head, cylinder, and sector parameters arrive on the 2EJ module they are entered into registers. The mode bits and function code go through a decoding process to determine which function is being executed. The go function code goes through a delay and sets term H21, which allows the 4 bits of the function code to be used as the first prom address.

4.4.2 2EJ MODULE - PROM SEQUENCER - ADDRESSING

Terms S0 through S7 terms contain the addresses for the prom chips. The prom address can be either the function code or the next prom address from the prom sequencer. The first prom address for a specific sequence is the 4-bit function code in terms F10 through F13. The first prom address in a sequence corresponds to an address in the function table.

After the first function code, subsequent addresses come from the prom sequencer's next address field. The prom sequencer continues using the next address field until it comes to a next address containing all zeros which returns it to the idle loop. (The next address field is terms W0 through W7. Terms W0 and W1 go to the prom address by way of terms Z0 and Z1.)

2.4.3 2EJ MODULE - PROM SEQUENCER - CONTROL FIELD

The control field terms (S8 through S13) come from the prom sequencer and act as an enabler for different parts of the sequence. Table 4-5 describes each bit in the control field.

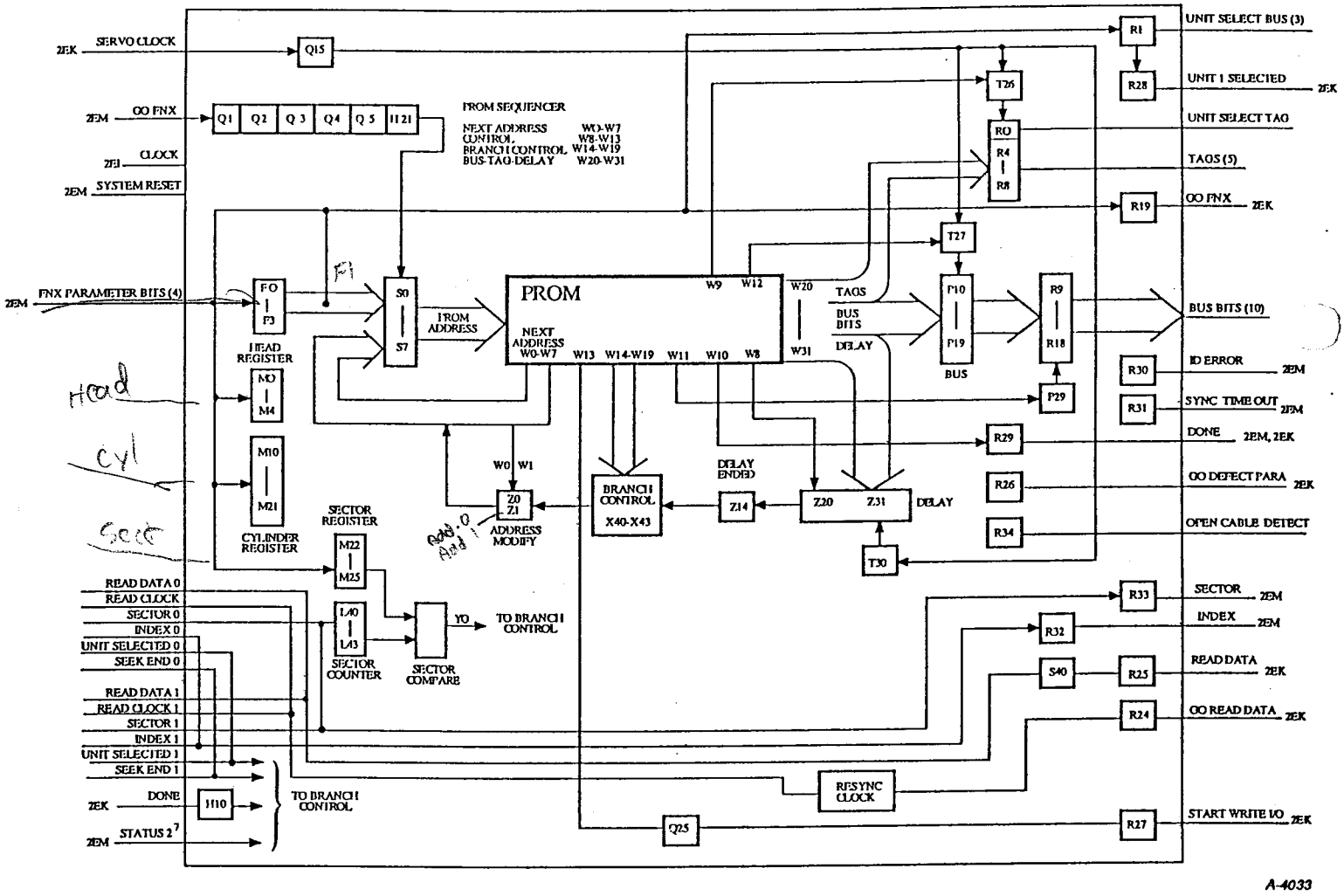


Figure 4-13. Prom Sequencer Block Diagram

Table 4-5. Prom Sequencer Control Field Bits

Control Field Bit	Bit Name	Function
S8	Delay	Enables the delay to be loaded into Z20 to Z31
S9	Strobe Tag	Latches tag values from the bus field.
S10	End	Stops execution and clears hardware (2EJ)
S11	Gate Bus	Sends bus bits to the drive (P29/M30)
S12	Strobe Bus	Latches bus bits from the bus field in P10 to P19 (T27)
S13	Start I/O	Starts a read or write transfer (term Q25)

4.4.4 2EJ MODULE - PROM SEQUENCER - BRANCH CONTROL

The bit assignments for the branch control field terms (S14 through S19) are shown in figure 4-14.

The branch control field terms (S14 through S19) are used to test for 16 different conditions. When the condition being tested for is true, a jump of one, two, or three locations can be done. Terms S16 through S19 are used to enable one of the four multiplexer chips (terms X40 through X43) and terms S14 and S15 select one of the four conditions being checked for by that chip. For example:

S14	S15	S16	S17	S18	S19
0	1	0	0	1	0

In this example terms S15 and S18 are 1. Under these conditions, the branch control field is checking for a mode 2 term (C22). Once the conditions are met, term X42 sets and goes through an exclusive OR with term W0.

When term X40 or X42 is set, bit 2^0 (term W0) of the prom address field is modified. When term X41 or X43 is set, bit 2^1 (term W1) of the prom address field is modified.

		X40	X41	X42	X43
Modified Address Bit		2^0	2^1	2^0	2^1
Command Word Bits		2^{15}	2^{16}	2^{17}	2^{18}	2^{19}
Field Bit # 0	1	2	3	4	5
2^{14}					
0	0	Mode 0 C20	Sector Compare Y0	Mode 4 C24	Unit Selected V9
1	0	ID Found Q8	Delay Ended Z14	Mode 1 C21	Seek End V10
0	1	Transfer Read Data Q16	Status 2^7 I17	Mode 2 C22	Select Status N3
1	1	End Transfer H10	Selected Status D1	Mode 6 C26	Select Status N4

Figure 4-14. Branch Control Fields

Branch=1 Branch=2

4.4.5 2EJ MODULE - PROM SEQUENCER - BUS, TAG, DELAY

When a delay (terms S20 through S31) is loaded into the delay counter, the delay bits are set (terms Z20-Z31). When the drive performs a function, the tags (terms S20-S25) corresponding to the function are set. Bus bits are set on the bus lines (terms S20 through S29).

4.4.6 2EJ MODULE - ID COMPARE

On a read or write, the ID is read from the disk and compared to the head, cylinder, and sector registers on the 2EJ module. As the ID comes in to the compare circuitry on the 2EJ module, each of its bits is compared to the corresponding bit of the 2EJ's registers in an exclusive OR. IF the ID does not compare to the ID in the 2EJ's registers, ID error is set in the general status code. As the ID is read from the registers to the compare circuit, it also goes to a circular shift path, which shifts it back into the registers. Because of this shift, when the compare is complete, the registers have the same value as when the compare was started. Figure 4-15 shows how the ID compare is done.

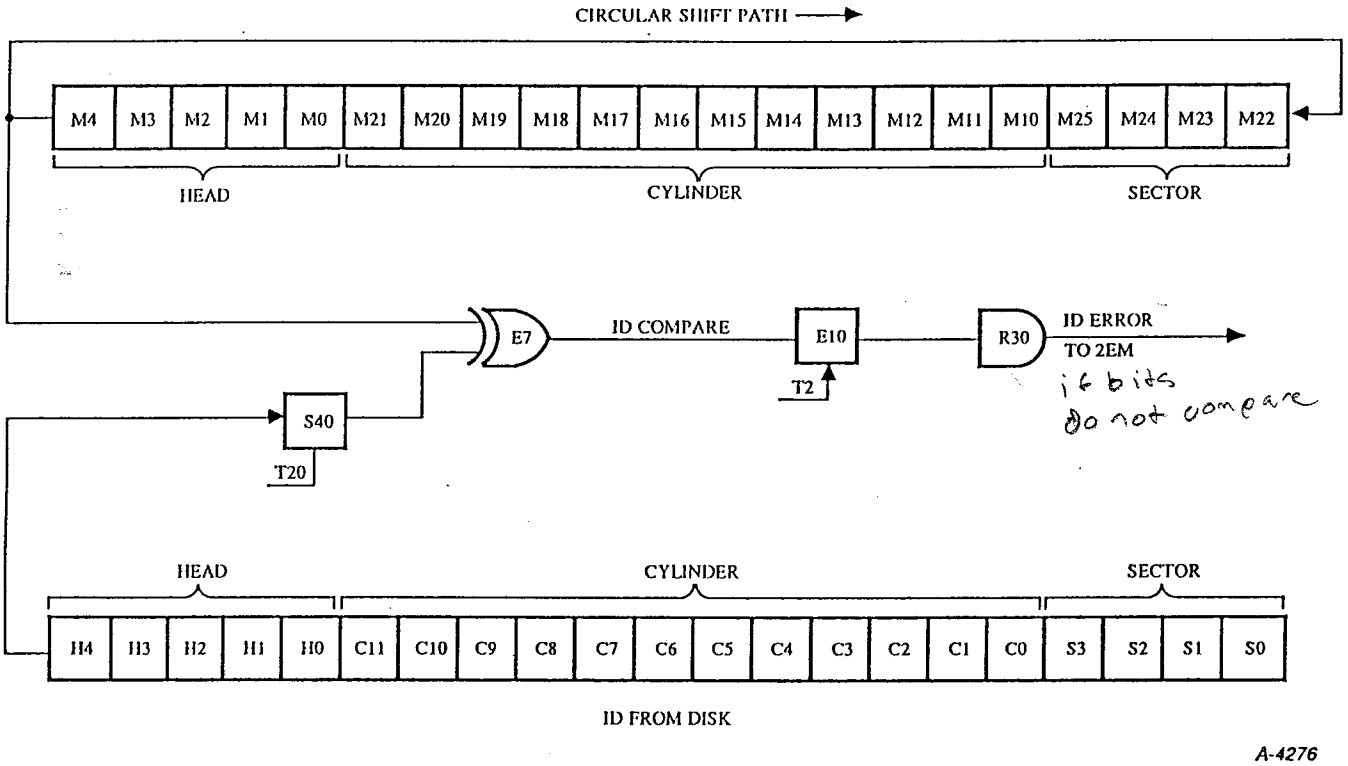


Figure 4-15. 2EJ ID Compare Circuit

4.5 2EK MODULE

The 2EK module (see figure 4-16) passes read data from the 2EJ module to the buffer and write data from the buffer to the DD-40. As the read and write data goes through the 2EK module, the data enters a 32-bit shifter, which generates the ECC code. At the same time the data enters the shifter, it is latched in term L20 (channel 0). From term L20, the data is passed to either the 2EB module or the disk.

At the end of a read operation, the shifter content is checked for a data error. If a data error occurred, the 2EK module notifies the 2EM module of this. The 2EK module, using a signal unit 1 selected from the 2EJ module, selects a servo clock from the DD-40. When a flaw is present, the defect detect circuit detects the location of the defect in a sector and disables the data circuitry during the defect.

The 2EK module has four channels, one for each data path. The Boolean terms correspond to the channel as shown below:

Boolean Term	Channel
0-99	0
100-199	1
200-299	2
300-399	3

4.5.1 2EK MODULE - WRITE

The 2EK module receives write data from the 2EB module one bit at a time. The data is first latched in term L21 and then goes to term L20 and the linear feedback shifter. From term L20, the data is sent through the output, term R4, to the disk. As a sector of data passes through the 2EK module on its way to the disk, the shifter continues to shift. When a full sector of data has been sent to the disk, the shifter contains an error-correction code unique to the data pattern just written. The contents of the shifter is written to the disk directly after the data. (The starting value of the shifter is all zeros.)

4.5.2 2EK MODULE - READ

The data path on a read is similar to a write. The data and the read clock are received from the 2EJ module. The data is latched in term L21. From term L21, the data goes to term L20 and the shifter. From term L20, the data is sent through the output, term R3, to the 2EB module. The shifter is set to all zeros at the beginning of the read. The shifter does the same thing on the read as it did on the write.

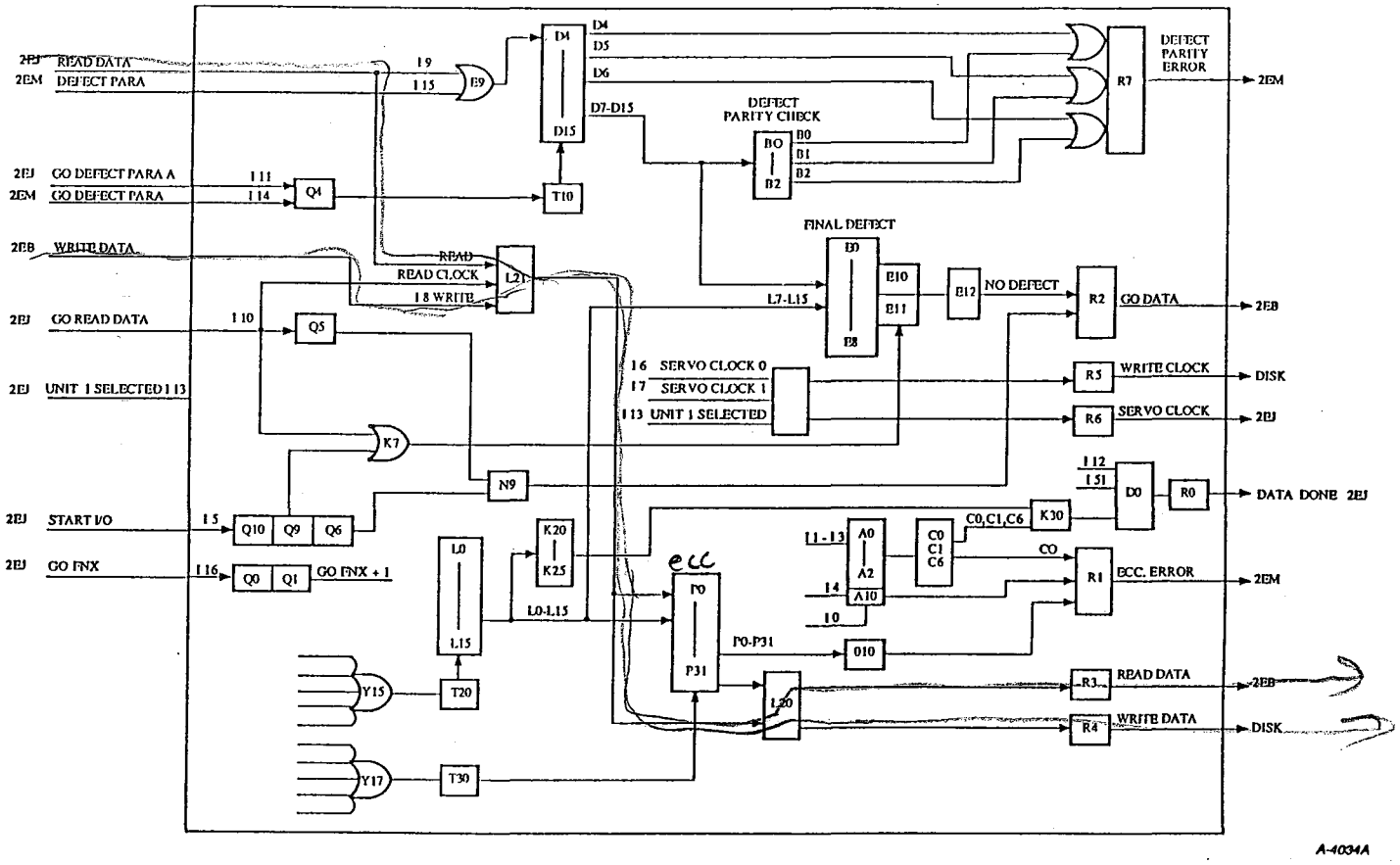


Figure 4-16. 2EK Single Channel Block Diagram

After the data has been read, the shifter contains the same 32-bit checkword as it generated on the write. The checkword is read from the disk following the last bit of data. As the checkword enters the shifter, the corresponding bits cancel out and the shifter is left with all zeros, indicating no error was detected.

4.5.3 2EK MODULE - CORRECTION VECTOR

Figure 4-17 shows a four-channel block diagram of the error-correction shifters for the 2EK module. Figure 4-18 shows a block diagram for an individual bit counter/shifter.

The contents of the shifter after an error has occurred can be used to correct the error if the error is no longer than a burst of 8 bits. This is done as follows:

1. The contents of the shifter is preshifted to the left by 65,536 minus (32,768 + 32) = 32,746 times. 65,536 = the length of the polynominal used. 32,768 = the number of data bits from one head in a sector. 32 = the number of check bits.

2. The shifter computes the correction vector by shifting until the lower 24 bits are all 0's. A counter keeps track of the number of positions shifted. When the correction vector is found, the inverse of the counter is loaded into bits 8 through 23 of the shifter. A 0 shift means the correction vector is applied starting on the first data bit. A shift of one means the correction vector is applied starting on the second data bit, and so on. The upper 8 bits of the shifter (24 through 31) contain the mask. Bits 8 through 23 contain the offset.

3. If the shifter is shifted 32,768 + 32 = 32,800 times and the lower 24 bits never equal 0, the error is uncorrectable. The inverse of the counter is all 1's, indicating an uncorrectable error.

4. The offset and mask (the upper 24 bits of the shifter) are sent to the controller/IOP as the correction vector. The offset is the inverse of the number of shifts before the correction vector was found. The offset is found in bits 8 through 23 of the correction vector. It is used to determine how far from the beginning of the sector (bit 2^0) the mask is applied.

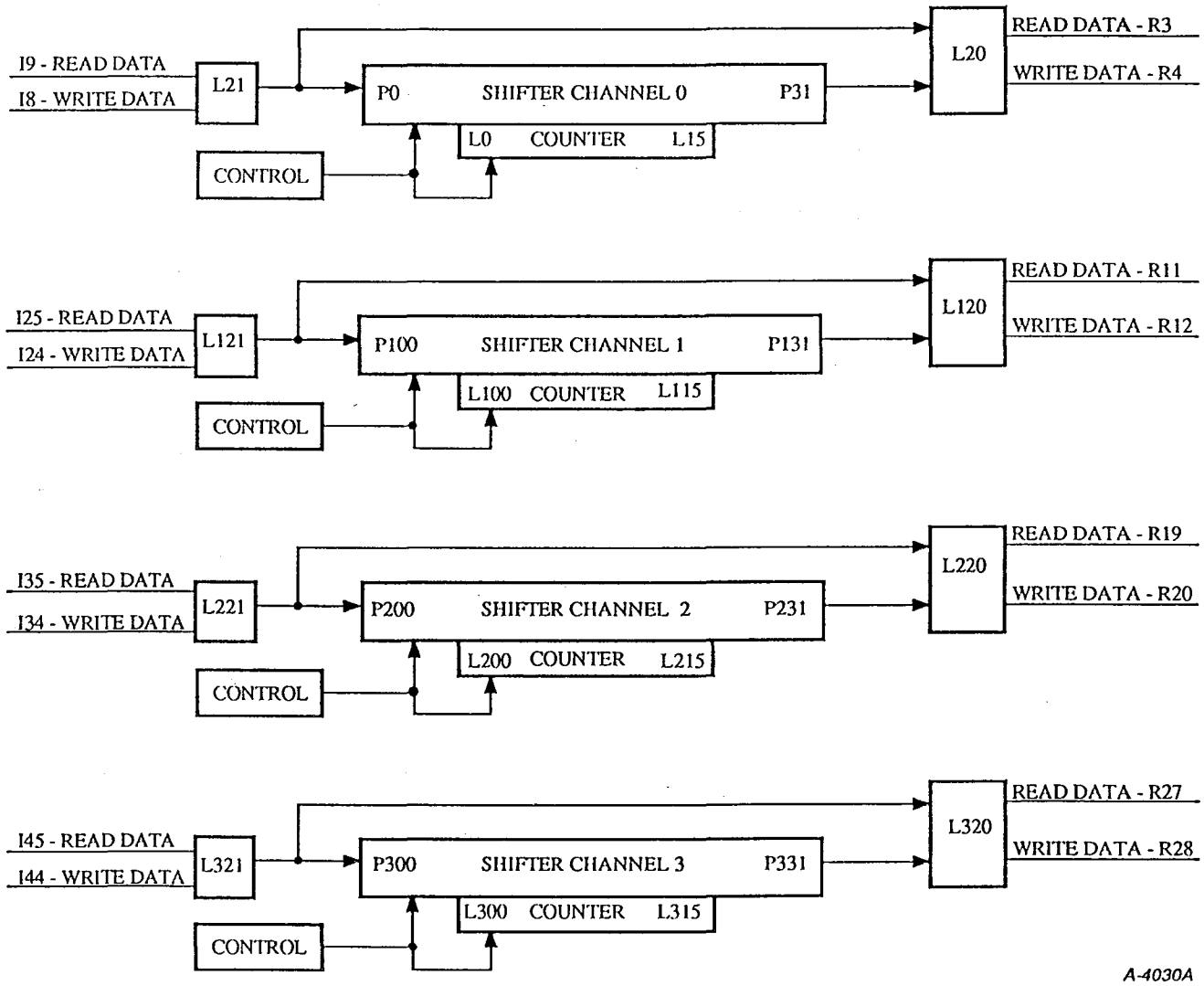
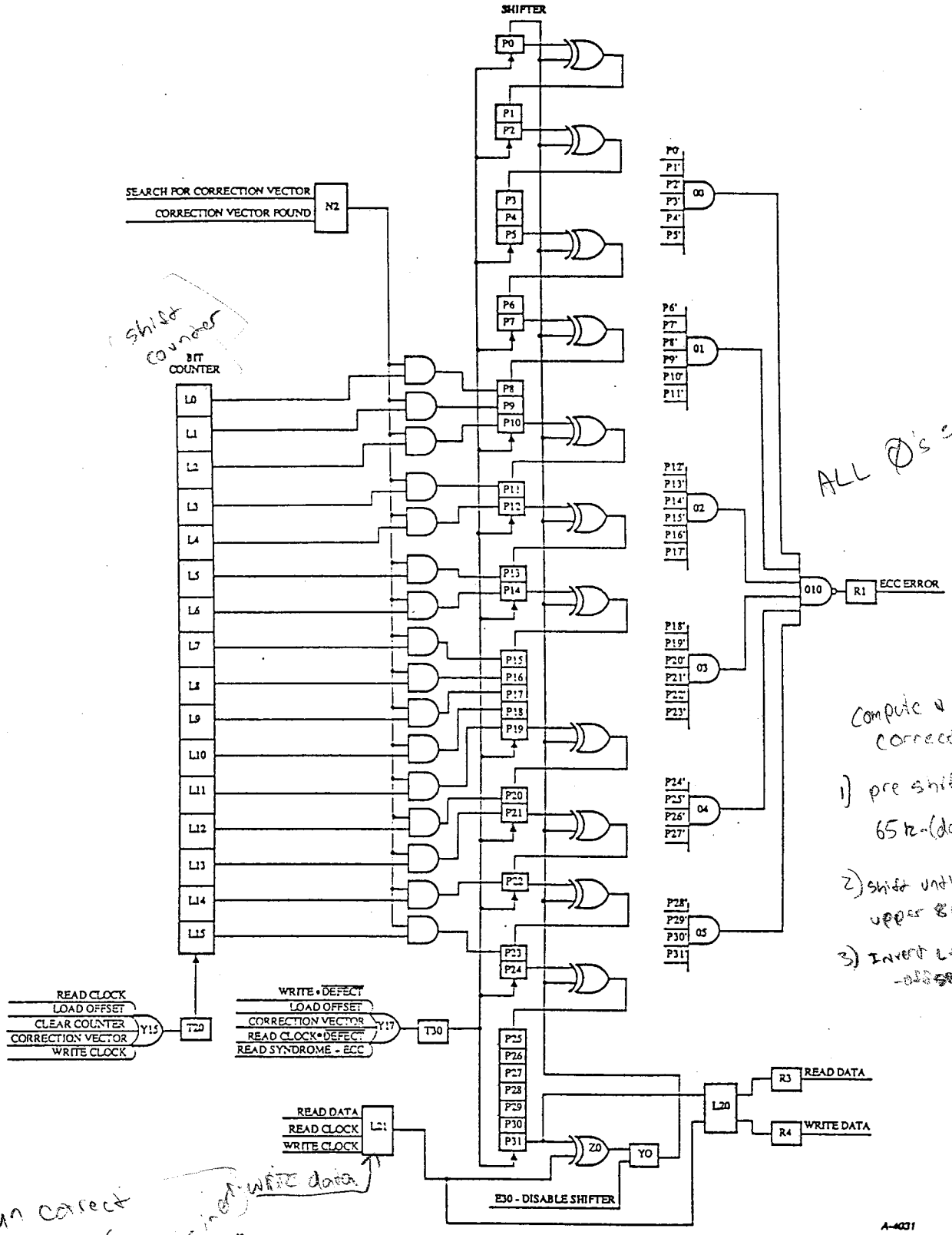


Figure 4-17. 2EK Module Correction Shifter Four Channel Block Diagram



shift counter

ALL 0's = no error

Compute & transfer correction vector

1) pre shift 65 k-(data bits + ECC

2) shift until lower 24 bits upper 8 bits = mask

3) Invert L terms → P8-P -offset

Can correct 1 to 8 bits but can detect 9 bits

2° write data

XX

mask

The mask determines which bits are in error. The mask is 8 bits wide and is contained in bits 24 through 31 of the correction vector. After the offset has determined the starting point of the mask, the mask is applied from that point 8 bits back toward the beginning of the sector. The bits that are set in the mask correspond to the bits that are in error. These bits are toggled to correct the error.

Figure 4-19 shows the mask and offset. Figure 4-20 is an example of a mask and offset and shows how these are applied to the data field.

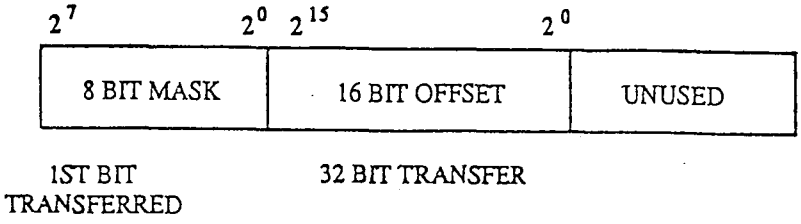


Figure 4-19. Mask and Offset

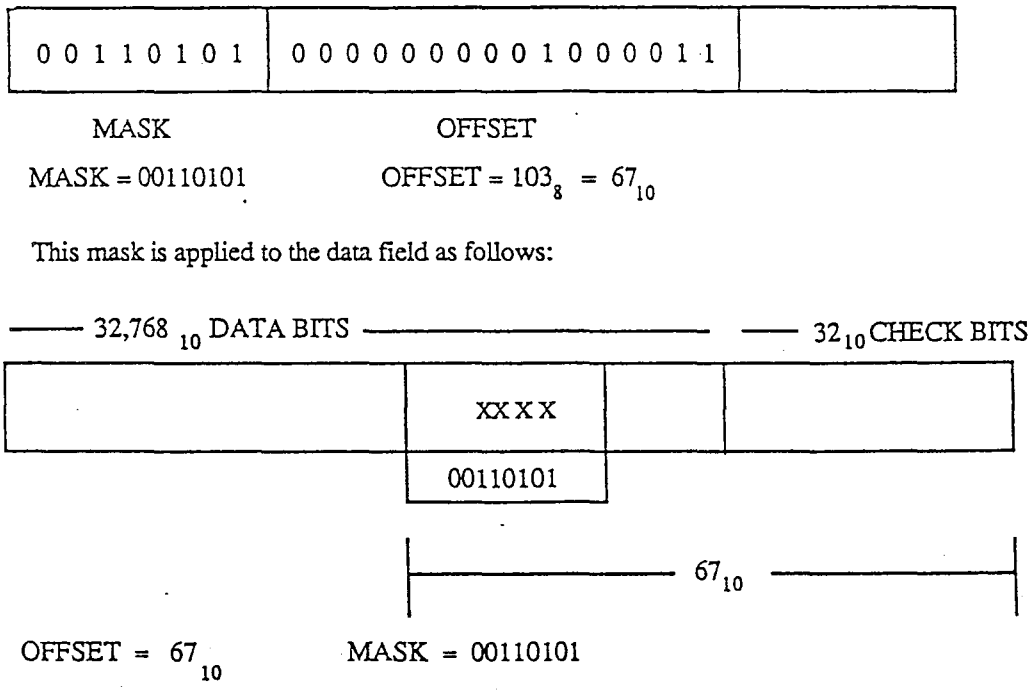


Figure 4-20. Example of a Mask and Offset

4.5.4 2EK MODULE - DEFECT DETECTION

Figure 4-21 is a block diagram of the defect detection circuitry in the 2EK module.

Defect detection is a method of handling a flaw in a sector so that the sector can be used for data storage. If a flaw has been detected in a sector when a drive is formatted, a defect parameter is written in the ID field . During a write operation, the defect parameter is read along with the ID field. As the defect parameter is read, it is loaded into terms D7 through D15 on the 2EK module. Three bits of parity (terms D4, D5, and D6) are used to check the integrity of the parameter. All 12 bits are transferred to the 2EK module through the 2EJ module, which reads and compares the ID field.

When the data field is written, the bit counter on the 2EK module increments with each data bit. At some point the upper 9 bits of the bit counter (terms L7 through L15) equal the upper 9 bits of the defect parameter (terms D7 through D15). At this point the upper 9 bits of the bit counter, the shifter, and the write data path are disabled and a 0's pattern is written over the defect area.

When a flaw is detected, its location is defined within 4 bytes. Because the flaw is only approximately defined, the defect area covers 16 bytes or 128 bits of the data area. When a sector has a defect in it, the number of bytes in the data area is increased by 16 bytes and the last gap is decreased by 16 bytes.

On a read operation, the defect is detected in the same way. The defect parameter is loaded from the ID field. When the defect area is detected, the read circuitry is disabled for 16 bytes.

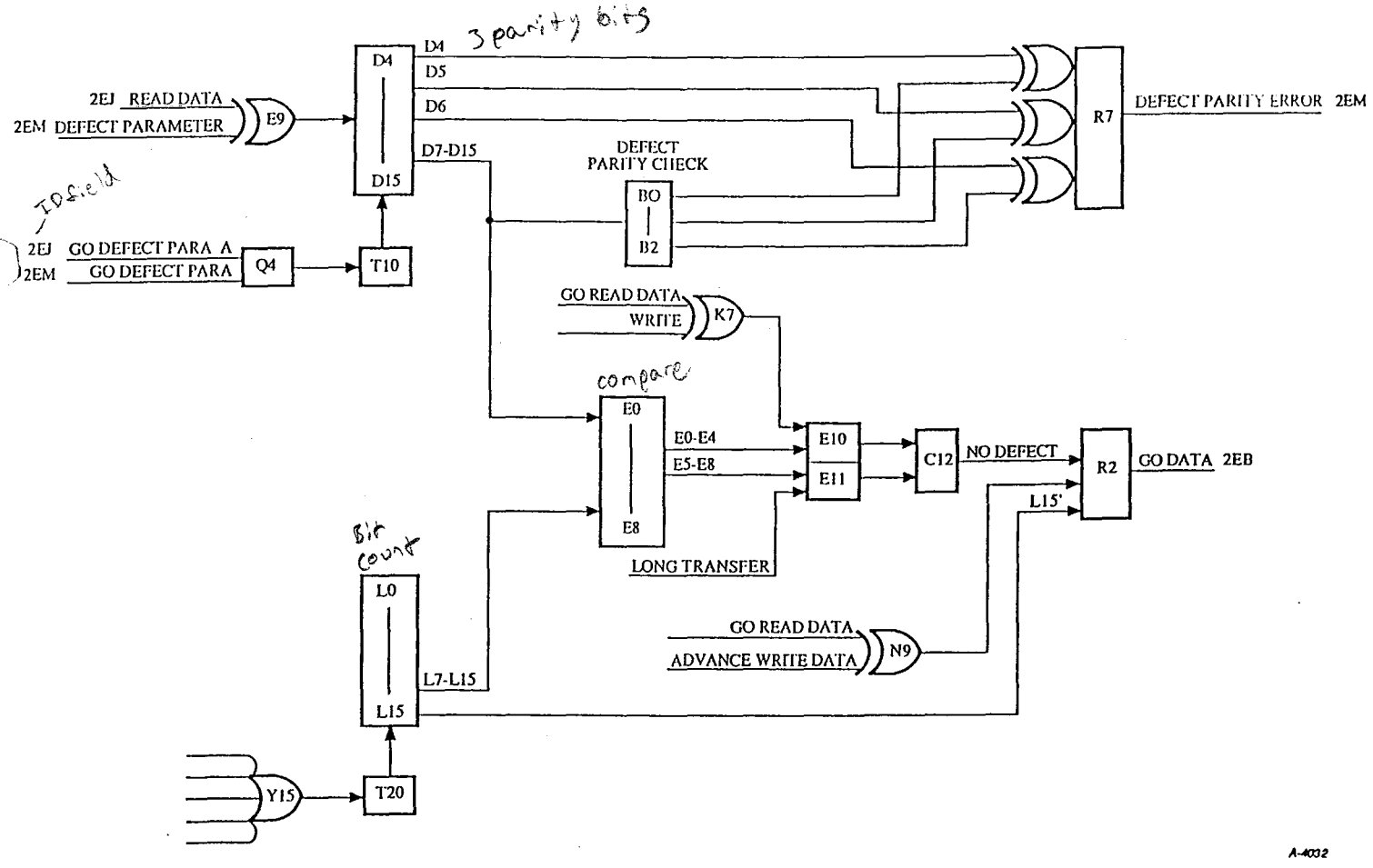


Figure 4-21. 2EK Module Defect Detection

5. DC-40 COOLING SYSTEM

The DC-40 is liquid cooled. This section describes the DC-40 cooling system. The following topics are covered:

- Theory of Operation - describes how the system functions
- Controls and Indicators - describes the controls and indicators of the cooling system.
- Procedures - describes the start-up, shut-down, and cold-start procedures and setting the superheat and subcooling.

5.1 OVERVIEW

The DC-40 cooling system draws heat from the modules of the DC-40 and delivers it to a water supply. A refrigerant acts as the intermediary, picking up heat from the modules and releasing it to the water. Two basic principles are involved in the operation of the cooling system: evaporation and condensation. The refrigerant (R-22) evaporates to absorb heat from the modules and condenses to release heat to the water supply. A large amount of heat is transferred when a change of state occurs.

Figures 5-1 and 5-2 show the components of the cooling system of the DC-40.

The DC-40 cooling system has been designed to handle the heat load generated by the DC-40 modules. The load generated by the modules cause the pressures and temperatures in the cooling system. The components of the system (the power of the compressor, the size of the expansion valve, etc.) must correspond to the load. The cooling system of the DC-40 has a capacity of two tons (see terminology below) because that amount of cooling corresponds to the load generated.

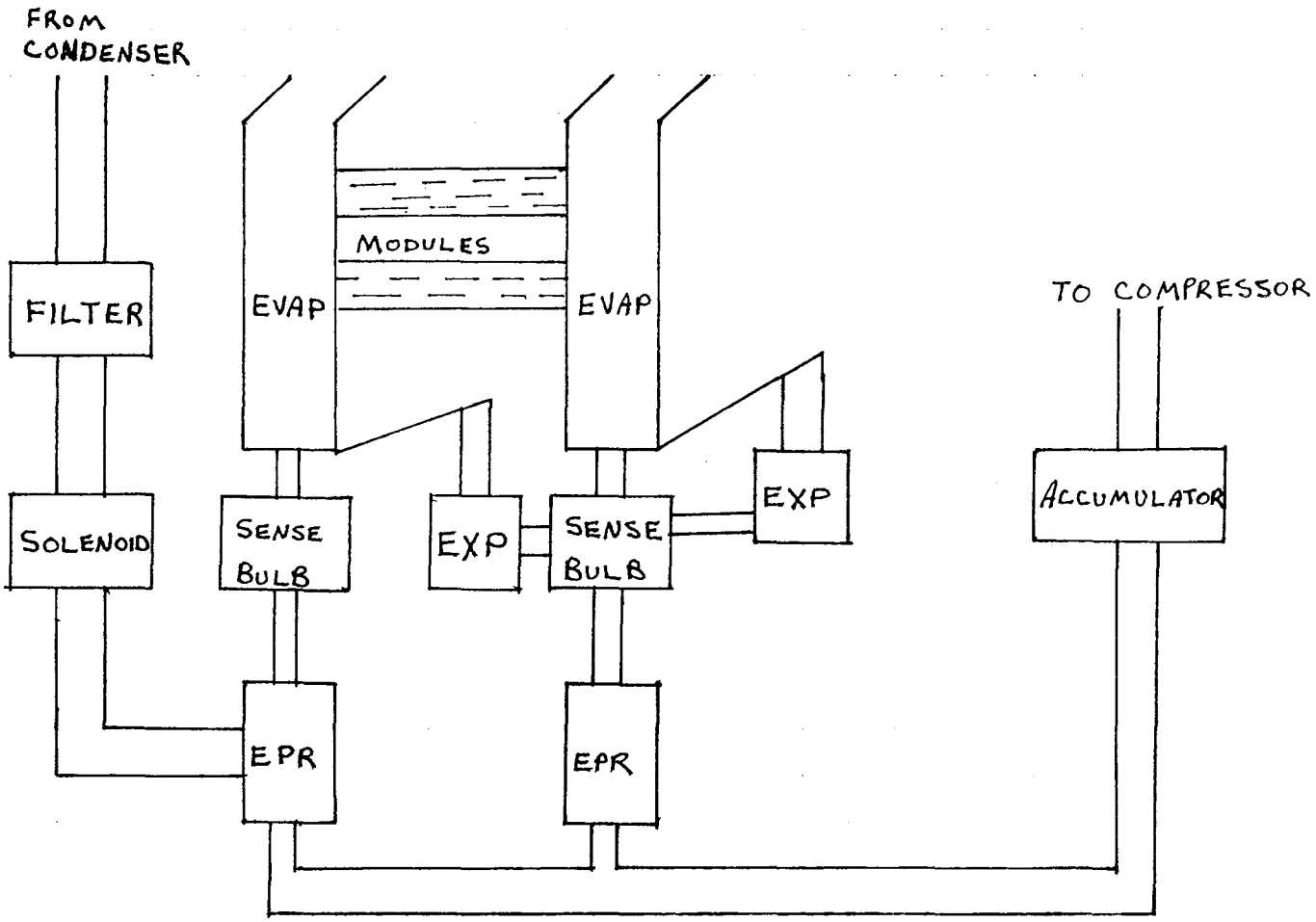


Figure. 5-1. DC-40 Cooling System - Front View

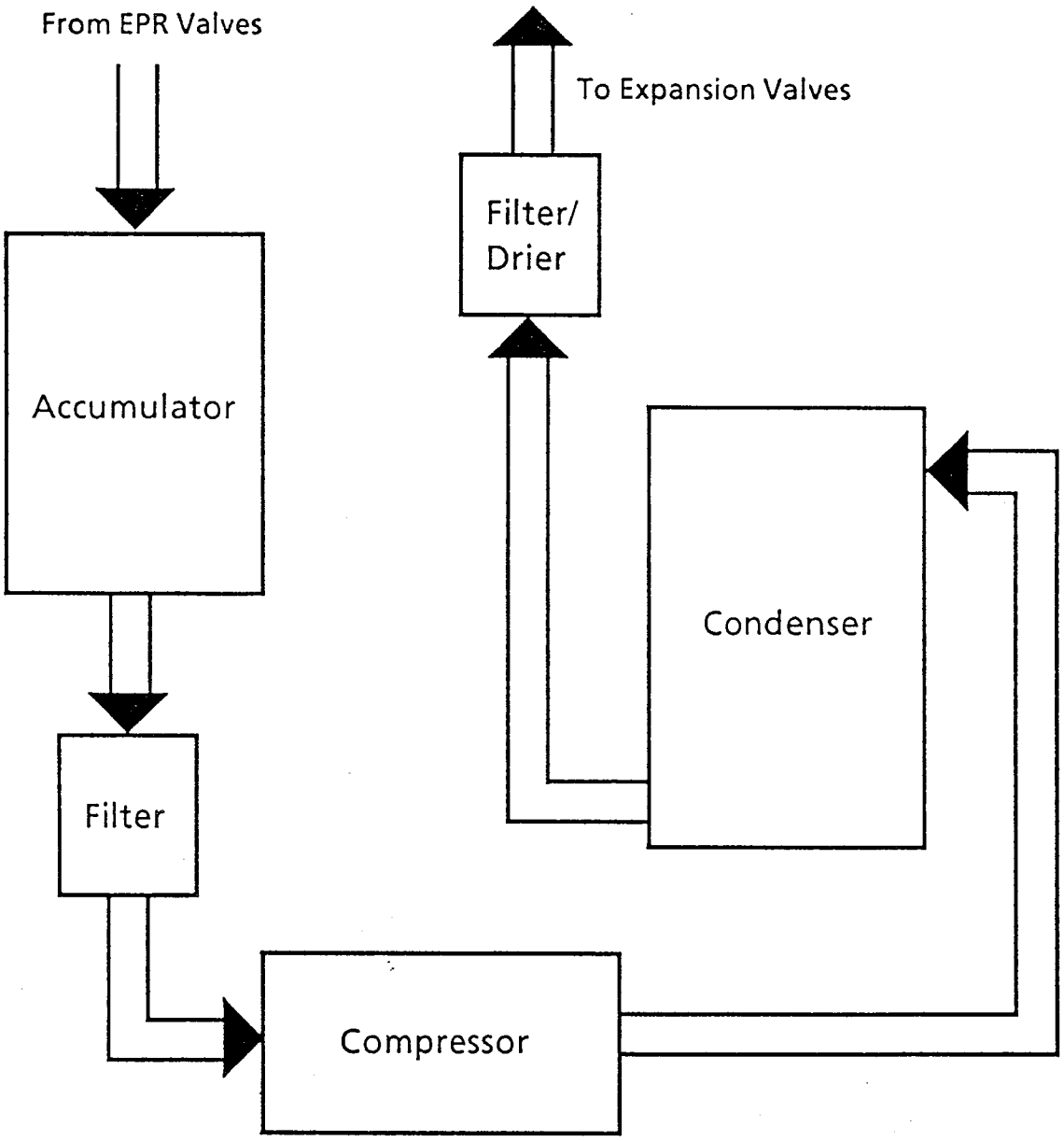


Figure 5-2. DC-40 Cooling System - Back View

5.2 TERMINOLOGY

To understand how the cooling system operates, you will need to be familiar with the following terms:

Ton - A measure of cooling capacity. One ton of cooling capacity is the amount of cooling generated by 1 ton of ice melting in 24 hours.

BTU - British thermal unit. A measure of heat. One BTU is the heat required to change the temperature of 1 lb of water 1 degree F, at 60 degrees F.

Heat of vaporization - Heat absorbed when a liquid changes to a gas.

Heat of condensation - Heat given off when a gas changes to a liquid.

Pounds per Square Inch - Psi. A measure of pressure.

Saturation temperature - Temperature at which a liquid changes to a gas and vice versa. The saturation temperature is also the boiling point temperature.

Load - Amount of heat (in BTUs) generated by the modules of the system.

Subcooling - Cooling of a ref igerant below the boiling point.

Superheating - Heating of a refrigerant above the boiling point.

Floodback - Condition that occurs when liquid refrigerant returns to the compressor.

R-22 - Refrigerant used in the DC-40 cooling system.

5.3 PRINCIPLES OF OPERATION

Figure 5-3 is a functional diagram of the DC-40 cooling system.

To understand how the cooling system works, you should be familiar with the following points:

- If pressure is increased on a gas, the temperature increases. If pressure is decreased on a gas, the temperature decreases.
- Changing the pressure on a liquid does not alter its temperature.

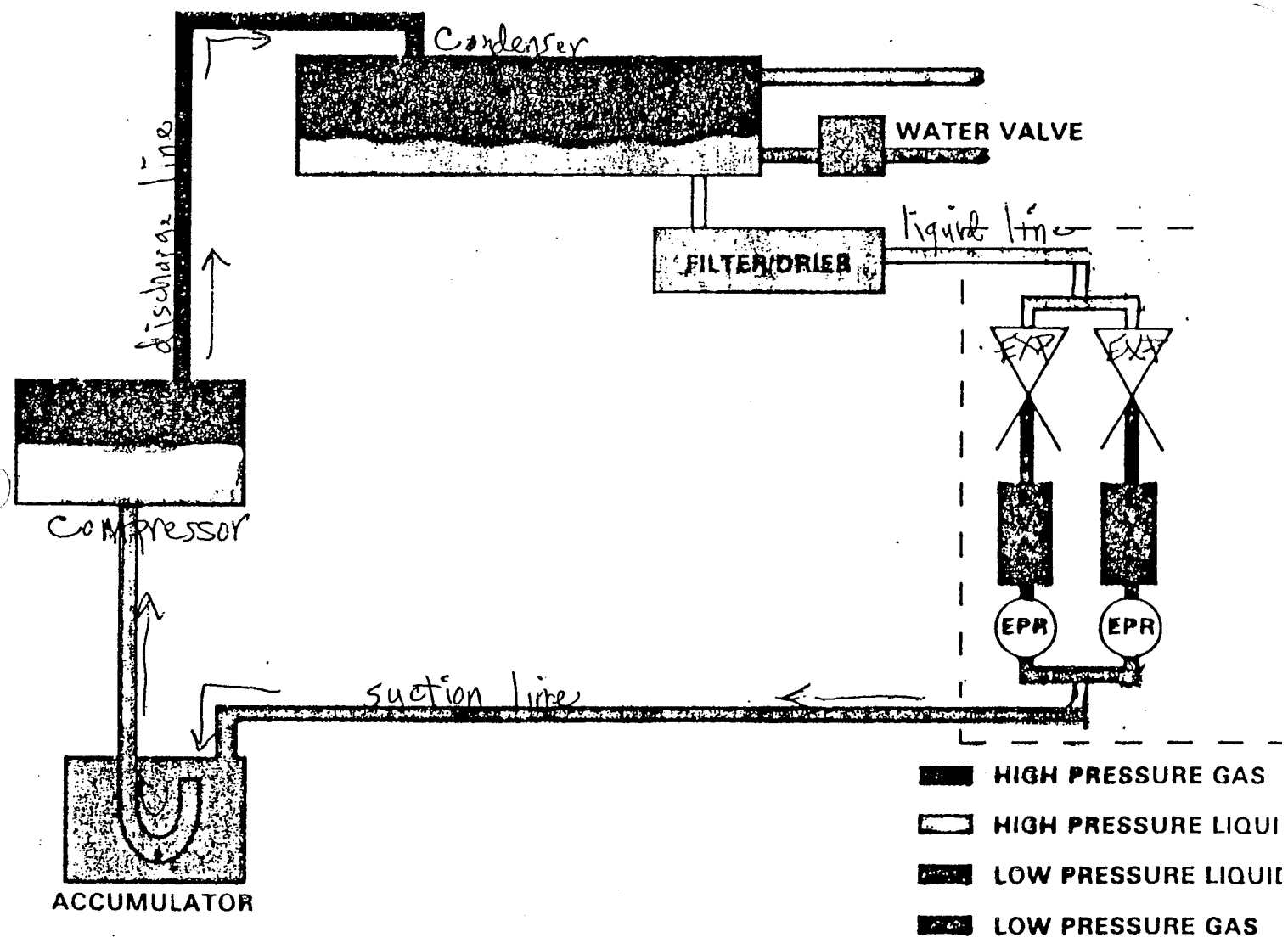


Figure 5-3. DC-40 Cooling System

- The temperature at which a liquid changes state (the saturation temperature or boiling point) depends on the pressure. A higher pressure means a higher saturation temperature; a lower pressure means a lower saturation temperature.

- When a liquid changes to a gas, it absorbs a large amount of heat from its surroundings. When a gas changes to a liquid, it gives up a large amount of heat to its surroundings.

- R-22 works as a refrigerant because it has low boiling points at low pressures. For example, at 200 Psi the boiling point of R-22 is only 100 degrees F.

- Since the boiling points of R-22 are so low at low pressures, to change it from a gas to a liquid with water as the coolant it is necessary to put it under high pressure. Increasing the pressure increases the boiling point.

- For each pressure exerted on it, a refrigerant has a change of state temperature. If the refrigerant is at the change of state temperature, it changes to a liquid if either the temperature is decreased or the pressure is increased. Similiarly, it changes to a gas if either the temperature is increased or the pressure is decreased.

- The volume of a gas is inversely proportional to the pressure exerted on it. That is, as you decrease the volume occupied by a gas, the pressure increases.

- The temperature and pressure of a gas are directly proportional. That is, as you increase the temperature of the gas, the pressure increases.

- The capacity of the compressor, the size of the expansion valve, the temperature and flow rate of the water supply are set by the heat load generated by the modules of the DC-40.

5.3.1 REFRIGERANT

For a refrigerant to be effective, it must have the following characteristics:

- It must be capable of being heated to a gas at the temperatures generated by the modules of the DC-40.

- It must be capable of being cooled by water to a liquid.

Water wouldn't work as a refrigerant in the DC-40 because its boiling point (212 degrees F) is much higher than could be reached as a result of being heated by the modules. The refrigerant must change state (that is, evaporate or condense) at temperatures within the range of the system. This leads to the most important characteristic of refrigerants: They have extremely low boiling points at normal atmospheric pressure (14.7 Psi). R-22, for example, boils at -44 degrees F at one atmosphere.

The problem to be solved in using a refrigerant like R-22 is to condense it to a liquid using water as the coolant. This can't be done if the boiling point is -44 degrees F, so the R-22 must be put under pressure. If the pressure is 200 PSI, the boiling point is elevated to 100 degrees F. Water can now be used to cool it. If pressure is then released on the refrigerant, it can readily be heated to a gas by the modules of the DC-40.

You can adjust the boiling point temperature of the refrigerant so that it is suited to the temperature of the evaporator and condenser in the system by adjusting the pressure exerted on it. The refrigerant is made to change state at the temperatures necessary for operation of the evaporator and condenser. Remember the change of state is when most of the heat is absorbed (evaporation) and released (condensation).

5.3.2 COMPRESSOR

The compressor takes in R-22 gas at low-pressure and temperature, and compresses it to a gas at a high-pressure and temperature. By compressing the gas, the boiling point of the R-22 is raised to a temperature that enables the cooling water to condense it. In the DC-40 cooling system, the R-22 gas is compressed to 200 Psi, which corresponds to a boiling point of 100 degree F.

The pressure into the compressor is called the suction pressure. The pressure out of the compressor is called the discharge pressure. The ratio of the discharge to the suction pressures determines the temperature of the discharge gas, as follows:

$$\frac{\text{discharge pressure}}{\text{suction pressure}} = \frac{\text{discharge temperature}}{\text{suction temperature}}$$

Since a compressor can only compress a gas, the suction temperature must be above the boiling point. If this is so, the discharge temperature will also be above the boiling point, though the boiling point is elevated by the increase in pressure on the gas.

The compressor is the energy source that makes the cooling system work. Heat will not travel from a lower temperature (suction gas temperature) to a higher temperature (discharge gas temperature). By supplying energy, the compressor makes this happen.

The heat load of the modules generates the suction gas. The capacity of the compressor is such that it can compress all the suction gas to discharge gas at the pressure (200 Psi) required for the condenser and evaporator to operate properly.

5.3.3 CONDENSER

The condenser is the cooling system component in which the heat of evaporation, picked up from the modules by the evaporator, is given off as the heat of condensation. In the condenser the refrigerant is cooled by a flow of water so that its temperature drops below the boiling point (100 degrees F at 200 Psi) and it condenses. The water supply carries off the heat to an external sink.

The condenser has the internal structure shown in figure 5-4.

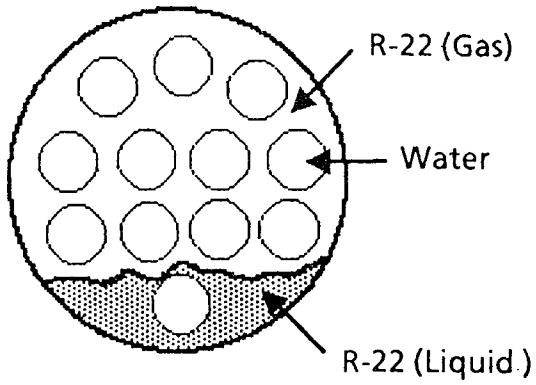


Figure 5-4. Structure of the Condenser

Cold water flows in the bottom of the condenser, travels up the tubes, and passes out at the top of the condenser. Hot R-22 gas from the compressor enters the top of the condenser and passes down between the tubes. R-22, cooled by a water supply below its boiling point, condenses and collects as a liquid at the bottom of the condenser, and passes out the liquid line.

Though it condenses to a liquid, the pressure on the R-22 refrigerant (200 Psi) does not change, so that the boiling point is also the same (100 degrees F). To ensure that a full liquid line is delivered to the expansion valve, it is required that the R-22 be cooled below the boiling point. This is called subcooling. To get the proper amount of subcooling, two factors need to be controlled:

- The proper amount of R-22 in the system.
- The proper temperature and flow rate of the water supply.

The temperature of the R-22 liquid line out of the bottom of the condenser should be the boiling point temperature less the degrees of subcooling, as follows:

```
 100 degrees F (boiling point temperature at 200 PSI)
-20  degrees F (subcooling)
 80  degrees F (liquid line temperature)
```

To get the proper amount of subcooling, the temperature and flow rate of the cooling water must be sufficient for the heat load generated by the modules. If the water cannot transfer all the heat, the discharge pressure increases, until the high pressure safety control trips, causing the compressor to stop.

5.3.4 EXPANSION VALVE

The expansion valve allows liquid refrigerant to pass into the evaporators. The DC-40 cooling system has two expansion valves, one for each evaporator. The expansion valves are designed for a full liquid line, 100 degrees F boiling point temperature (200 Psi), and 20 degrees F subcooling.

The expansion valves on the DC-40 are matched to the heat load generated by the system. That is, the expansion valves admit to the evaporators an amount of R-22 in liquid form that is precisely matched to the amount of heat the modules give off. In other words, the amount of R-22 admitted to the evaporators must be such that all of it can be evaporated to a gas by the heat of the modules. Because the heat load can change, the

expansion valves are under the control of the sense bulbs, which cause the expansion valves to open and close as necessary. As the sense bulbs heat up, they cause the expansion valve to open. As the sense bulbs cool down, they cause the expansion valves to close.

There is a rapid drop in pressure across the expansion valve into the evaporator. As a result of this, when the liquid R-22 crosses the expansion valve, it undergoes a rapid drop in its boiling point. Consequently, some of the R-22 vaporizes. (This is called the flash gas.) The R-22 that vaporizes draws most of its heat of vaporization from the liquid refrigerant, causing it to drop in temperature. Thus, the temperature in the evaporators is quite low. (The evaporators are called cold bars.)

The expansion valves determine the superheat generated within the evaporators. The superheat is the number of degrees above the boiling point to which the gaseous R-22 is heated by the modules. The DC-40 cooling system is designed for 5 to 8 degrees of superheat.

Two factors contribute to the amount of superheat generated in the evaporators:

- The heat load from the modules
- The amount of R-22 that crosses the expansion valve into the evaporator

The expansion valves admit the precise amount of liquid R-22 to the evaporators so that the heat of the modules can drive the R-22 to a gas and heat it 5 to 8 degrees F above the boiling point. The amount of R-22 in the evaporators sets the superheat, and the expansion valves regulate it. If too much R-22 is let in to the evaporators, the heat of the modules cannot drive the R-22 to the boiling point and a flooded evaporator results. If too little R-22 is let in, the evaporators overheat. The expansion valves can be adjusted to regulate the superheat.

The amount of superheat is measured at a pressure port just above the EPR valve. The pressure here corresponds to the boiling point for the gas. Five to eight degrees of superheat are necessary to ensure that the gaseous R-22 returning to the compressor does not liquify.

5.3.5 EVAPORATOR

The evaporator is the component of the DC-40 cooling system in which the heat of evaporation is absorbed from the modules by the R-22 refrigerant as it changes from a liquid to a gas. There are two evaporators in the DC-40 cooling system. Liquid R-22 enters each evaporator across an expansion valve and leaves through an EPR valve.

The heat of vaporization absorbed from the modules in the evaporator is the same amount of heat that is released to the cooling water as the heat of condensation in the condenser.

The gas that leaves the evaporators is superheated 5 to 8 degrees F above the boiling point by the heat load of the modules.

5.3.6 EPR VALVE

There are two EPR (Evaporator Pressure Regulator) valves in the DC-40 cooling system, one for each evaporator. Superheated gas from the evaporators flows through the EPR valves to the suction line.

The EPR valves maintain the pressure inside the evaporators at a predetermined value (i.e., 95 PSI). A spring inside each EPR valve holds the valve closed until the pressure reaches this value. In this way, the pressure and temperature of the gas in the evaporator can be regulated.

Since the pressure in the evaporator determines what the boiling point is, the EPR valves maintain a minimum boiling point. If the boiling point is too high (the EPR valve is closed too tight), the evaporators overheat. If the boiling point is too low (the EPR valve is too loose), the evaporators become too cold.

5.3.7 ACCUMULATOR

The accumulator is in the suction line between the evaporator and the compressor. To ensure that the R-22 in the suction line is a gas, the expansion valve is set for 5 to 8 degrees of superheat. If, because of a problem with the expansion valve, liquid R-22 returns in the suction line, the compressor could be damaged. The accumulator is in the suction line to prevent liquid R-22 from reaching the compressor.

Figure 5-5 shows the structure of the accumulator. Any liquid in the suction line falls into the accumulator. When the problem is corrected so that the suction line carries a superheated gas, the liquid in the accumulator boils off.

5.3.8 FILTER/DRIER

The filter/drier is in the liquid line between the condenser and the expansion valve. This component contains a desiccant that removes water from the refrigerant and a filter that strains foreign material from the liquid line. There is also a small filter in the suction line between the accumulator and the compressor.

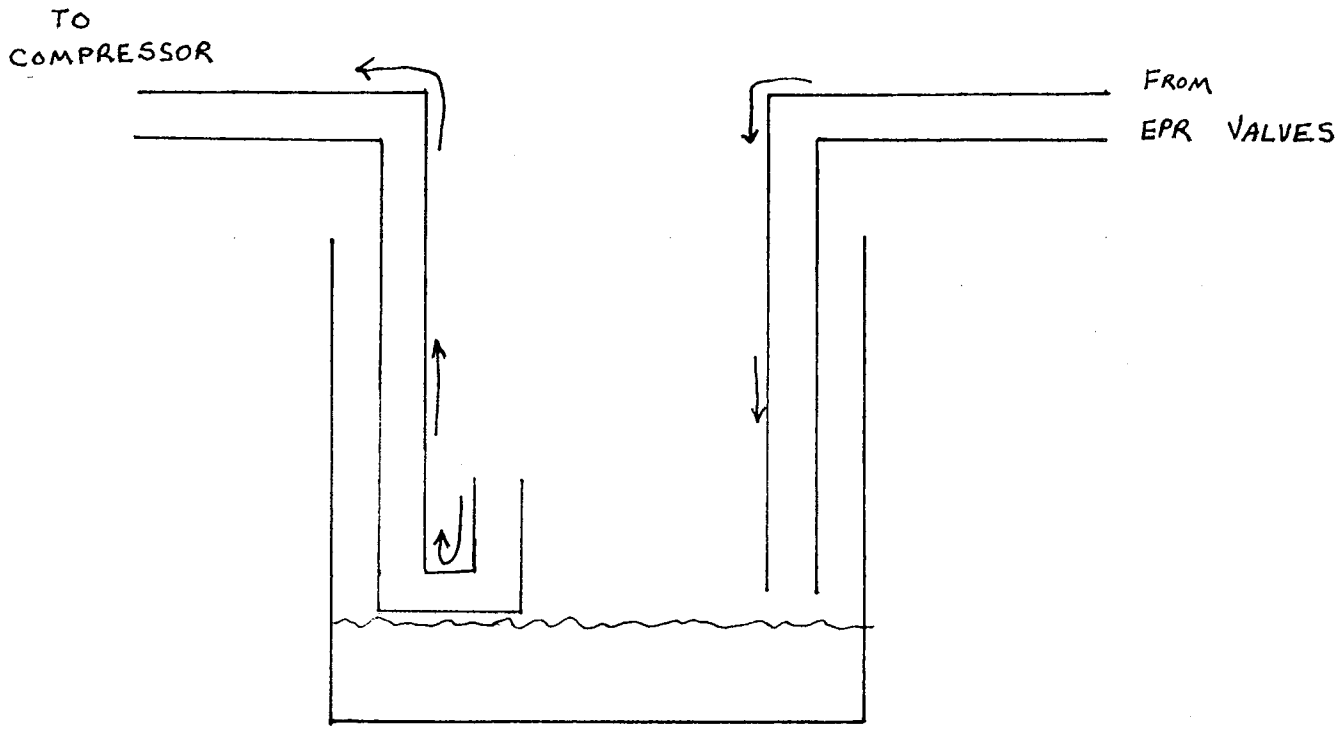


Figure 5-5. The Accumulator

5.3.9 SOLENOID VALVE

The solenoid valve is in the liquid line between the condenser and the expansion valves. It is an electrically operated valve that is either fully open or fully closed. When the system is powered on, the solenoid opens the flow of liquid R-22. When the system is powered off, the solenoid closes the flow. By closing the flow of R-22 to the evaporators, the solenoid enables the compressor to operate under pump down control which allows the compressor to operate until the pressure of the gas in the suction line drops below a specified pressure.

5.4 CONTROLS AND INDICATORS

This section describes the controls and indicators of the cooling system of the DC-40.

Figure 5-6 shows the controls and indicators of the cooling system control panel. Table 5-1 lists the functions of the cooling system controls and indicators.

Table 5-1. Cooling System Control Panel Controls and Indicators Functions

Name	Function
Solenoid By-Pass switch	When enabled, it applies power to the solenoid, even though the power switch is off.
Head-Pressure guage	Records the discharge pressure of of the compressor.
Suction pressure guage	Records the suction pressure of the gas.
High-pressure control	The high-pressure control enables you to set the maximum head pressure of the compressor (that is, the cut-out pressure). The normal high pressure setting is 275 PSI. When the pressure exceeds the setting, the compressor shuts off. It will not start until you press RESET.
Reset switch	Enables you to start the compressor after the head pressure has fallen below the high pressure setting.
Low-pressure control	The low-pressure control enables you to set the cut-in and cut-out pressures of the compressor. These are the pressures of the suction line at which the compressor turns on (cut-in) and off (cut-out).

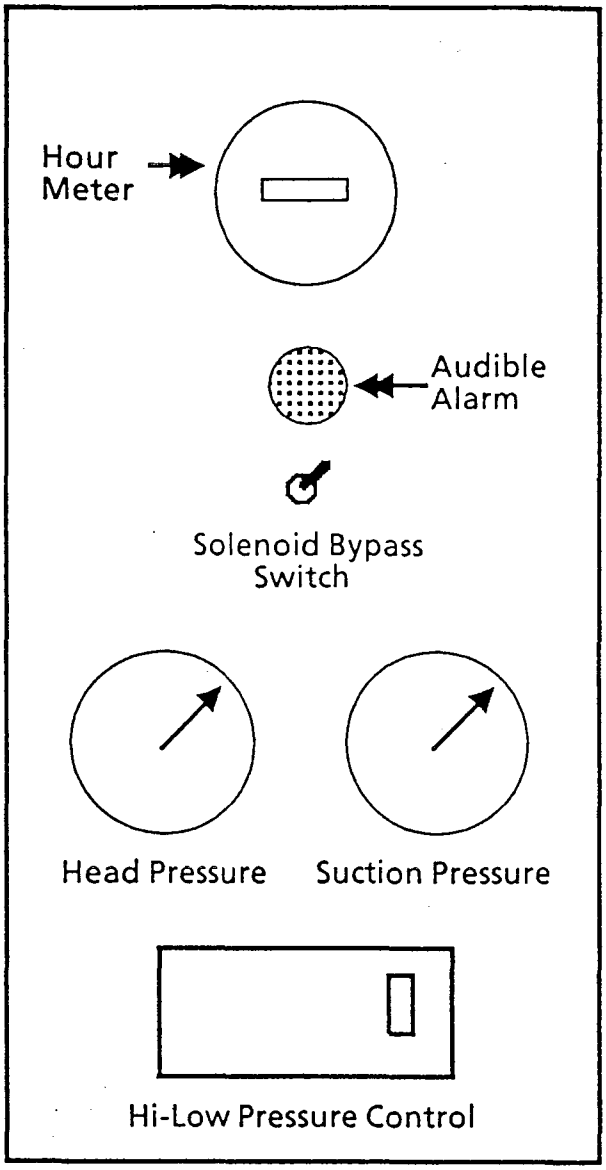


Figure 5-6. Cooling System Control Panel

Table 5-1. Cooling System Control Panel Controls and Indicators Functions (continued)

Name	Function
Low-Pressure Control (continued)	The settings are adjusted by turning the screws at the top of the gauge-box until the desired pressures are recorded on the gauge. The cut-out adjustment screw is to the left.

Table 5-2 lists the function of controls and indicators related to the cooling system that are not located on the cooling system control panel.

Table 5-2. Cooling System Controls and Indicators Functions

Name	Location	Function
Power-on switch	Front panel	Applies power to the modules. Applies power to the solenoid causing it to open and allow R-22 to flow into the expansion valve.
Power-off switch	Front panel	Removes power from the modules. Removes power from the solenoid causing it to close and stop the flow of R-22 to the expansion valve.
Pressure nozzle guage attachment	Above EPR valve	The point at which a pressure gauge can be attached to measure the pressure in the evaporators.
Sense bulb control	Above EPR valve	If this device is warm, it causes the the expansion valve to open, which allows R-22 to flow into the evaporator.
Oil Sight Glass	Front of compressor	The point at which the oil level in the the compressor can be read.

5.5 DC-40 COOLING SYSTEM START-UP PROCEDURE

Use the following procedure to start the DC-40 cooling system.

Press the power-on switch and the following sequence occurs:

1. The modules activate and generate a heat load. The solenoid is energized, allowing R-22 to flow in the liquid line.

2. Heat from the evaporators pass to the sense bulbs.

3. When the sense bulbs are warm, the expansion valve opens.

4. Pressure builds in the evaporators and causes the suction line pressure to build up.
5. When the suction pressure is equal to the cut-in pressure, the compressor starts.

5.6 COLD START PROCEDURE

If the DC-40 has been powered off for an extended period of time, the sense bulbs may not get hot enough to cause the expansion valves to open when the system is powered on. As a consequence, R-22 will not flow into the evaporators and an overtemp condition will occur. Execute the following procedure to start a cold DC-40:

1. Press the power ON switch.

2. Warm the sense bulbs by holding them in your hands.

(When the sense bulbs are warm enough, the expansion valves will open, allowing R-22 to flow into the evaporators, and the suction pressure will rise. The compressor starts when the suction pressure is equal to the cut-in pressure.)

5.7 POWER DOWN PROCEDURE

To power down the cooling system, press the power OFF switch.

//

WARNING

When powering off the DC-40, it is important to first press the POWER OFF switch on the power supply and refrigeration system control panel before turning off the COMPRESSOR and POWER SUPPLIES circuit breakers on the DC-40 power panel. The refrigeration system must be allowed to pump down (about 3 seconds) before removing all power in order to prevent damage to the compressor at start up.

//

When the power OFF switch has been pressed, the following sequence occurs:

1. Power is removed from the modules and the solenoid.

2. The solenoid closes the flow of refrigerant to the expansion valves.

3. As the last of the refrigerant in the evaporators is vaporized, the suction pressure falls off.

4. When the suction pressure falls to the cut-out pressure setting, the compressor stops.

5.8 USE OF THE SOLENOID BY-PASS SWITCH

The SOLENOID BY-PASS switch enables you to apply power to the solenoid when the system is powered down. Applying power to the solenoid causes it to open the flow of refrigerant in the liquid line causing the flow of refrigerant to the evaporators to continue and keep the suction pressure above the cut-in setting. The compressor continues to run, though the DC-40 is powered down.

When an overtemp condition occurs, execute the following steps:

1. Press the POWER OFF switch

2. Activate the SOLENOID BY-PASS switch

5.9 SUBCOOLING - MEASUREMENT AND ADJUSTMENT

The subcooling is the number of degrees below the boiling point to which the refrigerant is cooled in the condenser. For the DC-40, a subcooling of 20 degrees F must be maintained.

To measure the amount of subcooling, do the following:

1. Look at the head pressure gauge to get the pressure in the liquid line. This should be at 210 Psi.

2. Look at a pressure-temperature table for R-22 to get the boiling point temperature at the pressure observed. If the pressure is 210 Psi, the boiling point is 105 degrees F.

3. Measure the temperature of the liquid line between the condenser and expansion valve with a temperature probe.

4. The difference (boiling point minus liquid line temperature) is the amount of subcooling.

The following two factors control the amount of subcooling in the system:

1. Temperature and flow rate of the cooling water supply

2. Amount of R-22 in the cooling system

5.10 SUPERHEAT - MEASUREMENT AND ADJUSTMENT

The superheat is the number of degrees above the boiling point to which the refrigerant is heated in the evaporators. A superheat of 5 to 8 degrees F should be maintained for the DC-40.

To measure the superheat, do the following:

1. Measure the pressure at the pressure port just above the EPR valve.

2. Look at a pressure-temperature table for R-22 to get the boiling point temperature at the pressure measured.

3. Measure the temperature of the evaporator on the tubing between the EPR valve and the evaporator.

   (The difference (temperature of the evaporator minus boiling point) is the superheat.)

The superheat is controlled by adjusting the expansion valves. If the superheat is too low, the expansion valves should be closed enough to raise the superheat. If the superheat is too high, the valves should be opened.

5.11 CONDENSATION CONTROL

To hold condensation on the evaporators to a minimum, the temperature of the refrigerant in the evaporators must be above the dewpoint in the room. You control the temperature in the evaporators by adjusting the EPR valves.

The recommended dewpoint is 50 degrees F. If the suction line temperature is above this, condensation will be minimal.

6. MAINTENANCE

DD-40 PREVENTIVE MAINTENANCE INTERVALS

PMP	System	Power	Activity
W01	No	Yes	Examine error logs for previous weeks failures
Q01	No	Yes	General cleaning and inspection

PREVENTIVE MAINTENANCE PROCEDURES

DD-40 Disk Drive

PMP#	Time	
W01	15 min. +	Weekly System Log Analyze - Obtain error logs for previous weeks disk subsystem. Analyze any controller/disk failure for probable failure mode and potential maintenance action. Keep weekly printouts on file for trend analysis of failure modes.
Q01	30 min.	Drive Mechanics - Clean filters on front of the four spindles in the DD-40 drive cabinet. Inspect the drive cabinet and spindles for mechanical integrity (for loose nuts, bolts, cables, etc.) and cleanliness.

DCC2/DD-40 PREVENTIVE MAINTENANCE INTERVALS

PMP	System	Power	Activity
W01	No	Yes	Record refrigeration readings
M01	No	Yes	Column temperature measurement
M02	No	Yes	Power supply voltage measurement
M03	No	Yes	Cold bar/plate ground path measurement
S01	No	No	Torque bus leads and wedge screws
A01	No	No	Mechanical inspection

PREVENTIVE MAINTENANCE PROCEDURES

PMP	Time	
W01	30 min.	Weekly Refrigeration - Measure and record refrigeration readings on CRAY mainframe (form 1020). Only use the "Comp #1" columns for pressure and hot gas readings. Maintain a history file of the weekly refrigeration system check off sheets for trend analysis of possible failure modes.
M01	10 min.	Column Temperature Measurement - Using a fluke meter and temperature probe, measure and record the temperature of two cold bars at the top, middle and bottom of each column.
M02	10 min.	Power Supply Measurement - Using a fluke meter, measure the voltage at the center of the voltage bus bars. Compare this voltage with the panel meters. Adjust the power supply as needed. -2.00 +/- -0.01 volts -5.10 +/- -0.01 volts

PMP	Time	
M03	15 min.	Cold Bar Plate Check: 1. Verify that voltages are correct -2.00 +/- -0.01 volts -5.10 +/- -0.01 volts 2. Use a fluke meter with insulated probe tips 3. Set the meter to 200 mv dc 4. Measure the voltage from the center of the module cold plate to the CRAY mainframe cold bar, (adjacent to the module being checked). 5. Any module which has a reading over 20 mv should be identified and investigated.
S01	15 min.	Power Supply and Wedge Screw Torque Specification - Torque power supply leads and wedge screws to 120 in/oz.
A01	30 min.	DCC2/DC-40 Mechanical Inspection: 1. Power down the DCC2 cabinet. 2. Verify that all power supply and power cable connections are tight. 3. Visually inspect both the inside and outside of the DCC2 cabinet for loose screws, burnt wires and broken hardware. 4. Check for leaks on the refrigeration lines and connections in the DCC2.

7. TROUBLE-SHOOTING

This section describes how to trouble shoot the DC-40 and the DD-40. The following information is provided:

- DC-40 status codes
- DD-40 status codes
- XMD drive trouble shooting tests

7.1 STATUS CODES

There are two types of status codes; the DC-40 status codes and the DD-40 status codes. The DC-40 status codes include general and buffer status, and the DD-40 status codes include fault, sector, operating, diagnostic, and diagnostic execute status.

The following subsections describe the DC-40 and DD-40 status codes.

7.1.1 GENERAL STATUS (0014XX)

The general status codes apply to the DC-40. See table 7-1.

Table 7-1. General Status Codes

Status	Bit	Description
Sector number	2^0 - 2^3	The last sector in error or the last sector read.
Drive number	2^4-2^5	The drive with the last sector in error or the last sector read.

Table 7-1. General Status Codes (continued)

Status	Bit	Description
Channel error	2^6	A new function was received when a function was in progress. Also issued if a function 12 is decoded, because a function 12 is not used in the DC-40. Also issued if a parity error occurs.
Buffer error	2^7	Sets on a single or double-bit error. All single-bit errors are corrected by SECDED.
Unit ready	2^8	Indicates all four spindles are up to speed, the heads are loaded, and there are no faults in the spindles.
On-cylinder	2^9	Indicates that the servo has positioned the heads over the desired track without an error on any of the four drives.
Seek error	2^{10}	Indicates one of the following conditions on any of the four drives: • The spindle took too long to complete a seek • The head position is outside the data area • The spindle was commanded to seek past the highest numbered cylinder When seek error goes active, the MPU stops all servo commands. This keeps the heads at their present position. The seek error can only be cleared by a RTZ. (If more information is needed on seek error, refer to pages 1-149 to 1-150 in the Theory of Operations section of Control Data manual 83325100.)
Drive Fault	2^{11}	Indicates that one or more of the following faults occurred on any of the four drives: • Read and write fault • Write or read while off-cylinder • First seek fault • Write and write protected fault • Head select fault • Voltage fault

Table 7-1. General Status Codes (continued)

Status	Bit	Description
		See fault status under selected status for fault descriptions.
Error correction code (ECC) error	2^{12}	Indicates that the data read from the sector did not match the data written to the sector.
ID error	2^{13}	The sector ID did not match the ID stored in the registers of the 2EJ module.
Sync timeout	2^{14}	The sync byte was not found in the allotted amount of time.
Defect parity error	2^{15}	The parity bits and defect bits indicate an error in the defect field read from the disk.

NOTE

ECC error, ID error, sync timeout, and defect parity error contain the status for the last error or the last sector read.

7.1.2 BUFFER STATUS (0014XX)

The buffer status codes apply to the DC-40. See table 7-2.

Table 7-2. Buffer Status Codes

Status	Bit	Description
Double-bit error	2^6	Indicates that more than 1 bit was in error when a parcel was read from the full track buffer. This code is generated on both reads and writes.

The sector and drive number requested are given. The other bits reflect the sector and drive number.

7.1.3 FAULT STATUS (1000XX)

The fault status codes apply to the DD-40. See table 7-3.

Table 7-3. Fault Status Codes

Status	Bit	Description
Sector number	2^0-2^3	The last sector in error or the last sector read.
Drive number	2^4-2^5	The drive with the last sector in error or the last sector read.
Command error	2^6	Sets if a new function is received with a function in progress. Also sets if a function 12 is decoded, since a function 12 is not used in the DC-40.
Channel diagnostic mode	2^7	Sets when only the port is selected. The port is selected without a drive when a unit select function is issued with the lower 3 bits set. This condition is held until another unit select function is sent with bits 2^0 through 2^2 cleared to select the

Table 7-3. Fault Status Codes (continued)

Status	Bit	Description
		primary drive or set to select the shadow drive. (Pushing the RESET button also clears the bit.)
Read and write	2^8	The read gate and write gate are enabled at the same time.
Read or write and off-cylinder	2^9	Sets when the spindle is not on cylinder and it receives a read or write function.
First seek error	2^{10}	Sets if an error occurs in the initial powering on of the drive, spinning up of the spindle, or loading the heads to cylinder 0. (See page 1-148 of Control Data manual 83325100 for more information on first seek error.)
Write fault	2^{11}	A write fault is received when the following conditions occur: • Write gate with write protect • Write gate with no write clock • Write gate without write data • Open head • Write enable without arm enable
Write and write protected fault	2^{12}	A write is attempted when the drive is write protected.
Head select fault	2^{13}	Indicates that more than one head is selected.
Voltage fault	2^{14}	Voltage fault is active if +15V, -15V, +5V, or -5V is too low. Most of the logic needed to access the drive is disabled and the heads are unloaded. (See page 1-146 of Control Data manual 83325100 if more information is required.)

Table 7-3. Fault Status Codes (continued)

Status	Bit	Description
Valid status available	2^{15}	Indicates the status information is valid.

7.1.4 SECTOR STATUS (XXXXXX)

The sector status codes apply to the DD-40. See table 7-4.

Table 7-4. Sector Status Codes

Status	Bit	Description
Sector number	2^0-2^3	The last sector in error or the last sector read.
Drive number	2^4-2^5	The drive with the last sector in error or the last sector read.
Command error	2^6	Sets if a new function is received with a function in progress. Also sets if a function 12 is decoded, since a function 12 is not used in the DC-40.
Channel diagnostic mode	2^7	Sets when only the port is selected. The port is selected without a drive when a unit select function is issued with the lower three bits set. This condition is held until another unit select function is sent with bits 2^0 through 2^2 cleared to select the primary drive or set to select the shadow drive. (Pushing the RESET button also clears the bit.)

Table 7-4. Sector Status Codes (continued)

Status	Bit	Description
Sector count	2^8-2^{15}	This is a sector count from the drive. It does not represent the last sector read or the sector causing the error.

7.1.5 OPERATING STATUS (07XXXX)

The operating status codes apply to the DD-40. Table 7-5 lists the contents of the accumulator or status register 1. (The contents of status register 1 are passed to the accumulator.) Table 7-6 lists the operating status codes (that is, bits 2^8 through 2^{14} of the accumulator).

Table 7-5. Operating Status Codes (Bits 2^0 through 2^{15}).

Status	Bit	Description
Sector number	2^0-2^3	The last sector in error or the last sector read.
Drive number	2^4-2^5	The drive with the last sector in error or the last sector read.
Command error	2^6	Sets if a new function is received with a function in progress. Also sets if a function 12 is decoded, since a function 12 is not used in the DC-40.
Channel diagnostic mode	2^7	Sets when only the port is selected. The port is selected without a drive when a unit select function is issued with the lower three bits set. This condition is held until another unit select function is sent with bit 2^0 through 2^2 cleared to select the primary drive or set to select the shadow drive. (Pushing the RESET button also clears the bit.)

Table 7-5. Operating Status Codes (Bits 2^0 through 2^{15}) (continued)

Status	Bit	Description
Status codes	2^8-2^{14}	The codes in table 4-6 are listed in two ways: • Interface status code - the code (in octal) returned in status register 1 when you enter a status select code of 10001. • Diagnostic display code - the code (in hexadecimal) shown on the HDA front panel for a single drive within the DD-40 cabinet.
	2^{15}	Indicates the status code is valid.

Table 7-6. Operating Status Codes (Bits 2^8 through 2^{14})

Interface Status Code (octal)	Diagnostic Display Code (hex)	Status Description
100	00	Drive is ready and on-cylinder
101	01	Unloading heads
102	02	Stopping motor
103	03	Motor stopped okay
104	80	Fault was set before move - no move made
105	90	Recovered from speed loss, set seek error, dummy Return To Zero (RTZ) active
106	A1	Unable to unload heads before load - fault became active
107	07	Motor start in progress - no jog
110	08	Motor start in progress - with jog
111	09	Up to speed too soon - motor stopped
112	0A	Up to speed took too long - stop and try again
113	0B	Up to speed took too long - sensor fault

Table 7-6. Operating Status Codes (Bits 2^8 through 2^{14}) (continued)

Interface Status Code (octal)	Diagnostic Display Code (hex)	Status Description
114	0C	Too many start failures - no more tries
115	0D	Too many start failures - sensor fault
116	0E	Motor speed too fast
117	0F	Motor speed too slow
120	10	Speed loss recovery with seek error - no dummy RTZ
121	11	Unloading heads during speed loss recovery
122	12	Stopping motor during speed loss recovery
	FAULT DETECTED BEFORE SEEK ERROR WAS SET:	
123	A2	Fault after retract was set
124	A5	Demodulator active too late
125	A6	Cylinder counter time-out
126	A7	Fault after load complete
127	A8	Code 22 and too many retries
	DURING RECOVERY FROM SPEED DROP:	
130	18	Motor start in progress - with jog
131	19	Speed akay too soon - motor stopped
132	1A	Up to speed took too long - motor stopped
133	1B	Up to speed took too long - sensor fault
134	1C	Too many start failures - no more tries
135	1D	Too many start failures - sensor fault
136	1E	Speed too fast - programmable timer
137	1F	Speed too slow - programmable timer
140	AB	Code 25 and too many interrupts - fault before seek error
141	21	No heads unloaded signal before first load
142	22	Fault after retract set during load
	FAULT BEFORE SEEK ERROR:	
143	AC	Code 26 and too many attempts
144	AD	Code 27 and too many attempts
145	25	Demodulator active timeout during load
146	26	Cylinder counter timeout during load
147	27	Fault set after load complete
150	28	Code 22 and too many attempts

Table 7-6. Operating Status Codes (Bits 2^8 through 2^{14}) (continued)

Interface Status Code (octal)	Diagnostic Display Code (hex)	Status Description
	FAULT AFTER SEEK ERROR:	
151	B0	Cannot move in from outer guard band
152	B1	Demodulator Active signal lost
153	2B	Code 25 and too many attempts
154	2C	Code 26 and too many attempts
155	2D	Code 27 and too many attempts
156	2E	Sequence power delay
157	2F	Backup into outer guard band - fault before seek error
160	30	Cannot move in from outer guard band - RTZ
161	31	Demodulator Active signal lost - RTZ
162	B5	Timeout during RTZ turnaround and move out of guard band with fault set
163	33	Timeout during backup - Return To Zero
	TIMEOUT WITH FAULT DETECTED:	
172	B6	Out of guard band too soon
173	B7	Find cylinder pulse on track 1
174	B8	Find fine enable
175	B9	Settle in on track zero
	INNER GUARD BAND AND FAULT BEFORE SEEK ERROR:	
176	C0	During move
177	C1	During on-cylinder routine
	INNER GUARD BAND:	
200	40	During move
201	41	During on-cylinder routine
202	42	On track
	OUTER GUARD BAND:	
203	43	During move
204	44	During On-cylinder routine
205	45	On track
206	46	Seek timeout

Table 7-6. Operating Status Codes (Bits 2^8 through 2^{14}) (continued)

Interface Status Code (octal)	Diagnostic Display Code (hex)	Status Description
	CANNOT STOP ON TRACK:	
207	47	Too long to get on-cylinder sense
210	48	Demodulator active signal lost
211	49	Too many cylinder pulses
212	4A	Too many on-cylinder sense dropouts
	ON TRACK:	
213	4B	Lost on-cylinder sense
214	4C	Lost demodulator active
215	4D	Illegal cylinder address
216	4E	Voltage fault while on-track
217	C2	Inner guard band detected while on-track with fault
220	50	Recovering from low voltage (Vcc) reset
221	51	Recovering from MPU hang reset
222	52	Recovering from low voltage (Vcc) and speed drop
223	53	Recovering from MPU hang reset and speed drop
	FOUND OUTER GUARD BAND WITH FAULT SET:	
224	C3	During move
225	C4	During on-cylinder
226	C5	During on-track
227	C6	Seek timeout after fault
230	58	Non-maskable interrupt
231	59	Software interrupt
232	5A	Programmable timer failed
233	5B	Too many faults or over temperature
234	5C	Fan fault
235	5D	Seek error during scan
236	C7	Too long to get on-cylinder sense - fault set
237	5F	PIA test failed
240	60	Servo test failed - RTZ
241	61	Servo test failed - 1 track
242	62	Servo test failed - calibrate
243	63	Servo test failed - maximum track

Table 7-6. Operating Status Codes (Bits 2^8 through 2^{14}) (continued)

Interface Status Code (octal)	Diagnostic Display Code (hex)	Status Description
244	64	Calibrate values do not compare
245	65	Single track seek time is too long
246	66	Single track seek time is too short
247	67	Maximum track seek time is too long
250	68	Maximum track seek time is too short
251	69	Incorrect pre-seek status
252	6A	No speed signal during seek test
	RESERVED OR UNDEFINED:	
253	6B	
254	6C	
255	6D	
256	6E	
257	6F	
260	70	Self test complete
261	71	Fan on or not over temperature
262	72	EXECUTE switch will not release
DURING ON CYLINDER ROUTINE WITH FAULT SET:		
263	C8	Demodulator Active signal lost
264	C9	Too many cylinder pulses
265	CA	Too many cylinder sense dropouts
	WHILE ON TRACK WITH FAULT:	
266	CB	Lost on-cylinder sense
267	CC	Lost Demodulator Active signal
270	CD	Illegal cylinder address
271	CE	Voltage fault
	DUMMY RETURN TO ZERO ACTIVE:	
272	D0	Recovering from Vcc reset
273	D1	Recovering from MPU hang reset

Table 7-6. Operating Status Codes (Bits 2^8 through 2^{14}) (continued)

Interface Status Code (octal)	Diagnostic Display Code (hex)	Status Description
	RESERVED OR UNDEFINED:	
274	7C	
275	7D	
276	B3	Timeout during RTZ - fault before seek error
277	7F	Undefined

7.1.6 DIAGNOSTIC STATUS (1XXXXX)

The diagnostic status codes apply to the DD-40. See table 7-7.

Table 7-7. Diagnostic Status Codes

Status	Bit	Description
Sector number	2^0-2^3	The last sector in error or the last sector read.
Drive number	2^4-2^5	The drive with the last sector in error or the last sector read.
Command error	2^6	Sets if a new function is received with a function in progress. Also sets if a function 12 is decoded, since a function 12 is not used in the DC-40.

Table 7-7. Diagnostic Status Codes (continued)

Status	Bit	Description
Channel diagnostic mode	2^7	Sets when only the port is selected. The port is selected without a drive when a unit select function is issued with the lower 3 bits set. This condition is held until another unit select function is sent with bit 2^0 through 2^2 cleared to select the primary drive or set to select the shadow drive. (Pushing the RESET button also clears the bit.)
Field replaceable unit	2^8-2^{11}	This status shows 1 of 15 field replaceable parts that is the most likely failing drive part. The parts and their corresponding codes are listed below. This status indicates the most likely failing part after evaluating the status and fault history.
	2**15	Indicates that the status information is valid.
	Code / Part	
	0001 Power supply	
	0010 Control board	
	0011 Power amplifier	
	0100 Drive motor	
	0101 Read/write board	
	0110 Module	
	0111 Cooling fan	
	1000 I/O board	
	1001 Operators panel	
	1010 Mother board	
	1011 Actuator unlocking solenoid	
	1100 Belt	
	1101 Diagnostic display	
	1110 HDA interface board	
	1111 Air filter	

7.1.7 DIAGNOSTIC EXECUTE STATUS

The diagnostic execute status codes apply to the DD-40. See table 7-8.

Table 7-8. Diagnostic Execute Status Codes

Status	Bit	Description
	2^{15}	This bit starts the following series of servo tests: • RTZ • Single track seek • Servo recalibrate • Maximum seek Once the diagnostic has started it should not be interrupted. It will stop when an error is detected or when the tests have been completed.
	2^{0}-2^{7}	Same as fault status. See page 4-4.
	2^{8}-2^{14}	Set to zero.

7.2 XMD TROUBLE SHOOTING

The trouble analysis section of Control Data Corporation (CDC) manual 83325460 (volume 2) has two parts that are useful as an aid to trouble shooting the XMD drives. The first part provides a flowchart as an aid to trouble shooting. The second part explains the meanings of the fault LEDs and tells how to use the STEP and EXCE switches on the front of the drive. The trouble shooting flow charts reference procedures for electrical checks and adjustments (procedures 4101 to 4501) and repair and replacement (procedures 5101 to 5309). The procedures for electrical checks and adjustments are described in section 4 of the CDC manual. The procedures for repair and replacement are described in section 5 of the CDC manual.

The following trouble shooting flowcharts are provided in the CDC manual:

- TSP1 - Power check: Provides an overall check of drive power.
- TSP2 - ±5 V check: Describes how to isolate problems in the ±24 V leads.
- TSP3 - ±24 V load check: Describes how to isolate problems in the ±24 V loads.
- TSP4 - First seek check: Provides possible causes for the drive failing to successfully complete a first seek.
- TSP5 - Direct or RTZ seek check: Provides possible causes for the drive failing to successfully complete a direct or RTZ seek.
- TSP6 - Write check: Provides information for isolating the cause of write errors.
- TSP7 - Read check: Provides information for isolating the cause of read errors.
- TSP8 - Address mark check: Provides possible causes for read or write address mark problems.

The second part of the trouble analysis section of Control Data manual 83325460 (starting on page 3-20) explains the meanings of the fault LEDs and tells how to select and execute 18 different diagnostics by using the step and execute switches on the front of the drive. This part also defines the status codes (00 through FF) and gives a description, probable causes, and actions to be taken when trouble shooting.

Table 7-9 describes the switches and indicators on the XMD drives.

Table 7-9. XMD Drive Switches and Indicators Functions

Switch/Indicator	Description
Diagnostic mode switch	Used to place the unit in diagnostic mode and disables the interface (UP position). The diagnostic mode indicator lights when the switch is set to diagnostic mode. Setting the switch to the DOWN position permits normal controller selection on the interface.

Table 7-9. XMD Drive Switches and Indicators (continued)

Switch/Indicator	Description
Diagnostic step switch (STEP)	Used to step the status/diagnostic fault display pattern from 0 to F. Holding the switch down causes causes the numbers to increment continuously and wrap around from zero to F. Refer to the diagnostic execute switch. Note: the switch must be pressed for a minimum of 400 milliseconds to activate.
Diagnostic execute switch (EXEC)	Used to enter values in memory. The entries permit test selection, entry of test parameters, and test deselection. The switch must be pressed for a minimum of 400 milliseconds to activate.
Status/diagnostic fault display	Used to display current status when the unit is operating in normal mode or diagnostic options and error codes when operating in diagnostic mode.
Diagnostic mode indicator	Indicates that the drive is in diagnostic mode.
First seek indicator	Indicates that the drive failed a first seek/load attempt.
Read or write and not on-cylinder indicator	Indicates that read or write conditions existed during a seek operation (an off cylinder condition).
Write indicator	Indicates that a write fault occurred.
Read and write indicator	Indicates that a write and read command were active simultaneously.
Voltage indicator	Indicates that a below normal voltage condition occurred.
Head select indicator	Indicates a multiple head selection condition occurred.

When cylinder logging has been enabled through test 10, the fault indicators do not reflect fault conditions. Disregard fault indicators until cylinder logging has been disabled through test 0F.

7.2.1 Test Selection Procedure

Turning the diagnostics mode switch ON causes 00 to be displayed in the status/diagnostic fault display LEDs. Pressing the STEP switch after diagnostic mode selection allows the operator to increment the least significant (rightmost) display character. Once the desired character is displayed, the operator must press the execute switch to enter the character into memory.

This procedure must be repeated for the most significant character. Pressing the EXEC switch after entering the test number in memory initiates test execution, except in those instances where the test requires additional parameter entries. A description of the parameter entries is included with the corresponding test description. After test completion, test 00 is enabled (00 is displayed). To determine if an error occurred, the operator must turn the diagnostic mode switch to OFF and observe the display, or execute diagnostic test 00.

7.2.2 Test Descriptions

The diagnostic tests for the XMD spindles are listed in table 7-10. They are described in the sections following the table.

Table 7-10. Diagnostic Tests

Test Number	Test
00	Display status/error log
01	Display fault log or cylinder log
02	Perform MPU initialization
03	Switch display test
04	Calculate four most likely failed field replaceable units
05	Servo test
06	Clear status/error log
07	Clear fault log

Table 7-10. Diagnostic Tests (continued)

Test Number	Test
08	Direct seek
09	Random seek
0A	Display/alter load delay
0C	Display EPROM part number
0D	Load cylinder sddress
0E	Return to Zero
0F	Display cylinder log
10	Enable cylinder log
11	Disable over temperature fault
12	Enable over temperature fault

7.2.2.1 Test 00 - display status/error code log

This test displays the 16 most recently generated status/error codes. After test selection, the display provides a pointer to a memory location in the range of 20 to 2F. The pointer address minus one contains the last status/error condition detected. Pressing the STEP switch repeatedly allows the operator to display the contents of these locations starting at location 20. After displaying location 2F, the display returns to the pointer. The current status is contained in the location preceding the pointer. At the completion of a successful spindle power up operation, the expected contents are as follows: 70, 71, 02, 03, 2E, 07, 08, with 00 in all remaining locations. Refer to the description of test 02 to determine the expected contents of the log when test 00 is preceded by test 02. The operator must press the EXEC switch to end the test. If a drive has an error, the status codes can be looked up in the trouble analysis section of CDC manual 83325460 for the definition, probable cause, and corrective action.

Figure 7-1 is an example of a display sequence.

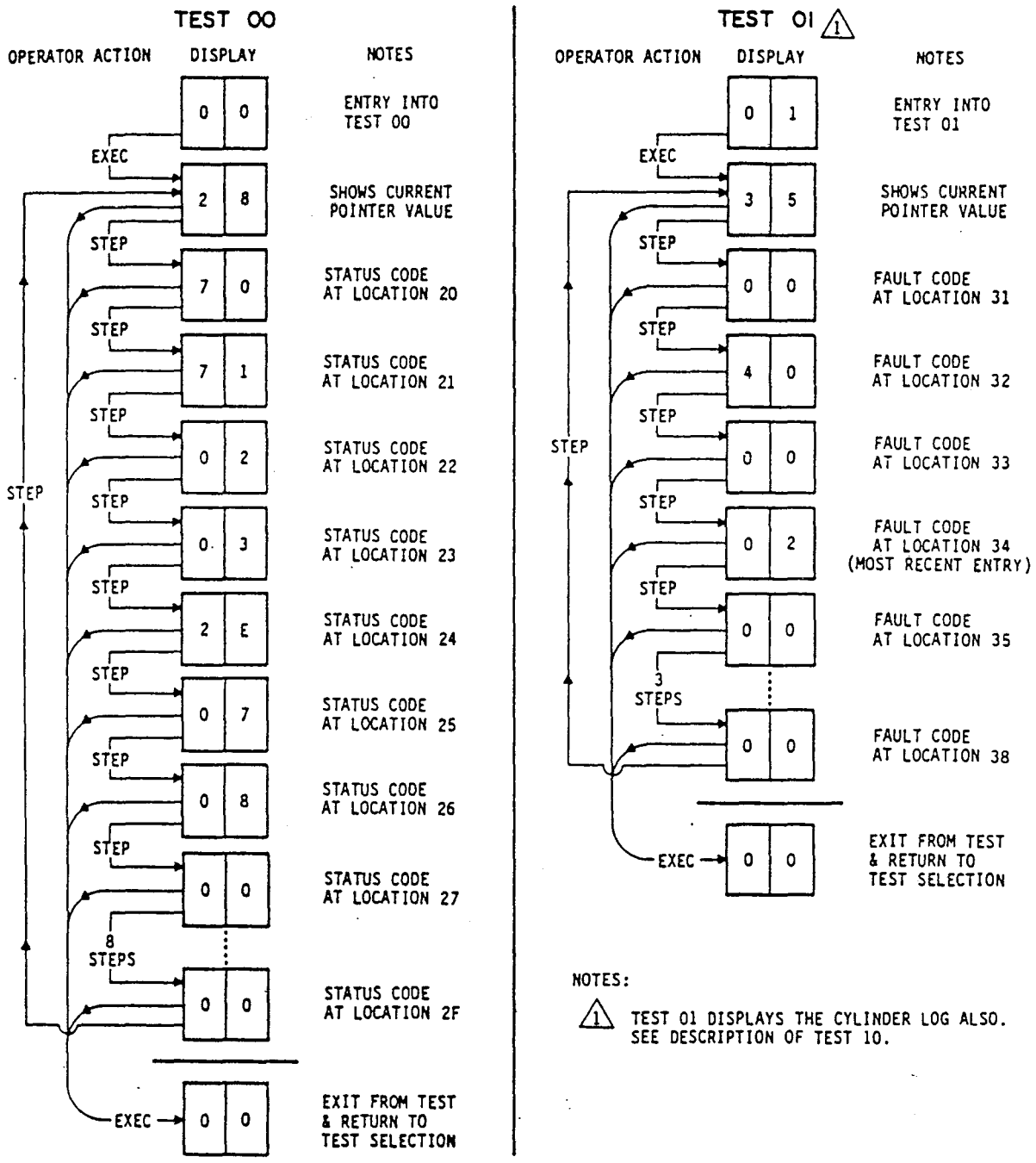


Figure 7-1. Display Sequence Examples

7.2.2.2 Test 01 - Display fault log or cylinder log

This test displays either the eight most recently generated fault conditions or the cylinder addresses of the last four seeks completed. After power is applied to the drive or test 0F is executed, test 01 displays the fault conditions. After test 10 is executed, test 01 displays cylinder addresses. Refer to the description of test 10 for instructions on using the cylinder log. The following paragraph discusses uses of the fault log.

Immediately after test selection, the display provides a pointer to a memory location in the range 31 through 38. (The pointer address minus one contains the last fault condition detected.) Pressing the STEP switch repeatedly allows the operator to display the contents of these locations starting at location 31. After displaying location 38, the display returns to the pointer. The current fault is in the location preceding the pointer. The operator must press the execute switch to end the test. Table 7-11 defines each bit of the fault byte.

Table 7-11. The Fault Byte

Bit	Description
0 (LSB)	Not used (01)
1	Voltage fault (02)
2	Write fault (04)
3	Read/write fault (08)
4	(Read/Write) off cylinder fault (10)
5	Head select fault (20)
6	First seek fault (40)
7 (MSB)	Not used (80)

7.2.2.3 Test 02 - perform MPU initialization

This test re-executes the MPU initialization procedure. If the spindle motor is operating, the test also re-executes the first seek operation (spindle motor is not recycled). At the conclusion of the initialization, the display returns to test selection (00 displayed).

The test 00 display of a successful initialization, occurring as a result of test 02, is determined by the condition of the drive prior to the initialization routine. If the spindle motor was stopped during the initialization, the pointer is set to 24 and the operator must continuously press the STEP switch to display the contents of the status/error log. The expected contents are as follows: 70, 71, 02, 03, with 00 in all remianing locations. If the spindle was turning when the initialization was started, the pointer is set to 24 and the operator must continuously press the STEP switch to display the contents of the status/error log. The expected contents are as follows: 70, 18, D1, 51, with 00 in all remaining locations.

7.2.2.4 Test 03 - switch display

This test contains two parts. Immediately after test selection, the display alternates between EE and 11, and also lights all of the fault indicators. This is repeated 10 times. The drive remains in test 03 until the EXEC and STEP switches are pressed simultaneously.

The operator may individually test the switches and test jumpers as follows:

Diagnostic mode	Head select fault and diagnostic mode.
LOCAL/REMOTE and START switches	In local mode, the write fault LED is lit, and the read/write fault LED lights when the START switch is pressed. In remote mode, the write fault LED lights when the controller has issued a pick and hold sequence. With the pick and hold sequence active, the read/write fault LED lights when the START switch is pressed.
Fault Clear	Voltage fault.
Servo Test Jumper	Read or write and not on cylinder fault. Note: Jumper J80 pins 10 and 13 on VDX board.
EXEC	Causes 80 to be displayed
STEP	Causes the 80 displayed by the EXEC switch to shift right 1 bit at a time (80, 40, 20, 10, 08, 04, 02, 01, 00).

The switch subtest can be executed a number of times. To exit the test, press the EXEC switch and STEP switch at the same time.

7.2.2.5 Test 04 - calculate four most likely failed field replaceable units

NOTE

Do not execute test 06, test 07, or test 10 prior to running test 04.

This test uses the status and fault history as displayed by test 00 and 01 to predict the most likely cause of a drive failure. If a cylinder log has been stored in place of a fault log, or if the status or fault logs have been cleared prior to test 04 (when a malfunction is suspected), the calculations for test 04 will be based on unreliable data.

Running the test generates a two digit hex display showing the first and second most likely failed unit (the leftmost digit is the most likely failed unit). Pressing the STEP switch changes the display to the third and fourth most likely failed unit (the leftmost digit is third likely unit). The field replaceable unit corresponding to each hex display is provided in table 7-12.

Table 7-12. Coding of Field Replaceable Units

Hex Display	Field Replaceable Unit
1	Power supply
2	Control board
3	Power smplifier
4	Drive motor
5	Read/write board
6	Head/disk assembly
7	Cooling fan
8	I/O board
9	Operator panel
A	Mother board
B	Carriage unlocking solenoid

Table 7-12. Coding of Field Replaceable Units (continued)

Hex Display	Field Replaceable Unit
C	Belt
D	Diagnostic display
E	HDA interface board
F	Air filter

7.2.2.6 Test 05 - servo

This test performs different seek operations. These operations are listed in table 7-13 in the order in which they occur.

Table 7-13. Servo Test Seek Operations

Operation	Number of Times Executed
RTZ	1
1 track seek	16
Servo recalibrate	8
Maximum length seek	16

Execution stops when an error is detected or the test completes.

7.2.2.7 Test 06 - clear status/error log

This test clears the status/error log. Because test 04 relies on a status history that would be cleared by test 06, you should run test 04 before running test 06. At the conclusion of the test, the log pointer is set to 20, but is not displayed.

7.2.2.8 Test 07 - clear fault log

This test clears the fault log. Because test 04 relies on a status history that test 07 will clear, you should run test 04 before running test 07. At the conclusion of the test, the log pointer is set to 31, but is not displayed.

7.2.2.9 Test 08 - direct seek

This test performs continuous seeks between cylinder 0 and the cylinder address loaded by test 0D. The operation is terminated by pressing the EXEC switch, or by active fault status.

7.2.2.10 Test 09 - random seek

This test performs random seeks within the limits of cylinder 0 and the maximum cylinder address (1419 decimal). Operation is terminated by pressing the EXEC switch, or by active fault status.

7.2.2.11 Test 0A - display/alter load (scan cycle) delay

This test displays and/or alters a count corresponding to the amount of delay between seeks during the scan cycle portion of the load operation. Each display increment represents 10 ms. A load delay count of 04 is displayed when the test is initially selected. To alter the load delay, press the STEP switch repeatedly to increment the display to the desired low order digit and press the EXEC switch. Repeat this operation to alter the high order digit. The load delay will remain altered until the MPU is reinitialized. A load delay occurs when test 02 is performed or AC power is reapplied.

7.2.2.12 Test 0C - display EPROM part number

This test displays the eight digit decimal part number of the EPROM located on the control board. The display is broken into 4 two-digit bytes starting with the most significant byte. To display the remaining bytes, press the STEP switch three times. To exit, turn off the DIAGNOSTIC MODE switch and then turn it back on.

NOTE

Turning off the DIAGNOSTIC MODE switch causes the drive to perform an RTZ operation.

7.2.2.13 Test 0D - load cylinder address

This test loads a number that is used as the upper cylinder address in test 08 (direct seek). The cylinder address is expressed as four hexadecimal digits (see figure 7-2). Initially, the display shows the upper two digits. Advance the righthand digit to the desired value by pressing the STEP switch, and load it into memory by pressing the EXEC switch. The display shifts to show the lower two digits. Repeat the above procedure to load the righthand and then the lefthand digit into memory. The test concludes when the EXEC switch has been pressed four times.

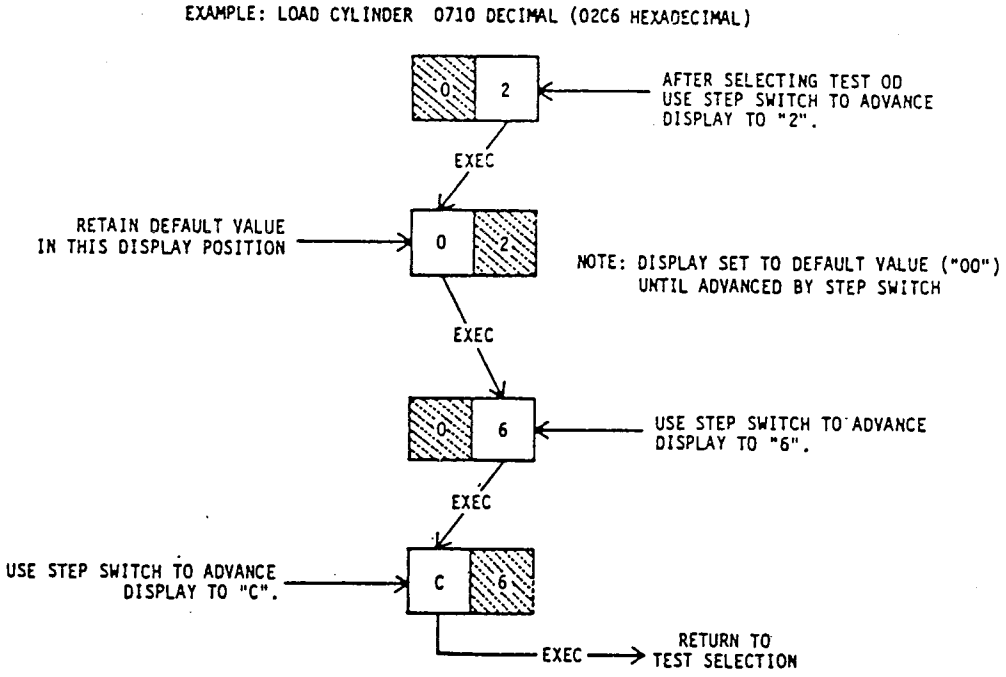


Figure 7-2. Loading an Address in Test 0D.

7.2.2.14 test 0E - return to zero

This test executes a RTZ seek and exits (display returns to 00).

7.2.2.15 test 0F - disable cylinder log

This test disables the cylinder address logging and enables a fault logging.

7.2.2.16 test 10 - enable cylinder log

This test causes the cylinder addresses, rather than fault conditions, to be loaded into the fault log. Following the execution of test 10, the display returns to test selection (00 displayed), then as the drive performs seek operations, the fault log stores the last four cylinder addresses that were accessed. (Figure 7-3 illustrates how to use test 10 to display the cylinder log.)

When the cylinder logging is in effect, the fault indicators on the status/fault display board may flash randomly, and test 04 is not usable.

7.2.2.17 test 11 - disable over temperature fault

//

WARNING

Prolonged operation with the over temperature fault disabled may degrade drive performance and damage the drive.

//

This test causes the MPU to disable the over temperature fault. The fault is prevented from interrupting the drive operation as it would under normal operating conditions.

The over temperature fault will remain disabled until one of the following conditions occur:

- Test 12 is performed to re-enable the over temperature fault
- Test 02 is performed to reinitialize the MPU
- Circuit breaker CB1 is switched OFF and ON

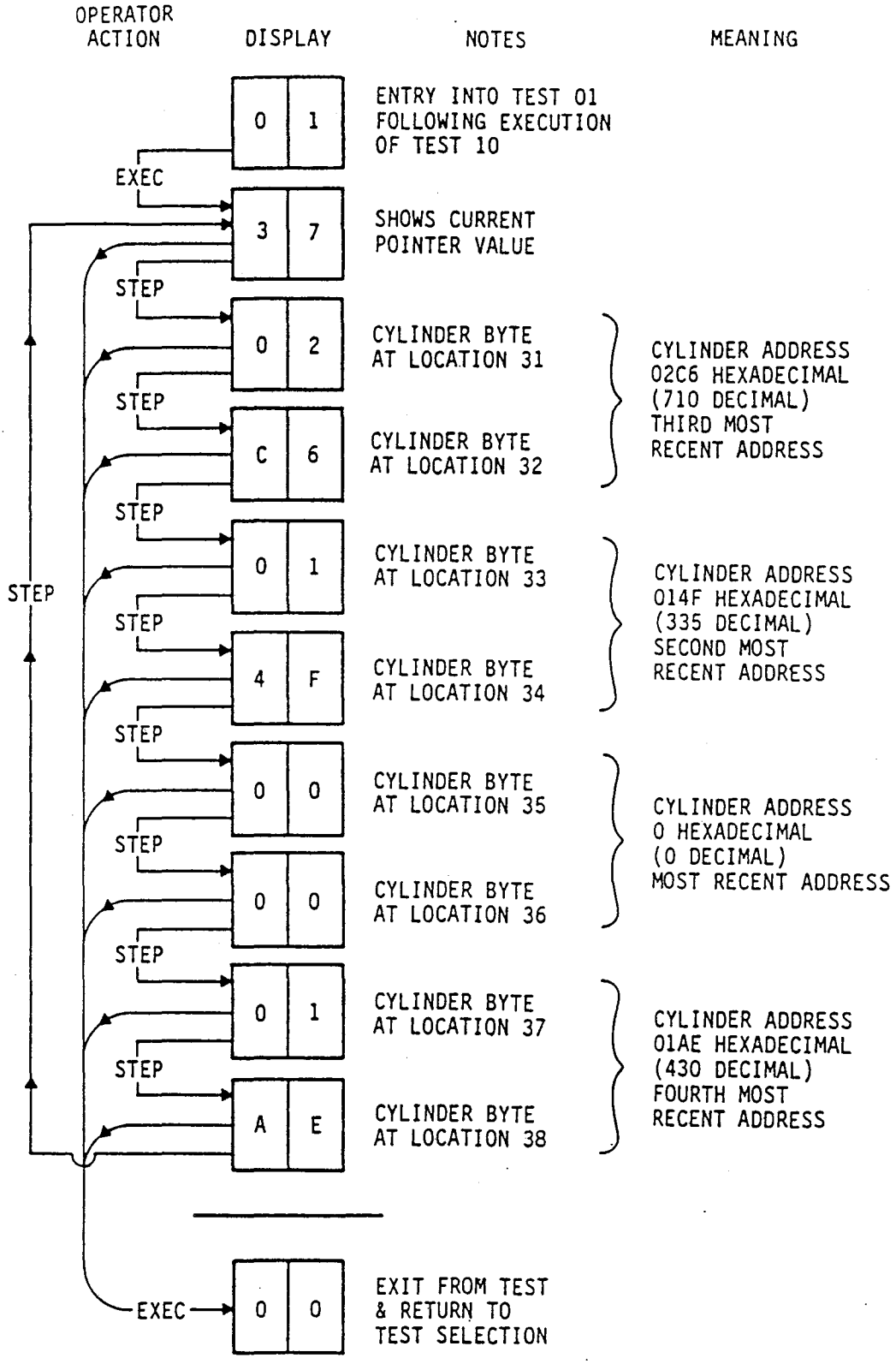


Figure 7-3. Displaying the Cylinder Log

7.2.2.18 test 12 - enable over temperature fault

This test causes the MPU to enable the over temperature fault. The drive is returned to normal operating condition. An over temperature fault will interrupt drive operation.

7.2.3 XMD Spindle Signals

The XMD spindles in the DD-40 consist of a Head Disk Assembly (HDA) (referred to as a module in Control Data documentation) and a number of boards. The XMD boards have cable connectors. The pins of these cable connectors are attachment points for measurement of XMD signals. Table 7-14 gives the connectors on the boards of the XMD spindles. Each spindle in the DD-40 has one set of boards. Table 7-14 also gives the tables in this manual in which the signals of each connector are described.

Table 7-14. Connectors on the XMD Boards

Board Name	Module Designation of the Board	Connector on the Board	Tables of Connector Signals
Control	VDX	J13, J14, J26 J28, J29	4-15 - 4-19
I/O	VJX	J17, J20, J27	4-20 - 4-22
Read/Write	WNX	J27, J30, J32	4-23 - 4-25
Power Ampilfier	UCX	J24, J25, J43 J69, J70	4-26 - 4-27
HDA Interface	BQC	J28, J32	4-28 - 4-29
Operator Panel	PBX	J26	4-30
Fault Display		J19	4-31

The signal on each pin of a connector is either an input or an output. If it is an input, it comes in to the board and has an origin. If it is an output, it goes out of the board and has a destination.

Tables 7-15 through 7-31 give the signals on each of the connectors on the boards of the XMD drives. For each signal, the tables provide the following information:

- Signal - the name of the signal.
- Diagram - the Control Data diagram on which the signal can be traced.
- I/O - whether the signal is an input to the connector or an output from the connector.
- Destination/Origin - the connector that is the destination of the signal if the signal is an output or the connector that is the origin of the signal if the signal is an input.
- Pin - the number of the pin which has the signal.

Table 7-15. Control Board Signals - VDX (J13)

Signal	Diagram	I/O	Destination/Origin	Pin
D/A bit 7	0307	Out	J17-1/J19-1*	1
D/A bit 6	0307	Out	J17-2/J19-2	2
D/A bit 5	0307	Out	J17-3/J19-3	3
D/A bit 4	0307	Out	J17-4/J19-4	4
D/A bit 3	0307	Out	J17-5/J19-5	5
D/A bit 2	0307	Out	J17-6/J19-6	6
D/A bit 1	0307	Out	J17-7/J19-7	7
D/A bit 0	0307	Out	J17-8/J19-8	8
+5V	0307	Out	J17-9/J19-9	9
Ground			J17-10/J19-10	10
Diagnostic Mode	0306	In	J19-11	11
Ground			J17-12/J19-12	12
Fault Data Clock	1305	Out	J19-13	13
Display Latch	0305	Out	J17-14/J19-14	14
Diagnostic Step	0307	In	J17-15/J19-15	15
Diagnostic Execute	0307	In	J17-16/J19-16	16

* Most of the signals on connector J13 have two destinations or origins.

Table 7-16. Control Board Signals - VDX (J14)

Signal	Diagram	I/O	Destination/Origin	Pin
Unit Select Switch	00301	Out	J20-59	1
Select Compare	0305	In	J20-60	2
Unit Select Switch 3	0301	Out	J20-57	3
Write Protected	0308	Out	J20-58	4
Unit Select Switch 2	0301	Out	J20-55	5
Frequency Counter 0	0320	In	J20-56	6
Unit Select Switch 1	0301	Out	J20-53	7
I/O Control 1	0305	Out	J20-54	8
Diagnostic Data 7	0320	Out	J20-51	9
Fault	0305	In	J20-52	10
I/O Control 2	0305	Out	J20-49	11
Diagnostic Mode	0306	Out	J20-50	12
I/O Control 3	0306	In	J20-47	13
RTZ	0305	In	J20-48	14
Head/Cylinder Address 3	0305	In	J20-45	15
Head/Cylinder Address 2	0305	In	J20-46	16
Seek Interrupt	0305	In	J20-43	17
Head/Cylinder Address 1	0305	In	J20-44	18
Head/Cylinder Address 0	0305	In	J20-41	19
Enable Diagnostic Data	0320	In	J20-42	20
Diagnostic Data 4	0320	Out	J20-39	21
Frequency Counter 3	0320	In	J20-40	22
Diagnostic Address 0	0320	In	J20-37	23
Write Protect Switch	0308	Out	J20-38	24
Diagnostic Address 1	0320	In	J20-35	25
Diagnostic Address 2	0320	In	J20-36	26
Read Cylinder Address	0306	Out	J20-33	27
Ready	0307	Out	J20-34	28
Frequency Counter 1	0320	In	J20-31	29
Start Enable	0306	In	J20-32	30
Hold + Local	0306	In	J20-29	31
Diagnostic Data 6	0320	Out	J20-30	32
N/C	0306	In	J20-27	33
Over Temperature	0306	In	J68-01	34
SMD Status Clock	0305	Out	J20-25	35
SMD	0310	In	J20-26	36
Reverse Offset	0315	In	J20-23	37
Offset Interrupt Request		In	J20-24	38
Diagnostic Interrupt			J20-21	39
On Cylinder			J20-22	40
Index			J20-19	41
Frequency Counter 2	0320	In	J20-20	42
N/U			J20-17	43

Table 7-16. Control Board Signals - VDX (J14) (continued)

Signal	Diagram	I/O	Destination/Origin	Pin
Diagnostic Data 5	0320	Out	J20-18	44
Sector			J20-15	45
Forward Offset	0315	In	J20-16	46
DC Master Clear			J20-13	47
Voltage Fault	0302	Out	J20-14	48
Head Address 4	0305	In	J20-11	49
Ground				50
Ground				51
Ground				52
Ground				53
Ground				54
Ground				55
Ground				56
Ground				57
Ground				58
Ground				59
Ground				60

Table 7-17. Control Board Signals - VDX (J26)

Signal	Diagram	I/O	Destination/Origin	Pin
Ground				1
+5V	0301	Out		2
Unit Select Switch 1	0301	In	J26-3	3
+5V	0301	Out		4
Unit Select Switch 2	0302	In	J26-5	5
Ground				6
Unit Select	0305	Out	J26-7	7
Start Switch	0306	In	J26-8	8
Unit Select Switch 0	0301	In	J26-9	9
Fault Clear Switch	0307	In	J26-10	10
Unit Select Switch 3	0301	In	J26-11	11
Fault	0305	Out	J26-12	12
Ready	0308	Out	J26-13	13
Write Protect Switch	0308	In	J26-14	14

Table 7-18. Control Board Signals - VDX (J28)

Signal	Diagram	I/O	Destination/Origin	Pin
Ground	0901	Out	J28-1	1
Ground	0901	Out	J28-2	2
Ground	0901	Out	J28-3	3
Ground	0901	Out	J28-4	4
+Servo Data	0904	In	J28-5	5
-Servo Data	0904	In	J28-6	6
Ground	0901	Out	J28-7	7
Ground	0901	Out	J28-8	8
-8.2V	0901	Out	J28-9	9
-8.2V RTN	0901	Out	J28-10	10

Table 7-19. Control Board Signals - VDX (J29)

Signal	Diagram	I/O	Destination/Origin	Pin
-5V	0301			1
-5V	0301			2
-5V	0301			3
-5V	0301			4
+5V	0301			5
+5V	0301			6
+5V	0301			7
+5V	0301			8
+5V	0301			9
+5V	0301			10
-24V	0301			11
-24V	0301			12
+24V	0301			13
+24V	0301			14
Ground	0301			15
Ground	0301			16
Disable Retract Power	0309	Out	N/C	17
Motor Sensor	0307	In	J24-18	18
3600 RPM		Out	J24-24	19
Disk Stopped	0308	In	J24-21	20
Current Sense	0319	In	J24-26	21

Table 7-19. Control Board Signals - VDX (J29) (continued)

Signal	Diagram	I/O	Destination/Origin	Pin
Diagnostic 1	0306	In	N/C	22
Speed Okay	0308	In	J24-28	23
Diagnostic 2	0306	In	N/C	24
Unlock Activator	0308	Out	J24-30	25
Motor Run	0306	Out	J24-27	26
Out Drive	0319	Out	J24-32	27
Ground	0307	In	J24-29	28
In Drive	0319	Out	J24-33	29
Power Amp Ground	0319	In	J24-31	30
Ground	0301			31
Disable Retract		Out	J24-33	32
+4.032 MHz	0310	Out	J30-12	33
-4.032 MHz	0310	Out	J30-11	34
N/U			J30-14	35
Ground Shield	0301		J30-13	36
Cylinder 768	0305	Out	J30-16	37
Write Gate	0308	In	J30-15	38
Ground Shield	0301		J30-18	39
N/U			J30-17	40
Ground Shield	0301		J30-20	41
Write Fault		In	J30-19	42
Head Address	0305	Out	J30-22	43
N/U			J30-21	44
Head/Cylinder Address 0	0305	Out	J30-24	45
N/U			J30-23	46
Head/Cylinder Address 3	0305	Out	J30-26	47
N/U			J30-25	48
Head/Cylinder Address 2	0305	Out	J30-28	49
Write Enable	0308	Out	J30-27	50
Head/Cylinder Address 1	0305	Out	J30-30	51
N/U			J30-29	52
+15V	0302	Out	J30-32	53
+15V	0302	Out	J30-31	54
-15V	0302	Out	J30-34	55
-15V	0302	Out	J30-33	56
Ground	0301			57
Ground	0301			58
Ground	0301			59
Ground	0301			60

Table 7-20. I/O Board Signals - VJX (J17)

Signal	Diagram	I/O	Destination/Origin	Pin
D/A bit 7	0210	In	J13-1	1
D/A bit 6	0210	In	J13-2	2
D/A bit 3	0210	In	J13-3	3
D/A bit 2	0210	In	J13-4	4
D/A bit 1	0210	In	J13-5	5
D/A bit 0	0210	In	J13-6	6
D/A bit 5	0210	In	J13-7	7
D/A bit 4	0210	In	J13-8	8
N/C	0210	In	J13-9	9
Ground	0210	In	J13-10	10
Diagnostic Mode			J13-11	11
Ground	0210	In	J13-12	12
Fault Data Clock			J13-13	13
N/C	0210	In	J13-14	14
Diagnostic Step	0203	Out	J13-15	15
Diagnostic Execute	0203	Out	J13-16	16

Table 7-21. I/O Board Signals - VJX (J20)

Signal	Diagram	I/O	Destination/Origin	Pin
Fan Sensor	0203	In	N/C	1
-24V	0201		N/C	2
+5V	0201	In	J40-6	3
+5V	0201	In	J40-6	4
+5V	0201	In	J40-6	5
-5V	0201	In	J40-2	6
-5V	0201	In	J40-2	7
-5V	0201	In	J40-2	8
Ground	0201			9
Ground	0201			10
Head/Cylinder Address 4	0208	Out	J14-49	11
Ground	0201			12
DC Master Clear	0209	In	J14-47	13
Voltage Fault	0209	In	J14-48	14
Sector	0211	In	J14-45	15

Table 7-21. I/O Board Signals - VJX (J20) (continued)

Signal	Diagram	I/O	Destination/Origin	Pin
Forward Offset	0209	Out	J14-46	16
N/U			J14-43	17
Diagnostic Data 5		In	J14-44	18
Index	0211	In	J14-41	19
Frequency Counter 2	0203	Out	N/C	20
Diagnostic Interrupt		Out	J14-39	21
On Cylinder		Out	J14-40	22
Reverse Offset	0209	Out	J14-37	23
Offset Interrupt Request	0209	Out	N/C	24
SMD Status Clock	0210	In	J14-35	25
SMD/SDI		Out	J14-36	26
SDI Reset		Out	J14-33	27
Fan Fault	0203	Out	N/C	28
Hold + Local	0208	Out	J14-31	29
Diagnostic Data 6		In	J14-32	30
Frequency Counter 1		Out	J14-29	31
Start Enable	0208	Out	J14-30	32
			33	
Ready	0211	In	J14-30	34
Diagnostic Address 1		Out	J14-25	35
Diagnostic Address 2		Out	J14-26	36
Diagnostic Address 0		Out	J14-23	37
Write Protect Switch		In	J14-24	38
Diagnostic Data 4		In	J14-21	39
Frequency Counter 3		Out	J14-22	40
Head/Cylinder Address 0	0208	Out	J14-19	41
Enable Diagnostic Data		Out	J14-20	42
Seek Interrupt	0209	Out	J14-17	43
Head/Cylinder Address 1	0208	Out	J14-18	44
Head/Cylinder Address 3	0208	Out	J14-15	45
Head/Cylinder Address 2	0208	Out	J14-16	46
I/O Control 3	0209	Out	J14-13	47
RTZ	0209	Out	J14-14	48
I/O Control 2	0209	In	J14-11	49
Diagnostic Mode	0209	In	J14-12	50
Diagnostic Data 7		In	J14-9	51
Fault	0209	Out	J14-10	52
Unit Select Switch 1	0209	In	J14-7	53
I/O Control 1	0209	In	J14-8	54
Unit Select Switch 2	0209	In	J14-5	55
Frequency Counter 0		Out	J14-6	56

Table 7-21. I/O Board Signals - VJX (J20) (continued)

Signal	Diagram	I/O	Destination/Origin	Pin
Unit Select Switch 3	0209	In	J14-3	57
Write Protected	0211	In	J14-4	58
Unit Select Switch 0	0209	In	J14-1	59
Select Compare	0208	Out	J14-2	60

Table 7-22. I/O Board Signals - VJX (J27)

Signal	Diagram	I/O	Destination/Origin	Pin
Ground	0205	In	J27-1	1
+Servo Clock	0205	In	J27-2	2
-Servo Clock	0205	In	J27-3	3
Ground	0205	In	J27-4	4
Data Strobe Late	0209	Out	J27-5	5
Data Strobe Early	0209	Out	J27-6	6
Address Mark Found	0211	In	J27-7	7
Address Mark Enable	0209	Out	J27-8	8
Ground	0207	Out	J27-9	9
Read Gate	0209	Out	J27-10	10
Ground	0207	Out	J27-11	11
Head Select Fault	0209	In	J27-12	12
Write Fault	0209	In	J27-13	13
Write Gate	0209	Out	J27-14	14
Ground	0205	In	J27-15	15
+ Read Clock	0205	In	J27-16	16
- Read Clock	0205	In	J27-17	17
Ground	0205	In	J27-18	18
+ NRZ Read Data	0205	In	J27-19	19
- NRZ Read Data	0205	In	J27-20	20
Ground	0207	Out	J27-21	21
+ Write Clock	0207	Out	J27-22	22
- Write Clock	0207	Out	J27-23	23
Ground	0207	Out	J27-24	24
+ Write Data	0207	Out	J27-25	25
- Write Data	0207	Out	J27-26	26

Table 7-23. Read/Write Board Signals - WNX (J27)

Signal	Diagram	I/O	Destination/Origin	Pin
Ground	0205	Out	J27-1	1
+Servo Clock	0205	Out	J27-2	2
-Servo Clock	0205	Out	J27-3	3
Ground	0205	Out	J27-4	4
Data Strobe Late	0209	In	J27-5	5
Data Strobe Early	0209	In	J27-6	6
Address Mark Found	0211	Out	J27-7	7
Address Mark Enable	0209	In	J27-8	8
Ground	0207	In	J27-9	9
Read Gate	0209	In	J27-10	10
Ground	0207	In	J27-11	11
Head Select Fault	0209	Out	J27-12	12
Write Fault	0209	Out	J27-13	13
Write Gate	0209	Out	J27-14	14
Ground	0205	Out	J27-15	15
+ Read Clock	0205	Out	J27-16	16
- Read Clock	0205	Out	J27-17	17
Ground	0205	Out	J27-18	18
+ NRZ Read Data	0205	Out	J27-19	19
- NRZ Read Data	0205	Out	J27-20	20
Ground	0207	In	J27-21	21
+ Write Clock	0207	In	J27-22	22
- Write Clock	0207	In	J27-23	23
Ground	0207	In	J27-24	24
+ Write Data	0207	In	J27-25	25
- Write Data	0207	In	J27-26	26

Table 7-24. Read/Write Board Signals - WNX (J30)

Signal	Diagram	I/O	Destination/Origin	Pin
+5V	0501	In	J40-6	1
+5V	0501	In	J40-9	2
-5V	0501	In	J40-2	3
N/C	0501	In	J40-9	4
-5V	0501	In	J40-2	5

Table 7-24. Read/Write Board Signals - WNX (J30) (continued)

Signal	Diagram	I/O	Destination/Origin	Pin
-5V	0501	In	J40-2	6
-5V	0501	In	J40-3	7
-5V	0501	In	J40-3	8
-5V	0501	In	J40-3	9
Shield Ground	0501		J29-31	10
-4.032 NHz	0503	In	J29-34	11
+4.032	0503	In	J29-33	12
Shield Ground	0501		J39-36	13
N/U	0501	In	J29-35	14
Write Gate	0502	Out	J29-38	15
T 768	0503	In	J29-37	16
N/U	0501	In	J29-40	17
Shield Ground	0501		J29-39	18
Write Fault	0507	Out	J29-42	19
Shield Ground	0501		J29-41	20
N/C	0501	In	J29-44	21
Head/Cylinder Address 4	0507	In	J29-43	22
N/C	0501	In	J29-46	23
Head/Cylinder Address 0	0507	In	J29-45	24
N/C	0501	In	J29-48	25
Head/Cylinder Address 3	0507	In	J29-47	26
Write Enable	0504	In	J29-50	27
Head/Cylinder Address 2	0507	In	J29-49	28
N/U	0501	In	J29-52	29
Head/Cylinder Address 1	0507		J29-51	30
+15V	0501	In	J29-54	31
+15V	0501	In	J29-53	32
-15V	0501	In	J29-56	33
-15V	0501	In	J29-55	34
Ground	0501			35
Ground	0501			36
Ground	0501			37
Ground	0501			38
Ground	0501			39
Ground	0501			40

Table 7-25. Read/Write Board Signals - WNX (J32)

Signal	Diagram	I/O	Destination/Origin	Pin
WOK	0506	In	J32-1	1
WSX	0506	In	J32-2	2
IMF	0506	In	J32-3	3
Ground			J32-4	4
+ Write Data	0504	Out	J32-5	5
- Write Data	0504	Out	J32-6	6
Ground			J32-7	7
Ground			J32-8	8
- Read Data	0504	In	J32-9	9
+ Read Data	0504	In	J32-10	10
Ground			J32-11	11
Ground			J32-12	12
+5V	0501	In	J32-13	13
+5V	0501	In	J32-14	14
-5V	0501	In	J32-15	15
-5V	0501	In	J32-16	16
Write Enable	0504	Out	J32-17	17
Arm Select 7	0506	Out	N/C	18
Arm Select 6	0506	Out	N/C	19
Arm Select 5	0506	Out	J32-20	20
Arm Select 4	0506	Out	J32-21	21
Arm Select 3	0506	Out	J32-22	22
Arm Select 2	0506	Out	J32-23	23
Arm Select 1	0506	Out	J32-24	24
Head Select 2	0506	Out	J32-25	25
Head Select 1	0506	Out	J32-26	26

Table 7-26. Power Amplifier Board Signals - UCX (J24)

Signal	Diagram	I/O	Destination/Origin	Pin
+24V	0401	In	J40-4	1
+24V	0401	In	J40-4	2
+24V	0401	In	J40-4	3
-24V	0401	In	J40-1	4
-24V	0401	In	J40-1	5

Table 7-26. Power Amplifier Board Signals - UCX (J24) (continued)

Signal	Diagram	I/O	Destination/Origin	Pin
-24V	0401	In	J40-1	6
±24V RTN	0401		J40-5	7
±24V RTN	0401		J40-5	8
N/C				9
±24V	0401		J40-5	10
N/C				11
N/C	0401			12
N/C				13
Over Temperature	0402	Out	J14-34	14
N/C				15
N/C	0401			16
N/C				17
Motor Sense	0403	Out	J29-18	18
Motor Up To Speed	0403	Out	N/C	19
N/C				20
Ground	0403	Out	N/C	21
N/C				22
N/C				23
3600 RPM Detect	0403	In	J29-19	24
N/U				25
Current Sense	0402	Out	J29-21	26
N/C				27
Speed Okay	0403	Out	J29-23	28
Ground	0403	Out	J29-28	29
Unlock Activator	0403	In	J29-25	30
Power Amp Ground	0402	Out	J29-30	31
Out Drive	0402	In	J29-27	32
Disable Retract	0402	In	J29-32	33
In Drive	0402	In	J29-29	34
+5V	0401	In	J40-6	35
+5V	0401	In	J40-6	36
-5V	0401	In	J40-2	37
-5V	0401	In	J40-2	38
Ground	0401			39
Ground				40

Table 7-27. Power Amplifier Board Signals - UCX

Signal	Diagram	I/O	Destination/Origin	Pin
	J25			
+24V	0403	Out	HDA	1
N/C	0401			2
Pull Solenoid	0403	Out	HDA	3
	J43			
Coil Voltage	0402	Out	HDA	1
Ground	0402	Out	HDA	2
Ground	0402	Out	HDA	3
Current Sense	0402	Out	HDA	4
	J69			
N/C	0401			1
Ground	0403	In	HDA	2
Speed Pulses	0403	In	HDA	3
N/C	0401			4
	J70			
Ground	0402		Retract Cap	1
N/C	0401			2
N/C	0401			3
N/C	0401			4
+24V To Retract Cap	0402	Out	Retract Cap	5

Table 7-28. HDA Interface Board Signals - BQC (J28)

Signal	Diagram	I/O	Destination/Origin	Pin
Ground	0901	In	J28-1	1
Ground	0901	In	J28-2	2
Ground	0901	In	J28-3	3
Ground	0901	In	J28-4	4

Table 7-28. HDA Interface Board Signals - BQC (J28) (continued)

Signal	Diagram	I/O	Destination/Origin	Pin
+Servo Data	0904	Out	J28-5	5
-Servo Data	0904	Out	J28-6	6
Ground	0901	In	J28-7	7
Ground	0901	In	J28-8	8
-8.2V	0901	In	J28-9	9
-8.2V RTN	0901	In	J28-10	10

Table 7-29. HDA Interface Board Signals - BQC (J32)

Signal	Diagram	I/O	Destination/Origin	Pin
WOK	0506	Out	J32-1	1
WSX	0506	Out	J32-2	2
IMF	0506	Out	J32-3	3
Ground			J32-4	4
+ Write Data	0504	In	J32-5	5
- Write Data	0504	In	J32-6	6
Ground			J32-7	7
Ground			J32-8	8
- Read Data	0504	Out	J32-9	9
+ Read Data	0504	Out	J32-10	10
Ground			J32-11	11
Ground			J32-12	12
+5V	0501	Out	J32-13	13
+5V	0501	Out	J32-14	14
-5V	0501	Out	J32-15	15
-5V	0501	Out	J32-16	16
Write Enable	0504	In	J32-17	17
Arm Select 7	0506	In	N/C	18
Arm Select 6	0506	In	N/C	19
Arm Select 5	0506	In	J32-20	20
Arm Select 4	0506	In	J32-21	21
Arm Select 3	0506	In	J32-22	22
Arm Select 2	0506	In	J32-23	23
Arm Select 1	0506	In	J32-24	24
Head Select 2	0506	In	J32-25	25
Head Select 1	0506	In	J32-26	26

Table 7-30. Operator Panel Board Signals - PBX (J26)

Signal	Diagram	I/O	Destination/Origin	Pin
Ground	0101		J26-01	1
+5V	0101	In	J26-02	2
Unit Select Switch 1	0102	Out	J26-03	3
+5V	0101	In	J26-04	4
Unit Select Switch 2	0102	Out	J26-05	5
Ground	0101		J26-06	6
Unit Selected	0102	In	J26-07	7
Start	0102	Out	J26-08	8
Unit Select Switch 0	0102	Out	J26-09	9
Fault Clear	0102	Out	J26-10	10
Unit Select Switch 3	0102	Out	J26-11	11
Fault Clear	0102	In	J26-12	12
Ready Alert/Ready	0102	In	J26-13	13
Write Protect	0102	Out	J26-14	14

Table 7-31. Fault Display Board Signals (J19)

Signal	Diagram	I/O	Destination/Origin	Pin
D/A bit 7	0602	In	J19-1	1
D/A bit 6	0602	In	J19-2	2
D/A bit 3	0602	In	J19-3	3
D/A bit 2	0602	In	J19-4	4
D/A bit 1	0602	In	J19-5	5
D/A bit 0	0602	In	J19-6	6
D/A bit 5	0602	In	J19-7	7
D/A bit 4	0602	In	J19-8	8
+5V	0601	In	J19-9	9
Ground	0601	In	J19-10	10
Diagnostic Mode	0601	Out	J19-11	11
Ground	0601	In	J19-12	12
Fault Data Clock	0602	In	J19-13	13
Display Latch	0602	In	J19-14	14
Diagnostic Step	0601	Out	J19-15	15
Diagnostic Execute	0601	Out	J19-16	16

7.2.4 XMD Drive Test Points

The boards of the XMD drives have test points. These are points on the board at which a scope can be attached to test a signal. Tables 7-33 through 7-38 give the test points on each of the XMD boards.

For each test point, the tables provide the following information:

- Location of the test point - the board coordinates (e.g., F5 by 46B) at which the test point is located.
- Signal - the name of the signal found at the test point.

Table 4-32 gives the tables in this manual in which the test points on each board are described.

Table 7-32. Test Point Tables

Board	Table
Control	4-33 and 4-34
I/O	4-35
Read/Write	4-36
Power Amplifier	4-37
HDA Interface	4-38

The pins of connector J80 on the control board are test points. Table 4-33 gives the signals on these pins.

Table 7-33. Control Board Test Points (J80)

Test Point	Signal
1	Position Error
2	- Settle In
3	Cylinder Pulses
4	+ Forward Seek Sync
5	Sector
6	Index
7	- Position
8	Tied High
9	Ground
10	Servo Test Mode
11	- Voltage Fault
12	Position Error
13	Ground
14	Filtered Position Error
15	Test Signal Input
16	1/2 V/Amp
17	Inner Guard Band
18	Valid Decode
19	- Motor Run
20	+5
21	Input Bias
22	-5
23	Input Bias
24	Input Bias
25	Outer Guard Band
26	Velocity

Table 7-34. Control Board Test Points

Test Point	Signal
F546B	T _ 8
B437A	Integrator Clamp
E447C	+ Coarse
D362D	- Track Follow
E276L	- Demodulator Active

Table 7-34. Control Board Test Points (continued)

Test Point	Signal
D365	+ Slope
J410	VCO
B904	+ Servo Tribits
B903	- Servo Tribits
G612	Swage Post
E147	
E936	Desired Velocity
J753	Current Error

Table 7-35. I/O Board Test Points

Test Point	Signal
D208	Index
E630	Sector
D441	Select Compare
E152	Unit Select Tag

Table 7-36. Read/Write Board Test Points

Test Point	Signal
B455	Write Gate
C735	Write Data
C760	Write Clock
C434	2F Clock
B729	
D023	NRZ Read Data
C348	Read Clock

Table 7-36. Read/Write Board Test Points (continued)

Test Point	Signal
E556	Write Enable
F748	Address Mark
H750	IMF
B544	Select Fault
J449	WSV
J549	WOK
C644	Address Mark Enable
B553	Read Gate
B645	Fault
C642	Write Fault
A450	LTD
B551	Address Mark Found
B112	
F108	-2 FRD OSC
G728	Write Data Compare

Table 7-37. Power Amplifier Board Test Points

Test Point	Signal
TP4 G700	+24V
TP2 G200	+5V
TP5 G900	±24V RET
TP3 G400	±5V RET
TP1 F900	-5V
TP6 H200	-24V

Table 7-38. HDA Interface Board Test Points

Test Point	Signal
1	Data IMF
2	Write Data
3	+5
4	-5
5	-8.2
6	+ Servo Data
7	- Servo Data
8	- Read Data
9	+ Read Data
10	Ground
11	Ground

7.2.5 A and B Cable Signals

The A and B cables connect the DD-40 drives to the DC-40. These cables are connected to the bulkhead on the DD-40 and routed to connectors on the I/O boards of the drives. There is one A cable for each drive. There is one B cable for drives A and B, and one for drives C and D. The A-cable signals are daisy-chained from the primary DD-40 to the shadow DD-40. The B-cable signals are not daisy-chained. Separate B cables connect the primary and shadow DD-40's to the DC-40.

Table 7-39 gives the signals on the A cable. The A cable can be plugged into connector J03 or J04 on the drive's I/O board. The connector that is not used for the A cable provides a daisy-chain connection to the shadow DD-40. Table 7-40 gives the signals on the B cable for the primary DD-40 and the shadow DD-40.

Table 7-39. I/O Board Signals - VJX - A Cable (J03/J04)

Signal	DC-40 - I/O	XMD - LO/HI
Unit Select Tag	R0 - 2EJ	22/52
Unit Select bit 0	R1 - 2EJ	23/53

Table 7-39. I/O Board Signals - VJX - A Cable (J03/J04) (continued)

Signal	DC-40 - I/O	XMD - LO/HI
Unit Select bit 1	R2 - 2EJ	24/54
Unit Select bit 2	R3 - 2EJ	26/56
Tag 1	R4 - 2EJ	1/31
Tag 2	R5 - 2EJ	2/31
Tag 3	R6 - 2EJ	3/33
Tag 4	R7 - 2EJ	30/60
Tag 5	R8 - 2EJ	27/57
Bus 0	R9 - 2EJ	4/34
Bus 1	R10 - 2EJ	5/35
Bus 2	R11 - 2EJ	6/36
Bus 3	R12 - 2EJ	7/37
Bus 4	R13 - 2EJ	8/38
Bus 5	R14 - 2EJ	9/39
Bus 6	R15 - 2EJ	10/40
Bus 7	R16 - 2EJ	11/41
Bus 8	R17 - 2EJ	12/42
Bus 9	R18 - 2EJ	13/43
Status 0	I18,I26,I34,I42 - 2EM	19/49
Status 1	I19,I27,I35,I43 - 2EM	17/47
Status 2	I20,I28,I36,I44 - 2EM	16/46
Status 3	I21,I29,I37,I45 - 2EM	15/45
Status 4	I22,I30,I38,I46 - 2EM	28/58
Status 5	I23,I31,I39,I47 - 2EM	20/50
Status 6	I24,I32,I40,I48 - 2EM	18/48
Status 7	I25,I33,I41,I49 - 2EM	25/45
Open Cable Detect	R34 - 2EJ	14/44
Busy	N/U	21/51
Spindle Sequence Pick	Controller Ground	29
Spindle Sequence Hold	Controller Ground	59

Table 7-40. I/O Board Signals - VJX - B Cable (J02)

Signal	I/O	XMD - LO/HI
	Primary DD-40	
Write Data	R4,R12,R20,R28 - 2EK	8/20
Ground		7
Write Clock	R5,R13,R21,R29 - 2EK	6/19
Ground		18
Servo Clock	I6,I22,I32,I42 - 2EK	2/24
Ground		1
Read Data	I5 - 2EJ	3/16
Ground		15
Read Clock	I6 - 2EJ	5/17
Ground		4
Seek End	I10 - 2EJ	10/23
Ground		11
Unit Selected	I9 - 2EJ	22/9
Ground		21
Index	I7 - 2EJ	12/24
Ground		25
Sector	I8 - 2EJ	13/26
	Shadow DD-40	
Write Data	R4,R12,R20,R28 - 2EK	8/20
Ground		7
Write Clock	R5,R13,R21,R29 - 2EK	6/19
Ground		18
Servo Clock	I7,I23,I33,I43 - 2EK	2/14
Ground		1
Read Data	I11 - 2EJ	3/16
Ground		15
Read Clock	I12 - 2EJ	5/17
Ground		4
Seek End	I16 - 2EJ	10/23
Ground		11
Unit Selected	I15 - 2EJ	22/9
Ground		21
Index	I13 - 2EJ	12/24
Ground		25
Sector	I14 - 2EJ	13/26

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