C90 4Meg Spare Memory Chip Scheme

There are a total of 2,048 spare chips in a 16 full size memory module system (1,024 spare chips for a 16 half size memory module system). Every bank on a 4 meg memory module will have one spare memory chip. Since two modules make up a section, there are actually two spare chips per bank per section. These two chips are configured uniquely, one for the lower data and check bits (2^0-2^{31},2^{64}-2^{71}) and one for the upper data and check bits (2^{32}-2^{63},2^{72}-2^{79}). The figures on pages 5 and 6 show the data paths for the full and half size modules. Therefore, every bank in a system has two unique configuration registers that store a failing chip code for that bank.

There are two ways to load the configuration register. The first way loads default values (no failing chip). This function is performed every time the clocks in the system are programmed. These values get loaded on the trailing edge of load complete. Both the ZK (wdata) and ZL (rdata) options get broadside loaded with default values on this signal.

The second way to load the configuration register is with actual write data. The ZK options will load their configuration registers first, and then serially shift data to the ZL options. To perform this load, all configuration registers are enabled by I/O master clear. The timing diagram on page 7 shows the preferred timing for a config operation. For a 16 module system, the actual load takes place on a memory write reference to the upper 1024 words of memory. The actual number of configuration registers is dependant on the number of banks in a system. There will be twice as many configuration registers in a system as there will be banks. The write data on the ZK option is used to load the configuration register. A majority rules is performed on the lower 12 bits ($2^{0\text{-}11}$) of module N before the data is actually latched into the configuration registers on the ZK option. The majority rules function performs a bitwise compare on three identical copies of the configuration code in these lower bit positions and generates a four bit code that gets loaded into the configuration registers. The purpose of the majority rules is to ensure configuration data integrity if the module has hardware failures on the write data path. Likewise, module N+1 performs a similar function on bits $2^{32\text{-}43}$ before it loads its configuration register.

Configuration codes 0-9 shift out the appropriate memory chip. Codes 10-14 are the same as a default code and do not shift any chips. Code 15 is a disable code, which disables the configuration register without overwriting its contents. The figures on pages 8-10 show the configuration codes, configuration word format and an

example of a failing bank.

Since the ZK options handle banks N+0, N+10, N+20 and N+30, the hardware dictates that all four configuration registers on a given ZK option be loaded before the serial transfer to the ZL options takes place. Page 11 has a functional diagram of the ZK option. To ensure proper loading of all configuration registers in a 16 full size module system, a sequential write to the upper 1024 words of memory would be the safest most straightforward method. The ZL option has inputs that receive data from two ZK options (four ZK options in the case of the half-sized memory module). Both ZL options operate in an identical fashion. They poll for a start bit from the ZK option and then process 16 bits of configuration data (banks N+0 through N+3). It takes 25 clock periods from the time the last bank is written until the serial transfer completes and the configuration registers on the ZL options are loaded.

From a software point of view, there are no differences in the implementation of the spare chip concept between the full size and the half size modules. However, when O.S. is brought up, the upper address in each bank must be written with either the configuration code for the bank or with the disable code (14 decimal) which will disarm the configuration registers. The disable code will be used if the configuration codes were written from the maintenance work station. This way the operating system will not change the configuration values but the configuration registers will get disarmed. The configuration codes as they should be written is shown on page 8.

From a hardware standpoint, a new chip type, the ZQ option, was introduced to be used on the half size module. Page 12 has a functional diagram of the ZQ option. The ZQ performs the same function as the ZK option, but can receive both true or compliment write data. Due to path lengths on the half size module, write data was distributed using both the true and compliment signals. The lower ZQ options (ZQ0-15) operate identical to the ZK option. The upper ZQ options (ZQ16-31) however, receive a true copy of write data, and invert that data before it is written into the configuration registers.

C90 4 Meg Memory Module Overview (Full Size)

SYSTEM:

- 1 Gword of memory with 1M x 4 BiCMOS memory chips.
- 20,480 memory chips stacked; 2,048 spare memory chips unstacked.
- 8 sections / 64 subsections / 128 bank groups (lower and upper subsections).
- 1024 banks: 1024 distinct read banks and 512 distinct write banks.
  (128 banks per modules)
- Bank arbitration on groups of 8 banks (lower/upper).
- Two modules per section -- 16 modules per system.
- 40 bits per module / 80 bit words.
- SBCDBD -- single-byte correction, double-byte detection.

SECTION:

- 8 sections per system.
- 16 CPU paths per section.

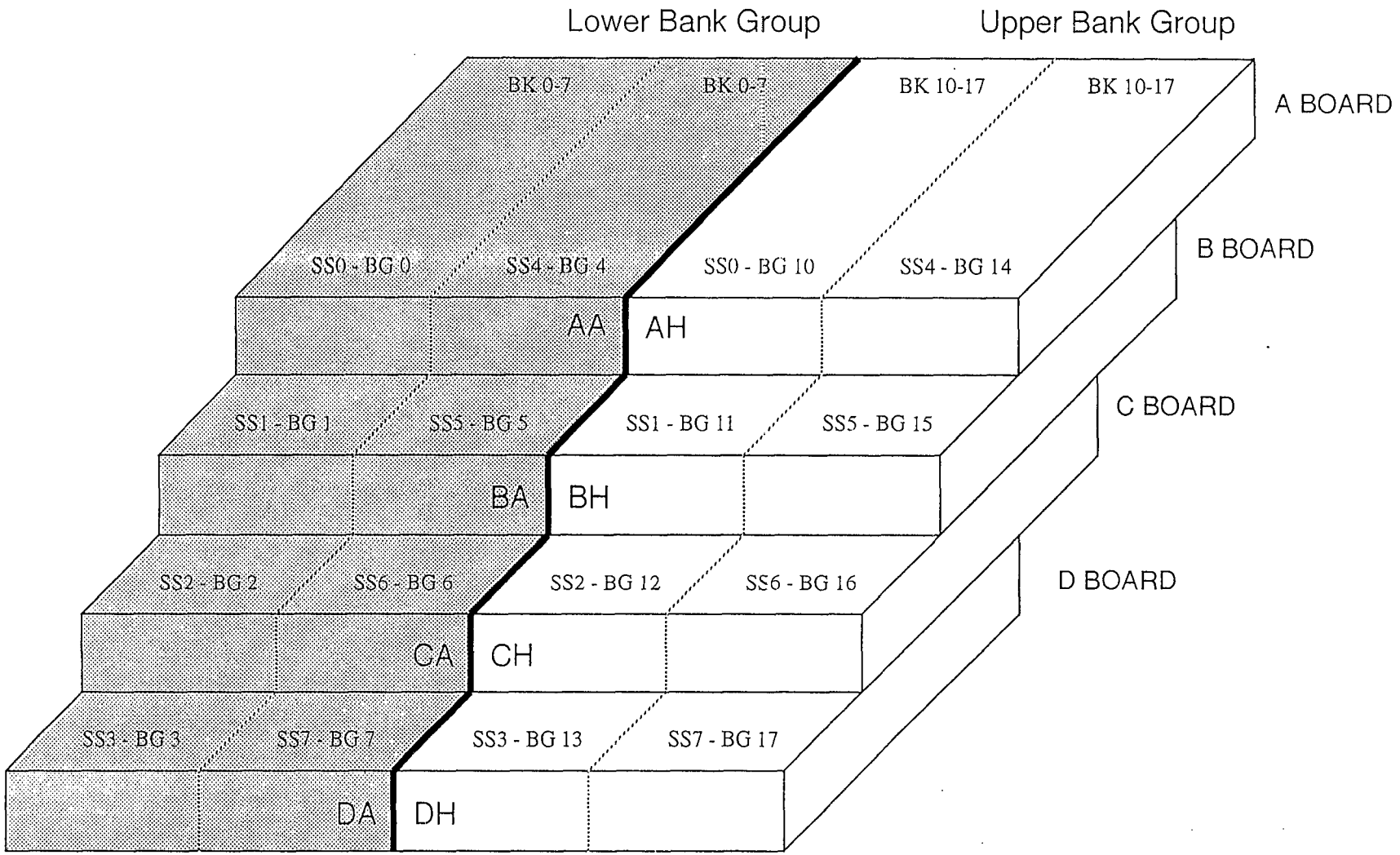
SUBSECTION:

- 8 subsections per section -- 16 bank groups per section (lower/upper).

BANK:

- 16 banks per subsections -- 8 in lower bank group / 8 in upper bank group.
- 11 memory chips per bank (40 bits) -- 1 spare memory chip per bank.

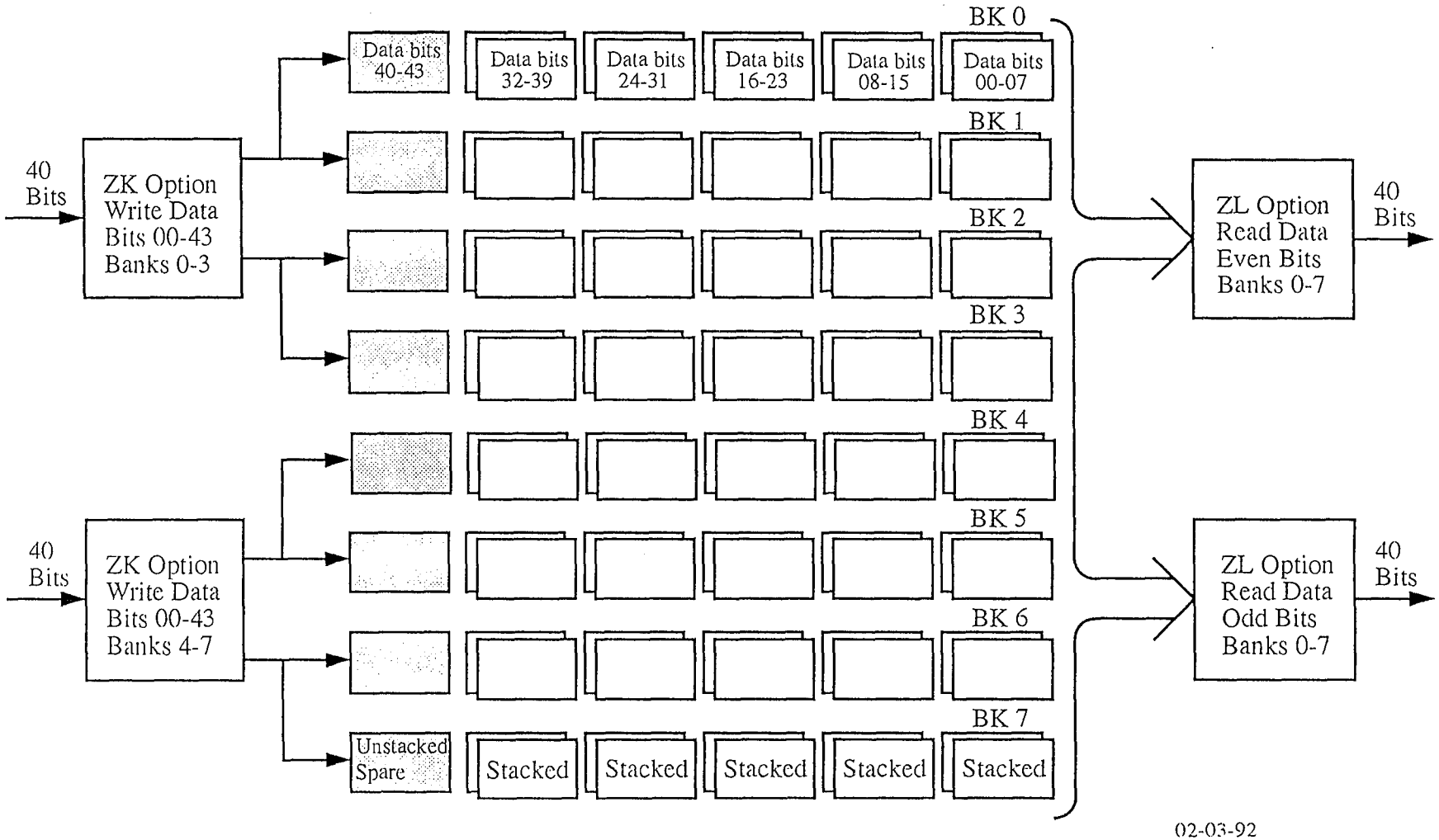
C90 4 Meg Memory Bank Group Module Layout (Full Size)



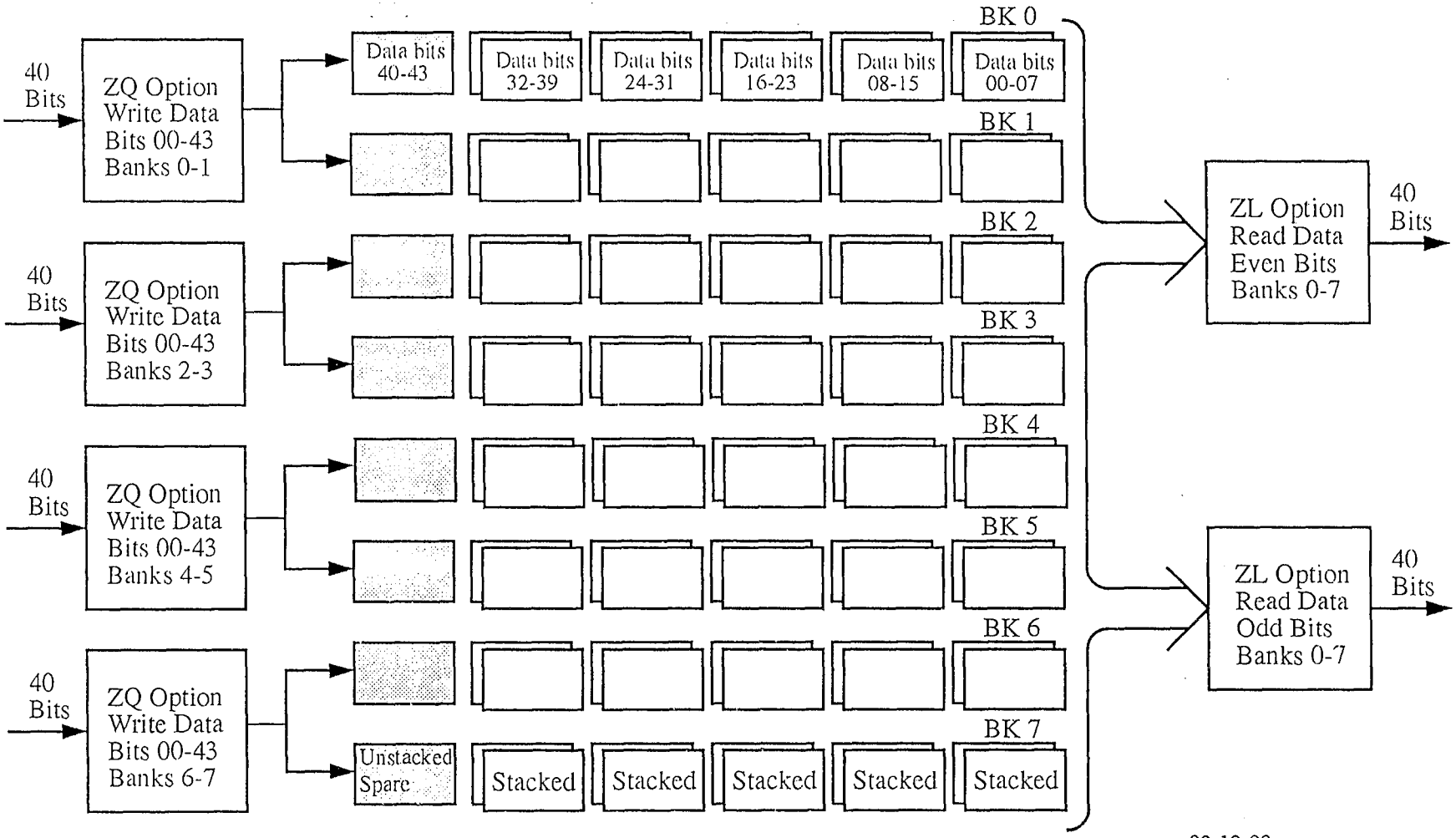
shaded area represents the half size memory module

02-03-92
tjd

C90 4 Meg Memory Module Data Paths (Full Size)



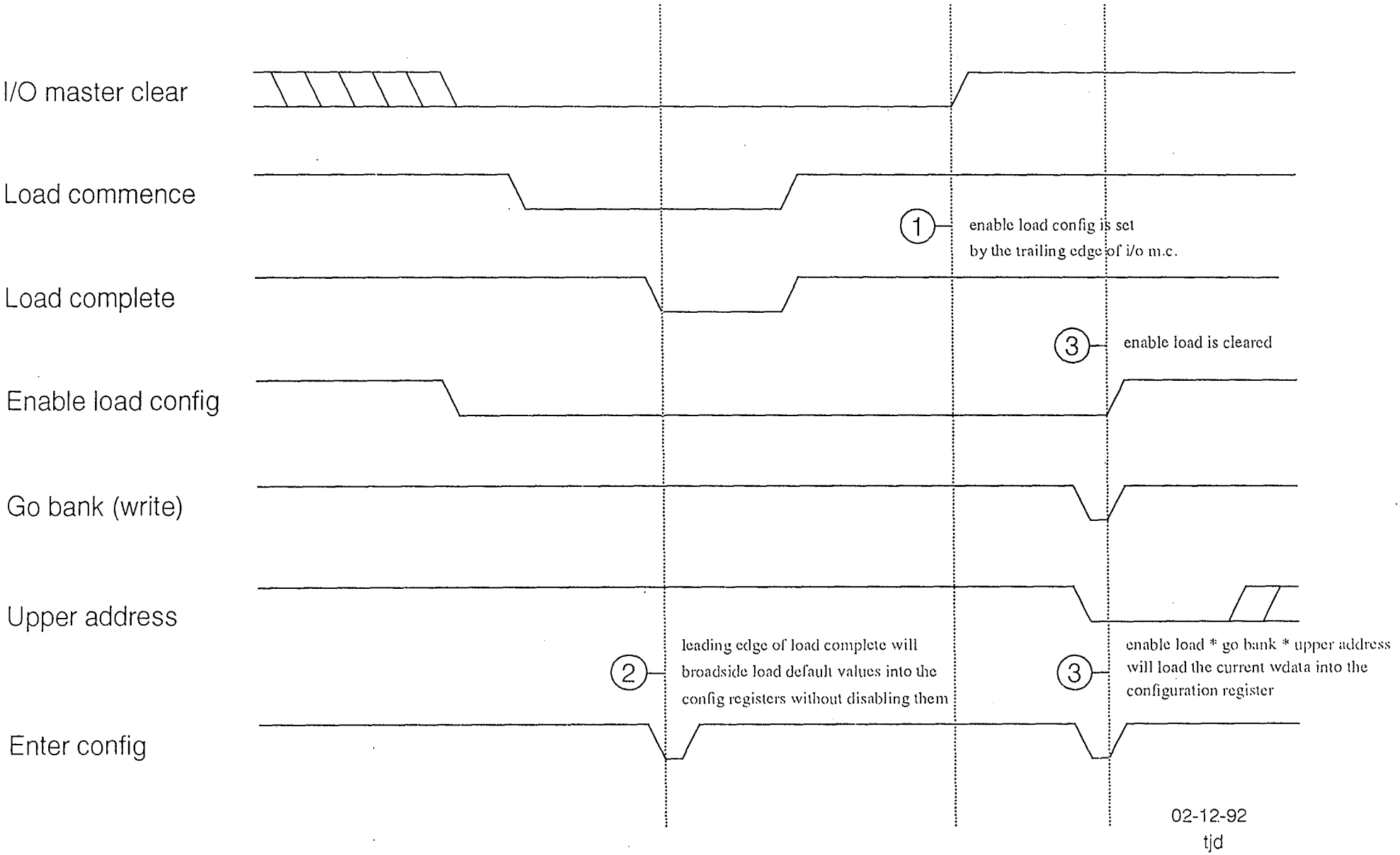
C90 4 Meg Memory Module Data Paths (Half Size)



02-12-92

tjd

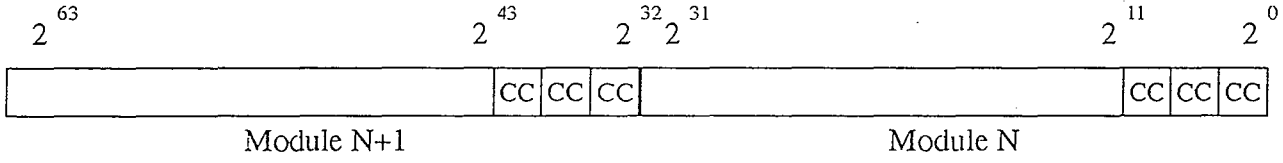
C90 4 Meg Memory Configuration Master Clear Sequence (TV's and Mainframe)



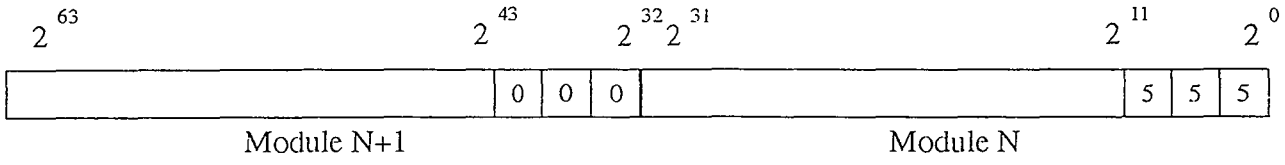
C90 4 Meg Memory Spare Chip Configuration Codes

CODE		MEANING
Decimal	Binary	
00-09	0000-1001	Deselect chip in row
10-13	1010-1101	Unused -- same as default configuration
14	1110	Disable configuration
15	1111	Default configuration

Configuration Codes



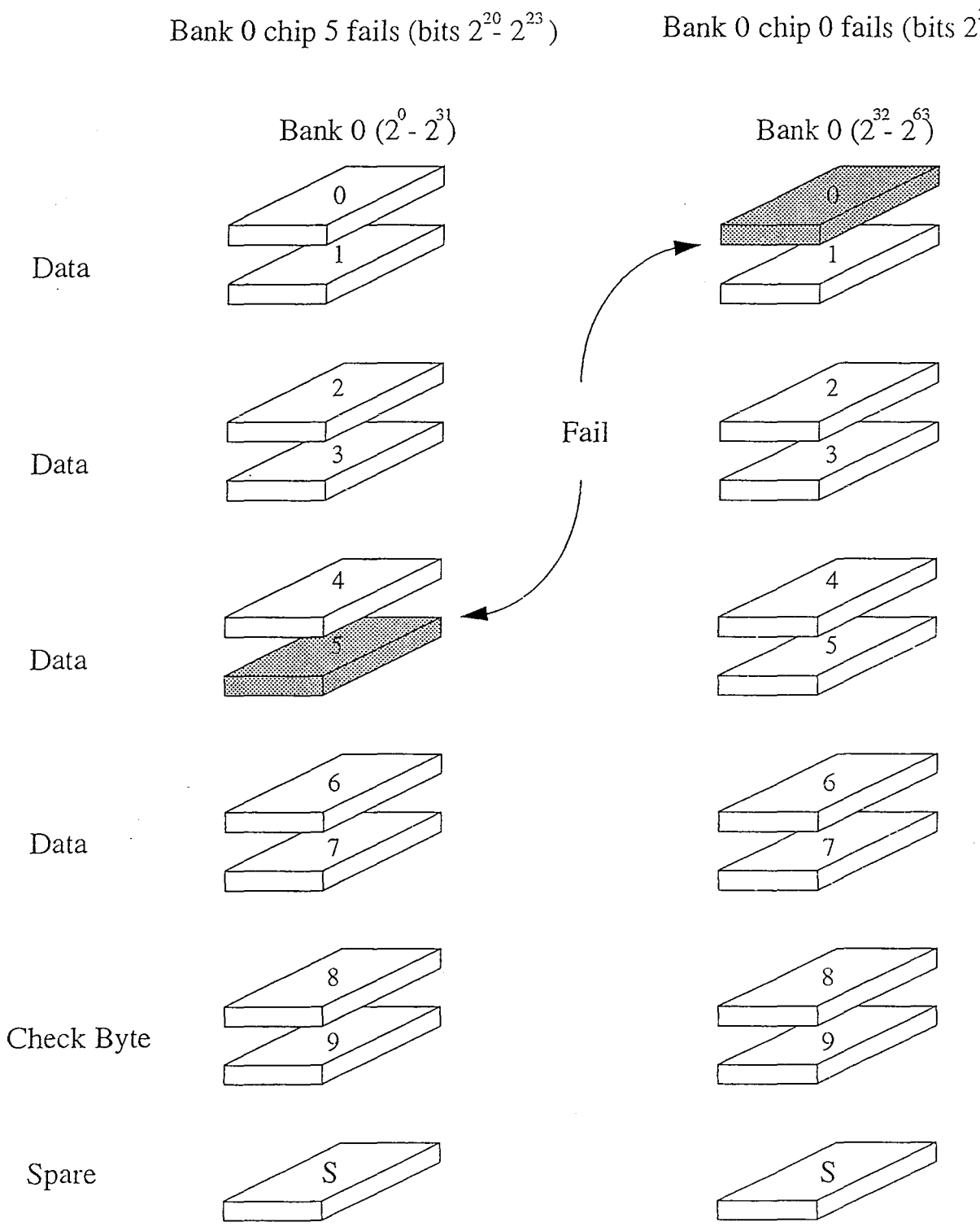
Configuration Word Format



Example: Configuration Word Format

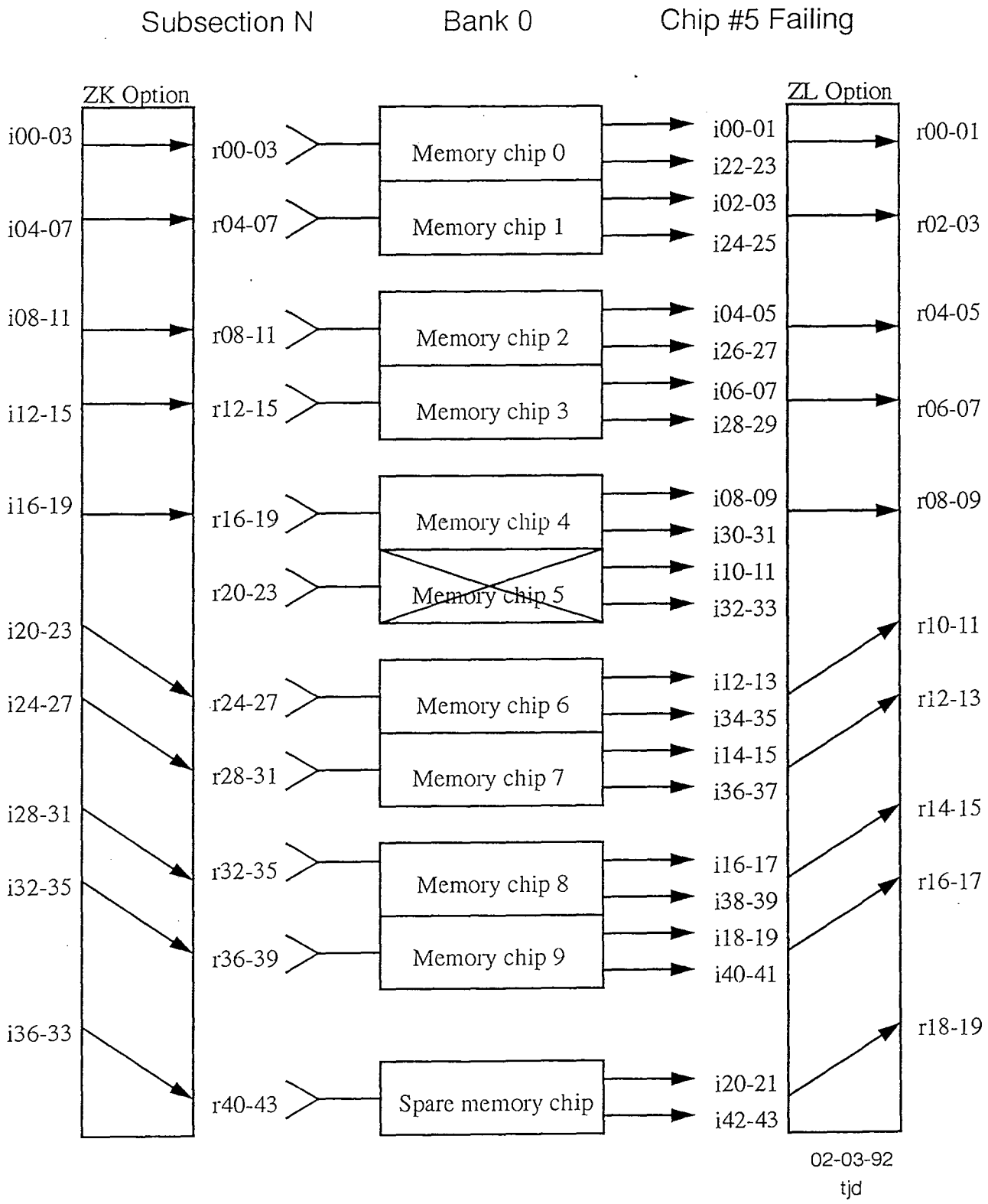
02-04-92
tjd

C90 4 Meg Memory Failing Chip Example



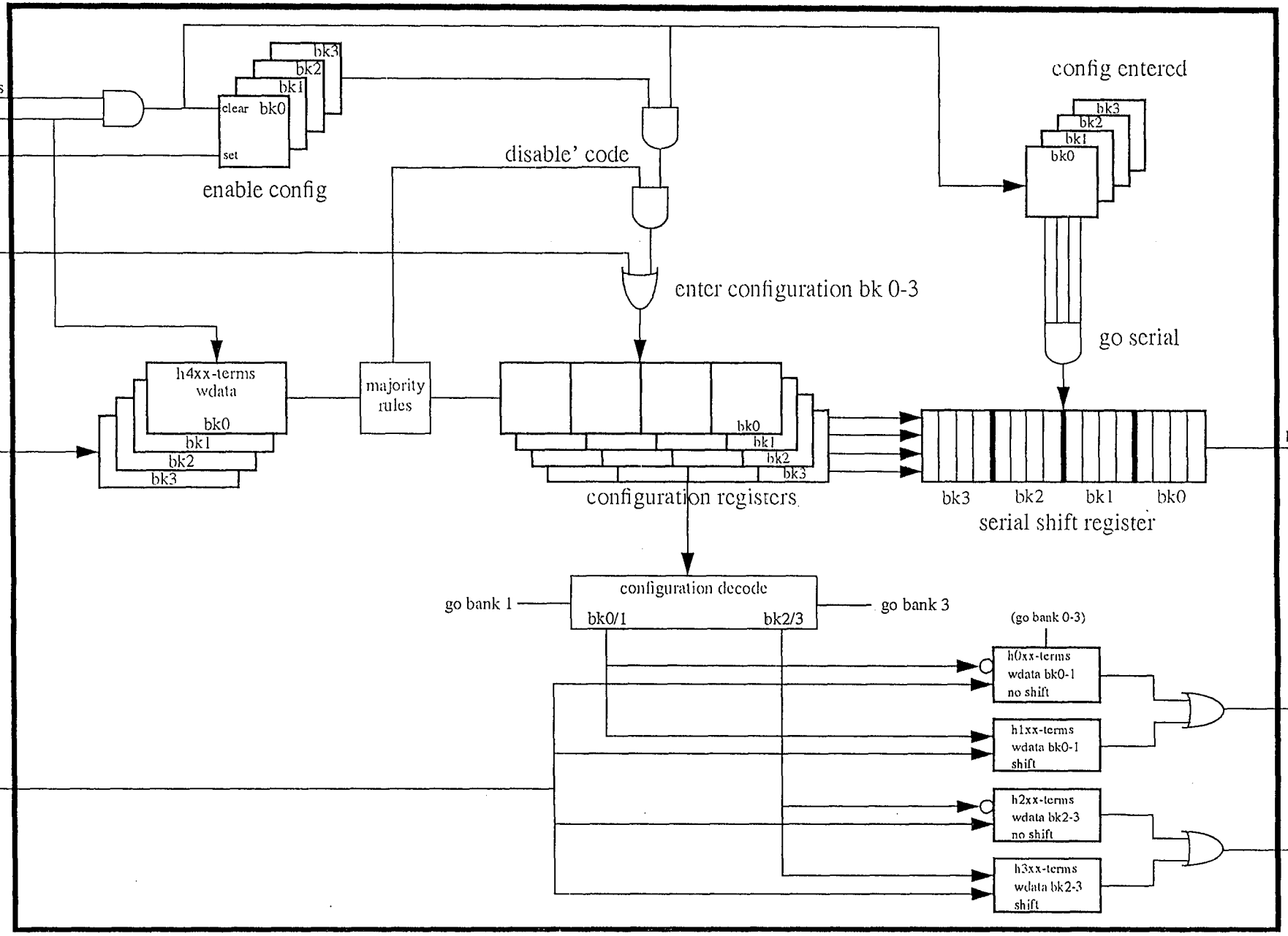
Note: Bank 0 physically exists across 2 modules

C90 4 Meg Memory Reconfiguration Data Path Example (Full Size)



C90 4Meg MEM4M Module

ZK Option -- wdata

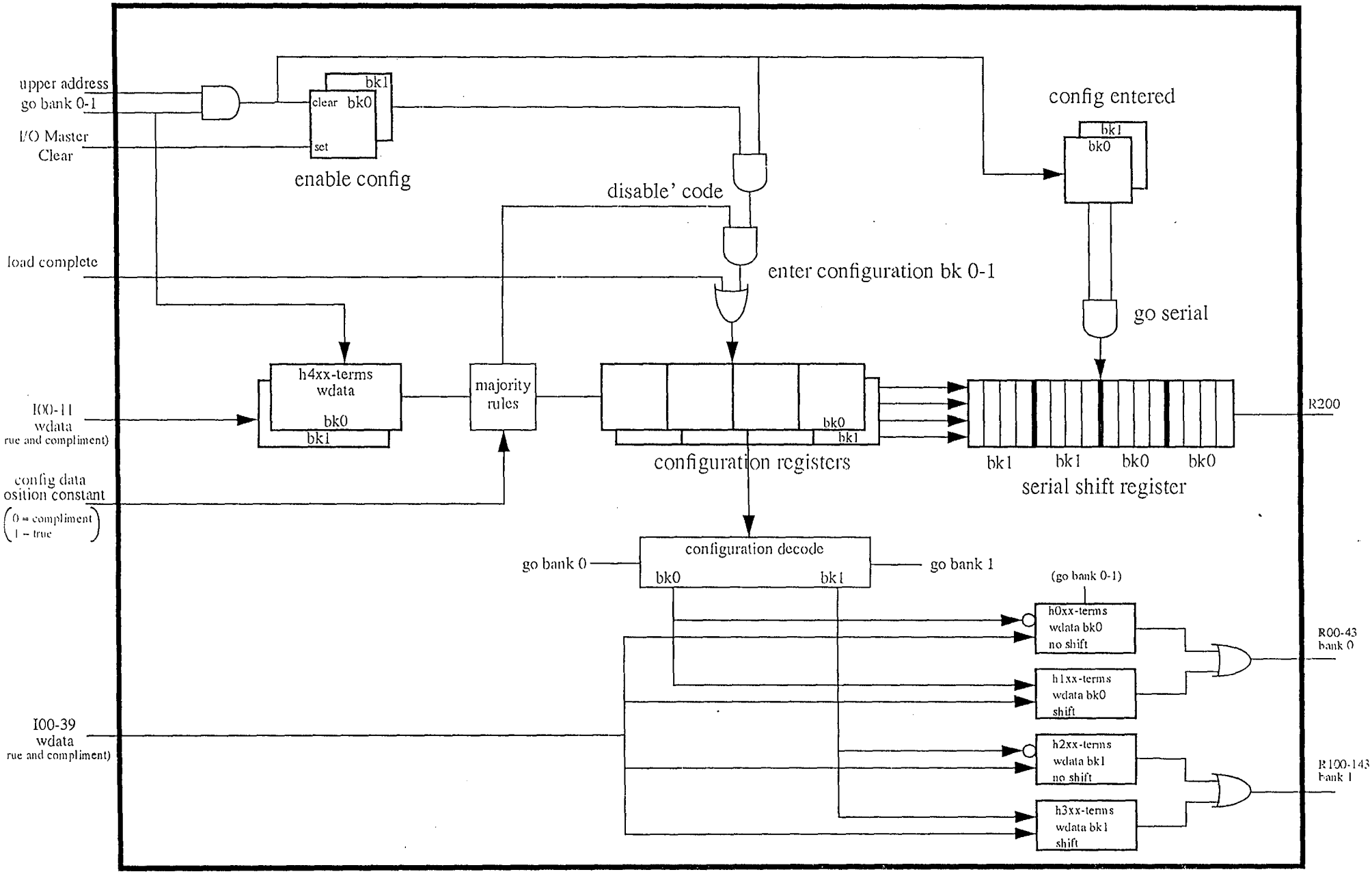


02-11-92

tjd

C90 4Meg HM4M Memory Module

ZQ Option -- wdata



02-11-92

tjd