EVALUATION OF MATERIALS

Your opinion about the quality of our training materials is important to us! Please take a moment and, in the space below, tell us how you would rate the effectiveness of our materials. Whenever possible, use specific manual numbers and page numbers to note errors or areas of confusion. An instructor will collect this page from you when you complete the course. Thank you for your valuable input!

CRAY Y-MP

Hardware Training Volume

VOLUME 1

HTV-0834

Revision	Description
F	April 1989 - The following pages are new: 1-6, 7, 8, 9, 10, 14, 18; 9-1, 7; 11-28, 29, 30, 31; 15-5, 6, 7, 8, 14, 15, 17, 18, 22; 16-11; 17-3, 6, 7, 8; 21-9, 10, 11. The following pages have had technical updates: 1-25, 26, 27, 28; 3-1, 17, 20, 21; 4-40, 41, 42, 43; 6-8; 11-3; 15-2, 9, 15, 18, 19; 16-4; 17-7; 18-2, 5; 20-7; 23-3; 24-12, 15; 25-3, 4; 26-4; 27-10, 11; 29-6; 31-1, 2, 6, 10, 16; 32-5; 33-8; 34-5, 8, 14, 28, 34; 36-5, 6, 7, 8; 37-6, 11, 13, 14, 15, 23, 27; 38-5, 8, 10, 13; 39-13, 14, 15, 18, 19; 40-4, 5; 12-24, 25, 27, 29, 31; 14-20. Sections 6A, 7A, 8A, 9A, 10A, and 128 Mword Overview are new sections to the manual. Manual reprinted.
G	July 1989 - The following pages are new: 7-1 through 7-15; 7A-1 through 7A-13; 8-8, 9, 10; 11-21, 22; 1-46. The following pages have had technical updates: 1-14; 4-8, 15, 20, 21; 8-5, 6, 7; 9-2; 9A-2, 6; 11-25; 15-2, 14, 15; 16-7; 17-6; 18-2; 29-6, 8, 9; 33-8, 10; 34-25; 35-27; 36-2; 8-6; 9-2; 9A-1, 2, 4, 6; 10-7 to 14; 10A-7 to 14; 10B-22 to 32; 11-8, 13, 14, 15, 16, 27; 15-15, 22, 23; 17-1; 37-10, 13, 19; 38-8, 10; 39-6, 13. Sections 4, 7, 7A, and 8 have been renumbered. Manual reprinted.
H	September 1989 - The following pages are new: 11-10, 11, 12. The following pages have had technical updates: 7-28; 7A-4; 8-6; 9A-1; 10A-2, 4; 10B-23. Manual reprinted.

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ACKNOWLEDGEMENTS

John E. Spiegel developed the technical information contained in this volume.

PREFACE

The development of the CRAY Y-MP officially started after the CRAY X-MP was introduced in the summer of 1982. The development of the CRAY Y-MP Training Volume, HTV-0834, officially started in January of 1986, when Boolean and PCLOAD charts could be obtained from the Y-MP Design Engineers, at which time the Floating Add was the first unit that was developed for this manual. The style and format used on the Floating Add went over well, so the rest of the manual followed using the same format.

Each unit or section of the manual is broken down into four subsections which are:

- Unit Description - Contains a general description of how the specific unit operates.
- Options Involved - Describe the individual components that make up the unit.
- Training Aids - Materials generated to explain in more depth difficult areas of the unit, using whatever means that will work.
- Block Diagram - Contains a pictorial description of the entire unit showing the components placement, bit assignments, etc.

The training volume, HTV-0834, can be used by a wide range of audiences, and I would certainly encourage its use. The many hours of labor of which I'm afraid to total, or of which it may be impossible to total, will begin to bear fruit by the many people that use this manual.

In gratitude I would like to thank the Y-MP Logic Design Engineers for the generous supply of Boolean comments and direction; STCO for allowing me the opportunity to work on the Y-MP equipment; Hardware Training Instructional Media and the Hardware Training Support Staff for their dedicated hard work producing professional documentation, and for putting up with the numerous changes each page has gone through; and Hardware Technical Support for allowing a smooth coordination among the departments involved in the Y-MP project. Without all of these people, there would be no HTV-0834.

John E. Spiegel
Hardware Training

REQUIREMENTS FOR COURSE COMPLETION

At the end of each course, an evaluation is written which asks whether the student completed the course. Due to the nature of the courses in Hardware Training, some courses are referred to as theory only; others are theory-lab courses. The determining factors of whether a student receives a Certificate of Completion or Certificate of Attendance are listed as follows:

Theory Only Courses

Theory only courses are courses which do not contain a scheduled period of lab instruction.

a) All exercises (in-class and take-home) are completed and handed in to the instructor.
b) Should a student miss an exercise or test due to absence, it is the responsibility of the student to make up the missing exercise.
c) Students pass with a minimum overall average of 70%.
d) Students attend all class sessions unless an excused absence is authorized by the instructor and/or supervisor.
e) Students are not tardy more than three times unless authorized by the instructor.
f) Students are responsible for informing the instructor for the reason of absence or tardiness.

Theory-lab Courses

Theory-lab courses are courses which do contain a scheduled period of lab instruction.

a) All of the above.
b) Student completes all prerequisites prior to class unless a variance is authorized by a system Supervisor or the Training Manager.
c) Student passes the pretest, when given, prior to the start of the instructional material.
d) A final written exam is passed by the student with a minimal grade of 70%.
e) Student passes the practical lab sessions and the final practical exam.
f) All lab check-off sheets for skills-based training are signed by both the student and instructor and are handed in to the instructor.

If the qualifications or standards as listed above are not met, the student will receive a Certificate of Attendance rather than a Certificate of Completion.

COURSE DESCRIPTION

CRAY Y-MP Computer System

Duration: 10 weeks, including practical lab.

Prerequisites:

- Cray employee
- Digital computer troubleshooting experience and/or computer technology degree
- A structured programming language, such as C or Pascal
- Hardware Systems Overview
- UFE-1 (UCL and Shell Programing)
- VMEbus Maintenance/Operation

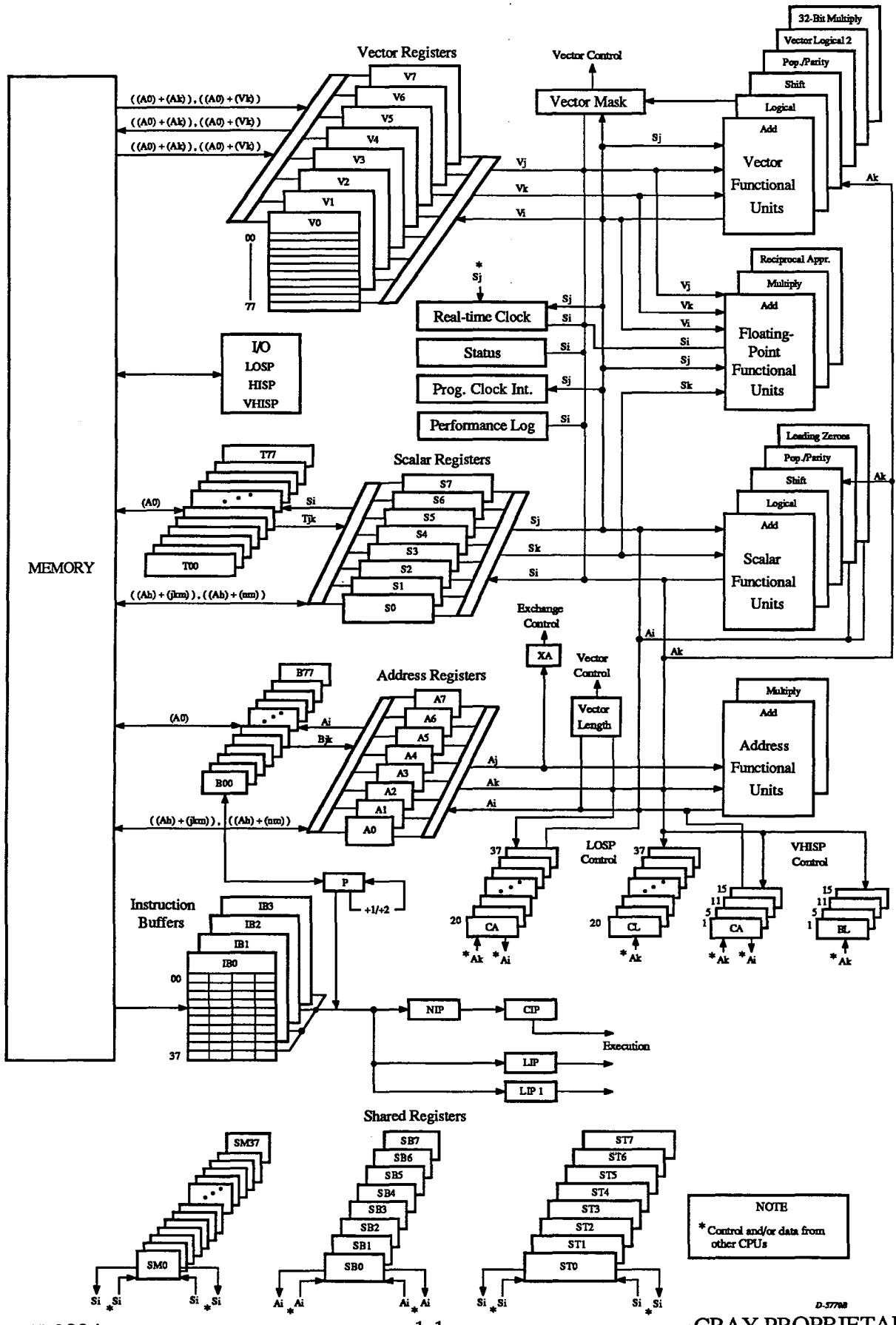
Description: This course deals with the theory of the CRAY Y-MP design combined with practical sessions using the memory, CPU tester, and system. For both new and experienced employees.

MATERIALS REQUIRED

The following materials will be required to complete the CRAY Y-MP Computer Systems course:

• HTV-0834	CRAY Y-MP Hardware Training Volume
• HTV-0854	CRAY Y-MP and X-MP EA Diagnostics Hardware Training Volume
• HTV-0857	CRAY Y-MP Module Test Hardware Training Volume
• HR-4001	CRAY Y-MP Functional Description Manual
• HTA-0845	CRAY Y-MP Block Diagram Size C
• HTV-0683	Power and Refrigeration Hardware Training Volume
• HTA-0860	CRAY Y-MP Chassis Locations (Map)
• HTA-0867	CRAY Y-MP Hardware Reference Card
• HTV-0669	IOS D Block Diagram Analysis Hardware Training Volume

CRAY Y-MP BLOCK DIAGRAM



CRAY Y-MP DESCRIPTION OF HARDWARE

Logic Chip

The CRAY Y-MP is built around the 2500-gate array MCA2500ECL Macrocell Array that is built by Motorola. The 2500-gate consists of 148 leads that are distributed on all four sides of the chip. Each side consists of 37 pins. The MCA2500ECL package size measures 1.14 x 1.14 x .105 inches. The average power draw is 7.5W at -4.5 volts, and 1.5W at -2.0 volts for a total of 9 watts. The maximum power draw is 14 watts.

The MCA2500ECL consists of 110 major cells and 68 output cells. A major cell consists of 56 transistors and 56 resistors that can be organized into a number of logical functions. A Logic Design Engineer can specify what logic functions he/she wants performed by ordering them from the Macrocell Library or by custom designing that logic function. The output cells consist of 15 transistors and 10 resistors. Their primary function is to drive the output pins. The output cells also can perform simple logic functions. The output cells logic functions can also be ordered from the Macrocell Library or they can be custom designed. When running short of a major cell, a spare output cell can be used.

Memory Chip

The CRAY Y-MP with 32 million words of memory uses the 64K x 1 RAM, ECL memory chip. The 64K x 1 package consists of 22 leads with eleven pins per side. The average power is 1.25 watts at a maximum of 1.5 watts.

Printed Circuit Board

The physical size of the printed circuit board (PCB) is 21.2 x 11.0 x .81 inches. The PCB consists of 12 layers which are 4 signals, 1 clock, 3 grounds, 2 -4.5 V or 1 -4.5 V and 1 -5.2 V and 2 -2.0 V layers. The CPU board has room for 78 logic chips per board. The memory board has 39 logic chips and 288 memory chips. The PCB has places for 79 feedthru (Jumper). Each feedthru (Jumper) consists of 48 pins, which are divided into 38 signal pins, five ground pins and five -2.0 V pins. The PCB also contains 24 edge connectors which are located on the "Z" and "Y" axis of the board. Each edge connector consists of 40 pins for a total of 960 pins.

Memory Module

The memory module consists of a double module that contains PCB layers (A, B, C, D). Each memory module draws 2844 watts. The physical size of the memory module is 23.3 x 12.8 x 1.39 inches. The cooling requirement is Fluorinert at 2 gallons per minute allowing a 10^{o} F

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YM18/01 J.E.S.

temperature rise through the module plate. The memory module consists of 96 edge connectors and 57 feedthru (Jumpers). There is also a monitoring connector for test point and temperature sensing on the memory module.

CPU Module

The CPU module consists of a double module that contains PCB layers (A, B, C, D). The physical size of the CPU module is 23.3 x 12.8 x 1.39 inches. The cooling requirement is Fluorinert at 2 gallons per minute that allows a 10^{o} F temperature rise through the module plate. The CPU module consists of 96 edge connectors and 79 feedthru (Jumpers). Also, the CPU module has a monitoring connector for test point and temperature sensing.

System

The CRAY Y-MP Computer System consists of eight CPU modules for a total of eight CPUs or one CPU module containing a single CPU and 32 memory modules. The memory modules are divided into four sections, with each section containing eight memory modules. The total power requirement is 163KVA that includes the power supply drops. The cooling requirement is 80 gallons of water per minute.

Memory Structure

The CRAY Y-MP Computer System uses (64K x 1) ECL memory chips that are organized into 256 banks for a total of 32 million words of storage.

The CRAY Y-MP memory incorporates four sections. Each section is divided into eight subsections, and each subsection contains eight banks, which makes 64 banks per section and 256 banks of total memory.

Physically, there are eight modules per section, and each module contains a 9-bit slice of the 72-bit word. Also, each module is organized into eight subsections. Subsections 0 and 1 are located on the A board, Subsections 2 and 3 are located on the B board, Subsections 4 and 5 are on the C board, and Subsections 6 and 7 are located on the D board.

There are four ports per CPU, and all of these ports share one physical path into memory. All eight CPUs can go to the same subsection as long as they are going to different banks within the subsection. Once a CPU has accessed a bank, that bank is held busy for 5 clock periods (CPs).

A 72-bit word is sent from the CPU module to the eight memory modules that make up a section. Data bits are divided into 9-bits per module. Memory module 0 or Mem. 0 contains data bits (2^{8} - 2^{0}) Mem. 1 contains bits (2^{17} - 2^{9}) and so on. Controls and Address that are sent from the CPUs must also be fanned out to the eight memory modules. This is called an Outboard fanout because they are done outside of the normal modules function. All memory modules assist in performing the 1-to-8 Outboard fanouts, and some of the modules perform more fanouts than other

memory modules. Once on the module, another fanout to the eight subsections takes place. This happens for the address, control, and data. This is referred to as an Onboard fanout, because this fanout happens only within a memory module.

Each subsection contains eight banks and each checks for conflicts amongst the CPUs for those eight banks. When a conflict occurs, the subsection allows the lowest letter CPU to have the highest priority to use the bank. The other CPU would be held out for 5 CPs. All CPUs letter designator are distributed evenly throughout memory. Memory Port conflicts are handled on the CPU module.

CPU STRUCTURE

Vector Registers

The CPU module contains eight Vector registers. Each Vector register contains 64 elements, and each element is 64 bits in length. The Vector registers contain their own Integer functional units which include the Vector Add, Vector Logical, Vector Logical 2, Vector Shift, and Vector population count. The Vector registers also use the Floating-point functional units which include the Floating Add, Floating Multiply, and Floating Reciprocal functional units. The Vector registers are block loaded from memory using Port A or Port B. On a write to memory Port C is used.

Scalar Registers

The CPU module also contains eight Scalar registers, and each Scalar register is 64 bits in length. The Scalar register contains their own functional units which include the Scalar Add, Scalar Logical, Scalar Shift, Scalar Leading Zeroes, and Scalar population count. The Scalar registers also share the Floating-point functional units with the Vector register. Before a Scalar register can use a Floating-point functional unit, it must first check for the unit being reserved by the Vector registers.

The Scalar registers can be loaded from memory one word at a time, or they can be loaded from the T registers. The T register, however, are block loaded from memory, and they are used as intermediate storage for the Scalar registers. There are 64_{10} T-registers that contain 64_{10} bits in length.

Address Registers

The CPU module contains eight Address registers, and each Address register contain 32 bits in length. The Address registers contain their own functional units which include the Address Add, Address Multiply, and the 32-bit Address Multiply that is inside the Floating-point Multiply functional unit. The Address registers can be loaded one word at a time from memory or from the B registers. There are 64_{10} B registers that are 32_{10} bits in length. The B registers are block loaded from memory, and they are used as intermediate storage for the Address registers.

Shared Registers

The Shared registers are used between the processors to pass information between the CPUs. The Shared registers contains the SB, ST, and SM registers. The Shared B registers (SB) are 32 bits in length, and there are eight SB registers. The SB registers are used to pass the A register from one processor to another. The ST registers are 64 bits in length. There are eight ST registers, and the ST registers are used to pass S registers from one processor to another. The SM or Semaphore registers are a 1-bit registers. There are 32_{10} Semaphore registers, and they are used for control between the two CPUs within the same cluster. The Shared registers are contained in nine identical clusters. Cluster 0 is not used, however, it causes the Shared instructions to issue as no-ops.

Instruction Buffers

There are four instruction buffers, and each instruction buffer contains 128_{10} parcels. A Fetch operation loads the instruction buffers. An instruction parcel can be 1 parcel, 2 parcels, or 3 parcels in length. The 3 parcel instruction is used by Scalar memory references and the (020, 040) instructions. Instructions are read from the instruction buffers and placed into the NIP register, and then advanced into CIP by the Go Issue signal. Once an instruction leaves CIP, another instruction will enter CIP. When a 2 parcel instruction issues, the instruction is executed from CIP and LIP. When a 3 parcel instruction issues, the instruction is executed from CIP, LIP, and LIP 1.

I/O Configuration

The I/O channels resides on the CPU modules. Since each CPU module is identical, the channels per the CPU modules are identical as well. Each CPU module contains one LOSP channel at 6 Mbytes, one HISP channel at 100 Mbytes, and a half of a VHISP channel at 1250 Mbytes. It takes two adjacent CPUs to make one VHISP channel. For an eight CPU system, there are eight LOSP, eight HISP, and four VHISP channels.

CRAY Y-MP/28

The CRAY Y-MP/28 consists of 11 modules of which there are three types: the CPUmodule, memory module, and shared modules. The CPU and memory modules are identical to the modules used in the CRAY Y-MP/832. The difference is in the shared module, which contains a single cold plate containing a revision 1 clock fanout board and a shared board. The shared board contains the shared logic which was spread across the other CPU modules in the CRAY Y-MP/832.

There are five types of options contained on the shared board. They are:

1 - (TO) option
1 - (TM) option
2 - (HH) options
14 - (JT) options
7 - (HS) options

CRAY Y-MP/28 (OPTIONS INVOLVED)

(HH0) Option

This option is used for CPU (0 - 3) DL/WS, which replaces the (HH0) option used in CPU 2 on the CRAY Y-MP/832 mainframe.

(HH1) Options

This option is the lowest interrupting channel number, replacing the (HH0) option used in CPU 4 slot on the CRAY Y-MP/832.

(JT10 - JT71) Options

The fourteen (JT) options condense the logic of two (JR) options onto one (JT) option. Each (JT) option handles 4 bits of the Shared register, whereas the (JR) handled 2 bits of the Shared registers. This is possible because shared logic from CPU (4 - 7) has been deleted on the (JT) option. The CRAY Y-MP/28 has two CPU modules. When running from CPU 0, the (JT10, JT11) options would not be used. When running a CRAY Y-MP/18, the (JT10, JT11) options would replace the missing CPU 1 module.

(HS1 - HS7) Options

The seven (HS) options replace the (HS14) option in the CRAY Y-MP/832 mainframe. The (HS1 - HS7) options are the buffer storage for the ST and SB registers and supply enough storage for seven clusters of SB/ST registers. The information below shows how the corresponding (JT, HS) options are used.

(HS1 - JT10, JT11) replaces missing CPU 1 in a CRAY Y-MP/1
(HS2 - JT20, JT21) replaces missing CPU 2 in a CRAY Y-MP/1 or CRAY Y-MP/2
(HS3 - JT30, JT31) replaces missing CPU 3 in a CRAY Y-MP/1 or CRAY Y-MP/2
(HS4 - JT40, JT41) replaces missing CPU 4 in a CRAY Y-MP/1, CRAY Y-MP/2, or CRAY Y-MP/4
(HS5 - JT50, JT51) replaces missing CPU 5 in a CRAY Y-MP/1, CRAY Y-MP/2, or CRAY Y-MP/4
(HS6 - JT60, JT61) replaces missing CPU 6 in a CRAY Y-MP/1, CRAY Y-MP/2, or CRAY Y-MP/4
(HS7 - JT70, JT71) replaces missing CPU 7 in a CRAY Y-MP/1, CRAY Y-MP/2, or CRAY Y-MP/4

(TO0, TM0) Options

The (TO) option supplies the logic option with the clock, while the (TM) supplies the (HS) register option with the write pulse.

The CRAY Y-MP/2 has 12 slots. The table below shows the modules and chassis locations.

Location 1	Shared/Clock
Location 2	CPU 0
Location 3	CPU 1
Location 4	Crossover
Location 5	Section 0 bits (2^0 - 2^{35})
Location 6	Section 0 bits (2^{36} - 2^{71})
Location 7	Section 1 bits (2^0 - 2^{35})
Location 8	Section 1 bits (2^{36} - 2^{71})
Location 9	Section 2 bits (2^0 - 2^{35})
Location 10	Section 2 bits (2^{36} - 2^{71})
Location 11	Section 3 bits (2^0 - 2^{35})
Location 12	Section 3 bits (2^{36} - 2^{71})

Serial number 1401 is the first CRAY Y-MP/28.

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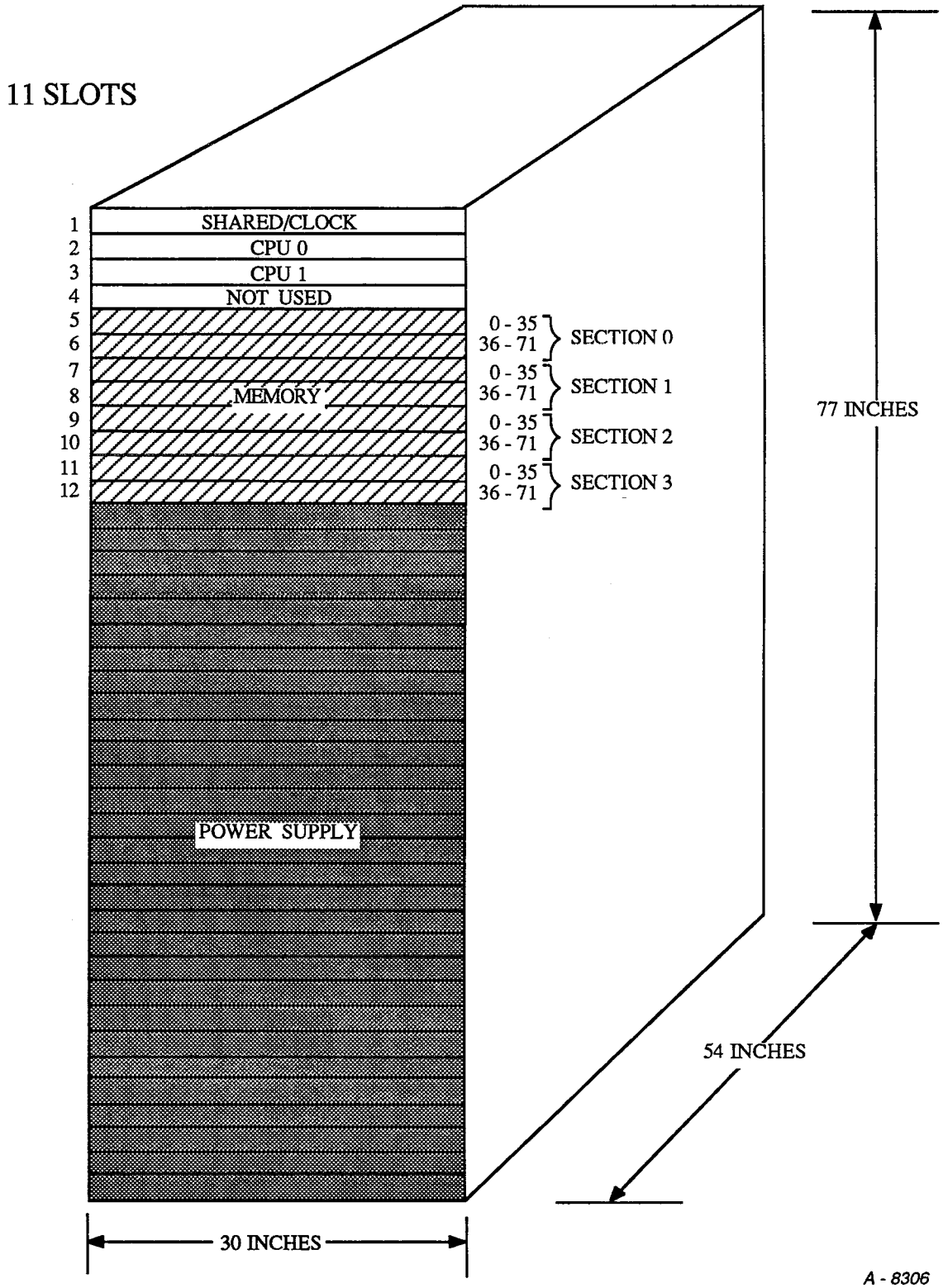
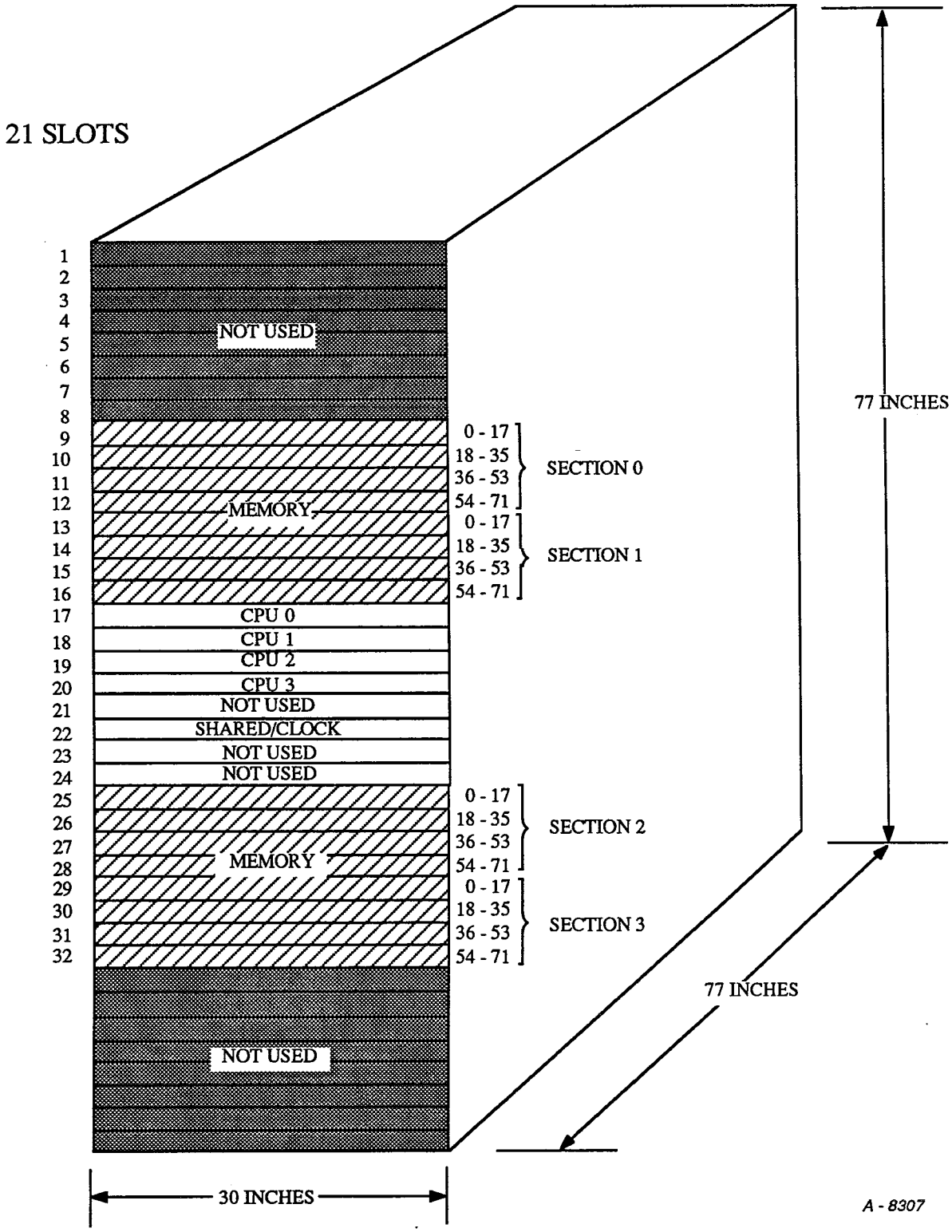
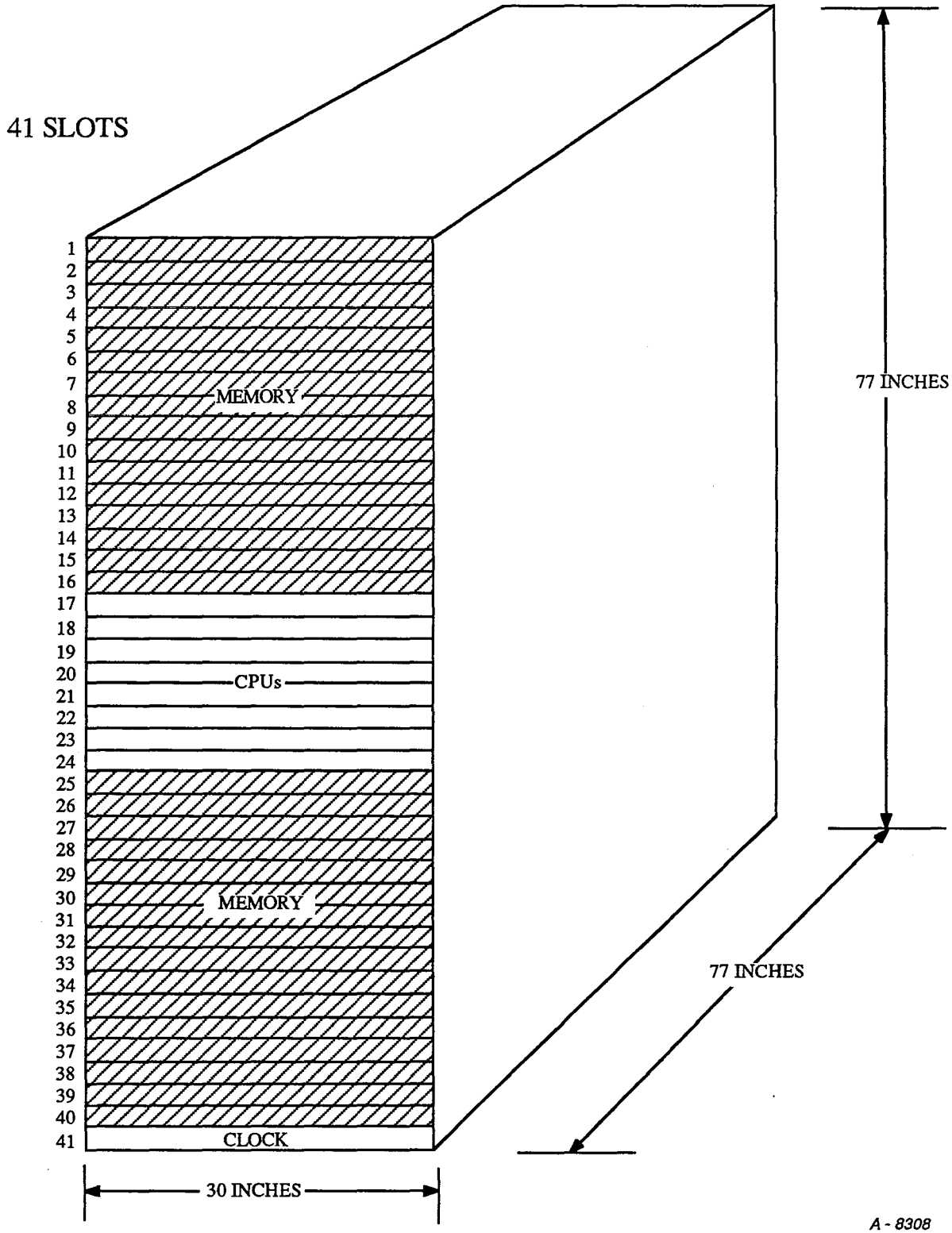


CRAY Y-MP2 DIMENSIONS



CRAY Y-MP4 DIMENSIONS



CRAY Y-MP8 DIMENSIONS

CRAY Y-MP MAINFRAME
DESIGN PARAMETER

LOGIC CHIP

CHIP SPECIFICATION:	MCA2500 ECL Macrocell Array 2500 gate array Lead = 148 37 pins per four sides Package size = 1.14 x 1.14 x .105 inches
POWER:	Average 7.5W at -4.5V plus 1.5W at -2.0 V = 9 watts Maximum = 14 watts

MEMORY CHIP

CHIP SPECIFICATION:	64K x 1 RAM, ECL (100K ECL compatible) Leads = 22 11 pin per two sides Package size = .54 x .36 x .09 (flat pack)
POWER:	Average 1.25 watts Maximum 1.50 watts

PRINTED CIRCUIT BOARD

SIZE:	21.2 x 11.0 x .081 inches
BOARD LAYERS:	12 layers - 4 signals 1 clock 3 grounds 2 -4.5 V or (one -4.5, one -5.2) 2 -2.0 V
CPU BOARD:	78 logic chips per board
MEMORY BOARD:	39 logic chips and 288 memory chips
EDGE CONNECTORS:	40 pins x 24 = 960 pins

YM18/05A

FEED THRU (JUMPERS):	38 signal pins x 79 = 3002 pins five ground pins x 79 = 395 pins five 2 volt pins x 79 = 395 pins

MEMORY MODULE

DOUBLE MODULE (ECL MEMORY):	Board layers (A, B, C, D)
POWER:	2844 watts -4.5 V at 7.5W x 39 x 4 = 1170 watts or 260 amps -2.0 V at 1.5W x 39 x 4 = 234 watts or 117 amps -5.2 V at 1.25 W x 39 x 288 x 4 = 1440 watts or 277 amps
SIZE:	23.3 x 12.8 x 1.39 inches
COOLING:	Fluorinert at 2 gallons per minute; 10 degrees F. temperature rise through the plate
EDGE CONNECTORS:	40 pins x 96 = 3840 pins
FEED THRU (JUMPERS):	(48 pins x 35) + (29 pins x 22)= 2318 pins
MONITORING CONNECTORS:	326 pins

CPU MODULE

DOUBLE MODULE:	Board layers (A, B, C, D)
POWER:	2808 watts -4.5 V at 7.5W x 78 x 4 = 2340 watts = 520 amps -2.0 V at 1.5W x 78 x 4 = 468 watts = 234 amps
SIZE:	23.3 x 12.8 x 1.39 inches
COOLING:	Fluorinert at 2 gallons per minute; 10 degrees F. temperature rise through plates
EDGE CONNECTOR:	40 pins x 96 = 3840 pins
FEED THRU (JUMPERS):	48 pins x 79 = 3792 pins
MONITORING CONNECTOR:	326 pins

YM18/06

SYSTEM

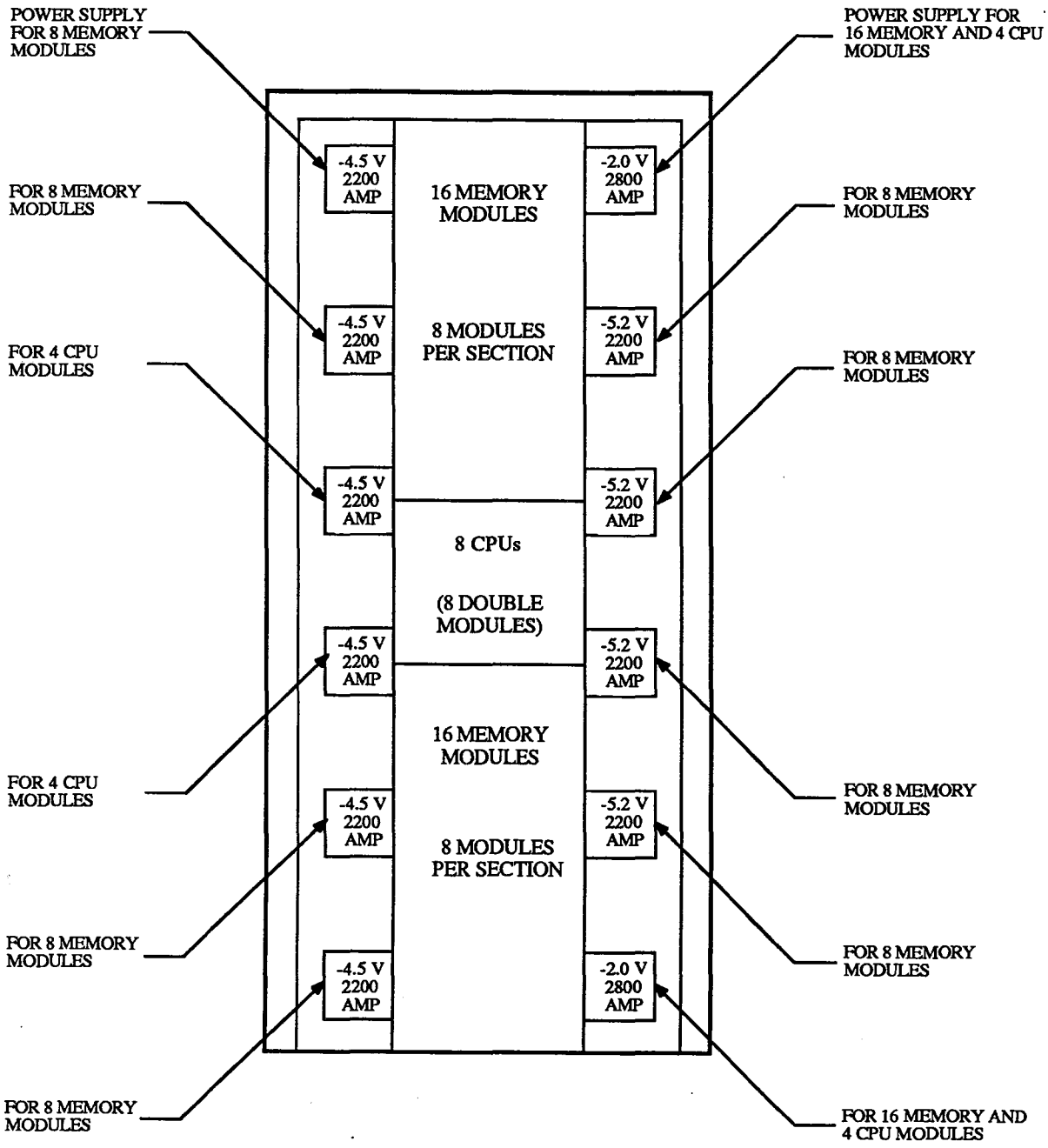
8 CPU MODULES:	8 modules x 2808W = 22,464 watts
32 MEMORY MODULES:	32 modules x 2844W = 91,008 watts
TOTAL POWER:	113,472 watts
NUMBER OF CHIPS:	2496 logic chips in 8 CPUs 4992 logic chips in ECL memory 7488 logic chips total 36,864 memory chip for 32 million words
PHYSICAL SIZE:	CPUs = 24 x 20 x 11.7 inches CPUs + memory = 24 x 20 x 58.4 inches Overall = 68 x 32 x 75
TOTAL POWER REQUIRED:	163 KVA (includes power supply drop)
COOLING REQUIRED:	80 gallons per minute of Fluorinert 42 tons cooled by chiller

YM18/07

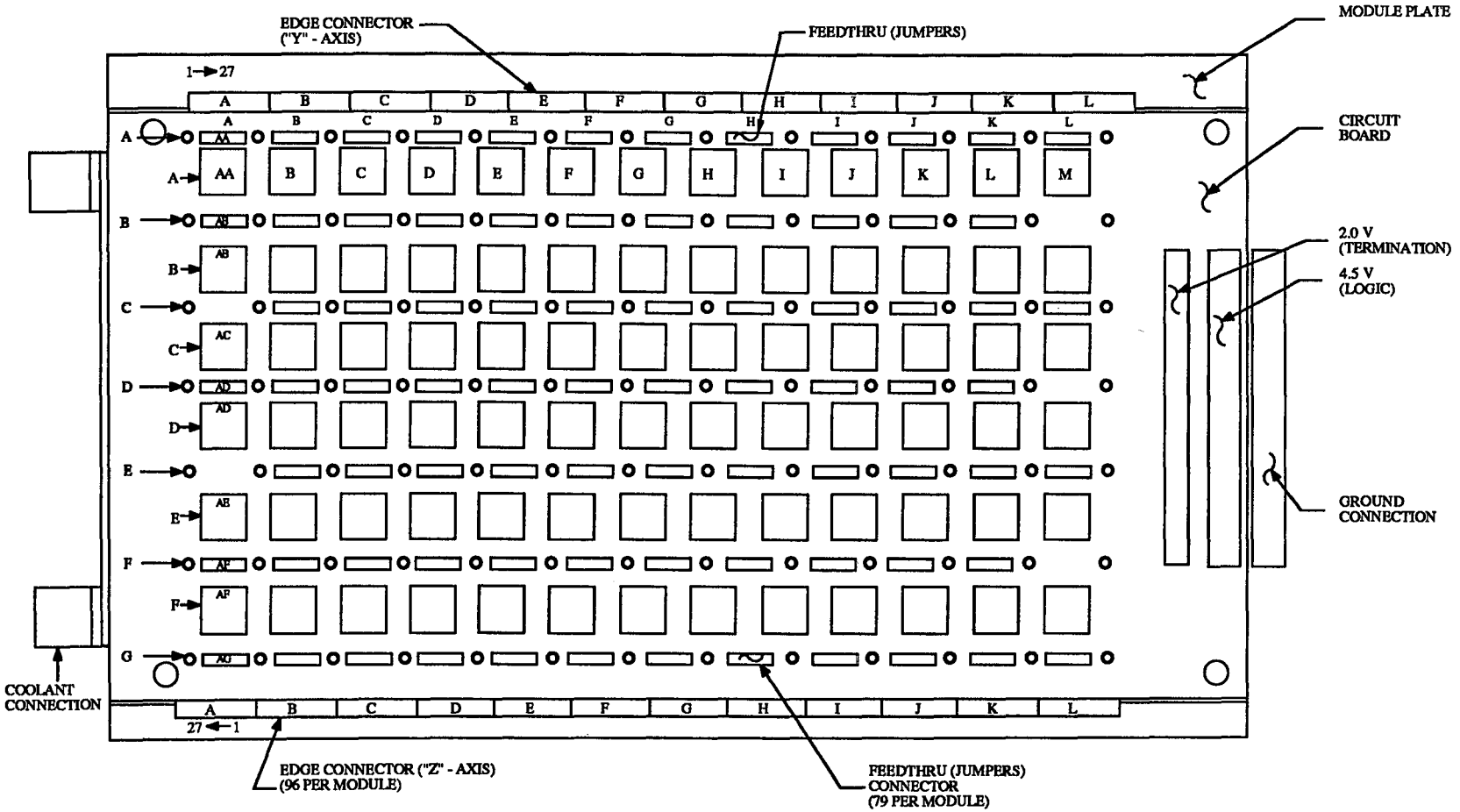
SECTION 0	1	DATA BITS 0 - 8	CPU 0 CPU 2	A0 - 16 A0 - 6	BANK BIT 2 A13 - 16	GOSS 0 - 7	SS RDO (0 - 2)							BANK BUSY (2^0) MEMORY
	2	DATA BITS 9 - 17	CPU 1 CPU 3	A0 - 16 A0 - 6	BANK BIT 2 A13 - 16	GOSS 0 - 7	SS RDO (0 - 2)							BANK BUSY (2^1) MEMORY
	3	DATA BITS 18 - 26	CPU 2 CPU 0	A7 - 12	BANK BITS 0 - 2 BANK BITS 0 - 1	GOSS 0 - 7 ABORT	SS RDO (0 - 2) W.E.			ABORT	W.E.			I/O MASTER CLEAR SEC. 0
	4	DATA BITS 27 - 35	CPU 3 CPU 1	A7 - 12	BANK BITS 0 - 2 BANK BITS 0 - 1	GOSS 0 - 7 ABORT	SS RDO (0 - 2) W.E.			ABORT	W.E.			3 CP W.E. SEC. 0
	5	DATA BITS 36 - 44	CPU 7 CPU 5	A7 - 12	BANK BITS 0 - 2 BANK BITS 0 - 1	GOSS 0 - 7 ABORT	SS RDO (0 - 2) W.E.			ABORT	W.E.			
	6	DATA BITS 45 - 53	CPU 6 CPU 4	A7 - 12	BANK BITS 0 - 2 BANK BITS 0 - 1	GOSS 0 - 7 ABORT	SS RDO (0 - 2) W.E.			ABORT	W.E.			
	7	DATA BITS 54 - 62	CPU 5 CPU 7	A0 - 16 A0 - 6	BANK BIT 2 A13 - 16	GOSS 0 - 7	SS RDO (0 - 2)							MCU INTER. ALL CPUs
	8	DATA BITS 63 - 71	CPU 4 CPU 6	A0 - 16 A0 - 6	BANK BIT 2 A13 - 16	GOSS 0 - 7	SS RDO (0 - 2)							I/O MASTER CLEAR SEC. 0, 1
SECTION 1	9	DATA BITS 0 - 8	CPU 1 CPU 3	A0 - 16 A0 - 6	BANK BIT 2 A13 - 16	GOSS 0 - 7	SS RDO (0 - 2)							BANK BUSY (2^0) MEMORY
	10	DATA BITS 9 - 17	CPU 2 CPU 0	A0 - 16 A0 - 6	BANK BIT 2 A13 - 16	GOSS 0 - 7	SS RDO (0 - 2)							BANK BUSY (2^1) MEMORY
	11	DATA BITS 18 - 26	CPU 3 CPU 1	A7 - 12	BANK BITS 0 - 2 BANK BITS 0 - 1	GOSS 0 - 7 ABORT	SS RDO (0 - 2) W.E.			ABORT	W.E.			I/O MASTER CLEAR SEC. 1
	12	DATA BITS 27 - 35	CPU 0 CPU 2	A7 - 12	BANK BITS 0 - 2 BANK BITS 0 - 1	GOSS 0 - 7 ABORT	SS RDO (0 - 2) W.E.			ABORT	W.E.			3 CP W.E. SEC. 1
	13	DATA BITS 36 - 44	CPU 4 CPU 6	A7 - 12	BANK BITS 0 - 2 BANK BITS 0 - 1	GOSS 0 - 7 ABORT	SS RDO (0 - 2) W.E.			ABORT	W.E.			CPU MASTER CLEAR CPU 0 - 7
	14	DATA BITS 45 - 53	CPU 7 CPU 5	A7 - 12	BANK BITS 0 - 2 BANK BITS 0 - 1	GOSS 0 - 7 ABORT	SS RDO (0 - 2) W.E.			ABORT	W.E.			I/O MASTER CLEAR CPU 0 - 7
	15	DATA BITS 54 - 62	CPU 6 CPU 4	A0 - 16 A0 - 6	BANK BIT 2 A13 - 16	GOSS 0 - 7	SS RDO (0 - 2)							FORCED 1s TO CPU
	16	DATA BITS 63 - 71	CPU 5 CPU 7	A0 - 16 A0 - 6	BANK BIT 2 A13 - 16	GOSS 0 - 7	SS RD0 (0 - 2)							FORCED 1s TO CPU
CPUs	17	CPU 0	CONFLICT RESOLUTION (YL) SECTION 0 SS: 0 - 3 0, 4, 10, 14		SHARED (JR) 0, 8, 16, 24, 32, 40, 48, 56	LOSP 20/21	VHISP 1	PRIORITY (HH) LOSP 24 - 27		ERROR LOGGER BIT (2^0)				FORCED 0s TO CPU 0 - 5
	18	CPU 1	SECTION 1 SS: 0 - 3 1, 5, 11, 15		1, 9, 17, 25, 33, 41, 49, 57	LOSP 22/23	VHISP 1	PRIORITY (HH) LOSP 20 - 23		ERROR LOGGER BIT (2^1)				
	19	CPU 2	SECTION 2 SS: 0 - 3 2, 6, 12, 16		2, 10, 18, 26, 34, 42, 50, 58	LOSP 24/25	VHISP 5	CPU 0 - 3 (HH) D.L., W.S.						
	20	CPU 3	SECTION 3 SS: 0 - 3 3, 7, 13, 17		3, 11, 19, 27, 35, 43, 51, 59	LOSP 26/27	VHISP 5	CPU 4 - 7 (HH) D.L., W.S.						
	21	CPU 4	SECTION 0 SS: 4 - 7 20, 24, 30, 34		4, 12, 20, 28, 36, 44, 52, 60	LOSP 30/31	VHISP 11	LOWEST INTERRUPT CHANNEL NUMBER (HH)						
	22	CPU 5	SECTION 1 SS: 4 - 7 21, 25, 31, 35		5, 13, 21, 29, 37, 45, 53, 61	LOSP 32/33	VHISP 11	ERROR LOGGER CONTROL (HH)						
	23	CPU 6	SECTION 2 SS: 4 - 7 22, 26, 32, 36		6, 14, 22, 30, 38, 46, 54, 62	LOSP 34/35	VHISP 15	PRIORITY (HH) LOSP 30 - 33		ERROR LOGGER BIT (2^2)				
	24	CPU 7	SECTION 3 SS: 4 - 7 23, 27, 33, 37		7, 15, 23, 31, 39, 47, 55, 63	LOSP 36/37	VHISP 15	PRIORITY (HH) LOSP 34 - 37		ERROR LOGGER BIT (2^3)				FORCED 0s TO CPU 0, 2, 4, 6, 7
SECTION 2	25	DATA BITS 0 - 8	CPU 2 CPU 0	A0 - 16 A0 - 6	BANK BIT 2 A13 - 16	GOSS 0 - 7	SS RDO (0 - 2)							BANK BUSY (2^0) MEMORY
	26	DATA BITS 9 - 17	CPU 3 CPU 1	A0 - 16 A0 - 6	BANK BIT 2 A13 - 16	GOSS 0 - 7	SS RDO (0 - 2)							BANK BUSY (2^1) MEMORY
	27	DATA BITS 18 - 26	CPU 0 CPU 2	A7 - 12	BANK BITS 0 - 2 BANK BITS 0 - 1	GOSS 0 - 7 ABORT	SS RDO (0 - 2) W.E.			ABORT	W.E.			I/O MASTER CLEAR SEC. 2
	28	DATA BITS 27 - 35	CPU 1 CPU 3	A7 - 12	BANK BITS 0 - 2 BANK BITS 0 - 1	GOSS 0 - 7 ABORT	SS RDO (0 - 2) W.E.			ABORT	W.E.			3 CP W.E. SEC. 2
	29	DATA BITS 36 - 44	CPU 5 CPU 7	A7 - 12	BANK BITS 0 - 2 BANK BITS 0 - 1	GOSS 0 - 7 ABORT	SS RDO (0 - 2) W.E.			ABORT	W.E.			SELECT DELAY TO CPUs
	30	DATA BITS 45 - 53	CPU 4 CPU 6	A7 - 12	BANK BITS 0 - 2 BANK BITS 0 - 1	GOSS 0 - 7 ABORT	SS RDO (0 - 2) W.E.			ABORT	W.E.			SELECT DELAY TO CPUs
	31	DATA BITS 54 - 62	CPU 7 CPU 5	A0 - 16 A0 - 6	BANK BIT 2 A13 - 16	GOSS 0 - 7	SS RDO (0 - 2)							I/O MASTER CLEAR SEC. 2, 3
	32	DATA BITS 63 - 71	CPU 6 CPU 4	A0 - 16 A0 - 6	BANK BIT 2 A13 - 16	GOSS 0 - 7	SS RDO (0 - 2)							SS BUSY SEL. TO CPUs
SECTION 3	33	DATA BITS 0 - 8	CPU 3 CPU 1	A0 - 16 A0 - 6	BANK BIT 2 A13 - 16	GOSS 0 - 7	SS RDO (0 - 2)							BANK BUSY (2^0) MEMORY
	34	DATA BITS 9 - 17	CPU 0 CPU 2	A0 - 16 A0 - 6	BANK BIT 2 A13 - 16	GOSS 0 - 7	SS RDO (0 - 2)							BANK BUSY (2^1) MEMORY
	35	DATA BITS 18 - 26	CPU 1 CPU 3	A7 - 12	BANK BITS 0 - 2 BANK BITS 0 - 1	GOSS 0 - 7 ABORT	SS RDO (0 - 2) W.E.			ABORT	W.E.			I/O MASTER CLEAR SEC. 3
	36	DATA BITS 27 - 35	CPU 2 CPU 0	A7 - 12	BANK BITS 0 - 2 BANK BITS 0 - 1	GOSS 0 - 7 ABORT	SS RDO (0 - 2) W.E.			ABORT	W.E.			3 CP W.E. SEC. 3
	37	DATA BITS 36 - 44	CPU 6 CPU 4	A7 - 12	BANK BITS 0 - 2 BANK BITS 0 - 1	GOSS 0 - 7 ABORT	SS RDO (0 - 2) W.E.			ABORT	W.E.			SS BUSY TO CPUs
	38	DATA BITS 45 - 53	CPU 5 CPU 7	A7 - 12	BANK BITS 0 - 2 BANK BITS 0 - 1	GOSS 0 - 7 ABORT	SS RDO (0 - 2) W.E.			ABORT	W.E.			BANK BUSY (2^0) TO CPUs
	39	DATA BITS 54 - 62	CPU 4 CPU 6	A0 - 16 A0 - 6	BANK BIT 2 A13 - 16	GOSS 0 - 7	SS RDO (0 - 2)							BANK BUSY (2^1) TO CPUs
	40	DATA BITS 63 - 71	CPU 7 CPU 5	A0 - 16 A0 - 6	BANK BIT 2 A13 - 16	GOSS 0 - 7	SS RDO (0 - 2)							4 CP BANK BUSY SEL. CPUs
	41	CLOCK	ALL CPUs LISTED ARE PHYSICAL											

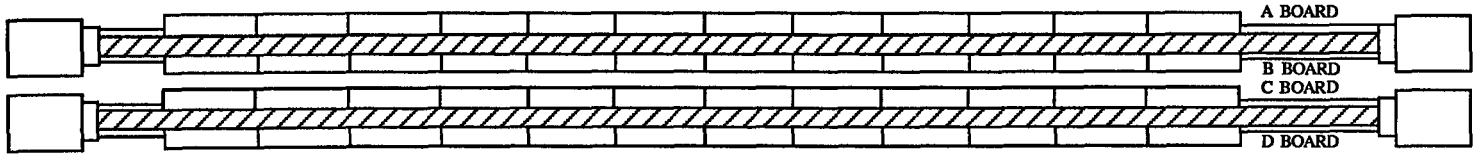
A-7122C

CRAY Y-MP CHASSIS LOCATIONS



CRAY Y-MP MODULES AND POWER SUPPLIES

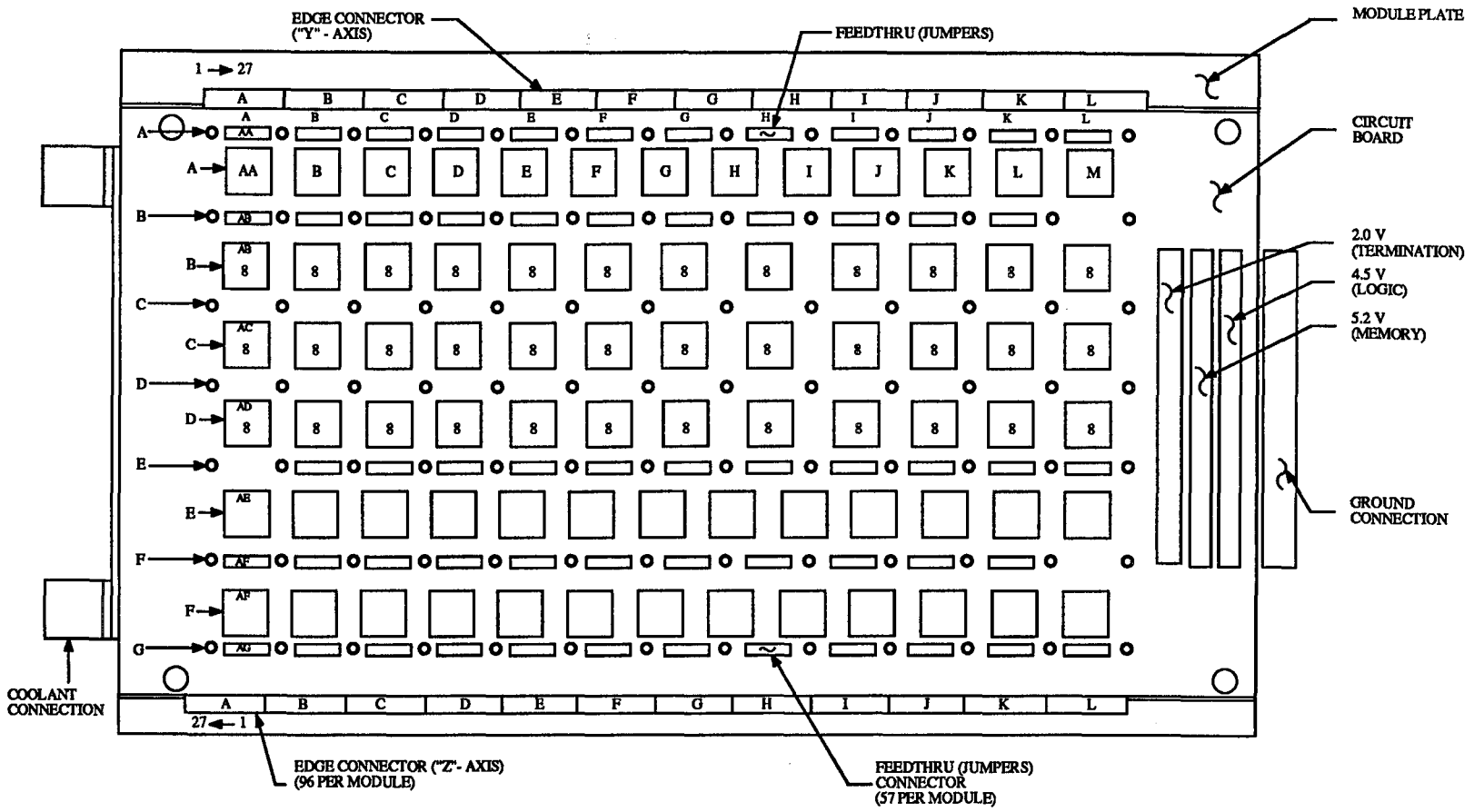




(4) 12 LAYER BOARDS ON (2) PLATES
BOARD DIMENSIONS : 11 X 21.2
PLATE SPACING : .73
GATE ARRAYS : 78 PER BOARD, 312 PER MODULE
AVE. POWER PER GATE ARRAY : 7.5 W OF 4.5 V, 1.5 W OF 20 V

Hardware Trng.
A-5147 J.E.S.

CRAY Y-MP CPU MODULE

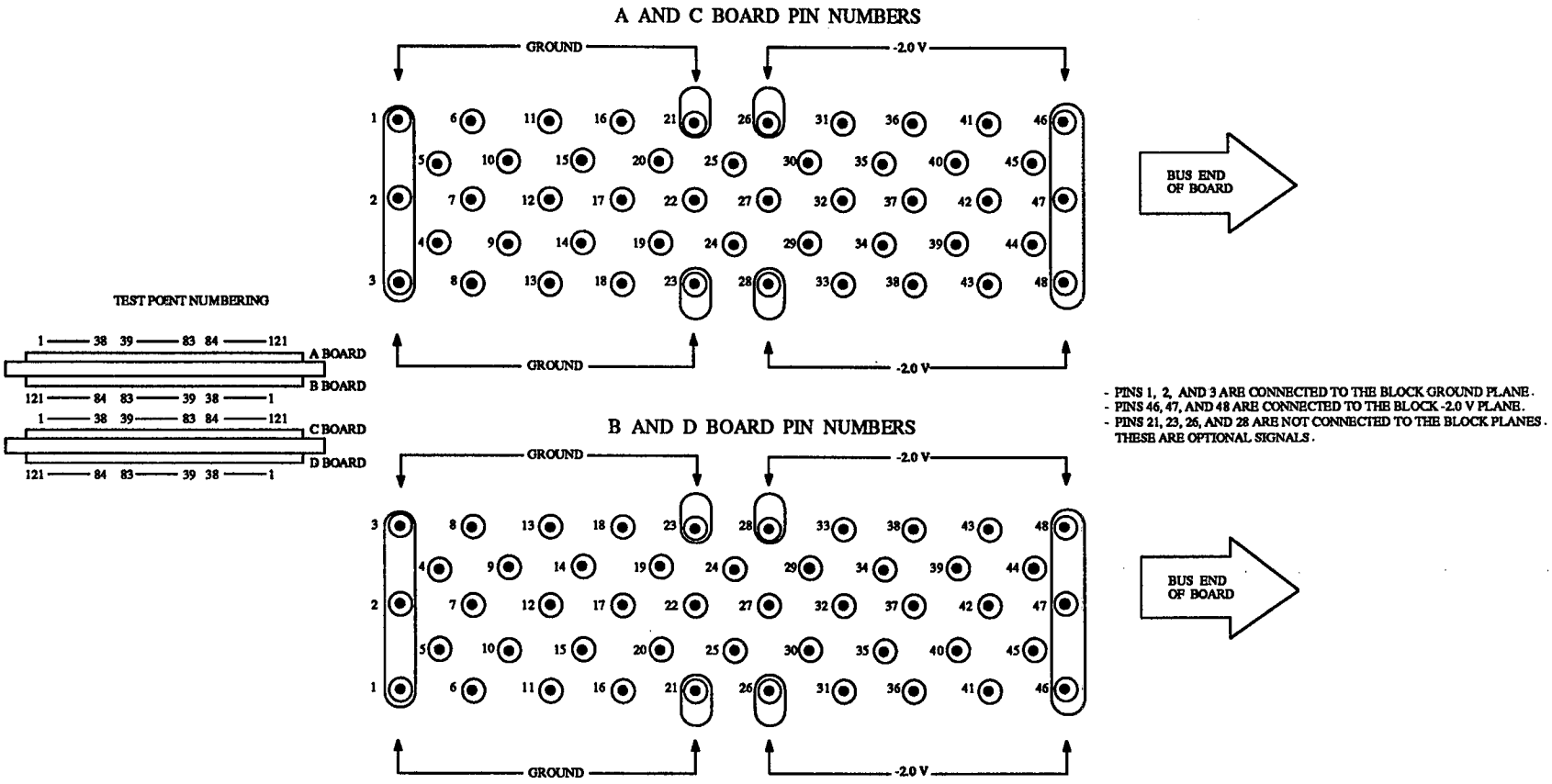


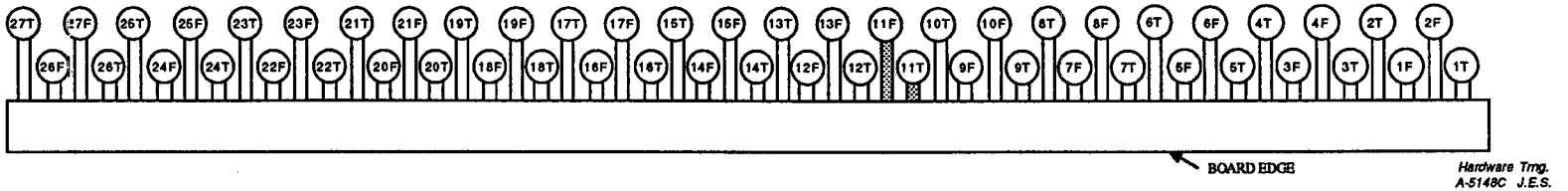
(4) 12 LAYER BOARDS ON (2) PLATES
BOARD DIMENSIONS : 11 X 21.2
PLATE SPACING : .73
GATE ARRAYS : 39 PER BOARD, 156 PER MODULE
AVE. POWER PER GATE ARRAY : 7.5 W OF 4.5 V 1.5 W OF 2.0 V
MEMORY CHIPS 64K X 1 ECL : 288 PER BOARD, 1152 PER MODULE
AVE. POWER PER MEMORY CHIP : 1.25 W OF 5.2 V

Hardware Trng.
A-5146 J.E.S.

CRAY Y-MP MEMORY MODULE (64K x 1)

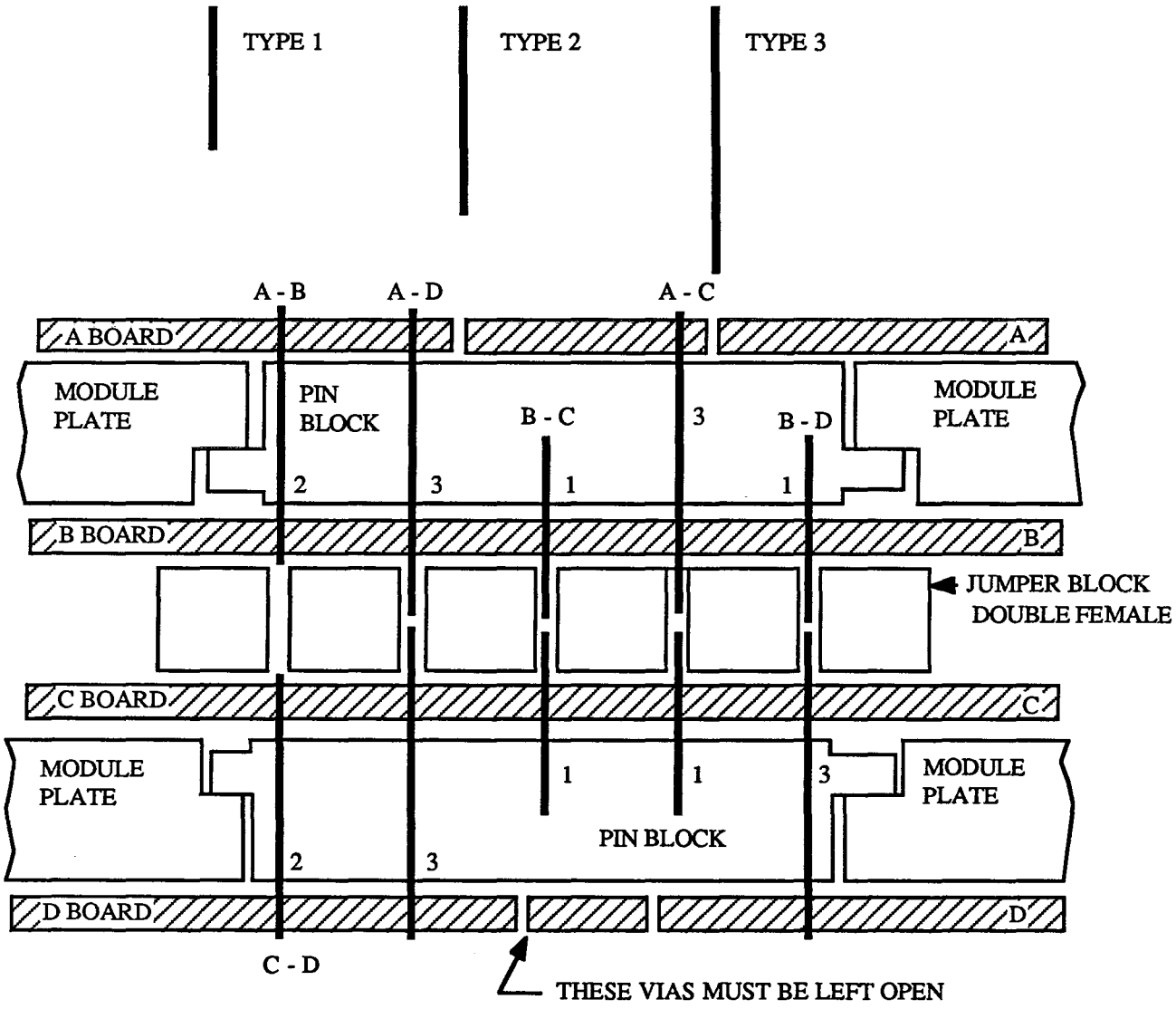
CRAY Y-MP FEEDTHRU CONNECTOR JUMPER PIN ASSIGNMENT





CRAY Y-MP EDGE CONNECTOR PIN ASSIGNMENTS

CONNECTOR PINS TYPE 1 - 3

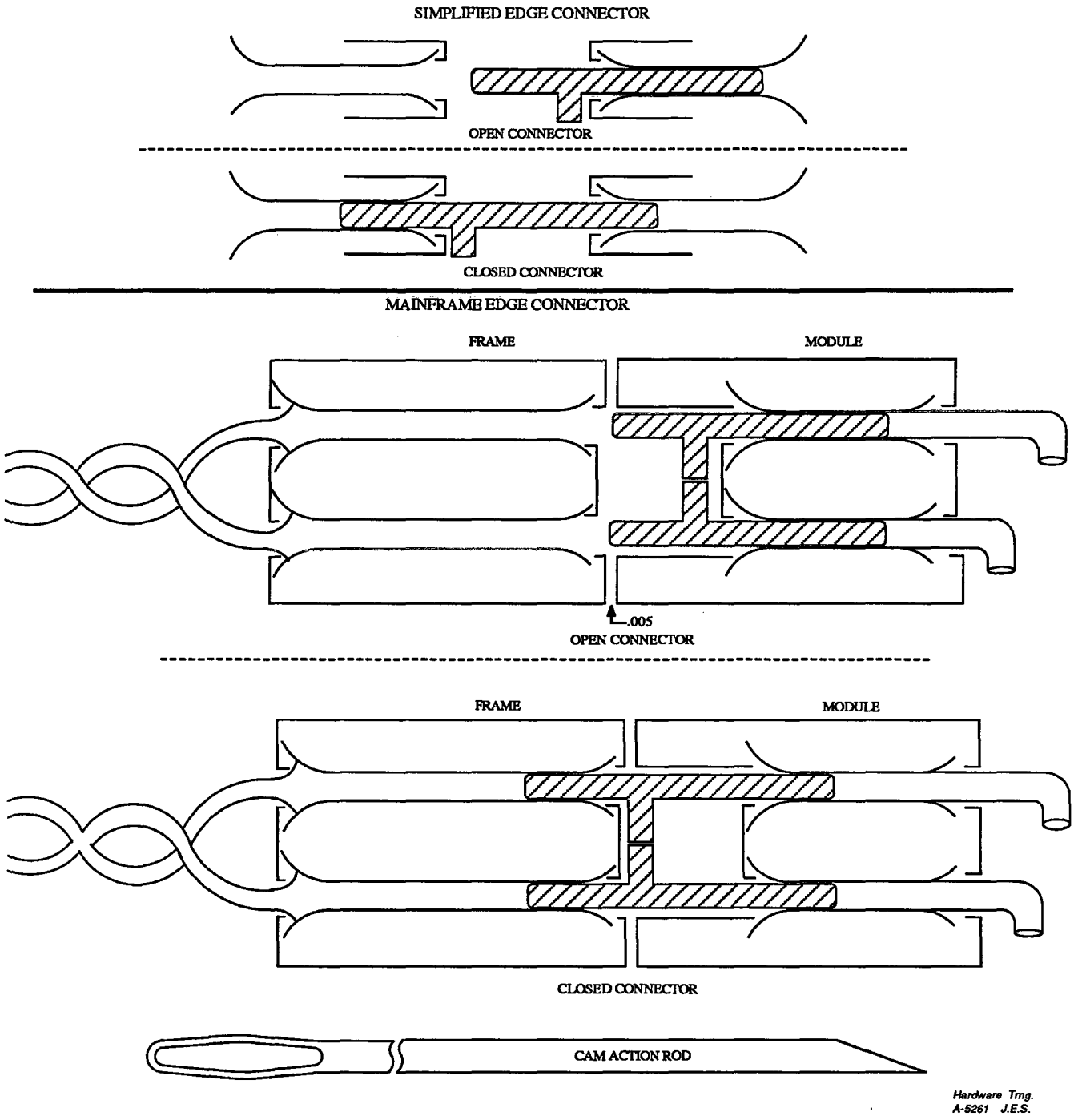


All pins will be stuffed into the pin blocks prior to assembly (no loose cage wires).

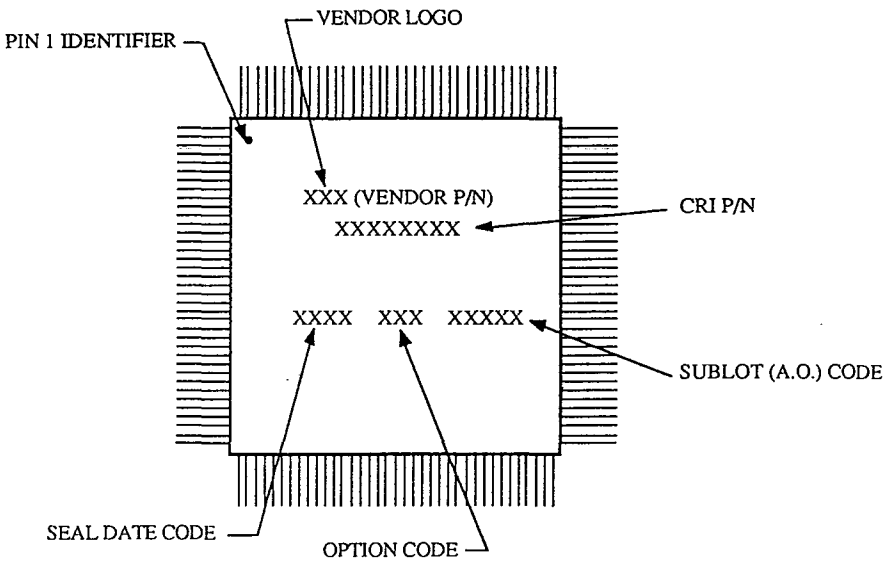
The pin lengths may be varied for each signal position in each block. A separate part number must be assigned for each block type. Please try to minimize the number of blocks.

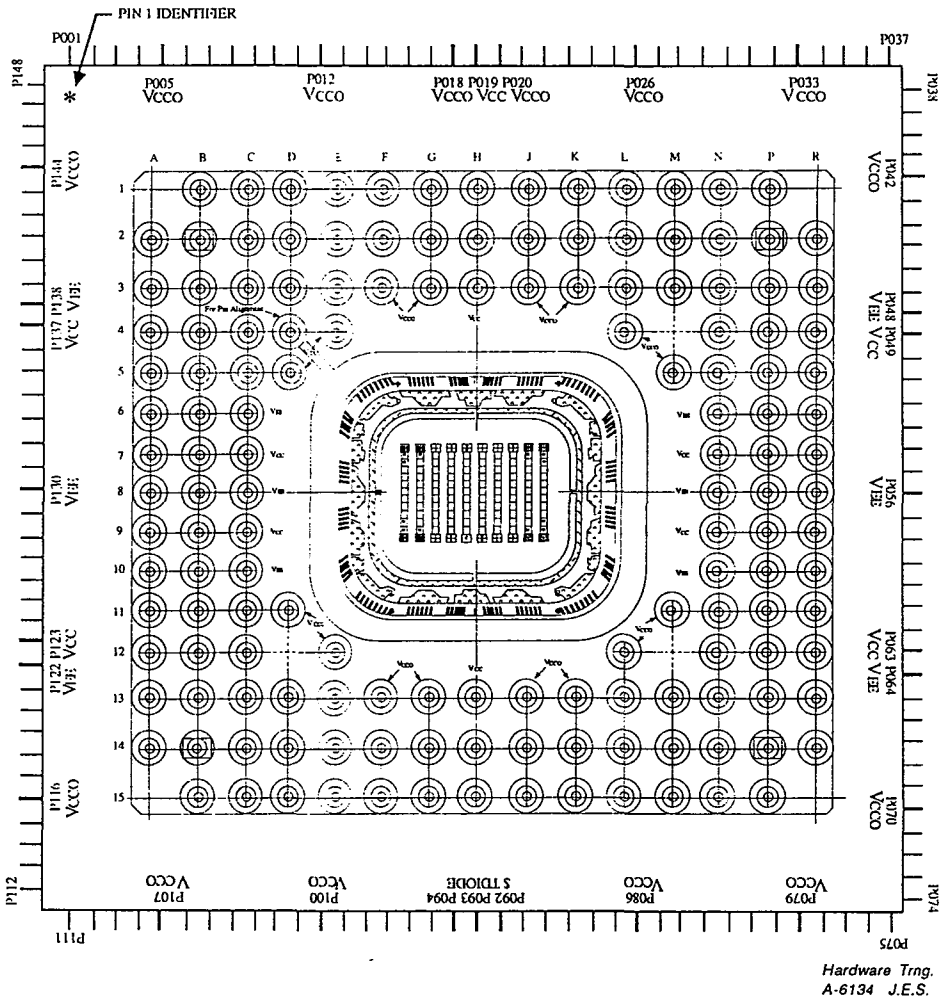
Hardware Trng.
A-6950 J.E.S.

CRAY Y-MP
POSSIBLE FEED THROUGH CONNECTOR PIN CONFIGURATIONS

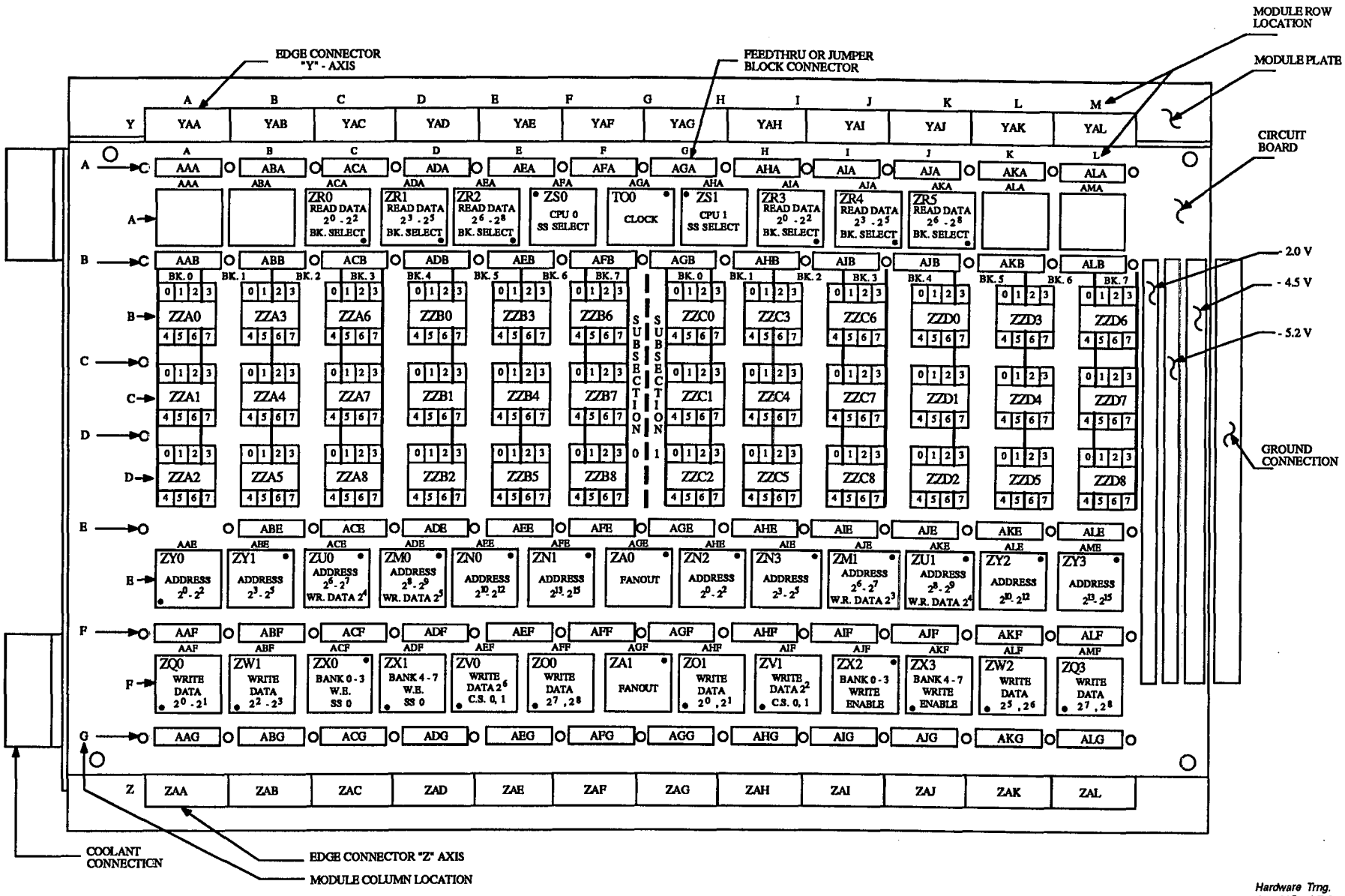


CRAY Y-MP EDGE CONNECTOR OPERATION

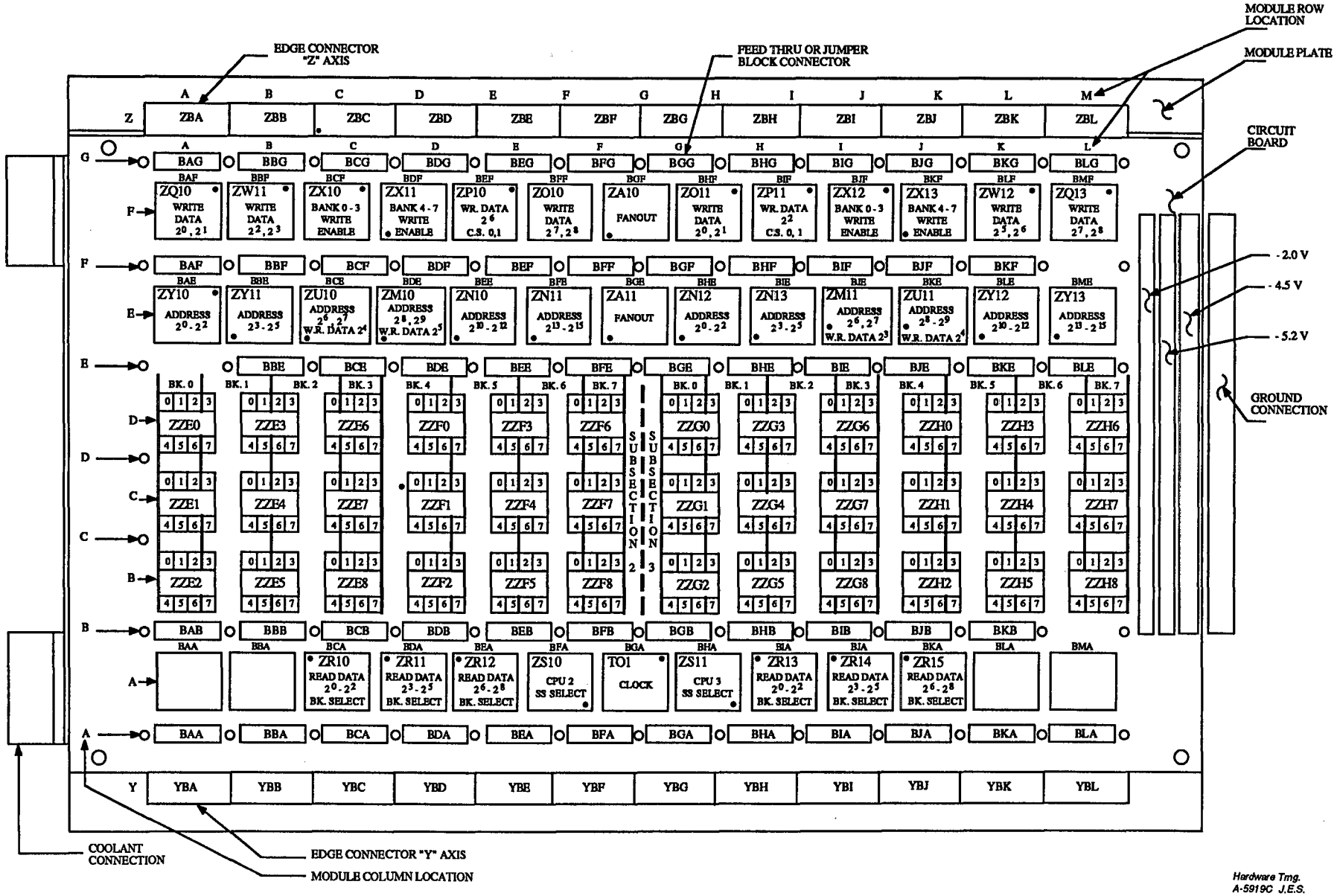




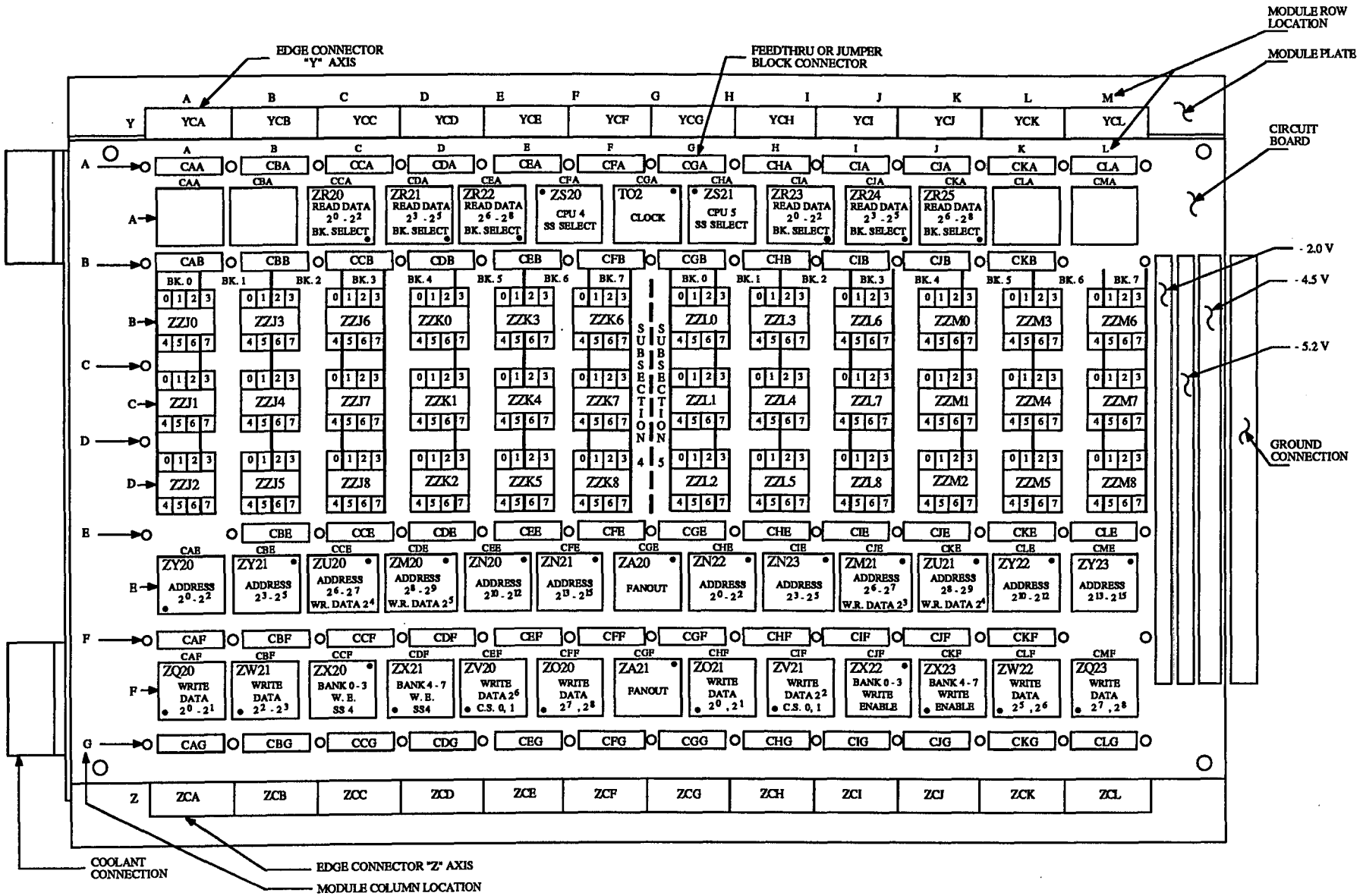
CRAY Y-MP PIN LOCATIONS FOR
148 PIN ARRAY PACKAGE



CRAY Y-MP MEMORY MAP
BOARD A

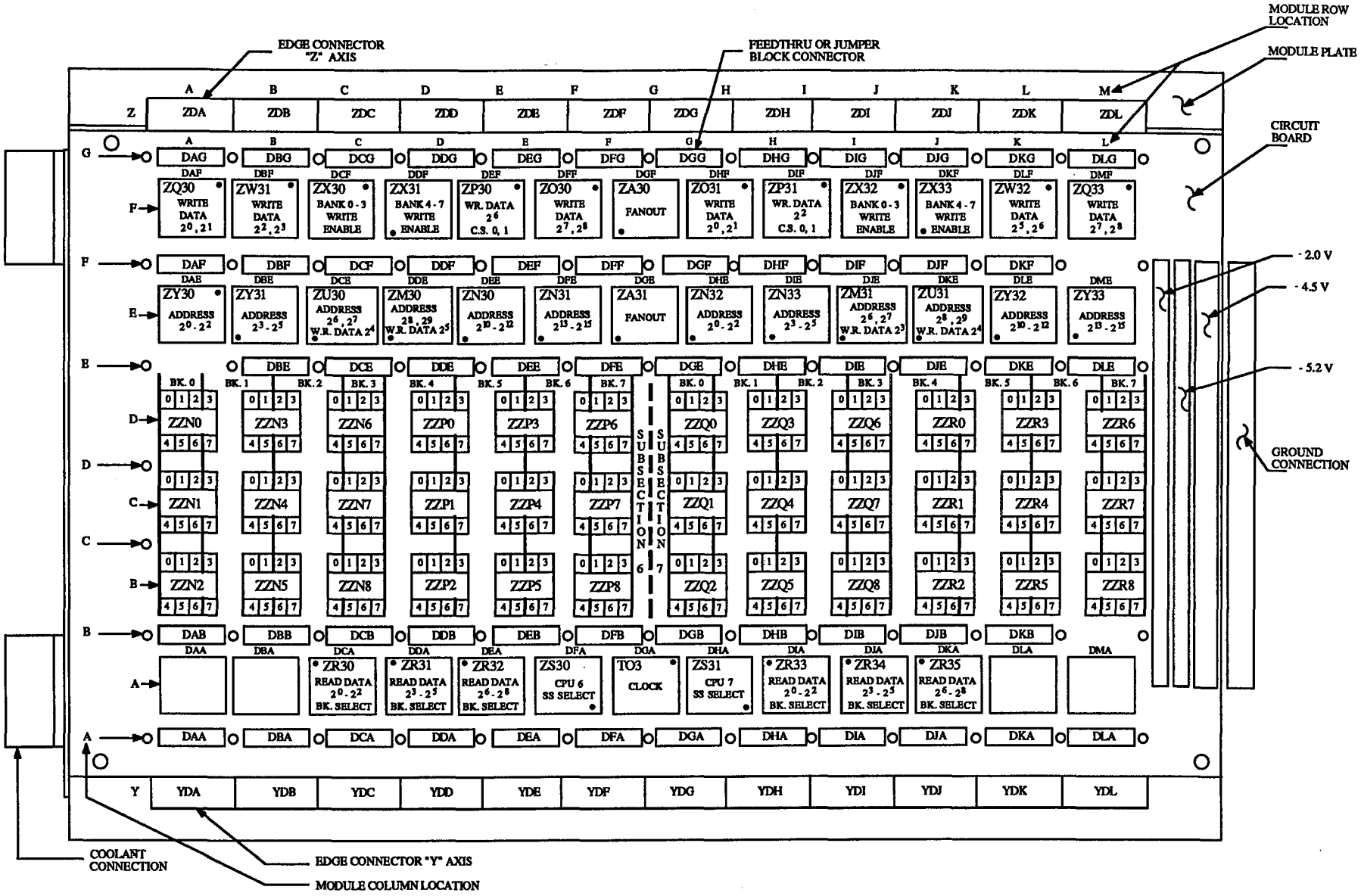


CRAY Y-MP MEMORY MAP
BOARD B

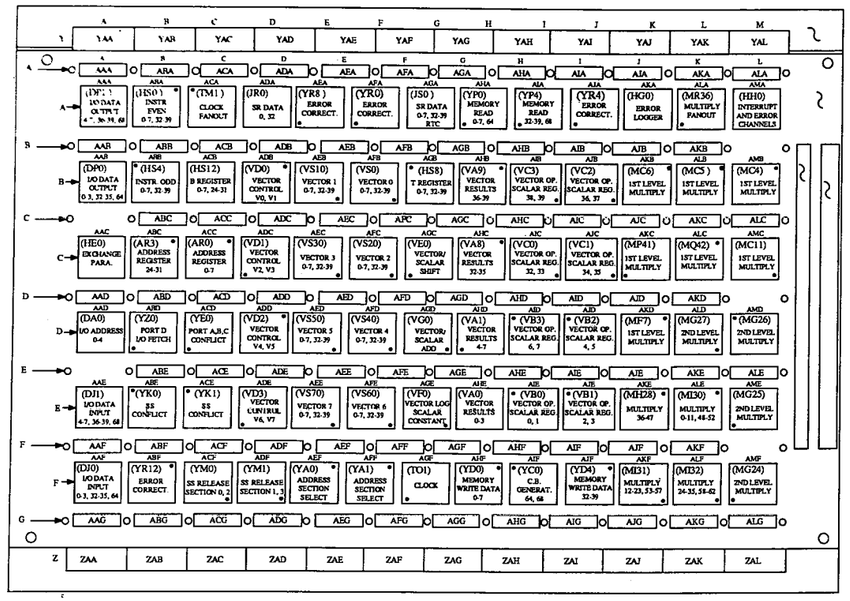


CRAY Y-MP MEMORY MAP
BOARD C

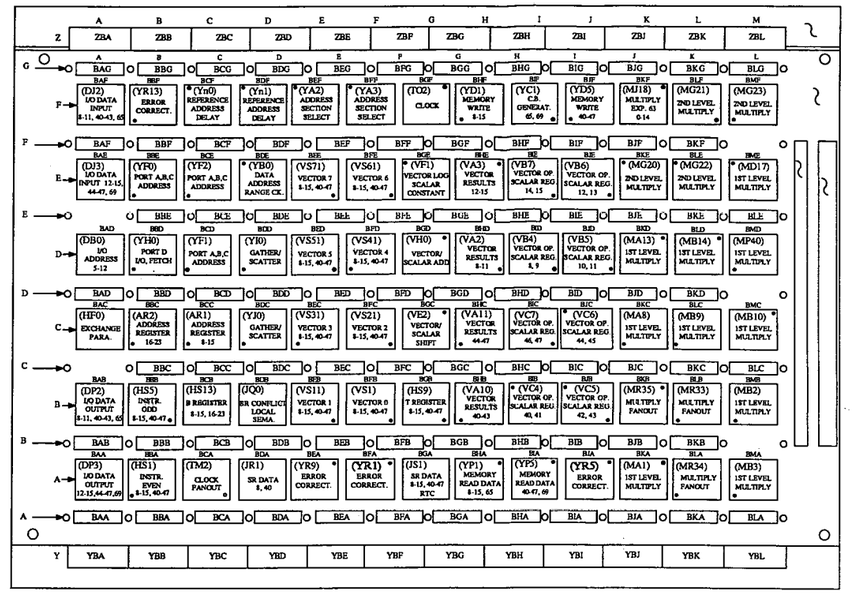
Hardware Tmg.
A-5920B J.E.S.



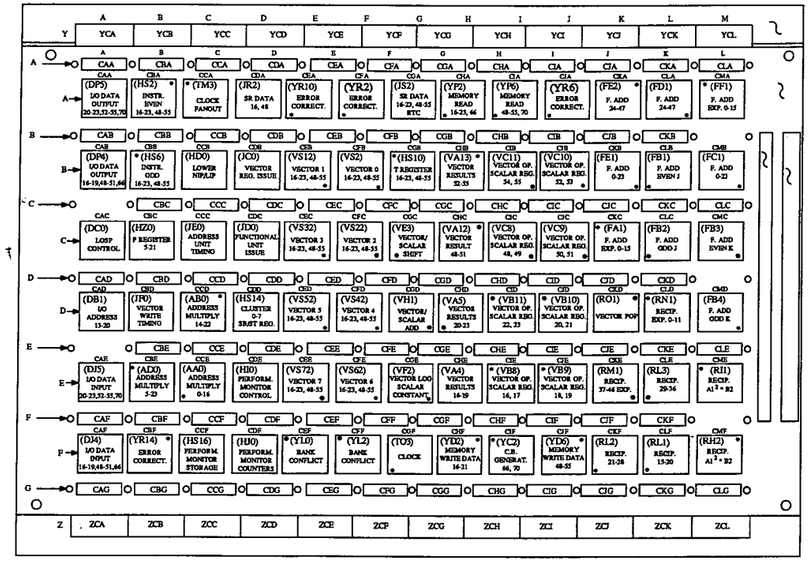
CRAY Y-MP MEMORY MAP
BOARD D



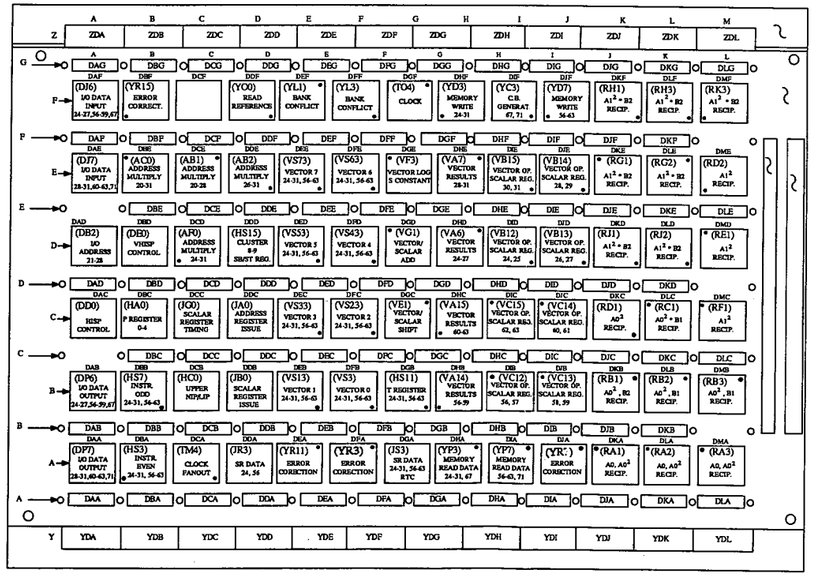
BOARD A (REV. 0)



BOARD B (REV. 0)



BOARD C (REV. 0)



BOARD D (REV. 0)

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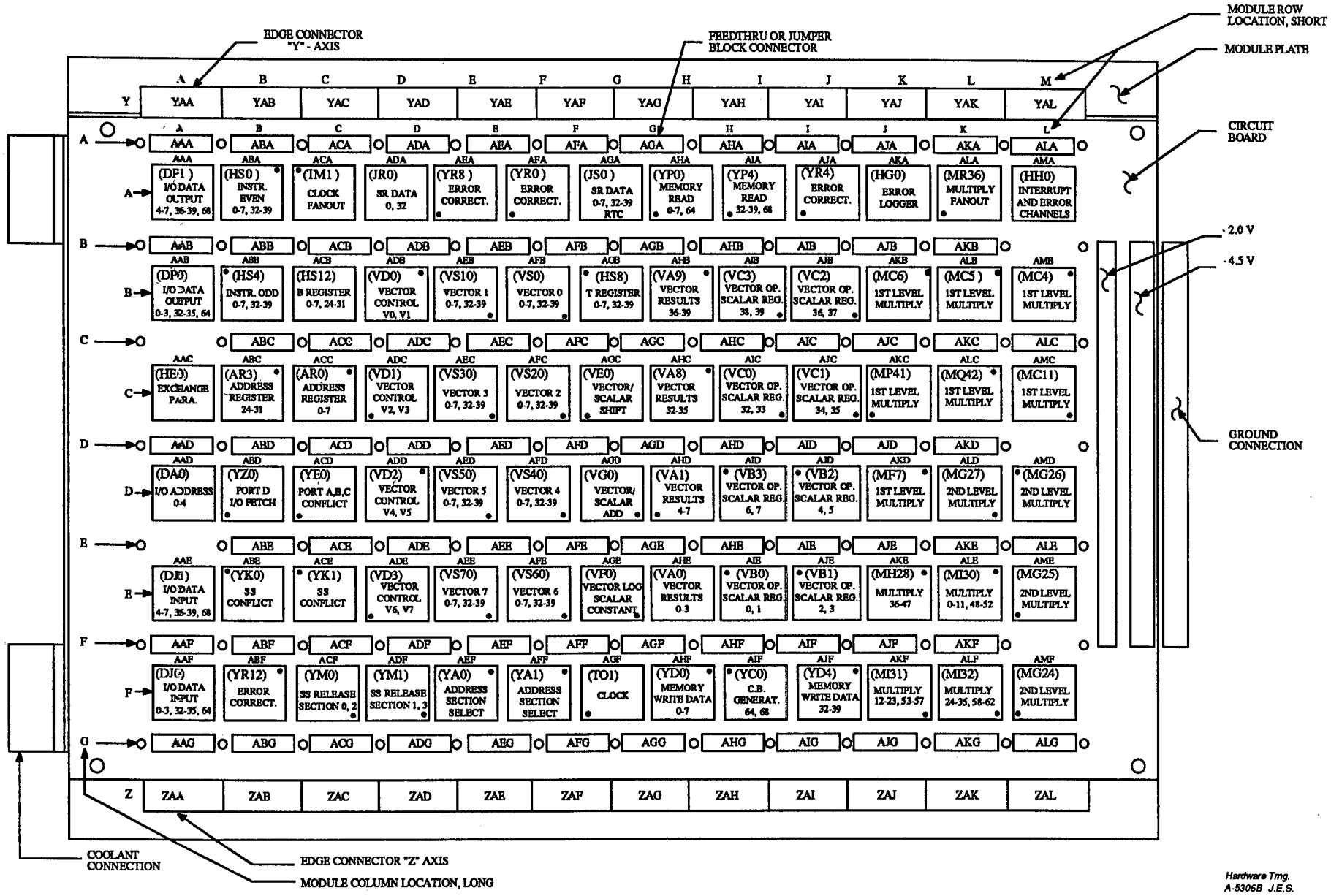
A-6346B J.E.S.

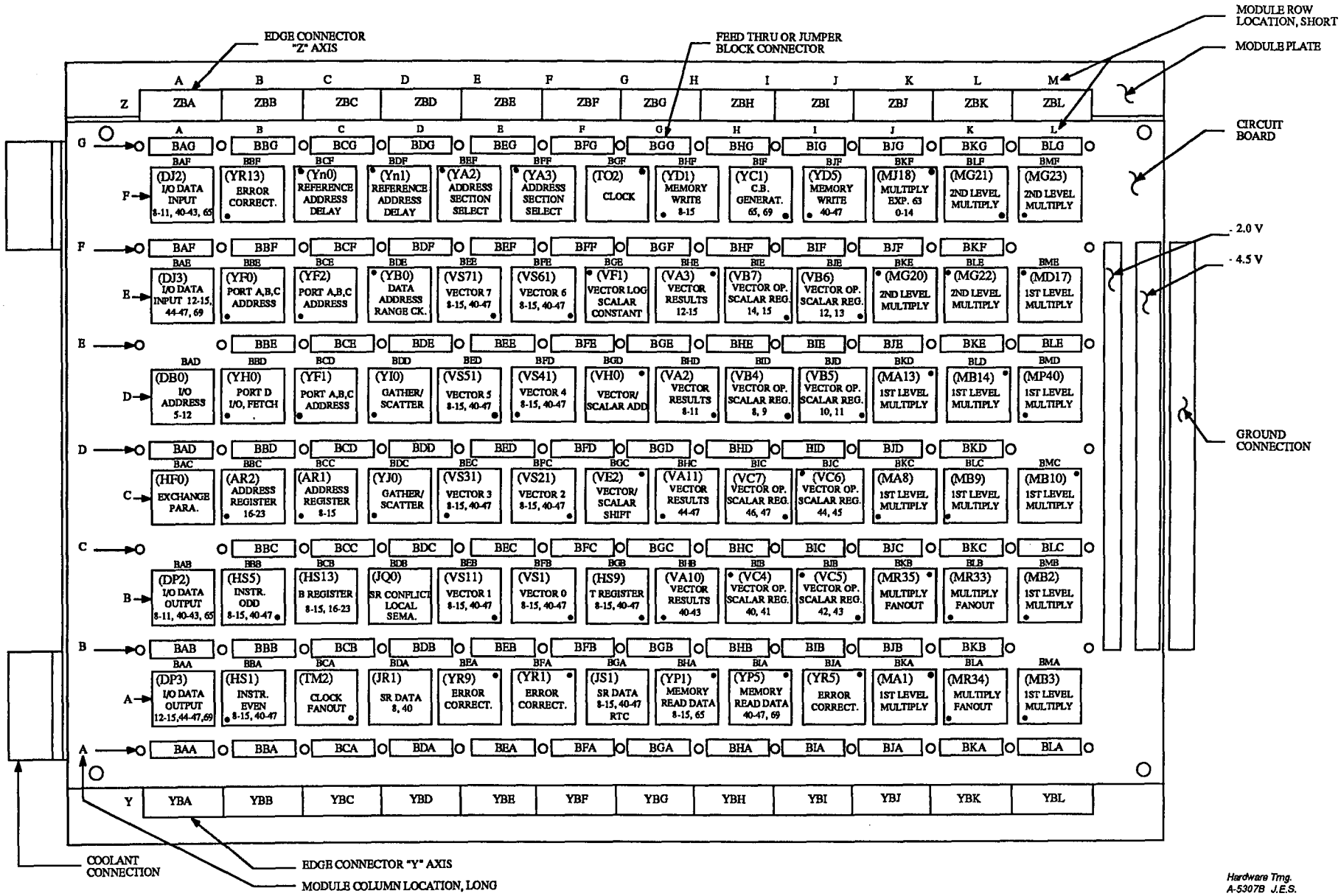
CRAY Y-MP CPU MAP - BOARDS A - D (REV. 0)

HTV-0834

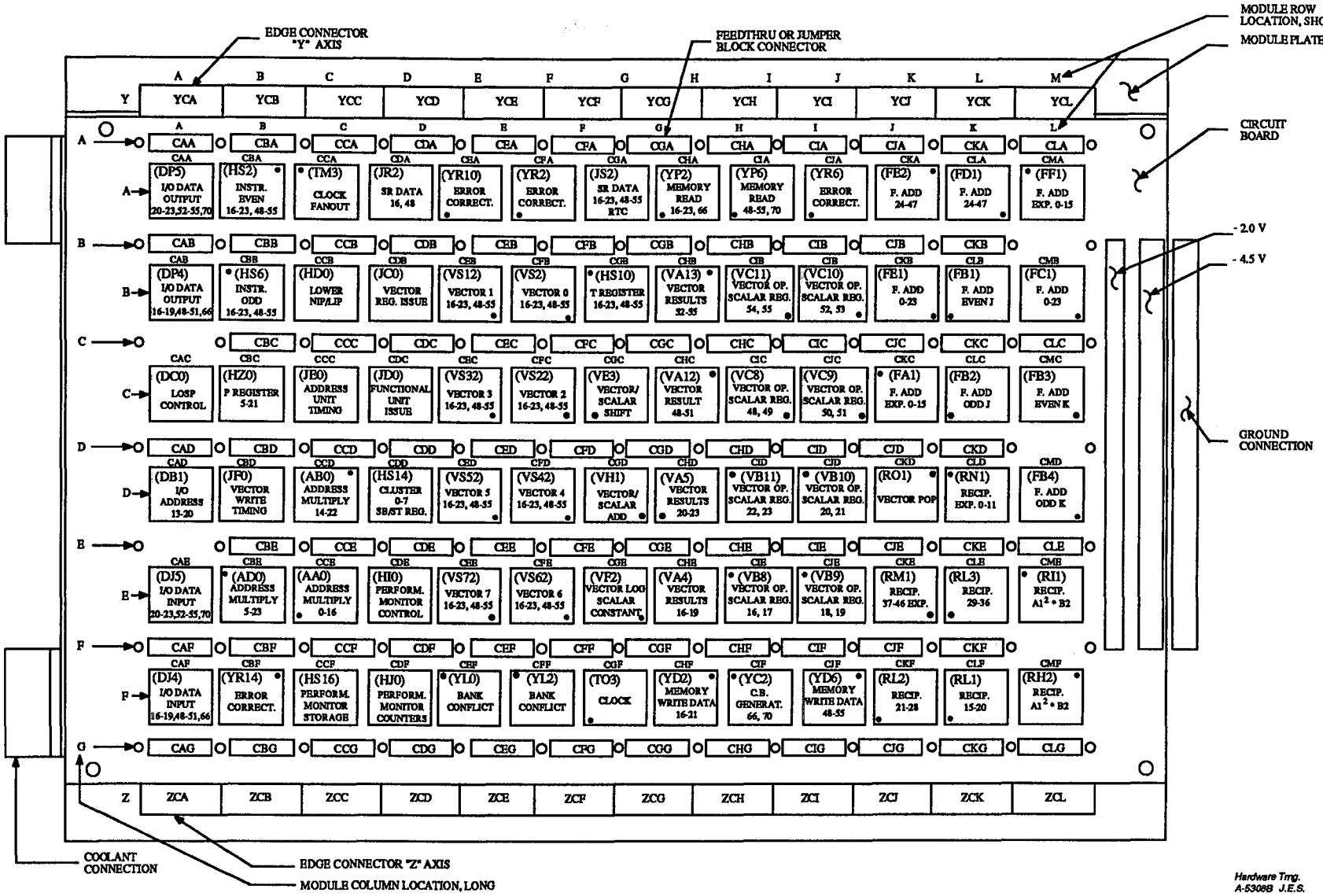
CRAY PROPRIETARY



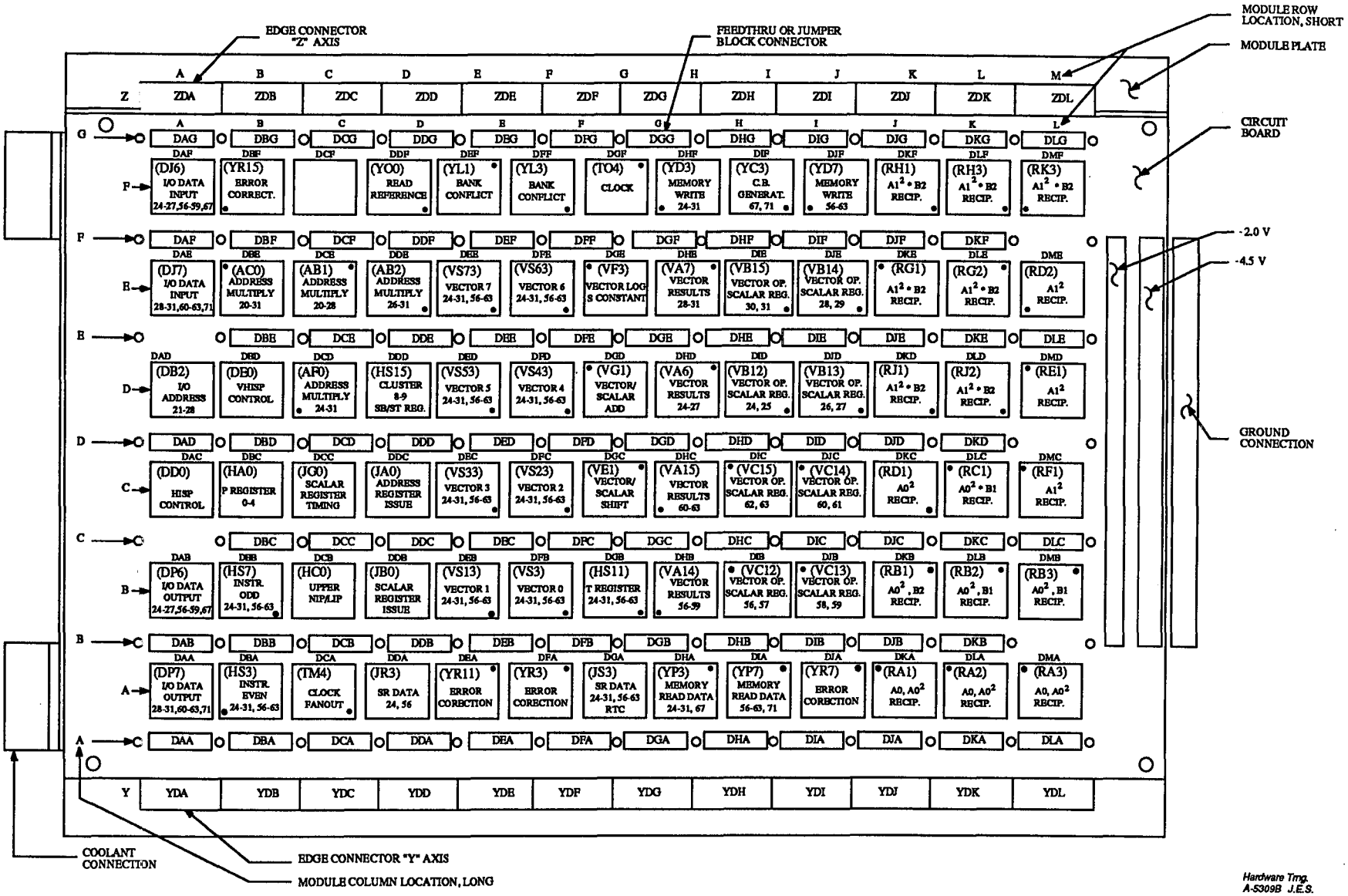
CRAY Y-MP CPU MAP - BOARD A (TRAINING USE ONLY)



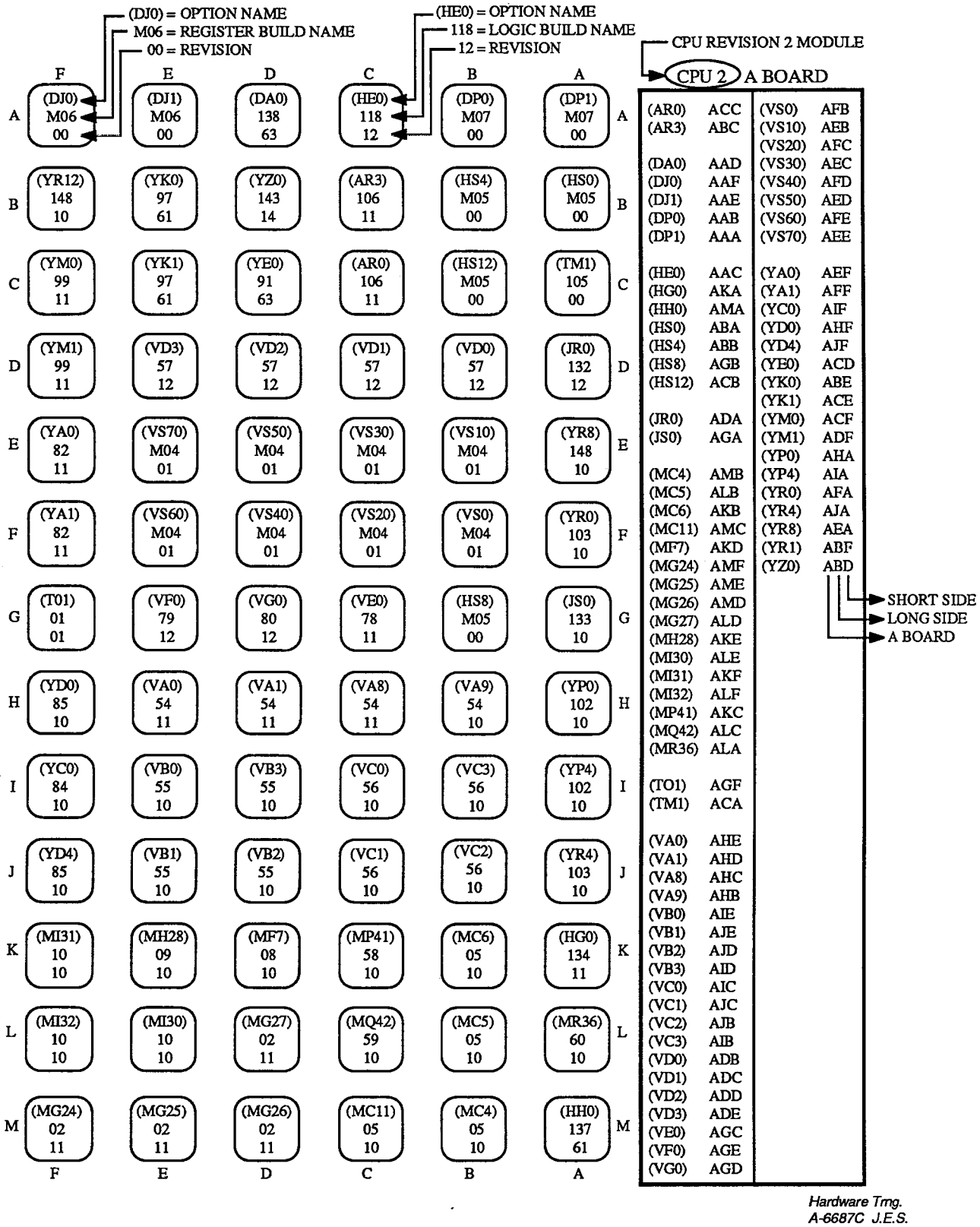
CRAY Y-MP CPU MAP - BOARD B
(TRAINING USE ONLY)



CRAY Y-MP CPU MAP - BOARD C
(TRAINING USE ONLY)



CRAY Y-MP CPU MAP - BOARD D
(TRAINING USE ONLY)



CRAY Y-MP MODULE A BOARD

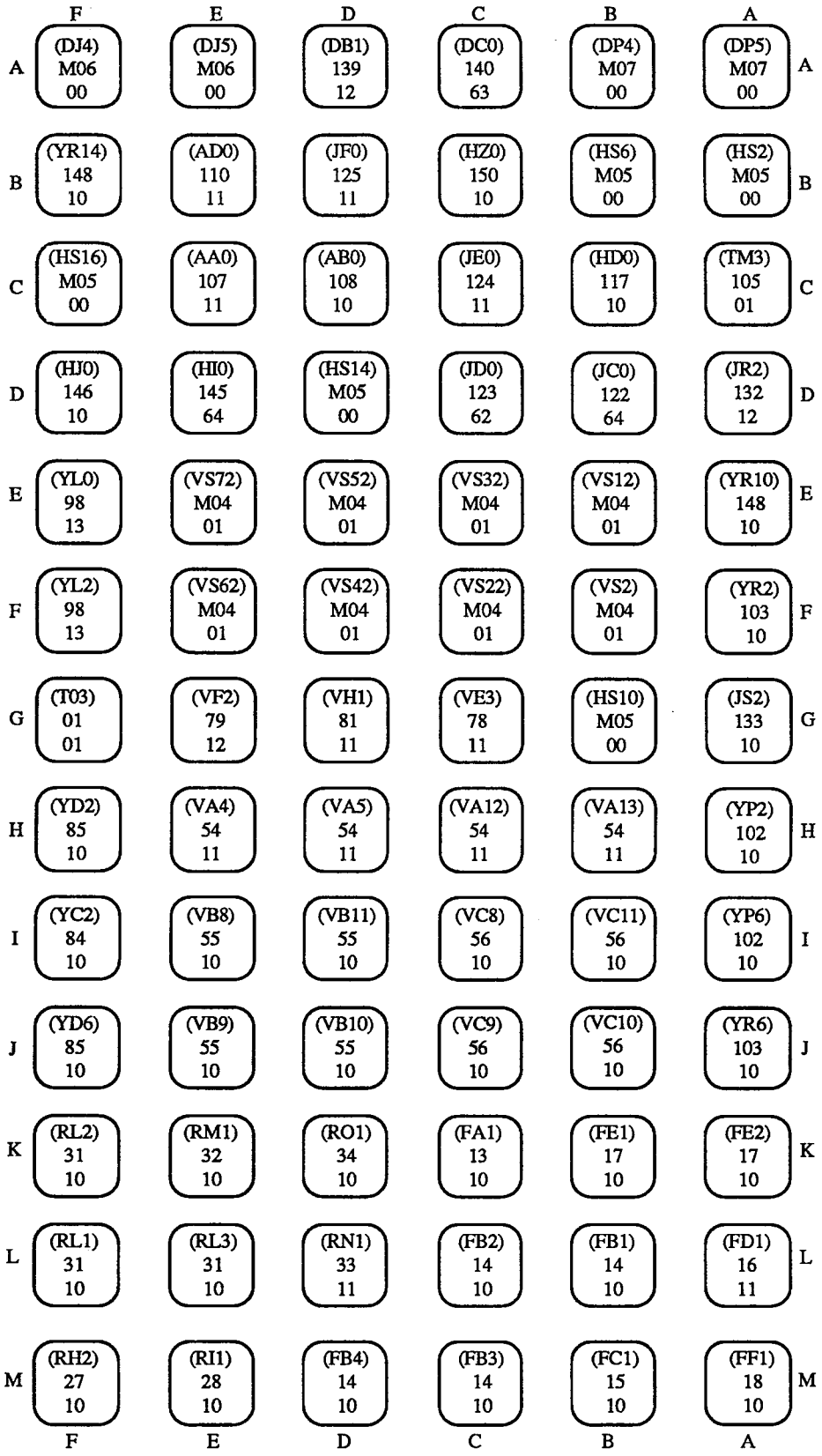
CPU 2 B BOARD

(AR1)	BCC	(VS41)	BFD
(AR2)	BBC	(VS51)	BED
		(VS61)	BFE
(DB0)	BAD	(VS71)	BEE
(DJ2)	BAF		
(DJ3)	BAE	(YA2)	BEF
(DP2)	BAB	(YA3)	BFF
(DP3)	BAA	(YB0)	BDE
		(YC1)	BIF
(HF0)	BAC	(YD1)	BHF
(HS1)	BBA	(YD5)	BJF
(HS5)	BBB	(YF0)	BBE
(HS9)	BGB	(YF1)	BCD
(HS13)	BCB	(YF2)	BCE
		(YH0)	BBD
(JQ0)	BDB	(YI0)	BDD
(JR1)	BDA	(YJ0)	BDC
(JS1)	BGA	(YN0)	BCF
		(YN1)	BDF
(MA1)	BKA	(YP1)	BHA
(MA8)	BKC	(YP5)	BIA
(MA13)	BKD	(YR1)	BFA
(MB2)	BMB	(YR5)	BJA
(MB3)	BMA	(YR9)	BEA
(MB9)	BLC	(YR13)	BBF
(MB10)	BMC		
(MB14)	BLD		
(MD17)	BME		
(MG20)	BKE		
(MG21)	BLF		
(MG22)	BLE		
(MG23)	BMF		
(MJ18)	BKF		
(MP40)	BMD		
(MR33)	BLB		
(MR34)	BLA		
(MR35)	BKB		
(TM2)	BCA		
(TO2)	BGF		
(VA2)	BHD		
(VA3)	BHE		
(VA10)	BHB		
(VA11)	BHC		
(VB4)	BID		
(VB5)	BJD		
(VB6)	BJE		
(VB7)	BIE		
(VC4)	BIB		
(VC5)	BJB		
(VC6)	BJC		
(VC7)	BIC		
(VE2)	BGC		
(VF1)	BGE		
(VH0)	BGD		
(VS1)	BFB		
(VS11)	BEB		
(VS21)	BFC		
(VS31)	BEC		

	A	B	C	D	E	F	
A	(DP3) M07 00	(DP2) M07 00	(HF0) 119 10	(DB0) 139 12	(DJ3) M06 00	(DJ2) M06 00	A
B	(HS1) M05 00	(HS5) M05 00	(AR2) 106 11	(YH0) 94 12	(YF0) 92 13	(YR13) 148 10	B
C	(TM2) 105 01	(HS13) M05 00	(AR1) 106 11	(YF1) 92 13	(YF2) 92 13	(YN0) 100 12	C
D	(JR1) 132 12	(JQ0) 131 66	(YJ0) 96 11	(YI0) 95 12	(YB0) 83 11	(YN1) 100 12	D
E	(YR9) 148 10	(VS11) M04 01	(VS31) M04 01	(VS51) M04 01	(VS71) M04 01	(YA2) 82 10	E
F	(YR1) 103 10	(VS1) M04 01	(VS21) M04 01	(VS41) M04 01	(VS61) M04 01	(YA3) 82 10	F
G	(JS1) 133 10	(HS9) M05 00	(VE2) 78 11	(VH0) 81 11	(VF1) 79 12	(TO2) 01 01	G
H	(YP1) 102 10	(VA10) 54 11	(VA11) 54 11	(VA2) 54 11	(VA3) 54 11	(YD1) 85 10	H
I	(YP5) 102 10	(VC4) 56 10	(VC7) 56 10	(VB4) 55 10	(VB7) 55 10	(YC1) 84 10	I
J	(YR5) 103 10	(VC5) 56 10	(VC6) 56 10	(VB5) 55 10	(VB6) 55 10	(YD5) 85 10	J
K	(MA1) 03 10	(MR35) 60 10	(MA8) 03 10	(MA13) 03 10	(MG20) 02 11	(MJ18) 11 10	K
L	(MR34) 60 10	(MR33) 60 10	(MB9) 04 10	(MB14) 04 10	(MG22) 02 11	(MG21) 02 11	L
M	(MB3) 04 10	(MB2) 04 10	(MB10) 04 10	(MP40) 58 10	(MD7) 06 10	(MG23) 02 11	M
	A	B	C	D	E	F	

Hardware Trng.
A-6682B J.E.S.

CRAY Y-MP CPU MODULE B BOARD

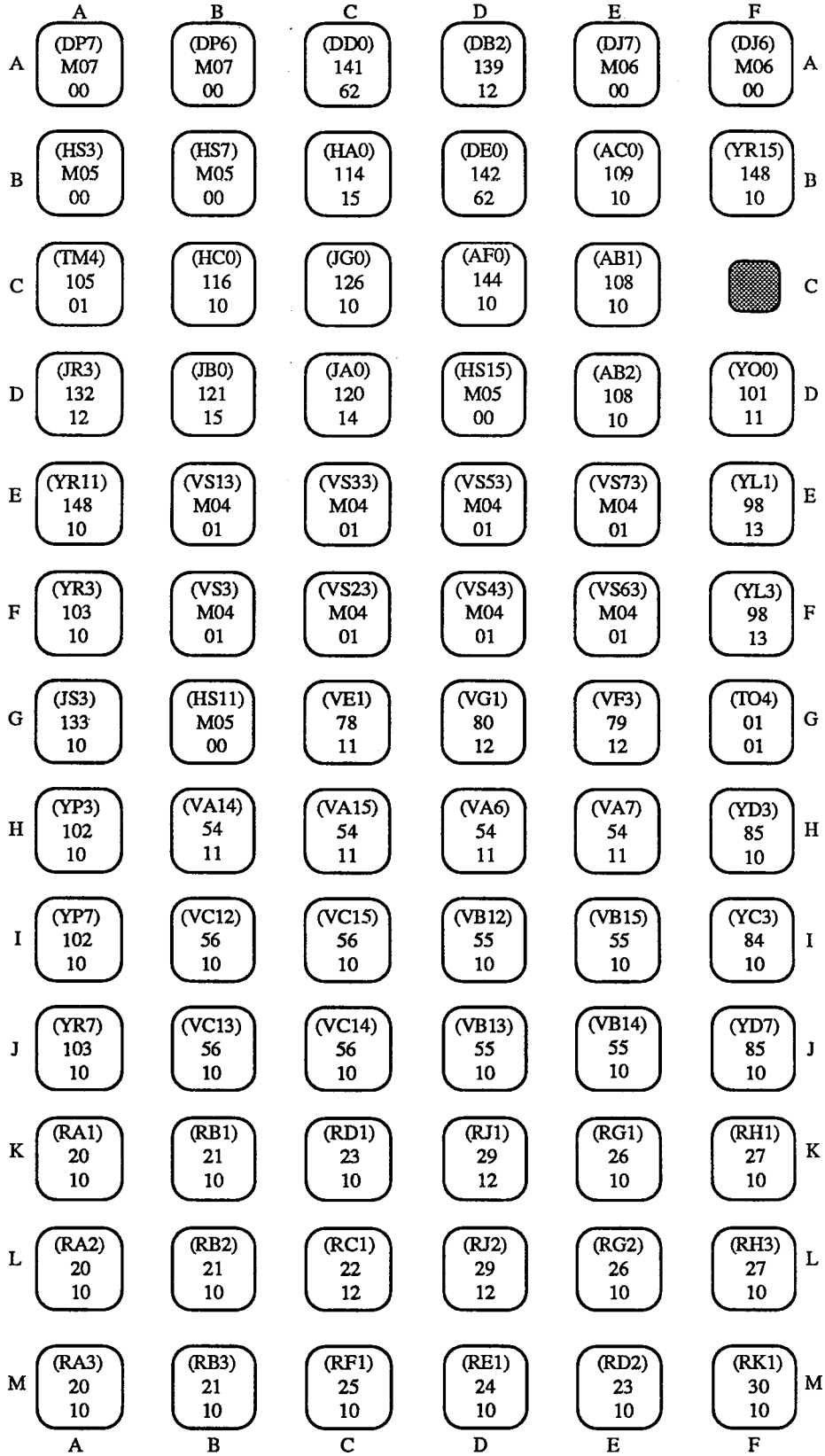


Hardware Trng.
A-6688B J.E.S.

CRAY Y-MP CPU MODULE C BOARD

CPU 2 D BOARD

(AB1)	DCE	(VF3)	DGE
(AB2)	DDE	(VG1)	DGD
(AC0)	DBE	(VS3)	DFB
(AF0)	DCD	(VS13)	DEB
		(VS23)	DFC
(DB2)	DAD	(VS33)	DEC
(DD0)	DAC	(VS43)	DFD
(DE0)	DBD	(VS53)	DED
(DJ6)	DAF	(VS63)	DFE
(DJ7)	DAE	(VS73)	DEE
(DP6)	DAB		
(DP7)	DAA	(YC3)	DIF
		(YD3)	DHF
(HA0)	DBC	(YD7)	DJF
(HC0)	DCB	(YL1)	DEF
(HS3)	DBA	(YL3)	DFF
(HS7)	DBB	(YO0)	DDF
(HS11)	DGB	(YP3)	DHA
(HS15)	DDD	(YP7)	DIA
		(YR3)	DFA
(JA0)	DDC	(YR7)	DJA
(JB0)	DDV	(YR11)	DEA
(JG0)	DCC	(YR15)	DBF
(JR3)	DDA		
(JS3)	DGA		
(RA1)	DKA		
(RA2)	DLA		
(RA3)	DMA		
(RB1)	DKB		
(RB2)	DLB		
(RB3)	DLC		
(RC1)	DKC		
(RD1)	DME		
(RD2)	DMD		
(RE1)	DMC		
(RF1)	DKE		
(RG1)	DLE		
(RG2)	DKF		
(RH1)	DLF		
(RH3)	DKD		
(RJ1)	DLD		
(RK1)	DMF		
(TM4)	DCA		
(TO4)	DGF		
(VA6)	DHD		
(VA7)	DHE		
(VA14)	DHB		
(VA15)	DHC		
(VB12)	DID		
(VB13)	DJD		
(VB14)	DJE		
(VB15)	DIE		
(VC12)	DIB		
(VC13)	DJB		
(VC14)	DJC		
(VC15)	DIC		
(VE1)	DGC		



Hardware Trng.
A-6689B J.E.S

CRAY Y-MP CPU MODULE D BOARD

CRAY Y-MP OPTION DESIGN STATUS

9-15-87

OPTION QUANTITY			ESTIMATED BOOLEAN RELEASED		
CPU Module Totals					
OP.	QTY.		EST.	BOL.	REL.
90	246	Motorola 2500	0	0	90
4	65	Register Memory	0	0	4
94	311		0	0	11
Memory Module Totals					
OP.	QTY.		EST.	BOL.	REL.
11	140	Motorola 2500	0	0	11
11	140		0	0	11

System Quantities

CPU Module - Motorola 246 x 8 Modules = 1968

CPU Module - Register 65 x 8 Modules = 520

Memory Module - Motorola 140 x 32 Modules = 4480

YM18/08

A series: Address Functions

OP.	QTY.	Function	EST.	BOL.	REL.
(AA)	1	Address Multiply			X
(AB)	3	" "			X
(AC)	1	" "			X
(AD)	1	" "			X
(AE)	1	" "			X
(AR)	4	Address Registers			X
6	11		0	0	6

D series: I/O

OP.	QTY.	Function	EST.	BOL.	REL.
(DA)	1	I/O Lower Address, Reference Control			X
(DB)	3	I/O Upper Address			X
(DC)	1	I/O Control			X
(DD)	1	I/O Control			X
(DE)	1	I/O Control			X
(DJ)	8 Reg.	Input Buffer			X
(DP)	8 Reg.	Output Buffer			X
7	23		0	0	7

F series: Floating-point Adder

OP.	QTY.	Function	EST.	BOL.	REL.
(FA)	1	Exponent Control			X
(FB)	4	Coefficient Alignment			X
(FC)	1	Final Sum 0 - 23			X
(FD)	1	Final Sum 24 - 47			X
(FE)	2	Coefficient Normalize			X
(FF)	1	Final Exponent Adjust			X
6	10		0	0	6

YM18/09

H series: Instruction Control

OP.	QTY.	Function	EST.	BOL.	REL.
(HA)	1	Lower Program Counter			X
(HB)	1	Upper Program Counter			X
(HC)	1	Upper NIP/LIP gh			X
(HD)	1	Lower NIP/LIP ijk			X
(HE)	1	Exchange Parameters XA, VL, CLN, Flags, Modes			X
(HF)	1	Exchange Parameters P, IBA, ILA, DBA, DLA			X
(HG)	1	Exchange Parameters Errors			X
(HH)	1	Error Log			X
(HI)	1	Performance Log			X
(HJ)	1	Performance Log Counters			X
(HS)	17 Reg.	Instruction Buffer/B/T/PM/Shared Registers			X
11	27		0	0	10

J series: Instruction Issue

OP.	QTY.	Function	EST.	BOL.	REL.
(JA)	1	Address Register Issue			X
(JB)	1	Scalar Register Issue			X
(JC)	1	Vector Register Issue			X
(JD)	1	Functional Unit Issue			X
(JE)	1	Address Register Timing/Functional Unit Timing			X
(JF)	1	Vector Write Timing			X
(JG)	1	Scalar Register Timing			X
(JQ)	1	Shared Register Control			X
(JR)	4	Shared Register Data Select			X
(JS)	4	CPU Shared Register Data - RT/PC			X
10	16		0	0	10

M series: Floating-point Multiply

OP.	QTY.	Function	EST.	BOL.	REL.
(MA)	3	First Level Multiply			X
(MB)	5	" " "			X
(MC)	4	" " "			X
(MD)	1	" " "			X
(MF)	1	" " "			X
(MG)	8	Second Level Multiply			X
(MH)	1	Final Sum 83 - 95			X
(MI)	3	Final Sum 47 - 58, 59 - 70, 71 - 82			X
(MJ)	1	Multiply Control and Exponent			X
(MP)	2	First Level Multiply			X
(MQ)	1	" " "			X
(MR)	4	Operand Delay			X
12	34		0	0	12

YM18/10

R series: Floating-point Reciprocal

OP.	QTY.	Function	EST.	BOL.	REL.
(RA)	3	Table Look-up A0, A0**2			X
(RB)	3	A0**2 x B1			X
(RC)	1	A0**2 x B1			X
(RD)	2	A1, A1**2 Final Sum			X
(RE)	1	A1**2 Sum -36 to -19			X
(RF)	1	" " -18 to -1			X
(RG)	2	A1**2 x B2 -33 to -25			X
(RH)	3	" " N - 26 to N - 18			X
(RI)	1	" " -12 to -2			X
(RJ)	2	" " -38 to -32			X
(RK)	1	" " -38 to -13			X
(RL)	3	Result 15 - 20, 21 - 28, 29 - 36			X
(RM)	1	Result 37 - 46			X
(RN)	1	Result 47 - 63			X
(RO)	1	Vector Pop Count			X
15	26		0	0	15

T series: Clock Fanout

OP.	QTY.	Function	EST.	BOL.	REL.
(TO)	8	Clock Fanout			X
1	8		0	0	1

V series: Vector/Scalar Functions

OP.	QTY.	Function	EST.	BOL.	REL.
(VA)	16	Vector Results			X
(VB)	16	Vector Operands/Scalar Registers - Lower			X
(VC)	16	Vector Operands/Scalar Registers - Upper			X
(VD)	4	Vector Register Control			X
(VE)	4	Vector/Scalar Shift			X
(VF)	4	Vector Mask/Ak/ Scalar Constant			X
(VG)	2	Vector/Scalar Add-Shift Control (FP Modes)			X
(VH)	2	Vector/Scalar Add-Scalar Pop/Leadz			X
(VS)	32 Reg.	Vector Registers			X
9	96		0	0	9

YM18/11

Y series: Memory Access

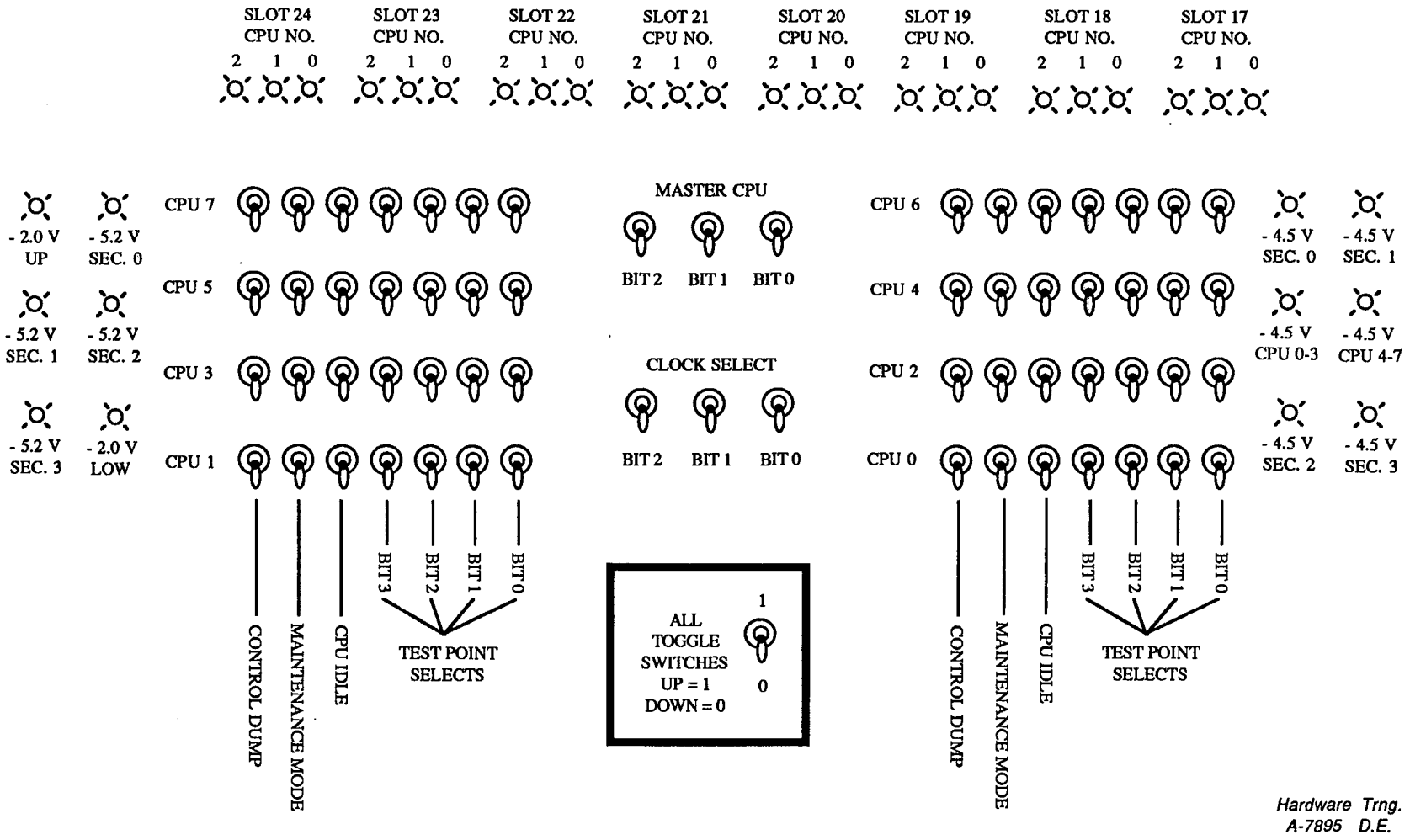
OP.	QTY.	Function	EST.	BOL.	REL.
(YA)	4	Address Selection Select			X
(YB)	1	Data Address Range Check			X
(YC)	4	Memory Check Byte Generation			X
(YD)	8	Memory Write Data Selection			X
(YE)	1	Port A, B, C Lower Address			X
(YF)	3	Port A, B, C Upper Address			X
(YZ)	1	Port D Lower Address			X
(YH)	1	Port D Upper Address			X
(YI)	1	Gather/Scatter Lower Address Stack-Ar Data			X
(YJ)	1	Gather/Scatter Upper Address Stack			X
(YK)	2	Subsection Conflict			X
(YL)	4	Bank Conflict			X
(YM)	2	Subsection Release Conflict			X
(YN)	2	Reference Address Delay			X
(YO)	1	Read Reference /Control Delay			X
(YP)	8	Memory Read Data Selection			X
(YR)	16	Error Correction - I/O Check Byte			X
17	60		0	0	17

MEMORY MODULE

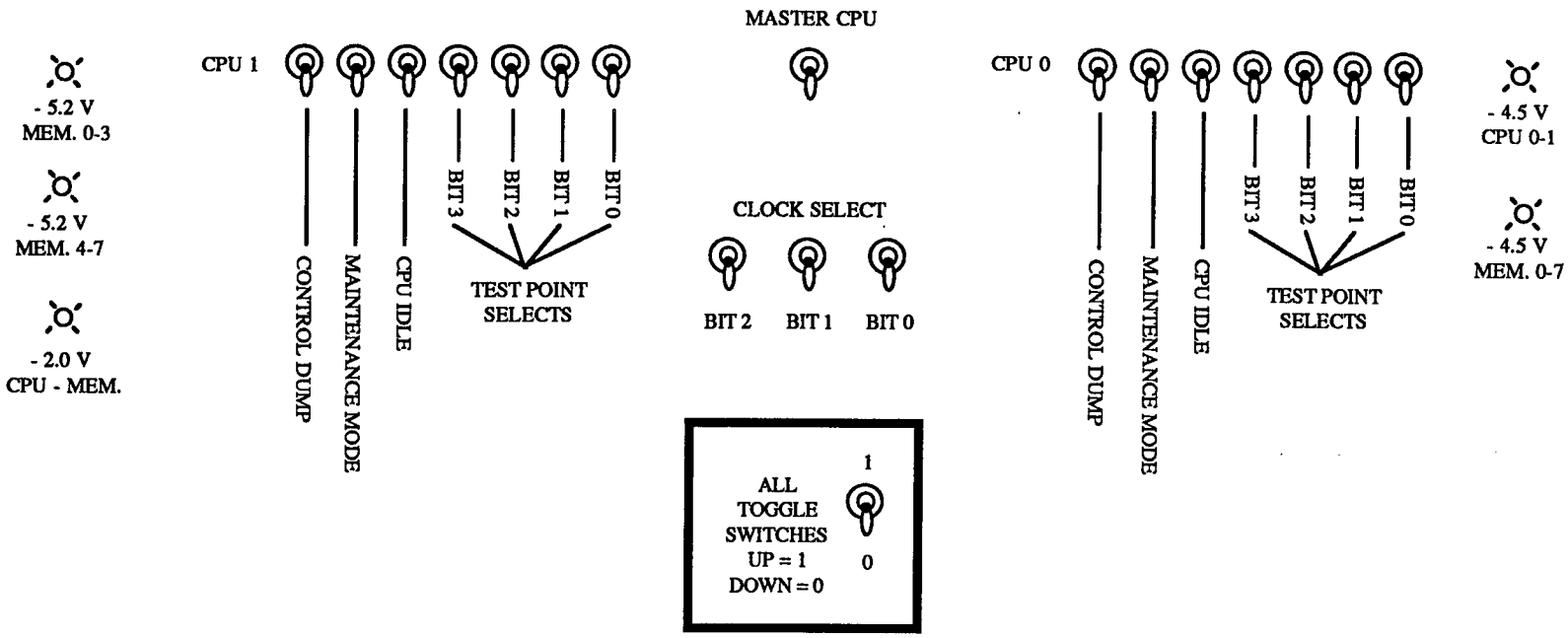
Z series: Memory

OP.	QTY.	Function	EST.	BOL.	REL.
(ZA)	8	Fanout			X
(ZM)	8	Address, Data Go SS Fanout			X
(ZN)	16	Address, CPU Bank Select			X
(ZO)	8	Data, 1 - 8 Fanout			X
(ZR)	24	Subsection Read Data			X
(ZS)	8	CPU Read Data			X
(ZU)	8	Address, Data, Go SS Fanout			X
(ZV)	8	Chip Select, Delay			X
(ZW)	16	Data, 1 - 8 Fanout			X
(ZX)	16	Bank Conflict			X
(ZY)	16	Address, CPU Bank Select			X
	4	Clock Fanout (TO)			
11	140		0	0	11

YM18/12A



CRAY Y-MP 8/32 MAINTENANCE PANEL

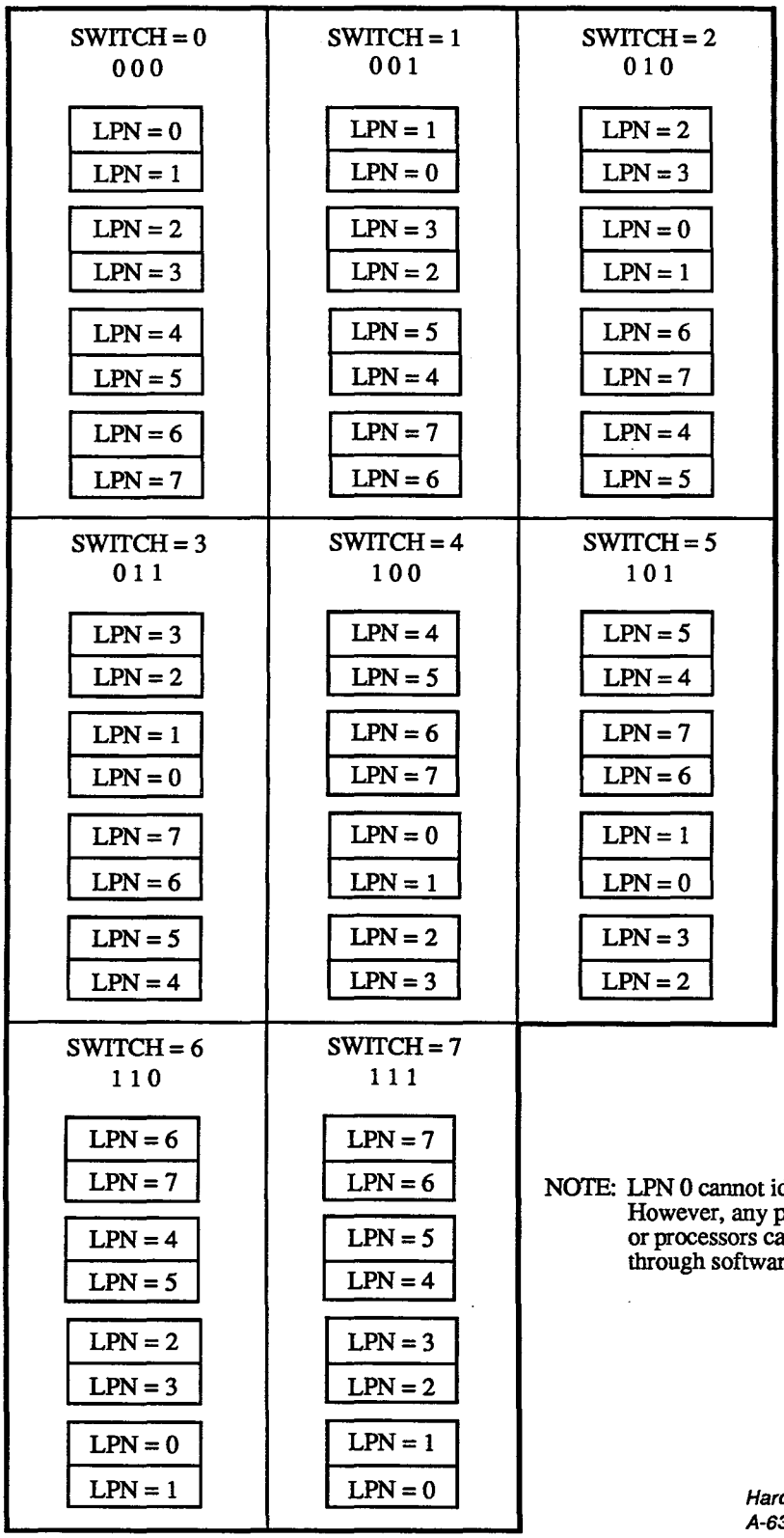


CRAY Y-MP 2/8 MAINTENANCE PANEL

CLOCK SWITCHES			DESCRIPTION	
BIT 2	BIT 1	BIT 0	FREQUENCY	PERIOD
0	0	0	160 MHz	6.25 ns
0	0	1	163 MHz	6.14 ns
0	1	0	166.667 MHz	6.00 ns
0	1	1	170 MHz	5.88 ns
1	0	0	AUXILIARY 0	
1	0	1	AUXILIARY 1	
1	1	0	CONHEX - EXTERNAL	
1	1	1	AUXILIARY 3	

Hardware Trng.
A-7897 D.E.

CRAY Y-MP 8/32 MAINTENANCE PANEL CLOCK SELECT



NOTE: LPN 0 cannot idle. However, any processor or processors can be idled through software.

Hardware Trng.
A-6391 J.E.S.

CRAY Y-MP LOGICAL PROCESSOR NUMBER LPN SWITCH SETTINGS

5.100 ns = 196.078 MHz
5.200 ns = 192.307 MHz
5.300 ns = 188.679 MHz
5.400 ns = 185.185 MHz
5.500 ns = 181.818 MHz
5.600 ns = 178.571 MHz
5.700 ns = 175.438 MHz
5.800 ns = 172.413 MHz
5.882 ns = 170.000 MHz
5.900 ns = 169.491 MHz
6.000 ns = 166.666 MHz
6.100 ns = 163.934 MHz
6.135 ns = 163.000 MHz
6.200 ns = 161.290 MHz
6.250 ns = 160.000 MHz
6.300 ns = 158.730 MHz
6.400 ns = 156.250 MHz
6.500 ns = 153.846 MHz
6.600 ns = 151.515 MHz
6.700 ns = 149.253 MHz
6.800 ns = 147.058 MHz
6.900 ns = 144.927 MHz
7.000 ns = 142.857 MHz
7.100 ns = 140.845 MHz
7.200 ns = 138.888 MHz
7.300 ns = 136.986 MHz
7.400 ns = 135.135 MHz
7.500 ns = 133.333 MHz
7.600 ns = 131.578 MHz
7.700 ns = 129.870 MHz
7.800 ns = 128.205 MHz
7.900 ns = 126.582 MHz
8.000 ns = 125.000 MHz
8.100 ns = 123.456 MHz
8.200 ns = 121.951 MHz
8.300 ns = 120.481 MHz
8.400 ns = 119.047 MHz
8.500 ns = 117.647 MHz
8.600 ns = 116.279 MHz
8.700 ns = 114.942 MHz
8.800 ns = 113.636 MHz
8.900 ns = 112.359 MHz
9.000 ns = 111.111 MHz
9.100 ns = 109.890 MHz
9.200 ns = 108.695 MHz
9.300 ns = 107.526 MHz
9.400 ns = 106.382 MHz
9.500 ns = 105.263 MHz
9.600 ns = 104.166 MHz
9.700 ns = 103.092 MHz
9.800 ns = 102.040 MHz
9.900 ns = 101.010 MHz
10.000 ns = 100.000 MHz

CRAY Y-MP MEGAHERTZ TO NANOSECOND

YM20/01A

CRAY Y-MP CPU TO MEMORY SECTION PRIORITY SCHEME

SECTION		0		1		2		3	
SUB SECTION		0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7
CPU PATH	0	A	H	D	E	C	F	B	G
	1	B	G	A	H	D	E	C	F
	2	C	F	B	G	A	H	D	E
	3	D	E	C	F	B	G	A	H
	4	H	A	E	D	F	C	G	B
	5	G	B	H	A	E	D	F	C
	6	F	C	G	B	H	A	E	D
	7	E	D	F	C	G	B	H	A

OUTBOARD FANOUT CN 0 - 7

CN 0 CPU A	CN 1 CPU B	CN 2 CPU C	CN 3 CPU D	CN 4 CPU E	CN 5 CPU F	CN 6 CPU G	CN 7 CPU H

CRAY Y-MP MAINTENANCE PANEL SELECTION SCHEME

SWITCH SETTING (CPU 0 MASTER)

	0	1	2	3	4	5	6	7
0	0	1	2	3	4	5	6	7
1	1	0	3	2	5	4	7	6
2	2	3	0	1	6	7	4	5
3	3	2	1	0	7	6	5	4
4	4	5	6	7	0	1	2	3
5	5	4	7	6	1	0	3	2
6	6	7	4	5	2	3	0	1
7	7	6	5	4	3	2	1	0

PHYSICAL CPU

A-7318A

CRAY Y-MP SYSTEM CONFIGURATION

CRAY Y-MP Mainframe Configuration

Specifications	2/116	2/216	4/116	4/132	4/216	4/232	4/416	4/432	8/432	8/464	8/832	8/864
CPUs	1	2	1	1	2	2	4	4	4	4	8	8
Central Memory Type Mem 128, Mem 64, Mem 32	Mem 64	Mem 64	Mem 32	Mem 64	Mem 32	Mem 64	Mem 32	Mem 64	Mem 32	Mem 64	Mem 32	Mem 64
Size (Mwords)	16	16	16	32	16	32	16	32	32	64	32	64
Banks	64	64	128	128	128	128	128	128	256	256	256	256
Modules	8	8	16	16	16	16	16	16	32	32	32	32
I/O Channels												
Low-speed (LOSP - 6 Mbytes)	1	2	1	1	2	2	4	4	4	4	8	8
High-speed (HISP - 100 Mbytes)	1	2	1	1	2	2	4	4	4	4	8	8
Very High-speed (VHISP - 1000 Mbytes)	1	1	1	1	1	1	2	2	2	2	2	2
Shared Register Clusters	7	7	7	7	7	7	7	7	7	7	9	9

Hardware Trng.
YM36/11 J.E.S.

CRAY Y-MP COOLING

Heat Load

The heat generated by the chips is conducted away from the die through the bottom of the chip case directly to the bottom plate. To ensure good thermal conductivity, a thin layer of conductive grease is applied between the chip and the bumps on the module plate. The power for each logic chip averages 7.5 watts for 4.5 volts and 1.5 watts for 2 volts for a total of 9 watts per chip. With 78 chips per board, this amounts to 2,808 watts per CPU module. The memory boards have 39 logic chips and 288 memory chips. Since the average power per memory chip is 1.25 watts, the heat generated by the memory module is 2,844 watts. The heat generated by the power supplies (the inefficiency of the supply), the heat generated by the buck transformers, and the loss in the diodes (a voltage drop of .7 volts times the 2,200 amps) amounts to a total of 45,000 watts. There are eight modules per eight CPUs in the CRAY Y-MP for a total of 22,464 watts. Also, there are 32 modules per memory for a total of 91,008 watts, plus the power supply consumption total of 158,472 watts per CRAY Y-MP.

By testing, it has been determined that a temperature rise of the coolant of 10 degrees Fahrenheit from 65 degrees to 75 degrees will satisfactorily cool the chips and keep the chip die temperature well below the 85 degrees Celsius set limit. The amount of coolant required to maintain the 10 degree temperature rise is two gallons per minute (GPM) per module. The temperature rise through the power supply plate can be higher than the module plate, approximately 15 - 20 degrees Fahrenheit. The required flow for the entire plate is 45 GPM.

A total flow of 205 GPM is being circulated through the system by a pump in the chiller unit. From the pump, the coolant flows through the chiller barrel, where it will be cooled down to 65 degrees Fahrenheit, plus or minus 3 degrees. It is important that the temperature does not go below the 65 degree mark to prevent any condensation in the mainframe. After the chiller barrel, the flow is divided into three circuits. One circuit, with a flow rate of 160 GPM, will provide cooling of the modules. The coolant flows into a 67-inch tall manifold which evenly distributes the flow to the 80 module plates. From the manifold it flows through a quick disconnect no-leak coupling through a hose to the plate, through the plate and out through an outlet hose, then a coupling and into the outlet manifold. The other circuit, with a flow rate of 45 GPM, will provide cooling for the power supply and plate. Just before this circuit enters the plate, it is split in two for the two plate inlets. Ball valves are added before the two inlets to the plate so that the flow can be regulated to achieve an even temperature rise through the two plate passes. From the power supply plate outlet and the outlet manifold, the coolant will flow back to the inlet of the pump to complete the circuit.

The chiller is a refrigeration system with a compressor, condenser, and an evaporator. The chiller barrel is the evaporator, where refrigerant (R22) goes from a low pressure liquid to a low pressure gas, and takes the heat from the coolant. It then flows to the compressor, where it is compressed into a high pressure, high temperature gas, and then goes to the condensing unit where freon (R22) is condensed to a high pressure liquid. In this process, it gives up heat to the condenser cooling water.

Hardware Trng.
YM13/28 J.E.S.

Module Chassis

The module chassis is designed as an open frame consisting of vertical bars, the length of which is the height of the chassis (67 inches).

There are three types of bars:

1. The heavy corner piece that is 1/2 x 6 inches cross-section and which gives the chassis the mechanical strength.

2. The wire routing bar with the same cross-section. They are very similar and have the same function as on the CRAY X-MP mainframe to support the wiremat.

3. The thin bars with cross-section of .2 x 1 inch that are located between the corner pieces and the routing bars.

All the bars are mounted to six spacer plates that tie all the parts together to form a structural chassis. There are 13 bars on each side of the spacer plates: two corner bars, two wire routing bars, and nine thin bars. Each bar has 84 slots for the 80 module plates and four extra. The wired connectors are mounted between the bars, so it is very important to hold the distance between the bars to a very tight tolerance.

The spacer plates are made of two pieces, which make it possible to build the chassis in two pieces for ease of assembly and wiring. Both halves can be wired at the same time, thus cutting the wiring time in half.

The six spacer plates divide the chassis into five sections, with each section holding eight modules. The two top sections hold half of the memory, namely 16 modules. The middle section is for the entire CPU section, eight CPU modules, and the remaining 16 memory modules in the two lower sections. Above and below the CPU section are spaces for wires to cross from one side of the chassis to the other side. This was done for the VHISP channel wires that come from the side of the chassis opposite to where the SSD is located.

The material for the chassis is hot rolled steel because of its strength, easy machinability, and ability to maintain the required straightness and flatness.

Power Supply Plate

Behind the module chassis and tied to the spacer plates is the power supply plate. The plate is formed like a "T", with the top of the T being seven inches long. This part is tied to the chassis. Special shouler screws are used to ensure tight vertical alignment tolerance. This is important because this part of the plate is also used as the ground connection for the module plates.

The module plates are tied to the power supply plate, with four captive screws for each plate. The other part of the power supply plate is two inches thick and 67 inches high by 34 inches long. This is where the 12 power supplies and the 12 buck transformers are mounted. There are six 4.5 volt power supplies mounted on one side, and four 5.2 volt supplies and two 2 volt supplies mounted on the other side.

Because the power supplies are mounted so close to the modules, the voltage drop in the power busses and in the ground return will be held to a minimum. Each power supply will have a heavy power bus (1 x 1 inch copper) that will run towards the modules, and will also have a vertical section 1/2 x 4 inches brazed to it. From here, there are short "L" shaped bus straps going directly to the modules.

The 4.5 volt and 5.2 volt power supplies are capable of 2,200 amps of output, and the 2 volt power supply is capable of 2,800 amps, which is only slightly more than the expected requirement. These power supplies are designed by Schott Corporation in Minneapolis, Minnesota; the same manufacturer as the current CRAY X-MP power supplies.

Besides being the mounting plate for the power supplies and the buck transformers, the power supply plate is carrying the cooling media (Fluorinert FX74) for cooling the power supplies, the diodes, and the buck transformers. The plate has two sets of cooling passes. One set has passes through the plate to conduct the heat away from the power supply cases, the diodes, and the buck transformers. The other set provides coolant for the internal serpentine tube that runs through the power supplies. The coolant comes out of the plate, through a hose to the power supply connection, through the internal tube to the output connection, and then back to the plate through a hose. The internal pass will cool approximately 1/2 of the heat generated by the power supply.

Power Distribution

All the power required for the mainframe, approximately 160KVA, is produced by the motor generator (MG). The power cables for the mainframe come up through the floor on both sides of the power supply plate, where they are tied into a series of terminal blocks.

From the terminal blocks the wires are routed up along the power supply plate and branch off to the power terminals on the buck transformers. A set of terminals are connected to the variac and the power supply is connected to one of six sets of output terminals. The set selected depends on the load on the power supply so that the variac can adjust the voltage within the required range. The DC power distribution from the power supply output bus is described in the power supply plate section.

POWER CONSUMPTION

CPU Module = 2808 watts

Logic chip = 7.5 watts for 4.5 volts
+ 1.5 watts for 2.0 volts
9.0 watts per logic chip
x 312.0 watts per module (78 x 4)
CPU power = 2808 watts per CPU
x 8 8 CPUs
22,464 watts

Memory Module = 2844 watts

Logic chip = 9.0 watts per logic chip
x 156.0 logic chips per module
1404 watts

Memory chip = 1.25 watts per memory chip
x 1152 watts per module (288 x 4)
1440 watts per module

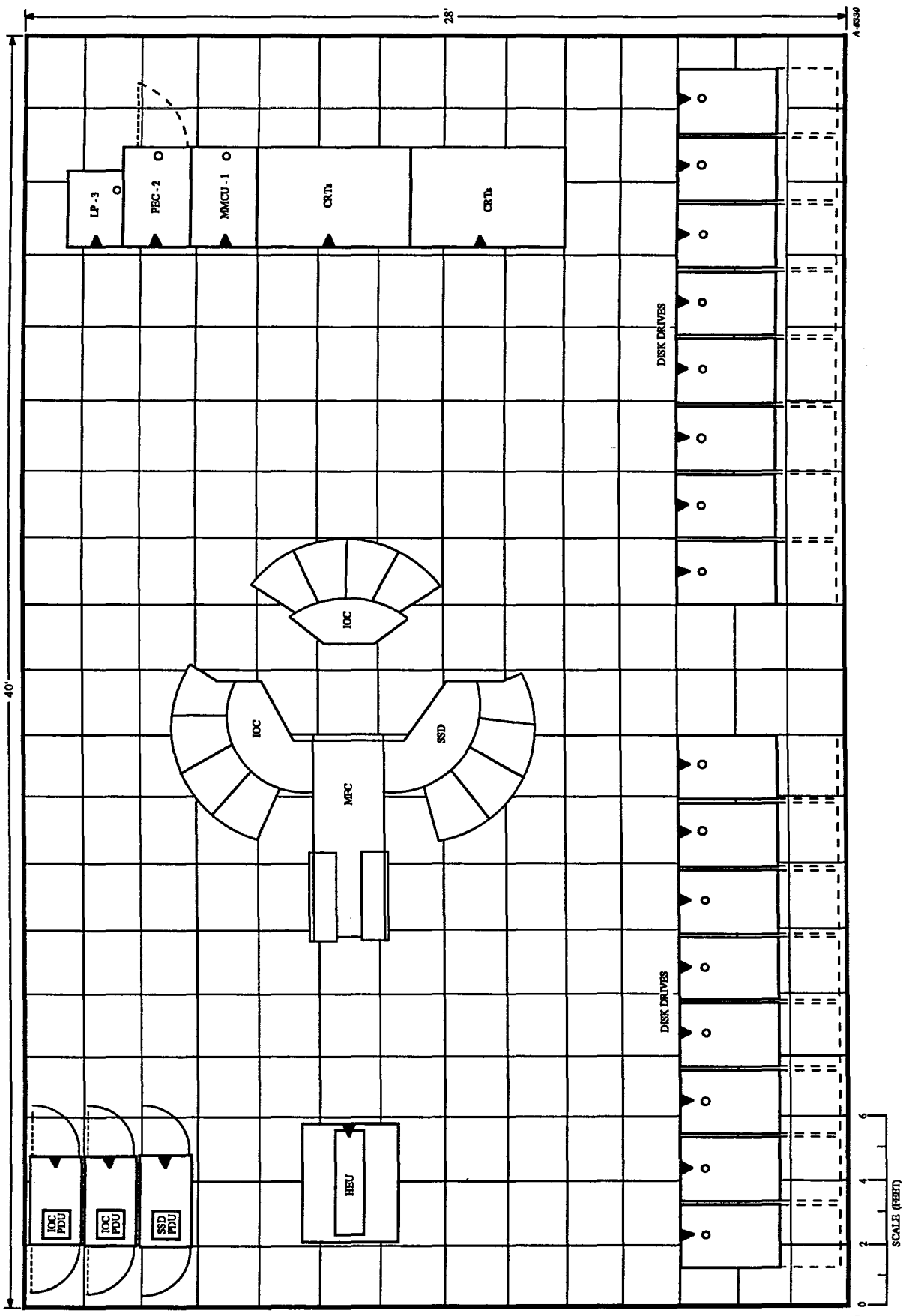
1440 watts logic
+ 1404 watts memory
2844 watts per memory module
x 32 modules per memory
Memory power 91,008 watts

Power Supplies = 45,000 watts

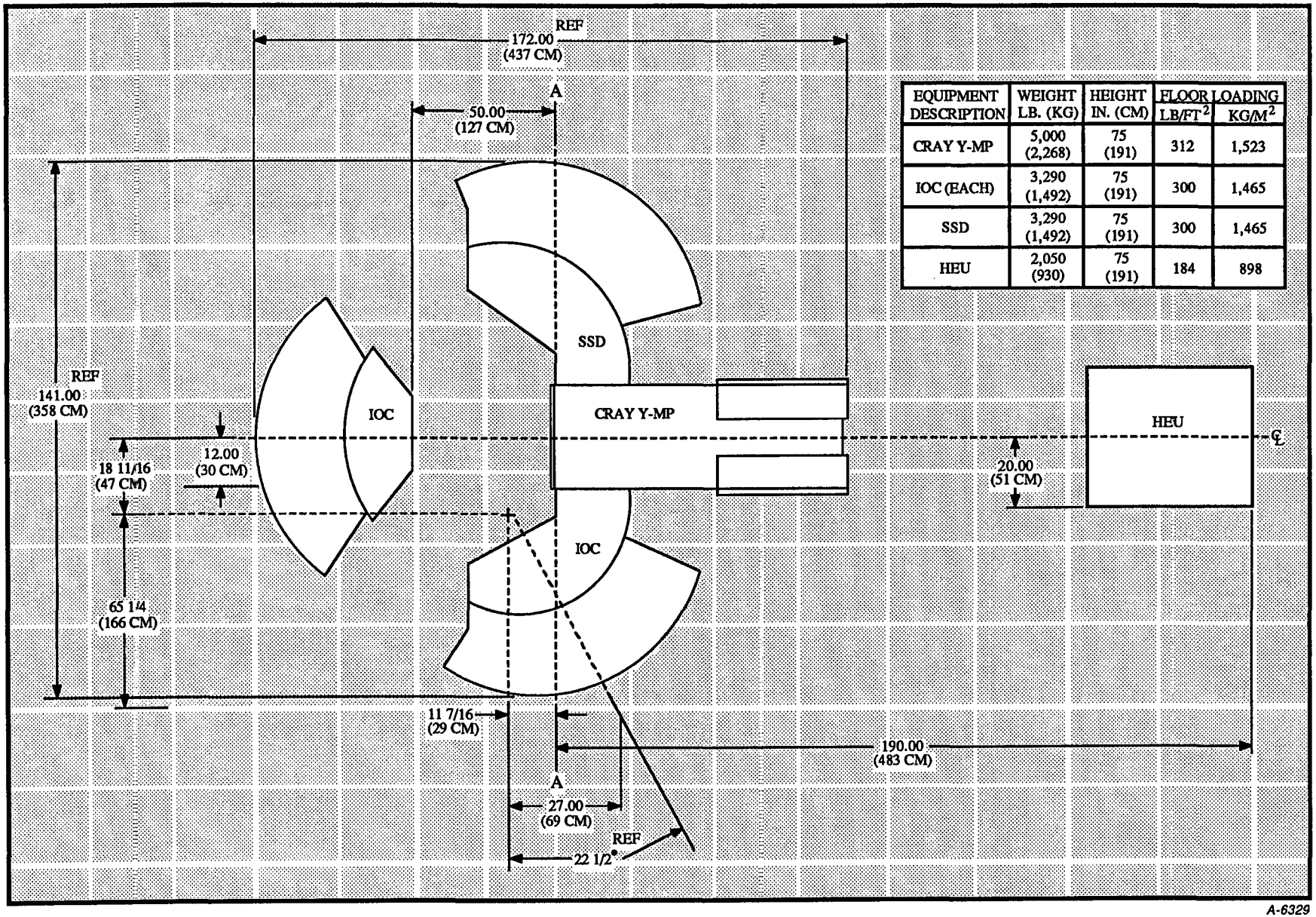
Heat from power supplies (inefficiency)
Buck transformers
= Loss in diodes (.7 volts x 220 amps)

Total Watts: 22,464 = CPU watts per 8 CPUs
91,008 = Memory watts per 32 modules
+ 45,000 = Power supplies
158,472 watts

Hardware Trng.
YM15/42 J.E.S.

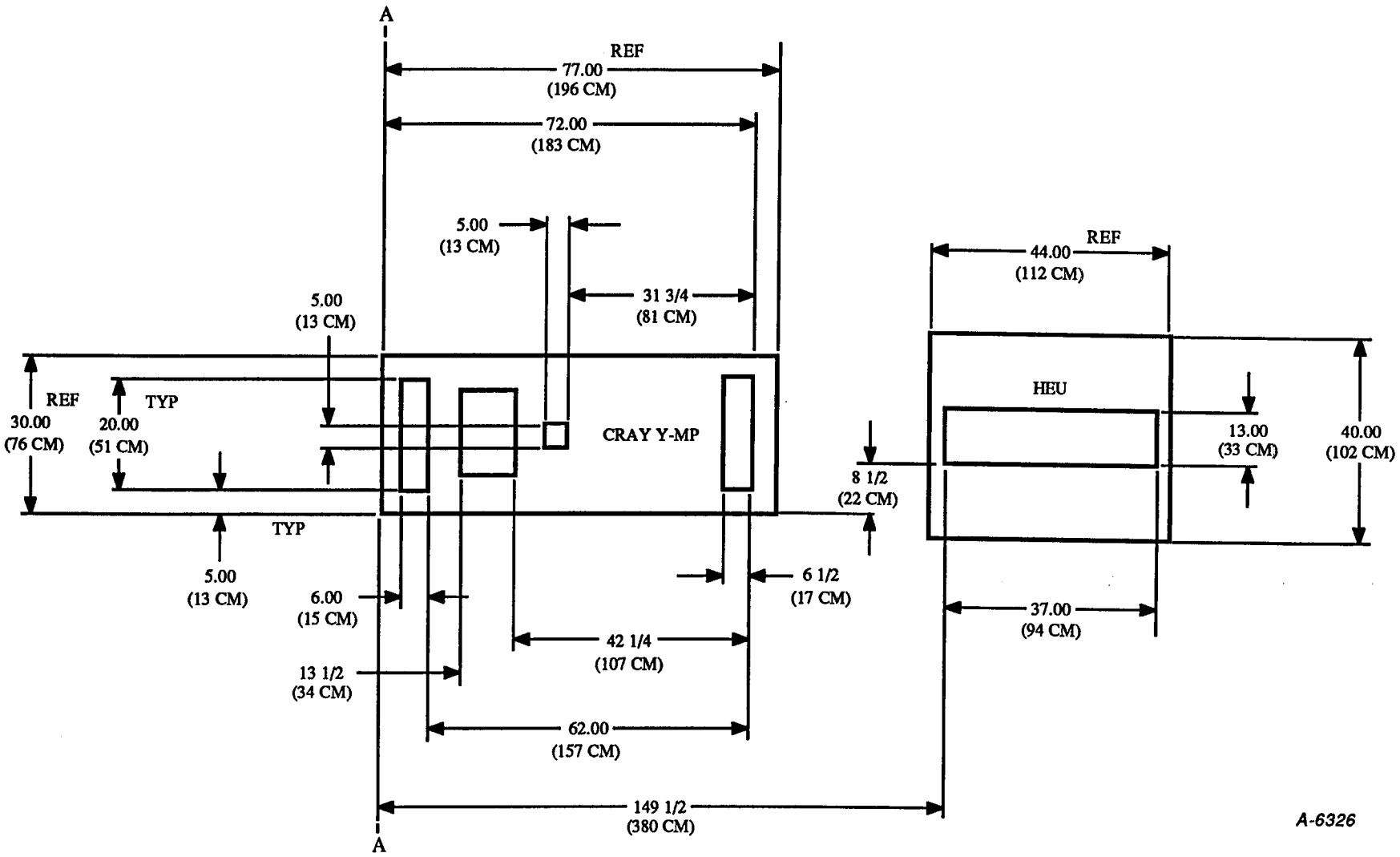


CRAY Y-MP COMPUTER ROOM ARRANGEMENT

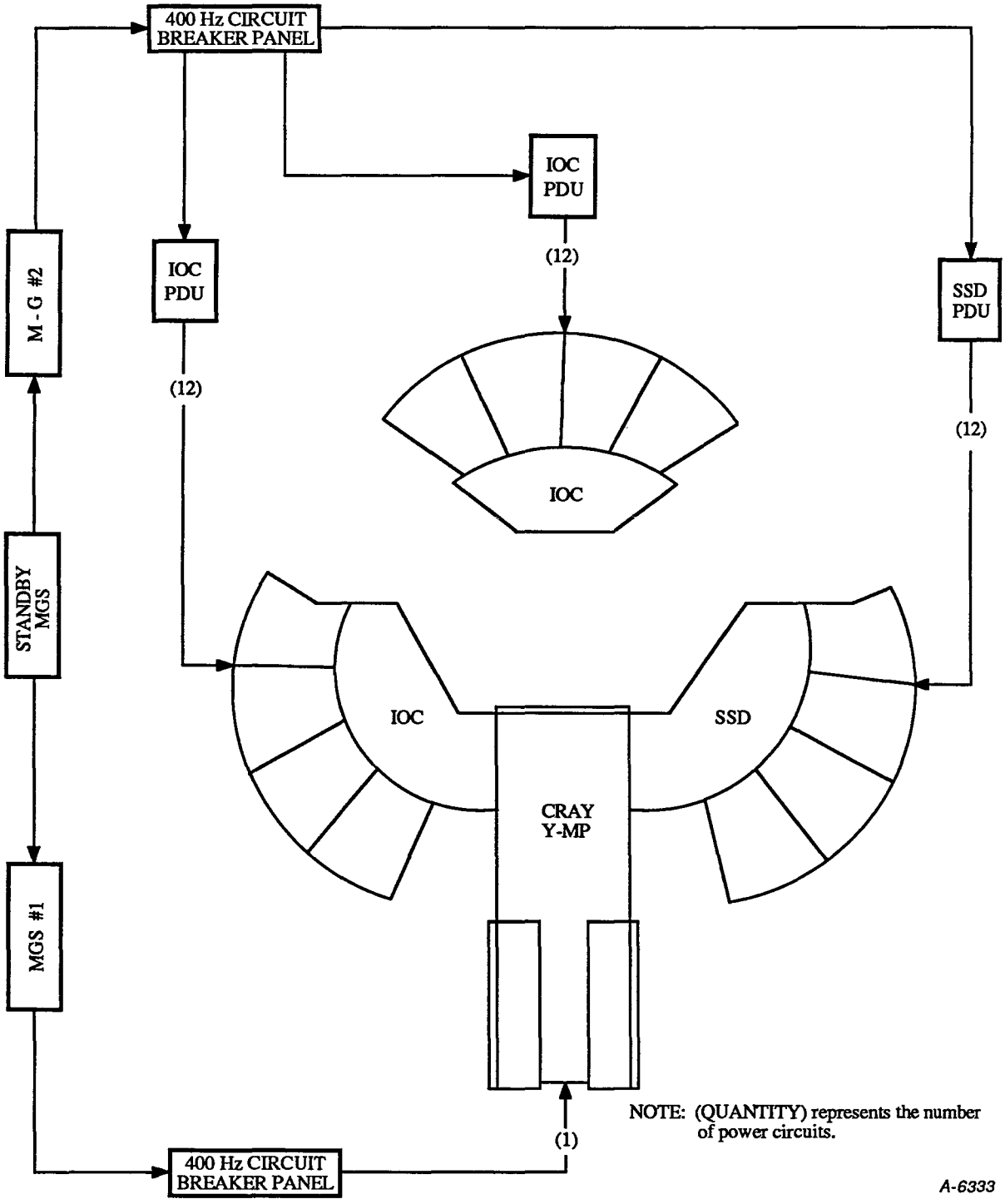


EQUIPMENT DESCRIPTION	WEIGHT LB. (KG)	HEIGHT IN. (CM)	FLOOR LOADING LB/FT^2	FLOOR LOADING KG/M^2
CRAY Y-MP	5,000 (2,268)	75 (191)	312	1,523
IOC (EACH)	3,290 (1,492)	75 (191)	300	1,465
SSD	3,290 (1,492)	75 (191)	300	1,465
HEU	2,050 (930)	75 (191)	184	898

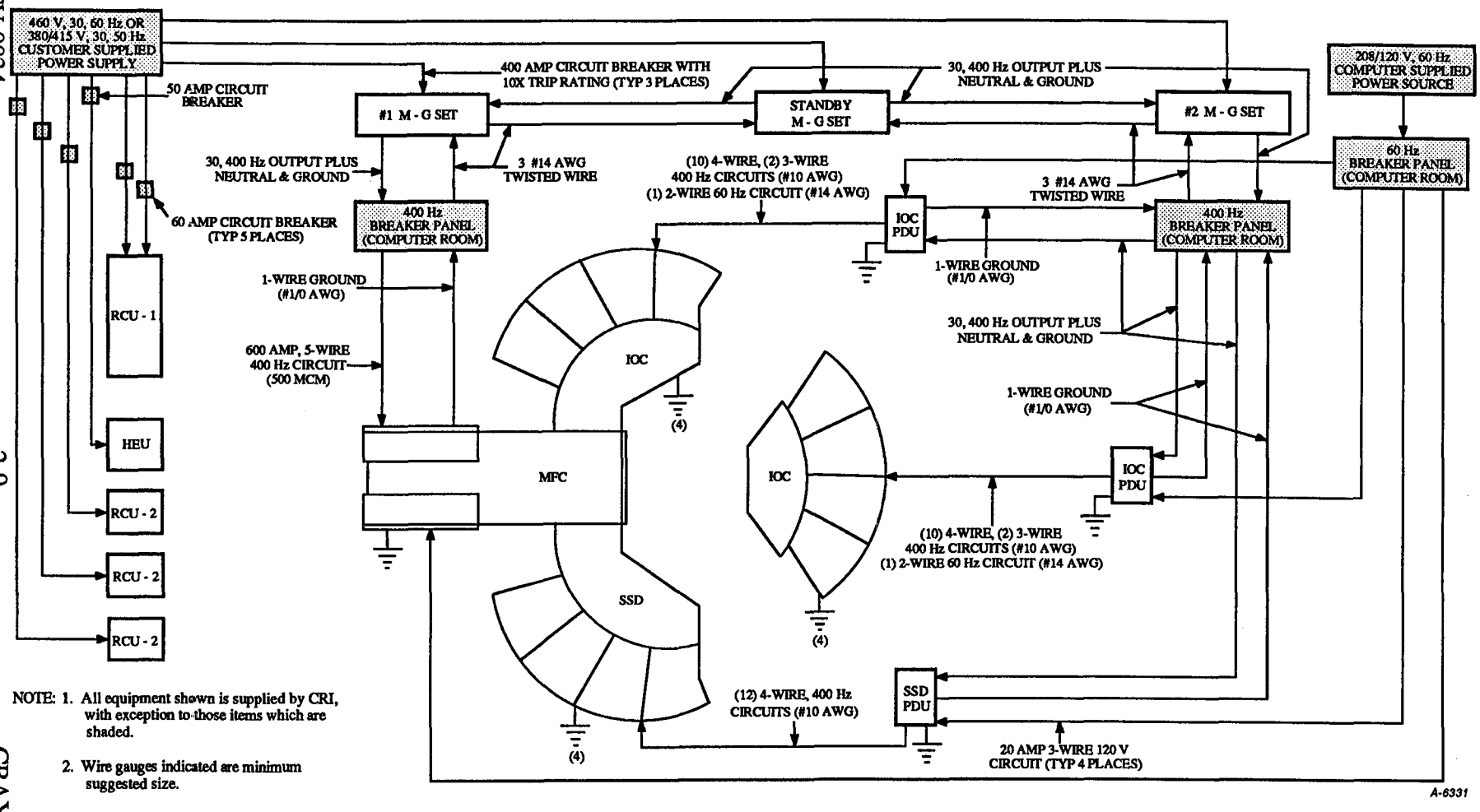
CRAY Y-MP STANDARD PLACEMENT



FLOOR CUTOUTS - CRAY Y-MP AND
HEAT EXCHANGER UNIT



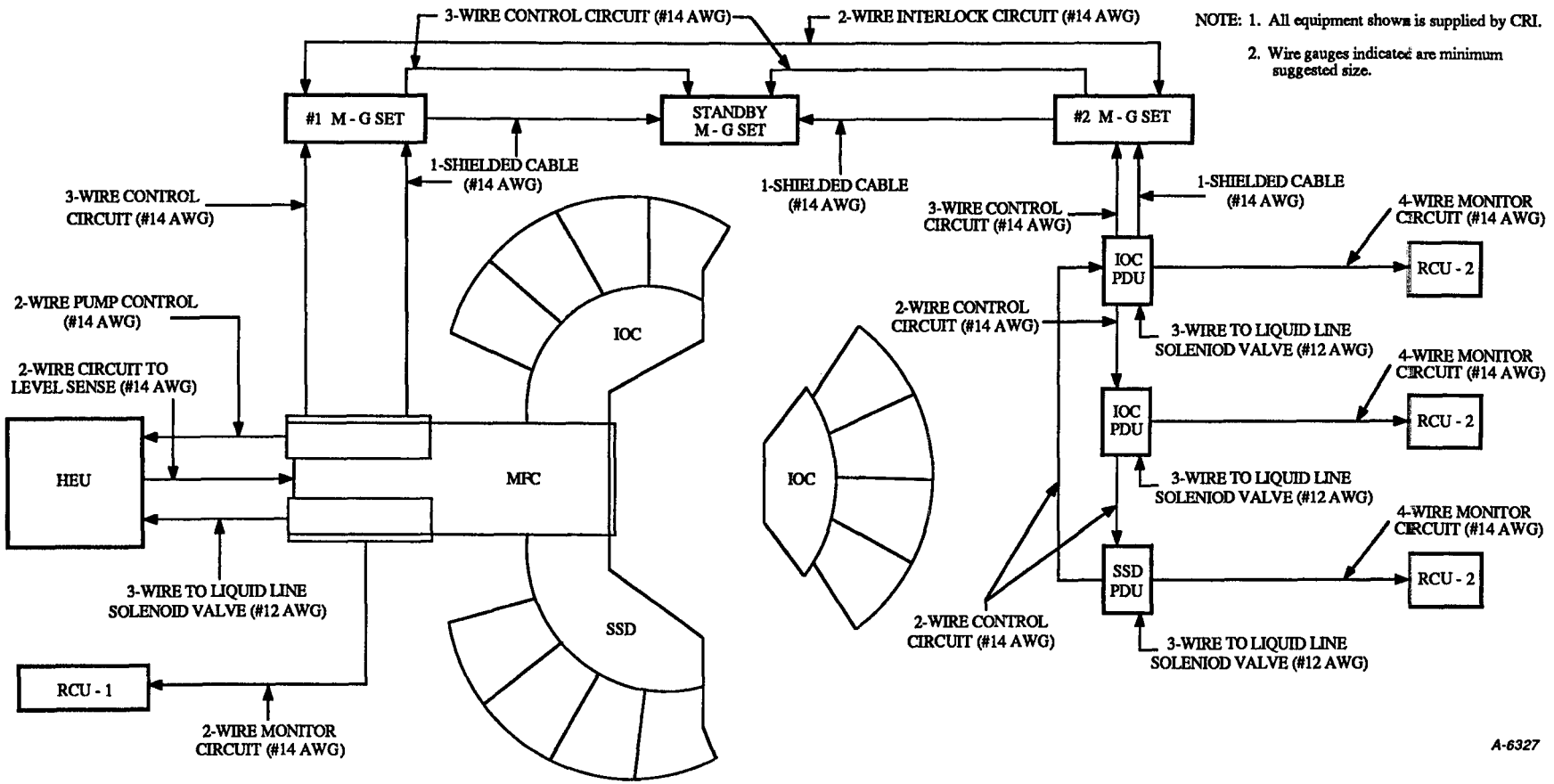
CRAY Y-MP POWER DISTRIBUTION



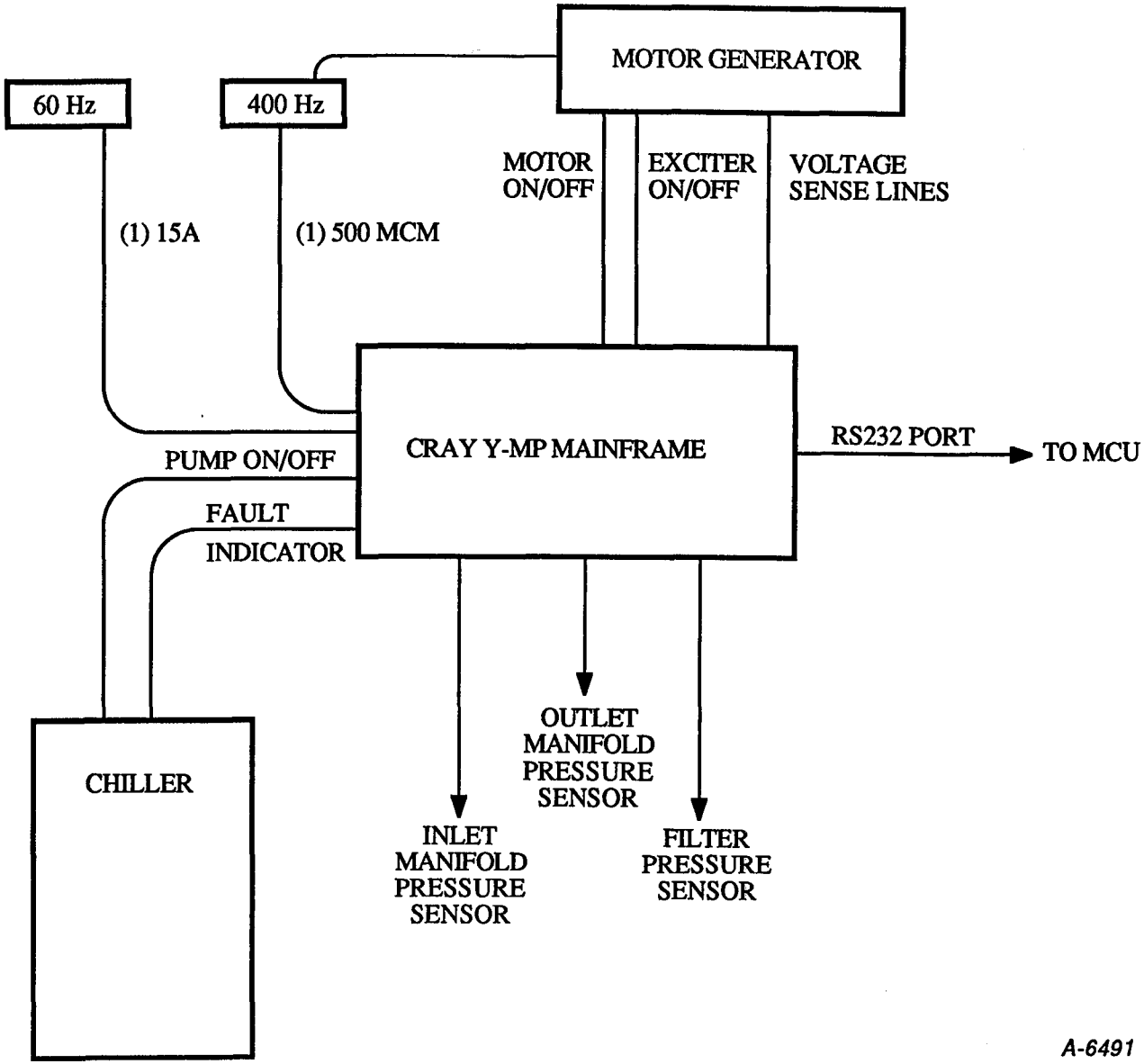
NOTE: 1. All equipment shown is supplied by CRI, with exception to those items which are shaded.

2. Wire gauges indicated are minimum suggested size.

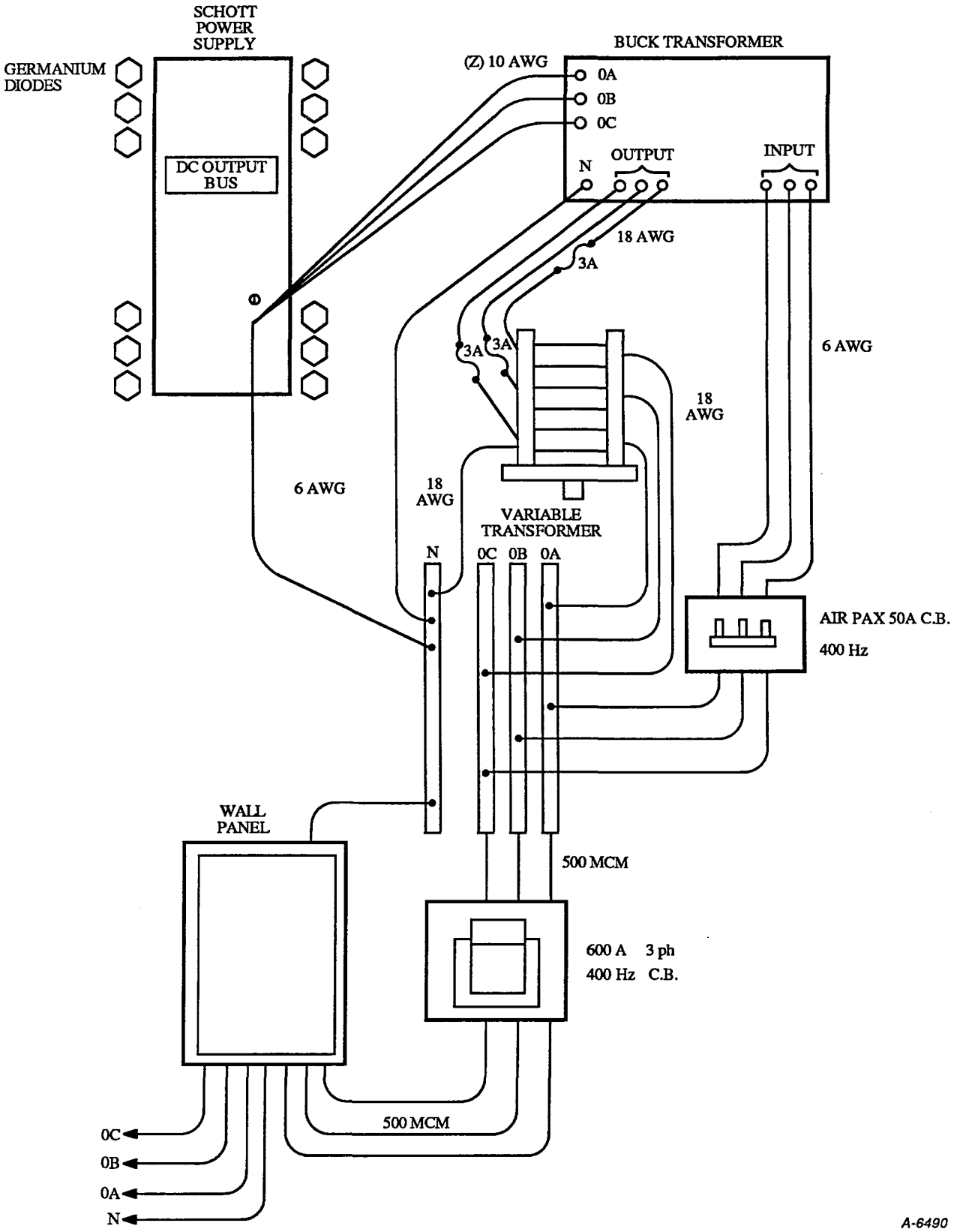
CRAY Y-MP POWER LINES WIRE DIAGRAM
(sheet 1 of 2)



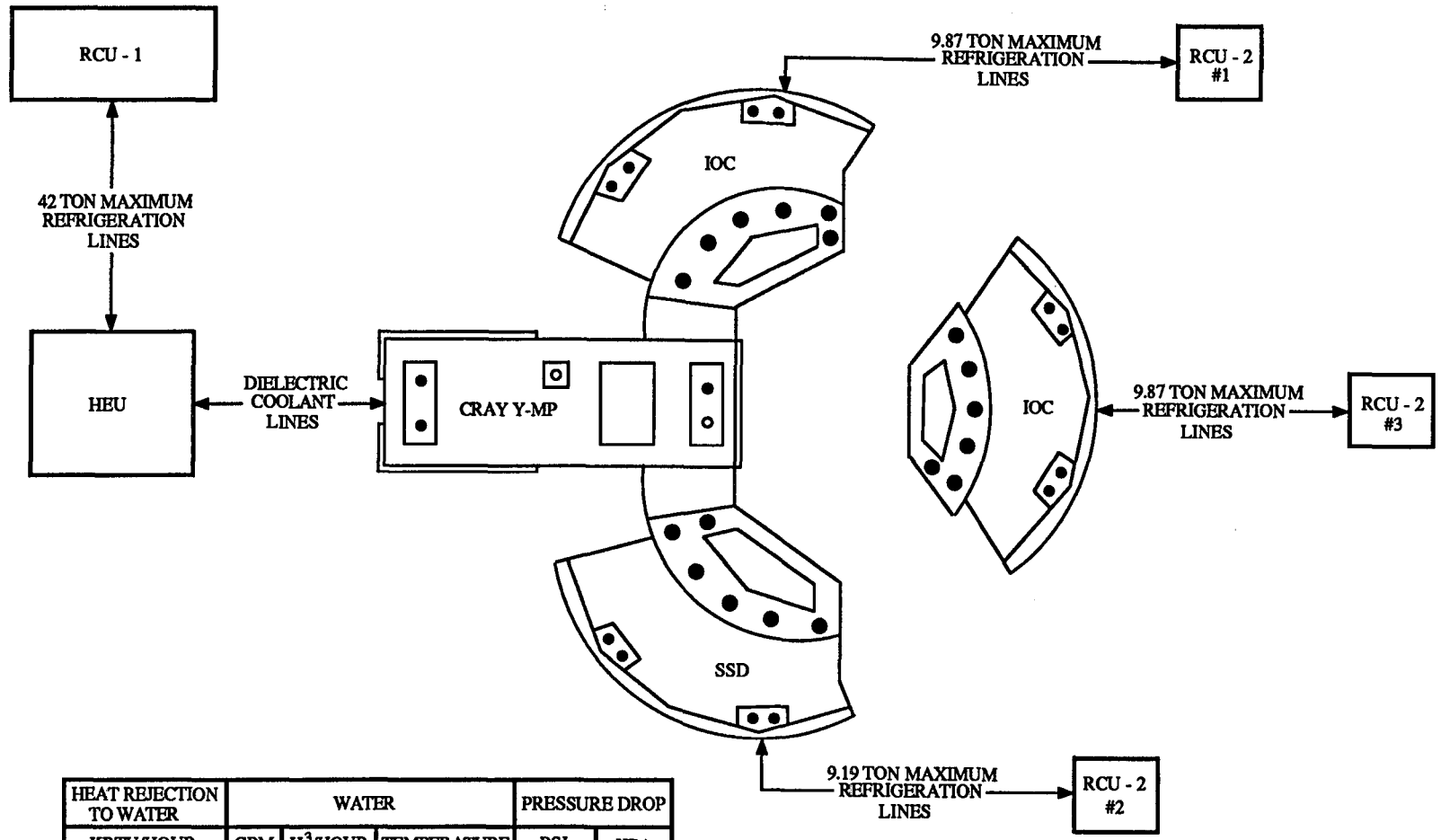
CRAY Y-MP CONTROL LINES WIRE DIAGRAM
(sheet 2 of 2)



CRAY Y-MP POWER AND SIGNAL LINES



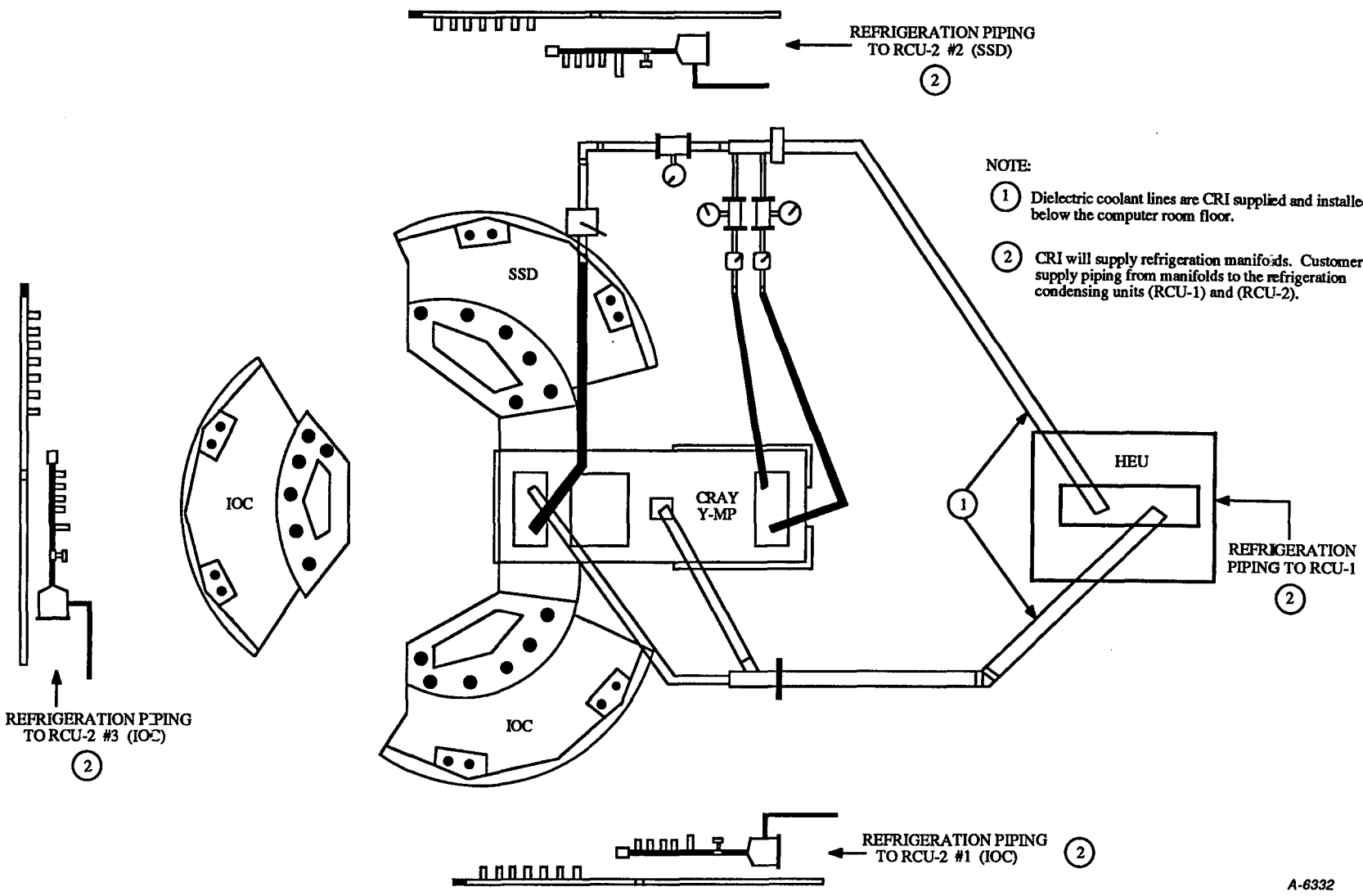
CRAY Y-MP MAINFRAME POWER DISTRIBUTION



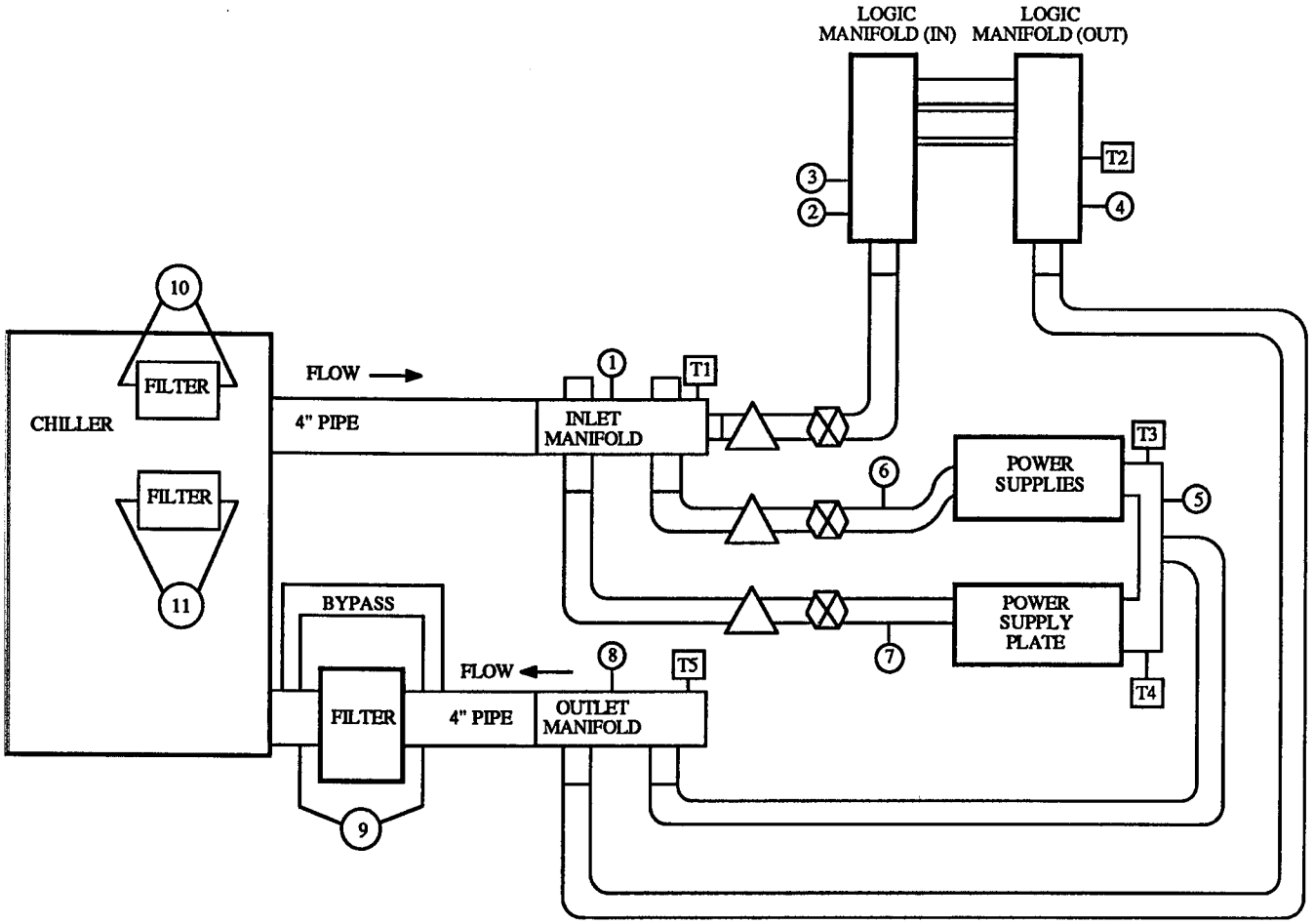
	HEAT REJECTION TO WATER	WATER			PRESSURE DROP	
	KBTU/HOUR	GPM	H^3/HOUR	TEMPERATURE	PSI	KPA
RCU - 1 (MFC)	571	38	8.63	60° INLET 90° OUTLET	10	69
RCU - 2 (IOC) (EACH)	153	11	2.52	60° INLET 90° OUTLET	10	69
RCU - 2 (SSD)	145	10	2.16	60° INLET 90° OUTLET	10	69

A-6328

CRAY Y-MP COOLING



CRAY Y-MP COOLING DIAGRAM



1. PRESSURE TRANSDUCER PROTECTS INLET PIPES
2. LOGIC CIRCUIT PRESSURE PROTECTION
3. BACK-UP FOR NUMBER 2 ABOVE
4. OUTLET PRESSURE (NEEDED TO ADJUST VALVE IN INLET)
5. POWER SUPPLY PLATE AND SUPPLIES (NEEDED TO ADJUST VALVE AT INLET)
6. POWER SUPPLY CIRCUIT PROTECTION
7. POWER SUPPLY PLATE PROTECTION
8. OUTLET MANIFOLD FOR ALL SYSTEM PEFORMANCE
9. DIFFERENTIAL PRESSURE FOR FILTER CHANGE

10, 11 DIFFERENTIAL PRESSURE ON FILTERS

BALL VALVE

FLOW METER

TEMPERATURE PROBE

PRESSURE TRANSDUCER

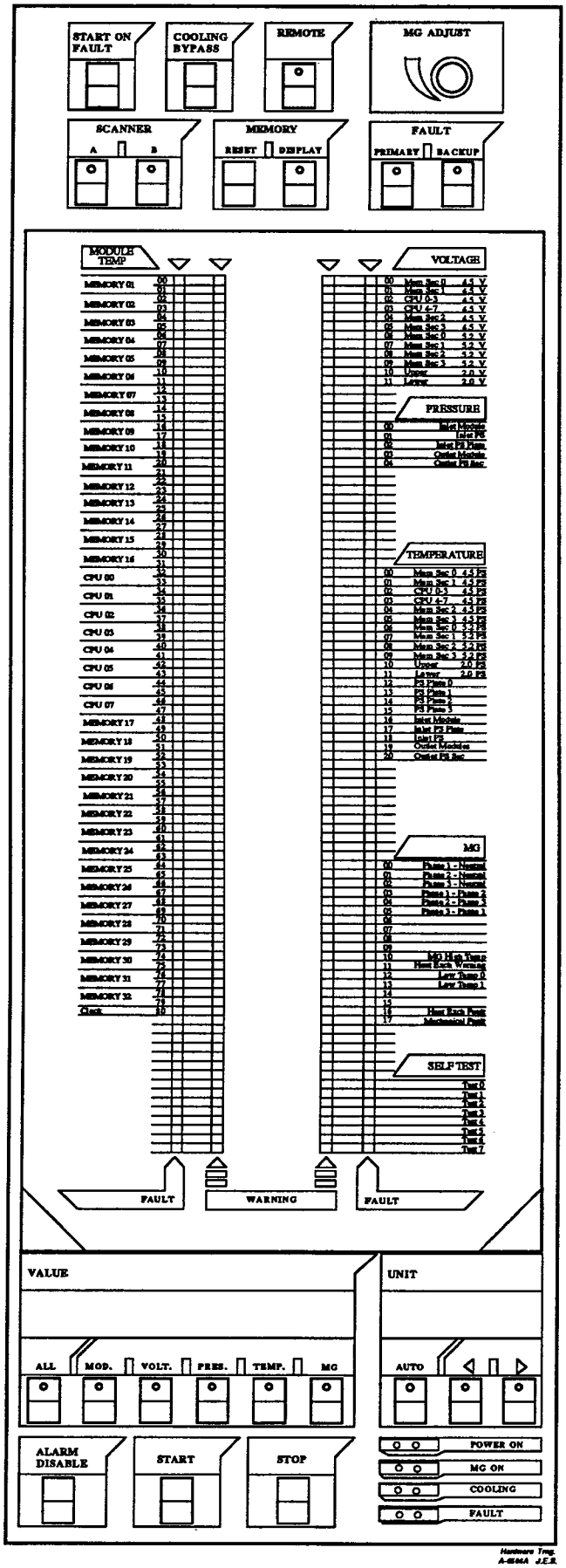
A-6489

CRAY Y-MP TEMPERATURE AND PRESSURE TRANSDUCERS LOCATION

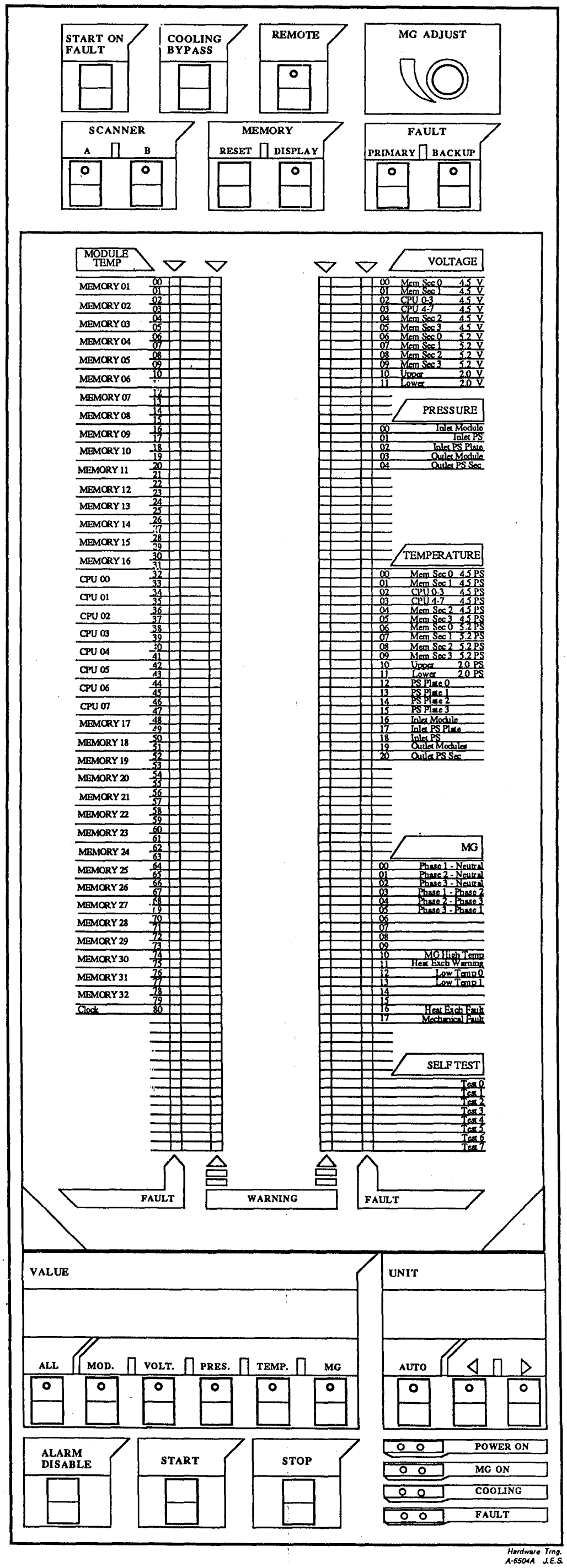
OBJECTIVES - CRAY Y-MP Controller

Upon completion of this section, the student will be able to:

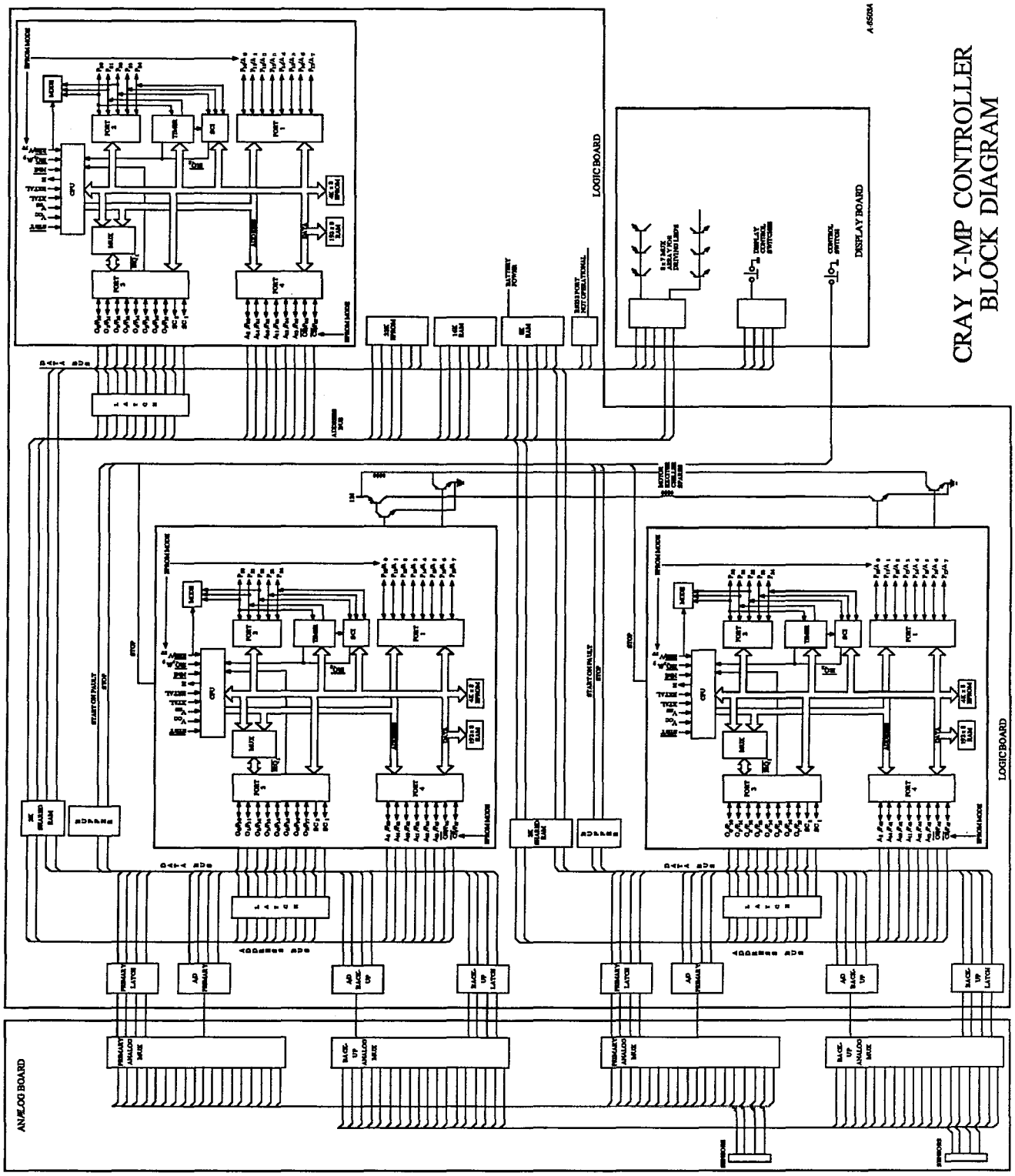
- Understand the function of the CRAY Y-MP controller and its block diagram
- Isolate a failing board or sensor

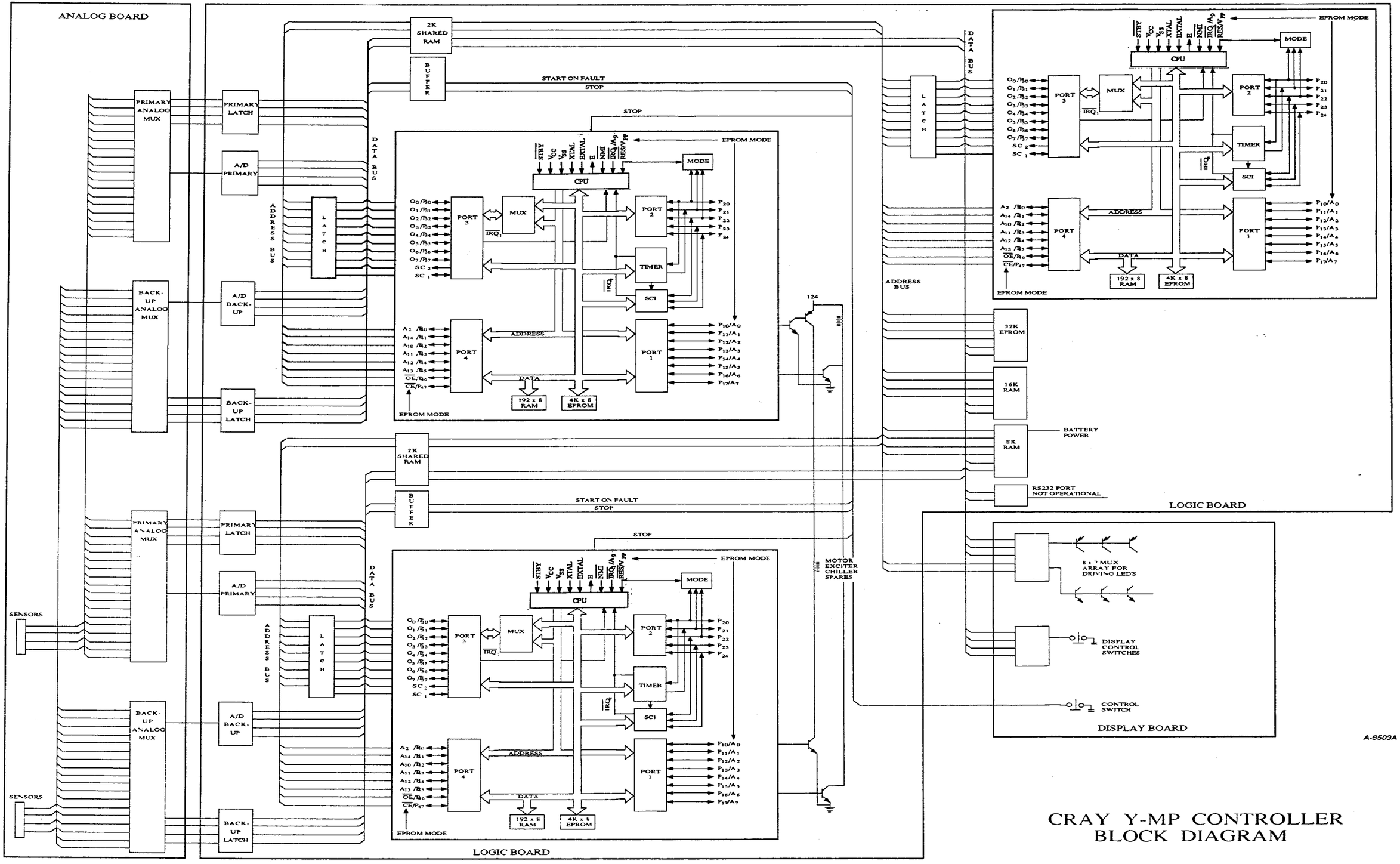


CRAY Y-MP SYSTEM MONITOR



CRAY Y-MP SYSTEM MONITOR


CRAY Y-MP CONTROLLER
BLOCK DIAGRAM
LOGIC BOARD
DISPLAY BOARD
ANALOG BOARD
A-65034



CRAY Y-MP CONTROLLER BLOCK DIAGRAM

CRAY Y-MP CONTROLLER

General Description

The power control and warning system for the CRAY Y-MP consists of:

1. Two identical scanners that monitor external sensors.
2. A main processor that monitors the two scanners.
3. The display panel for displaying the faults.
4. Sensor mounted throughout the system.
5. Power supplies for the control.

Mechanical Description

The main processor and both scanners are contained on a large printed circuit board. This board is then mounted in its own enclosure behind the display board. The display is another printed circuit that contains the fault indicators and the system start/stop switches. This board is mounted on the front of the cabinet. Sensors are located throughout the cabinet and are used to sense temperature, pressure, voltages, etc.

Scanner Description

Each scanner is identical and consists of a microprocessor that controls an A - D converter, an analog multiplexer, and shut-off relays.

Microprocessor

The main processor within the scanner has a standard address/data bus, external ports, plus internal EPROM and RAM. This configuration allows a system where all the programming for the scanner is contained within the on-chip EPROM and the external port is used for controlling the shut-off relays (this prevents a failure on the buses from disabling the scanner). The only failure that will prevent the scanner from powering off the system during a fault is either a failure of the microprocessor or multiple failures of the relays.

A - D Converter

Two ICL7115 converters are used for each scanner. The 7115 is a 14-bit resolution, 40us conversion rate, and CMOS design. Each scanner has a 7115 used to monitor a set of "primary" sensors and a second 7115 to monitor a set of "backup" sensors. This allows the scanner to continue to operate if either of the converters or its input fail, so long as the sensors are

checked in an ANDed condition. Some sensors may be checked in an ORed condition depending on the mode.

Analog Multiplexer

Each A - D converter has a multiplexer. This multiplexer controls which sensor is being monitored by the A - D converter. The multiplexing will be a 4051 which is an eight channel.

Port 1

Port 1 of the microprocessor is used to drive 14 relay. The relays are K1 - K14

RELAY	FUNCTION
K1	Turns on the MG motor
K2	Turns on the MG exciter
K3	Turns on the HEU and RCU
K4 through K6	(Not used)
K7	Turns off the main 400 Hz circuit breaker
K8	Prevents the computer system from powering up once it has powered down
K9	Turns on the remote alarm
K10	Enables Start
K11	Supplies power to other control system relays
K12	Enables remote operation of the computer system
K13	Turns the local alarm on and off
K14	Prevents the control system microprocessor from circulating coolant through the mainframe without first pressing the Cooling Bypass switch

Shared Memory

Each scanner has 2K of memory that is shared with the main processor. The scanner can write to memory, but can not read; and the main processor can read, but can not write. This memory is used to transfer scanner status to the main processor.

Sensors

Sensors are located throughout the cabinet to detect possible faults. These sensors are for monitoring: coolant pressure, temperatures, air flow, etc. Most items monitored have both a primary and a backup sensor. The primary sensor is used by the primary A - D converters on both scanners and the backup sensors are used by the backup A - D converters on both scanners.

Temperature

Up to 32 temperature pairs may be monitored (12 are used). All temperature monitoring within the cabinet is done by thermistors.

Pressure

Up to 16 pairs of pressure transducers may be monitored by each scanner (6 are used). The coolant pressure will be measured at nine points.

Power Supply Voltage

Up to 16 power supply voltages may be monitored (only 12 are used). The voltage inputs are differential (require both a ground and voltage input). This allows the voltage to be measured at the module without errors from voltage drops in the bussing or ground planes. The same voltage input is used for both primary and backup sensing.

Motor-Generator Voltages

Up to 12 inputs may be monitored for 400 Hz inputs (6 are used). Each input is measured phase-to-phase and phase-to-neutral (total of six measurements per 400 Hz input). Primary sensing for faults is the phase-to-neutral measurements and the backup sensing is the phase-to-phase measurements (example phase 2-to-3 is the backup for phase 1-to-neutral).

Contacts

Eight pairs of contacts are provided. The first set of eight indicate a shut-down fault. The present system requires that one be used to detect if the chiller is on. The second set of contacts are used to indicate a warning. The present system does not have a requirement for warning contacts.

Low Temperature

Up to 4 moisture sensors may be used for low temperature sensing (1 is used). A relative humidity sensor will be used to detect low temperature.

Self Checks

Internal power supplies and voltage reference are also checked. The scanners will power the system off if these internal references are not within limits with respect to each other.

Module Temp

Up to 96 module temperatures can be sensed (81 are used). The temperature monitoring will be done by thermistors located on the modules.

Main Processor

The main processor interfaces each of the scanners and provides a control of all non-shutoff functions. The main processor will control:

1. The display panel
2. Both an internal and a remote horn
3. Provides an undefined interface to a remote computer

The main processor interfaces each scanner via a shared 2K memory. The main processor can only read data from the 2K memory, and then uses this data for controlling lights, horns, etc.

Horns

An internal horn will be provided to indicate faults. Switches are provided for the site to select when the horn will sound:

1. A warning (out of specifications, but in operating limits)
2. A fault (system is outside limits and timing out to power off)
3. System has powered off because of a fault

A contact is provided for a remote horn. This remote horn will have the same function as the horn provided within the cabinet.

Memory

This memory is to store faults that occurred before the cabinet powered off, but it stores ONLY where the fault occurred, and NOT when the value, or number of times the fault occurred. Back up power for the memory is a capacitor, and has an expected charge that will last one week.

RS232

A RS232 interface will be provided, but no software will be provided at this time. The use of this port is undefined.

Display

The display consists of:

1. Warning and fault LEDs
2. Digital meter
3. Operator control switches
4. Maintenance switches (for C.E. only)

The display panel is mounted on the front center of the cabinet. This allows the status of the sensors to be viewed without opening the door.

YM15/36A

LEDs

Both warning and fault LEDs are provided for each fault. All fault LEDs are red and indicate that the cabinet is timing out to shut off, or has shut off because of that fault. Warning LEDs are yellow and indicate that the cabinet is outside of normal limits, but still operating. The warnings are provided to indicate that something should be adjusted/fixed before the warning develops into a shut-down fault.

Digital Meter

Will display an average of the last 16 value scanned. What is displayed is controlled by the operator switches.

Operator Switches

The operator is provided with switches for starting and stopping the system plus switches for controlling the operation of the digital meter. Meter switches determine if the meter will scan through all the measured functions, only some of the functions, or only view one item.

ALL	Scans all system control sensors.
MOD.	Scans all Flow sensors of modules.
Volt.	Scans all DC voltage.
PRES.	Scans coolant pressure.
TEMP.	Scans the power supply plate and transformers.
MG	Scans the phase of MG, low temperature, and chiller fault.
AUTO	Scans a selected sensor group.
< (DOWN)	Will force the scanner to scan from 80 to 0.
> (UP)	Will force the scanner to scan from 0 to 80.
ALARM DISABLE	This switch will disable the horn until a new fault occurs, or until the same fault reappears.
START	This switch will power on the system.
STOP	This switch will power off the system.

Maintenance Switches

Another set of switches are provided for the C.E. These switches provide additional control of the display.

START ON FAULT	This will allow the operator to power on with a fault.

YM15/37A

COOLING BYPASS	Turns on the cooling pump in the Heat Exchanger unit without power on. This is disable if powered off with a high pressure fault.
REMOTE	This will allow the system to start and stop from a remote device. This can be via the RS232 port of the main processor via an external contact or via an external 20 -120 voltage. The remote signal can only start the system if the remote switch is on and if the start was previously pushed. It can NOT restart the system after it has powered off with a fault.
MG ADJUST	Is a potentiometer that will vary the output of the MG.
SCANNER	Will enable the operator to view scanner A and/or B data. When both A and B or neither is selected, it is an average of both.
MEMORY DISPLAY	The main processor stores all previous faults and warnings that occurred after the MG is started. This switch will allow you to display the memory.
MEMORY RESET	This switch will clear the memory without power off the system.
FAULT PRIMARY/ BACKUP	These switches will allow you to view the primary or backup fault.

Operational Requirements

Startup

The start up sequence is initialized by either a REMOTE START signal (if in remote) or by the start switch. Each scanner performs checks before starting:

1. Each scanner performs self checks to determine if the internal reference are within limit and checks Memory address for correct operation.
2. Then temperature/volt/pressure sensors are checked for zero reading.
3. All other sensors are checked for normal conditions.

Both the chiller and the motor-generator motor are started if the initial checks were within limit. The motor-generator exciter is then started after a delay of two minutes and if all the sensors are within limits.

Scanning

Each scanner will scan all faults within 0.1 seconds. All warnings and faults are recorded. The scanner will continue scanning all sensors until the system is powered off.

Shut-off Faults

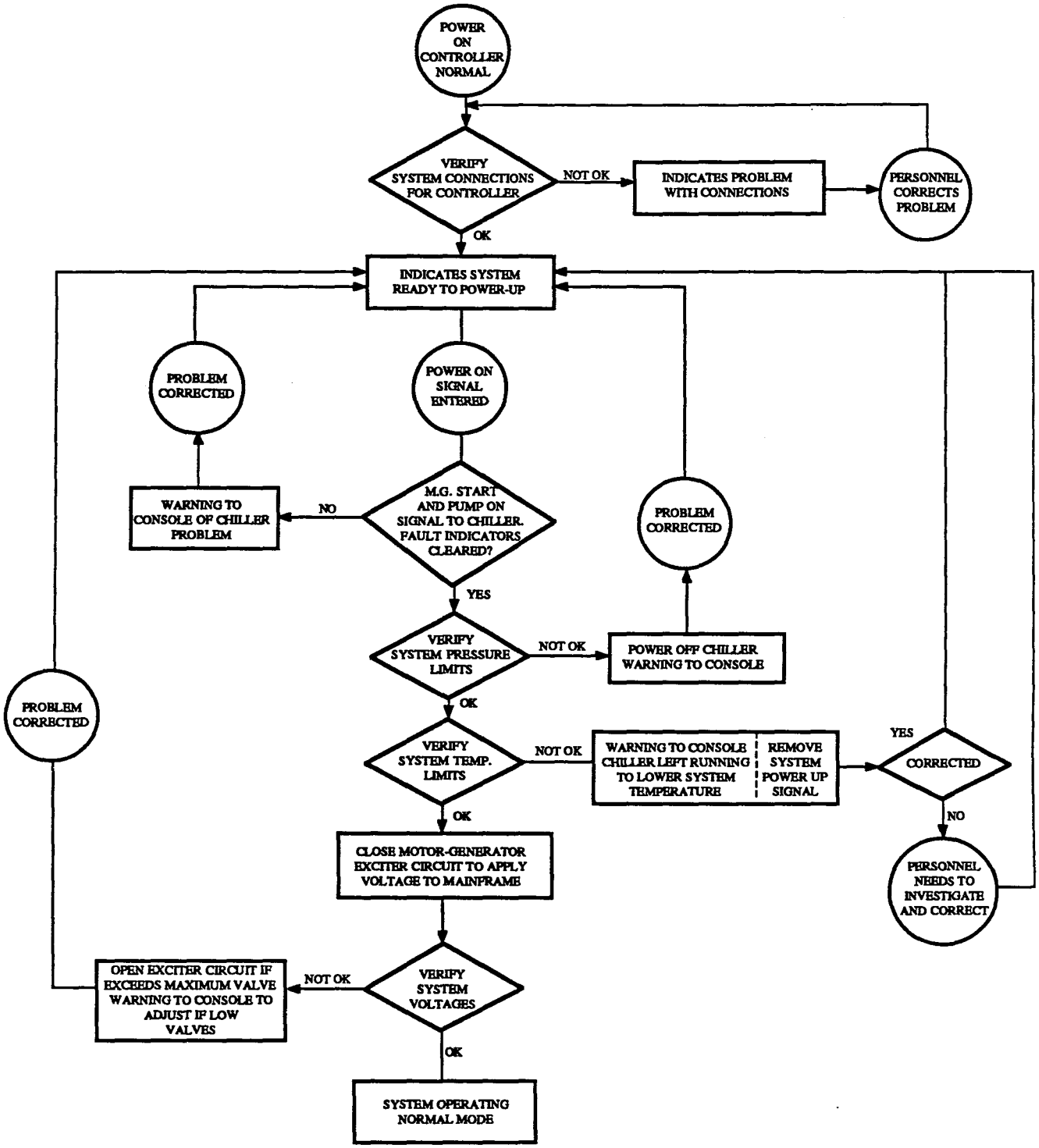
Each scanner monitors both a set of primary and a set of backup sensors. A scanner must sense a fault on both the primary and/or backup of the same item before powering off.

Shut-off Sequence

The following is the shut-off sequence for all faults except low-temperature:

1. The motor-generator exciter is powered off.
2. The motor-generator motor is powered off if the 400 Hz voltage has not dropped after .5 seconds (ride-through time).
3. If the 400 Hz is still present after an additional .5 seconds, then the main input circuit breaker is tripped. (This may happen in new installation where the cabinet was wired to the wrong motor-generator or where someone had jumpered the motor-generator controls).
4. The chiller will remain on until the coolant temperature from the plates is < 70 F.

Motor-generator exciter and the chiller are powered off at step 1 for a low temperature.

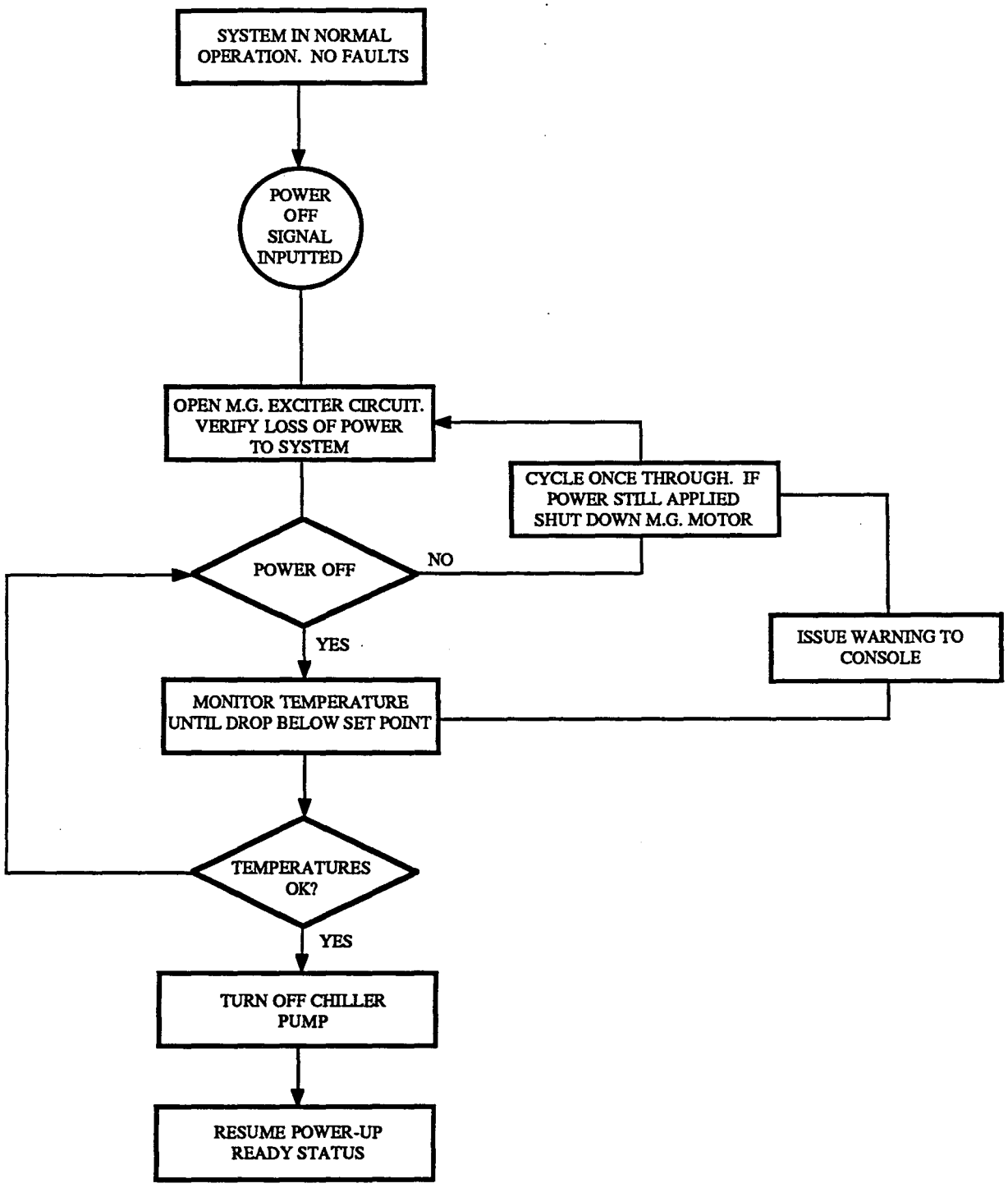


NOTE:

System is fully configured in the "Normal" operation mode.

A-6499

CRAY Y-MP POWER UP FLOW CHART

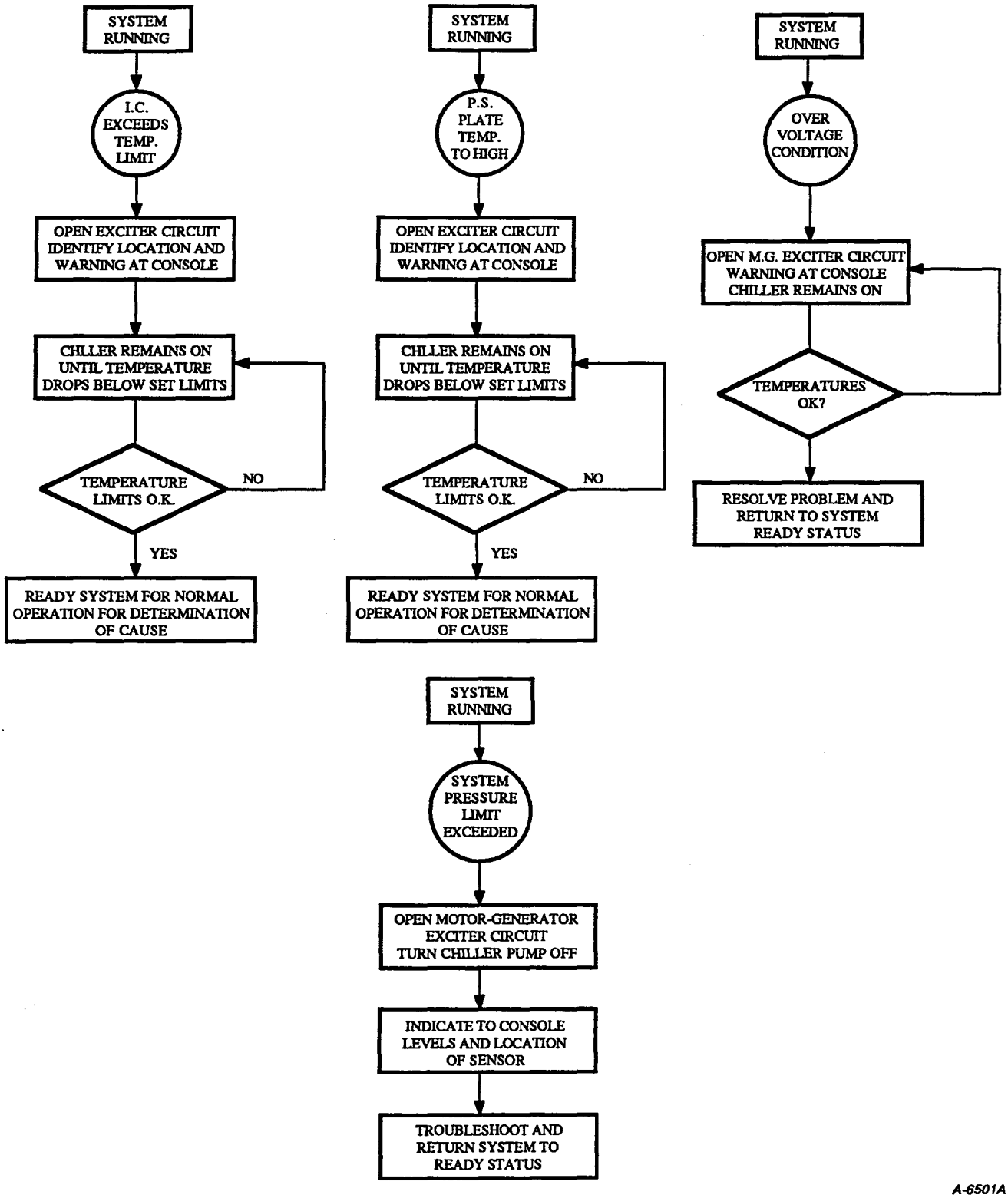


NOTE:

1. System is operating in "Normal" mode.
2. Assume no problem with coolant system.

A-6500

CRAY Y-MP SYSTEM FLOW CHART
(sheet 1 of 2)



CRAY Y-MP SYSTEM FLOW CHART
(sheet 2 of 2)

	ON LIMITS				OFF LIMITS				METER	TIMEOUT
	HIGH		LOW		HIGH		LOW			
	FAULT	WARNING	WARNING	FAULT	FAULT	WARNING	WARNING	FAULT		
MODULES	140 F	130 F	50 F	40 F	150 F	140 F	40 F	30 F	YES	10 SEC.
-4.5 BUS	5.35V	4.90V	4.01V	0.10V	2.25V	1.75V	NONE	NONE	YES	0.4 SEC.
-5.2 BUS	6.18V	5.67V	4.63V	0.10V	2.60V	2.10V	NONE	NONE	YES	0.4 SEC.
-2.0 BUS	2.74V	2.64V	1.78V	0.10V	1.00V	0.80V	NONE	NONE	YES	0.4 SEC.
PRESSURE	80 PSI	75 PSI	-4 PSI	-8 PSI	20 PSI	15 PSI	-4 PSI	-8 PSI	YES	0.4 SEC.
TRANSFORMER TEMPERATURE	200 F	190 F	50 F	40 F	210 F	200 F	40 F	30 F	YES	10 SEC.
PLATE TEMPERATURE	110 F	100 F	50 F	40 F	120 F	110 F	40 F	30 F	YES	10 SEC.
INPUT TEMPERATURE	90 F	85 F	50 F	40 F	90 F	85 F	40 F	30 F	YES	10 SEC.
OUTPUT TEMPERATURE	100 F	NONE	50 F	NONE	NONE	110 F	40 F	NONE	YES	NONE
M. G. VOLT PH-NEUTRAL	144V	132V	108V	60V	60V	50V	NONE	NONE	YES	0.4 SEC.
M. G. VOLT PH-PHASE	250V	229V	187V	104V	104V	87V	NONE	NONE	YES	0.4 SEC.
M. G. WARN CONTACT	NONE	NONE	OPEN CONTACT	NONE	NONE	NONE	OPEN CONTACT	NONE	NO	NONE
HEU WARN CONTACT	NONE	NONE	OPEN CONTACT	NONE	NONE	NONE	OPEN CONTACT	NONE	NO	NONE
LOW PRESSURE	NONE	NONE	>95% RH	NONE	NONE	NONE	>95% RH	NONE	NO	1 MIN.
HEU FAULT CONTACT	NONE	NONE	OPEN CONTACT	NONE	NONE	NONE	OPEN CONTACT	NONE	NO	10 SEC.
MECHANICAL BACKUP	NONE	NONE	OPEN CONTACT	NONE	NONE	NONE	OPEN CONTACT	NONE	NO	10 SEC.

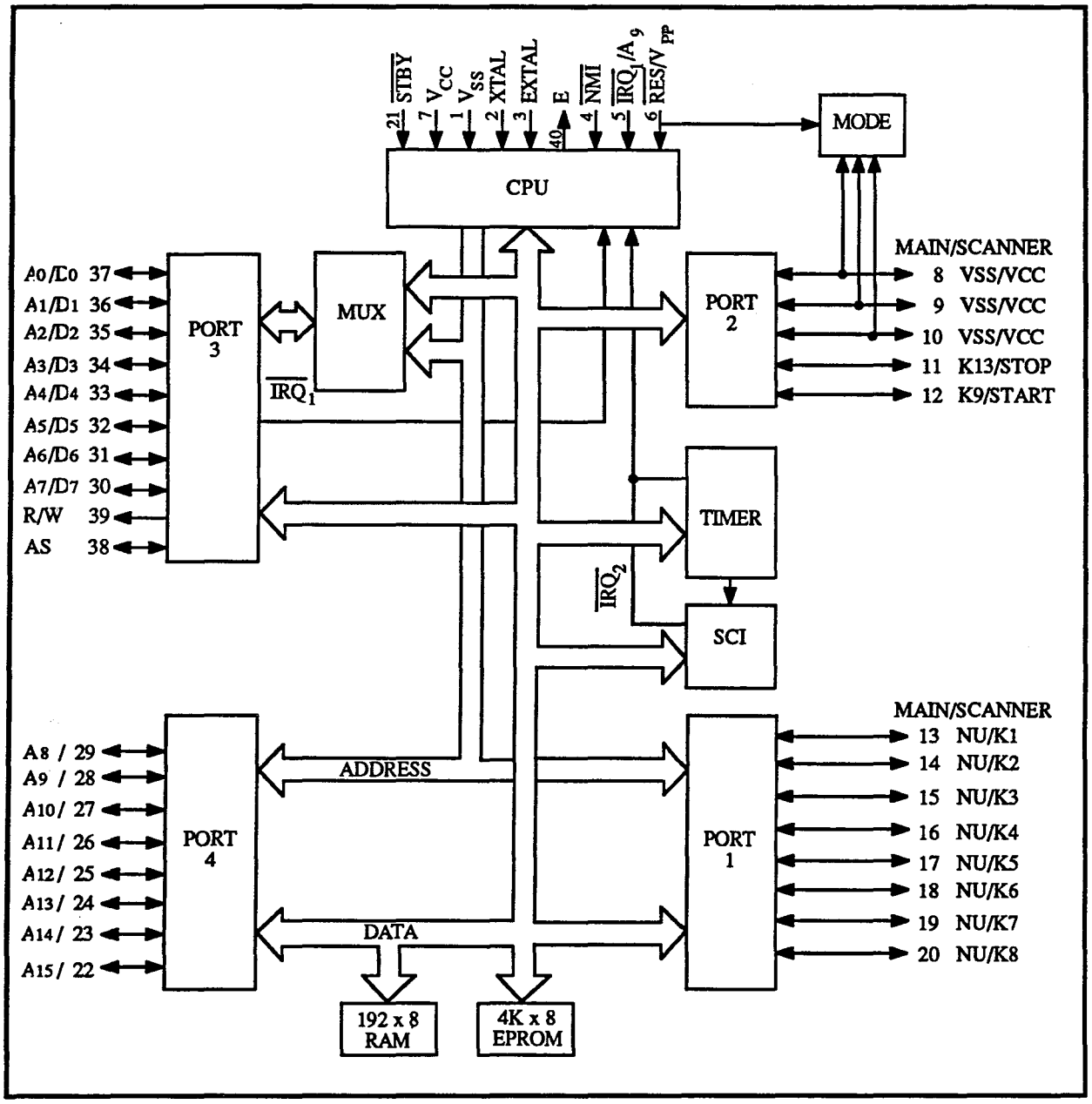
A-7671A

CRAY Y-MP CONTROLLER LIMITS

	MODE #0 HEAT EX. OFF EXCITER OFF SOF SWITCH NA			MODE #1 HEAT EX. ON EXCITER OFF SOF SWITCH NA			MODE #2 HEAT EX. OFF EXCITER ON SOF SWITCH NA			MODE #3 HEAT EX. ON EXCITER ON SOF SWITCH NA			MODE #4 HEAT EX. OFF EXCITER OFF SOF SWITCH NA			MODE #5 HEAT EX. S/S EXCITER OFF SOF SWITCH NA			MODE #6 HEAT EX. OFF EXCITER S/S SOF SWITCH NA			MODE #7 HEAT EX. S/S EXCITER S/S SOF SWITCH NA			MODE #8 HEAT EX. ON EXCITER S/S SOF SWITCH NA		
	AND /OR	HIGH LIMIT	LOW LIMIT	AND /OR	HIGH LIMIT	LOW LIMIT	AND /OR	HIGH LIMIT	LOW LIMIT	AND /OR	HIGH LIMIT	LOW LIMIT	AND /OR	HIGH LIMIT	LOW LIMIT	AND /OR	HIGH LIMIT	LOW LIMIT	AND /OR	HIGH LIMIT	LOW LIMIT	AND /OR	HIGH LIMIT	LOW LIMIT	AND /OR	HIGH LIMIT	LOW LIMIT
MODULES	OR	OFF	OFF	AND	ON	ON	AND	OFF	OFF	AND	ON	ON	AND	OFF	OFF	AND	OFF	ON	AND	OFF	OFF	AND	OFF	ON	AND	ON	ON
-4.5 BUS	OR	OFF	OFF	AND	OFF	OFF	AND	ON	ON	AND	ON	ON	AND	OFF	OFF	AND	OFF	OFF	AND	ON	NONE	AND	ON	NONE	AND	ON	NONE
-5.2 BUS	OR	OFF	OFF	AND	OFF	OFF	AND	ON	ON	AND	ON	ON	AND	OFF	OFF	AND	OFF	OFF	AND	ON	NONE	AND	ON	NONE	AND	ON	NONE
-2.0 BUS	OR	OFF	OFF	AND	OFF	OFF	AND	ON	ON	AND	ON	ON	AND	OFF	OFF	AND	OFF	OFF	AND	ON	NONE	AND	ON	NONE	AND	ON	NONE
PRESSURE	OR	OFF	OFF	OR	ON	ON	OR	OFF	OFF	OR	ON	ON	OR	OFF	OFF	OR	OFF	ON	OR	OFF	OFF	OR	OFF	ON	OR	ON	ON
TRANSFORMER TEMPERATURE	OR	OFF	OFF	AND	ON	ON	AND	OFF	OFF	AND	ON	ON	AND	OFF	OFF	AND	OFF	ON	AND	OFF	OFF	AND	OFF	ON	AND	ON	ON
PLATE TEMPERATURE	OR	OFF	OFF	AND	ON	ON	AND	OFF	OFF	AND	ON	ON	AND	OFF	OFF	AND	OFF	ON	AND	OFF	OFF	AND	OFF	ON	AND	ON	ON
INPUT TEMPERATURE	OR	OFF	OFF	AND	ON	ON	AND	OFF	OFF	AND	ON	ON	AND	OFF	OFF	AND	OFF	ON	AND	OFF	OFF	AND	OFF	ON	AND	ON	ON
OUTPUT TEMPERATURE	OR	OFF	OFF	AND	ON	ON	AND	OFF	OFF	AND	ON	ON	AND	OFF	OFF	AND	OFF	ON	AND	OFF	OFF	AND	OFF	ON	AND	ON	ON
M. G. VOLT PH-NEUTRAL	OR	OFF	OFF	AND	OFF	OFF	AND	ON	ON	AND	ON	ON	AND	OFF	OFF	AND	OFF	OFF	AND	ON	NONE	AND	ON	NONE	AND	ON	NONE
M. G. VOLT PH-PHASE	OR	OFF	OFF	AND	OFF	OFF	AND	ON	ON	AND	ON	ON	AND	OFF	OFF	AND	OFF	OFF	AND	ON	NONE	AND	ON	NONE	AND	ON	NONE
M. G. WARN CONTACT	OR	ON	ON	OR	ON	ON	OR	ON	ON	OR	ON	ON	OR	ON	ON	OR	ON	ON	OR	ON	ON	OR	ON	ON	OR	ON	ON
HEU WARN CONTACT	OR	NONE	NONE	OR	NONE	ON	OR	NONE	NONE	OR	NONE	ON	OR	NONE	NONE	OR	NONE	NONE	OR	NONE	NONE	OR	NONE	NONE	OR	NONE	NONE
LOW TEMPERATURE	OR	ON	ON	OR	ON	ON	OR	ON	ON	OR	ON	ON	OR	ON	ON	OR	ON	ON	OR	ON	ON	OR	ON	ON	OR	ON	ON
HEU FAULT CONTACT	OR	NONE	NONE	OR	NONE	NONE	OR	NONE	NONE	OR	NONE	NONE	OR	NONE	NONE	OR	NONE	NONE	OR	NONE	NONE	OR	NONE	NONE	OR	NONE	NONE
MECHANICAL BACKUP	OR	ON	ON	OR	ON	ON	OR	ON	ON	OR	ON	ON	OR	ON	ON	OR	ON	ON	OR	ON	ON	OR	ON	ON	OR	ON	ON

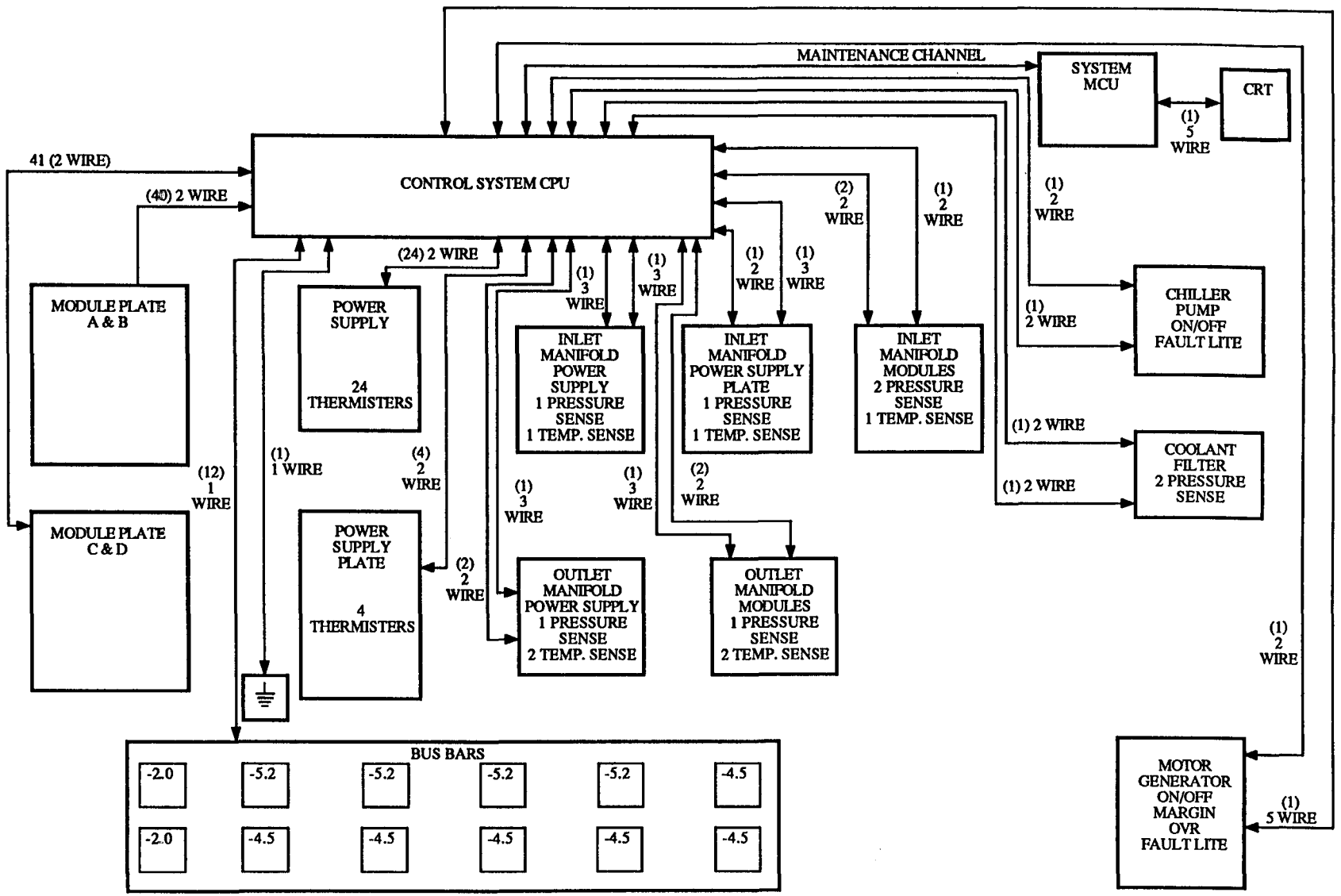
A-7672

CRAY Y-MP CONTROLLER SOFTWARE MODES



A-6509A

CONTROLLER CPU BLOCK DIAGRAM

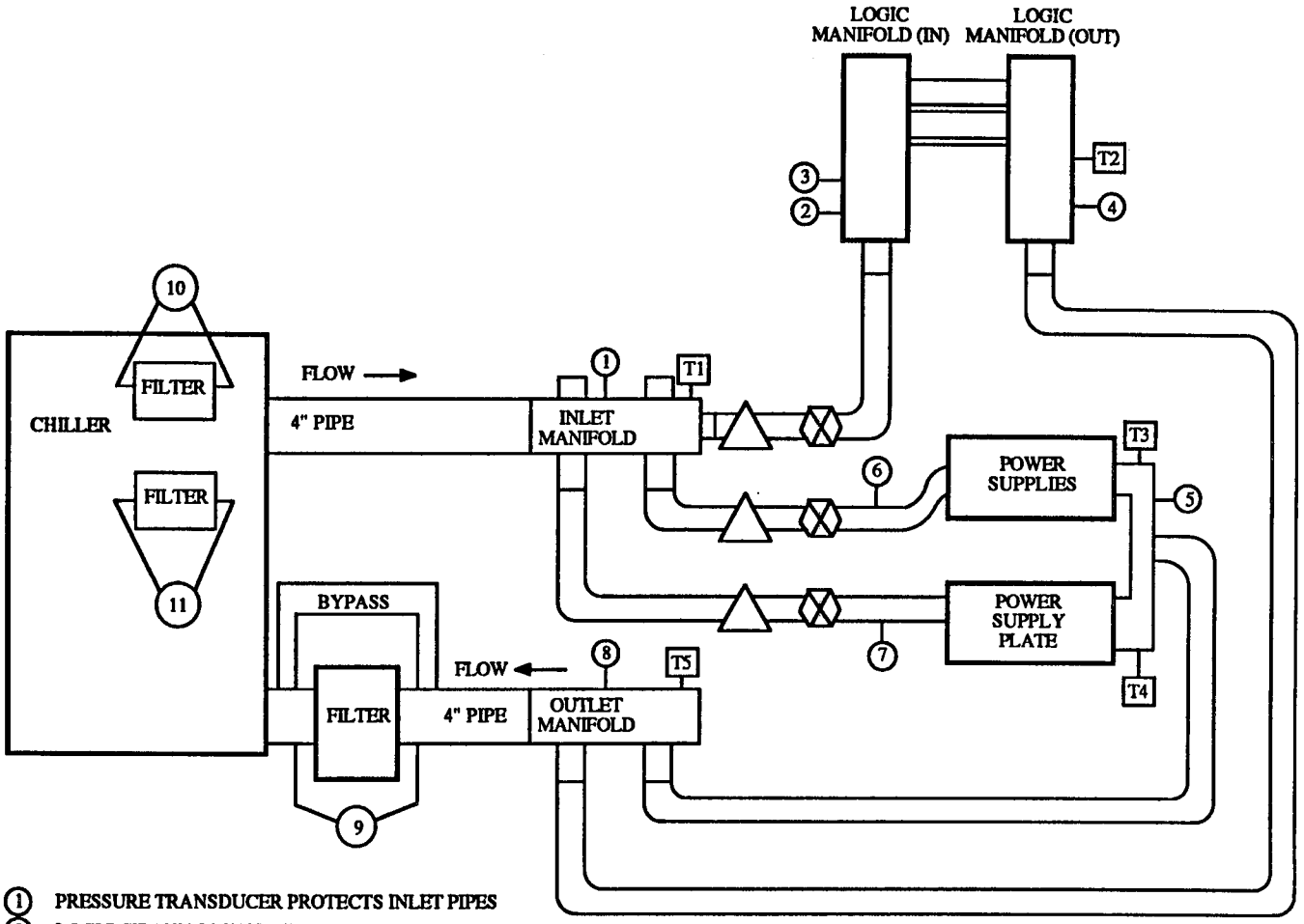


NOTE 1: Total I/O pins = 423 (excluding maintenance channel).

2: Diagram does not show mechanical backup system components.

A-6502A

CRAY Y-MP CONTROLLER SYSTEM BLOCK DIAGRAM



1. PRESSURE TRANSDUCER PROTECTS INLET PIPES
2. LOGIC CIRCUIT PRESSURE PROTECTION
3. BACK-UP FOR NUMBER 2 ABOVE
4. OUTLET PRESSURE (NEEDED TO ADJUST VALVE IN INLET)
5. POWER SUPPLY PLATE AND SUPPLIES (NEEDED TO ADJUST VALVE AT INLET)
6. POWER SUPPLY CIRCUIT PROTECTION
7. POWER SUPPLY PLATE PROTECTION
8. OUTLET MANIFOLD FOR ALL SYSTEM PEFORMANCE
9. DIFFERENTIAL PRESSURE FOR FILTER CHANGE
10. DIFFERENTIAL PRESSURE ON FILTERS
11. DIFFERENTIAL PRESSURE ON FILTERS

BALL VALVE

FLOW METER

TEMPERATURE PROBE

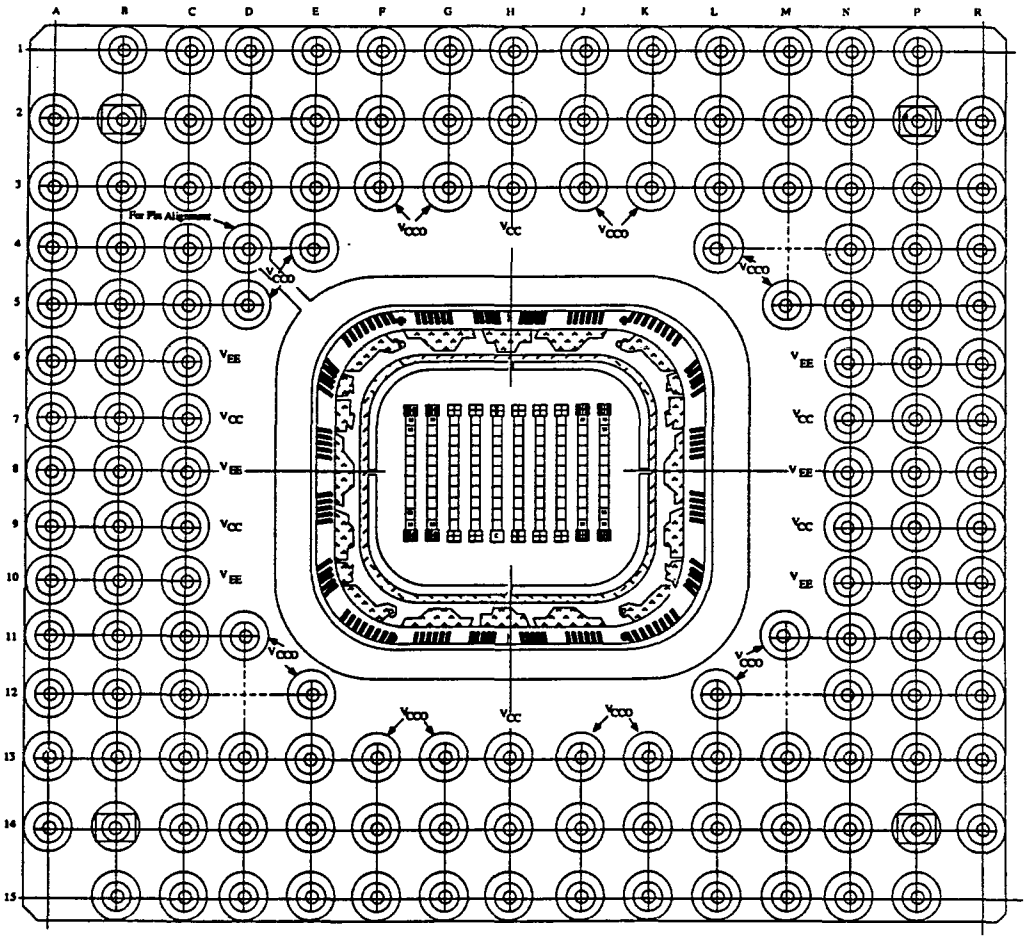
PRESSURE TRANSDUCER

A-6489

CRAY Y-MP TEMPERATURE AND PRESSURE TRANSDUCERS LOCATION

MOTOROLA

MCA2500ECL Macrocell Array



MACROCELL APPROACH

- **REDUCTION IN POWER OF AS MUCH AS 12 TO 1**
- **HIGH PACKING DENSITY OFFERS A REDUCTION IN SYSTEM COMPONENT COUNT OF UP TO 100 TO 1**
- **SUBSTANTIAL IMPROVEMENT IN CIRCUIT SPEEDS**
- **REDUCED POTENTIAL SYSTEM COST**

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BUILDING BLOCKS OF THE CRAY Y-MP MCA2500 ECL MACROCELL ARRAY

The Macrocell Array is actually an extension of the gate-array concept. Instead of gates, however, each cell in the array contains a number of unconnected transitors and resistors. Stored within a computer are the specifications for creating interconnecting patterns that can transform the unconnected transistors and resistors within each cell into logic functions called Macros.

Presently, the Macrocell library contains more than 80 different logic functions, some of which Cray Research has custom designed.

To generate an LSI design, the designer need only be concerned with developing his circuits by selecting the appropriate Macros from the Macro library, placing these in the desired cell location and creating the necessary cell interconnecting pattern. The computer itself generates the proper intra-connecting pattern within each cell.

The Macrocell approach offers a tremendous reduction in delivery time. From the time the customer gives the go ahead signal for generating the metal mask until he receives the finished parts is typically 13 weeks.

Compared to gate arrays, the use of higher components density and more efficient designed subcircuits (macros) yields a substantial improvement in performance (circuit speed), while a greater utilization of on-chip components reduces potential system costs.

Compared with systems developed with discrete logic (separately packaged logic function) the high packing density of the MCA2500 ECL chips offers up to 100 to 1 reduction in system component counts, with a power dissipation improvement (reduction) of as much as 12 to 1.

ESD Sensitivity - Y-MP Gate Array

ESD tests on the 148-pin gate array indicates 100% failure upon a discharge of 200V input pin to input pin, 67% failure at 600V input pin to ground.

The Fairchild 16-gate product has ESD sensitivity in the 600V to 1500V range. Process variations (mask alignment, oxide thickness, etc.) can lower this susceptibility to < 500V. Experience within CRI manufacturing facility has been as high as 50% fallout between inventory and module test. The current limit of 500V during ESD audits will have to be lowered to < 50V to ensure good yield through the manufacturing process.

MCA2500 ECL HANDLING PRECAUTIONS

Static damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged inputs are easiest to detect because the inputs have been completely destroyed and are either shorted to Vcc, shorted to Vee, or open circuited. The effect is that the device will no longer responds to signals present at the damaged inputs. Less severe cases are more difficult to detect because they show up as intermittent failures or as degraded performances. Another effect of static damage is that the input generally have increased leakage current. The MCA2500ECL logic chip is not immune to static voltage discharge that can be generated during handling. The static voltage generated by a person walking across a waxed floor have been measured in the 4-15kV ranges (depending on humidity, surface conditions, etc.). Therefore, the following precautions should be observed:

1. Do not exceed the maximum ratings specified in the electrical characteristics.

2. All unused device inputs should be connected to Vee and Vcc.

3. All low-impedance equipment (pulse generators, etc.) should be connected to the inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.

4. A module containing MCA2500ECL devices is merely an extension of the device, and the same handling precautions apply. Contacting edge connectors wired directly to MCA2500ECL inputs can cause damage. Plastic wrapping should be avoided.

5. All MCA2500ECL devices should be stored or transported in material that are antistatic. MCA2500ECL devices must not be inserted into conventional plastic "snow" styrofoam or plastic trays, but should be left in their original containers until ready for use.

6. All MAC2500ECL devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended.

7. Nylon or other static generating material should not come in contact with the MCA2500ECL devices.

8. If automatic handlers are being used, high levels of static electricity may be generated by the movement of the device, the belts or the modules. Reduce static build-up by using ionized air blowers or room humidifiers. All parts of the machine which come into contact with the top, bottom or side of the MCA2500ECL package must be grounded to metal or other conductive material.

9. When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.

10. The following steps should be observed during wave solder operations:

    a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.

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b. The loading and unloading work bencher should have conductive tops which are grounded to an earth ground.

c. Operator must comply with precautions previously explained.

d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.

11. The following steps should be observed during board-cleaning operations:

a. Vapor degreasers and baskets must be ground to an earth ground.

b. Brush or spray cleaning should not be used.

c. Assemblies should be placed into a vapor degreaser immediately upon removal from the antistatic container.

d. Cleaned assemblies should be placed in antistatic containers immediately after removed from the cleaning basket.

e. High velocity air movement or applications of solvents and coating should be employed only when assembled printed circuit boards containing MCA2500ECL devices are grounded and static eliminator is directed at the board.

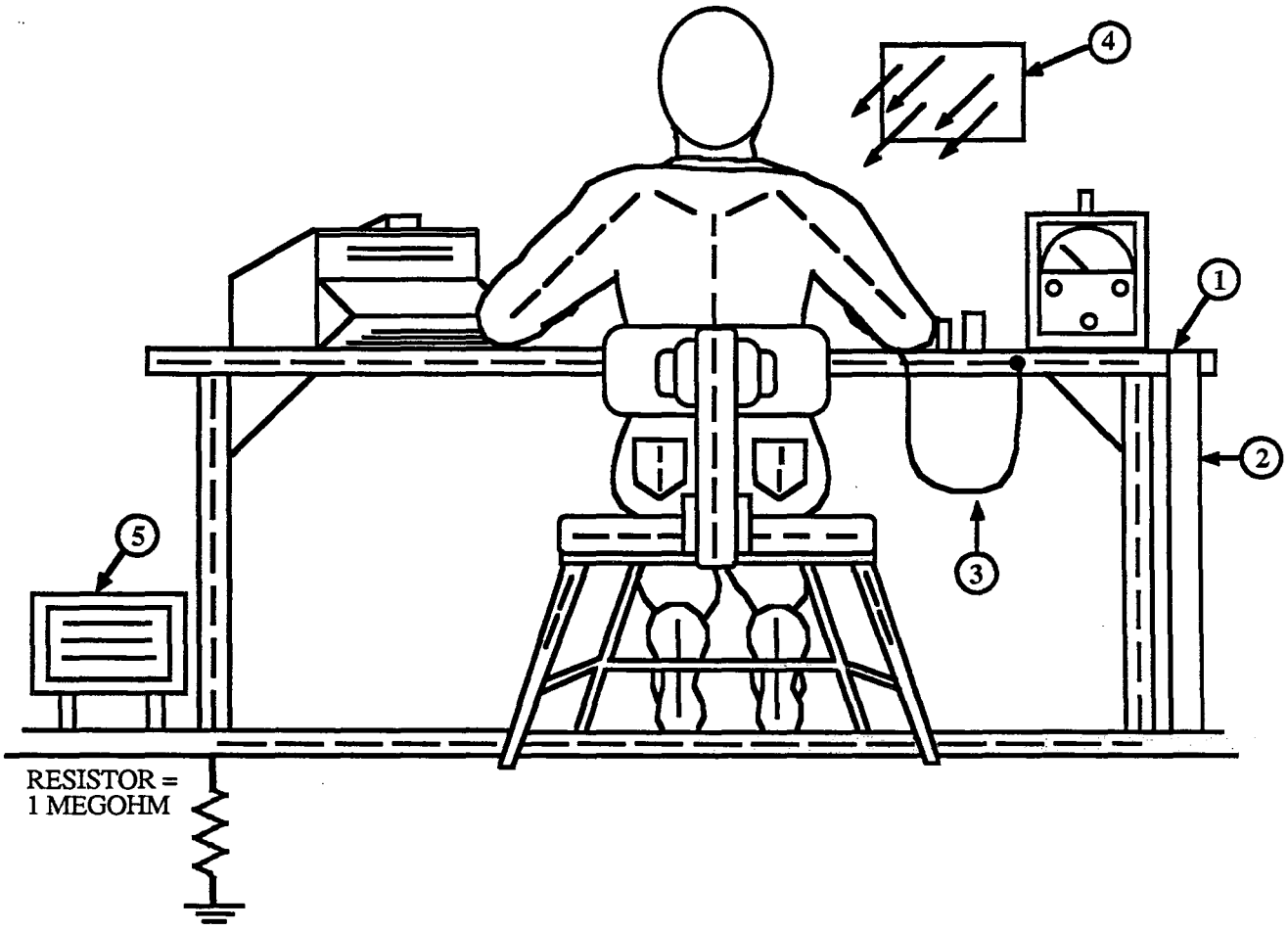
12. The use of static detection meters for production line surveillance is highly recommended.

13. Equipment specifications should alert users to the presence of MCA2500ECL devices and require familiarization with specification prior to performing any kind of maintenance or replacement of devices or modules.

14. Do not insert or remove MCA2500ECL devices from test with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.

15. Double check test equipment setup for proper polarity of Vee and Vcc before conducting parametric or functional testing.

16. Do not recycle shipping rails or trays. Continuous use causes deterioration of their antistatic coating.



NOTES:

1. 1/16 inch conductive sheet stock covering bench top work area.

2. Ground strap.

3. Wrist strap in contact with skin and smocks.

4. Static neutralizer. (Ionized air blower directed at work.)
   Primarily for use in areas where direct grounding is impractical.

5. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%.
   CAUTION: Building heating and cooling systems usually dry the air causing the relative humidity inside of buildings to be less than outside humidity.

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TYPICAL MANUFACTURING WORK STATION

FEATURES OF THE MCA2500 ECL MACROCELL ARRAY

The MCA2500 ECL Macrocell Array uses the high performance MOSAIC II (Motorola Oxide Isolated Self-Aligned Implated Circuits) process and contains approximately 2500 equivalent gates with actual gate delays of 300 to 350 ps (typical). The MCA2500 ECL chip consists of 178 cells. There are 110 major cells (M) and 68 output cells (0).

Major Cells

Each Major Cell can be divided into two independent half cells, independent quarter cells, or a three quarter and a quarter cell. As an example, the upper half of a Major Cell could be designated a 3-bit Adder Sum (M285) the other half a 3-bit Adder Carry (M286). Outputs of a Major Cell can only drive inputs of other macros within the array, The Major Cells in the array comprise the internal area on the chip and are used for the majority of logic capability. Each Major Cell contains 56 transistors and 56 resistors. These components are connected on first layer metal to form logic functions with four 2-level series-gated structures. Each macro in the major cell library specifies how much of the cell (either 1/4, 1/2, 3/4 or 1 entire Major Cell) is needed to implement that particular function. The power, ground, and bias supply lines are automatically accomplished by the CAD (Computer Aided Design) system. The channels in the vertical direction are accomplished on first layer metal while the channels in the horizontal direction are accomplished on second layer metal. The second layer metal is separated from the first layer by a dielectric isolation. Metal runs on the chip have little effect of delay times because of the dielectirc isolation between metal and active devices. Connection between first layer and second layer metal are accomplished with VIA's. The interconnecting of cells on the array can be compared to routing lines on a two sided PC board. A third layer of metal is used for power distribution to minimize voltage drops and is completely transparent to the user.

Although the chip is large, good yields are experienced since most of the chip is composed of metal for interconnecting the macros. The total emitter area of the active device is the primary concern of determining the yield.

Output Cells or X Cells

The Output Cells are located at the top and bottom of the array. The Output Cells are used to interface to logic outside the chip by providing 60 ohm drive capability. Each Output Cell contains 15 transistors and 10 resistors. These components are connected together on first layer metal to form logic functions with one full series-gated structures. Functions requiring two series-gated structures can be formed by using two adjacent output cells. Output cells have a typical current source of 3.5 ma. The primary output of the Output Cell is labeled "X" as in X252 "XA" and when it is used, it must be connected to the base of an output emitter follower located near the bonding pad. When the "X" Output Cell is used and tied to a 60 ohm resistor to a -2.0 V it provides a typical current load of 30 ma.

The "Z" outputs as in X252 "ZA" cannot go off the board, but can be used as inputs inside the package. The "Z" output cannot feed into input with an asterisk (*) input. However, the "Z" output can feed into an input with an asterisk that has a circle around it (Ⓢ). When running short on Major Cells, Output Cells with "Z" output can be used. The "Z" outputs have a larger voltage swing since a tap resistor is not used in the Output Cell macros. The "Z" output load can be selected from 0 or 1.0 ma.

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Lower Level Input

Inputs that are connected to an input follower are marked with an asterisk, *, and are connected to the lower level of a series gated structure. Unmarked inputs go directly to the base of a transistor connected in the upper level of a series gated structure. These two different types of inputs are differentiated in order to specify different propagation delays, and different rules for connecting to input compensation networks and to input package pins.

The reset and set inputs of a flip-flops and latches are also marked with an asterisk to indicate that they cannot be connected to package pins even though they are not connected to an input follower.

For Major Cell macros, upper level inputs and lower level inputs marked with a circle around the asterisk, ⊛ , are allowed to be connected to package pins or to "Z" outputs of an Output Cell macro. Stated differently, Major cells macros with input marked with an asterisk (with no circle around it) are not allowed to be connected to package pins or to the "Z" outputs of an Output Cell macro due to potential saturation problems.

Upper Level Input

Inputs with no markings are considered upper level inputs and can be connected by package pins or other major cells. Package pins originate from Output Cells with the "X" output used.

Clock Pulse Generator Cell

The Clock Pulse Generator Cell is not used. The Macro Cells are used to generate the clock on the chip. Each option has its own clock pulse shaper (t0, t1, t2).

MCA2500 ECL CONSIDERATIONS

The MCA2500 ECL is a 148 leaded pin package. An inner ring connects the power leads with the shortest bonding wire length. The numbering of the pins are labeled with the column number (A-R) followed by the row number (1-15). The ground for the output followers of the Output Cells (Vcc0) is separated from the ground for the rest of the logic (Vcc). The current supplied to (Vcc) is rather constant while the current supplied to (Vcc0) changes when outputs are switching.

The MCA2500 ECL package has 120 I/O pins, 6 Vee pins, 6 Vcc pins and 16 Vcc0 pins and one pin for orientation.

Test Diode

A method is available on the CAD system for placing a test diode on pin H14 of the 149-pin grid package. With the test diode in place, the junction temperature and the thermal characteristics of the package can be tested. Pin H14 is the only pin that can be used for placing the test diode. The cathode (-) is connected to pin H14 and the anode (+) is connected to Vcc0 pin K13 and J13.

Internal Unused Inputs or Outputs

The unused outputs can be left floating unconnected. Unused inputs in the array will automatically be forced to a low voltage (Logic "1") by the CAD system (the input base is shorted to the emitter). There are no provisions for providing a high voltage (Logic "0") on an unused input. A (Logic "0") can be generated using a spare inverter from a Major Cell.

Package Pins to Macro Inputs

For Major Cell and Output Cell macros, upper level inputs and lower level inputs marked with a circle around the asterisk (⊛) are allowed to be connected to package pins. Inputs of Major Cell and Output Cell macros marked with an asterisk (with no circle around it) are not allowed to be connected to package pins, but only fed by major macro cell outputs.

Package Pins Connected to Macro Outputs

It is not allowed to connect Major Cell macro outputs to package pins. Also, it is not allowed to connect the "Z" output of an Output Cell macro to a package pin since these are used to drive internal loads. The X output of an Output Cell macro are only connected to an I/O pin by connecting the X output to the base of the output emitter follower near the bonding pad (via the CAD system).

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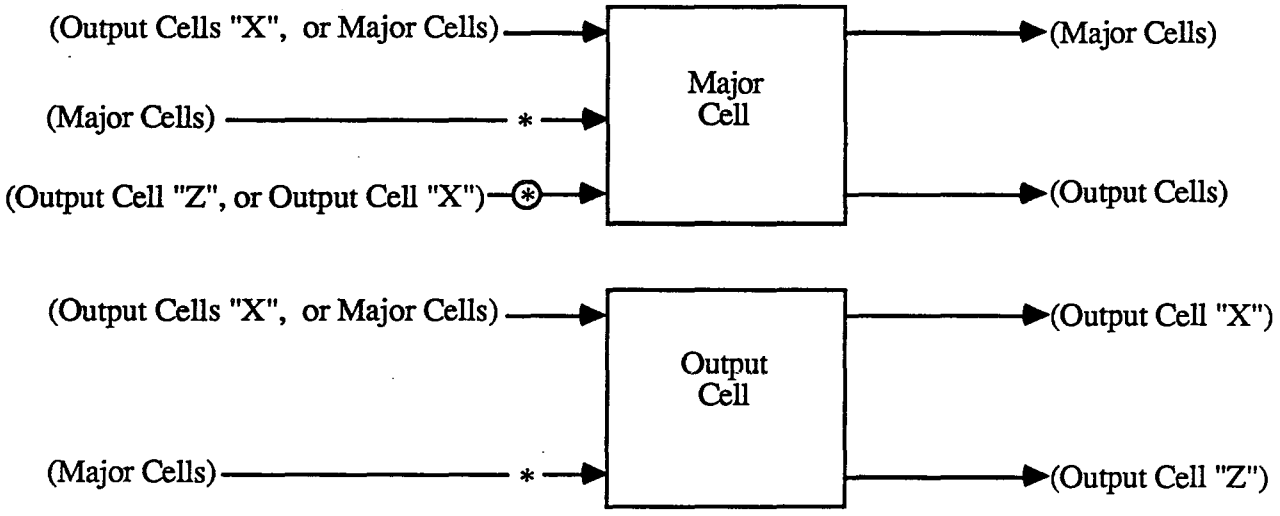
Internal Connections

Outputs of Major Cell macros can be connected to any input of a Major or Output Cell macro. For Major Cell macros, upper level inputs and lower level inputs marked with an asterisk and a circle around it ⊛ are allowed to be connected to the "Z" output of the Output Cell macro.

The X output of an Output Cell macro can only be connected to the output emitter follower near the bonding pad. The output of the bonding pad can be connected to macro input, the same rules for package pins connected to macro inputs.



Output cell "X" must go off the Macrocell Array.
Output cell "Z" cannot go off the Macrocell Array.

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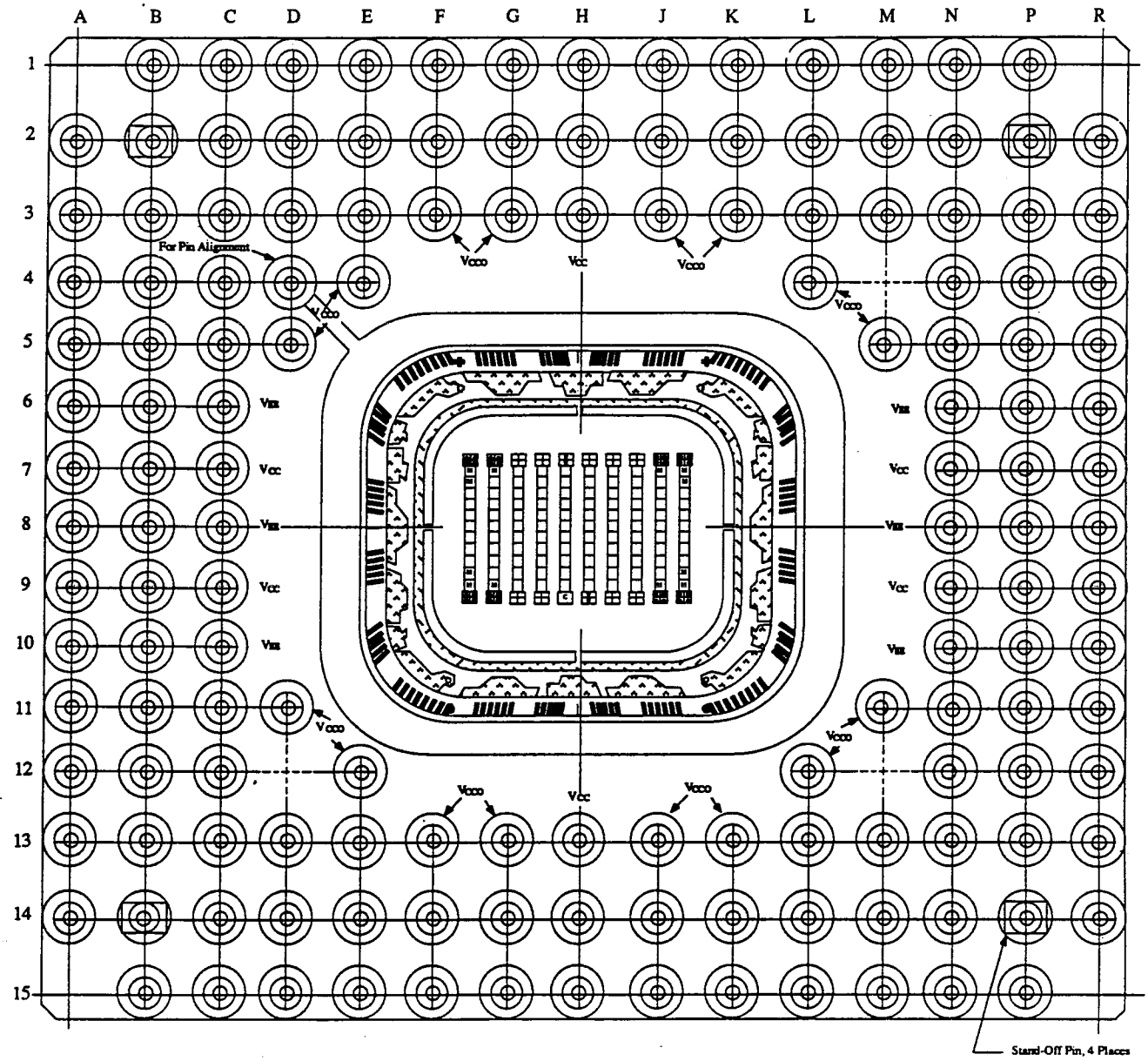
A-5297 J.E.S.

CRAY Y-MP MAJOR CELLS OR OUTPUT CELL CONNECTIONS



NOTES: VCC pins - H3, H13, C7, N7, C9, N9
VEE pins - C8, N8, C6, N6, C10, N10
VCCO pins - F3, G3, J3, K3, E4, L4, D5, M5, D11, M11, E12, L12, F13, G13, J13, K13
Pin D4 is connected to the seal ring, but isolated electrically.

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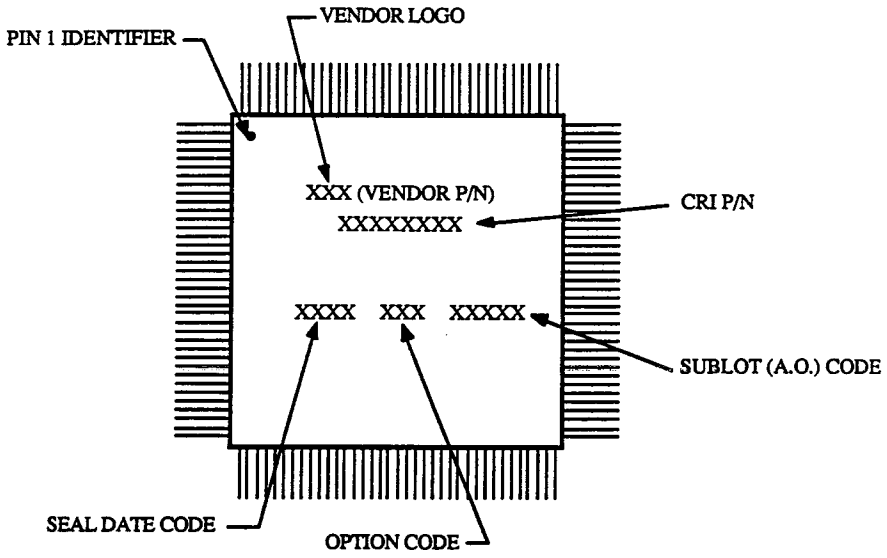
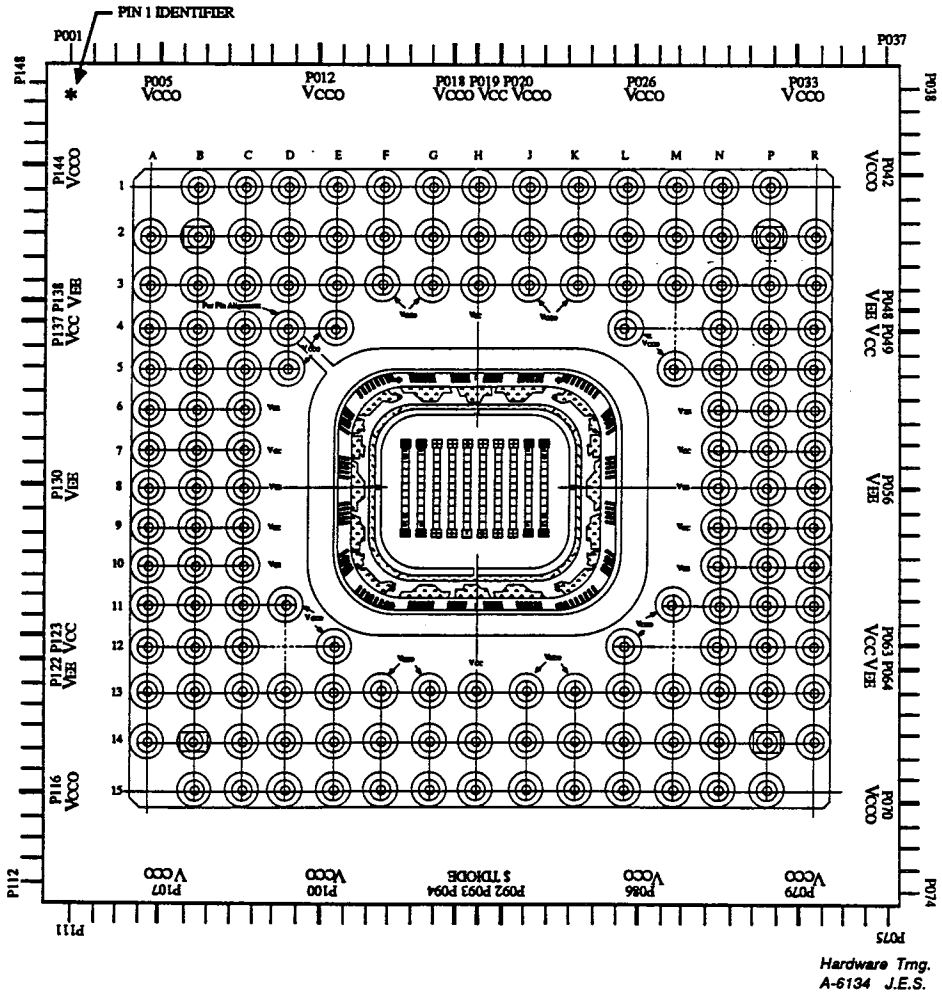
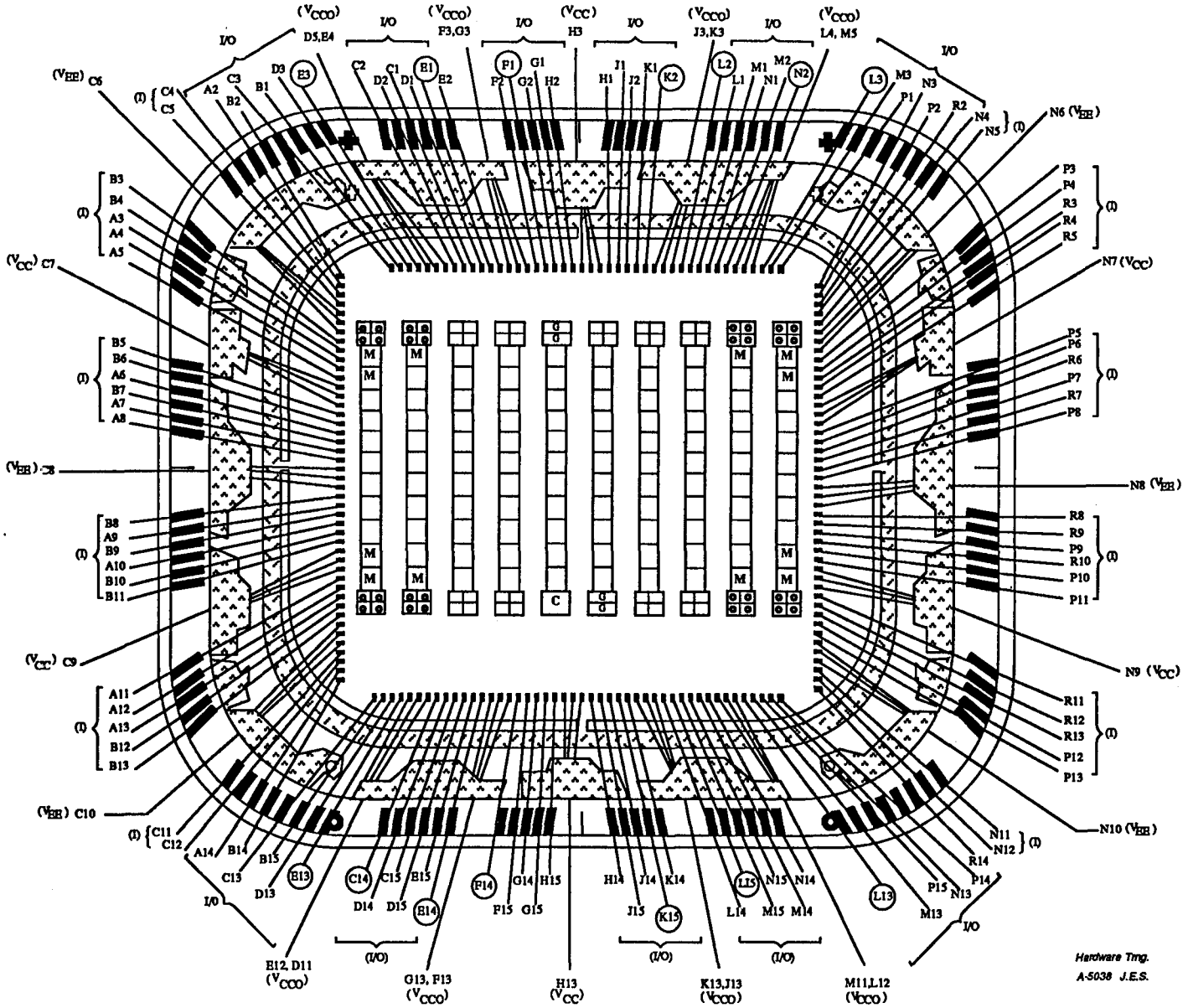
CRAY Y-MP MOTOROLA PIN LOCATIONS FOR 149 PIN GRID ARRAY PACKAGE





CRAY Y-MP PIN LOCATIONS FOR
148 PIN ARRAY PACKAGE



NOTE: NUMBERS SHOWN ARE WIRE BOND LEAD NUMBERS AND DO NOT CORRESPOND WITH PIN NUMBERS.

1. 149 total pins; Pin D4 is for alignment only, 52 Input pins (I), 68 Input/Output pins (I/O), and 28 power pins.

CRAY Y-MP I/O PIN ASSIGNMENTS FOR 149-PIN GRID ARRAY PACKAGE

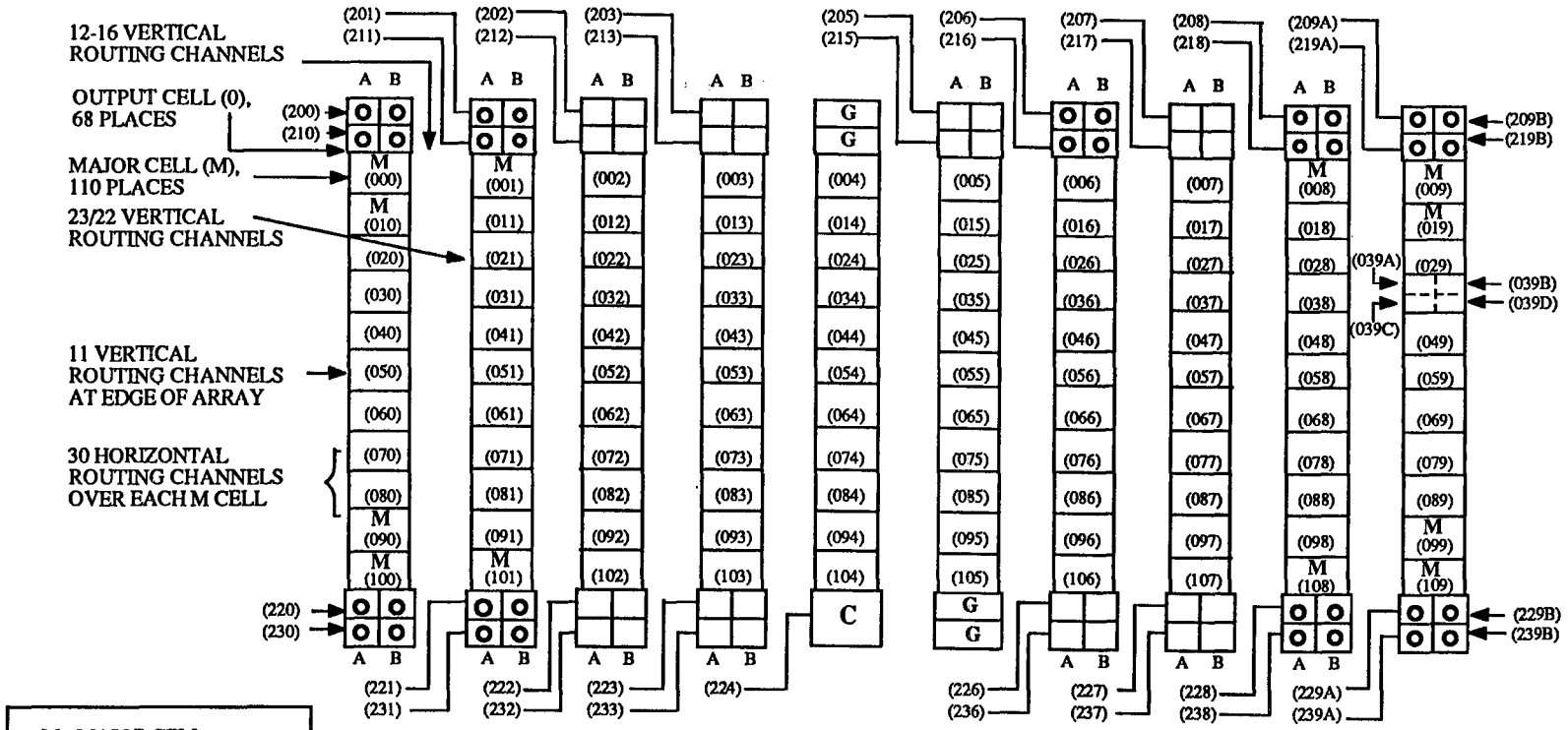


TABLE 1 - Basic Macrocell Array Features

1. 178 total cells (110 major cells and 68 output cells).
2. Up to 2760 equivalent gates if full adders and latches are used in all the cells.
3. Up to 2100 equivalent gates if flip-flops and latches are used in all the cells.
4. Die size - 263 mils x 274 mils.
5. Power Dissipation - 8.0 watts typical.
6. 3.1 mW per equivalent gate (for 2100 gates and 6.5 watts).
7. Major cell delays - 0.25 to 1.25 ns typ (0.35 to 1.77 ns max.)
8. Output cell delays - 0.5 to 1.0 ns typ (0.65 to 1.5 ns max.)
9. Certain macros can drive 25 ohm loads (Not used).
10. All output cells can drive 50 ohm loads.
11. Edge speed - 0.4 ns min 20 to 80% (0.6 ns min with edge rate slow down option).
12. Ambient temperature range (with heat sink and 750 lfpm air flow) = 0°C to 70°C.
13. θJA = 3.3 °C/W with heatsink and 750 lfpm air flow in a 149-pin grid array package.
14. Maximum operating junction temperature, TJ = 130°C
15. Voltage compensated, V_{EE} = -4.2 to -5.72 V.
16. Interfaces with both MECL 10K and 10KH with a 100K option also available.
17. On-chip clock pulse generator (Not used).

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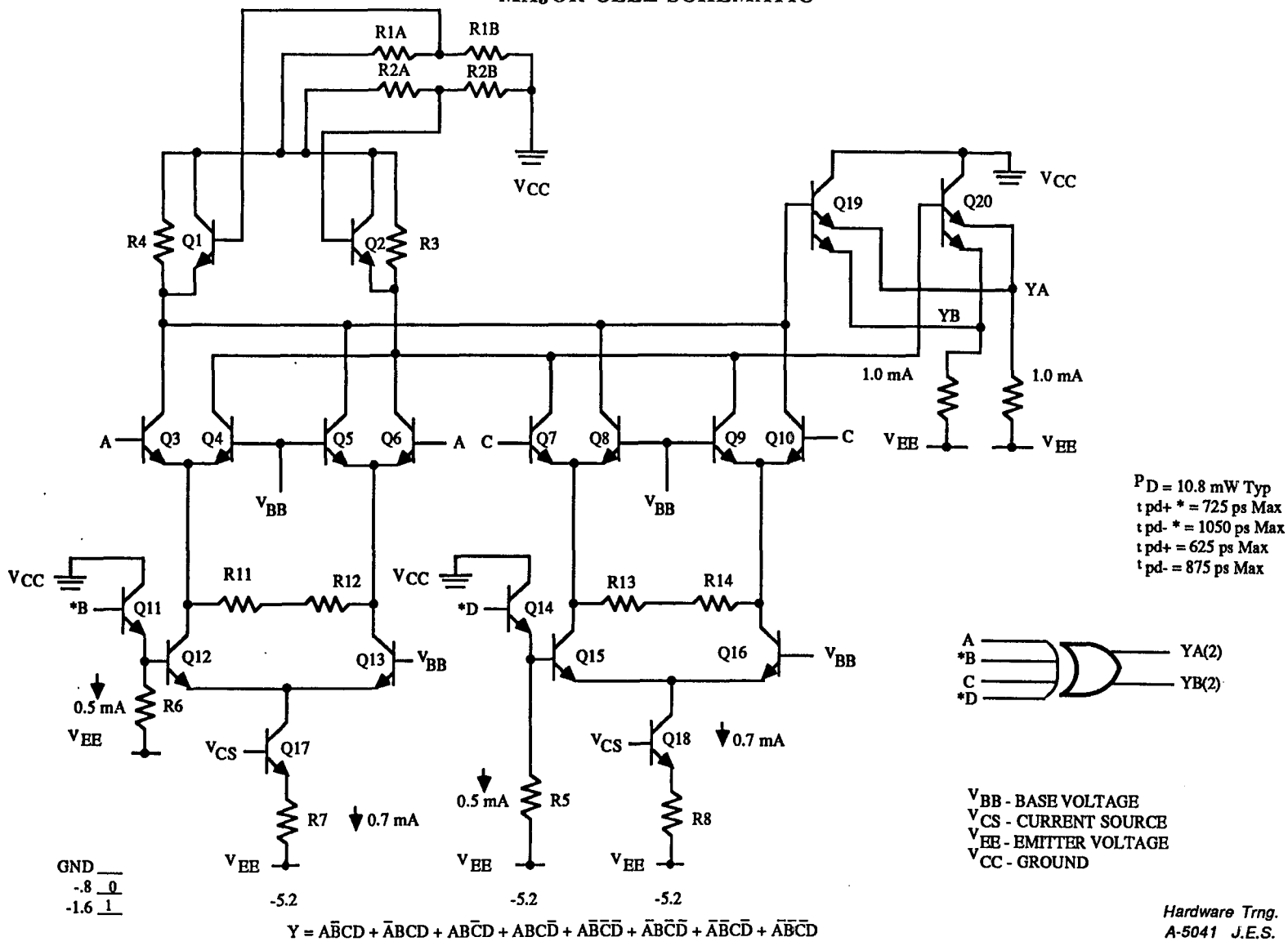
CRAY Y-MP MCA2500ECL MACROCELL ARRAY LAYOUT

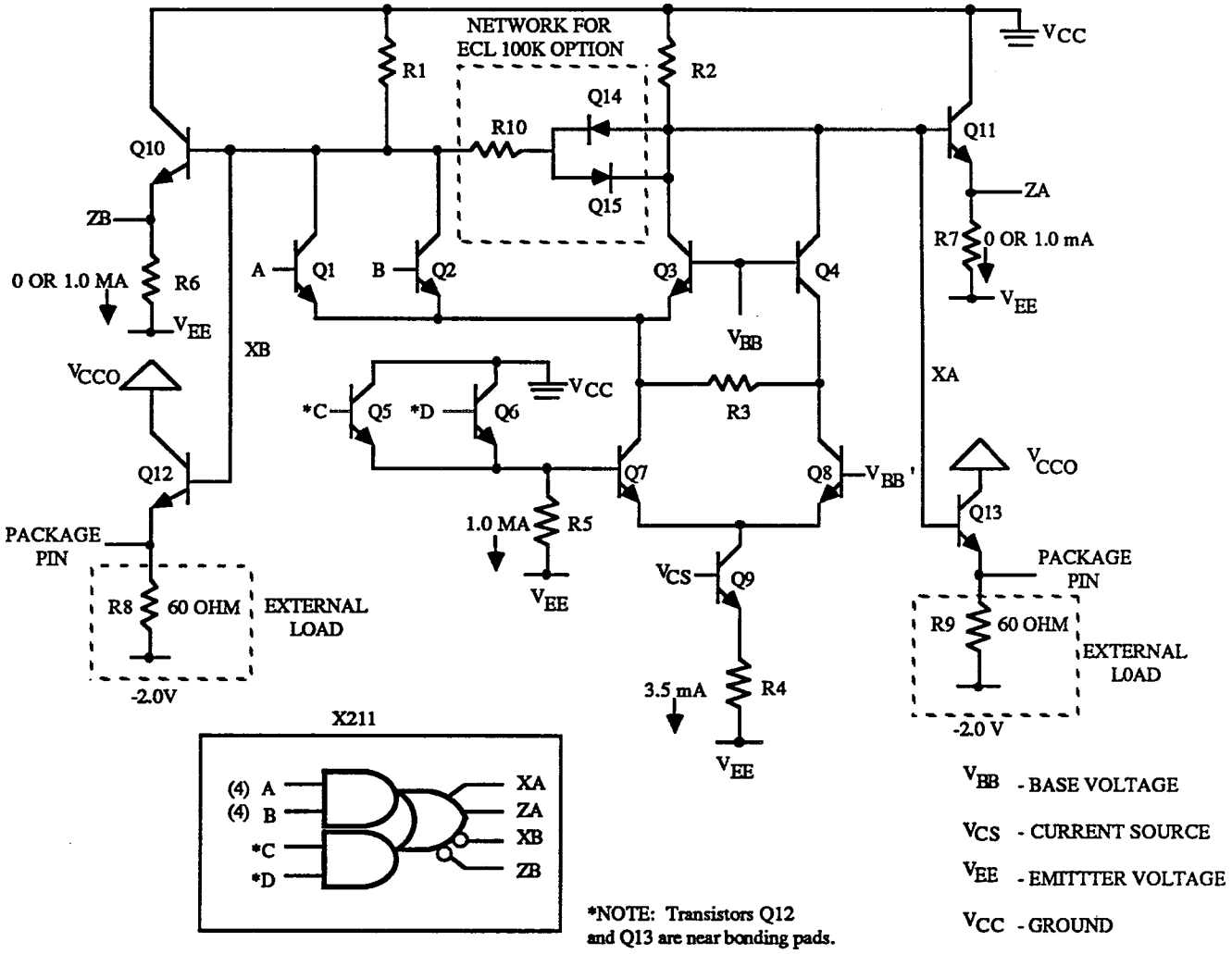
MAJOR CELL SCHEMATIC



$$Y = A\bar{B}CD + \bar{A}BCD + AB\bar{C}D + ABC\bar{D} + A\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}\bar{C}D$$

CRAY Y-MP SCHEMATIC OF 4-INPUT EXCLUSIVE OR GATE (M224)

OUTPUT CELL SCHEMATIC



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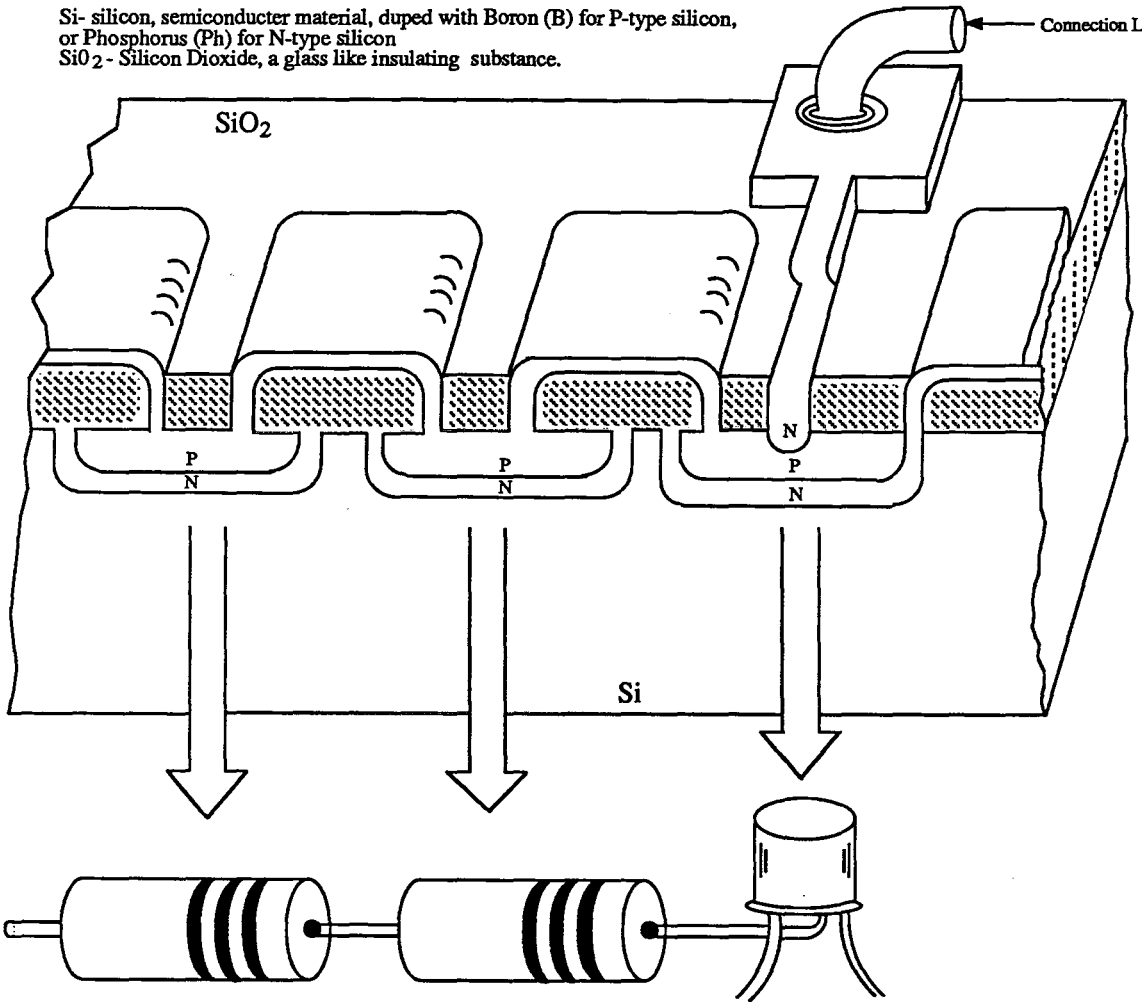
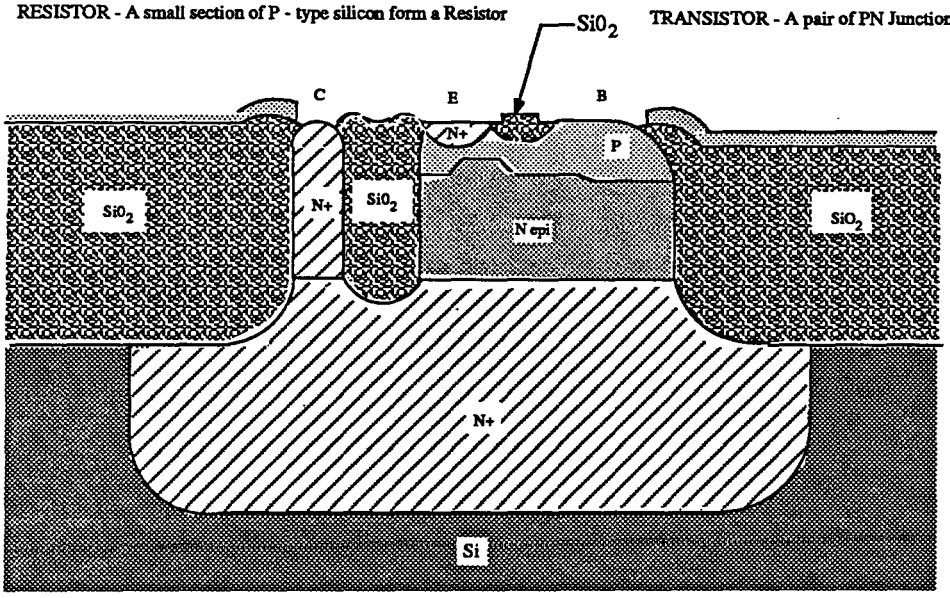
CRAY Y-MP SCHEMATIC OF OUTPUT CELL, X211 OR-AND GATE

Si- silicon, semiconducter material, duped with Boron (B) for P-type silicon, or Phosphorus (Ph) for N-type silicon
SiO_2 - Silicon Dioxide, a glass like insulating substance.



RESISTOR - A small section of P - type silicon form a Resistor

TRANSISTOR - A pair of PN Junctions forms an NPN TRANSISTOR



Cross-Section of MOSAIC II Process

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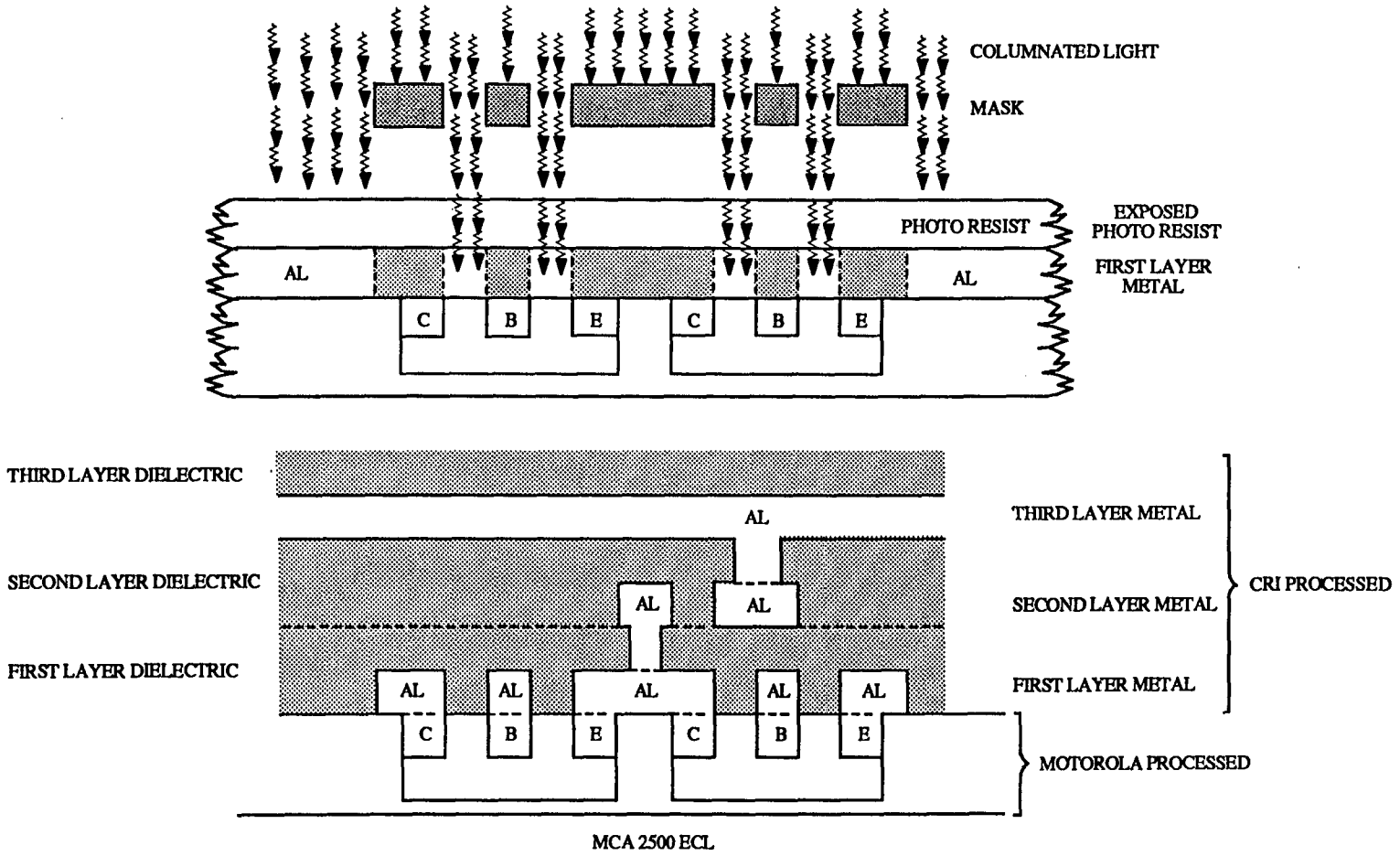
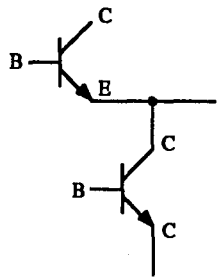
CRAY Y-MP INTEGRATED CIRCUITS

MOSAIC II - A New Process for High Speed, High Density Bipolar Circuits

A new process called MOSIAC II[1] is used in the MCA2500ECL in order to achieve the high performance requirements of 0.30 ns (typical) for internal gate delays. The process is oxide isolated in the same manner as was its predecessor, MOSIAC I. The key improvement over MOSIAC I is the implementation of walled emitter structures. Usage of the walled emitter greatly reduces the device area and the parasitic capacitances associated with the device. A reverse master mask technique (RMMT) is used to minimize the collector to emitter leakage current. The reverse master mask structure is the inactive base areas covered by oxide on either side of the emitter. The active base and emitter are both implanted using this oxide for mask edge definition, so they both can be implanted without an intermediate masking step. Eliminating the step reduces the collector-emitter leakage current in a walled-emitter device. Separating the active and inactive base implants also allows a reduced series base resistance without compromising the current gain of the active device. Reduction of series base resistance is critical for building small devices with high performance characteristics. The collector resistance has been kept low with the aid of a thin epi, and a deep n + collector. The width of the emitter stripe is only 2 microns. Three levels of metalization have been used, two for interconnection wiring and the third for power bus distribution.

[1] M. G. Farrell and S. Mastroianni, U. S. Patent 4,199,380, April 2, 1980.





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CRAY Y-MP MCA 2500 ECL INTEGRATED CIRCUIT

CELL ARRAY TERMINOLOGY

The term cell array is used to describe a VLSI circuit which contains one or more logic macro cells.

The term macrocells is used to describe a logical function which is performed internal to the cell array. A macro has one or more identical outputs which are logically formed from two or more inputs. Each macro is correspondent to a Boolean equation defined in the macrocell specification.

CELL ARRAY MACRO SYNTAX

The macro definition is a shorthand (high level) expression stating the function of the particular macrocell and its outputs and arguments. Outputs always appear on the left side of the equal sign and the function with its arguments are written to the right of the equal sign.

All signal names are a single letter plus up to three numbers (for example, A, A0, A12) and each new letter then serves as a natural delineator in a string.

Legal Characters and Definitions

Comma

- Delineates identical output signals in a Boolean equation
  EXAMPLE: K, M = AB

- Delineates functional arguments which are functionally separable
  EXAMPLE: P6 = PCARRY (C5-0, E4-0)
  C5-0 are the Carries.
  E4-0 are the Enables.

Semicolon

- Serves as an indicator for the latched gate and also delineates the Boolean expression from the clocking term
  EXAMPLE: Q3-0 - D3-0/E;T
  D3-0/E is the Boolean expression.
  T is the clocking term.

Colon

- Conditional indicator which says that execution of the expression to the left of the colon is based upon the result of the expression to the right of the colon
  EXAMPLE: Q = E:DCD(ALL-0)/S+W
  The output Q is equal to the data E located at address specified by All-0 if the chip is selected. The condition is the decode of the address.

Exclamation Point

- Serves to indicate concatenation of functions within a macro
  EXAMPLE: Y1!Y2 = Sumcarry (A, BC, D)
  Means Y1 = Sum (A, BC, D)
  Y2 = Carry (A, BC, D)
  Y3!Y4 = AB;T/E1
  Y3 is the D Flip-Flop output port
  Y4 is the D Latch output port

Dash

- Serves to indicate a contiguous string of signal names
  EXAMPLE: D5-0
  Means D5 D4 D3 D2 D1 D0

Parentheses

- Associate arguments with a particular functional
  EXAMPLE: S = SUM(A, D, C)
  Signals A, B and C are SUMmed.

- Serves as a grouping of Boolean terms

  EXAMPLE: (ABC) $\overline{(DEF)}$
  Which is the result of ABC ANDed with the result of $\overline{DEF}$

Brackets

- Serves as a grouping of Boolean terms, especially showing assignment to a particular gate
  EXAMPLE: I = [(AB)] + [(CD)] + [(EF)] + [(GH)]
  Which shows inputs A, B to one gate; C, D to another, etc.

Slash Mark

- To be read as an "if" condition
  EXAMPLE: Q7 = DCD (A2-0)/E1E2
  1 of 8 decodes appear at the output if E1 and E2 are true.

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Reversed Slash Mark

- To be read as "EXCLUSIVE OR"
  EXAMPLE: A\B
  A "EXCLUSIVE OR" B

Plus Sign

- To be read as "OR"
  EXAMPLE: A + B
  A "OR" B

Equal Sign

- Delineation between output and input terms indicating equality

Functions

- PCARRY - propagate carry
- DCD - decode
- SUM - an addition
- CARRY - carry (result from a sum)
- MUX - multiplex (select one from many)
- DIFF - differential input

Special Notes

- 0 or !0 or Z999 = forced "0"

- # = forced "1"
  Consider the string C5-0 = C5 C4 C3 C2 C1 C0.
  If you want C3 left open, then write C5 C4 # C2 C1 C0.

- The terms appearing in all macro definitions are merely dummy variables which are replaced by the signal names used in the Boolean defining a particular operation!
  EXAMPLE: The macro definition - P6 = PCARRY (C5-0, E5-1) could appear as:
  D12 = PCARRY(B11-6,G10-6) or as:
  M= B6G6G7G8G9G10 + B7G7G8G9G10 + B8G8G9G10 + B9G9G10 + B10G10 + B11

- If any 0 or # appear in a Boolean expression, then the entire sequence of terms specified by the macro definition must be written explicitly.
  EXAMPLE: Q2-0 = SUM(A2-0, 1)/E2E1E0
  Suppose A1 = 0 always.
  Then write: Q2-0 = SUM(A2 0 A0,1)/E2E1E0

- The number of signals appearing in the argument for a function must always be consistent with the number of signals displayed in the macro definition.

- In any case where an expression is used in the elementary Boolean expression rather than the macro form, all signal names must be written in the defined complete form.

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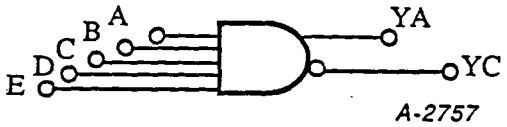
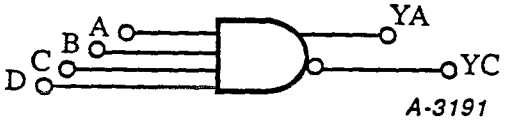
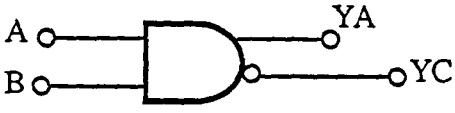
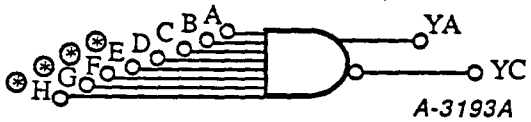
MACROCELL LIBRARY

	EQUATION	CELL	SCHEMATIC
M 200	FIVE INPUT AND/NAND EXPANDED BOOLEAN: YA = ABCDE YC = $\overline{YA}$ MACRO BOOLEAN: YA = ABCDE YC = $\overline{YA}$	1/4 M	 A-2757
M 201	FOUR INPUT AND/NAND EXPANDED BOOLEAN: YA = ABCD YC = $\overline{YA}$ MACRO BOOLEAN: YA = ABCD YC = $\overline{YA}$	1/4 M	 A-3191
M 202	TWO INPUT AND/NAND EXPANDED BOOLEAN: YA = AB YC = $\overline{YA}$ MACRO BOOLEAN: YA = AB YC = $\overline{YA}$	1/4 M	 A-3192
M 203	EIGHT INPUT AND/NAND EXPANDED BOOLEAN: YA = ABCDEFGH YC = $\overline{YA}$ MACRO BOOLEAN: YA = ABCDEFGH YC = $\overline{YA}$	1/2 M	 A-3193A

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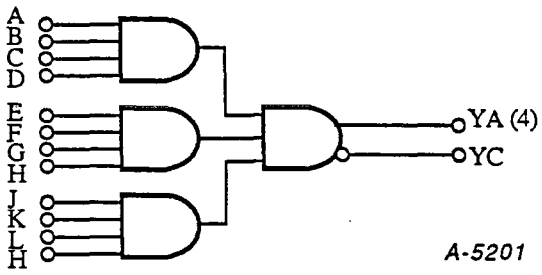
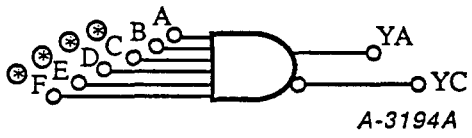
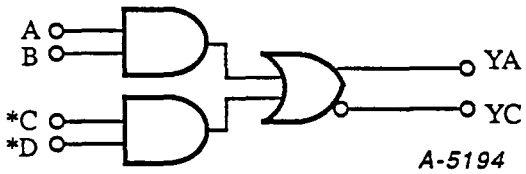
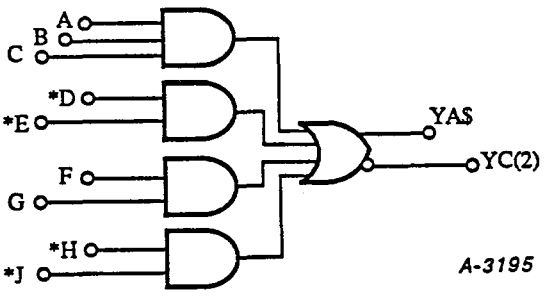
	EQUATION	CELL	SCHEMATIC
M 204	TWELVE INPUT AND/NAND EXPANDED BOOLEAN: YA = $\overline{ABCDEFGHJKLH}$ YC = $\overline{YA}$ MACRO BOOLEAN: YA = $\overline{ABCDEFGHJKLH}$ YC = $\overline{YA}$	FULL M	 A-5201
M 207	SIX INPUT AND/NAND EXPANDED BOOLEAN: YA = $\overline{ABCDEF}$ YC = $\overline{YA}$ MACRO BOOLEAN: YA = $\overline{ABCDEF}$ YC = $\overline{YA}$	1/4 M	 A-3194A
M 211	(2, 2) SUM OF PRODUCTS EXPANDED BOOLEAN: YA = $\overline{AB}$ + CD YC = $\overline{YA}$ MACRO BOOLEAN: YA = $\overline{AB}$ + CD YC = $\overline{YA}$	1/4 M	 A-5194
M 212	(3, 2, 2, 2) SUM OF PRODUCTS EXPANDED BOOLEAN: YA = $\overline{ABC}$ + DE + FG + HJ YC = $\overline{YA}$ MACRO BOOLEAN: YA = $\overline{ABC}$ + DE + FG + HJ YC = $\overline{YA}$	1/2 M	 A-3195

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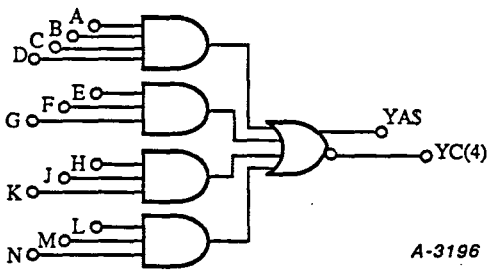
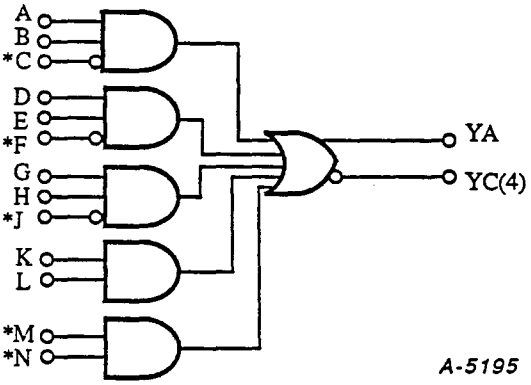
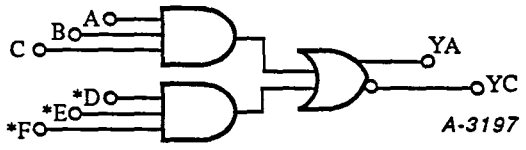
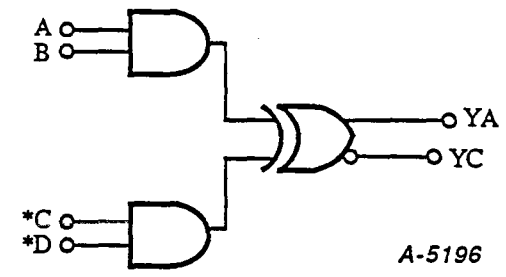
	EQUATION	CELL	SCHEMATIC
M 213	FULL M (4, 3, 3, 3) SUM OF PRODUCTS EXPANDED BOOLEAN: YA = $\underline{AB}$CD + EFG + HJK + LMN YC = $\overline{YA}$ MACRO BOOLEAN: YA = $\underline{AB}$CD + EFG + HJK + LMN YC = $\overline{YA}$		
M 215	FULL M (3, 3, 3, 2, 2) SUM OF PRODUCTS EXANDED BOOLEAN: YA = $\underline{AB\overline{C}}$ + $\underline{DE\overline{F}}$ + $\underline{GH\overline{J}}$ + KL + MN YC = $\overline{YA}$ MACRO BOOLEAN: YA = $\underline{AB\overline{C}}$ + $\underline{DE\overline{F}}$ + $\underline{GH\overline{J}}$ + KL + MN YC = $\overline{YA}$		
M 219	1/4 M (3, 3) SUM OF PRODUCTS EXPANDED BOOLEAN: YA = $\underline{AB}$C + DEF YC = $\overline{YA}$ MACRO BOOLEAN: YA = $\underline{AB}$C + DEF YC = $\overline{YA}$		
M 221	1/4 M (2, 2) XOR EXPANDED BOOLEAN: YA = $\underline{AB\overline{C}}$ + $\underline{AB\overline{D}}$ + $\underline{CD\overline{A}}$ + $\underline{CD\overline{B}}$ YC = $\overline{YA}$ MACRO BOOLEAN: YA = $\underline{AB}$\CD YD = $\overline{YA}$		

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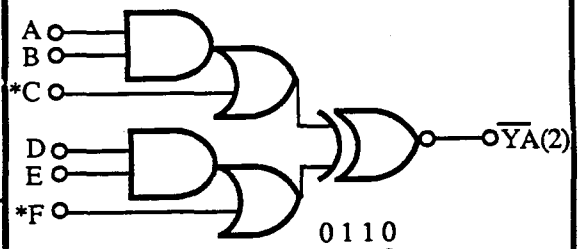
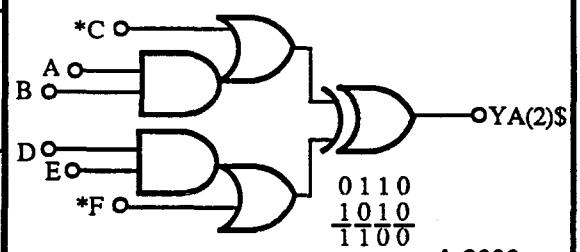
	EQUATION	CELL	SCHEMATIC
M 223	**FOUR INPUT XOR** EXPANDED BOOLEAN: $YA = A\bar{B}CD + \bar{A}BCD + A\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + AB\bar{C}D + AB\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D$ MACRO BOOLEAN: YA = A\B\C\D	1/2 M	 INPUT | OUTPUT 0 0 0 0 | 0 0 0 0 1 | 1 0 0 1 1 | 0 0 1 1 1 | 1 1 1 1 1 | 0 Note: Output goes high when an odd number of inputs are high. A-3198
M 224	**FOUR INPUT XNOR/ INVERTED XOR** EXPANDED BOOLEAN: $YA = \bar{A}\bar{B}CD + \bar{A}\bar{B}\bar{C}\bar{D} + ABCD + AB\bar{C}\bar{D} + A\bar{B}C\bar{D} + A\bar{B}\bar{C}D + \bar{A}BC\bar{D} + \bar{A}B\bar{C}D$ MACRO BOOLEAN: $YA = \overline{(A\backslash B\backslash C\backslash D)}$	1/2 M	 INPUT | OUTPUT 0 0 0 0 | 1 0 0 0 1 | 0 0 0 1 1 | 1 0 1 1 1 | 0 1 1 1 1 | 1 Note: Output goes low when an odd number of inputs are high. A-3199
M225	**(2, 1 - 2, 1) XNOR** EXPANDED BOOLEAN: $\overline{YA} = AB\bar{D}E + AB\bar{F} + C\bar{D}E + CF + \bar{A}\bar{C}F\bar{D} + \bar{B}\bar{C}F\bar{D} + \bar{A}C\bar{F}\bar{E} + \bar{B}C\bar{F}\bar{E}$ MACRO BOOLEAN: YA = (AB + C)\(DE + F) YA' = (AB + C)\(DE + F)'	1/2 M	 0 1 1 0 1 0 1 0 1 1 0 0 A-5197
M 226	**(2, 1 - 2, 1) XOR** EXPANDED BOOLEAN: $YA = C\overline{DEF} + AB\overline{DEF} + DE\overline{CAB} + F\overline{CAB}$ MACRO BOOLEAN: YA = (AB + C)\(DE + F)	1/2 M	 0 1 1 0 1 0 1 0 1 1 0 0 A-3200

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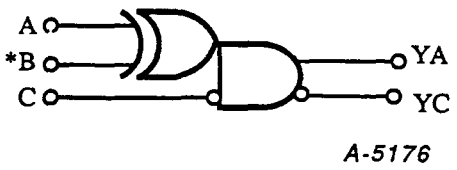
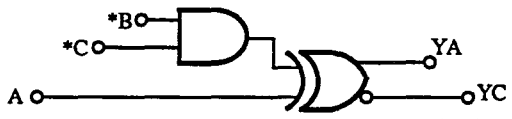
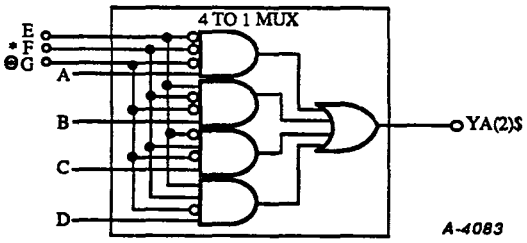
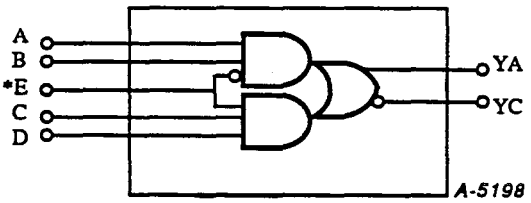
	EQUATION	CELL	SCHEMATIC
M 227	**(1, 1 - 1) XOR AND** EXPANDED BOOLEAN: YA = $A\overline{BC} + B\overline{AC}$ YC = $\overline{YA}$ MACRO BOOLEAN: YA = (A\B) $\overline{C}$ YC = $\overline{YA}$	1/2 M	 A-5176
M 228	**(1 - 2) XOR** EXPANDED BOOLEAN: YA = $A\overline{B} + A\overline{C} + \overline{A}BC$ YC = $\overline{YA}$ MACRO BOOLEAN: YA = A\BC YC = $\overline{YA}$	1/4 M	 A-3201
M 251	**4-TO-1 MULTIPLEXER WITH ENABLE** EXPANDED BOOLEAN: YA = $\overline{A}\overline{E}\overline{F}\overline{G} + B\overline{E}\overline{F}\overline{G} + C\overline{E}\overline{F}\overline{G} + DE\overline{F}\overline{G}$ MACRO BOOLEAN: 0 1 2 3 YA = MUX (A, B, C, D) : DCD (F, E) + $\overline{G}$	FULL M	 A-4083 LOGIC EQUIVALENTS
M 254	**2-TO-1 MULTIPLEXER** EXPANDED BOOLEAN: YA = $CDE + AB\overline{E}$ YC = $\overline{YA}$ MACRO BOOLEAN: 0 1 YA = MUX (AB, CD) : DCD (E) YC = $\overline{YA}$	1/4 M	 A-5198 LOGIC EQUIVALENTS

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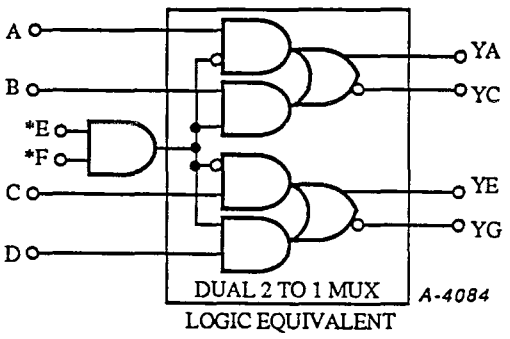
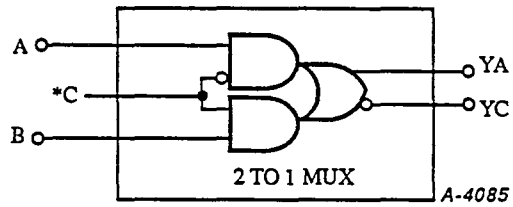
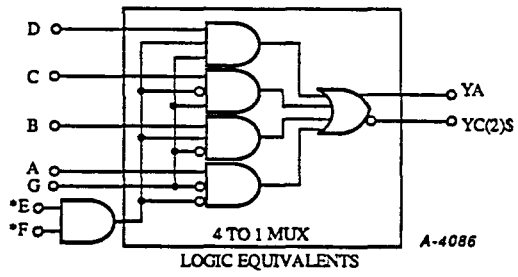
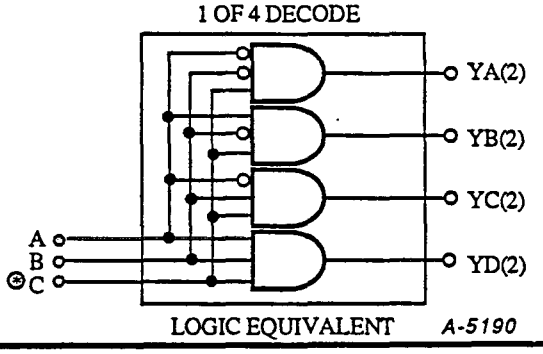
	EQUATION	CELL	SCHEMATIC
M 255	1/2 M **DUAL 2-TO-1 MULTIPLEXER** EXPANDED BOOLEAN: $YA = A\overline{EF} + BEF \quad YE = C\overline{EF} + DEF$ $YC = \overline{YA} \quad YG = \overline{YE}$ MACRO BOOLEAN: $YA = MUX\ (\overset{0}{A}, \overset{1}{B}) : DCD\ (EF)$ $YE = MUX\ (\overset{0}{C}, \overset{1}{D}) : DCD\ (EF)$ $YC = \overline{YA}$ $YG = \overline{YE}$		 LOGIC EQUIVALENT
M 256	1/4 M **2-TO -1 MULTIPLEXER** EXPANDED BOOLEAN: $YA = A\overline{C} + BC$ $YC = \overline{YA}$ MACRO BOOLEAN: $YA = MUX\ (\overset{0}{A}, \overset{1}{B}) : DCD\ (C)$ $YC = \overline{YA}$		 LOGIC EQUIVALENT
M 259	1/2 M **4-TO 1 MULTIPLEXER** EXPANDED BOOLEAN: $YA = A\overline{G}\overline{EF} + B\overline{G}EF + CG\overline{EF} + DGEF$ $YC = \overline{YA}$ MACRO BOOLEAN: $YA = MUX\ (\overset{0}{A}, \overset{1}{B}, \overset{2}{C}, \overset{3}{D}) : DCD\ (G, EF)$ $YC = \overline{YA}$		 LOGIC EQUIVALENTS
M 261	1/2 M **1 OF 4 DECODE WITH ENABLE** EXPANDED BOOLEAN: $YA = C\overline{AB}$, $YB = CA\overline{B}$, $YC = C\overline{AB}$ $YD = CAB$ MACRO BOOLEAN: $\overset{3}{YD}, \overset{2}{YC}, \overset{1}{YB}, \overset{0}{YA} = DCD\ (B, A)/C$		

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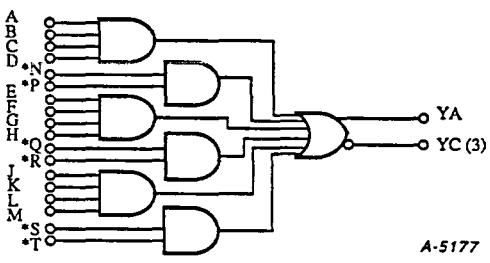
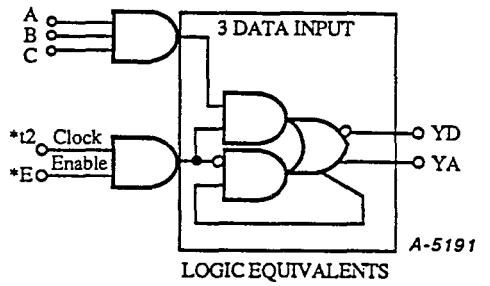
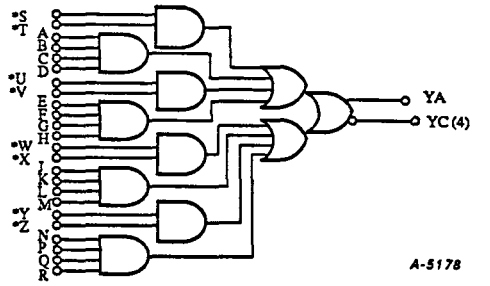
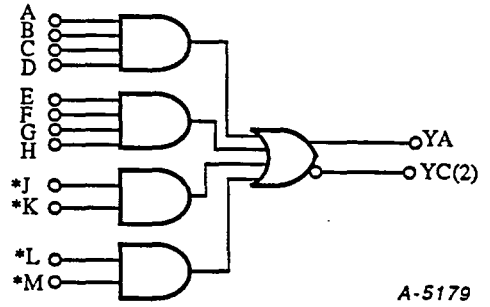
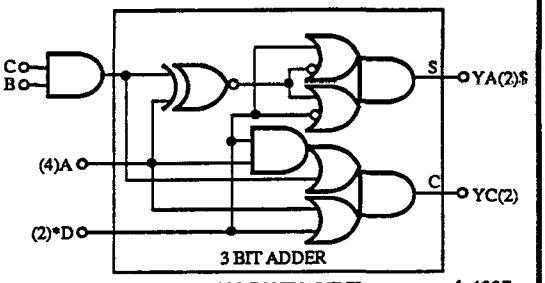
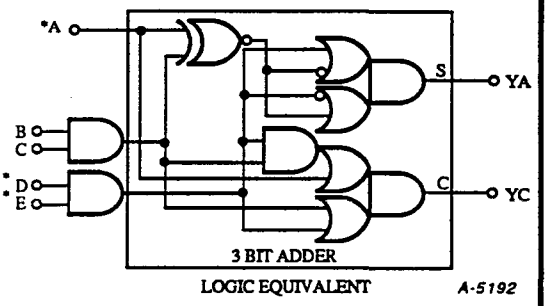
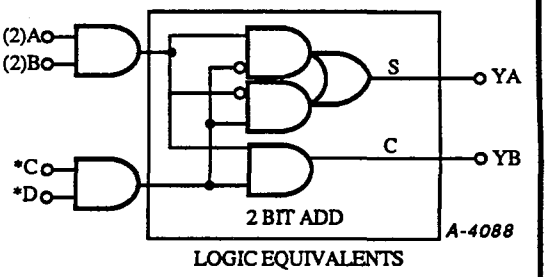
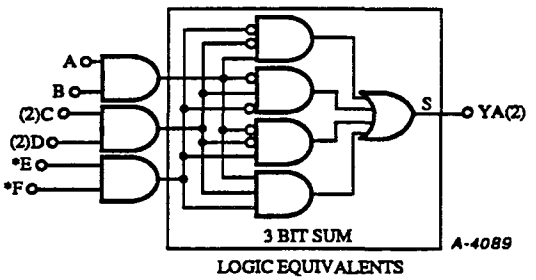
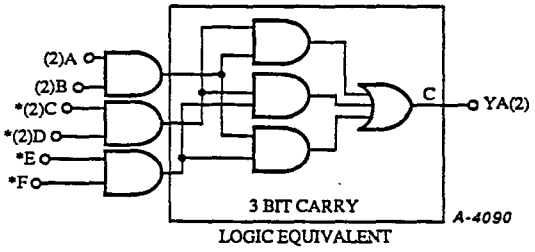
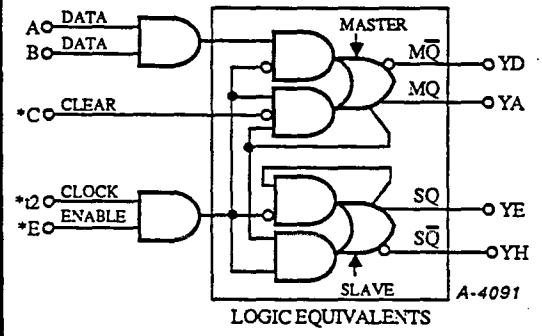
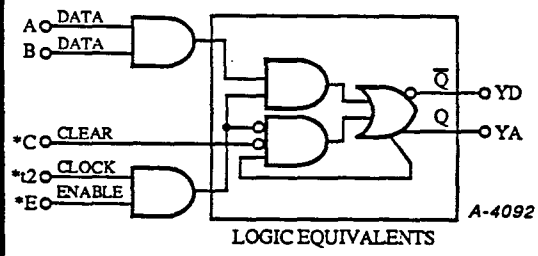
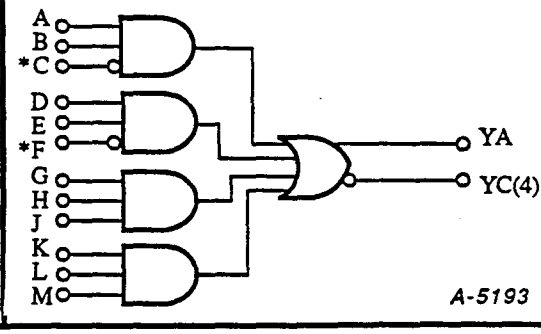
	EQUATION	CELL	SCHEMATIC
M 277	(4, 4, 4, 2, 2, 2) SUM OF PRODUCTS EXPANDED BOOLEAN: YA = ABCD + EFGH + JKLM + NP + QR + ST MACRO BOOLEAN: YA = $\overline{ABCD + EFGH + JKLM + NP + QR + ST}$ YC = $\overline{YA}$	3/4 M	
M 278	3 DATA INPUT D LATCH EXPANDED BOOLEAN: MACRO BOOLEAN: YA = ABC ; t2 E YD = $\overline{YA}$ Note: $\overline{YD}$, YA = DLY(ABC)	1/4 M	 LOGIC EQUIVALENTS
M 279	(4, 4, 4, 4, 2, 2, 2, 2) SUM OF PRODUCTS EXPANDED BOOLEAN: YA = ABCD + EFGH + JKLM + NPQR + ST + UV + WX + YZ YC = $\overline{YA}$ MACRO BOOLEAN: YA = ABCD + EFGH + JKLM + NPQR + ST + UV + WX + YZ YC = $\overline{YA}$	FULL M	
M 280	(4, 4, 2, 2) SUM OF PRODUCTS EXPANDED BOOLEAN: YA = ABCD + EFGH + JK + LM YC = $\overline{YA}$ MACRO BOOLEAN: YA = ABCD + EFGH + JK + LM YC = $\overline{YA}$	1/2 M	

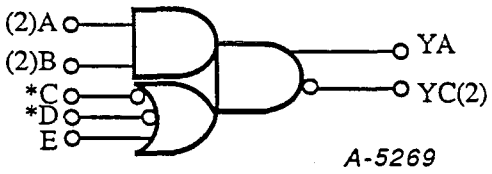
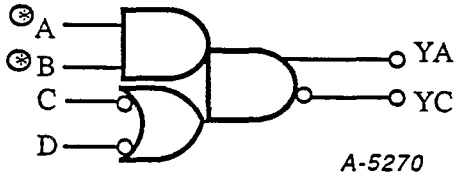
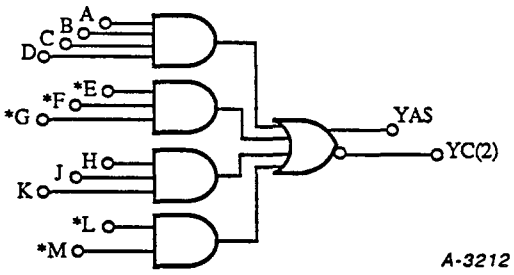
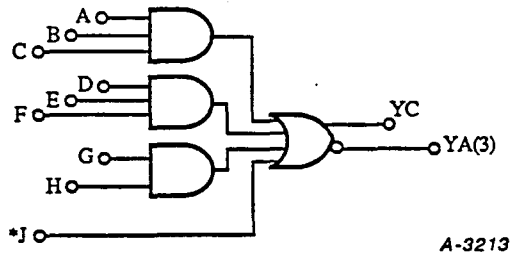
Hardware Trng. *J.E.S.*

	EQUATION	CELL	SCHEMATIC
M 281	**3 BIT ADDER SUM/CARRY** EXPANDED BOOLEAN: YA = ABCD + $\overline{A}\overline{B}\overline{C}$D + $\overline{A}$BC$\overline{D}$ + A$\overline{B}\overline{C}\overline{D}$ YC = ABC + BCD + AD + ABCD MACRO BOOLEAN: YA !YC = SCY (A, BC, D) YA = SUM (A, BC, D) YC = CARRY (A, BC, D)	FULL	
M282	**3 BIT ADDER SUM/CARRY** EXPANDED BOOLEAN: YA = $\overline{A}\overline{B}\overline{C}\overline{D}\overline{E}$ + $\overline{A}$BC$\overline{D}\overline{E}$ + $\overline{A}\overline{B}$CD$\overline{E}$ + ABCDE YC = ABC$\overline{D}\overline{E}$ + A$\overline{B}$CD$\overline{E}$ + $\overline{A}$BCD$\overline{E}$ + ABCDE MACRO BOOLEAN: YA !YC = SCY (A, BC, DE) YA = SUM (A, BC, DE) YC = CAR (A, BC, DE)	1/2 M	
M 284	**2 BIT ADDER/HALF ADD** EXPANDED BOOLEAN: YA = AB$\overline{C}$ + AB$\overline{D}$ + $\overline{A}$CD + $\overline{B}$CD YB = ABCD MACRO BOOLEAN: YA!YB = SCY (AB, CD) YA = SUM (AB, CD) YB = CAR (AB, CD)	1/4 M	
M 285	**3 BIT ADDER SUM** EXPANDED BOOLEAN: YA = AB$\overline{C}\overline{D}\overline{E}\overline{F}$ + $\overline{A}$BCD$\overline{E}\overline{F}$ + $\overline{A}\overline{B}$CD$\overline{E}\overline{F}$ + ABCDEF MACRO BOOLEAN: YA = SUM (AB, CD, EF)	1/2 M	

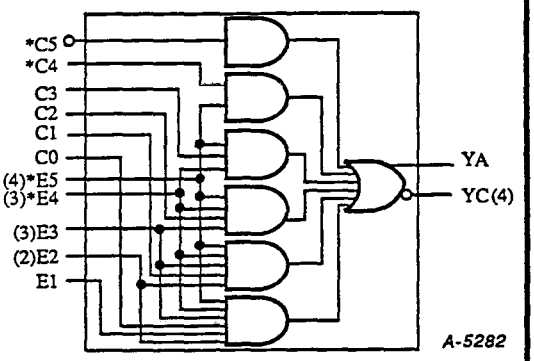
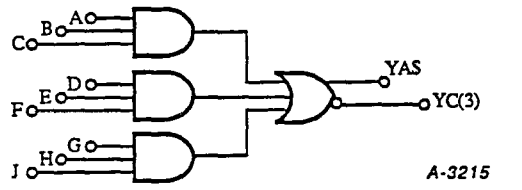
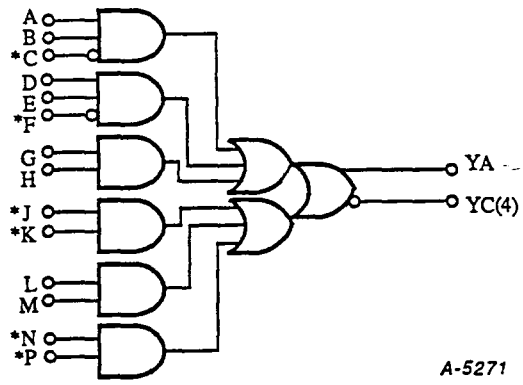
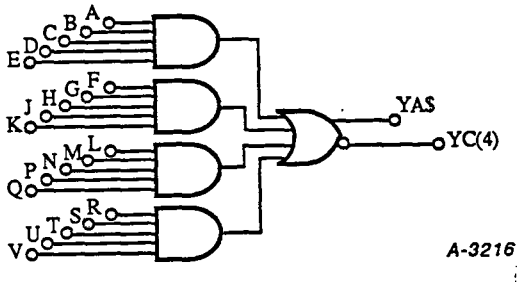
Hardware Trng. *J.E.S.*

	EQUATION	CELL	SCHEMATIC
M 286	3 BIT ADDER CARRY EXPANDED BOOLEAN: YA = ABCD + DCEF +ABEF MACRO BOOLEAN: YA = CAR (AB, CD, EF)	1/2 M	
M 291	D FLIP-FLOP WITH RESET (POSITIVE CLOCK) (MACRO FUNCTION: D LATCH-DELAY WITH SET) EXPANDED BOOLEAN: MACRO BOOLEAN: YD, YA; YH, YE = AB; t2 E + $\overline{C}$ YD = $\overline{YA}$ YH = $\overline{YE}$ NOTE: YE = DLY (YA)	1/2 M	
M 293	D LATCH WITH RESET (POSITIVE CLOCK) EXPANDED BOOLEAN: MACRO BOOLEAN: YA = AB; t2 E + $\overline{C}$ YD = $\overline{YA}$	1/4 M	
M311	EXPANDED BOOLEAN: YA = AB$\overline{C}$ + D$\overline{E}$F + GHJ + KLM YC = $\overline{YA}$ MACRO BOOLEAN: YA = AB$\overline{C}$ + D$\overline{E}$F + GHJ + KLM YC = $\overline{YA}$	FULL M	

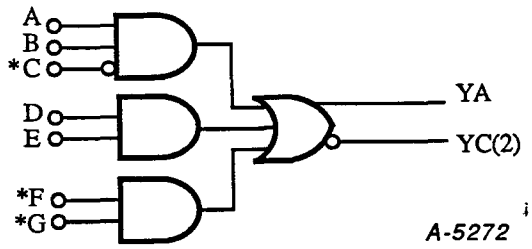
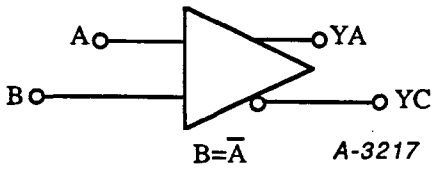
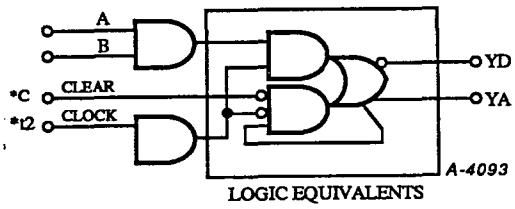
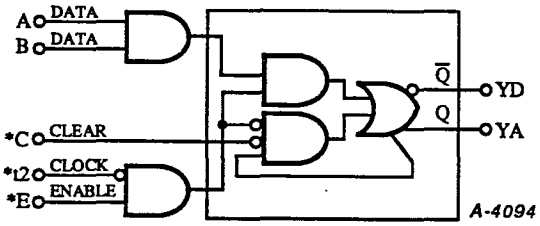
Hardware Trng. *J.E.S.*

	EQUATION	CELL	SCHEMATIC
M 312	(3, 3, 3) AND/OR EXPANDED BOOLEAN: YA = $\overline{ABC}$ + $\overline{ABD}$ + ABE YC = $\overline{YA}$ MACRO BOOLEAN: YA = AB ($\overline{C}$ + $\overline{D}$ + E) YC = $\overline{YA}$	1/2 M	 A-5269
M 313	(2, 2) SUM OF PRODUCTS EXPANDED BOOLEAN: YA = $\overline{ABC}$ + $\overline{ABD}$ YC = $\overline{YA}$ MACRO BOOLEAN: YA = $\overline{AB}$(CD)' YC = $\overline{YA}$	1/4 M	 A-5270
M 314	(4, 3, 3, 2) SUM OF PRODUCTS EXPANDED BOOLEAN: YA = $\overline{ABCD}$ + EFG + HJK + LM YC = $\overline{YA}$ MACRO BOOLEAN: YA = $\overline{ABCD}$ + EFG + HJK + LM YC = $\overline{YA}$	1/2 M	 A-3212
M 319	(3, 3, 2, 1) SUM OF PRODUCTS EXPANDED BOOLEAN: YC = $\overline{ABC}$ + DEF + GH + J YA = $\overline{YC}$ MACRO BOOLEAN: YC = $\overline{ABC}$ + DEF + GH + J YA = $\overline{YC}$	3/4 M	 A-3213

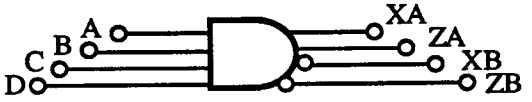
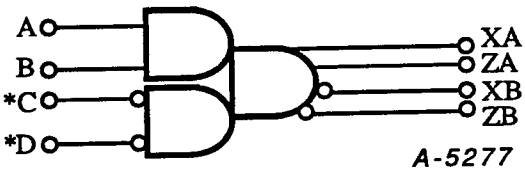
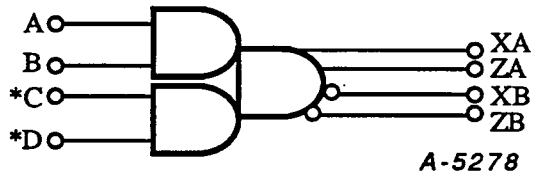
Hardware Trng. *J.E.S.*

	EQUATION	CELL	SCHEMATIC
M 321	(6, 6, 4, 4, 2, 2) SUM OF PRODUCTS (MACRO FUNCTION: PROPAGATE CARRY) EXPANDED BOOLEAN: PROPAGATE CARRY YA = C0 E1 E2 E3 E4 E5 + C1 E2 E3 E4 E5 + C2 E3 E4 E5 + C3 E4 $\overline{E5}$ + C4 E5 + C5 YC = $\overline{YA}$ MACRO BOOLEAN: YA = PCY (C5, C4, C3, C2, C1, C0, E5, E4 E3, E2, E1) YC = $\overline{YA}$	FULL M	
M 322	(3, 3, 3,) SUM OF PRODUCTS EXPANDED BOOLEAN: YA = $\overline{ABC}$ + DEF + GHJ YC = $\overline{YA}$ MACRO BOOLEAN: YA = $\overline{ABC}$ + DEF + GHJ YC = $\overline{YA}$	3/4 M	
M 323	(3, 3, 2, 2, 2, 2) SUM OF PRODUCTS EXPANDED BOOLEAN: YA = $\overline{ABC}$ + $\overline{DEF}$ + GH + JK + LM + NP YC = $\overline{YA}$ MACRO BOOLEAN: YA = $\overline{ABC}$ + $\overline{DEF}$ + GH + JK + LM + NP YC = YA	FULL M	
M 324	(5, 5, 5, 5) SUM OF PRODUCTS EXPANDED BOOLEAN: YA = $\overline{ABCDE}$ + FGHJK + LMNPQ + RSTUV YC = $\overline{YA}$ MACRO BOOLEAN: YA = $\overline{ABCDE}$ + FGHJK + LMNPQ + RSTUV YC = $\overline{YA}$	FULL M	

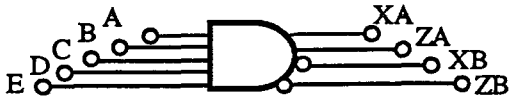
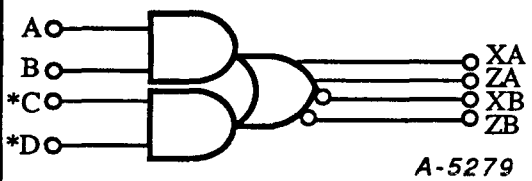
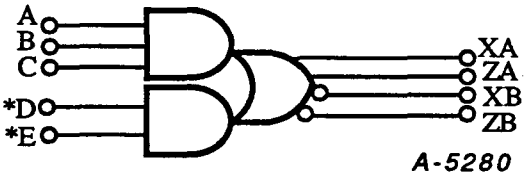
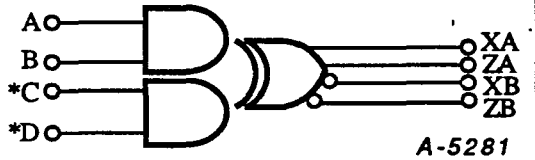
Hardware Trng. *J.E.S.*

	EQUATION	CELL	SCHEMATIC
M 331	EXPANDED BOOLEAN: YA = $AB\overline{C}$ + DE + FG YC = $\overline{YA}$ MACRO BOOLEAN: YA = $AB\overline{C}$ + DE + FG YC = $\overline{YA}$	1/2 M	
M 374	**DIFFERENTIAL FANOUT** EXPANDED BOOLEAN: YA = A YC = B NOTE: THIS IS A DIFFERENTIAL IN/ DIFFERENTIAL OUT BUFFER WITH A = $\overline{B}$ MACRO BOOLEAN: YA = DIF (A, B) NOTE: MACRO VALID IF A = $\overline{B}$ YC = $\overline{YA}$	1/4 M	
M 391	**D FLIP-FLOP WITH RESET (NEGATIVE CLOCK) (MACRO FUNCTION: D LATCH-DELAY WITH SET)** EXPANDED BOOLEAN: MACRO BOOLEAN: YA = AB; t2 + $\overline{C}$ YD = $\overline{YA}$ NOTE: YA = DLY(AB)	1/2 M	 LOGIC EQUIVALENTS
M 393	**D LATCH WITH RESET (NEGATIVE CLOCK)** EXPANDED BOOLEAN: MACRO BOOLEAN: YA = AB; t2 E + $\overline{C}$ YD = $\overline{YA}$ NOTE: YA = DLY(AB)	1/4 M	 LOGIC EQUIVALENTS

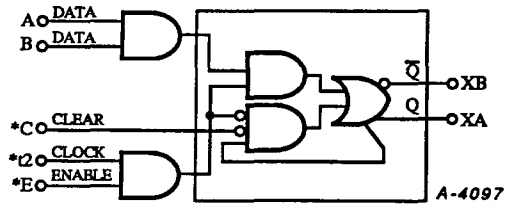
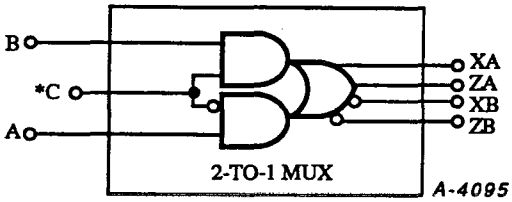
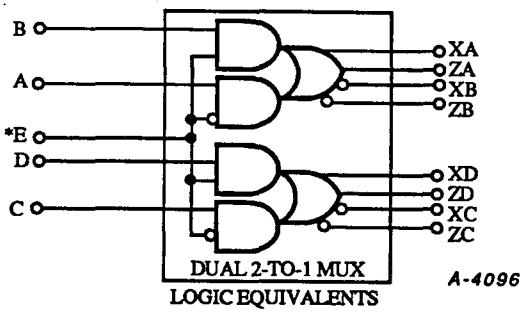
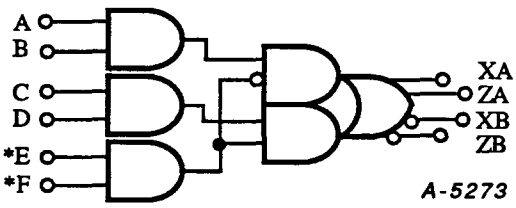
A-8417

	EQUATION	CELL	SCHEMATIC
	OUTPUT MACROS-X CELLS		OUTPUT CELLS ARE USED TO INTERFACE THE INTERNAL AND OUTSIDE LOGIC AND PROVIDE 60 OHM DRIVE CAPABILITY ON THE "X" OUTPUT.
X 201	**TWO INPUT AND/NAND** EXPANDED BOOLEAN: XA, ZA = AB XB, ZB = $\overline{XA}$, $\overline{ZA}$ MACRO BOOLEAN: XA, ZA = AB XB, ZB = $\overline{XA}$, $\overline{ZA}$	1 X	 A-3221
X 202	**FOUR INPUT AND/NAND** EXPANDED BOOLEAN: XA, ZA = ABCD XB, ZB = $\overline{XA}$, $\overline{ZA}$ MACRO BOOLEAN: XA, ZA = ABCD XB, ZB = $\overline{XA}$, $\overline{ZA}$	1 X	 A-3222
X 203	**(2, 2') INPUT AND/NAND** EXPANDED BOOLEAN: XA, ZA = AB$\overline{CD}$ XB, ZB = $\overline{XA}$, $\overline{ZA}$ MACRO BOOLEAN: XA, ZA = AB$\overline{CD}$ XB, ZB = $\overline{XA}$, $\overline{ZA}$	1 X	 A-5277
X 204	**(2, 2) INPUT AND/NAND** EXPANDED BOOLEAN: XA, ZA = ABCD XB, ZB = $\overline{XA}$, $\overline{ZA}$ MACRO BOOLEAN: XA, ZA = ABCD XB, ZB = $\overline{XA}$, $\overline{ZA}$	1 X	 A-5278

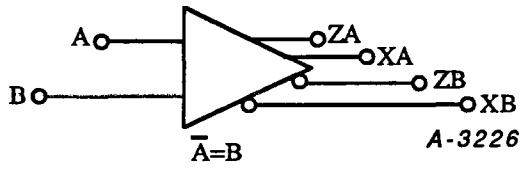
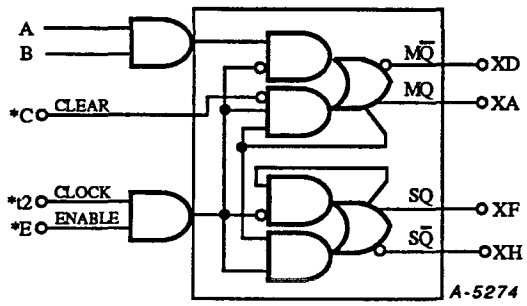
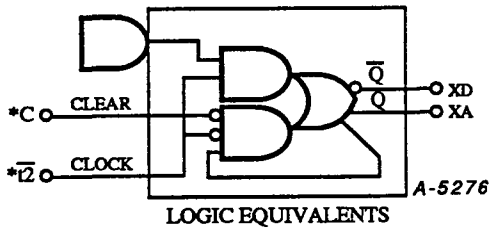
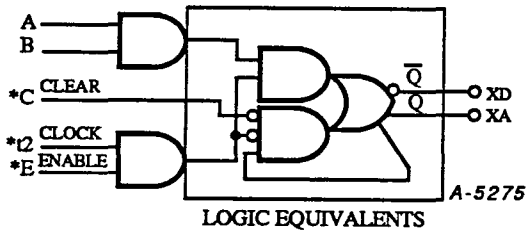
A-8012

	EQUATION	CELL	SCHEMATIC
X 205	**FIVE INPUT AND/NAND** EXPANDED BOOLEAN: XA, ZA = ABCDE XB, ZB = $\overline{XA}$, $\overline{ZA}$ MACRO BOOLEAN: XA, ZA = ABCDE XB, ZB = $\overline{XA}$, $\overline{ZA}$	1 X	 A-3223
X 211	**(2, 2) AND/OR** EXPANDED BOOLEAN: XA, ZA = AB + CD XB, ZB = $\overline{XA}$, $\overline{ZA}$ MACRO BOOLEAN: XA, ZA = AB + CD XB, ZB = $\overline{XA}$, $\overline{ZA}$	1 X	 A-5279
X 212	**(3, 2) AND/OR** EXPANDED BOOLEAN: XA, ZA = ABC + DE XB, ZB = $\overline{XA}$, $\overline{ZA}$ MACRO BOOLEAN: XA, ZA = ABC + DE XB, ZB = $\overline{XA}$, $\overline{ZA}$	1 X	 A-5280
X 221	**(2, 2) AND/XOR** EXPANDED BOOLEAN: XA, ZA = AB\CD XB, ZB = $\overline{XA}$, $\overline{ZA}$ MACRO BOOLEAN: XA, ZA = AB\CD XB, ZB = $\overline{XA}$, $\overline{ZA}$	1 X	 A-5281

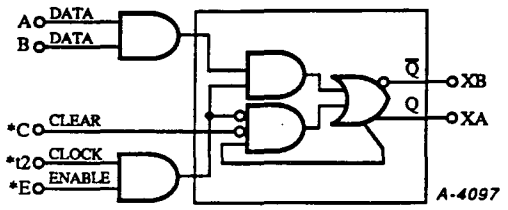
A-8013

	EQUATION	CELL	SCHEMATIC
X 227	**D LATCH WITH RESET (POSITIVE CLOCK)** EXPANDED BOOLEAN: MACRO BOOLEAN: XA = AB: t2 E + $\overline{C}$ XB = $\overline{XA}$	1 X	 LOGIC EQUIVALENTS D LATCH WITH RESET (POSITIVE CLOCK)
X 251	**2-TO-1 MULTIPLEXER** EXPANDED BOOLEAN: XA = A$\overline{C}$ + BC XB, ZB = $\overline{XA}$, $\overline{ZA}$ MACRO BOOLEAN: XA, ZA = MUX (A, B): DCD (C) XB, ZB = $\overline{XA}$, $\overline{ZA}$	1 X	 LOGIC EQUIVALENTS
X 252	**DUAL 2-TO-1 MULTIPLEXER** EXPANDED BOOLEAN: XA, ZA = $\overline{A}$E + BE XB, ZB = $\overline{XA}$, $\overline{ZA}$ XD, ZD = $\overline{C}$E + DE XC, ZC = $\overline{XD}$, $\overline{ZD}$ MACRO BOOLEAN: XA, ZA = MUX (A, B): DCD (E) XB, ZB = XA, ZA XD, ZD = MUX (C, D): DCD (E) XC, ZC = $\overline{XD}$, $\overline{ZD}$	2 X	 LOGIC EQUIVALENTS
X 254	**2-TO-1 MUX** EXPANDED BOOLEAN: XA, ZA = AB$\overline{EF}$ + CDEF XB, ZB = $\overline{XA}$, $\overline{ZA}$ MACRO BOOLEAN: XA, ZA = MUX (AB, CD): DCD (FF) XB, ZB = $\overline{XA}$, $\overline{ZA}$	1 X	

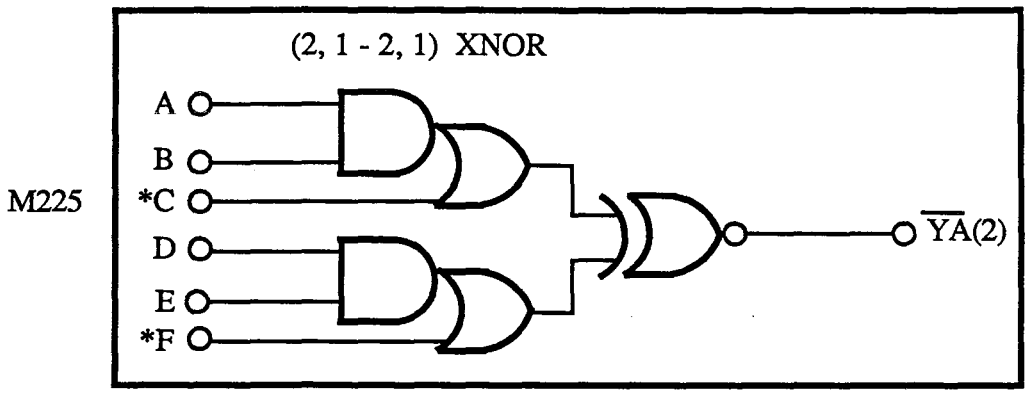
A-8014

EQUATION	CELL	SCHEMATIC
X 271	**DIFFERENTIAL FANOUT** 1 X EXPANDED BOOLEAN: XA, ZA = B XB, ZB = A NOTE: THIS IS A DIFFERENTIAL IN/ DIFFERENTIAL OUT BUFFER WITH A = $\overline{B}$ MACRO BOOLEAN: XA, ZA = DIFF (A, B) XB, ZB = $\overline{XA}$, $\overline{ZA}$ NOTE: MACRO VALID IF A = $\overline{B}$	
X 291	**D FLIP-FLOP WITH RESET (POSITIVE CLOCK)** 2 X EXPANDED BOOLEAN: MACRO BOOLEAN: XD, XA! XH XE = AB; t2 E + $\overline{C}$ XD = $\overline{XA}$ XH = $\overline{XE}$	
X 291	**D LATCH WITH RESET (NEGATIVE CLOCK)** 2 X EXPANDED BOOLEAN: MACRO BOOLEAN: XA = AB; $\overline{t2}$ + $\overline{C}$ XD = $\overline{XA}$	
X 292	**D LATCH WITH RESET (POSITIVE CLOCK)** 1 X EXPANDED BOOLEAN: MACRO BOOLEAN: XA = AB; t2 E + $\overline{C}$ XD = $\overline{XA}$	

A-8015

EQUATION	CELL	SCHEMATIC
X 377	1 X **D LATCH WITH RESET (POSITIVE CLOCK)** EXPANDED BOOLEAN: MACRO BOOLEAN: XA = AB; t2 E + $\overline{C}$ XB = $\overline{XA}$	 LOGIC EQUIVALENTS D LATCH WITH RESET (POSITIVE CLOCK)

Hardware Tmg. *J.E.S.*



LOGIC EQUIVALENTS

MACRO BOOLEAN:

$$YA' = [(AB + C)\backslash(DE + F)]' \text{ or } YA = (AB + C)\backslash(DE + F)$$

SAME AS

$$YA' = (AB + C)\backslash(DE + F)'$$

$$\underset{[X\backslash Y]'}{A} \quad \text{SAME AS} \quad \underset{X\backslash Y'}{B}$$

TRUTH TABLE:

X	Y		A	B
0	0	=	1	1
0	1	=	0	0
1	0	=	0	0
1	1	=	1	1

EXPANDED BOOLEAN: Multiply one side of the exclusive-or by the inverse of the other side, and vice versa.

$$\overline{YA} = ABDE + ABF + CDE + CF + \overline{A}\overline{C}\overline{F}\overline{D} + \overline{B}\overline{C}\overline{F}\overline{D} + \overline{A}\overline{C}\overline{F}\overline{E} + \overline{B}\overline{C}\overline{F}\overline{E}$$

$(DE + F)$ inverted is $(\overline{D} + \overline{E})(\overline{F})$

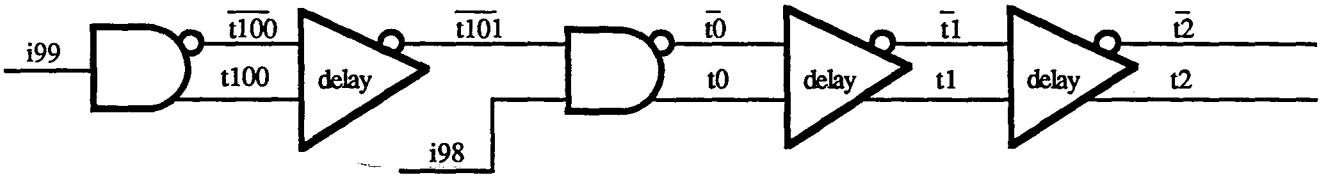
$(AB + C)$ inverted is $(\overline{A} + \overline{B})(\overline{C})$

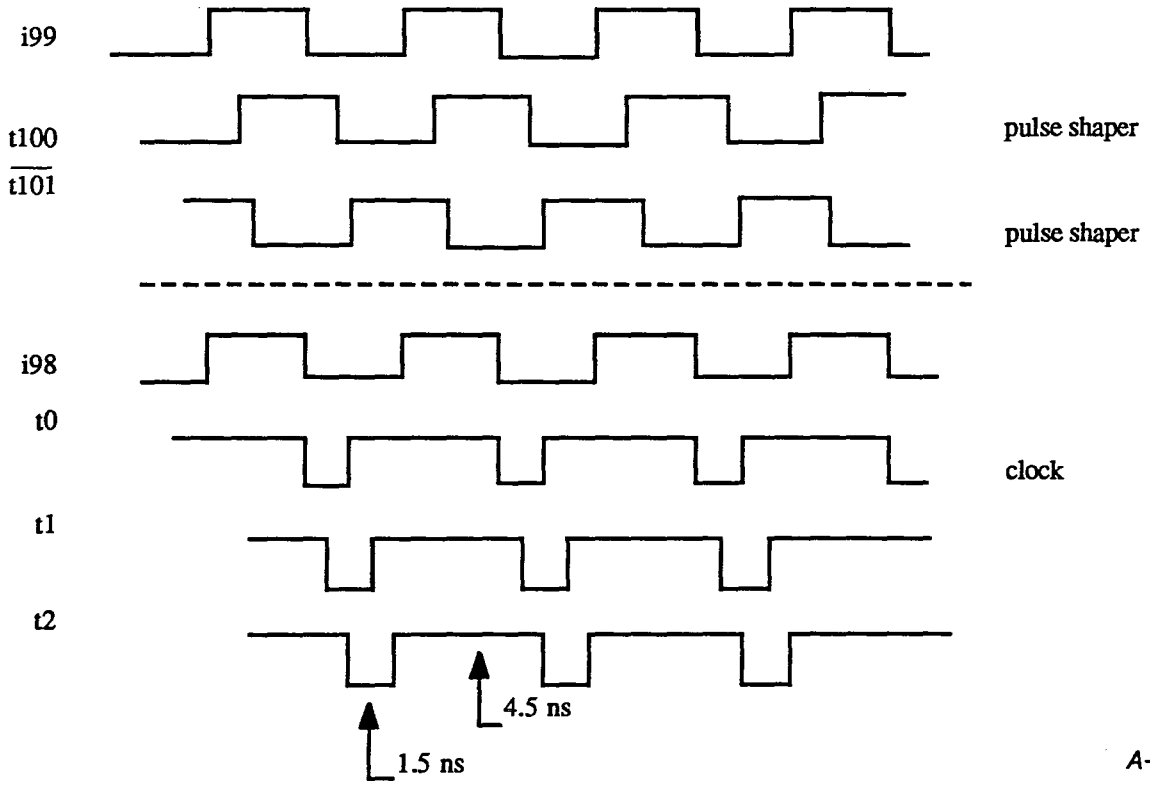
Hardware Trng.
A-7179 J.E.S.

CRAY Y-MP M225 MCA2500 MACROCELL

```
ts = 1/5   ----------------------------------------------------

m202     4     t0      = i98  t101'
m374     8     t1      = dif(t0, t0')          .clock
m374    32     t2      = dif(t1, t1')

m202           t100    = i99                   .pulse shape
m374           t101    = dif(t100, t100')      .pulse shape

ts = 0     ----------------------------------------------------
```

i98 - Raw Clock
i99 - Pulse Shaper
i99, i98 happen at the same time

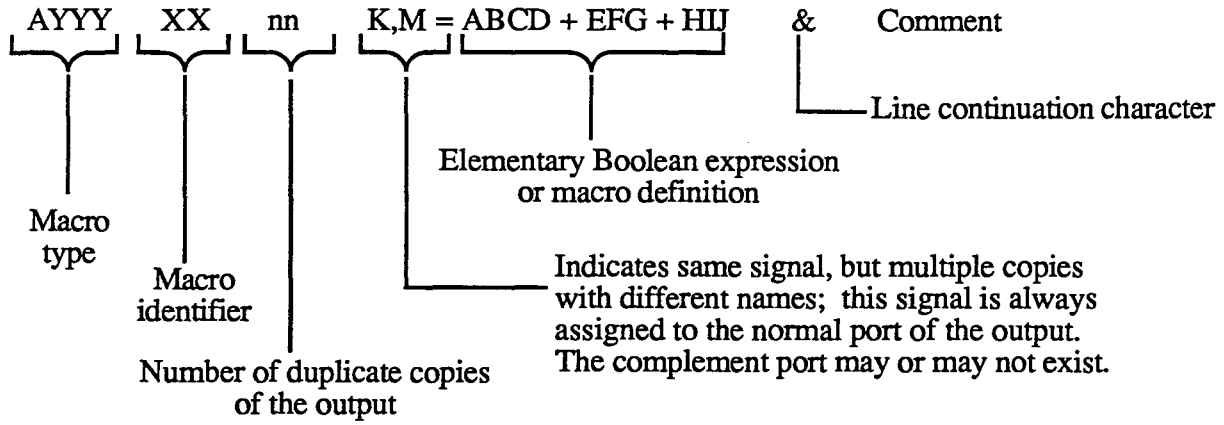




CRAY Y-MP CLOCK PULSE CIRCUIT

CELL ARRAY MACRO SCHEMATICS

General Format



Specific Rules

- Right hand side of equation may be macro definition of Boolean.
- The following format can be used with a group of equations to indicate that the group comes from one chip:

```
AYYY   G = CA
       I = DA
       K = EB   ──►  All generated on and/or by the same macro
       M = FB
```

- The explanation of the generated signal will be provided in the rightmost column (Comment). Including comments saves hours for all the CRI employees who may ever have need to study and understand the Boolean.
- The force"0" is constructed within each cell array by a force "0" generator and is used to set any input or product term to a logic "0".
  EXAMPLE: M212 K9 = ABC + DE + FG + 0#
  means K9 = ABC + DE + + FG
- Any unused input ports to a macro will be set to force "1" specified by "#" in the Boolean statement.
  EXAMPLE: M201 K = ABC#
  means input D of the M201 macro definition is set to force "1"
- Unused output ports of a macro will be left open or terminated according to the special rules described in layout section.

Hardware Trng.
YM17/19 J.E.S.

MACRO BOOLEAN CONSIDERATIONS

The Macro boolean reads very similar to the CRAY X-MP with some exceptions:

Time segments are layed out differently for the CPU board, than for the memory board, latch time is anywhere from (0/4 - 0/9). There are typically four macrocell times between latches.

Example:

Latch	ts	ts	ts	ts	Latch
ts 0/9	10/19	20/27	28/35	36/43	ts 0/9

The time segments for the memory board are latch time segment, ts 0, with four macrocell times between latches.

Example:

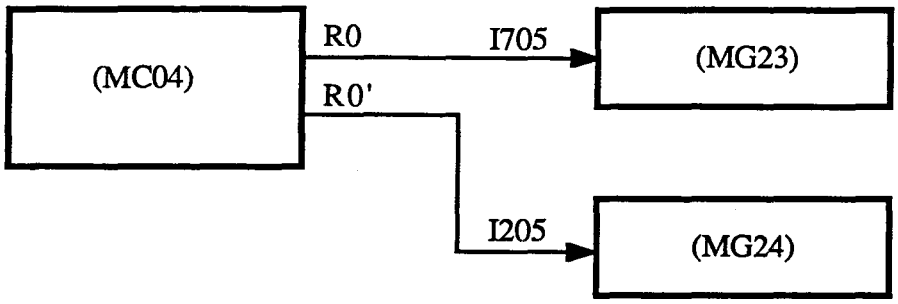
Latch	ts	ts	ts	ts	Latch
ts 0	1	2	3	4	ts 0

An option is the same name for a MCA2500 ECL chip.

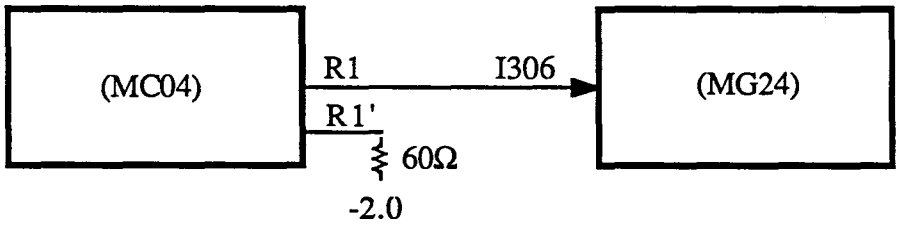
On rare occasions, not all outputs (R terms) have a complementary pair (true, false). A complementary pair must be used for VIA's on the module. The true R term can go to one option while the false R term can go to another option. The R terms are listed in the PC Loading Charts per each option.

Example:

On the (MC04) option, R0 goes to (MG23), while R0' goes to (MG24).



Here, only R1 is used, and it comes into the (MG24) as I306.



4 Lower case letters are used in the Macro Boolean, but some exceptions of upper case can also be found.

```
OPTION: YC
REV:    100
DATE:   12-07-86
TITLE:  MEMORY CHECK BYTE GENERATION (4 USED)


INPUTS:

I00-15  TS=47   LL=3.   16      Ai/EXCHANGE DATA          CP3     AR
I16-31  TS=39   LL=2.   16      B DATA                    CP5     HR
I32-47  TS=39   LL=2.   16      Vj/Si/T DATA              CP4,5   VB,C
I48-49  TS=39   LL=2.   2       I/O CHECK BYTE                    YQ
I50-61  TS=29   LL=1.   12 T/C  PARTIAL CHECK BYTE                YC
I62     TS=47   LL=3.   1  C    SELECT A DATA             (1-2)   J-
I63     TS=47   LL=3.   1  C    SELECT B DATA             (1-2)   J-
I64     TS=47   LL=3.   1  C    ENTER DATA STACK          (3-2)   Y-
I65     TS=27   LL=1.   1  C    PORT C CONFLICT DELAYED   (3-2)   YK
I66     TS=47   LL=3.   1  C    PORT D CONFLICT DELAYED   (3-2)   YK
I67-70  TS=47   LL=3.   4  C    PORT C SECTION ENABLES    (1-2)   YK
I71-74  TS=39   LL=2.   4       4-2 FANIN/FANOUT
I75-76  TS=39   LL=2.   2       Vk DATA MAINTENANCE CB            VB,C
I77-78  TS=39   LL=2.   2       I/O DATA MAINTENANCE CB           YQ
I79     TS=0    FORCE.  1  C    MAINTENANCE MODE
I80     TS=0    FORCE.  1  C    MAINTENANCE SELECT
I98-99  TS=0    CLOCK.  2  C    CLOCK

OUTPUTS:

R00-01  TS=20   LL=1.   4       SECTION 0 CHECK BYTE              EXT
R02-03  TS=20   LL=1.   4       SECTION 1 CHECK BYTE              EXT
R04-05  TS=20   LL=1.   4       SECTION 2 CHECK BYTE              EXT
R06-07  TS=20   LL=1.   4       SECTION 3 CHECK BYTE              EXT
R08-15  TS=20   LL=1.   16      PARTIAL CHECKBYTE                 YC
2 R16   TS=10   LL=0.   4       4-2 FANIN/FANOUT


.       TOTAL PINS 119 (83 INPUTS + 36 OUTPUTS)

eject

.Option Design Change History

.GARN 9-189A, DATED 03-16-87, INTRODUCES THIS OPTION.
.DCN 200 DATED 12-15-86 AT 15:00 IS INSTALLED IN IN THIS BOOLEAN
.DCN 222 DATED 02-26-87 AT 16:00 IS INSTALLED IN IN THIS BOOLEAN
.DCN 224 DATED 02-27-87 AT 12:30 IS INSTALLED IN IN THIS BOOLEAN
.DCN 236 DATED 03-18-87 AT 13:00 IS INSTALLED IN IN THIS BOOLEAN
.OPTION RELEASED - REV. 100


eject
TS = 20/47 ----------------------------------------------------------
```

```
M212    F10=I48 E14 U16'+E13 U16'+D14 E10                .PORT B GO REFERENCE
M219    F11=U16 D14'D10'+V7 V8 D11                       .       RELEASE

M314    F20=E30 E31 E23 U26'+C24 E23 U26'+I48 E24 U26'+D24 E20 .PORT C GO REF
M219    F21=U26 D24'D20'+V7 V8 D21                       .       RELEASE
M207    F22=E30 E31 C18 C25'S0'                          .       ENTER DATA VBT
M202    F23=E20 D20'                                     .       HOLD YF ADDRESS
M219    F24=D24'E24+D24 D20'H0                           .       HOLD DATA
M314    F25=E30 E31 E25+C24 E20+C25 C23'                 .       REFERENCE STK 0
        F26=E30 E31 E25 C24+C25 E20+C24 C23              .       REFERENCE STK 1

M313    G0=E40'S0'(I23 I29)'                             .GO PORT A      CP1
M202    G1'=I24                                          .GO PORT B
M313    G2=E40'(I25 J4')'                                .GO PORT C
M202    G3=I26                                           .B/T + SCALAR
        G4=I27                                           .G/S + SCALAR
        G5=I26 I27                                       .SCALAR REFERENCE
        G6=I28                                           .S READ
        G7'=I29                                          .EXCHANGE SEQUENCE
M256    G8=MUX(I30,P1):DCD(S0)                           .XA 4

TS = 0/6  ------------------------------------------------------------------

M291  2 H100',H0'=G5'I49;T2                      .SCALAR   CP2 + MASTER CLEAR
M293    H1=G3 G4';T2                             .B/T      CP2
M291    H2=G6 G5;T2                              .S READ   CP2
M293    H3=H2;T2 E0'                             .S READ   CP3
eject
TS = 0/6  ------------------------------------------------------------------

M291    J100,J0=G7;T2                            .EXCHANGE SEQUENCE
```

```
input:
        i0-8    ts=35    ll=3  .ss0 read data
        i10-18  ts=35    ll=3  .ss n+1
        i20-28  ts=35    ll=3  .ss n+2
        i30-38  ts=35    ll=3  .ss n+3
        i40-48  ts=35    ll=3  .ss n+4
        i50-58  ts=35    ll=3  .ss n+5
        i60-68  ts=35    ll=3  .ss n+6
        i70-78  ts=35    ll=3  .ss n+7
        i80     ts=45    ll=3  .fan-out
        i90-92  ts=45    ll=3  .ss select code
        i98-99  ts=0     clock

output:
        r0-8    ts=10    ll=0  .cpu n read data
        r10-17  ts=10    ll=0  .fan-out

eject

.Option Design Change History

.garn no. 9-132, dated 9/18/86, introduces this option.

eject

ts = 1/5 ------------------------------------------------------------

m202  4  t0'   = i98 t101'                          .clock
m374 12  t1    = dif(t0,t0')
m374 36  t2    = dif(t1,t1')

m202     t100  = i99                                .pulse shape
m374     t101  = dif(t100,t100')                    .

ts = 0 -------------------------------------------------------------

m291 2  a0-2    = i90-92   ; t2                     .ss select code

ts = 2 -------------------------------------------------------------

m261 2  b3,b2,b1,b0 = dcd(a2,a1)/#

ts = 4 -------------------------------------------------------------

m259    c0-8   =i30-38 b1 a0 +i20-28 b1 a0' +i10-18 b0 a0 +i0-8   b0 a0'
        c10-18 =i70-78 b3 a0 +i60-68 b3 a0' +i50-58 b2 a0 +i40-48 b2 a0'

ts = 0 -------------------------------------------------------------

x227    r0-8'   = c0-8' c10-18' ; t2                .cpu read data

x227    r10-17  =  i80 ; t2                         .fan-out
```

```
m259    e2      = mux( b2,b12,b22,b32):dcd(d1,d0)          .bk0 we
        e3      = mux(b42,b52,b62,b72):dcd(d1,d0)          .bk0
m259    e10     = mux( !0,b11,b21,b31):dcd(d11,d10)        .bk1 we
        e11     = mux(b41,b51,b61,b71):dcd(d11,d10)        .bk1
m259    e12     = mux( b2,b12,b22,b32):dcd(d11,d10)        .bk1 we
        e13     = mux(b42,b52,b62,b72):dcd(d11,d10)        .bk1
m259    e20     = mux( !0,b11,b21,b31):dcd(d21,d20)        .bk2 we
        e21     = mux(b41,b51,b61,b71):dcd(d21,d20)        .bk2
m259    e22     = mux( b2,b12,b22,b32):dcd(d21,d20)        .bk2 we
        e23     = mux(b42,b52,b62,b72):dcd(d21,d20)        .bk2
m259    e30     = mux( !0,b11,b21,b31):dcd(d31,d30)        .bk3 we
        e31     = mux(b41,b51,b61,b71):dcd(d31,d30)        .bk3
m259    e32     = mux( b2,b12,b22,b32):dcd(d31,d30)        .bk3 we
        e33     = mux(b42,b52,b62,b72):dcd(d31,d30)        .bk3
m259    e40     = mux( !0,b11,b21,b31):dcd(d41,d40)        .bk4 we
        e41     = mux(b41,b51,b61,b71):dcd(d41,d40)        .bk4
m259    e42     = mux( b2,b12,b22,b32):dcd(d41,d40)        .bk4 we
        e43     = mux(b42,b52,b62,b72):dcd(d41,d40)        .bk4
m259    e50     = mux( !0,b11,b21,b31):dcd(d51,d50)        .bk5 we
        e51     = mux(b41,b51,b61,b71):dcd(d51,d50)        .bk5
m259    e52     = mux( b2,b12,b22,b32):dcd(d51,d50)        .bk5 we
        e53     = mux(b42,b52,b62,b72):dcd(d51,d50)        .bk5
m259    e60     = mux( !0,b11,b21,b31):dcd(d61,d60)        .bk6 we
        e61     = mux(b41,b51,b61,b71):dcd(d61,d60)        .bk6
m259    e62     = mux( b2,b12,b22,b32):dcd(d61,d60)        .bk6 we
        e63     = mux(b42,b52,b62,b72):dcd(d61,d60)        .bk6
m259    e70     = mux( !0,b11,b21,b31):dcd(d71,d70)        .bk7 we
        e71     = mux(b41,b51,b61,b71):dcd(d71,d70)        .bk7
m259    e72     = mux( b2,b12,b22,b32):dcd(d71,d70)        .bk7 we
        e73     = mux(b42,b52,b62,b72):dcd(d71,d70)        .bk7

m202    e99     = d103 b1                                  .cpua-go-we

m261    e103,e102,e101,e100 = dcd(d101,d100)/d102'  .cpua bank decode
        e107,e106,e105,e104 = dcd(d101,d100)/d102   .   a  "     "

ts = 2 ------------------------5 qcells ----------------------9.2---

m322    f0      = e1  d2  e3  +e0  d2'  e2  +e99 e100 b2  .bk0 we
        f1      = e11 d12 e13 +e10 d12' e12 +e99 e101 b2  .bk1 we
        f2      = e21 d22 e23 +e20 d22' e22 +e99 e102 b2  .bk2 we
        f3      = e31 d32 e33 +e30 d32' e32 +e99 e103 b2  .bk3 we
        f4      = e41 d42 e43 +e40 d42' e42 +e99 e104 b2  .bk4 we
        f5      = e51 d52 e53 +e50 d52' e52 +e99 e105 b2  .bk5 we
        f6      = e61 d62 e63 +e60 d62' e62 +e99 e106 b2  .bk6 we
        f7      = e71 d72 e73 +e70 d72' e72 +e99 e107 b2  .bk7 we

ts = 0 ------------------------------------------------------------

m391    g0-7    = f0-7 ; t2                                .bk0-7 we cp1
        g10-17  = g0-7 i85 ; t2                            .bk0-7 we cp2

ts = 1 ------------------------------------------------------------

m202    h0-7'   = g0-7' g10-17'                            .bk0-7 we cp1-2


ts = 1  ----------------------29 qcells----------------------9.1---

m261    j3,j2,j1,j0 = dcd(d1,d0)/d2'            .bank0 go-cpu
```

```
m2B6    c41 = carry(a11 b04,a10 b05,a09 b06)   .sum bit n-29
m2B5    c42 =   sum(a08 b07,a07 b08,a06 b09)   .sum bit n-30
m2B6    c43 = carry(a08 b07,a07 b08,a06 b09)   .sum bit n-29
m2B5    c44 =   sum(a05 b10,a04 b11,a03 b12)   .sum bit n-30
m2B6    c45 = carry(a05 b10,a04 b11,a03 b12)   .sum bit n-29
m2B5    c46 =   sum(a02 b13,a01 b14,a00 b15)   .sum bit n-30
m2B6    c47 = carry(a02 b13,a01 b14,a00 b15)   .sum bit n-29
m202    c48 = a12 b03                          .sum bit n-30

eject
ts = 10/19 ------------------------------------------------------------

m2B5    c50 =   sum(a11 b05,a10 b06,a09 b07)   .sum bit n-29
m2B6    c51 = carry(a11 b05,a10 b06,a09 b07)   .sum bit n-28
m2B5    c52 =   sum(a08 b08,a07 b09,a06 b10)   .sum bit n-29
m2B6    c53 = carry(a08 b08,a07 b09,a06 b10)   .sum bit n-28
m2B5    c54 =   sum(a05 b11,a04 b12,a03 b13)   .sum bit n-29
m2B6    c55 = carry(a05 b11,a04 b12,a03 b13)   .sum bit n-28
m2B5    c56 =   sum(a02 b14,a01 b15,a00 b16)   .sum bit n-29
m2B6    c57 = carry(a02 b14,a01 b15,a00 b16)   .sum bit n-28
m202    c58 = a12 b04                          .sum bit n-29

m2B5    c60 =   sum(a11 b06,a10 b07,a09 b08)   .sum bit n-28
m2B6    c61 = carry(a11 b06,a10 b07,a09 b08)   .sum bit n-27
m2B5    c62 =   sum(a08 b09,a07 b10,a06 b11)   .sum bit n-28
m2B6    c63 = carry(a08 b09,a07 b10,a06 b11)   .sum bit n-27
m2B5    c64 =   sum(a05 b12,a04 b13,a03 b14)   .sum bit n-28
m2B6    c65 = carry(a05 b12,a04 b13,a03 b14)   .sum bit n-27
m2B5    c66 =   sum(a02 b15,a01 b16,a00 b17)   .sum bit n-28
m2B6    c67 = carry(a02 b15,a01 b16,a00 b17)   .sum bit n-27
m202    c68 = a12 b05                          .sum bit n-28

m2B5    c70 =   sum(a11 b07,a10 b08,a09 b09)   .sum bit n-27
m2B5    c71 =   sum(a08 b10,a07 b11,a06 b12)   .sum bit n-27
m2B5    c72 =   sum(a05 b13,a04 b14,a03 b15)   .sum bit n-27
m2B5    c73 =   sum(a02 b16,a01 b17,a00 b18)   .sum bit n-27
m202    c74 = a12 b06                          .sum bit n-27

eject
ts = 20/27 ------------------------------------------------------------

m281    d00 =   sum(c00,c01,c02)       .sum bit n-33
m281    d01 = carry(c00,c01,c02)       .sum bit n-32
m281    d02 =   sum(c03,c10,c12)       .sum bit n-33
m281    d03 = carry(c03,c10,c12)       .sum bit n-32
m281    d04 =   sum(c14,c16,c18)       .sum bit n-33
m281    d05 = carry(c14,c16,c18)       .sum bit n-32

m281    d10 =   sum(c11,c13,c15)       .sum bit n-32
m281    d11 = carry(c11,c13,c15)       .sum bit n-31
m281    d12 =   sum(c17,c20,c22)       .sum bit n-32
m281    d13 = carry(c17,c20,c22)       .sum bit n-31
m281    d14 =   sum(c24,c26,c28)       .sum bit n-32
m281    d15 = carry(c24,c26,c28)       .sum bit n-31

m281    d20 =   sum(c21,c23,c25)       .sum bit n-31
m281    d21 = carry(c21,c23,c25)       .sum bit n-30
m281    d22 =   sum(c27,c30,c32)       .sum bit n-31
m281    d23 = carry(c27,c30,c32)       .sum bit n-30
m281    d24 =   sum(c34,c36,c38)       .sum bit n-31
m281    d25 = carry(c34,c36,c38)       .sum bit n-30

m281    d30 =   sum(c31,c33,c35)       .sum bit n-30
```

```
m391    F3      = E3  D70' ;T2                  .SIGN BIT
X377    R22-10  = J22-10      ;T2               .EXP J+K
x377    R24-23  = J24-23      ;T2               .EXP J+K
x377    R26     = J26         ;T2               .EXP BORROW 52-48
x377    R27     = J27         ;T2               . "    "    57-53
x377    R28     = J28         ;T2               . "    "    62-58
M391    F50     = D50 D70' ;T2
m391    F60     =D60  ;T2
m391    F61     =D61 D70' ;T2

m391    F70     =D70;T2


TS = 10/17 ------------------------------------------------------

M284    F300    = F0
m284    F350    = F50
m284    F361-360= F61-60
m284    F370    = F70

TS = 20/27 ------------------------------------------------------

M284    F200    = F300
m284    F250    = F350
m284    F261-260= F361-360
m284    F270    = F370

TS = 18/23 ------------------------------------------------------

M228    F100'   = # \ F200
m228    F150'   = # \ F250
m228    F161-160' = # \ F261-260
m228    F170'   = # \ F270

TS = 0/7 --------------------------------------------------------
                                                .(CP=IN+3)
X377    R3      =F160 ;T2                       .STRONG ROUND TRUNCATE
x377    R4      =F161 ;T2                       .COMPLEMENT
x377    R5      = F150 ;T2                      .INTEGER
x377    R6      = F100  ;T2                     .UNDERFLOW
x377    R8      = F170  ;T2                     .GO ADDRESS MPLY
x377    R9'     = F170' F100' ;T2               .UNDERFLOW TO MH28
M391    G2      = F2  ;T2                       .RANGE ERROR
m391    G3      = F3  ;T2                       .SIGN BIT

                                                .CP=IN + 4
M391    H3-2    = G3-2 ; T2                     .SIGN, RANGE

TS = 9/15 -------------------------------------------------------

M228    H213-212' = # \ H3-2

TS = 18/23 ------------------------------------------------------

M228    H113-112' = # \ H213-212

TS = 27/33 ------------------------------------------------------

M228    H13-12' = # \ H113-112

TS = 0/7 --------------------------------------------------------
                                                .CP = IN + 5
X377    R7      =H12; T2                        .RANGE
x377    R25     =H13; T2                        . SIGN BIT
```

```
TS = 9/15 ------------------------------------------------------------

X201    R0      = A1 A0'                                    .CONSTANT A
      5 R1      = A1 A0                                     .CONSTANT B
        R2      = A0                                        .CONSTANT C

M203    B0      = A10' A11' A12' A13' A14' A15'             .EXPJ 5-0 =0
        B1      = A16' A17' A18' A19' A20' A21'             .EXPJ 11-6=0
        B2      = A22' A23' A24'                           .     14-12=0

        B4      = A30' A31' A32' A33' A34' A35'             .EXPK 5-0 =0
        B5      = A36' A37' A38' A39' A40' A41'             .EXPK 11-6=0
        B6      = A42' A43' A44'                           .     14-12=0

M219    B7      = A23 A24 + A43 A44                        .OPERAND UNDEFINED
M226    B8      = A25 \ A45                                .SIGN BIT

M228 2  B23-11  = A23-11 \ A43-31                          .ENABLE EXP J+K
        B10     = A10 \ A30                                .
        B24     = A24 \ A44                                .
        B43-30  = A23-10   A43-30                          .CARRY EXP J+K
TS = 18/23 -----------------------------------------------------------

M200    C0      = B0 B1 B2                                 .EXPJ=0
        C1      = B4 B5 B6                                 .EXPK=0
M202    C2      = B7                                       .OPERAND UNDEFINED
M202    C3      = B8                                       .SIGN BIT


M219    C10     = B31 + B30 B11                            .CARRY 1-0
M212    C11     = B30 B11 B12 + B31 B12 + B32              .      2-0
M213    C12     = B30 B11 B12 B13 +B32 B13 + B31 B12 B13 &.    3-0
                  B33
M321    C13     = PCARRY(B34,B33,B32,B31,B30,0  ,B14,B13,B12,B11,#  )
                                                           .C13=CARRY 4-0
      2 C14     = PCARRY(B35,B34,B33,B32,B31,B30,B15,B14,B13,B12,B11)
                                                           .C14=CARRY 5-0
M213    C15     = B36 B17 B18 B19 + B37 B18 B19 + &        .CARRY 9-6
                  B39 + B38 B19
M321    C16     = PCARRY(B41,B40,B39,B38,B37,B36,B21,B20,B19,B18,B17)
                                                           .C16=CARRY 11-6

M201    C20     = B19 B18 B17 B16                          .ENABLE 9-6
M203    C21     = B21 B20 B19 B18 B17 B16                  .ENABLE 11-6

TS = 26/32 -----------------------------------------------------------
M219    C30     = B36 + C14 B16                            .CARRY 6-0
M212    C31     = C14 B16 B17 + B36 B17 + B37              .      7-0
M213    C32     = C14 B16 B17 B18 + B36 B17 B18 + &        .      8-0
                  B38 + B37 B18
M219    C33     = C15 + C14 C20                            .      9-0
M212    C34     = C14 C20 B20 +C15 B20 + B40               .      10-0
M219    C35     = C16 + C14 C21                            .      11-0
M212    C36     = C14 C21 B22 +C16 B22 + B42               .      12-0
M213    C37     = C14 C21 B22 B23 + C16 B22 B23 + &        .      13-0
                  B43 + B42 B23

M202    C124-111= B24-11
HTV-0834 C130   = B30
```

```
inputs:

        i00-23    ts=40   .ll=3  J operand bits 24 to 47  (cp2) (false)
        i30-53    ts=40   .ll=3  K operand bits 24 to 47  (cp2) (false)
        i60       ts=40   .ll=3  signs unequal            (cp2) (true)
        i61-62    ts=39   .ll=3  section carry            (cp3) (t/f)
        i63       ts=31   .ll=2  section enable           (cp3) (true)
        i98-99    ts=00   .clock


outputs:

        r00-23    ts=28   .ll=2  final sum bits 24 to 47  (cp4)
        r24       ts=35   .ll=3  section carry            (cp3)
        r25       ts=27   .ll=2  section enable           (cp3)
        r26       ts=26   .ll=2  sum bits 24 to 31 = 00   (cp4)
        r27       ts=26   .ll=2  sum bits 32 to 39 = 00   (cp4)
        r28       ts=26   .ll=2  sum bits 40 to 47 = 00   (cp4)
        r29       ts=28   .ll=2  sum bits 24 to 47 = 00   (cp4)
        -30       ts=25   .ll=2  sum bit 24               (cp3)
```

```
m293   "a00' = i00; t2          .J operand bit n+00
m293   "a01' = i01; t2          .J operand bit n+01
m293   "a02' = i02; t2          .J operand bit n+02
m293   "a03' = i03; t2          .J operand bit n+03
m293   "a04' = i04; t2          .J operand bit n+04
m293   "a05' = i05; t2          .J operand bit n+05
m293   "a06' = i06; t2          .J operand bit n+06
m293   "a07' = i07; t2          .J operand bit n+07
m293   "a08' = i08; t2          .J operand bit n+08
m293   "a09' = i09; t2          .J operand bit n+09
m293   "a10' = i10; t2          .J operand bit n+10
m293   "a11' = i11; t2          .J operand bit n+11
m293   "a12' = i12; t2          .J operand bit n+12
m293   "a13' = i13; t2          .J operand bit n+13
m293   "a14' = i14; t2          .J operand bit n+14
m293   "a15' = i15; t2          .J operand bit n+15
m293   "a16' = i16; t2          .J operand bit n+16
m293   "a17' = i17; t2          .J operand bit n+17
m293   "a18' = i18; t2          .J operand bit n+18
m293   "a19' = i19; t2          .J operand bit n+19
m293   "a20' = i20; t2          .J operand bit n+20
m293   "a21' = i21; t2          .J operand bit n+21
m293   "a22' = i22; t2          .J operand bit n+22
m293   "a23' = i23; t2          .J operand bit n+23
```

```
      2  d42     = i46  ; t2                    .    4
      3  d50-51  = i54-55;t2                    .    5
      2  d52     = i56  ; t2                    .    5
      3  d60-61  = i64-65;t2                    .    6
      2  d62     = i66  ; t2                    .    6
      3  d70-71  = i74-75;t2                    .    7
      2  d72     = i76  ; t2                    .    7

ts = 1    ----------------------96 qcells----------------------9.1---

m259    e0-2   = mux(b0-2  , b10-12, b20-22, b30-32):dcd(d1,d0).bk0 addr
        e3-5   = mux(b40-42, b50-52, b60-62, b70-72):dcd(d1,d0).bk0 addr
m259    e10-12 = mux(b0-2  , b10-12, b20-22, b30-32):dcd(d11,d10).bk1 addr
        e13-15 = mux(b40-42, b50-52, b60-62, b70-72):dcd(d11,d10).bk1 addr
m259    e20-22'= mux(b0-2', b10-12', b20-22', b30-32'):dcd(d21,d20).bk2 addr
        e23-25'= mux(b40-42',b50-52',b60-62',b70-72'):dcd(d21,d20).bk2 addr
m259    e30-32'= mux(b0-2',b10-12', b20-22', b30-32'):dcd(d31,d30).bk3 addr
        e33-35'= mux(b40-42',b50-52',b60-62', b70-72'):dcd(d31,d30).bk3 addr
m259    e40-42 =mux(b0-2   ,b10-12 ,b20-22 ,b30-32 ):dcd(d41,d40).bk4 addr
        e43-45 =mux(b40-42 ,b50-52 ,b60-62 ,b70-72 ):dcd(d41,d40).bk4 addr
m259    e50-52 =mux(b0-2   ,b10-12 ,b20-22 ,b30-32 ):dcd(d51,d50).bk5 addr
        e53-55 =mux(b40-42 ,b50-52 ,b60-62 ,b70-72 ):dcd(d51,d50).bk5 addr
m259    e60-62'=mux(b0-2'  ,b10-12',b20-22',b30-32'):dcd(d61,d60).bk6 addr
        e63-65'=mux(b40-42',b50-52',b60-62',b70-72'):dcd(d61,d60).bk6 addr
m259    e70-72'=mux(b0-2'  ,b10-12',b20-22',b30-32'):dcd(d71,d70).bk7 addr
        e73-75'=mux(b40-42',b50-52',b60-62',b70-72'):dcd(d71,d70).bk7 addr

m202    e102    = d2
        e112    = d12
        e122    = d22
        e132    = d32
        e142    = d42
        e152    = d52
        e162    = d62
        e172    = d72

ts = 2   ----------------------24 xcells----------------------9.2---

x251    r0      = mux(e0, e3)        :dcd(e102)        .bank0 addr
x254    r1      = mux(e1  e2', e4  e5'):dcd(e102)      .    0 cs-0
        r2      = mux(e1' e2', e4' e5'):dcd(e102)      .    0 cs-1

x251    r3      = mux(e10, e13)       :dcd(e112)       .bank1 addr
x254    r4      = mux(e11  e12', e14  e15'):dcd(e112)  .    1 cs-0
        r5      = mux(e11' e12', e14' e15'):dcd(e112)  .    1 cs-1

x251    r6      = mux(e20, e23)       :dcd(e122)       .bank2 addr
x254    r7      = mux(e21  e22', e24  e25'):dcd(e122)  .    2 cs-0
        r8      = mux(e21' e22', e24' e25'):dcd(e122)  .    2 cs-1

x251    r9      = mux(e30, e33)       :dcd(e132)       .bank3 addr
x254    r10     = mux(e31  e32', e34  e35'):dcd(e132)  .    3 cs-0
        r11     = mux(e31' e32', e34' e35'):dcd(e132)  .    3 cs-1

x251    r12     = mux(e40, e43)       :dcd(e142)       .bank4 addr
x254    r13     = mux(e41  e42', e44  e45'):dcd(e142)  .    4 cs-0
        r14     = mux(e41' e42', e44' e45'):dcd(e142)  .    4 cs-1

x251    r15     = mux(e50, e53)       :dcd(e152)       .bank5 addr
x254    r16     = mux(e51  e52', e54  e55'):dcd(e152)  .    5 cs-0
```

```
eject
TS = 0/6 ----------------------------------------------------------------

M293    X0-6'=I7-13;T2 Y3                .BREAKPOINT REGISTER

M291    X110',X10'=I95;T2                .CONTROL DUMP
        X11'=X10';T2
        X12=Y5;T2                        .WAIT FOR FETCHES
        X13=U12;T2                       .FOUR FETCHES COMPLETE

TS = 10/47 ---------------------------------------------------------------

M279    Y0'=C100 X0'+C100'X0+C101 X1'+C101'X1+C102 X2'+C102'X2+C103 X3'+C103'X3
M277    Y1'=C104 X4'+C104'X4+C105 X5'+C105'X5+C106 X6'+C106'X6
M393    Y2'=DLY(R36')                    .ENTER BREAKPOINT
M202  2 Y3'=Y2'
M211    Y4'=X10'+X11                     .BEGIN CONTROL DUMP
M219    Y5=Y4+X12 X13'J10'               .WAIT FOR FETCHES

M207    Y10=I96 F0 F3'F1'F8 Z0           .005(i2) ENTER BREAKPOINT
M202    Y11=Y2 Z0'                       .HOLD PATH

TS = 30/37 ---------------------------------------------------------------

M201 12 Z0=I90 I91 I92 I93               .ISSUE


TS = 0/7 -----------------------------------------------------------------

X227    R0-6=B0-6 B10-16;T2              .P REGISTER

TS = 10/17 ---------------------------------------------------------------

X212    R07'=H20 H2'H3'+ H10           .BRANCH IN CIP
X201    R08,Z8=H10 H109'                 .ENTER LIP 01
        R09=H11 H109'                    .ENTER LIP 1
```

```
        K4=I34 I35;T2                       .S0=0
        K5=I36;T2                           .S0 SIGN BIT

TS = 10/17 ------------------------------------------------------------------

M277    L0'=K0'H4+K1'H4+K0 K1 H5+K2 H6+K2'H7+H2'        .GO A0 BRANCH
        L1'=K3'H4+K4'H4+K3 K4 H5+K5 H6+K5'H7+H3'        .GO S0 BRANCH
M202    L2-3=H0-1                                       .005,006-007
        L4=J100                                         .ENTER EXCHANGE P
M212    L5=H1+X110+J110                                 .006-007 + CD + M.C.
M202    L6'=H20 J100'
eject
TS = 0/6 --------------------------------------------------------------------

M291    M100-104,M0-4=B2-6 W0-4;T2      .IB READ ADDRESS
        M105-106,M5-6=V7-8;T2           .IB READ BUFFER
M278  4 M7'=V0'V1 I41;T2                .ENABLE READ
      2 M8=V2'V4'V5;T2                  .GO READ IB 0
      2 M9=V3'V4'V6;T2                  .GO READ IB 1

M291    M110,M10=V2 V4';T2              .IB0 READOUT VALID
        M111,M11=V3 V4';T2              .IB1 READOUT VALID


M291    N100-104,N0-4=W10-14;T2         .IB WRITE ADDRESS
        N105-106,N5-6=U8-9;T2           .IB FETCH BUFFER
      2 N7=I41;T2                       .FETCH ACTIVE
M293  2 N8=I42;T2                       .GO WRITE
        N9=U3;T2                        .FETCH END AROUND
M291    N10=N7;T2                       .FETCH ACTIVE DELAYED

M293    N11-16'=N1-6';T2                .WRITE ADDRESS DELAYED
M291    N20-24=W20-24;T2                .FETCH STARTING ADDRESS
```

```
TS = 10/17 ------------------------------------------------------------
-
M221    F0-1=E2-3'E0-1'\E2-3'E10                        .BIT ENABLE
        F2-3=E2-3 E0-1 \E2-3 E10                        .BIT CARRY
        F4-5=E12' E0-1'\E12' E10                        .Sk FOR 050,051
M202    F6'=K13'K14'                                    .SELECT T OR Si TO MEM
        F7=E32
TS = 20/27 ------------------------------------------------------------
-
M254    G0-1=MUX(F2-3,F0-1'F2-3'):DCD(E11)              .S LOGICAL
        G2-3'=MUX(C20-21'E10',C22-23'E10'):DCD(S3)      .Si FOR 050
X204    #,G4= # # F0'F2'                                .SUM 0 CP3
X221    #,G5=F2\F1'F3'                                  .    1
X201    #,G6-7=E30-31
TS = 32/38 ------------------------------------------------------------
-
M254    H0-1=MUX(I10-11 V2,I8-9 V2):DCD(S4')            .Ak,CON,VM + ST,SM,RT
M314    H2-3=G2-3 F4-5 V3 S4+G0-1 V3 S4+I16-17 V3 S4'   .T + LOG
M254    H4-5=MUX(I14-15 V4,I13-14 V4):DCD(F7)           .SHIFT
M225    H6=(I18+V5')\(G6+V5')'                          .S ADD CP5
        H7=(I18 G6+V5')\(G7+V5')'
M254    H8-9=MUX(I16-17 K13,E2-3):DCD(K14)              .T OR Si TO MEM

@       H10-11=H0-1'H2-3'
        H12-13=H4-5'H6-7

TS = 40/47 ------------------------------------------------------------
-
X201    #,J0-1=G4-5                                     .SUM CP3
```

```
TS = 20/27 ------------------------------------------------------------------
M202    D0=Z8 H8                                .ADVANCE P BY 2
M211    D1=Z8 H8+C0
M207    D3= # # C1 C2                           .ENABLES
        D4= # # C1 C2 C3
        D5= # # C1 C2 C3 C4
        D6= # C5 C1 C2 C3 C4
        D7= # C6 C2 C3 C4 C5
eject
TS = 30/37 ------------------------------------------------------------------
M221    E0=I17 D0'\C0                           .P+1 OR P+2
        E1=I17 D1'\C1'
M226    E2=(I17 D1'+C1')\(Z999+C2')
M225    E2'=(I17 D1'+C1')\(Z999+C2')'
        E3-6'=(I17 D1'+D3-6')\(Z999+C3-6')'

M202    E10'=I15 I16                            .TWO + THREE PARCEL IN NIP
        E11'=I17                                .THREE PARCEL IN NIP
M212    E12'=I17 C0'+C1'+D7'Q0'                 .NEXT WORD INVALID
        E13'=I17 C0'+C1'+D7'                    .BUFFER BOUNDARY
M202    E14=Q1                                  .CURRENT IB WORD VALID

M202    F0'=I15                                 .NIP 005-007,01X   BRANCH
        F1-3'=I20-22                            .    h1,h2,g0
M261    F4,F5,F6,F7=DCD(I20,I19)                .    DECODE h1,h0
M202    F8'=I18                                 .    i2

TS = 40/47 ------------------------------------------------------------------
M207    G0=F0 F3'F1'F8'Z0                       .005(i2)'
```

1 LOCATION 01 CRAY Y-MP WIRE TABS S/N 1001 01-08-88 PAGE 1

SOURCE TERM	PIN	TS	DESTINATION LOC	TERM	PIN	TS	LEN	DESCRIPTION
00-I000	zaf25	43	<- 01	10-R003	zab01	10	22	CPU0 Address Bit 0
00-I001	zaf24	42	<- 01	10-R015	zbb27	10	22	CPU0 Address Bit 1
00-I002	zaf23	44	<- 01	10-R029	zcb01	10	23	CPU0 Address Bit 2
00-I003	zbg08	44	<- 01	10-R041	zdb27	10	23	CPU0 Address Bit 3
00-I004	zbg07	44	<- 01	10-R005	zaf12	10	24	CPU0 Address Bit 4
00-I005	zbg06	45	<- 01	10-R018	zbe18	10	24	CPU0 Address Bit 5
00-I006	zaf01	42	<- 01	10-R031	zcf12	10	22	CPU0 Address Bit 6
00-I007	zaf02	42	<- 01	10-R044	zde18	10	22	CPU0 Address Bit 7
00-I008	zaf26	42	<- 01	10-R006	zag16	10	21	CPU0 Address Bit 8
00-I009	zaf27	42	<- 01	10-R019	zbf16	10	22	CPU0 Address Bit 9
00-I010	zbh18	42	<- 01	10-R032	zcg15	10	21	CPU0 Address Bit 10
00-I011	zbh17	41	<- 01	10-R045	zdf16	12	20	CPU0 Address Bit 11
00-I012	zbh16	42	<- 01	10-R046	zdh10	11	21	CPU0 Address Bit 12
00-I013	zah26	43	<- 01	10-R008	zah18	10	22	CPU0 Address Bit 13
00-I014	zah17	41	<- 01	10-R021	zbg12	11	20	CPU0 Address Bit 14
00-I015	zah16	41	<- 01	10-R034	zch18	10	20	CPU0 Address Bit 15
00-I016	zae26	41	<- 01	10-R047	zdg12	11	20	CPU0 Chip Sel. Bit 0
00-I017	zae14	37	<- 03	10-R043	zdf05	10	19	CPU0 Go Write
00-I018	zae22	33	<- 03	10-R004	zae10	10	14	CPU0 Abort
00-I019	zai24	32	<- 03	10-R005	zaf12	10	12	CPU0 Abort
00-I020	zad27	40	<- 17	00-R000	zaj21	27	62	CPUa Sec. 0 Write Data Bit 0
00-I021	zae15	44	<- 17	00-R001	zaj20	27	65	CPUa Sec. 0 Write Data Bit 1
00-I022	zbe01	42	<- 17	00-R002	zaj19	26	64	CPUa Sec. 0 Write Data Bit 2
00-I023	zbe02	42	<- 17	00-R003	zaj18	27	64	CPUa Sec. 0 Write Data Bit 3
00-I024	zah27	43	<- 17	00-R004	zai15	25	64	CPUa Sec. 0 Write Data Bit 4
00-I025	zbe26	44	<- 17	00-R005	zai14	25	66	CPUa Sec. 0 Write Data Bit 5
00-I026	zbf01	45	<- 17	00-R006	zai13	26	66	CPUa Sec. 0 Write Data Bit 6
00-I027	zah03	44	<- 17	00-R007	zai12	25	65	CPUa Sec. 0 Write Data Bit 7
00-I028	zah05	44	<- 17	00-R008	zbi12	26	64	CPUa Sec. 0 Write Data Bit 8
00-I030	zac20	44	<- 01	10-R002	zab20	11	23	CPU0 GoSS 0
00-I031	zaj22	45	<- 01	10-R010	zak08	10	24	CPU0 GoSS 1
00-I032	zbc20	45	<- 01	10-R016	zbb08	10	24	CPU0 GoSS 2
00-I033	zbj04	43	<- 01	10-R022	zbk21	11	22	CPU0 GoSS 3
00-I034	zcc20	44	<- 01	10-R028	zcb20	11	23	CPU0 GoSS 4
00-I035	zcj04	44	<- 01	10-R036	zck08	10	23	CPU0 GoSS 5
00-I036	zdc22	45	<- 01	10-R042	zdb08	10	24	CPU0 GoSS 6
00-I037	zdj15	41	<- 01	10-R048	zdk21	11	20	CPU0 GoSS 7
00-I040	zac07	44	<- 01	10-R000	zaa27	10	23	CPU0 GoSS 0 * Bank Bit 2**2'
00-I041	zad21	44	<- 01	10-R001	zaa01	10	23	CPU0 GoSS 0 * Bank Bit 2**2
00-I042	zai07	43	<- 01	10-R011	zal20	11	22	CPU0 GoSS 1 * Bank Bit 2**2'
00-I043	zaj21	43	<- 01	10-R012	zal08	11	22	CPU0 GoSS 1 * Bank Bit 2**2

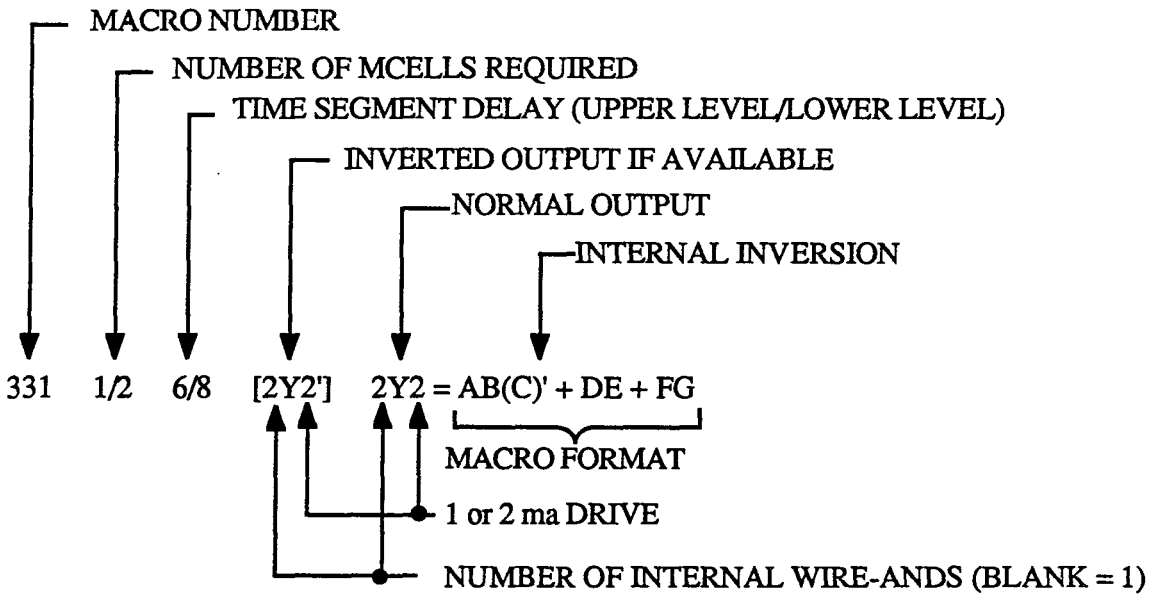
CRAY PROPRIETARY

SPECIAL CHARACTERS

1)	\	-	Indicates an exclusive-or function
2)	!0	-	Force 0 (or Z999)
3)	#	-	Indicates a forced 1
4)	&	-	Continue boolean on next line
5)	.	-	Begin comment field
6)	eject	-	Page eject command
7)	FORCE	-	On face sheet instead of LL = Indicates TS = X
8)	CLOCK	-	On face sheet instead of LL = Indicates clock inputs
9)	*,⊛	-	* and⊛ inputs are connected to an input follow (lower level series gate input). Unmarked upper level inputs and⊛ inputs can be connected to package pins while * input cannot.
10)	(2)	-	Number in ( ) at input indicate fan-in other than 1
11)	(4)	-	Number in ( ) at output indicate the total number of internal wire OR's
12)	$	-	$ at the output indicate internal collector dots
13)	$\overline{A}$	-	Indicates A not
14)	A'	-	Indicates A not
15)	+	-	Indicates an Ored function
16)	AB	-	Indicates that A is Anded with B
17)	r0 - 8'	-	Indicates that r0-r8 are all inverted or that r0', r1', r2', r3', r4', r5', r6', r7', r8'
18)	@	-	Wired-OR condition in theory, or Wired-And in electron flow

Hardware Trng.
YM17/09 J.E.S.

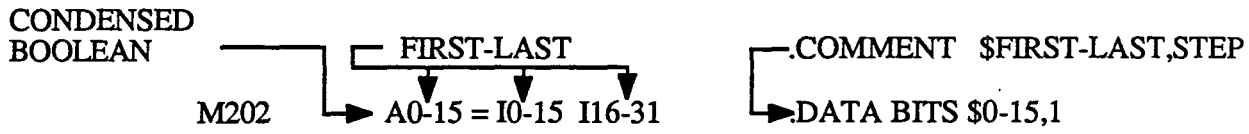
FORMAT EXAMPLE



MACRO BOOLEAN FORMATS

MUX	X = MUX (0,1) : DCD (2^0)
MUX	X = MUX (0,1,2,3) : DCD (2^1 , 2^0)
DCD	3210 = DCD (2^1 , 2^0)
SCY	Sum, Carry = SCY (A,B,C,D)
PCY	X = PCY (C5,C4,C3,C2,C1,C0:E5,E4,E3,E2,E1) (M321)
DIF	X = DIF (true, complement) DIFFERENTIAL RECEIVER

SPECIAL SYNTAX



X/Z1 OUTPUTS	X---	Rxx, (Z1 output) = (boolean)
Z1 OUTPUTS	X---	# ,(Z1 output) = (boolean) True, False = (boolean)
M/S LATCHES	M291	(master output) , (slave output) = AB ; t2
	or	
	M291	(slave output) = AB ; t2

Hardware Trng.
YM17/10 J.E.S.

M	Mcell	ts	Boolean
M200	1/4	7	[Y2'] Y2 = ABCDE
M201	1/4	6	[Y2'] Y2 = ABCD
M202	1/4	5	[Y2'] Y2 = AB
M203	1/2	7/8	[Y2'] Y2 = ABCDEFGH (****)
M204	1	12	[Y2'] 4Y2 = ABCDEFGHJKLH
M207	1/4	6	[Y2'] Y2 = ABCDEF (****)
M211	1/4	6/8	[Y2'] Y2 = AB + CD (* *)
M212	1/2	7/8	[2Y2'] Y2 = ABC + DE (* *) + FG + HJ (* *)
M213	1	7	[4Y2'] Y2 = ABCD + EFG + HJK + LMN
M215	1	8	[4Y2'] Y2 = AB(C)' (*) + DE(F)' (*) + GH(J)' (*) + KL + MN (* *)
M219	1/4	6/8	[Y2'] Y2 = ABC + DEF (* * *)
M221	1/4	7/8	[Y2'] Y2 = AB \ CD (* *)
M223	1/2	7/8	2Y2 = A (2) \ B (*) \ C (2) \ D (*)
M224	1/2	7/8	2Y2 = (A (2) \ B (*) \ C (2) \ D (*))'
M225	1/2	7/8	2Y2 = (AB + C) \ (DE + F)'
M226	1/2	7	2Y2 = (AB + C (*)) \ (DE + F (*))
M227	1/2	6/7	[Y2'] 2Y2 = (A (*) \ B) (C)'
M228	1/4	6/7	[Y2'] Y2 = A \ BC (* *)
M251	1	6/8	2Y2 = MUX(A,B,C,D (0 1 2 3)):DCD(F,E (*)) + (G)' (*)
M254	1/4	7/8	[Y2'] Y2 = MUX(AB,CD (0 1)):DCD(E (*))
M255	1/2	5/7	[Y2'] Y2 = MUX(A,B (0 1)):DCD(EF (* *)) [Y2'] Y2 = MUX(C,D (0 1)):DCD(EF (* *))
M256	1/4	5/6	[Y2'] Y2 = MUX(A,B (0 1)):DCD(C (*))
M259	1/2	6/8	[2Y2'] Y2 = MUX(A,B,C,D (0 1 2 3)):DCD(G (* *),EF)
	or		[2Y2'] Y2 = A(G)' (* *) (EF)' + B(G)' (* *) (EF) + CG(EF)' (* *) + DG(EF) (* *)
M261	1/2	5/6	2Y1 (3), 2Y1 (2), 2Y1 (1), 2Y1 (0) = DCD(B,A)/C (*)

Hardware Trng.
YM17/11 J.E.S.

M	Mcell	ts	Boolean
M277	3/4	8/9	[3Y2'] Y2 = ABCD + EFGH + JKLM + NP + QR + ST
M279	1	9	[4Y2'] Y2 = ABCD + EFGH + JKLM + NPQR+ ST + UV + WX+ YZ
M280	1/2	7/9	[2Y2'] Y2 = ABCD + EFGH + JK + LM
M281	1	7/8	(Sum, Car) 2Y2,2Y2 = SCY(A,BC,D)
M282	1/2	11	(Sum,Car) Y2,Y2 = SCY(A,BC,DE)
M284	1/4	6/8	(Sum,Car) Y1,Y2 = SCY(AB,CD)
M285	1/2	8/9	2Y2 = SUM (AB,CD,EF)
M286	1/2	6	2Y2 = CAR (AB,CD,EF)
M311	1	7/8	[4Y2'] Y2 = AB(C)' + DE(F)' + GHJ + KLM
M312	1/2	6/7	[2Y2'] Y2 = AB((C)' + (D)' + E)
M313	1/4	6/7	[Y2'] Y2 = AB(CD)'
M314	1/2	7/9	[2Y2'] Y2 = ABCD + EFG + HJK + LM
M319	3/4	7	[3Y2'] Y2 = ABC + DEF + GH + J
M321	1	8/9	[4Y2'] Y2 = PCY(C5,C4,C3,C2,C1,C0:E5,E4,E3,E2,E1)
	or		[4Y2'] Y2 = ABCDEF + GHJKLM + NPQR + STUV + WX + YZ
M322	3/4	6	[3Y2'] Y2 = ABC + DEF + GH
M323	1	8/9	[4Y2'] Y2 = AB(C)' + DE(F)' + GH + JK + LM + NP
M324	1	7	[4Y2'] Y2 = ABCDE + FGHJK + LMNPQ + RSTUV
M331	1/2	6/8	[2Y2'] Y2 = AB(C)' + DE + FG
M374	1/4	4	[Y2'] Y2 = DIF(A,B)

DELAY GATES

M278	1/4	7	[Y1'] Y1 = DLY(ABC)
M393	1/4	7	[Y1'] Y1 = DLY(AB)

Hardware Trng.
YM17/12 J.E.S.

M	Mcell	ts	Boolean

LATCHES

M278 1/4 0-6 [Y1'] Y1 = ABC;t2* E*

M291 1/2 0-6,16 [mY1'] mY1 ,[sY1'] sY1 = AB;t2* E* + (C)'*

M293 1/4 0-6 [Y1'] Y1 = AB;t2* E + (C)'*

M391 1/2 43-6 [sY1'] sY1 = AB;t2* + (C)'*

Hardware Trng.
YM17/13 J.E.S.

X	Ocell	ts	Boolean
X201	1	7	[X'] X = AB
		8	[Z1'] Z1 =
X202	1	8	[X'] X = ABCD
		9	[Z1'] Z1 =
X203	1	7/9	[X'] X = AB(CD)'**
		8/10	[Z1'] Z1 =
X204	1	7/9	[X'] X = ABCD**
		8/10	[Z1'] Z1 =
X205	1	8	[X'] X = ABCDE
		9	[Z1'] Z1 =
X211	1	7/8	[X'] X = AB + CD**
		7/9	[Z1'] Z1 =
X212	1	7/9	[X'] X = ABC + DE**
		8/10	[Z1'] Z1 =
X221	1	8/9	[X'] X = AB \ CD**
		8/10	[Z1'] Z1 =
X251	1	7/9	[X'] X = MUX(A,B)0 1:DCD(C)*
		8/10	[Z1'] Z1 =
X252	2	7/10	[X'] X = MUX (A,B)0 1:DCD(E)*
			[X'] X = MUX(C,D)0 1:DCD(E)
		8/10	[Z1'] Z1 =
			[Z1'] Z1 =
X254	1	7/9	[X'] X = MUX(AB,CD)0 1:DCD(EF)**
		8/9	[Z1'] Z1 =
X271	1	6	[X'] X = DIF(A,B)
		5	[Z1'] Z1 =

Hardware Trng.
YM17/14 J.E.S.

X	Ocell	ts	Boolean

LATCHES

X291 2 0-7,17 [mX'] mX ,[sX'] sX = AB;t2* E* + (C)*

X291 2 42-7 [sX'] sX = AB;t2*' + (C)*'

X292 1 0-7 [X'] X = AB;t2* E* + (C)*'

Hardware Tmg.
YM17/15 J.E.S.

PCB INFORMATION - REVISION 2

Terminology

- Termination point - The pin of the termination resistor.
- Main foil path - The path from the transmitter to the termination point.
- Load - An LSI package input pin.
- Tap - The region of the main foil path where stubs are connected.
- Stub - The foil path from the tap to a load.
- One time segment = 1 TS = 100 ps

Foil Paths Information

Terminations

A 60 ohm Ohmega resistor to V_{TT} = -2 volts is connected at the pin of the IC package which is the last load on the transmission line, but in some cases, the termination resistor is standalone (for example, not at a package pin).

All IC package outputs are terminated.

- Complementary pairs must be terminated on the same board pair (for example, A and B or C and D), but both signals do not have to use the same Z-axis connector block.

All unused inputs of an IC are terminated.

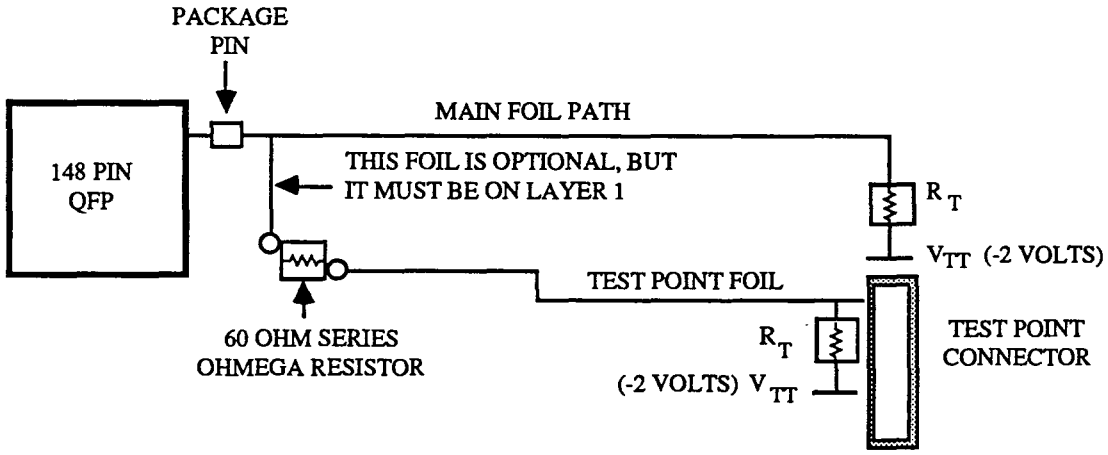
Unused differential inputs are tied to a high/low pair.

Boolean face sheet will identify balanced output groups of single-ended (SE) outputs by key-words "SE", "SEA", "SEB", etc.

Test Points

Test point signals will be foiled on layer one from a source pin to a via. The via will connect to a series 60 ohm Ohmega resistor which connects to the test point foil. The test point foil goes to the test point connector. A 60 ohm termination Ohmega resistor terminates the test point foil.

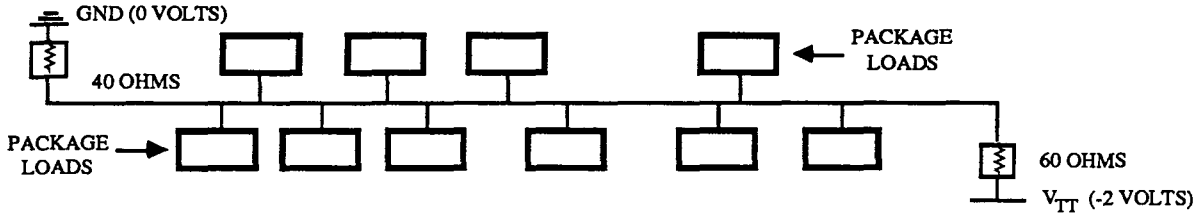
The foil from the package pin to the via is routed on layer one so that it can be cut on a populated PC board. This foil is optional, and some unconnected test points should be left near each package location.



TEST POINTS

Force "0" and "1" Signals

Force "0" is done by using a 40 ohm Ohmega resistor with one side connected to ground and the other connected to a foil which is terminated by the usual 60 ohm Ohmega resistor.



FORCE 0 CIRCUIT

Hardware Trng.
YM15/21B J.E.S.

Force "1" is done by connecting a 60 ohm Ohmega resistor to the IC input. The other side of the Ohmega resistor is connected to -2 volts (V_{TT}).

A Force "1" or "0" may also be done by using a spare gate on an IC if one is available.

Static Signals

Up to ten (10) loads may exist on the path from a transmitter.

A static signal may be wire-OR'ed to only ONE dynamic signal path.

Between Module Paths

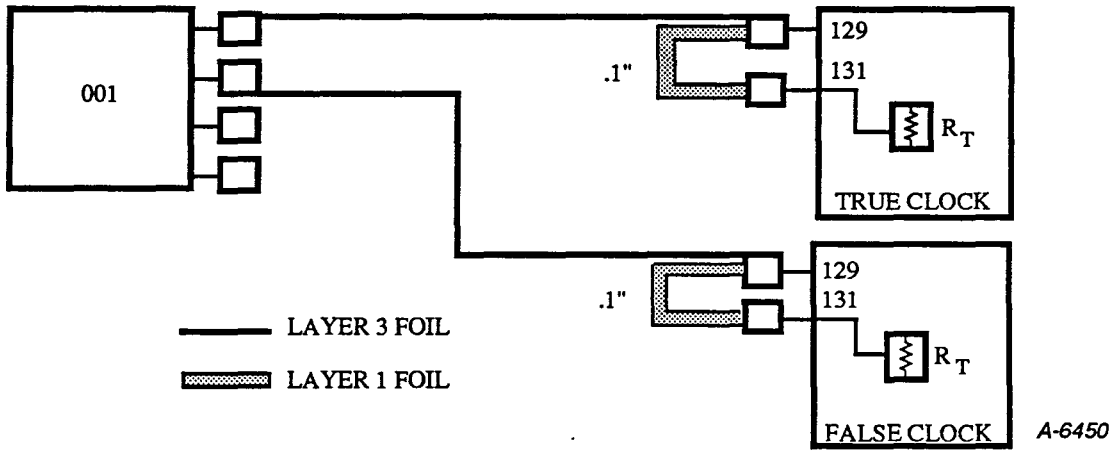
Twisted Pair Wire (Gore DXN 1186)

tdw = 100 ps/in * 1 + conn delay
1 = wire length = maximum [8 inches, point-to-point length + 4 inches]

Clock Nets

Every 2500 option which requires a clock will be designed for either a true or inverted clock input at pin number 129. The pulse width control input is at pin 131.

Layer 1 foil must be in an open area such that it can be cut on a populated board.



MCA2500 CLOCK CONNECTION

Hardware Trng.
YM15/22B J.E.S.

Definitions

One time segment = 1 TS = 100 ps (the smallest increment of time is 0.1 TS = 10 ps).

Internal AC Load Types

MCELL Switch = MS
XCELL Switch = XS
Low Level Emitter Follower = LL
Wire "AND" Emitter Follower = WA
Interconnect metal = MET

Fanin = FI which is the number of unit D. C. loads a gate input is equivalent to.

Fanout = FO which is the number of unit D.C. loads a gate output is driving.

Internal wire "AND" = IWA is the total number of internal wire AND's a macro output contains.

A * gate input is a low level input which has the possibility of saturation problems if driven from an external package pin.

A (*) gate input is a low level input which may be driven from an external package pin as per the rules state herein.

Gate Types That May Exist

MCELL with 1 ma Emitter Follower = Y1
MCELL with 2 ma Emitter Follower = Y2
XCELL with 1 ma Internal Emitter Follower = Z
XCELL with External Emitter Follower = X

Hardware Trng.
YM15/30A J.E.S.

OBJECTIVES - CRAY Y-MP Memory Hardware

Upon completion of the section, the student will be able to:

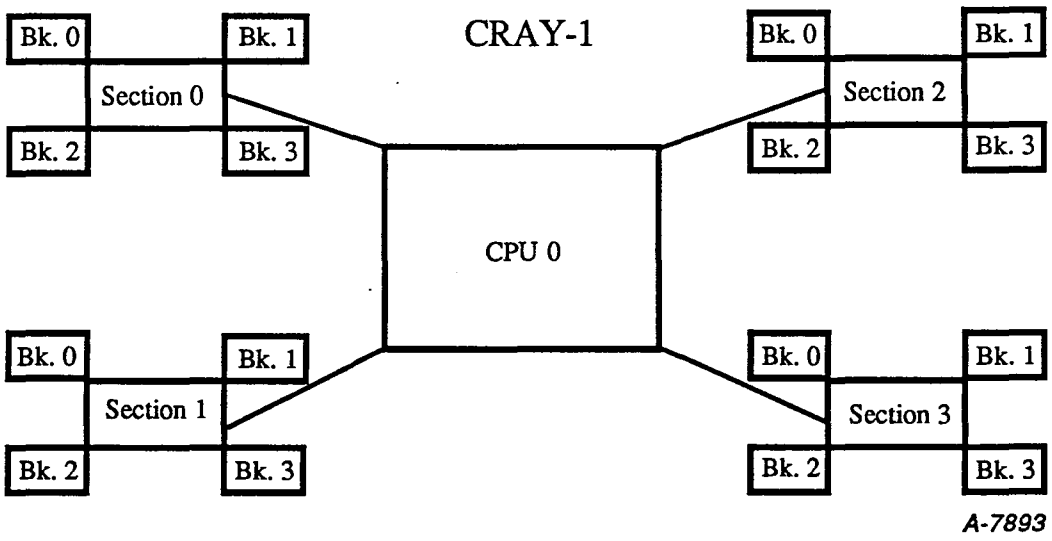
- Describe the overall specification of the memory including size, speed, data format, and address format
- Determine the failing memory module, option type, or memory chip given the failing address or data bit
- Intepret Memory Parity Error information
- Define with respect to time and use the control signals
- Trace the Data, Address, and Controls signals

CRAY MAINFRAMES MEMORY HARDWARE COMPARISONS

Each new generation of the Cray mainframes from CRAY-1 to CRAY X-MP, and to the CRAY Y-MP has addressed memory in a different and unique way which advanced the hardware to better resolve Bank conflicts. Each new generation of the Cray machine has become the stepping stone for the next new generation of machine to learn and build from, as demonstrated here.

CRAY-1 Memory

With the introduction of the CRAY-1 in 1976 with 1 mega word of memory at 64 bits and 8 check bits, memory was partitioned into four sections called Section 0, 1, 2, and 3. Each section contained four banks for a total of 16 banks. Any one bank can only be referenced every four clock periods. With four sections addressing the same banks within each section, by the time the reference comes back to the same bank (for example Section 0 Bank 0), Bank 0 would have dropped its bank busies.



The CRAY-1 memory can serve up to one memory request every clock period at 12.5 nanoseconds. The memory request could come from the CPU or the I/O. The CPU and I/O sections shared memory via a single port access. If simultaneous requests occurred from the CPU and I/O, the CPU would take priority. The CRAY-1 also has a unique way of referencing memory during a Fetch or HISP reference request, where all four sections would be accessed for four clock periods, delivering four Cray words to the Instruction Buffer or HISP Buffers per clock period for a total of 16 words.

Hardware Trng.
YM26/22 J.E.S.

Bank conflicts within the same section would restrict memory requests. A request to a particular bank causes that bank to go busy for four clock periods. For that reason, memory can handle one request per clock period only if a particular bank has not been accessed more often than every four clock periods.

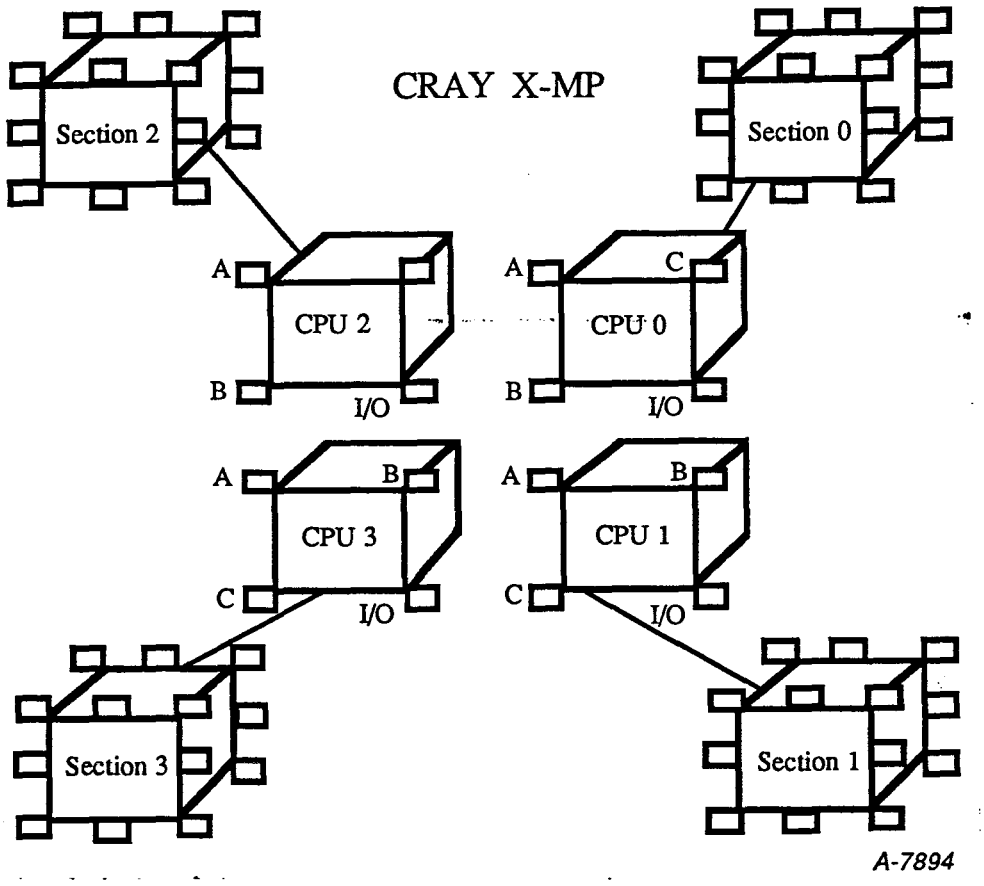
CRAY X-MP Memory

The problem with the CRAY-1 memory was its single access to any given section. This problem was addressed in the CRAY X-MP which led, among other things, to the end of production of the CRAY-1.

What was added to the CRAY X-MP was another level of control to a memory access called Ports A, B, C, and I/O. Ports fixed the CRAY-1 single access problem in a unique manner by allowing more than one memory reference to occur each clock period within the same CPU as long as the memory references are to different sections.

In the CRAY X-MP/2, another reference could be made to the same section one clock period apart as long as the reference was not to the same bank. If a bank conflict occurred, the lower priority port would be held. In the CRAY X-MP/4 a bank conflict would shut down all four ports.

What the CRAY X-MP memory did was take the best parts of the CRAY-1 memory, which were the sections, and improve on the single section reference. The CRAY X-MP was introduced in 1982 as a two processor mainframe with 1, 2, or 4 million words of memory, and later in 1984 as a four processor mainframe with 8 or 16 million words of memory. In May 1988 the CRAY X-MP EA was introduced with up to 64 million words of memory . Memory was once again divided into four Sections, namely 0, 1, 2, and 3, similar to the CRAY-1. Each section contained up to eight banks per section in the CRAY X-MP/2 and 16 banks per section in the CRAY X-MP/4, for a total of 32 banks in the CRAY X-MP/2 and 64 banks in the CRAY X-MP/4.



Each CPU contained four ports, and each CPU contained its own access path to each memory section. Each CPU has an independent path to each section so that four references from different CPUs can occur to each section in the same clock period, as long as the references are to different banks. This allows up to 16 references per clock period on the CRAY X-MP/4. With each CPU having four ports, a CPU could reference memory with four different operations using the four ports to the four different sections and not have a conflict.

For example, CPU 0 wants to perform two successive vector reads of memory. In the CRAY-1 the first vector read would issue and the second would have to wait in CIP until the first vector read had finished. In the CRAY X-MP both vector reads are allowed to issue one clock period apart. The first vector read would select Port B while the second vector read would select Port A. Both vector reads will continue execution as long as the two ports, A and B, do not request the same section in the same clock period. When this happens the port with the odd increment, or stride, would have the highest priority. If there is a tied situation where both ports have an even/odd stride, Port B would go first because it was issued first.

The four ports can be classified by what type of references use the ports. There are two read ports, A and B, one write port, C, and one I/O port which could be either a read or write operation used by the I/O channels.

Read Port A	-	Vector, B Register, Address Reference
Read Port B	-	Vector, T Register, Scalar Reference
Write Port C	-	Vector, B/T Register, Scalar/Address Reference
I/O Port	-	LOSP, HISP, VHISP Reference

Hardware Trng.
YM26/24 J.E.S.

The ports make more efficient use of the section. The Fetch operation in the CRAY X-MP took an even more radical approach than the CRAY-1 by allowing eight words to be read out of memory per clock period. This was accomplished by having CPU 0 and CPU 1 sharing their read paths from memory along with CPU 2 and CPU 3 sharing their read path from memory during a Fetch operation. When CPU 0 wanted to perform a Fetch, it would use CPU 1's read path from memory for the duration of the Fetch sequence and activate all four sections similar to the CRAY-1. This resulted in eight words being delivered to the Instruction Buffers for four clock periods for a total of 32 Cray words.

CRAY X-MP Memory Control

The CRAY X-MP, with the additions of the ports, has added a second dimension to the memory control. The memory control on the CRAY X-MP can be broken down into the intra CPU conflicts and inter CPU conflicts. The intra CPU conflicts happen within the CPU memory control and solves for section or port conflicts. In the case when two or more ports want the same section within the same CPU, the port that would get the section is determined by the port with the odd increment, or stride, in memory. If both ports have odd or even increments, the first priority is the first one issued. When a memory reference instruction has issued, the port's priority is determined at that time and is used throughout the time that the port is active. First issued is determined when a port is requested and no other ports are active; that port is then the first issued. For a Gather/Scatter type instruction where the (Vk) operand is used as the increment value, a default of an odd increment is chosen. The I/O Port has the lowest priority and is not allowed if Fetch or Exchange are active, or if Port A/B/C has a reference to the same section as I/O within the same clock period, unless it is a lockout condition where one I/O reference is made as the highest priority.

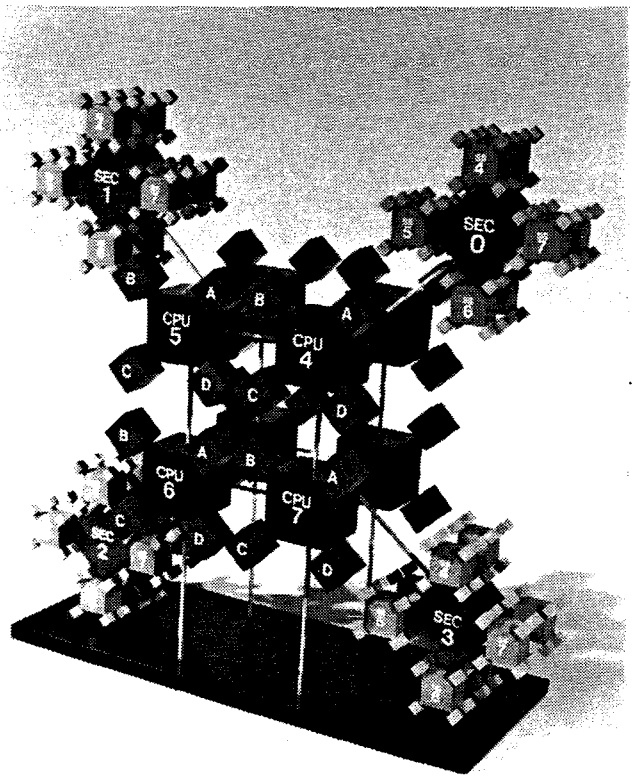
The inter CPU conflicts are similar to the CRAY-1 Bank Conflicts, and on the CRAY X-MP they occur when two or more CPUs request the same bank in the same section, called a simultaneous bank conflict. A priority counter determines which CPU can go first. The priority counter allows each CPU a shot at being first. A bank conflict can also occur when a CPU is requesting a bank that has previously been accessed and is busy, in which case the CPU would have to wait for the bank busies to go away, which could be for one, two, or three clock periods. Once a bank is accessed, it is held busy for four clock periods.

CRAY Y-MP Memory

While the CRAY X-MP has improved on the CRAY-1's memory with the addition of ports, the CRAY Y-MP has also improved upon the CRAY X-MP memory control. The improvements made in the CRAY Y-MP memory were accomplished by increasing the number of banks and adding a third level to the memory control, called Subsection.

The CRAY Y-MP mainframe has eight processors, currently with 32 or 64 million words of memory. Memory is divided into four sections similar to the CRAY-1 and CRAY X-MP. Each section is divided into eight subsections, with each subsection containing eight banks for a total of 256 banks. The CRAY Y-MP uses the four ports similar to the CRAY X-MP. These ports are called A, B, C, and D.

The increase in the number of banks has decreased the number of simultaneous bank conflicts. When a simultaneous bank conflict occurs, an evenly distributed pattern determines which CPU would have the highest priority. When performing a Fetch operation the words are read from memory one word at a time, without sharing the other CPUs read paths as in the CRAY X-MP. The instruction buffers are interleaved on even and odd words with separate write and read controls. This allows instruction parcels to be read from the instruction buffer and written into the instruction buffer simultaneously with different even or odd addresses. Not sharing the other CPUs read path during a Fetch operation prevents one CPU from holding up another CPU during a Fetch operation. In a 32 bank CRAY X-MP/2 or CRAY X-MP/4, any CPU requesting a Fetch or Exchange would request all 32 banks in memory for the duration of the Fetch or Exchange sequence preventing any other CPU from making a memory reference. Adding more banks and not sharing read paths during a Fetch greatly reduces the number of Bank Conflicts on the CRAY Y-MP.



Subsection Control

Adding subsections to the CRAY Y-MP allows the memory conflict checking to be split into two stages. The first stage resolves section and subsection conflicts independently in each CPU. Within each CPU each subsection, acting like a bank, goes busy when referenced by that CPU and cannot be referenced again by that CPU until the busy clears. The second stage, at each subsection, resolves the simultaneous bank and bank busy conflicts between the eight possible references from the eight CPUs and the eight banks within a subsection. When a CPU reference is allowed in a subsection, a release signal is sent to that CPU to clear the subsection busy in that CPU. A subsection conflict is treated as an intra CPU conflict, and occurs when a port has requested a subsection that is busy.

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Read Port A	-	Vectors, B Registers, Scalar Reference
Read Port B	-	Vectors, T Registers References
Write Port C	-	Vectors, B/T Registers, Scalar Reference
Read/Write Port D	-	Fetch, I/O Reference

The port with the odd increment has the highest priority. When in a tied situation where the ports in conflict have an even or odd increment, the priority goes to the one first issued. Port D, when being used by a Fetch operation, would have the highest priority unless I/O is using Port D in an I/O Lockout condition.

Once a subsection conflict is resolved for a Simultaneous Access conflict to the same section, the subsection requested within the section is compared against any previous port references to see if the requested subsection has been previously referenced.

If the subsection has been referenced and not released, the requesting port reference would be held. What this allows is more than one reference to be active in the same section and hold any port references which are in conflict with a previous memory reference subsection. In the CRAY X-MP/2 this same condition occurred in the section as long as there was not a bank conflict, where two or more ports wanted the same bank, in which case one of the ports would be held. In the CRAY X-MP/4 more than one reference was allowed to the same section as long as the memory reference was to a different bank. When a Bank conflict occurred all ports would be held regardless of what section was being requested.

Bank Control

The CRAY Y-MP inter CPU conflicts occurs when two or more CPUs have requested the same bank. Bank conflicts occur as a Simultaneous Bank conflict or a CPU requesting a bank which has been previously referenced and is busy. A bank in the CRAY Y-MP, if accessed, is held busy for 4 CPs. If two CPUs request the same bank, at the same clock period, one of the CPUs would have to wait 5 CPs, of which 1 CP is a Simultaneous Bank conflict and 4 CPs of Bank Busy. To determine the priority on bank conflicts, a hardwired priority has been set up depending on which section and subsection is being referenced. From the predetermined path, the memory control determines which CPU has the higher priority. The priority is such that a CPU with a CPU A reference has the highest priority, while a CPU with a letter CPU H would have the lowest priority. The following table shows the CPUs letter reference.

CPU to Memory Priority

Section		0		1		2		3	
Subsection		0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7
CPU PATH	0	A	H	D	E	C	F	B	G
	1	B	G	A	H	D	E	C	F
	2	C	F	B	G	A	H	D	E
	3	D	E	C	F	B	G	A	H
	4	H	A	E	D	F	C	G	B
	5	G	B	H	A	E	D	F	C
	6	F	C	G	B	H	A	E	D
	7	E	D	F	C	G	B	H	A

For example, if CPU 3 went to Section 1, Subsection 5, its CPU letter reference would be CPU C when competing for any of the banks in Subsection 5. This means any reference from CPU A or CPU B for the same bank as CPU C wanted would cause CPU C to wait.

The CRAY Y-MP memory control is far superior to the CRAY-1 or CRAY X-MP. However, the CRAY Y-MP got where it is by taking the best from the CRAY-1 and the CRAY X-MP and continuing with the evolution process by improving on the CRAY X-MP by adding more banks and managing the banks from a third level of control called subsections. A Subsection conflict is handled on a CPU level, as a Bank conflict is handled among the various CPUs.

The CRAY-1 can be thought of as a one dimensional memory with memory being divided into four sections. The CRAY X-MP is a two dimensional memory array with section and ports, while the CRAY Y-MP is a three dimensional memory with sections, subsections, and ports. Each generation of machine has added more CPU which presents a new challenge to resolving conflicts in memory, caused by multi-CPU accesses to memory.

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CRAY Y-MP MEMORY (64K x 1) ECL

The CRAY Y-MP uses (64K x 1) ECL memory chips, which are organized into 256 banks, for a total of 32 million words of storage.

The CRAY Y-MP memory incorporates four sections, with each section containing eight subsections. Each subsection then contains 8 banks for a subsection total of 64 banks and a memory total of 256 banks.

Physically, there are eight modules per section, each module containing a 9-bit slice of the 72-bit word. Each module is also organized into eight subsections. Subsections 0 and 1 are located on the A Board of the module, Subsections 2 and 3 are on the B board, Subsections 4 and 5 are on the C board and Subsections 6 and 7 are located on the D board.

There are four ports per CPU, all four ports can be accessing four different sections within the same clock period. All eight CPUs can go to the same subsection, as long as they are going to different banks within the subsection. Once a CPU has accessed a bank, that bank is held busy for 5 clock periods (CPs).

A 72-bit word is sent from the CPU module to the eight memory modules which make up a section. Data bits are divided into 9 bits per module. Memory module 0 or Memory 0 contains data bits (2^8 - 2^0). Memory 1 contains bits (2^{17} - 2^9), and so on. Controls and address which are sent from the CPUs must also be fanned out to the eight memory modules. This is called an Outboard fanout because they are done outside of the normal module's function. These Outboard fanouts are carried out by the (ZW, ZO, ZA, ZS, ZQ) options. All memory modules assist in performing the 1 to 8 Outboard fanouts, some of the modules performing more fanouts than other memory modules. Once on the module, another fanout to the eight subsections takes place. This happens for the address, control and data and is referred to as an Onboard fanout, because this fanout happens only on a memory module.

Once a particular CPU has accessed a subsection, the controls Go Subsection (GOSS) and GOSS bank bits are routed to the two (ZX) options that control the subsection. The (ZX) option performs a subsection conflict check on the eight banks within the subsection among all CPUs. Only one CPU can access a bank at a time. Once the CPU has accessed a bank, that bank is held busy for 5 CPs. When a conflict occurs such that two or more CPUs want the same bank, called a Simultaneous Bank conflict, the CPU with the lowest number "i" term would have the highest priority to use the bank.

Read Operation To Subsection 0

During a Read operation, only the address and control are sent from the CPU module. The address is latched and held in the (ZY0, ZY1, ZU0, ZM0, ZN0, ZN1) options by the GOSS CPU (A - H). The (ZX0, ZX1) options for Subsection 0 will resolve any CPU conflict involving the particular bank. When the conflict is resolved, the (ZX) will supply the latched address on the (Z-) option with a Bank (0 - 7) Select Code. The Select Code will assign a particular CPU to a bank. The address is presented to the Memory bank for 5 CPs.

To set up the appropriate Read paths back to a particular CPU, two things must be done: first, 1 of 8 banks needs to be selected from within Subsection 0, and secondly, 1 of 8 subsections needs to be selected for a particular CPU. Before the Read data will enter the (ZR) option from the bank that was being addressed, the (ZR0, ZR1, ZR2) are sent a CPU (A - H) Read Bank Select Code, which assigns a Bank (0 - 7) to a particular CPU (A - H). Where the Read Select Code is generated depends on which CPU has requested a bank. If CPU (A) requests Bank (0 - 3), the Select Code is generated by the (ZX0) option. If CPU (A) requests Bank (4 - 7), then the (ZX1) will supply the code. When CPU (B) or (F) requests Bank (0 - 7), the (ZY1) will supply the code. When CPU (C) or (G) requests Bank (0 - 7) the (Zn0) will supply the code. If CPU (D) or (H) request Bank (0 - 7), the (ZN1) will supply the code. Finally, if CPU (E) requests Bank (0 - 7), the (ZY0) will supply the code. The Read Bank Select Code is (000) for Bank 0 or (111) for Bank (N + 7). Subsection 1 has different (Z-) assignments.

Once the Read Bank Select Code is set up on the (ZR) options, it is delayed while the address is being presented to the (64K x 1) chip. The words sent from Subsection 0's banks are routed to the (Zr) options. The (Zr's) will steer the data from Banks (0 - 7) to the appropriate CPU (A - H), performing a 1 of 8 Bank Select. CPU (A - H) data bits are then sent to the (ZS) options. The (ZS) options have been set up such that all Subsections (0 - 7) send their data to (ZS0) for CPU (A), (ZS1) for CPU (B), etc. The (ZS0) for CPU (A) would then have to select the 9 bits of data from 1 of 8 subsections. To do this the (ZS) options are supplied with a 3-bit SS Select code. The SS Select Code comes from the CPU modules through a 1-to-8 Outboard fanout on the (ZS0, ZS1, ZS20) options. The (ZS0) for CPU (A), or CPU 0, will then output the data to the CPU 0 module.

Write Operation To Subsection 0

On a Write operation to memory, the address, control, and data are sent from the CPU module to a particular section. The CPU module determines the section to which these signals are sent. Once sent to the section, the Control and Address signals undergo a 1 to 8 Outboard fanout to each module within the section. Data is not fanned out, but is split up into 9 bits per module. Memory module 0, or Memory 0, receives data bit (2^8 - 2^0) and so on. The 9 bits of data enter the (ZQ0, ZW1, ZU0, ZM0, ZV0, ZO0) options for Subsection 0, along with GOSS 0 CPU (A - H). The GOSS 0 CPU (A - H) signals will latch and hold the data for the correct CPU. The same thing happens for the address, but this is performed on the (ZY0, ZY1, ZU0, ZM0, ZN0, ZN1) options, for Subsection 0. Once the (ZX0, ZX1) options have resolved any conflict among the CPUs, the (ZX) will generate a Bank (0 - 7) Select Code, which is then sent to the latched data and address (Z-) options. The Bank (0 - 7) Select Code will assign a particular CPU (A - H) to a specific Bank (0 - 7). The Select Code sent from the (ZX) option is (000) for CPU 0, (001) for CPU 1, etc; however, on the address and data (Z-) options, not all the options receive the true state of the Select Code. The (ZM0, ZV0, ZO0) for data and (ZM0, ZN0, ZN1) for address receive an inverted Select Code, while the (ZQ0, ZW1, ZU0) for data and the (ZY0, ZY1, ZU0) for address receive the true Select Code.

The data is then steered to the correct bank within Subsection 0 for the CPU (A - H) that was requesting a Write reference. The Write Enable is supplied for 3 CPs by the (ZX) option which is assigned to that bank. Banks (0 - 3) are controlled by (ZX0), while (ZX1) controls Banks (4 - 7). The address and data are held on the memory chip for 5 CPs by the (Z-) options. The chip select is supplied by the (ZV0) option. There are two (64K x 1) chips per bit position, so there are two chips for data bit (2^0), etc. Which chip is selected is dependent on CS-0 or CS-1. Both CS-0 and CS-1 come from address bit (2^{16}) on the memory module or address bit (2^{19}) of the absolute address. If address bit (2^{19}) equals a zero, CS-0 is Enabled. If address bit (2^{19}) equals a one, CS-1 is enabled. When a CPU sends an Abort to the (ZV/ZP) options the (ZV/ZP) will disable CS-0 and CS-1. When an Abort occurs on a Write operation to memory, nothing is written; on a Read operation zeroes are read from memory.

	SUBSECTION			SECTION		CPU PRIORITY							
	2^4	2^3	2^2	2^1	2^0	a	b	c	d	e	f	g	h
00	0	0	0	0	0	0	1	2	3	7	6	5	4
01	0	0	0	0	1	1	2	3	0	4	7	6	5
02	0	0	0	1	0	2	3	0	1	5	4	7	6
03	0	0	0	1	1	3	0	1	2	6	5	4	7
04	0	0	1	0	0	0	1	2	3	7	6	5	4
05	0	0	1	0	1	1	2	3	0	4	7	6	5
06	0	0	1	1	0	2	3	0	1	5	4	7	6
07	0	0	1	1	1	3	0	1	2	6	5	4	7
10	0	1	0	0	0	4	5	6	7	3	2	1	0
11	0	1	0	0	1	5	6	7	4	0	3	2	1
12	0	1	0	1	0	6	7	4	5	1	0	3	2
13	0	1	0	1	1	7	4	5	6	2	1	0	3
14	0	1	1	0	0	4	5	6	7	3	2	1	0
15	0	1	1	0	1	5	6	7	4	0	3	2	1
16	0	1	1	1	0	6	7	4	5	1	0	3	2
17	0	1	1	1	1	7	4	5	6	2	1	0	3
20	1	0	0	0	0	0	1	2	3	7	6	5	4
21	1	0	0	0	1	1	2	3	0	4	7	6	5
22	1	0	0	1	0	2	3	0	1	5	4	7	6
23	1	0	0	1	1	3	0	1	2	6	5	4	7
24	1	0	1	0	0	0	1	2	3	7	6	5	4
25	1	0	1	0	1	1	2	3	0	4	7	6	5
26	1	0	1	1	0	2	3	0	1	5	4	7	6
27	1	0	1	1	1	3	0	1	2	6	5	4	7
30	1	1	0	0	0	4	5	6	7	3	2	1	0
31	1	1	0	0	1	5	6	7	4	0	3	2	1
32	1	1	0	1	0	6	7	4	5	1	0	3	2
33	1	1	0	1	1	7	4	5	6	2	1	0	3
34	1	1	1	0	0	4	5	6	7	3	2	1	0
35	1	1	1	0	1	5	6	7	4	0	3	2	1
36	1	1	1	1	0	6	7	4	5	1	0	3	2
37	1	1	1	1	1	7	4	5	6	2	1	0	3

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CRAY Y-MP CPU - CPU PRIORITIES

CPU A - H DESIGNATORS

On the memory module, the CPU is given a letter designator by the Subsection the CPU is trying to access to keep the interconnects between the boards as short as possible.

Section 0 CPU 0 is called CPU (A) in Subsection 0, 1, 4, and 5 and CPU (H) in Subsection 2, 3, 6, and 7. The table below shows the other combinations.

SECTION 0

Priorities	A	B	C	D	E	F	G	H	(A - highest, H - lowest)
SS0	CPU 0	CPU 1	CPU 2	CPU 3	CPU 7	CPU 6	CPU 5	CPU 4	* - wire name
SS1	CPU 0	CPU 1	CPU 2	CPU 3	CPU 7	CPU 6	CPU 5	CPU 4	*
SS2	CPU 4	CPU 5	CPU 6	CPU 7	CPU 3	CPU 2	CPU 1	CPU 0	
SS3	CPU 4	CPU 5	CPU 6	CPU 7	CPU 3	CPU 2	CPU 1	CPU 0	
SS4	CPU 0	CPU 1	CPU 2	CPU 3	CPU 7	CPU 6	CPU 5	CPU 4	*
SS5	CPU 0	CPU 1	CPU 2	CPU 3	CPU 7	CPU 6	CPU 5	CPU 4	*
SS6	CPU 4	CPU 5	CPU 6	CPU 7	CPU 3	CPU 2	CPU 1	CPU 0	
SS7	CPU 4	CPU 5	CPU 6	CPU 7	CPU 3	CPU 2	CPU 1	CPU 0	

SECTION 1

Priorities	A	B	C	D	E	F	G	H	(A - highest, H - lowest)
SS0	CPU 1	CPU 2	CPU 3	CPU 0	CPU 4	CPU 7	CPU 6	CPU 5	* - wire name
SS1	CPU 1	CPU 2	CPU 3	CPU 0	CPU 4	CPU 7	CPU 6	CPU 5	*
SS2	CPU 5	CPU 6	CPU 7	CPU 4	CPU 0	CPU 3	CPU 2	CPU 1	
SS3	CPU 5	CPU 6	CPU 7	CPU 4	CPU 0	CPU 3	CPU 2	CPU 1	
SS4	CPU 1	CPU 2	CPU 3	CPU 0	CPU 4	CPU 7	CPU 6	CPU 5	*
SS5	CPU 1	CPU 2	CPU 3	CPU 0	CPU 4	CPU 7	CPU 6	CPU 5	*
SS6	CPU 5	CPU 6	CPU 7	CPU 4	CPU 0	CPU 3	CPU 2	CPU 1	
SS7	CPU 5	CPU 6	CPU 7	CPU 4	CPU 0	CPU 3	CPU 2	CPU 1	

SECTION 2

Priorities	A	B	C	D	E	F	G	H	(A - highest, H - lowest)
SS0	CPU 2	CPU 3	CPU 0	CPU 1	CPU 5	CPU 4	CPU 7	CPU 6	* - wire name
SS1	CPU 2	CPU 3	CPU 0	CPU 1	CPU 5	CPU 4	CPU 7	CPU 6	*
SS2	CPU 6	CPU 7	CPU 4	CPU 5	CPU 1	CPU 0	CPU 3	CPU 2	
SS3	CPU 6	CPU 7	CPU 4	CPU 5	CPU 1	CPU 0	CPU 3	CPU 2	
SS4	CPU 2	CPU 3	CPU 0	CPU 1	CPU 5	CPU 4	CPU 7	CPU 6	*
SS5	CPU 2	CPU 3	CPU 0	CPU 1	CPU 5	CPU 4	CPU 7	CPU 6	*
SS6	CPU 6	CPU 7	CPU 4	CPU 5	CPU 1	CPU 0	CPU 3	CPU 2	
SS7	CPU 6	CPU 7	CPU 4	CPU 5	CPU 1	CPU 0	CPU 3	CPU 2	

SECTION 3

Priorities	A	B	C	D	E	F	G	H	(A - highest, H - lowest)
SS0	CPU 3	CPU 0	CPU 1	CPU 2	CPU 6	CPU 5	CPU 4	CPU 7	* - wire name
SS1	CPU 3	CPU 0	CPU 1	CPU 2	CPU 6	CPU 5	CPU 4	CPU 7	*
SS2	CPU 7	CPU 4	CPU 5	CPU 6	CPU 2	CPU 1	CPU 0	CPU 3	
SS3	CPU 7	CPU 4	CPU 5	CPU 6	CPU 2	CPU 1	CPU 0	CPU 3	
SS4	CPU 3	CPU 0	CPU 1	CPU 2	CPU 6	CPU 5	CPU 4	CPU 7	*
SS5	CPU 3	CPU 0	CPU 1	CPU 2	CPU 6	CPU 5	CPU 4	CPU 7	*
SS6	CPU 7	CPU 4	CPU 5	CPU 6	CPU 2	CPU 1	CPU 0	CPU 3	
SS7	CPU 7	CPU 4	CPU 5	CPU 6	CPU 2	CPU 1	CPU 0	CPU 3	

One of the advantages of lettering the CPUs is that when the (ZX) option checks for Subsection conflicts and a decision needs to be made as to which CPU will get a particular bank, the lowest lettered CPU would have the highest priority. Because of the way the CPU letters are distributed among the Subsections, all CPUs are treated the same when using the law of averages.

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CRAY Y-MP MEMORY OPTIONS PER MODULE

OPTION TYPE	NUMBER USED	DESCRIPTION
ZM	8	2 Address / 1 data, GOSS F.O.
ZN	16	3 Address / 2 CPU bank select
ZO	8	2 data / two 1 - 8 F.O.
ZP	4	Chip Select / 1 Data / four 1 - 1 F.O.
ZQ	8	2 Data / two 1 - 8 F.O.
ZR	24	3 bits SS Read Data
ZS	8	CPU Read Data / one 1 - 8 F.O.
ZV	4	Chip Select / 1 Data / four 1 - 1 F.O.
ZW	8	2 data / two 1 - 8 F.O.
ZX	16	4 bank control / 4 W.E., 8 Go Read
ZY	16	3 Address / 2 CPU Bank Select
ZU	8	2 Address / 1 Data / 4 GOSS F.O.
ZA	8	Fanout
TO	4	Clock Distribution
	140 total options	

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CRAY YMP MEMORY (OPTIONS INVOLVED) (64K x 1) ECL MEMORY

(ZA0, ZA1, ZA10, ZA11, ZA20, ZA21, ZA30, ZA31) Options

The (ZA) options are used to fanout memory information from the various CPUs. Since this fanout is done on the memory modules themselves, it is referred to as an Onboard fanout. In general, the (ZAs) fanout the Address, Chip Select, Data, and the Go Write to Subsections (0 - 7). The various (ZA) options can be differentiated by what data or address bits are being fanned out for the particular CPU. The (ZA) options also perform a 1 to 8 fanout to the eight memory modules within a section. (ZA1, ZA11) fanout address bits (2^{11}, 2^{10}, 2^{9}, 2^{8}) on memory modules (0 - 7) for all eight CPUs; this is called an Outboard fanout.

(ZM0, ZM1, ZM10, ZM11, ZM20, ZM21, ZM30, ZM31) Options

The (ZM) options are capable of handling 2 address bits and 1 write data bit for each subsection. (ZM0) is for Subsection 0, etc. The (ZMs) are able to latch and hold the address and data from all eight CPUs. When the time is right for a particular CPU to use 1 of 8 banks within a subsection, the (ZMs) will decode a Bank (0 - 7) Select Code, and steer the address and write data to the appropriate bank. The (ZM) options have been set up to receive an inverted CPU Select Code (') and an inverted GOSS ('); this is done to optimize the number of pins per option. The (ZMs) also have a fanout which is used to assist in the GOSS fanout on each module.

(ZN0-ZN3, ZN10-ZN13, ZN20-ZN23, ZN30-ZN33) Options

The (ZN) options are capable of handling 3 address bits. There are two (ZN) options per subsection with (ZN0, ZN1) being used for Subsection 0, etc. The (ZN) is able to latch and hold the address for all eight CPUs. When the (ZNs) receive the CPU Select Code, they steer the particular CPU to the correct bank. The (ZNs) receive inverted controls similar to the (ZM) options. The (ZNs) are responsible for generating the Read Bank Selects (2^{2}, 2^{1}, 2^{0}) for CPUs (N and N + 4). (ZN0) generates the Read Bank Selects for CPUs (C/G) in Subsection 0, (ZN1) is used for CPUs (D/F), also in Subsection 0, etc. These control signals are then sent to the (ZR) options.

(ZO0, ZO1, ZO10, ZO11, ZO20, ZO21, ZO30, ZO31) Options

The (ZO) options are capable of handling 2 write data bits. The (ZOs) perform the same functions as the (ZM) options, and receive inverted controls as well. The (ZO) options assist in the initial 1 to 8 fanout of address and controls to the eight memory modules. There is one (ZO) option for each of the eight subsections. The (ZOs) also assist in the 1 to 8 Outboard fanout of address and controls from the various CPUs to the eight modules within a section.

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(ZP10, ZP11, ZP30, ZP31) Options

Each (ZP) option handles 1 data bit, the chip select, and the Abort signal for a subsection. There is one (ZP) option for subsection 2, 3, 6, and 7. Since there are two (64K x 1) memory chips per bit, or 144 chips per 72-bit word, chip select 0 selects the lower 72 chips and chip select 1 selects the upper 72 chips. When the Abort signal is present, the chip selects are forced to zeroes, preventing a Write operation from completing or during a Read, causing zeroes to be read from memory. The (ZP) options also perform a 1 to 2 fanout of Master Clear, 3 CP Write Enable, Bank Busy (2^1, 2^0) to the two (ZX) options in the subsection.

(ZQ0, ZQ3, ZQ10, ZQ13, ZQ20, ZQ23, ZQ30, ZQ33) Options

The (ZQ options perform the same function as the (ZM) options, except that the (ZQs) receive the true GOSS and Bank Select Code. There is one (ZQ) used per subsection. Each (ZQ) contains 2 bits of data of the 9 bits per module. The (ZQs) also perform a 1 to 8 fanout of the GOSS and Bank bit (2^2) to the eight modules within a section for all CPUs.

(ZR0, ZR1, ZR2, ZR3, ZR4-ZR5, ZR10-ZR15, ZR20-ZR25, ZR30-ZR35) Options

The (ZR) options are called Subsection Bank Data Selects. Each (ZR) option handles 3 bits of the 9 bits per subsection on a Read. (ZR0 - ZR2) are assigned to Subsection 0, and (ZR3 - ZR5) are for Subsection 1, etc. The (ZRs) delay the CPU (A - H) Read Bank Selects, while the memory bank is being Read. The (ZRs) steer the Read Data to 1 of 8 (ZS) options by decoding the CPU (A - H) Read Bank Selects. The (ZR0) handles read data bits (2^2, 2^1, 2^0) of Subsection 0, while (ZR1) handles bits (2^5, 2^4, 2^3), and (ZR2) handles bits (2^8, 2^7, 2^6), etc.

(ZS0, ZS1, ZS2, ZS3, ZS4, ZS5, ZS6, ZS7) Options

The (ZS) options are called the CPU Subsection Selects. There is one (ZS) per CPU per module. (ZS0) receives an SS Select Code from CPU 0 and selects 9 bits of data from 1 of 8 subsections. (ZS1) does the same for CPU 1, etc. The (Zs's) then send the 9 bits of read data to their particular CPU. The (ZSs) also perform a 1 to 8 Outboard fanout on subsection Read Select bits (2^2, 2^1, 2^0) for all CPUs.

(ZU0, ZU1, ZU10, ZU11, ZU20, ZU21, ZU30, ZU31) Options

The (ZU) options handle 2 address bits and 1 data bit each. There is one (ZU) per subsection. The (ZU) options perform the same functions as the (ZM) options, except that the (ZUs) receive the true, rather than the inverted, GOSS and Bank Select Codes. Like the (ZMs), the (ZUs) assist in the GOSS fanout on each module.

Hardware Trng.
YM15/16A J.E.S.

(ZV0, ZV1, ZV20, ZV21) Options

The (ZV) options each handle 1 Data bit, the Chip Select, and the Abort signal. There is one (ZV) for subsection 0, 1, 4, and 5. Since there are two (64K x 1) memory chips per bit, or 144 chips per 72-bit word, Chip Select 0 selects the lower 72 chips, and Chip Select 1 selects the upper 72 chips. When the Abort signal is present the Chip Selects are forced to zeroes, preventing a Write operation from completing, or during a Read, causing zeroes to be read from memory. The (ZV) options also perform a 1 to 2 fanout of Master Clear, 3 CP Write Enable, and Bank Busy (2^1, 2^0) to the two (ZX) options per subsection.

(ZW1, ZW2, ZW11, ZW12, ZW21, ZW22, ZW31, ZW32) Options

The (Zw) options perform the same functions as the (ZM) options, except that the (ZWs) receive a true GOSS and Bank Select Code. There is one (ZW) used per subsection. Each (ZW) contains 2 bits of data of the 9 bits per module. The (ZWs) also perform a 1 to 8 Outboard fanout on the address and controls to the eight modules within a section for all CPUs.

(ZX0, ZX1, ZX2, ZX3, ZX10-ZX13, ZX20-ZX23, ZX30-ZX33) Options

The (ZX) options perform the Subsection Conflict Check. There are two (ZX) options per subsection; (ZX0) checks for subsection conflicts on Banks (0 - 3), while (ZX1) checks for subsection conflicts on Banks (4 - 7), etc. The (ZX0, ZX1) are the control portion of the memory module. When a CPU requests a reference for a specific bank, it may have to wait for that bank to drop busy. Once the CPU gets the request for a reference, it then has to compete with the other CPUs for the bank. Typically, the CPU with the lowest I term value in the subsection has the highest priority for the bank. Once the CPU finally gets its request honored, the CPU will hold the bank busy for 5 CPs. The (ZX) option then generates a Bank (0 - 7) Select Code which assigns a particular CPU to a specific bank. A Go Read CPU (A - H) is generated when there is no Write Reference. Read Select bits (2^1, 2^0) are generated for CPU (A) only, and are sent to the (ZR) options. Read Select bits for CPUs (B - H) are done on the (ZY0, ZY1, ZN0, ZN1) options for Subsection 0.

(ZY0, ZY1, ZY2, ZY3, ZY10-ZY13, ZY20-ZY23, ZY30-ZY33) Options

The (ZY) options handle 3 address bits and supply two CPU Read Bank Selects. (ZY0) handles address bits (2^2, 2^1, 2^0) and CPU (E) Read Banks Selects while (ZY1) handles address bits (2^5, 2^4, 2^3) and CPU (B/F) Read Bank Select for Subsection 0. The (ZY) options will latch and hold the 3 address bits from the various CPUs. The address bits are then steered to the bank determined by the decode of the Bank (0 - 7) Select Code received from the (ZX) options. The Bank (0 - 7) Select Code assigns a particular CPU to the bank which was initially requested for by the (ZX) options. The (ZYs) receive a true GOSS and CPU-Select Code, similar to the (ZU) options.

Hardware Trng.
YM15/17 J.E.S.

(ZZ) Option

The (ZZ) option identifies the I terms coming into a group of eight memory chips , and R terms of the data leaving the memory chip. Coming into the memory chips are Address, Write Enable, Chip Select, and 1-bit of data, when using the (64K x 1) ECL 100K compatible memory chips.

CRAY Y-MP MEMORY
(64K x 1) ECL

GENERAL

SIZE:	32 million words
BANKS:	256 Banks
SECTIONS:	4 Sections
SUBSECTIONS:	8 per Section
BANK PER SECTION:	64 Banks
BANK PER SUBSECTION:	8 Banks
MEMORY CHIP:	64K x 1 ECL RAM 15 nsec access, 100K compatible
CPU ACCESS:	4 ports per CPU These share one physical path into memory
MODULE PER SECTION:	8 modules per section each has a 9-bit slice, each has 8 CPU paths into memory
SECTION ACCESS:	The same CPU can go back to the same Subsection every 5 CPs or more. All 8 CPUs can go to the same Subsection as long as they are going to different Banks.

Hardware Trng.
YM15/18 J.E.S.

CRAY Y-MP MEMORY DOCUMENTATION

PCTAB Central Processing Unit (CPU)

PCTAB CPU documents connections between options and between the options and edge connectors on the CPU module. This document lists all of the options in alphabetical and numerical order. The connectors are also listed in numerical order. The connector documentation is found after the listing of options.

PCTAB CPU lists all of the I and R terms specific to each option and connector. Accompanying this information is the source/destination of the signal for each I and R term.

CPU Jumper Manual

CPU jumper manual documents the physical location and type of each jumper pin used on the CPU to transfer a signal from one printed circuit (PC) board to another.

PCTAB Memory

PCTAB memory documents option to option, option to edge connector, and option to memory chip connections on the memory module. The options and memory chips are listed in alphabetical and numerical order. The connectors are documented following the option/memory chip listing.

PCTAB memory lists the source of the I terms and the destination of the R terms for each option, memory chip, and edge connector.

Memory Jumper Manual

Memory jumper manual documents physical location of each jumper pin used on the memory module. It also documents the type of jumper pin used at each location.

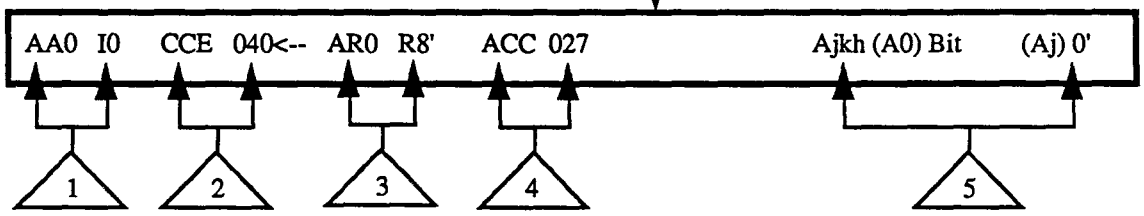
Wire tabs

Wire tabs document the connections between modules in the mainframe. The modules are listed in numerical order dictated by their physical location in the mainframe. It lists the source of the I terms and destination of the R terms for each connector used on a module.

PCTAB CPU

CHIP COPY: AA0 LOCATION: CCE OPTION TYPE: AA PCTAB P/N 10178600 REV. A FOR CPU4 MODULE

AA0	I0	CCE	040<--	AR0	R8'	ACC	027	Ajkh (A0) Bit	(Aj) 0'
AA0	I1	CCE	041<--	AR0	R9'	ACC	029	Ajkh (A0) Bit	(Aj) 1'
AA0	I2	CCE	043<--	AR0	R10'	ACC	031	Ajkh (A0) Bit	(Aj) 2'
AA0	I3	CCE	044<--	AR0	R11'	ACC	034	Ajkh (A0) Bit	(Aj) 3'
AA0	I4	CCE	045<--	AR0	R12'	ACC	087	Ajkh (A0) Bit	(Aj) 4'
AA0	I5	CCE	046<--	AR0	R13'	ACC	084	Ajkh (A0) Bit	(Aj) 5'
AA0	I6	CCE	047<--	AR0	R14'	ACC	082	Ajkh (A0) Bit	(Aj) 6'
AA0	I7	CCE	050<--	AR0	R15'	ACC	078	Ajkh (A0) Bit	(Aj) 7'



1 OPTION INPUT - The option is (AA0). The signal enters the option on I0.

2 PHYSICAL LOCATION - The (AA0) option is physically located on board C, column C, row E.

CCE
- Row (short side of module)
- Column (long side of module)
- Board designator

The input I0 is pin 40 on (AA0) option.

3 SOURCE OF SIGNAL - The signal sent to (AA0) I0 comes from (AR0) R8'.

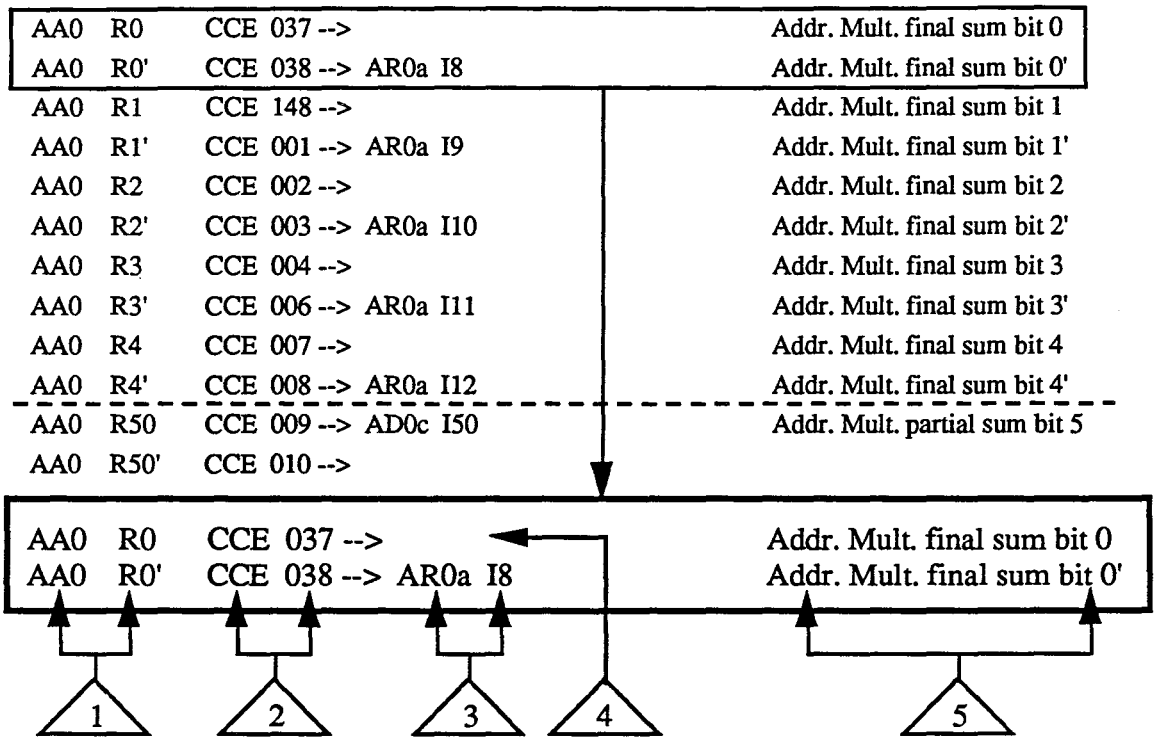
4 PHYSICAL LOCATION - The (AR0) option is physically located on board A, column C, row C.

The output R8' leaves the option via pin 27.

5 DESCRIPTION OF THE SIGNAL

YM36/02

PCTAB CPU (continued)



1 SOURCE OF SIGNAL - Address multiply final sum bit $2^{0'}$ leaves the (AA0) option as term R0'.

2 PHYSICAL LOCATION - The (AA0) is physically located on board C, column C, row E. The output term R0' leaves the option via pin 38.

3 DESTINATION OF THE SIGNAL - The address multiply final sum bit $2^{0'}$ is sent to the (AR0). The signal enters the option as term I8.

NOTE

The lower case letter following the option name specifies which PC board the option resides on. (Example: AR0a)

---

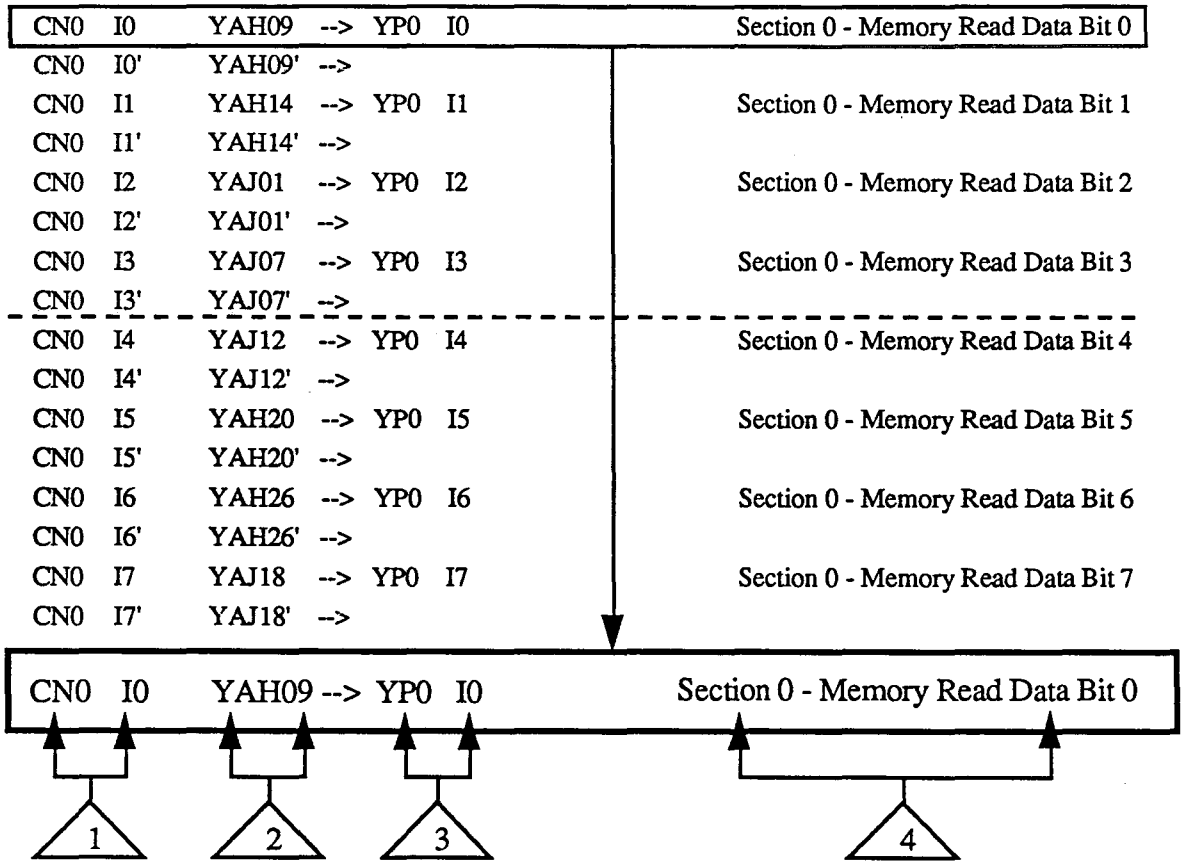
4 UNUSED SIGNAL - Since there is no destination listed for this signal, it is not being used.

5 DESCRIPTION OF THE SIGNAL

YM36/03

PCTAB CPU (continued)

CONNECTOR: CN0 PCTAB P/N 10178600 REV. A FOR CPU4 MODULE PAGE 844



1 CONNECTOR - Connector CN0 is being used to bring the read data bit 2^0 onto the module. The signal comes onto the module as term I0.

2 PHYSICAL LOCATION - CN0 is physically located on the Y axis, board A , row H. I0 enters the connector via pin 9.

3 DESTINATION OF THE SIGNAL - Read data bit 2^0 is sent from the connector to the (YP0) option. This signal enters the option as term I0.

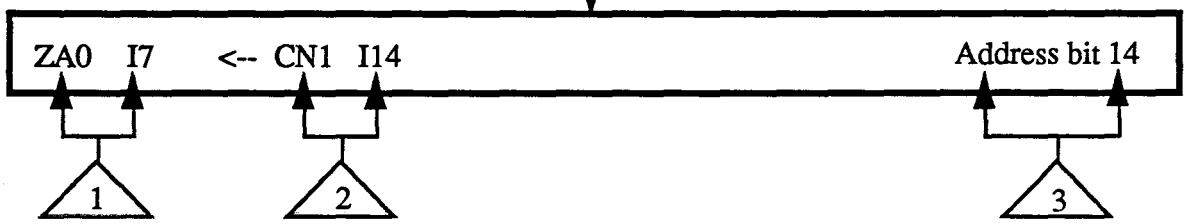
4 DESCRIPTION OF THE SIGNAL

YM36/04

PCTAB Memory

CHIP COPY: ZA0 LOCATION: AGE OPTION TYPE: ZA PCTAB P/N 31142015 09/06/88 13:22:29 PAGE 9

ZA0	I0	<-- CN3	I15	address bit 15
ZA0	I1	<-- CN3	I14	address bit 14
ZA0	I2	<-- CN3	I13	address bit 13
ZA0	I3	<-- CN2	I15	address bit 15
ZA0	I4	<-- CN2	I14	address bit 14
ZA0	I5	<-- CN2	I13	address bit 13
ZA0	I6	<-- CN1	I15	address bit 15
ZA0	I7	<-- CN1	I14	address bit 14



1 OPTION INPUT - Address bit 2^{14} is sent to the (ZA0) option. The signal arrives on the option as term I7.

2 SOURCE OF THE SIGNAL - The signal comes from a connector called CN1. The signal leaves the connector as I14.

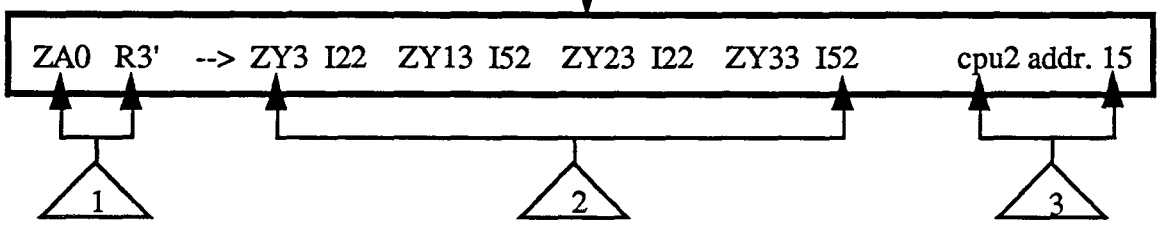
3 DESCRIPTION OF THE SIGNAL

YM36/05

PCTAB Memory (continued)

CHIP COPY: ZA0 LOCATION: AGE OPTION TYPE: ZA PCTAB P/N 31142015 09/06/88 13:22:29 PAGE 9

ZA0	R0	-->	ZN1	I32	ZN11	I42	ZN21	I32	ZN31	I42	cpu3 addr. 15
ZA0	R0'	-->	ZY3	I32	ZY13	I42	ZY23	I32	ZY33	I42	cpu3 addr. 15
ZA0	R1	-->	ZN1	I31	ZN11	I41	ZY21	I31	ZN31	I41	cpu3 addr. 14
ZA0	R1'	-->	ZY3	I31	ZY13	I41	ZY23	I31	ZY33	I41	cpu3 addr. 14
ZA0	R2	-->	ZN1	I30	ZN11	I40	ZN21	I30	ZN31	I40	cpu3 addr. 13
ZA0	R2'	-->	ZY3	I30	ZY13	I40	ZY23	I30	ZY33	I40	cpu3 addr. 13
ZA0	R3	-->	ZN1	I22	ZN11	I52	ZN21	I22	ZN31	I52	cpu2 addr. 15
ZA0	R3'	-->	ZY3	I22	ZY13	I52	ZY23	I22	ZY33	I52	cpu2 addr. 15



1 SOURCE OF THE SIGNAL - CPU2 address bit 2^{15} leaves the (ZA0) option as term R3'.

2 DESTINATION OF THE SIGNAL - The signal is sent to four different options: (ZY3), (ZY13), (ZY23), and (ZY33). This signal enters (ZY3) and (ZY23) as term I22.
On (ZY13) and (ZY33) it enters the options as term I52.

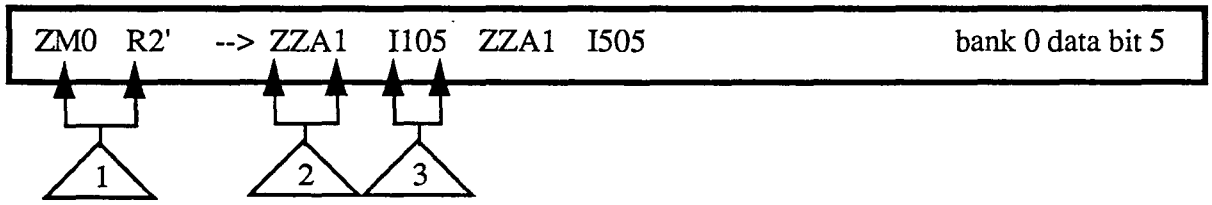
3 DESCRIPTION OF THE SIGNAL

YM36/06

PCTAB Memory (continued)

CHIP COPY: ZM0 LOCATION: ADE OPTION TYPE: ZM PCTAB P/N 31142015 09/06/88 13:22:32 PAGE 26

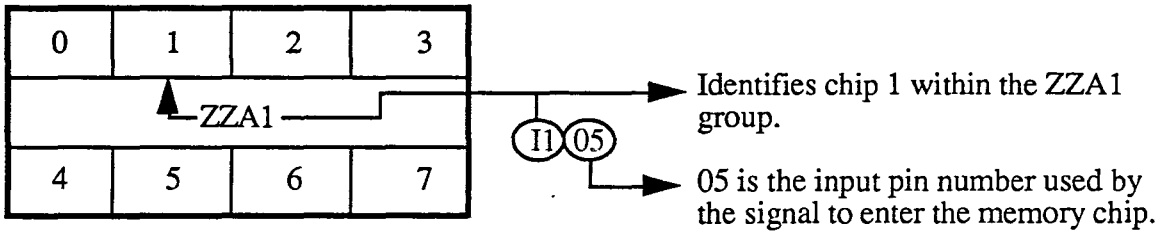
ZM0 I80	<-- CN4 I30						goss 0
ZM0 I81	<-- CN5 I30						goss 0
ZM0 I82	<-- CN6 I30						goss 0
ZM0 I83	<-- CN7 I30						goss 0
ZM0 I98	<-- T00 R27						clock
ZM0 I99	<-- T00 R27						clock
ZM0 R0	--> ZZA2 I608	ZZA2 I208	ZZA2 I108	ZZA1 I608	ZZA1 I208		
	--> ZZA1 I108	ZZA0 I608	ZZA0 I208	ZZA0 I108			
ZM0 R0'	--> ZZA2 I508	ZZA2 I408	ZZA2 I8	ZZA1 I508	ZZA1 I408		
	--> ZZA1 I8	ZZA0 I508	ZZA0 I408	ZZA0 I8			
ZM0 R1	--> ZZA2 I612	ZZA2 I212	ZZA2 I112	ZZA1 I612	ZZA1 I212		
	--> ZZA1 I112	ZZA0 I612	ZZA0 I212	ZZA0 I112			
ZM0 R1'	--> ZZA2 I512	ZZA2 I412	ZZA2 I12	ZZA1 I512	ZZA1 I412		
	--> ZZA1 I12	ZZA0 I512	ZZA0 I412	ZZA0 I12			
ZM0 R2	--> CN40 I22						ss0 bank 0 wd 5
ZM0 R2'	--> ZZA1 I105	ZZA1 I505					bank 0 data bit 5



1 SOURCE OF THE SIGNAL - Bank 0 data bit 5 leaves (ZM0) option as term R2'.

2 GROUP NAME - Bank 0 data bit 5 is sent to a group of memory chips called ZZA1. The ZZA1 group contains eight memory chips.

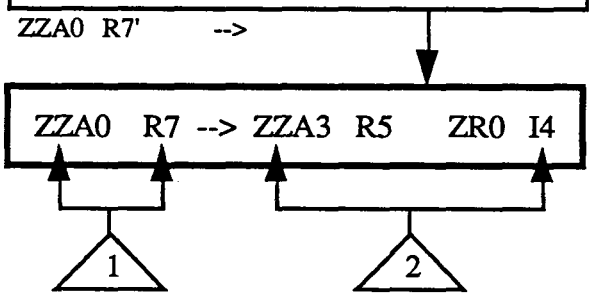
3 CHIP AND INPUT DESIGNATOR - I105 can be broken into two parts:



YM36/07

PCTAB Memory (continued)

```
ZZA0 R0      --> ZZA0 R2      ZR0 I0
ZZA0 R0'     -->
ZZA0 R1      --> ZZA0 R5      ZR0 I2
ZZA0 R1'     -->
ZZA0 R2      --> ZZA0 R0      ZR0 I0
ZZA0 R2'     -->
ZZA0 R3      --> ZZA0 R1      ZR0 I3
ZZA0 R3'     -->
-------------------------------------
ZZA0 R4      --> ZZA0 R6      ZR0 I1
ZZA0 R4'     -->
ZZA0 R5      --> ZZA0 R1      ZR0 I2
ZZA0 R5'     -->
ZZA0 R6      --> ZZA0 R4      ZR0 I1
ZZA0 R6'     -->
ZZA0 R7      --> ZZA3 R5      ZR0 I4
ZZA0 R7'     -->
```



1 SOURCE OF THE SIGNAL - The read data bit leaves the group of memory chips called ZZA0. R7 specifies that chip 7 of the group is being used.

2 DESTINATION OF THE SIGNAL - ZZA0 chip 7 sends the read data bit to the (ZR0) option. The read data bit enters (ZR0) as term I4. Also listed as a destination of this read data bit is a memory chip, ZZA3 R5. The reason this memory chip is listed is because the two outputs of ZZA0 R7 and ZZA3 R5 are wire-ORed together.

NOTE

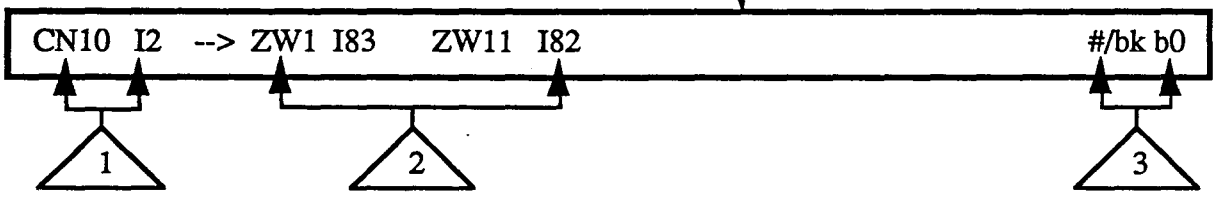
ZZA0 R7 and ZZA3 R5 handle the same data bit. The difference between the two chips is that one of the chips is for chip select 0 and the other is for chip select 1.

YM36/08

PCTAB Memory (continued)

CONNECTOR: CN10 PCTAB P/N31142015 09/06/88 13:24:22 PAGE 841

```
CN10 I0    --> ZQ0 I81    ZQ10 I80    ZQ20 I81    ZQ30 I81        bk b2
CN10 I0'   --> ZQ0 I80    ZQ10 I81    ZQ20 I80    ZQ30 I80        bk b2'
CN10 I1    --> ZQ0 I82    ZQ0  I83                                goss 0
CN10 I1'   --> ZW1 I80                                            goss 0
CN10 I2    --> ZW1 I83    ZW11 I82                                #/bk b0
CN10 I2'   -->                                                    #/bk b0
CN10 I3    --> ZW1 I81                                            a0/#
CN10 I3'   -->                                                    a0/#
CN10 I4        ZO0 I80    ZO0  I81                                #/abort
CN10 I4'   -->                                                    #/abort
CN10 I5    --> ZO0 I82                                            (a0)/#
CN10 I5'   -->                                                    (a0)/#
```



1 CONNECTOR - The connector CN10 is being used to bring bank bit 2^0 onto the memory module. The term used for this signal is I2.

2 DESTINATION OF THE SIGNAL - Bank bit 2^0 is sent to two options, (ZW1) and (ZW11). The signal enters (ZW1) as I83. On (ZW11) this signal is I82.

3 DESCRIPTION OF THE SIGNAL - #/bk b0
a/ b

MEM0	A
MEM1	A
MEM2	B
MEM3	B
MEM4	B
MEM5	B
MEM6	A
MEM7	A

This comment can be used to describe two different signals. The "#" is the first comment which will be called "A". Bk b0 is the second comment which will be called "B". The "#" symbolizes an unused signal. CN10 I2 is not being used on MEM0, MEM1, MEM6, or MEM7. These four modules use the comment in the "A" position. CN10 I2 is being used by bk b0 on MEM2, MEM3, MEM4, and MEM5. These four modules use the comment in the "B" position.

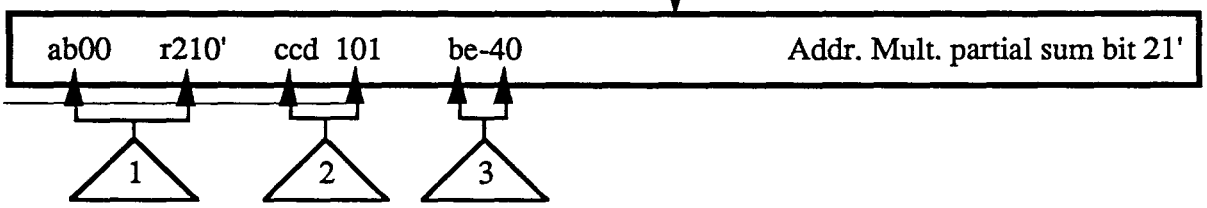
YM36/09

NOTE

The layout is the same for both memory and the CPU.

03/29/89 Y-MP JUMPER LISTING P/N 31194950 REVISION A FOR CPU4 MODULE PAGE 1

OPTION	TERM	LOC PIN	JUMPERS	DESCRIPTION
aa00	r000'	cce 038	cf-35	Addr. Mult. final sum bit 0'
aa00	r001'	cce 001	dg-29	Addr. Mult. final sum bit 1'
aa00	r002'	cce 003	dg-44	Addr. Mult. final sum bit 2'
aa00	r003'	cce 006	dg-22	Addr. Mult. final sum bit 3'
aa00	r004'	cce 008	cf-05	Addr. Mult. final sum bit 4'
ab00	r210'	ccd 101	be-40	Addr. Mult. partial sum bit 21'
ab00	r211'	ccd 103	be-36	Addr. Mult. partal sum bit 21'
ab00	r212'	ccd 106	bd-33	Addr. Mult. partial sum bit 21'



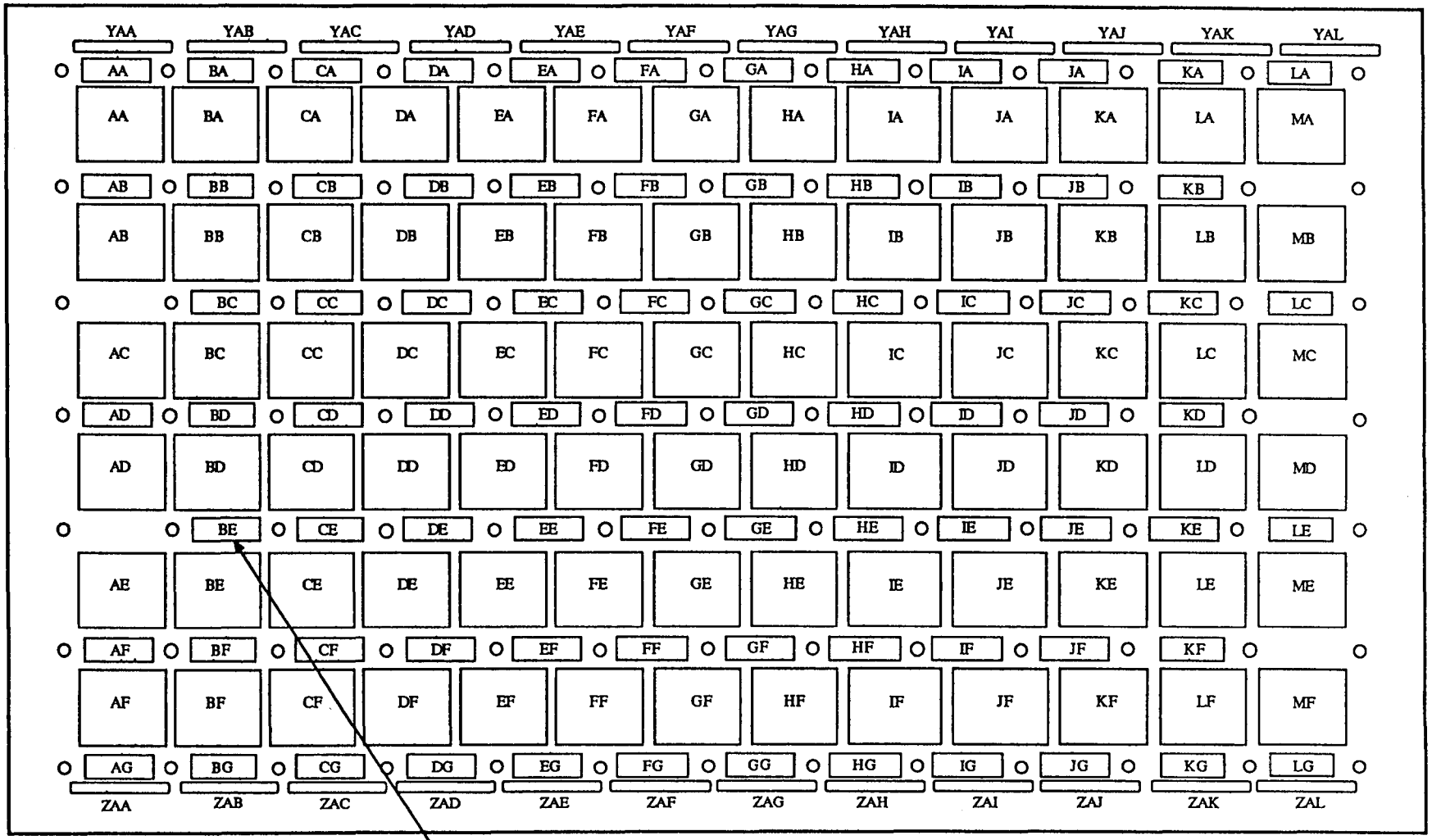
1 SOURCE OF SIGNAL - Address multiply partial bit 21' leaves the (AB0) option at term r210'.

2 PHYSICAL LOCATION - (AB0) is physically located on board C, column C, row D. R210' leaves the option via pin 101.

3 JUMPER PIN LOCATION - This signal from (AB0) r210' is being sent off the PC board to another PC board of the module. To do this a jumper pin is used. The jumper pin used for this example is physically located at column B, row E.

The location BE consists of 48 jumper pins. The pin used to send Address multiply partial sum bit 21' to another PC board is jumper pin 40.

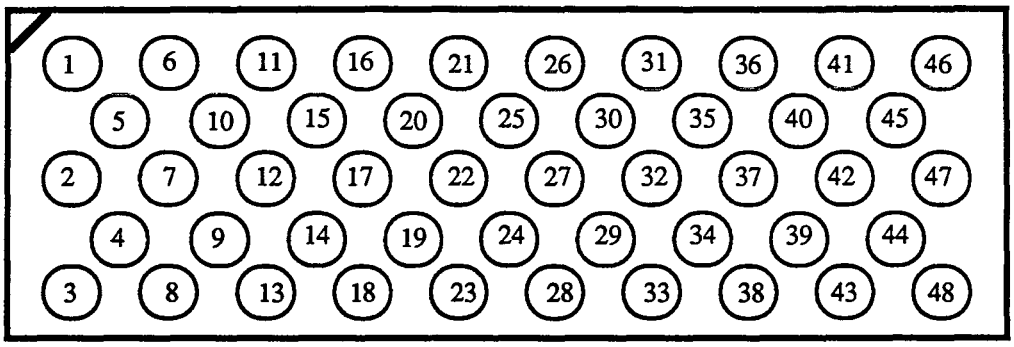
YM36/10



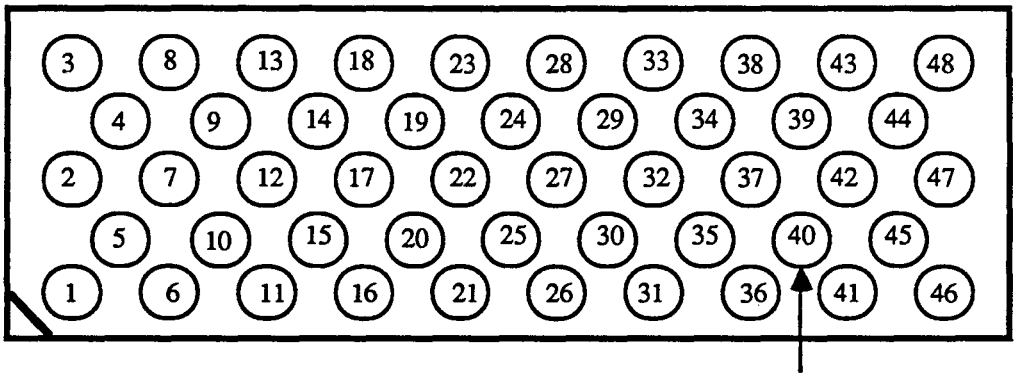
This map shows the physical locations of the jumper pins.
For the example BE-40, the group of jumper pins are located here.

CRAY Y-MP PHYSICAL LOCATION MAP FOR A AND C BOARDS

CRAY Y-MP JUMPER BLOCK LAYOUT



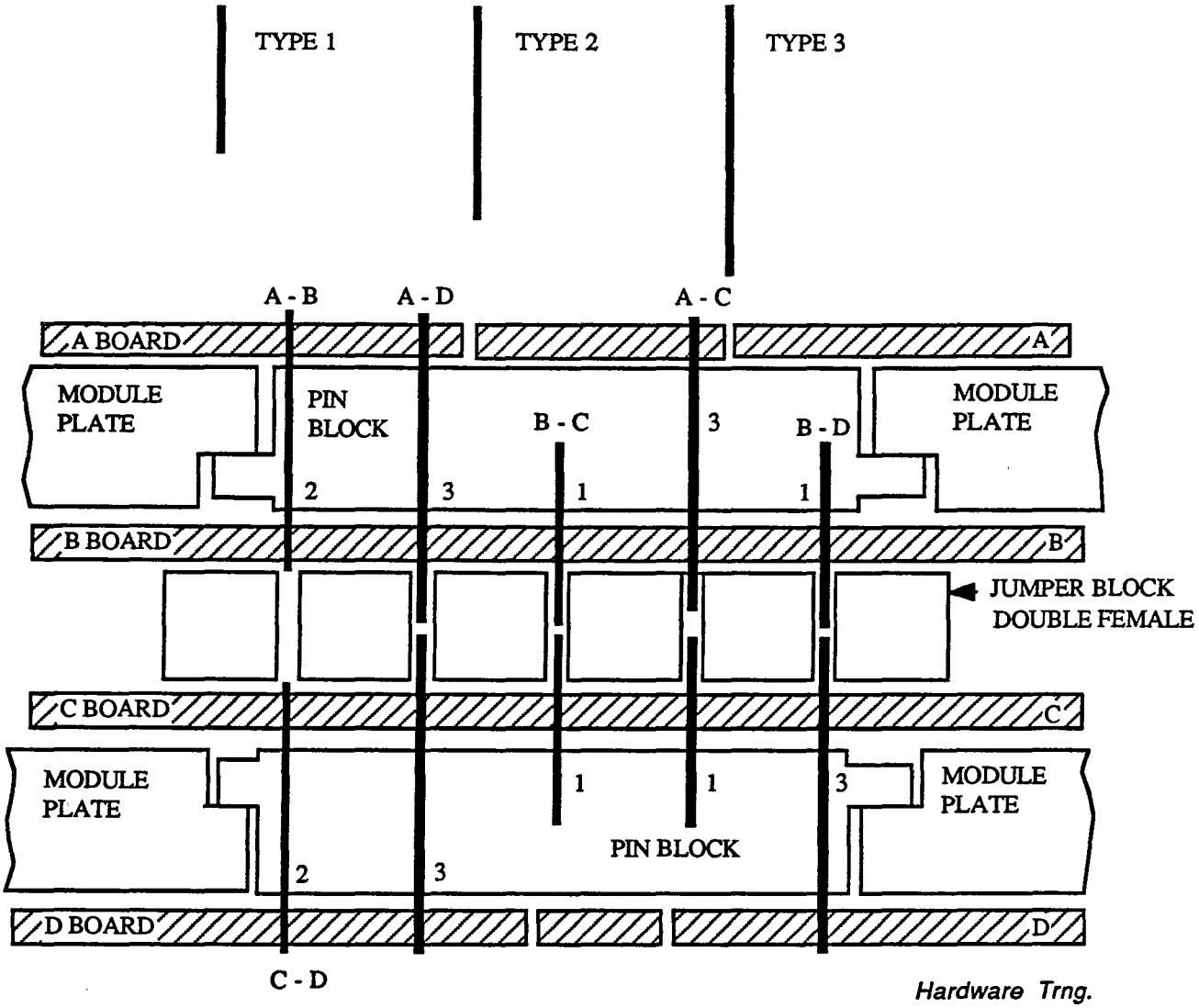
The jumper block layout shows the numbering scheme of the jumper pins within one group. The dark line at the top left hand corner designates pin 1. This placement of pin 1 is true if looking at the A or C board of the module. If looking at the B or D board of the module, pin 1 would be located at the lower left hand corner. The jumper layout of the B and D board looks like the diagram below.



For the example BE-40, pin 40 is located here if looking at the B or D boards.

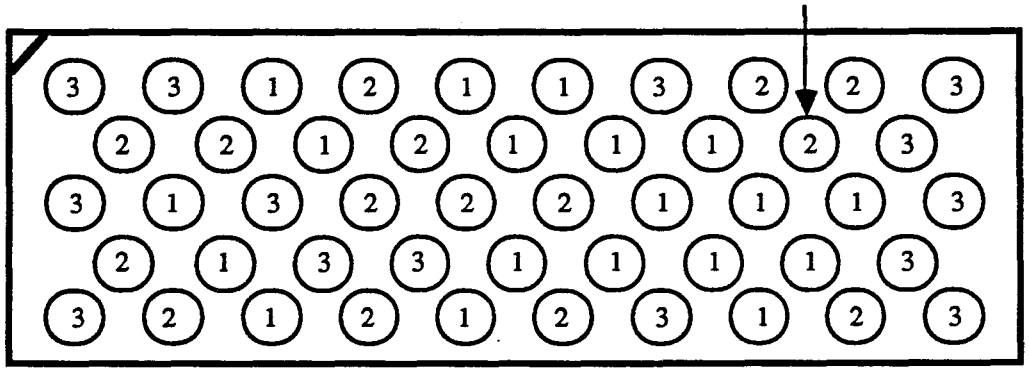
YM35/06

The next section of the jumper pin manual lists the type of jumper pins used at each location. There are three types of jumper pins: type 1, type 2, and type 3.



Hardware Trng.
A-6950 J.E.S.

For the example BE-40, the type of jumper pin used for pin 40 on the C/D half of the module is type 2.

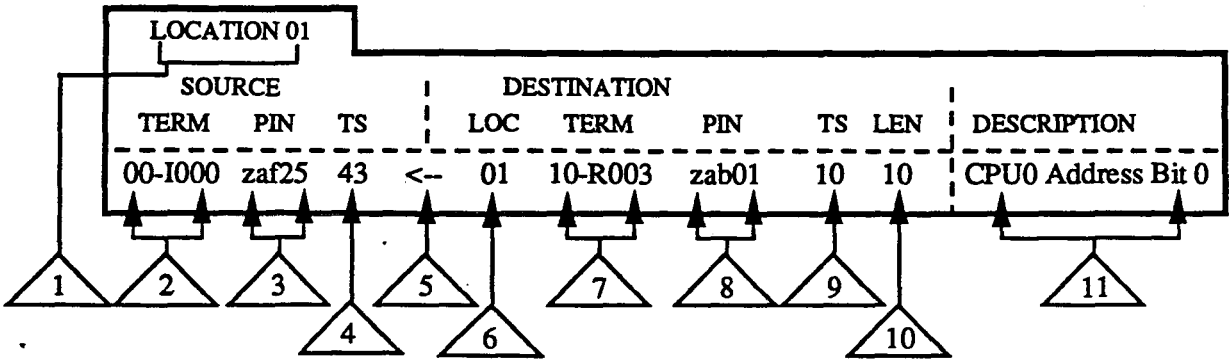


BOARD C
BLOCK BE

YM35/07A

Wire Tabs

LOCATION 01			CRAY Y-MP WIRE TABS S/N 1014					PAGE 1
SOURCE				DESTINATION				
TERM	PIN	TS	LOC	TERM	PIN	TS	LEN	DESCRIPTION
00-I000	zaf25	43	<-- 01	10-R003	zab01	10	10	CPU0 Address Bit 0
00-I001	zaf24	42	<-- 01	10-R015	zbb27	10	11	CPU0 Address Bit 1
00-I002	zaf23	44	<-- 01	10-R029	zcb01	10	12	CPU0 Address Bit 2
00-I003	zbg08	44	<-- 01	10-R041	zdb27	11	12	CPU0 Address Bit 3
00-I004	zbg07	44	<-- 01	10-R005	zaf12	10	12	CPU0 Address Bit 4
00-I005	zbg06	45	<-- 01	10-R018	zbe18	10	12	CPU0 Address Bit 5
00-I006	zaf01	42	<-- 01	10-R031	zcf12	10	10	CPU0 Address Bit 6
00-I007	zaf02	42	<-- 01	10-R044	zde18	10	10	CPU0 Address Bit 7



1 MODULE LOCATION - Location 01 specifies the module seated at physical location 1 in the chassis of the mainframe. Location 1 in the CRAY Y-MP/832 mainframe seats MEM0 in Section 0 of the memory.

2 TERM - The term is the connector being used by the signal. For this example the connector is CN0. The term is I0.

3 PIN - The pin is the physical location of CN0 I0. CN0 I0 is located on the Z axis, board A, row F, pin 25.

4 TS - The time segment (TS) specifies when the signal arrives on the module. For this example, CPU0 address bit 2^0 arrives on the module at TS 43.

5 ARROW - The arrow designates the direction of the signal. The arrow always points to the destination of the signal.

NOTE

Ignore the source and destination comments of the heading because the comments are not always correct.

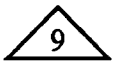
---

6 LOC. - Location (Loc.) specifies the physical location of the module in the mainframe where the signal came from.

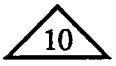
A-8523

TERM - The term is the connector used on the module. For this example the connector is CN10 R3.

PIN - This is the physical location of CN10 R3. CN10 R3 is located on the Z axis, board A, row B, pin 1.



TS - This is the TS in which the signal CPU0 address bit 2^0 leaves the module. This signal leaves the module at TS 10.



LEN - LEN specifies the length of the wire used to transfer the signal. The wire used to transfer address bit 2^0 is 10 inches in length.

DESCRIPTION OF THE SIGNAL

A-8524

CRAY Y-MP MEMORY DOCUMENTATION

PCBDA, PCBDB, PCBDC, PCBDD

Documents where the memory options are located called "chip map" and also contains a "connector map" which tells the loading on the "Z" and "Y" edge connectors. PCBDA loads board A, PCBDB loads board B, PCBDC loads board C and PCBDD loads board D.

PCLDA, PCLDB, PCLDC, PCLDD

Documents the loading of Data, Address and Control from the edge connectors to the logic chips. Each CPU's path into the memory module is documented. PCLDA handles CPU A/B; PCLDB handles CPU C/D; PCLDC handles CPU E/F; and PCLDD handles CPU G/H. PCLDA loads board A, PCLDB loads board B, PCLDC loads board C and PCLDD loads board D when looking at a particular option.

SUBSECTION DATA A - D

Documents the Writting or Reading of the data into each memory chip within the 8 banks per subsection. Subsection Data A contains subsection 0, 1; Subsection Data B contains subsection 2, 3; Subsection Data C contains subsection 4, 5 and Subsection Data D contains subsection 6, 7.

BANK SUBSECTION 0 - 7

Documents the loading of the Address and Control into each memory chip within the 8 banks per subsection 0-7.

MPT ZM-ZZ

Documents what comes into each pin of the 148 pin chip for options ZM-ZZ.

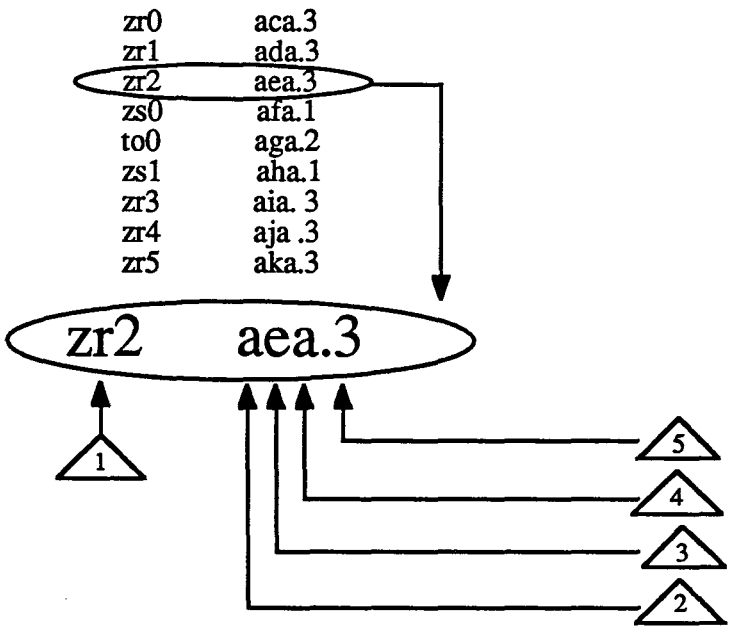
OPTIONS ZA-ZZ BOOLEAN

Documents the Boolean equation used inside the logic chips. The Boolean equations are translated into an arrangement of macro cells which perform logical functions for the computational process.

Hardware Trng.
YM15/01 J.E.S.

$pcbda 9-10-86

$chip map



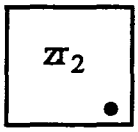
1 OPTION TYPE - In this example the option is a (zr2).

2 BOARD DESIGNATOR - The (zr2) option is found on the A board.

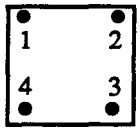
3 COLUMN DESIGNATOR - The (zr2) option is on the A board in Column E, or the longside of the module.

4 ROW DESIGNATOR - The (zr2) option is on the A board in Column E, Row A. Row A is on the short side of the module.

5 PIN ALIGNMENT - The (zr2) option has alignment .3. This puts alignment asterisk in the lower right corner on the memory module, if the coolant connections are to your left.

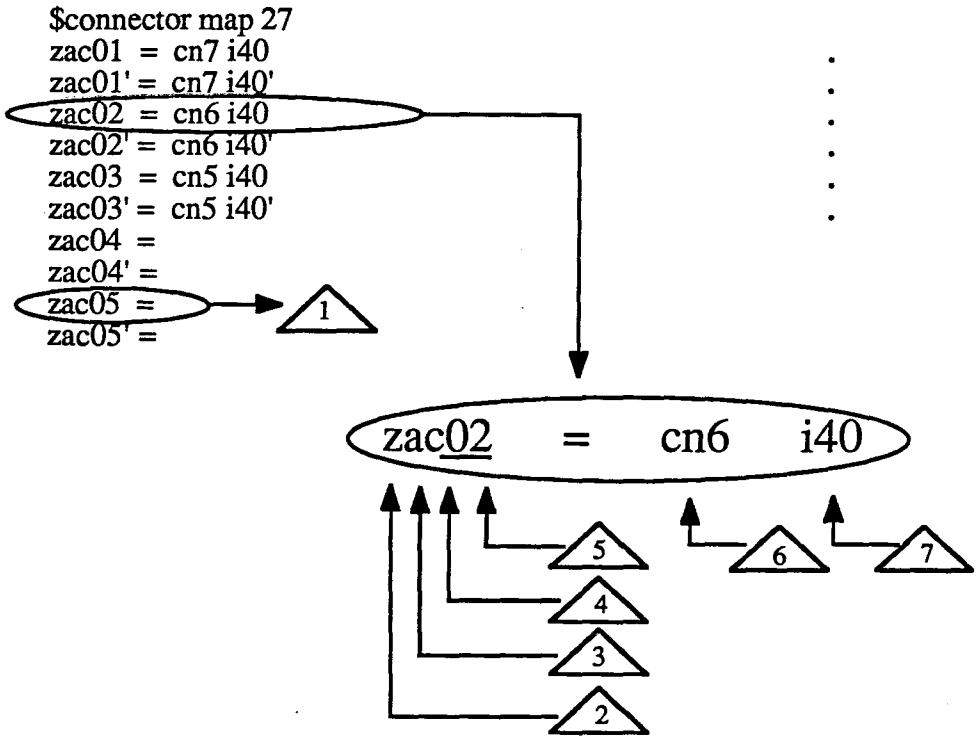


In general the placement is



Hardware Trng.
A-6258A J.E.S.

PCBDA $ CONNECTOR MAP 27



1 CONNECTOR MAP 27 - Unused pin on the edge connector, the edge connector has 27 pins.

2 AXIS DESIGNATOR - The Edge Connector is located on the "z" axis or it can be the "y" axis.

3 BOARD DESIGNATOR - The Edge Connector is found on the A board. The letters would range from A to D for boards A through D.

4 COLUMN DESIGNATOR - Read as Board A, Column C. Identifing a 27 pin Edge Connector on the "z" axis of the memory module.

5 PIN DESIGNATOR - Board A, Column C, pin 02. Pin 02 is a true pin, pin 02' would be the false pin.

6 PINS LOGICAL VARIABLE - Identifies what the pin is being used for. In this case pin 02 is used by CPU 6.

7 PIN BOOLEAN TERM - Pin 02, on Edge Connector C, has an input Boolean term i40 from CPU 6.

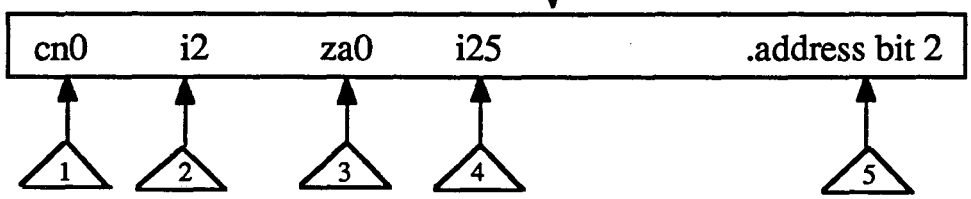
Hardware Trng.
YM15/02 J.E.S.

PCLDA - PC LOAD FILE

```
pcload:pclda
rev:   0
date:  09-19-86
title: pc load file for cpu0 , 1 and a board

$net list cn0  **************  cpu0 ************************

cn0 i0    za0  i27                                    .address bit 0
cn0 i0'                                                .
cn0 i1    za0  i26                                    .address bit 1
cn0 i1'                                                .
cn0 i2    za0  i25                                    .address bit 2
cn0 i2'                                                .
```



1 CONNECTOR NUMBER - Connector Number 0 = cn0

Connector Number 7 = cn7

cn0 - cn7 for the 8 CPU load paths on to and off from the memory module.

2 EDGE CONNECTOR TERM - Input term into the module from CPU 0, which comes into the edge connector as term (i2). The letter "i" for input, or the letter "r" for output.

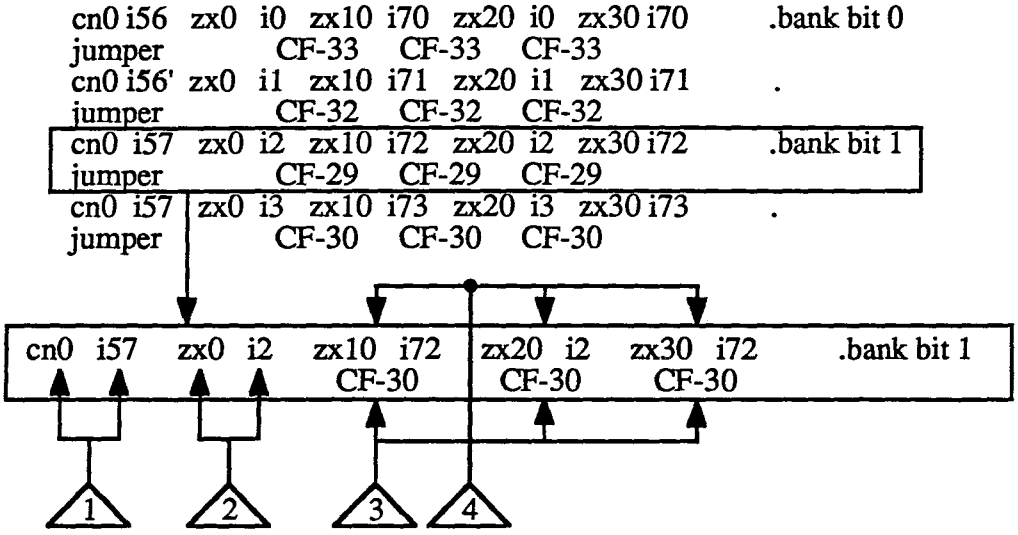
3 OPTION TYPE - CPU 0 will come into the (za0) option type.

4 OPTION INPUT TERM - I25 is the input term into the (za0) option.

5 PCLDA COMMENT - I2 coming in from the Edge Connector is Address bit 2 from CPU 0 goes into the (za0) option as i25.

Hardware Trng.
YM15/03A J.E.S.

PCLDA - PC Load File (continued)



1 CPU INPUT - CPU 0 Bank Bit 1 signal comes into the memory module as i57.

2 OPTION INPUT - The Bank Bit 1 signal comes into the (zx0) option as i2. Because the original Bank Bit 1 signal arrived on the A board, it will go directly to the (zx0) option.

3 JUMPER LOCATION - To send the Bank Bit 1 signal to B, C and D boards a type 3 jumper is needed. This jumper is located in Column C, Row F, pin number 30.

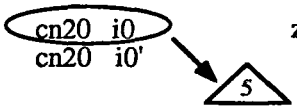
CF-30
- row - short side of module
- column - long side of module

4 BOARD DESIGNATOR - The (zx10) option is located on the B board indicated by the "1" in the number 10, just as the (zx20) option is on the C board and the (zx30) is on the D board.

Hardware Trng.
YM15/04 J.E.S.

PCLDA - D (continued)

$ y connector fan-out : master clear



zs30 i80

.master clear

$ z connector fan-out inputs

cn10 i26 zq20 i82
cn10 i26' zw21 i80
cn10 i27 zw21 i81
cn10 i27'
cn10 i28 zo20 i80
cn10 i28'
cn10 i29 zo20 i82
cn10 i29'

zq20 i83

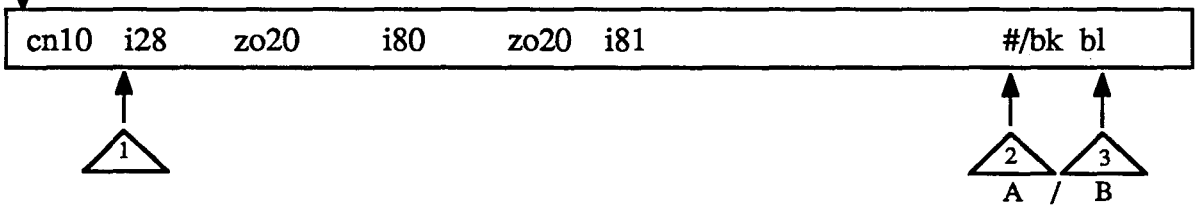
zo20 i81

.goss 4

4 → .a2/#

.#/bk bl

6 → .(a2)/#



1 cn10 i28 - cn10 i28 comes in on the "z" connector denoted by cn10.

2 Not Used - # symbolizes that when in a particular slot of the machine the particular term is not used.

Mem. 0, A
Mem. 1, A
Mem. 2, B
Mem. 3, B
Mem. 4, B
Mem. 5, B
Mem. 6, A
Mem. 7, A

The first two and last two are the same configuration, as are the middle four.

3 #/bk bl - Abbreviated, Bank bit 1. When in A position, cn 10 i28 is not used. When in B position, cn 10 i28 is Bank bit 1.

4 a2/# - Abbreviate for address 2 or address bit 2 when used in A's position.

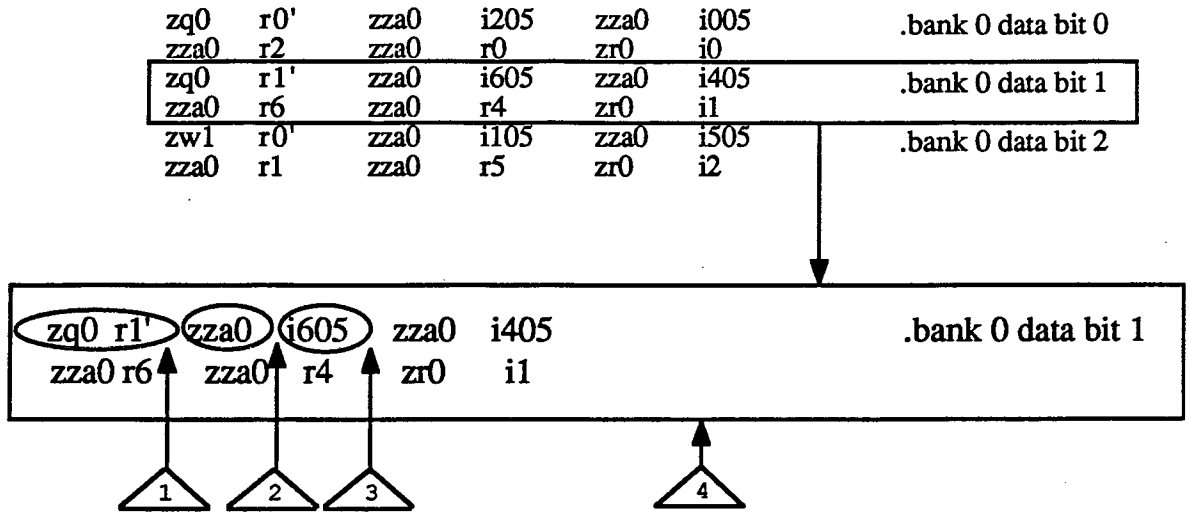
5 cn20 i0 - cn20 i0 comes in on the "y" connector denoted by cn20.

6 (a2)/# - (a2)/#, address bit 2 is used when in the A's position, a2 is in the inverted state shown by (a2).

Hardware Trng.
YM15/05 J.E.S.

Subsection Data A - D

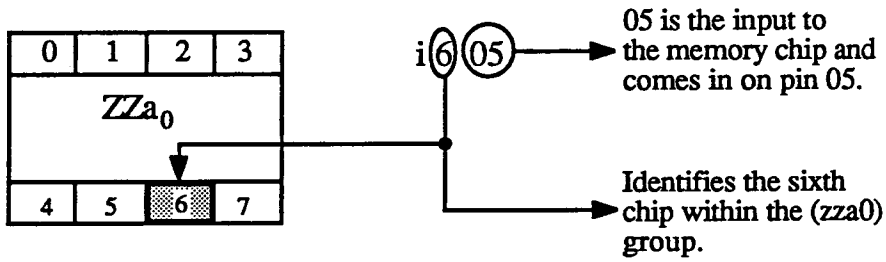
$ subsection 0 : data bits



1 ORIGINATION - Bank 0 data bit 1 leaves the (zq0) option as term r1'.

2 GROUP DESCRIPTION - Bank 0 bit 1 is sent to a group of memory chips called zza0. The zza0 group contains 8 memory chips.

3 CHIP AND INPUT DESIGNATOR - The i605 can be broken into two parts:

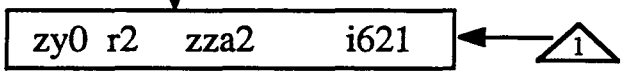


4 LINE READS AS - Bank 0 data bit 1 leaves the (zq0) option on r1'on a Write operation to the (zza0) group, chip 6, and (zza0) group, chip 4, and comes into chips 6 and 4 on pin 05. Bank 0 data bit 1 will leave (zza0) chip 6 as r6 on a Read operation and come into (zr0) option as i1. Bank 0 data bit 1 will leave (zza0) chip 4 as r4 and come into (zr0) option on i01. Depending on the Chip Selects either r4 or r6 is Read but not both, same as on a Write operation.

Hardware Trng.
YM15/06 J.E.S.

BANK SUBSECTION 0 - 7

zy0	r0	zza2	i619	zza2	i219	zza2	i119	zza1	i619	zza1	i219 &
		zza1	i119	zza0	i619	zza0	i219	zza0	i119		
zy0	r0'	zza2	i519	zza2	i419	zza2	i019	zza1	i519	zza1	i419 &
		zza1	i019	zza0	i519	zza0	i419	zza0	i019		
zy0	r1	zza2	i620	zza2	i220	zza2	i120	zza1	i620	zza1	i220 &
		zza1	i120	zza0	i620	zza0	i220	zza0	i120		
zy0	r1'	zza2	i520	zza2	i420	zza2	i020	zza1	i520	zza1	i420 &
		zza1	i020	zza0	i520	zza0	i420	zza0	i020		
zy0	r2	zza2	i621	zza2	i221	zza2	i121	zza1	i621	zza1	i221 &
		zza1	i121	zza0	i621	zza0	i221	zza0	i121		
zy0	r2'	zza2	i521	zza2	i421	zza2	i021	zza1	i521	zza1	i421 &
		zza1	i021	zza0	i521	zza0	i421	zza0	i021		

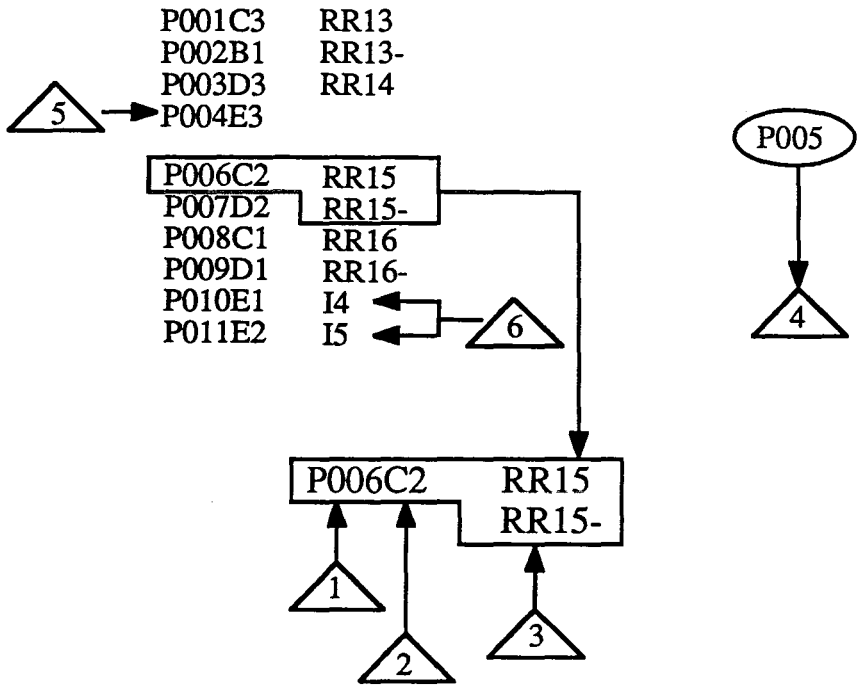


The Bank Subsection 0 - 7 reads the same as the Subsection Data A - D, except the Bank Subsection 0 - 7 documents Address and Control to the memory module as per Subsection 0 - 7. The Subsection Data A-D documents only the data per the module boards A - D.

1 This portion of Bank Subsection 0 would read as the (zy0) option outputs as r2, r2 is address bit 2^2 for bank (n+0). Address bit 2^2 or r2 goes to the (zza2) group, chip 6 and comes into the memory chip on pin 21.

MPT ZM-ZZ MAP TABLE

```
$$$$ OPTION ZM * DATE 07-11-86 * MPTBL ****
$$$$ DATE OF LAST CHANGE  07-11-86 ****
```



1 PIN NUMBER - P006 calls out pin 6 of the 148 pin package.

2 INTERNAL PIN ASSIGNMENTS - Internal chip pad C2 is in Column C, Row 2.

3 PIN TERM - Pin 6 is an output term from the "R" term meaning output. The output term is R15 true. In the case with R15-, R15- is the false output.

4 POWER/GROUND - Power/ground is sometimes right justified. P005 happens to be VCC0.

5 UNUSED PIN - An unused pin is left blank.

6 INPUT PINS - Input pins are identified by the letter "I" as in I4 or I5.

Hardware Trng.
YM15/08 J.E.S.

LOGICAL VARIABLES

Z AXIS

cn 0-7 ↓ ↘ (Connector Number) A - H on Memory Module	i0-16	Address
	i17	Go Write
	i18-19	Abort
	i20-28	Data in
	i30-37	GOSS 0-7
	i40-55	GOSS Bank Bit 2^1 , 2^0
	i56-63	Bank bit 1, 0 (four copies)
cn 10	i0-47	Fanout
	r0-51	
	r100-151	
	r200-251	
	r700-751	

Y AXIS

cn 0-7	i70-72	Subsection Readout Select
A-H	i0	Master Clear
cn 20	i1	3 CP Write Enable
	i2-3	Bank Busy Select
	i10-13	Clock Input
	i20-23	1-8 Fanout
	r0-8	Read Data
	r10-13	
	⋮	
	r70-73	

IN GENERAL

cn 30	I/O channels
cn 40	Deadstart Panel
cn 50	Test Points

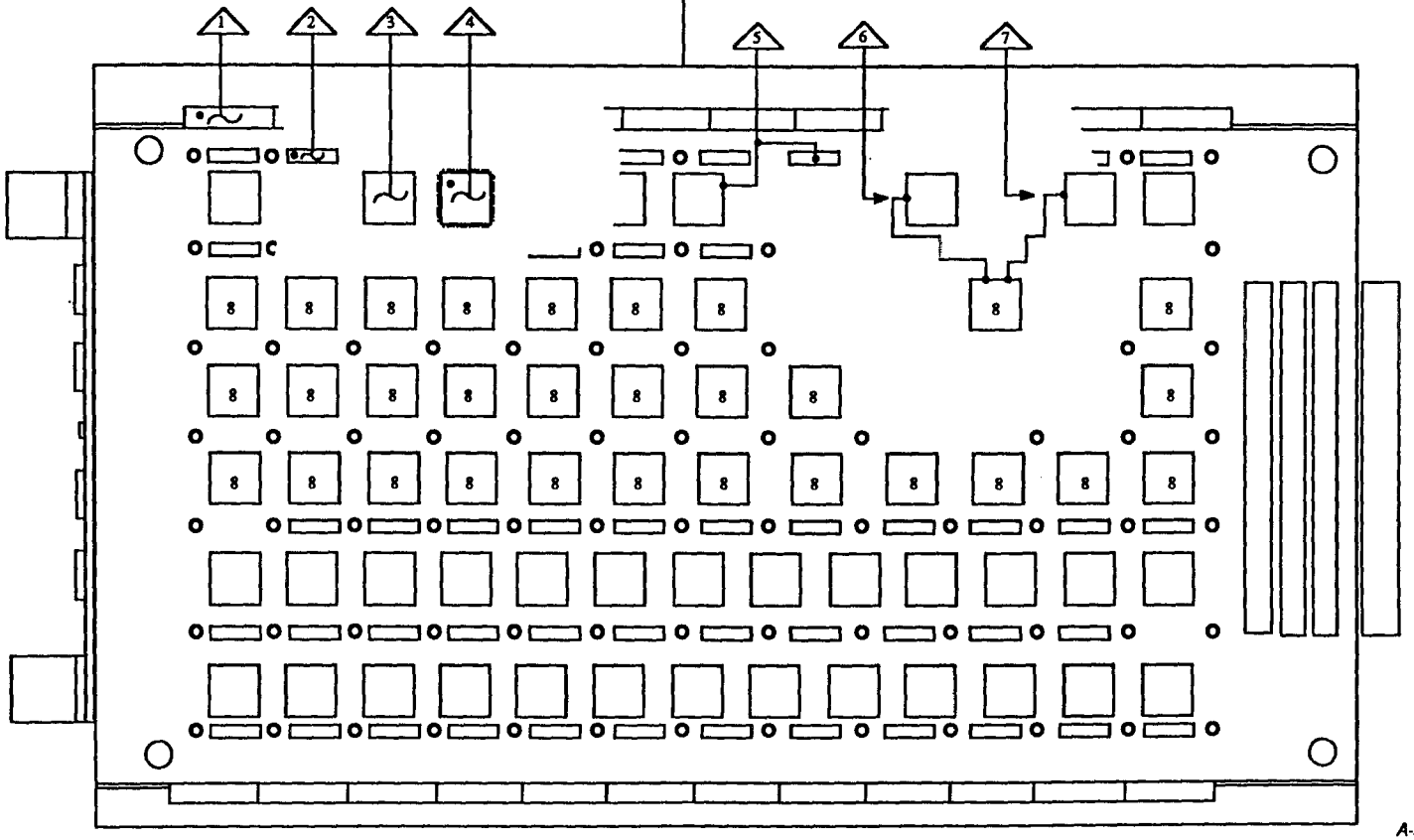
Hardware Trng.
YM15/09B J.E.S.

COMPONENTS PLACEMENT AND ASSIGNMENT DOCUMENTATION

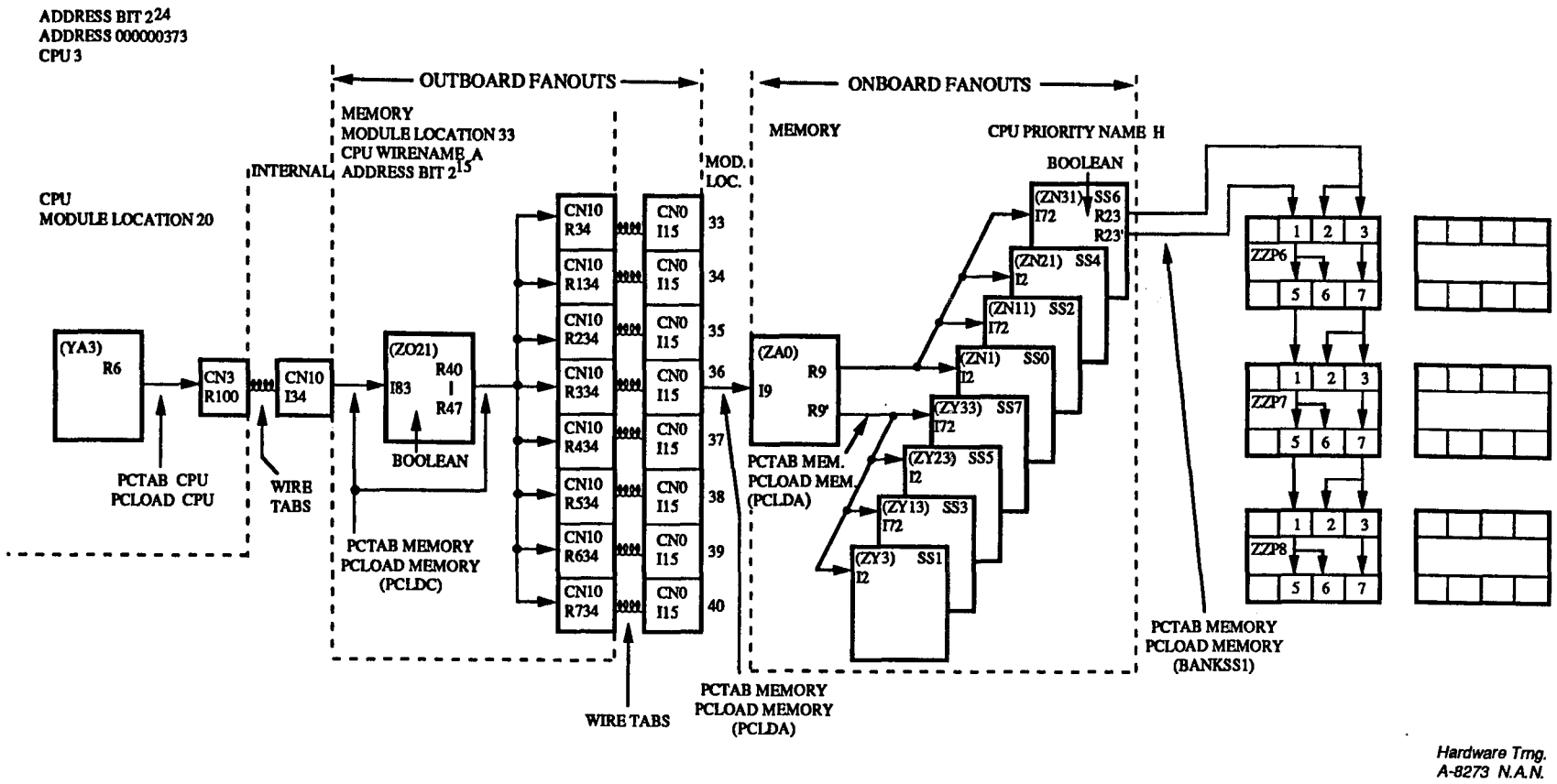
1. EDGE CONNECTOR - PCBDA - PCBDD UNDER $ CONNECTOR MAP 27.
2. FEED THRU, JUMPERS - CALLED OUT WHEN USED IN PCLDA - PCLDD AS "JUMPER".
3. OPTION PLACEMENT AND TYPE - PCBDA - PCBDD UNDER $ CHIP MAP, ALSO GIVES THE CHIPS ROTATION.
4. OPTION PIN ASSIGNMENT - MPT ZM-ZZ, ASSIGNS ALL 148 PINS A SIGNAL.

LOGIC PATHS DOCUMENTATION

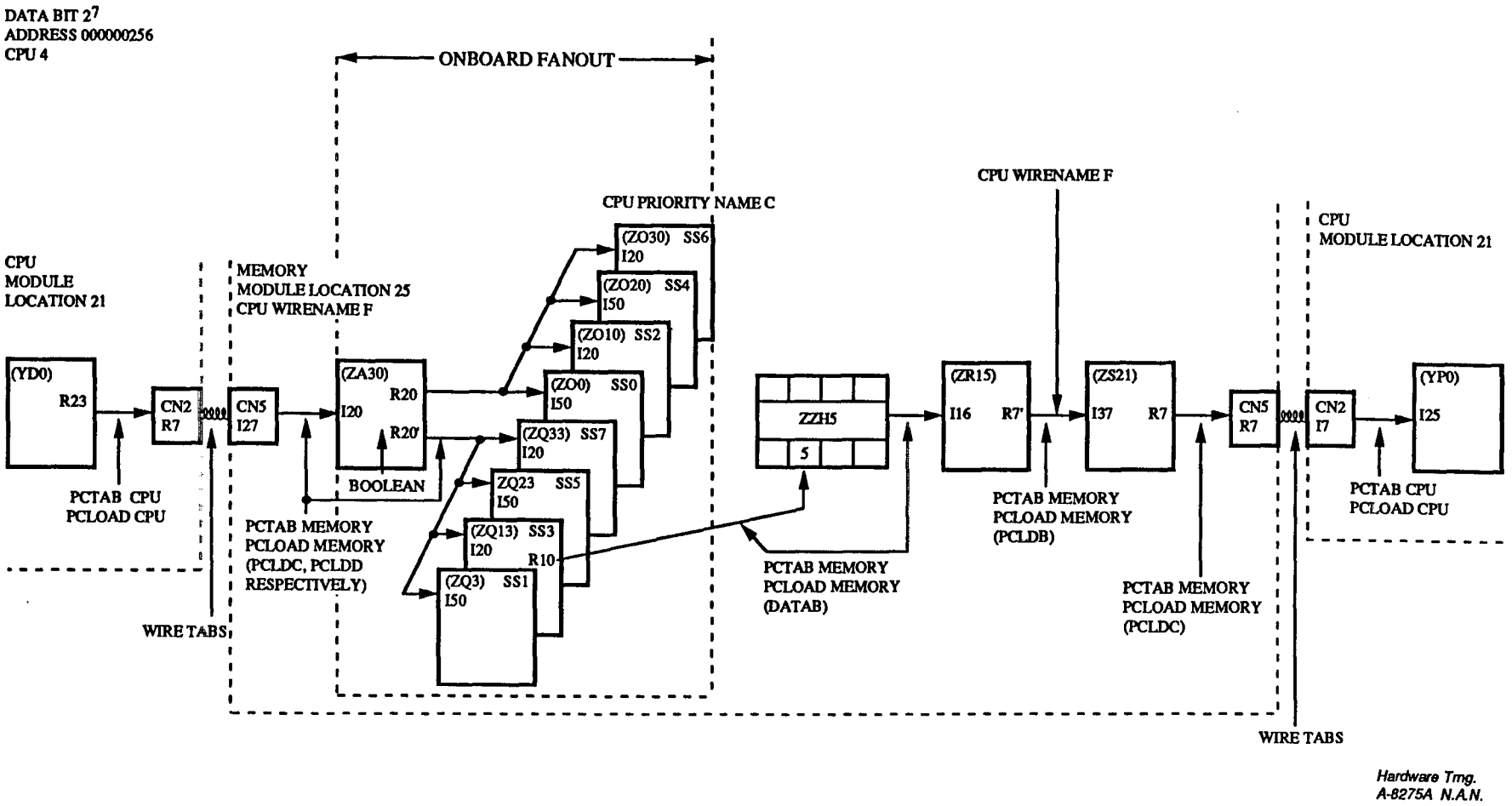
5. EDGE CONNECTOR USAGE - PCLDA - PCLDD TAKE THE SIGNAL FROM THE EDGE CONNECTOR TO AN OPTION TYPE OR "JUMPER".
6. DATA TO OR FROM THE MEMORY CHIP - SUBSECTION DATA A - D, SUBSECTION DATA A CONTAINS SUBSECTION 0, 1 DATA.
7. ADDRESS/CONTROL TO MEMORY CHIP - BANK SUBSECTION 0 - 7.



CRAY Y-MP MEMORY (64K x 1)
DOCUMENT ASSIGNMENT



CRAY Y-MP ADDRESS FLOW



CRAY Y-MP DATA FLOW

CRAY Y-MP MODULE LOCATIONS

MEMORY DATA	MEMORY MODULE LOCATION Section 0	Section 1	Section 2	Section 3
Bits 2^0 - 2^8	Location 1	9	25	33
Bits 2^9 - 2^{17}	Location 2	10	26	34
Bits 2^{18} - 2^{26}	Location 3	11	27	35
Bits 2^{27} - 2^{35}	Location 4	12	28	36
Bits 2^{36} - 2^{44}	Location 5	13	29	37
Bits 2^{45} - 2^{53}	Location 6	14	30	38
Bits 2^{54} - 2^{62}	Location 7	15	31	39
Bits 2^{63} - 2^{71}	Location 8	16	32	40

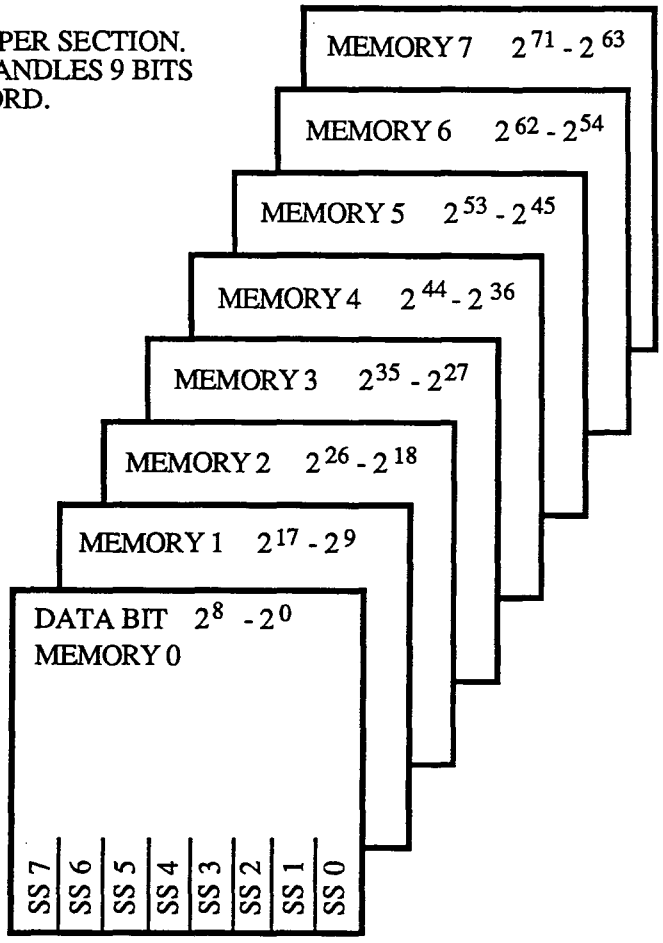
CPU NUMBER	LOCATION
0	Location 17
1	Location 18
2	Location 19
3	Location 20
4	Location 21
5	Location 22
6	Location 23
7	Location 24

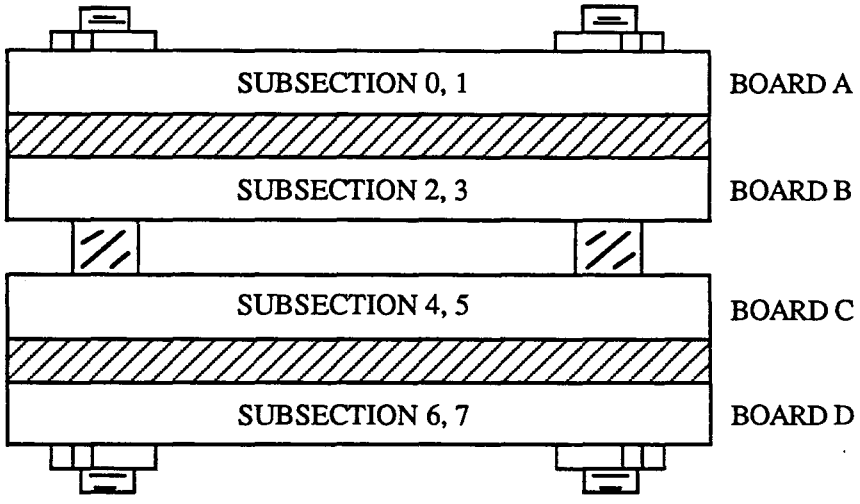
MEMORY ADDRESS

2^{24} 2^{23} 2^{22} 2^{21} 2^{20}	2^{19}	2^{18} 2^{17} 2^{16} 2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^9 2^8	2^7 2^6 2^5	2^4 2^3 2^2	2^1 2^0
X X X X X	X	X X X X X X X X X X X	X X X	X X X	X X
2^{15} 2^{14} 2^{13} 2^{12} 2^{11}	2^0 C.S.	2^{10} 2^9 2^8 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0	2^2 2^1 2^0	0 - 7 GOSS	0 - 3 Sec.

Hardware Trng.
YM03/11 J.E.S.

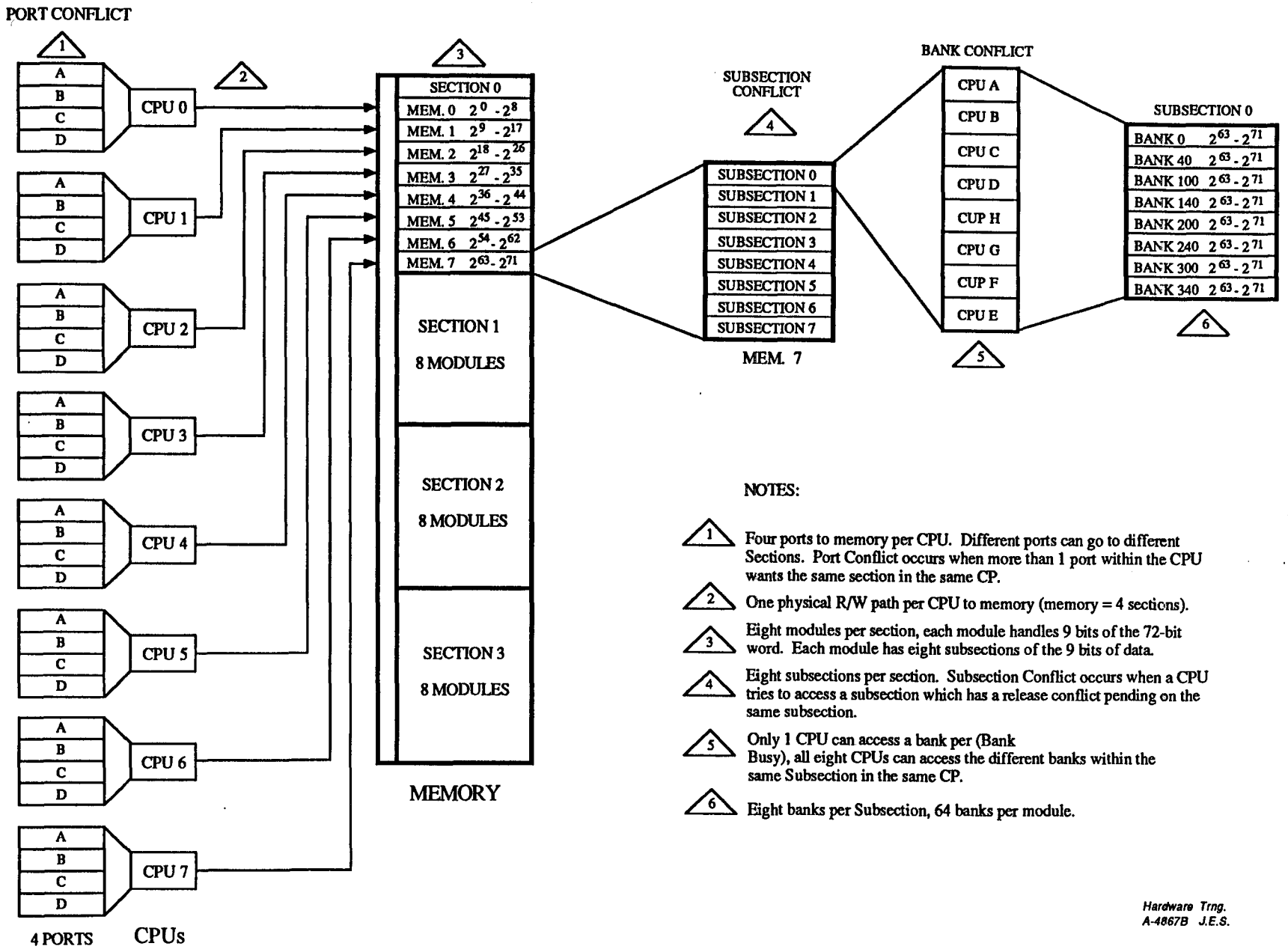
EIGHT MODULES PER SECTION.
EACH MODULE HANDLES 9 BITS
OF THE 72-BIT WORD.





Hardware Trng.
A-4921A J.E.S.

CRAY Y-MP MEMORY MODULE/SUBSECTION LAYOUT



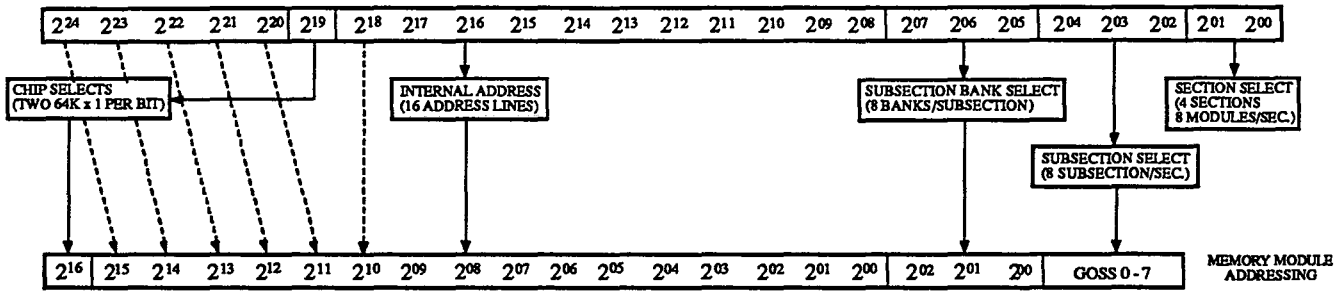
NOTES:

1. Four ports to memory per CPU. Different ports can go to different Sections. Port Conflict occurs when more than 1 port within the CPU wants the same section in the same CP.
2. One physical R/W path per CPU to memory (memory = 4 sections).
3. Eight modules per section, each module handles 9 bits of the 72-bit word. Each module has eight subsections of the 9 bits of data.
4. Eight subsections per section. Subsection Conflict occurs when a CPU tries to access a subsection which has a release conflict pending on the same subsection.
5. Only 1 CPU can access a bank per (Bank Busy), all eight CPUs can access the different banks within the same Subsection in the same CP.
6. Eight banks per Subsection, 64 banks per module.

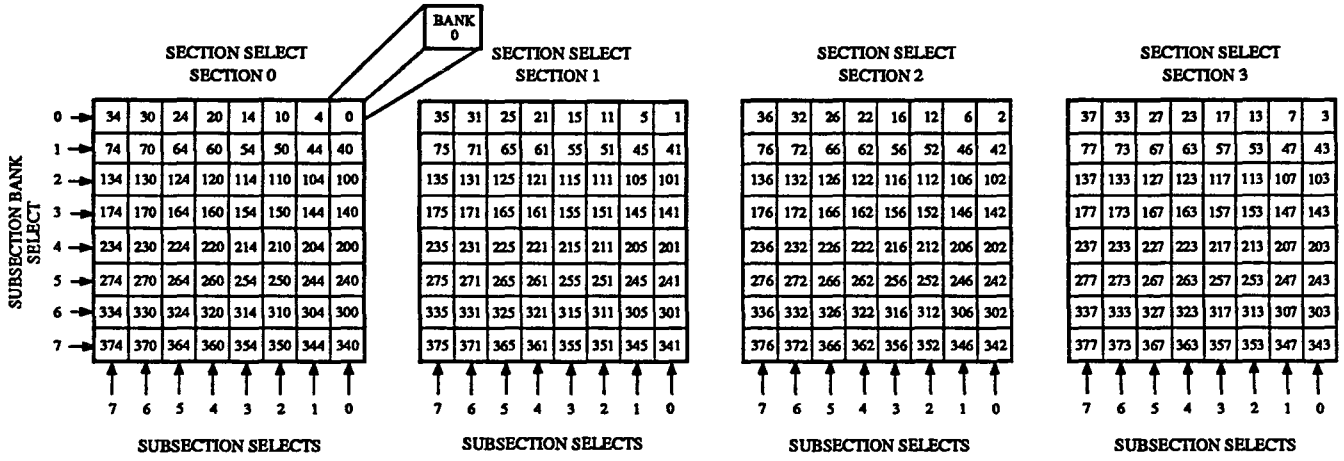
Hardware Trng.
A-4867B J.E.S.

CRAY Y-MP MEMORY SUBSECTION

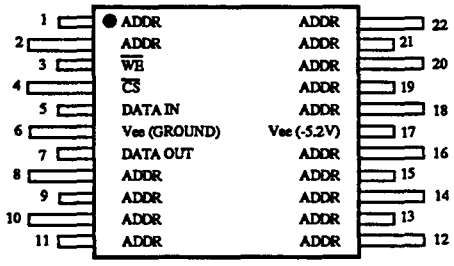
ADDRESS



BANK/SUBSECTION LAYOUT



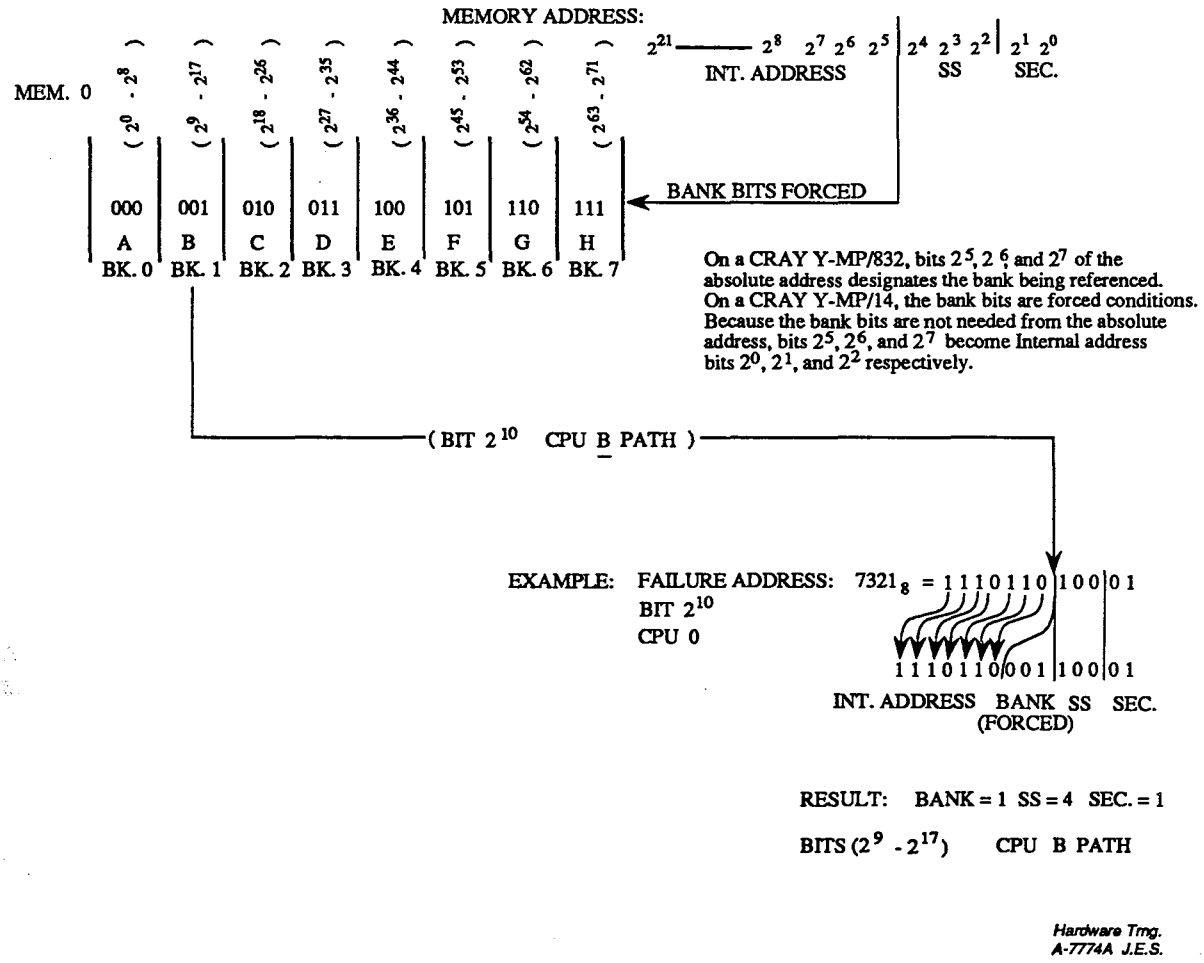
64K ECL MEMORY CHIP



Hardware Trng. A-4920A J.E.S.

CRAY Y-MP MEMORY ADDRESSING

- 1 MODULE PER SECTION; 72 BITS PER MODULE
- 4 TOTAL MEMORY MODULES
- 32 BANK MACHINE
- 1 BANK PER SUBSECTION
- MEMORY ADDRESS



CRAY Y-MP/14 MEMORY LAYOUT

- 2 MODULES PER SECTION; 36 BITS PER MODULE
- 8 TOTAL MEMORY MODULES
- 64 BANK MACHINE
- 2 BANKS PER SUBSECTION
- MEMORY ADDRESS

MEMORY ADDRESS:

2^{22} ——— 2^8 2^7 2^6 | 2^5 | 2^4 2^3 2^2 | 2^1 2^0

INT. ADDRESS | BANK | SS | SEC.

2^0

	MEM0 (2^0 - 2^8) MEM1 (2^{36} - 2^{44})				MEM0 (2^9 - 2^{17}) MEM1 (2^{45} - 2^{53})				MEM0 (2^{18} - 2^{26}) MEM1 (2^{54} - 2^{62})				MEM0 (2^{27} - 2^{35}) MEM1 (2^{63} - 2^{71})			
SECTION	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
SUBSECTION	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7
	00X	00X	00X	00X	01X	01X	01X	01X	10X	10X	10X	10X	11X	11X	11X	11X
CPU 0	A	H	H	A	A	H	H	A	B	G	G	B	B	G	G	B
PATH 1	H	A	A	H	H	A	A	H	G	B	B	G	G	B	B	G
									C	F	F	C	C	F	F	C
									F	C	C	F	F	C	C	F
									D	E	E	D	D	E	E	D
									E	D	D	E	E	D	D	E

BANK BITS (2^2,2^1) FORCED

Bit 2^5 of the absolute address is bank bit 2^0. On a CRAY Y-MP8, bits 2^6 and 2^7 of the absolute address are bank bits 2^1 and 2^2 respectively. On a CRAY Y-MP2, bank bits 2^1 and 2^2 are forced. Because bank bits 2^1 and 2^2 do not come from the absolute address, bits 2^6 and 2^7 become part of the Internal address. Bit 2^6 becomes Internal address bit 2^0. Bit 2^7 becomes Internal address bit 2^1.

(BIT 2^{10} CPU B PATH)

YL CONFLICT CHECK

SEC.		0		1		2		3	
SS		0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7
CPU PATH	0	A	H	G	B	C	F	E	D
	1	H	A	B	G	F	C	D	E

EXAMPLE: FAILURE ADDRESS: 7321_8 = 1 1 1 0 1 1 0 1 0 0 0 1

BIT 2^{10}

CPU 1

1 1 1 0 1 1 0 1 0 0 0 1

INT. ADDRESS BANK SS SEC.

(2^1, 2^2 FORCED)

RESULT: BANK = 2 SS = 4 SEC. = 1

BITS (2^9 - 2^{17}) CPU B PATH MEM 0

Hardware Trng
A-7782C J.E.S.

CRAY Y-MP2/XY MEMORY LAYOUT

- 4 MODULES PER SECTION; 18 BITS PER MODULE
- 16 TOTAL MEMORY MODULES
- 128 BANK MACHINE
- 4 BANKS PER SUBSECTION
- MEMORY ADDRESS

		MEM 0 (2^0-2^8) MEM 1 (2^{18}-2^{26}) MEM 2 (2^{36}-2^{44}) MEM 3 (2^{54}-2^{62})								MEM 0 (2^9-2^{17}) MEM 1 (2^{27}-2^{35}) MEM 2 (2^{45}-2^{53}) MEM 3 (2^{63}-2^{71})							
SECTION		BITS 0-8, 18-26, 36-44, 54-62								BITS 9-17, 27-35, 45-53, 63-71							
		0		1		2		3		0		1		2		3	
SUBSECTION		0145	2367	0145	2367	0145	2367	0145	2367	0145	2367	0145	2367	0145	2367	0145	2367
CPU PATH		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	0	A	H	G	B	E	D	C	F	B	G	H	A	F	C	D	E
	1	C	F	A	H	G	B	E	D	D	E	B	G	H	A	F	C
	2	E	D	C	F	A	H	G	B	F	C	D	E	B	G	H	A
	3	G	B	E	D	C	F	A	H	H	A	F	C	D	E	B	G

2^{23} —— 2^8 2^7 | 2^6 2^5 | 2^4 2^3 2^2 | 2^1 2^0
INT. ADDR. | BK. | SS | SEC.
2^1 2^0

BANK BIT (2^2) FORCED

Bits (2^5) and (2^6) of the Absolute address are bank bits (2^0) and (2^1) respectively. On a CRAY Y-MP8 bit (2^7) of the Absolute address is bank bit (2^2). On a CRAY Y-MP4 bank bit (2^2) is forced. Because bank bit (2^2) does not come from bit (2^7) of the Absolute address, bit (2^7) becomes Internal address bit (2^0).

(BIT (2^{10}) CPU H PATH)

YL CONFLICT CHECKS

SEC.		0		1		2		3	
SS		0145	2367	0145	2367	0145	2367	0145	2367
CPU PATH	0	A	H	G	B	F	C	D	E
	1	C	F	B	G	H	A	E	D
	2	F	C	D	E	A	H	G	B
	3	H	A	E	D	C	F	B	G

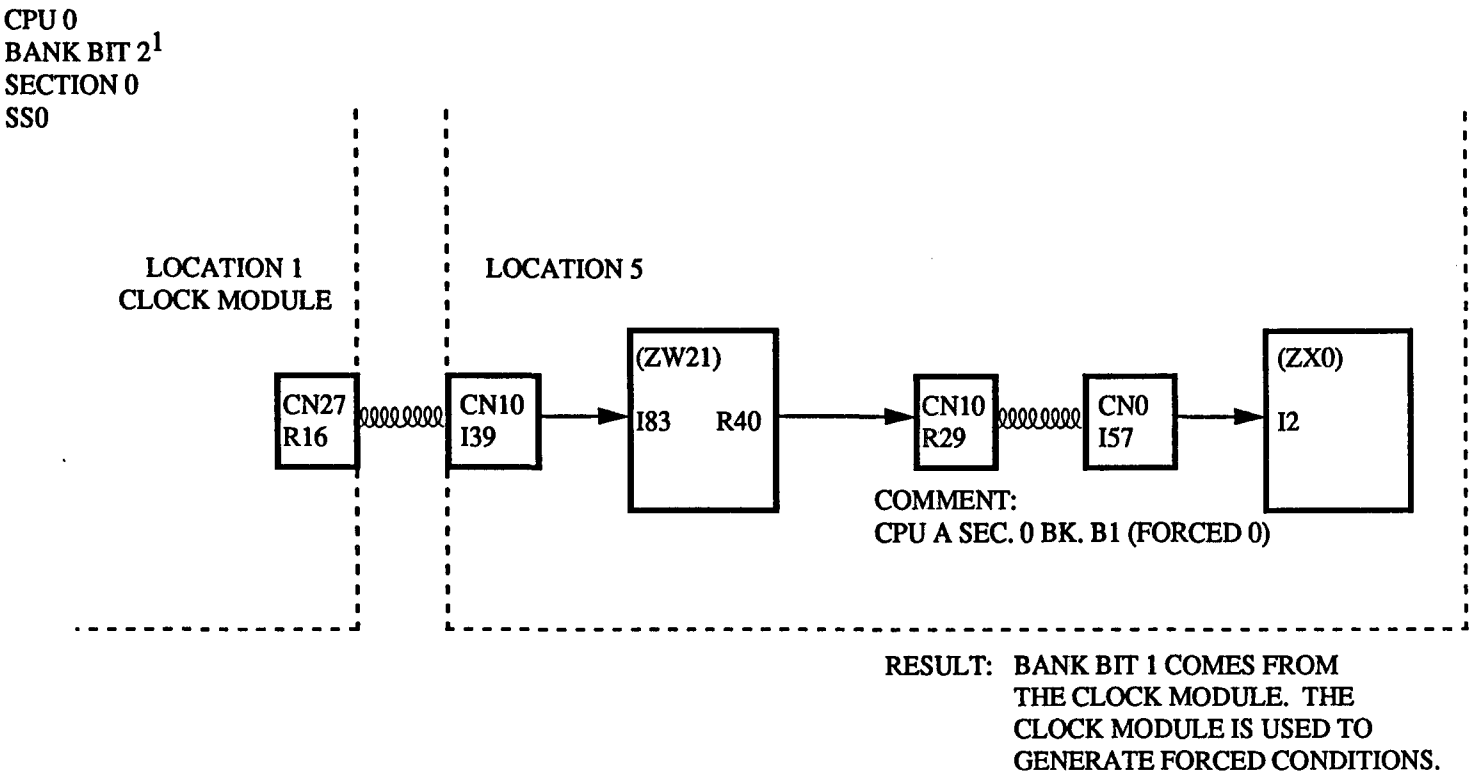
EXAMPLE: FAILURE ADDRESS: 7321_8 = 1 1 1 0 1 1 0 1 0 0 0 1
BIT (2^{10})
CPU 0

1 1 1 0 1 | 1 1 0 | 1 0 0 | 0 1
INT. ADDR. | BK. | SS | SEC.

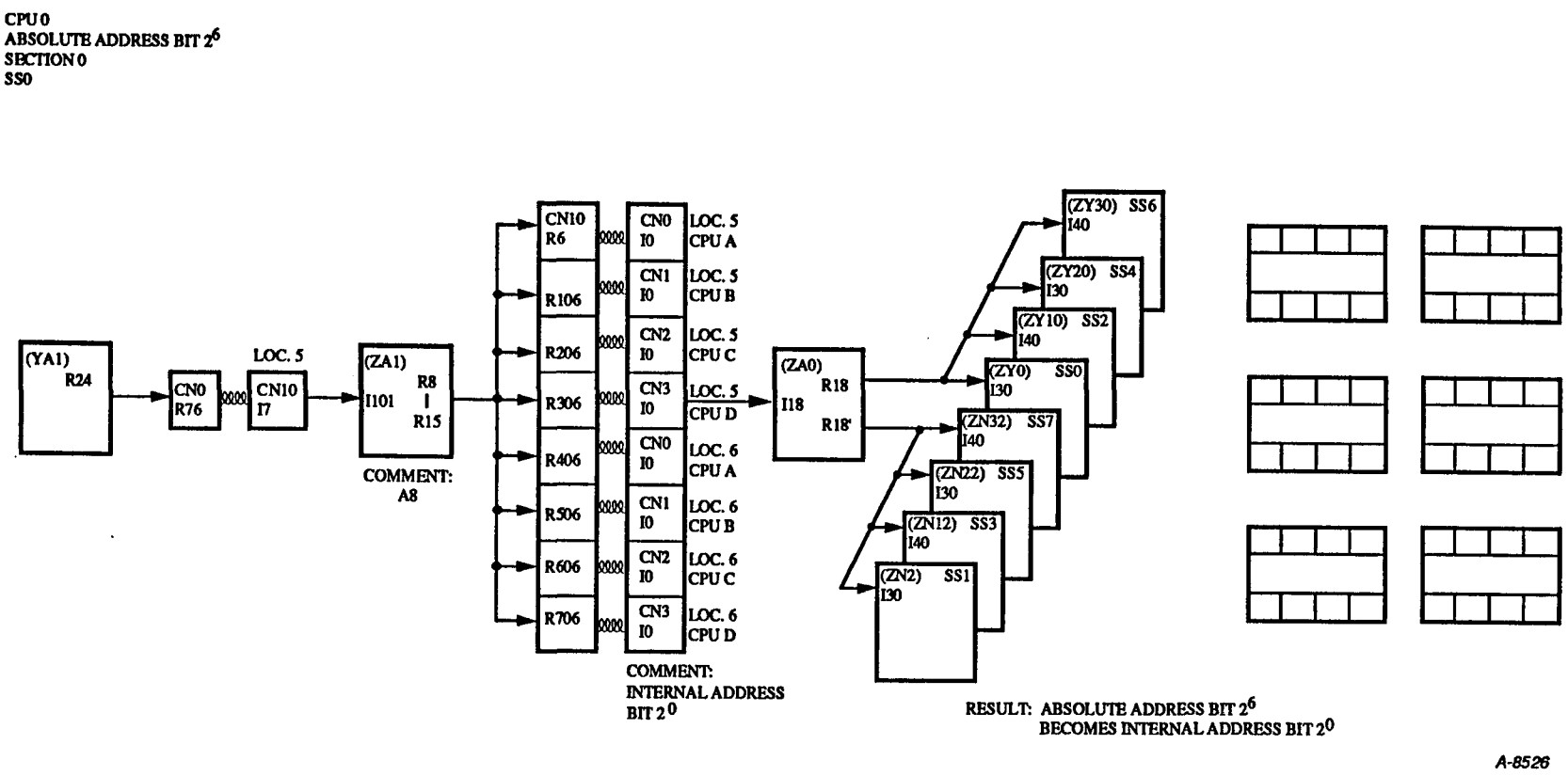
RESULT: BANK 6, SS 4, SEC. 1
BITS (2^9 - 2^{17}) CPU H PATH MEM 0

Hardware Trng.
A-7781B J.E.S.

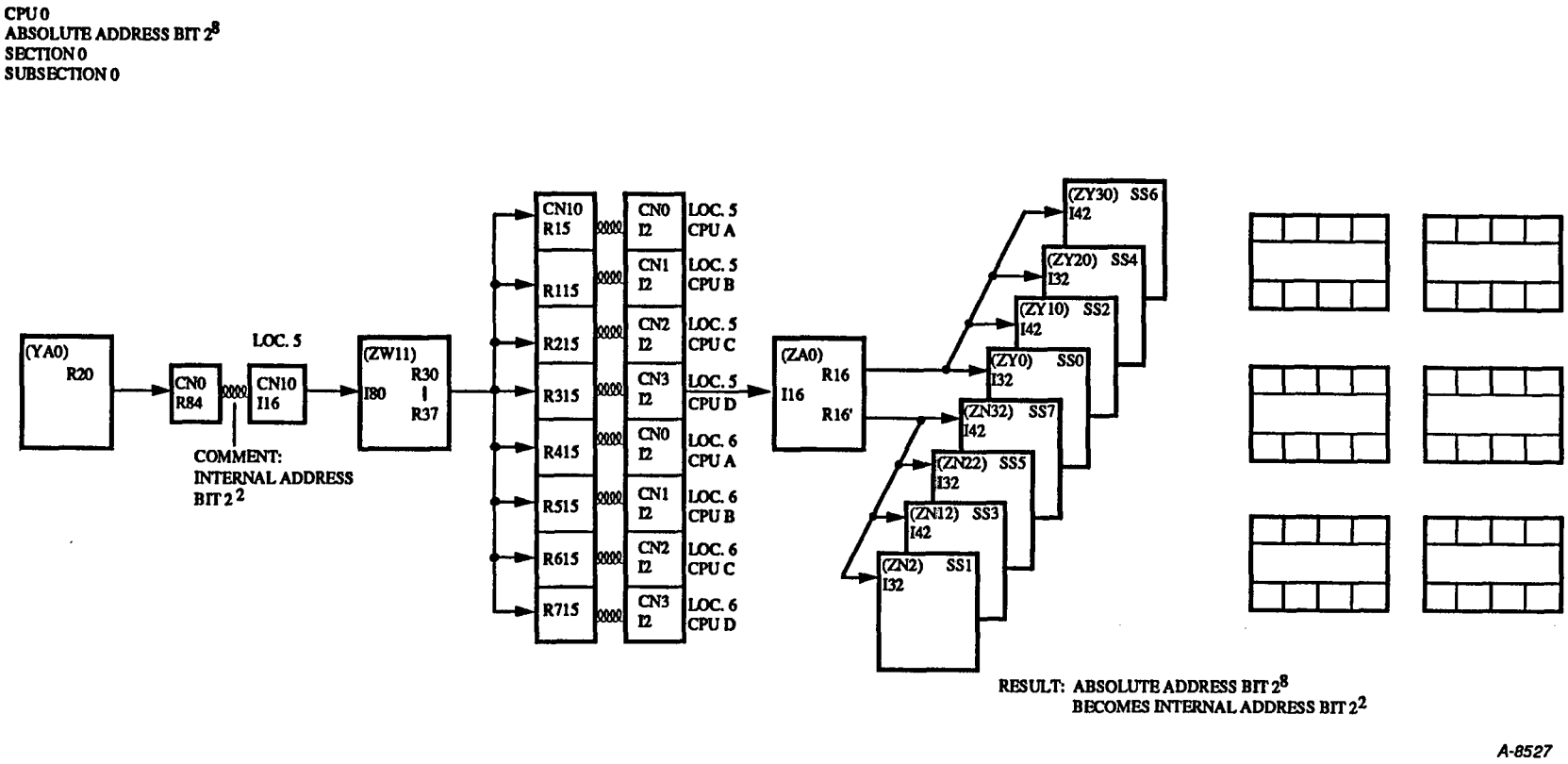
CRAY Y-MP4/xy



CRAY Y-MP/28 BANK BIT 2^1



CRAY Y-MP/28 ADDRESS FLOW



CRAY Y-MP/28 ADDRESS FLOW

MEMORY MODULE

DATA BIT	MEM. 0	MEM. 1	MEM. 2	MEM. 3	MEM. 4	MEM. 5	MEM. 6	MEM. 7
N	2^0	2^9	2^{18}	2^{27}	2^{36}	2^{45}	2^{54}	2^{63}
N + 1	2^1	2^{10}	2^{19}	2^{28}	2^{37}	2^{46}	2^{55}	2^{64} CB0
N + 2	2^2	2^{11}	2^{20}	2^{29}	2^{38}	2^{47}	2^{56}	2^{65} CB1
N + 3	2^3	2^{12}	2^{21}	2^{30}	2^{39}	2^{48}	2^{57}	2^{66} CB2
N + 4	2^4	2^{13}	2^{22}	2^{31}	2^{40}	2^{49}	2^{58}	2^{67} CB3
N + 5	2^5	2^{14}	2^{23}	2^{32}	2^{41}	2^{50}	2^{59}	2^{68} CB4
N + 6	2^6	2^{15}	2^{24}	2^{33}	2^{42}	2^{51}	2^{60}	2^{69} CB5
N + 7	2^7	2^{16}	2^{25}	2^{34}	2^{43}	2^{52}	2^{61}	2^{70} CB6
N + 8	2^8	2^{17}	2^{26}	2^{35}	2^{44}	2^{53}	2^{62}	2^{71} CB7

NOTE: To locate the bad memory chip you need the failing Address and the failing bit.

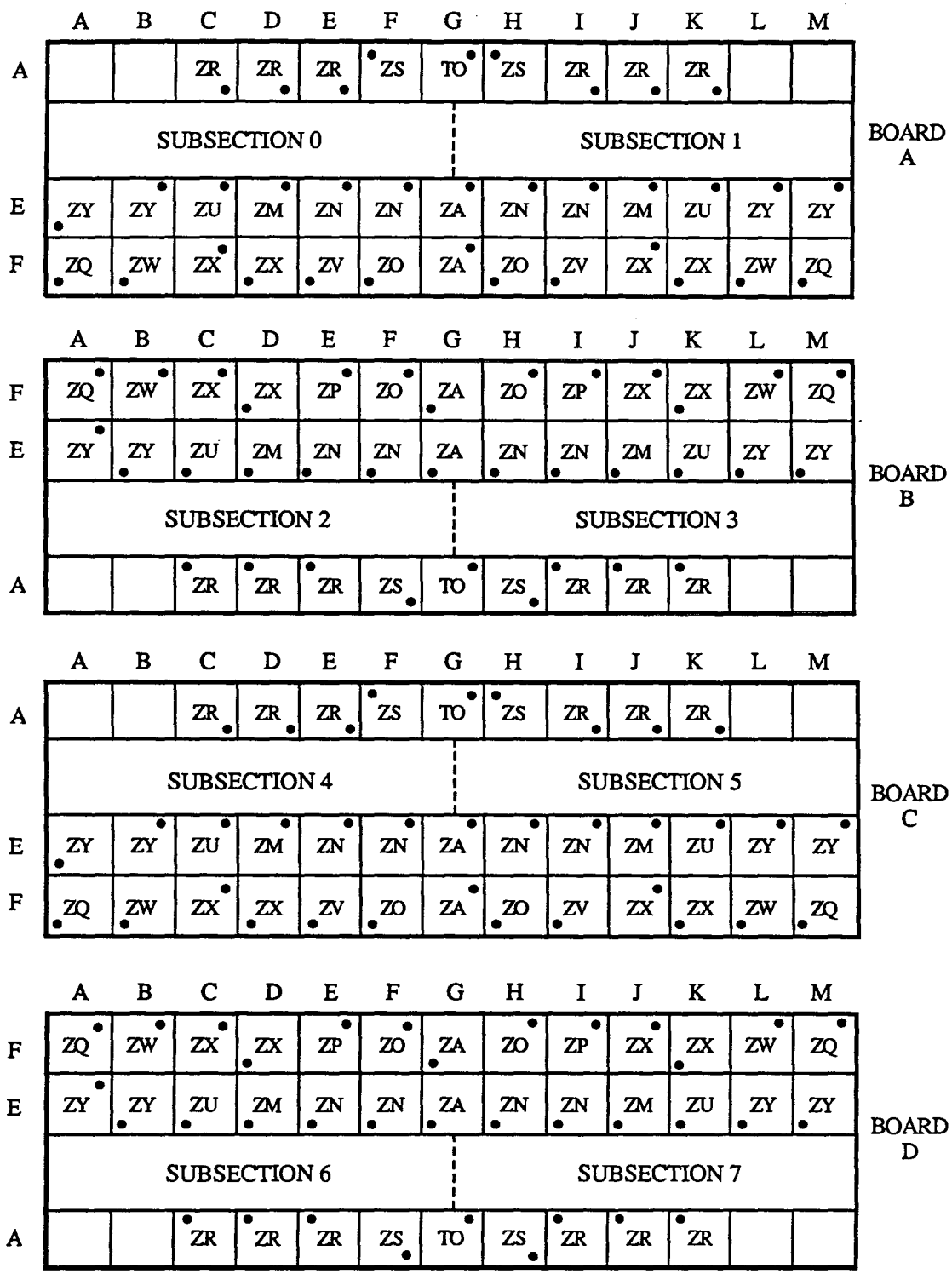
From the failing address calculate:

1. Section _____
2. Subsection _____
3. Subsection Bank _____
4. Chip Select _____

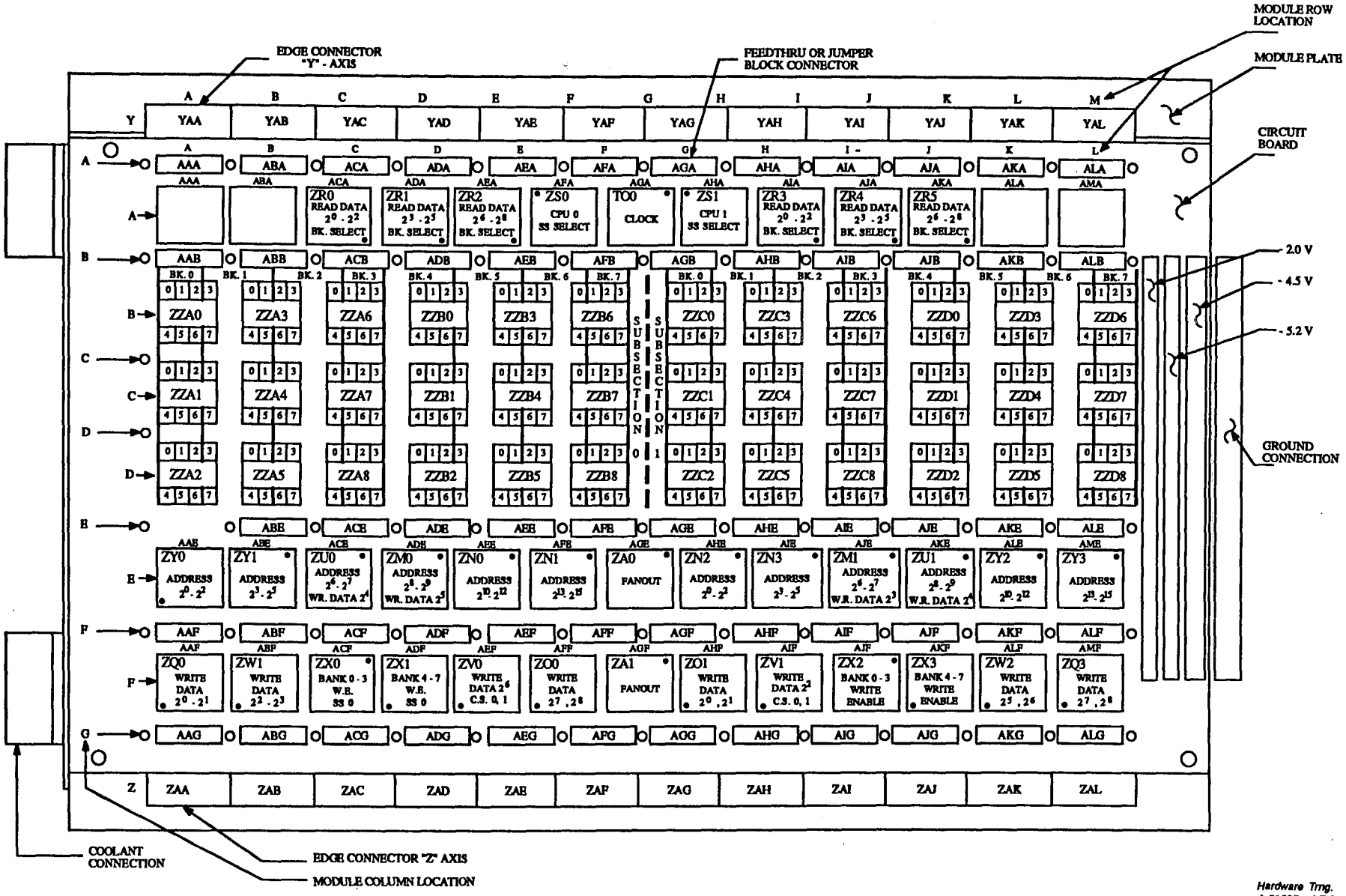
Failing bit is associated to Data bits (N - N + 8).
Failing module is associated with the failing bit.

Hardware Trng.
A-4818 J.E.S.

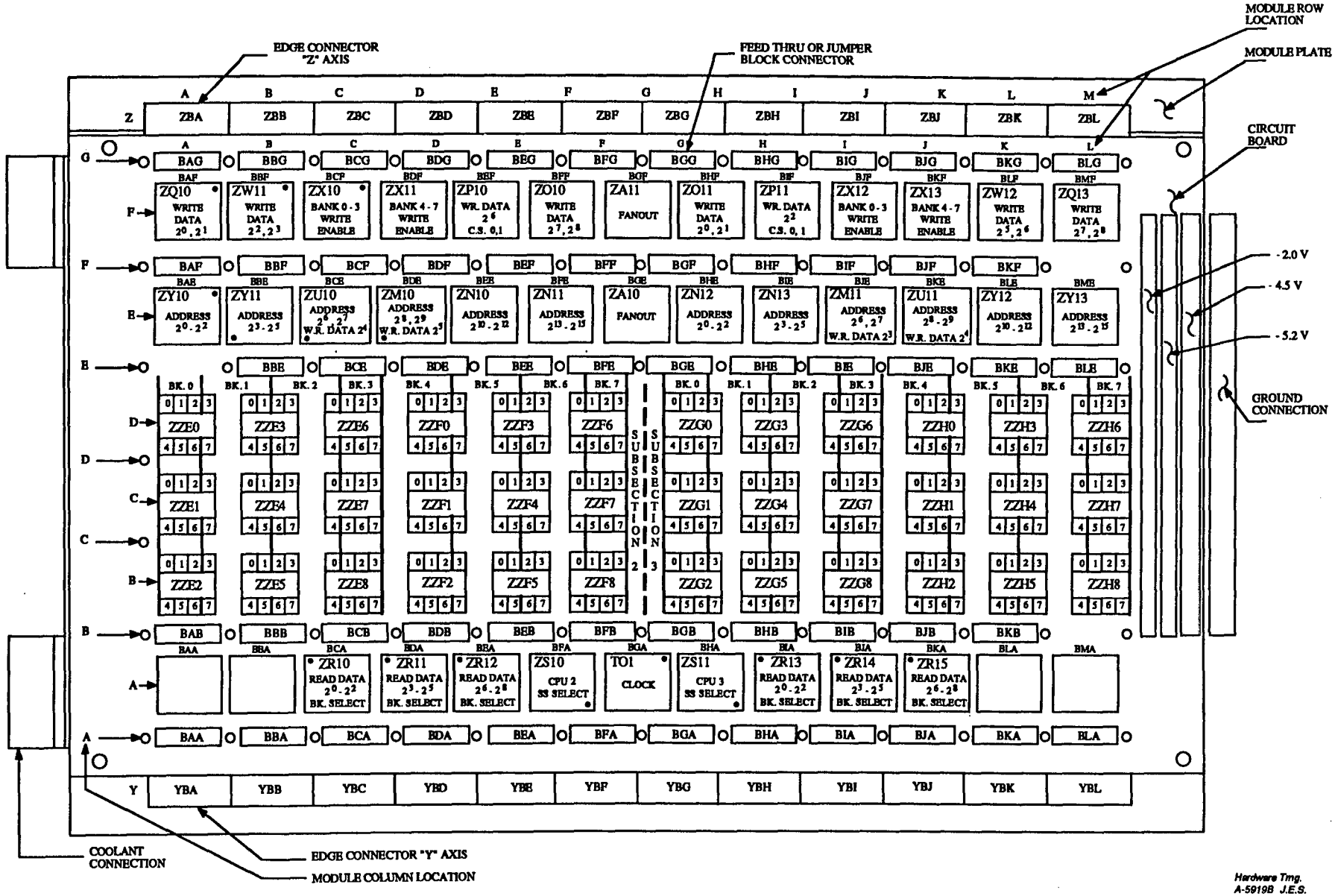
CRAY Y-MP MODULE BIT ASSOCIATION



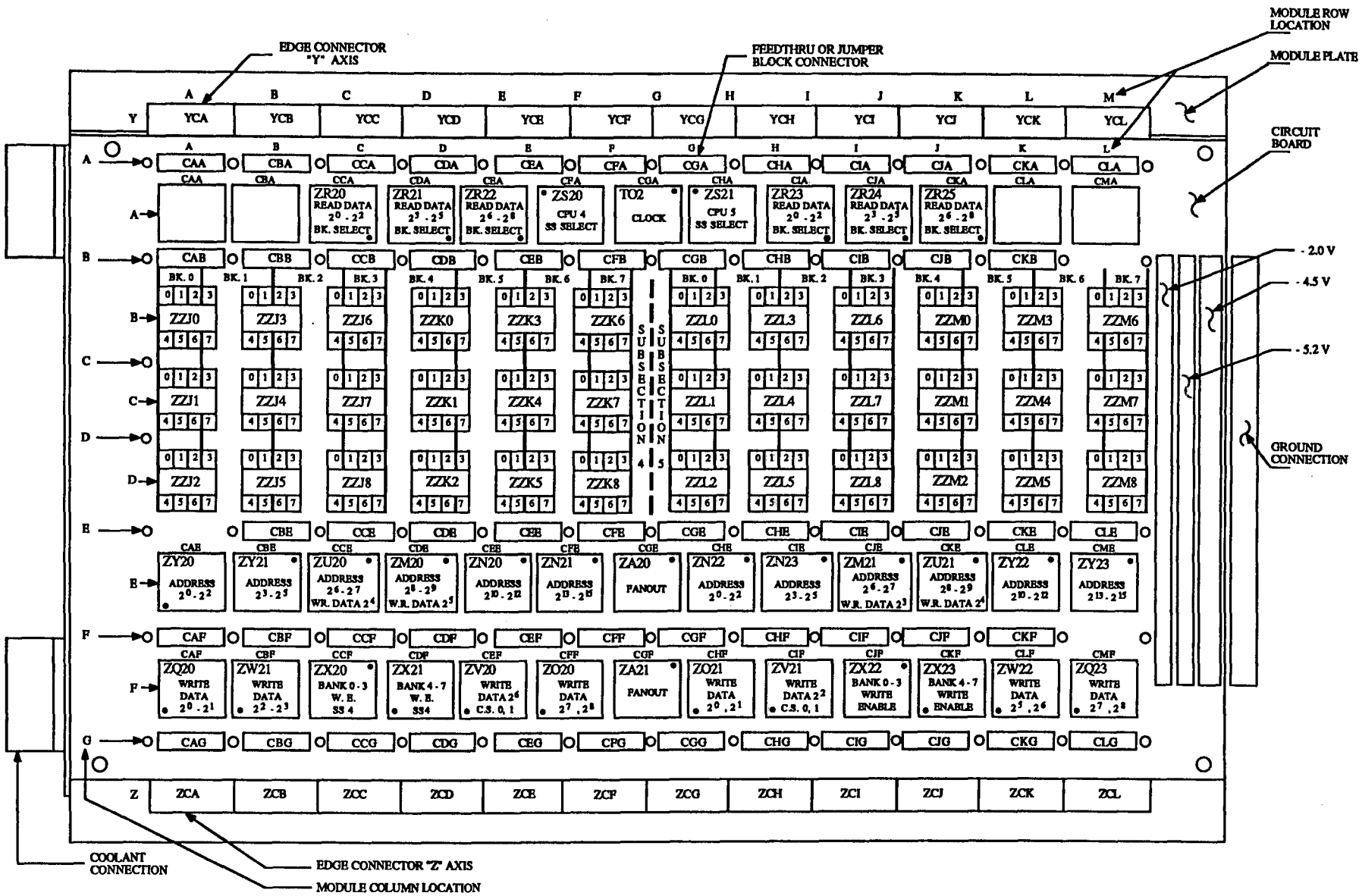
CRAY Y-MP MODULE/SUBSECTION LAYOUT



CRAY Y-MP MEMORY MAP
BOARD A

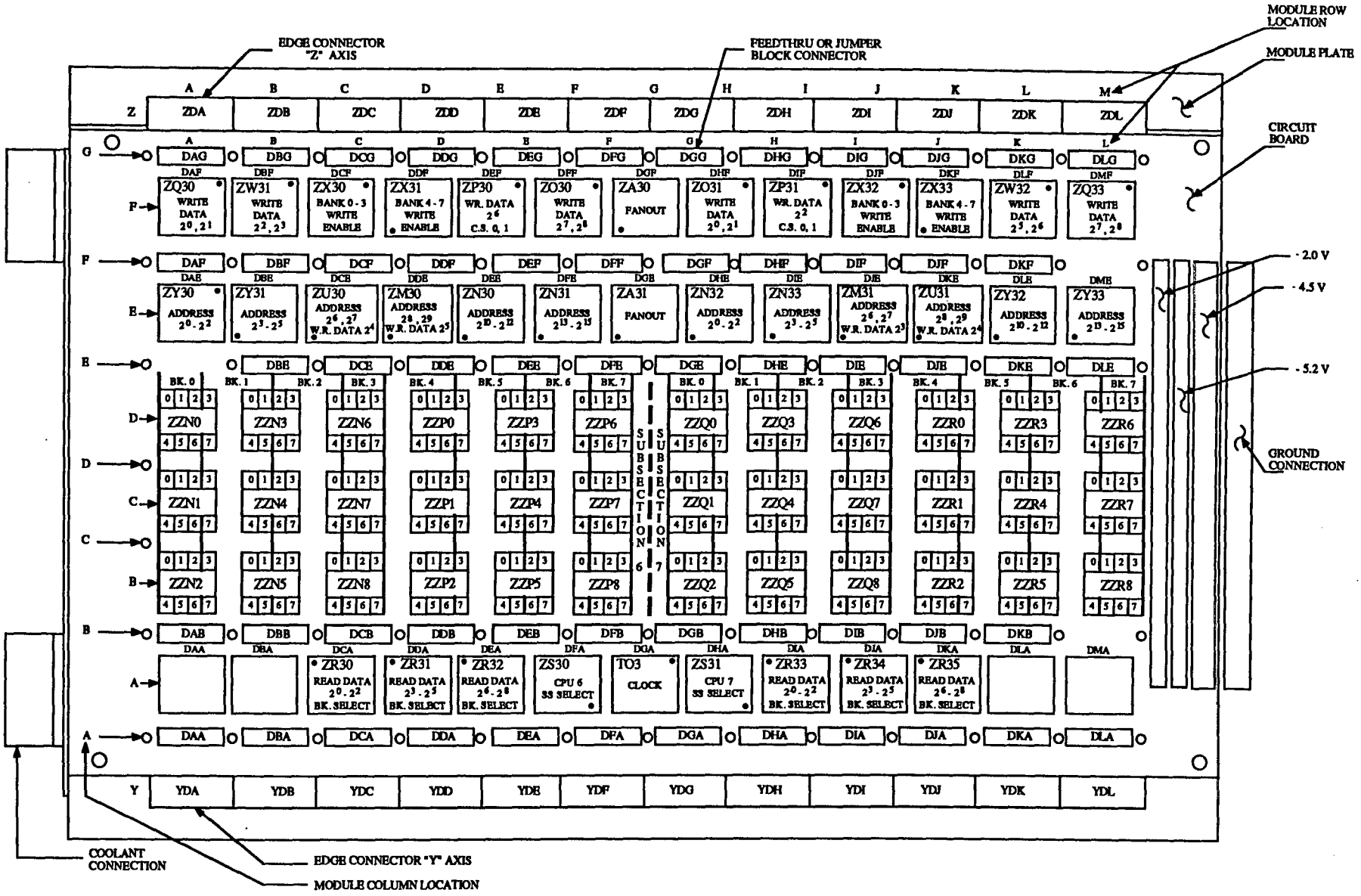


CRAY Y-MP MEMORY MAP
BOARD B

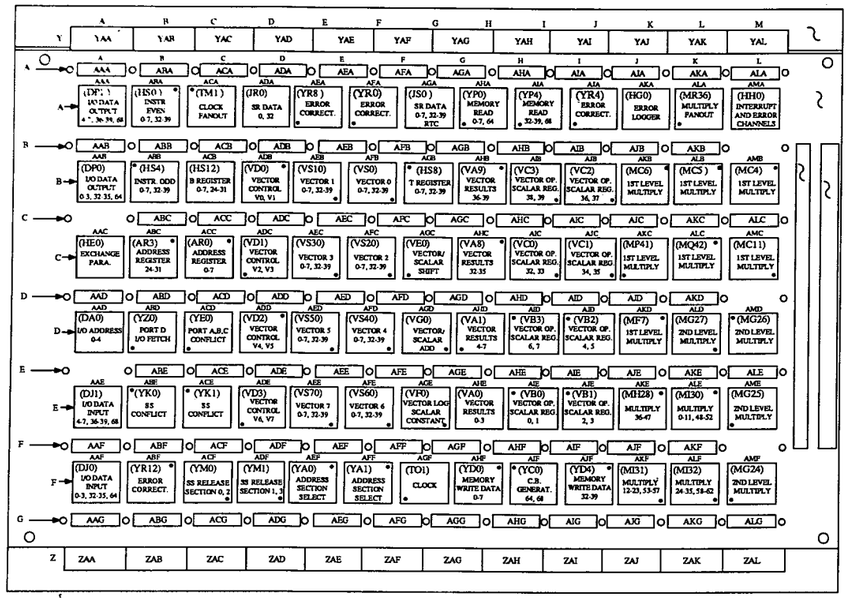


CRAY Y-MP MEMORY MAP
BOARD C

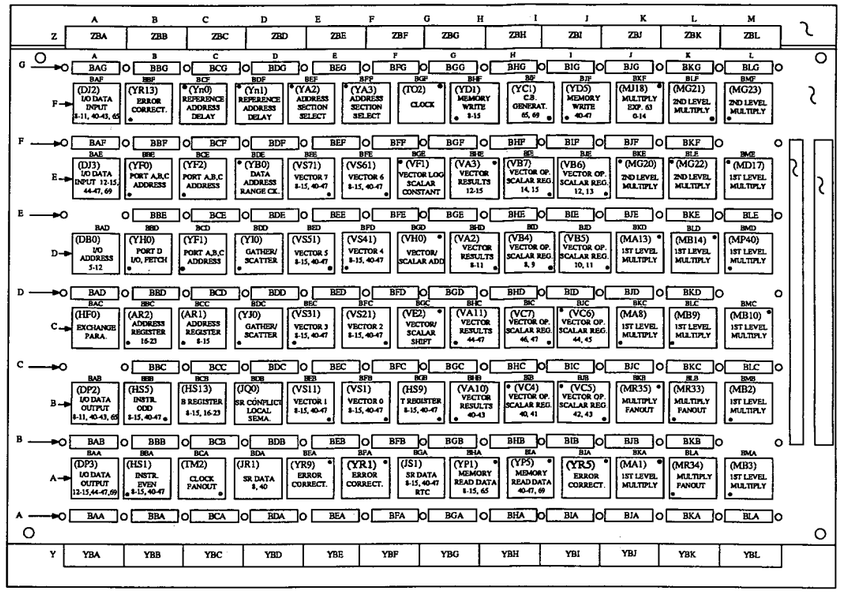
Hardware Trng.
A-5920B J.E.S.



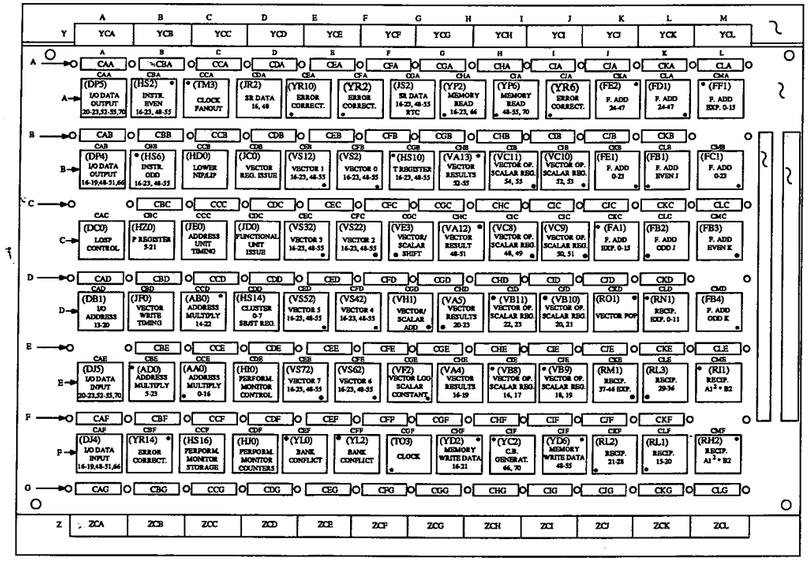
CRAY Y-MP MEMORY MAP
BOARD D



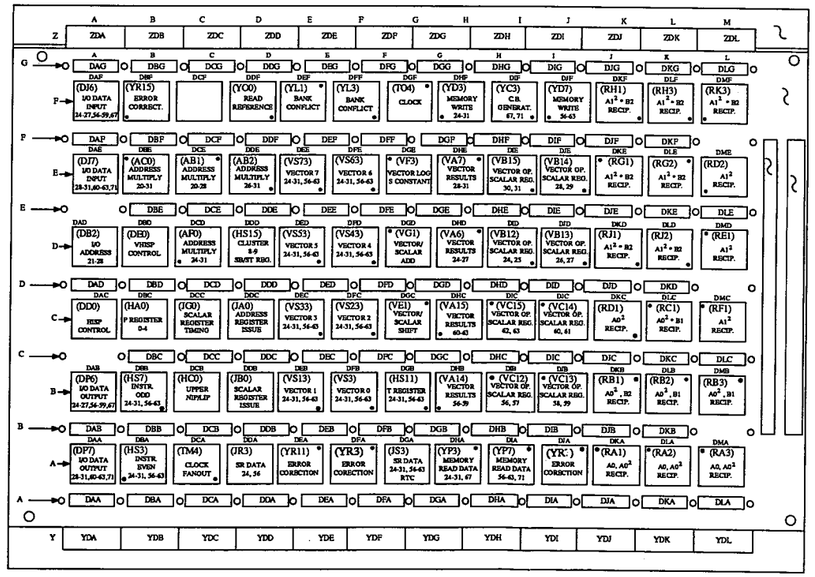
BOARD A (REV. 0)



BOARD B (REV. 0)



BOARD C (REV. 0)



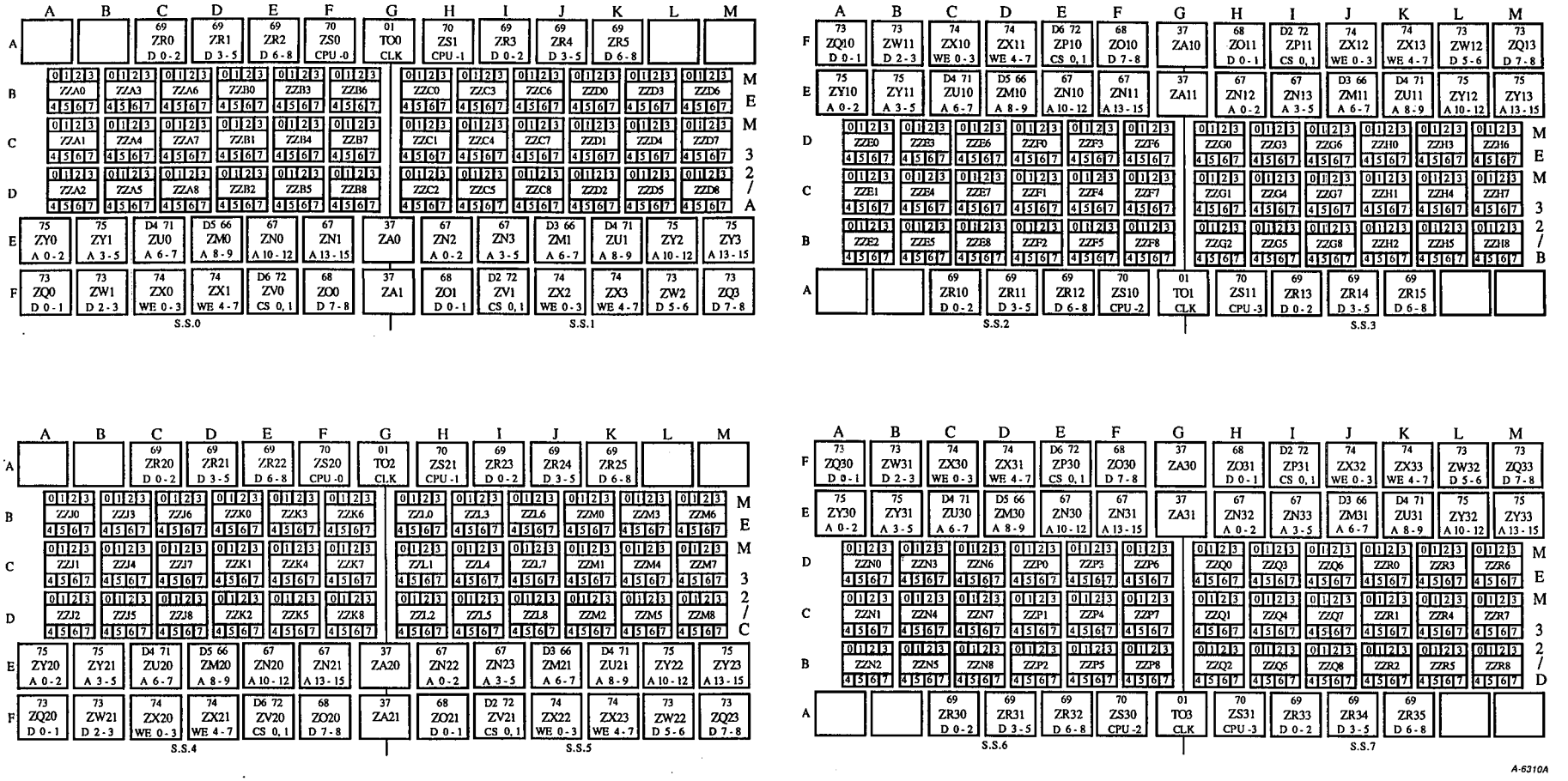
BOARD D (REV. 0)

Hardware Tmg.
A-6346B J.E.S.

CRAY Y-MP CPU MAP - BOARDS A - D (REV. 0)

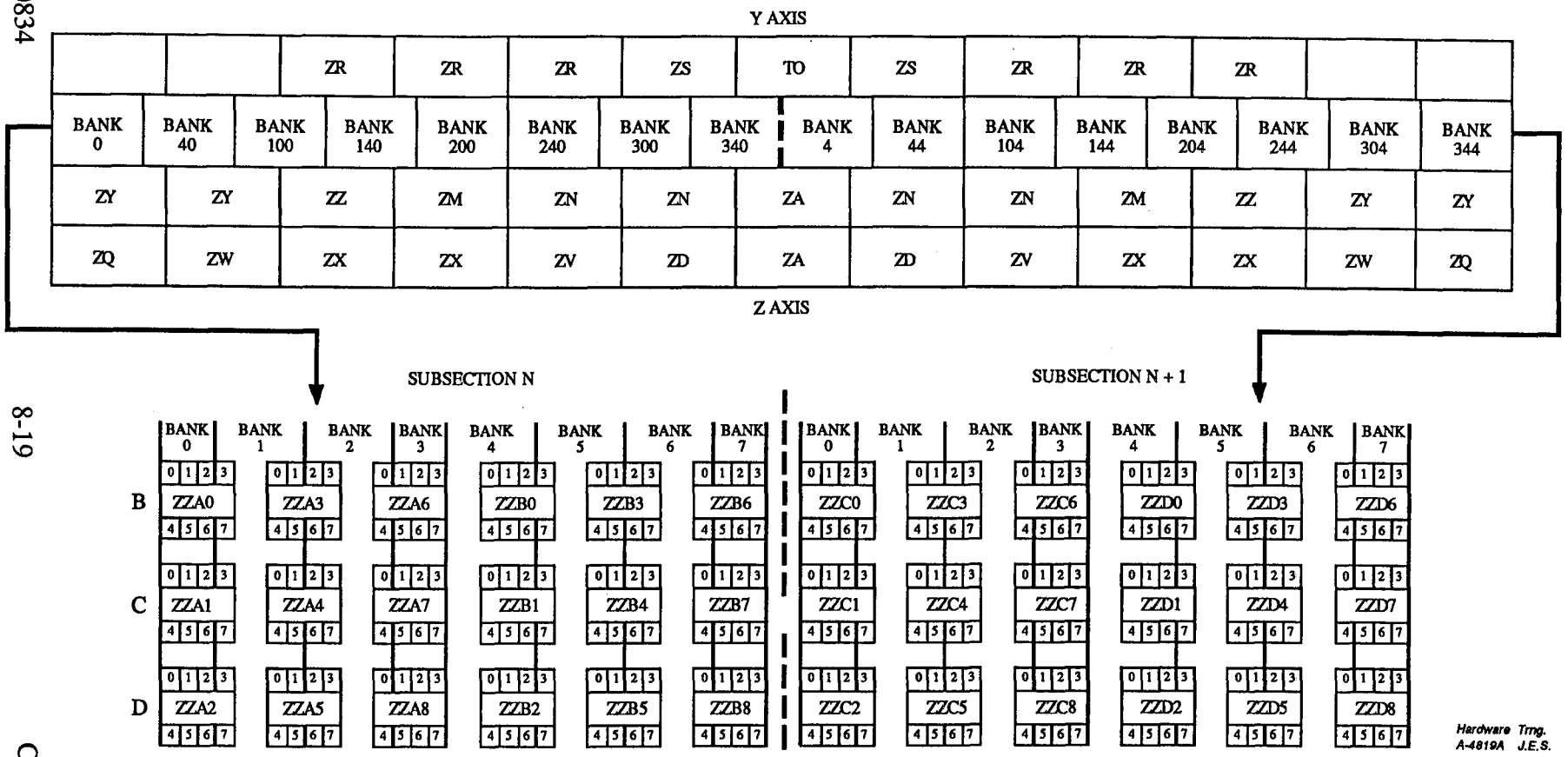
HTV-0834

CRAY PROPRIETARY

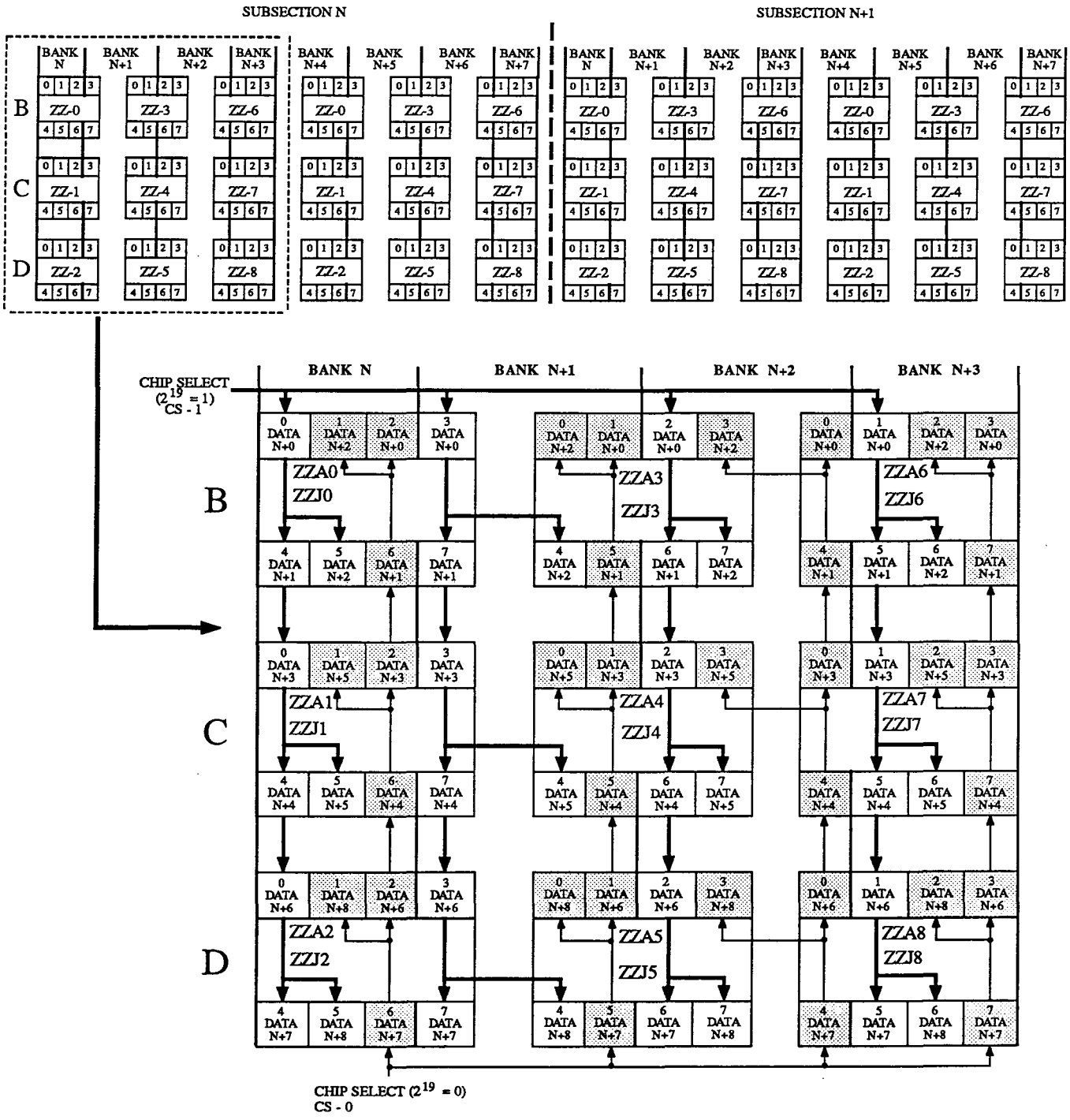


CRAY Y-MP 8/32 MEMORY - 64K x 1

CRAY Y-MP 8/32 MEMORY - 64K x 1



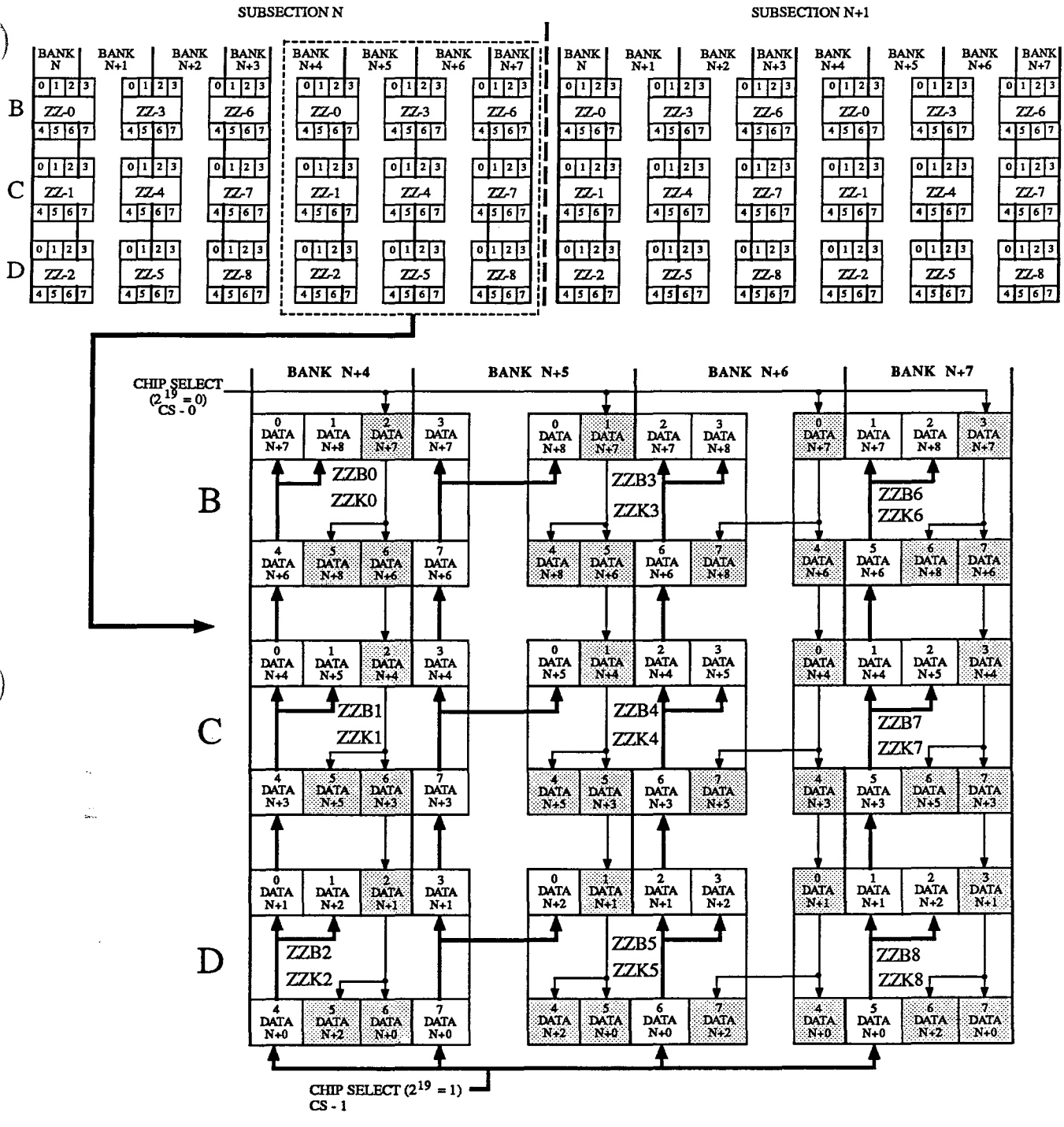
CRAY Y-MP BANK/SUBSECTION LAYOUT



NOTE: EACH BANK HAS 18 MEMORY CHIPS (64K x 1) WHICH IS DIVIDED INTO 9 DATA BITS PER MODULE (N+0 - N+8) AND TWO CHIP SELECTS (2^{19} = 0, 2^{19} = 1)

Hardware Trng. A-4851 J.E.S.

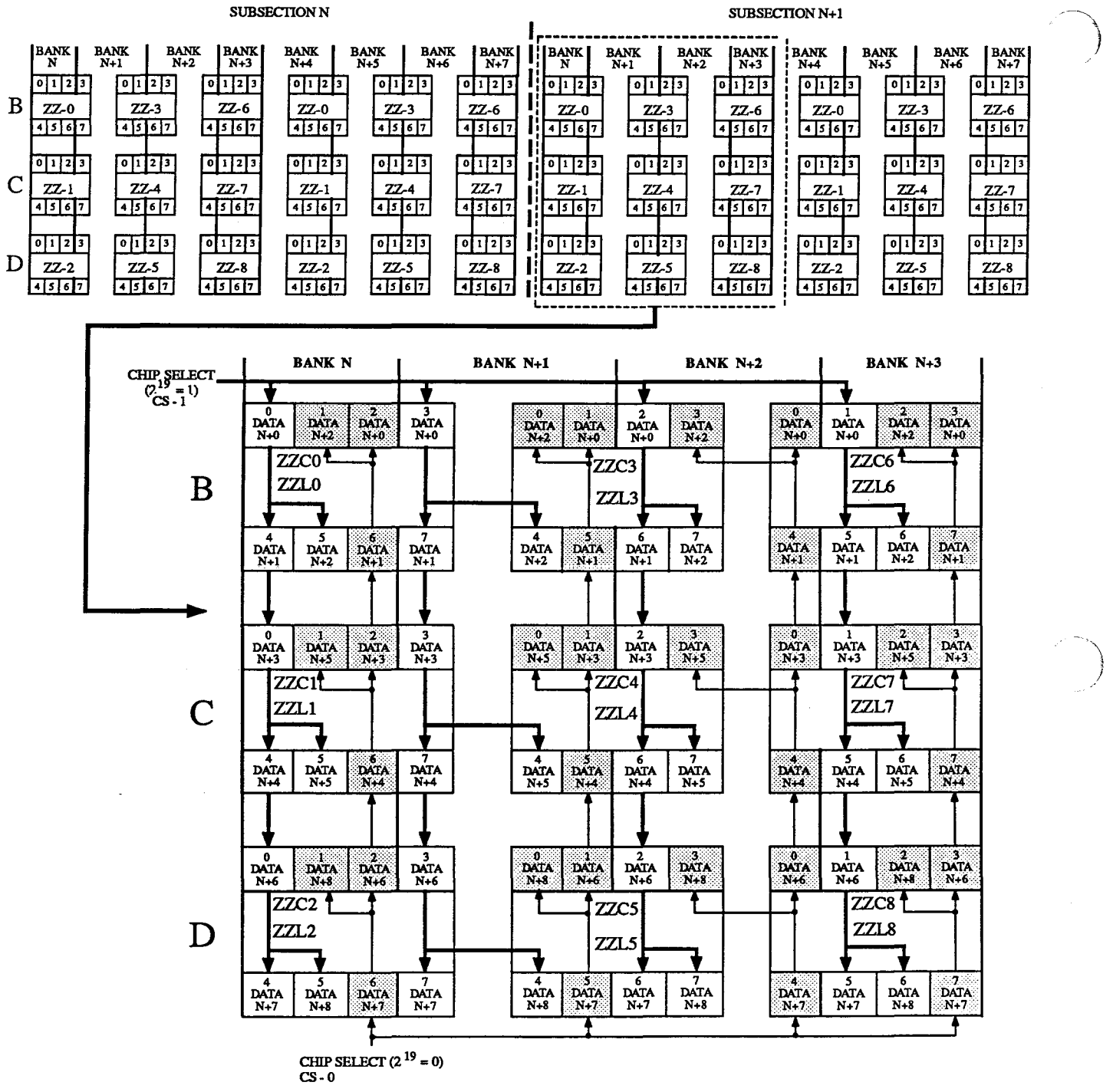
CRAY Y-MP MEMORY BOARD A/C SUBSECTION 0/4
BANKS (N - N + 3) (64K x 1) LOCATOR



NOTE: EACH BANK HAS 18 MEMORY CHIPS (64K x 1) WHICH IS DIVIDED INTO 9 DATA BITS PER MODULE (N+0 - N+8) AND TWO CHIP SELECTS ($2^{19} = 0, 2^{19} = 1$)

Hardware Trng.
A-4890 J.E.S.

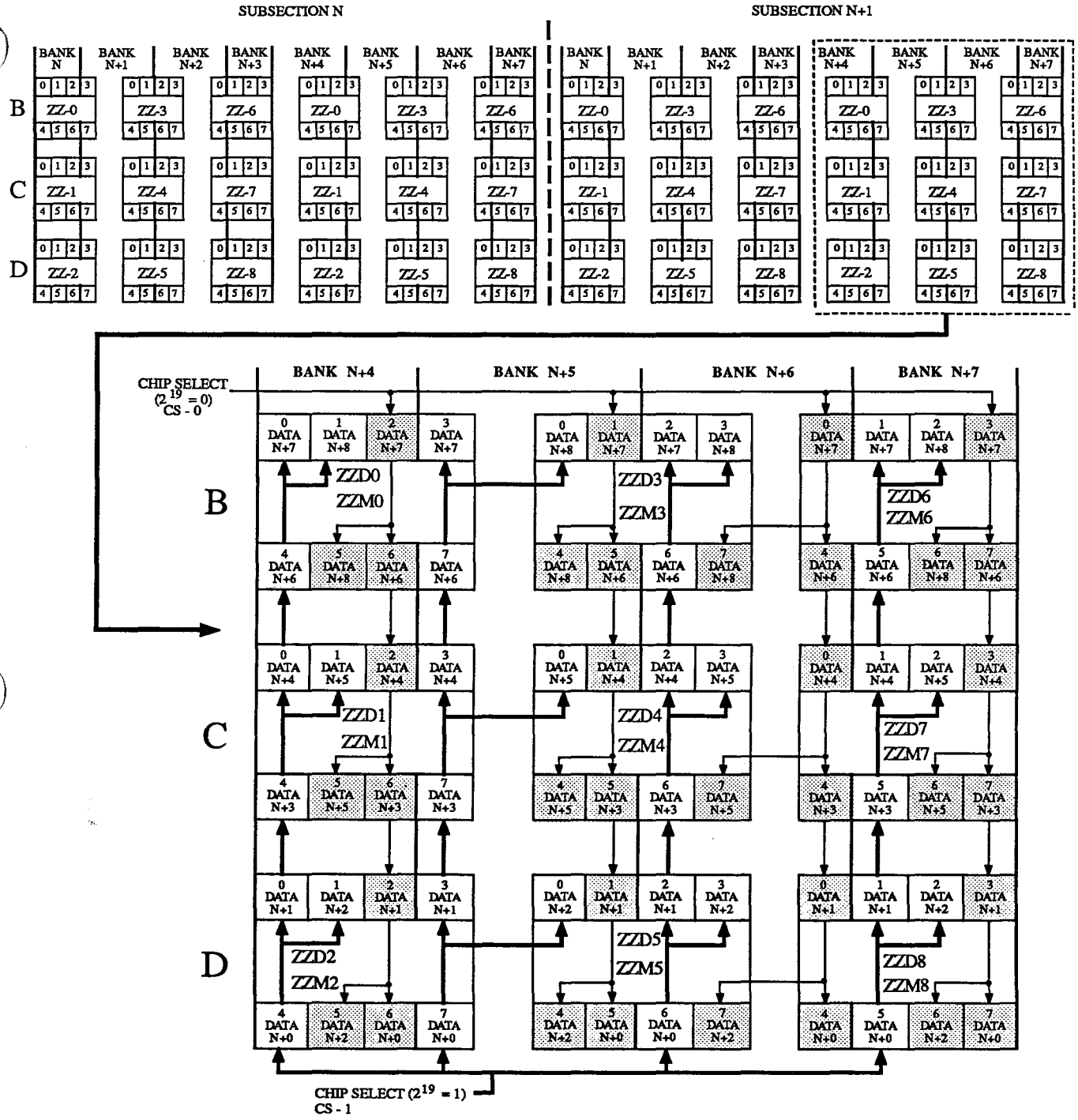
CRAY Y-MP MEMORY BOARD A/C SUBSECTION 0/4
BANKS (N + 4 - N + 7) (64K x 1) LOCATOR



NOTE: EACH BANK HAS 18 MEMORY CHIPS (64K x 1) WHICH IS DIVIDED INTO 9 DATA BITS PER MODULE (N+0 - N+8) AND TWO CHIP SELECTS ($2^{19} = 0, 2^{19} = 1$)

Hardware Trng. A-5914 J.E.S.

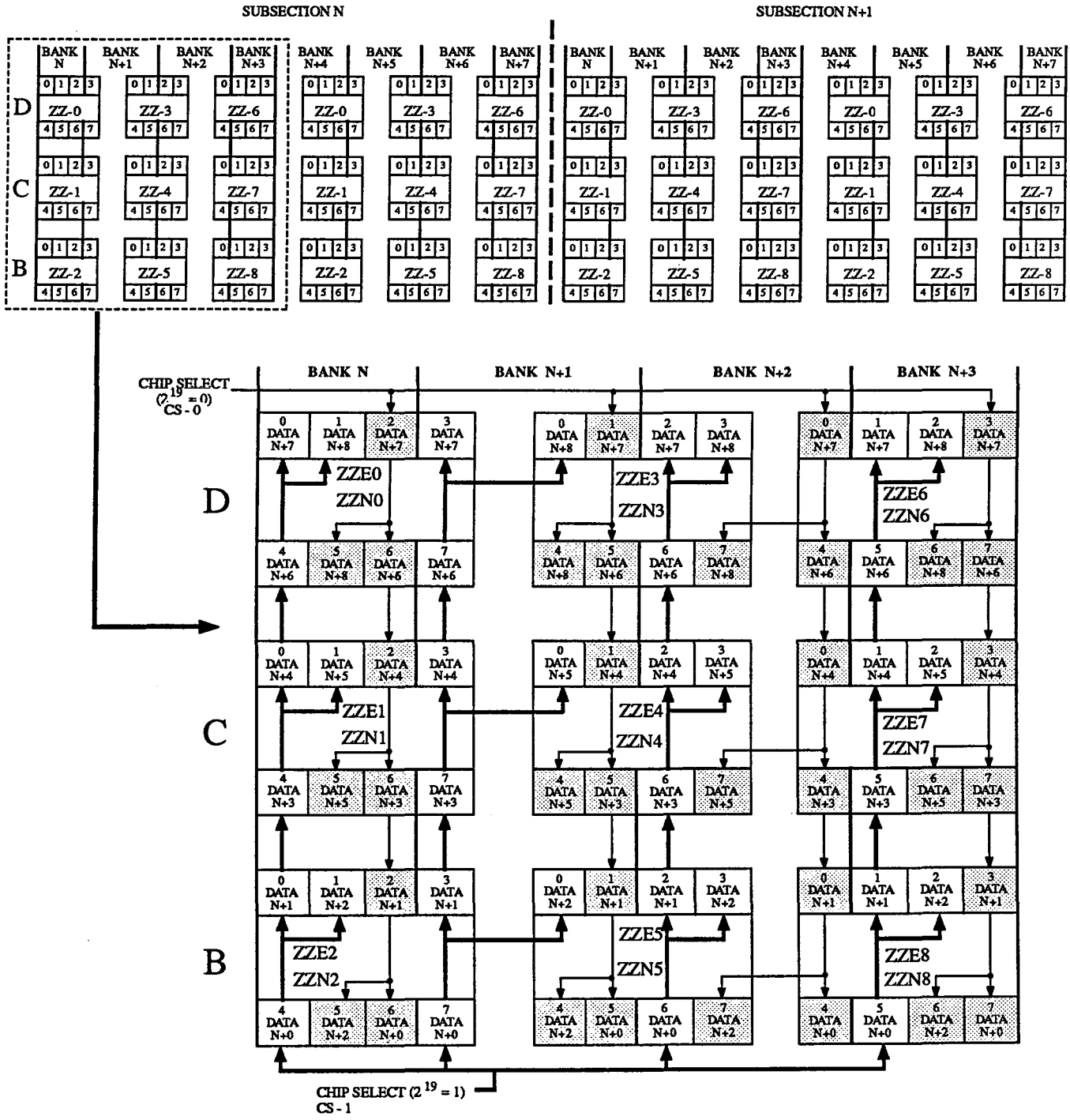
CRAY Y-MP MEMORY BOARD A/C SUBSECTION 1/5
BANKS (N - N + 3) (64K x 1) LOCATOR



NOTE: EACH BANK HAS 18 MEMORY CHIPS (64K x 1) WHICH IS DIVIDED INTO 9 DATA BITS PER MODULE (N+0 - N+8) AND TWO CHIP SELECTS ($2^{19} = 0$, $2^{19} = 1$)

Hardware Tmg. A-5915 J.E.S.

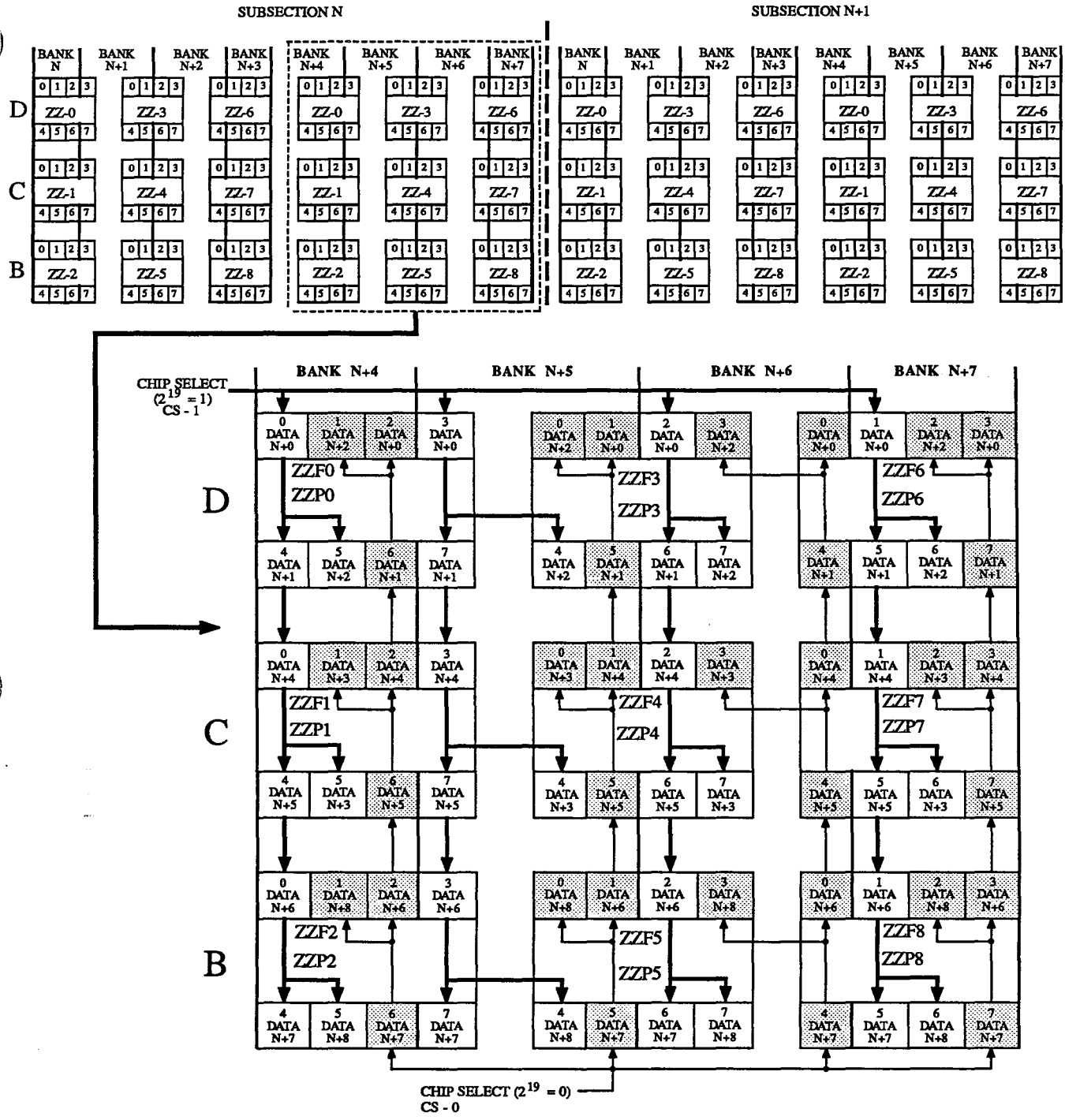
CRAY Y-MP MEMORY BOARD A/C SUBSECTION 1/5 BANKS (N + 4 - N + 7) (64K x 1) LOCATOR



NOTE: EACH BANK HAS 18 MEMORY CHIPS (64K x 1) WHICH IS DIVIDED INTO 9 DATA BITS PER MODULE (N+0 - N+8) AND TWO CHIP SELECTS (2^{19} = 0, 2^{19} = 1)

Hardware Trng. A-4889B J.E.S.

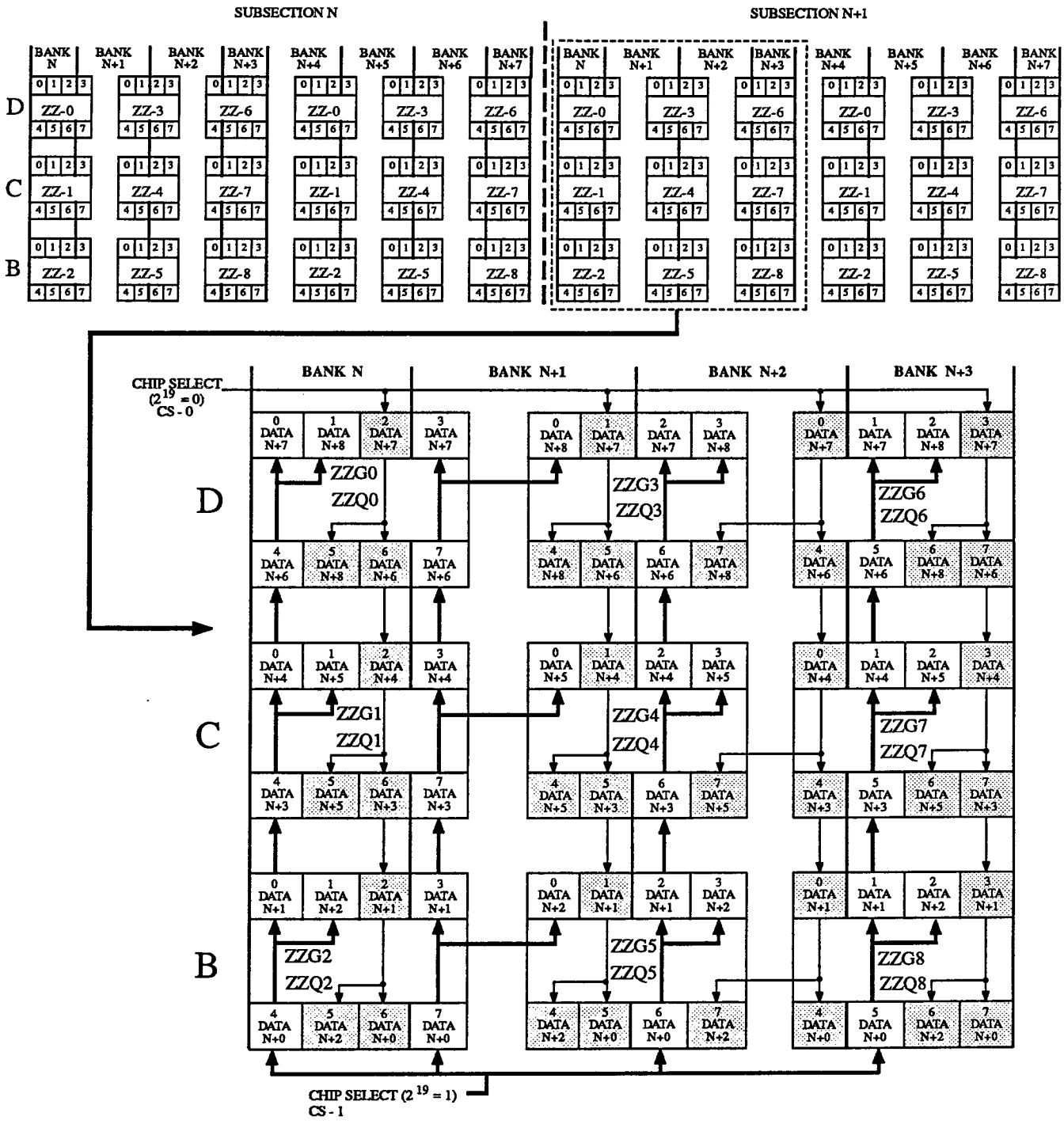
CRAY Y-MP MEMORY BOARD B/D SUBSECTION 2/6
BANKS (N - N + 3) (64K x 1) LOCATOR



NOTE: EACH BANK HAS 18 MEMORY CHIPS (64K x 1) WHICH IS DIVIDED INTO 9 DATA BITS PER MODULE (N+0 - N+8) AND TWO CHIP SELECTS ($2^{19} = 0, 2^{19} = 1$)

Hardware Trng. A-4891 J.E.S.

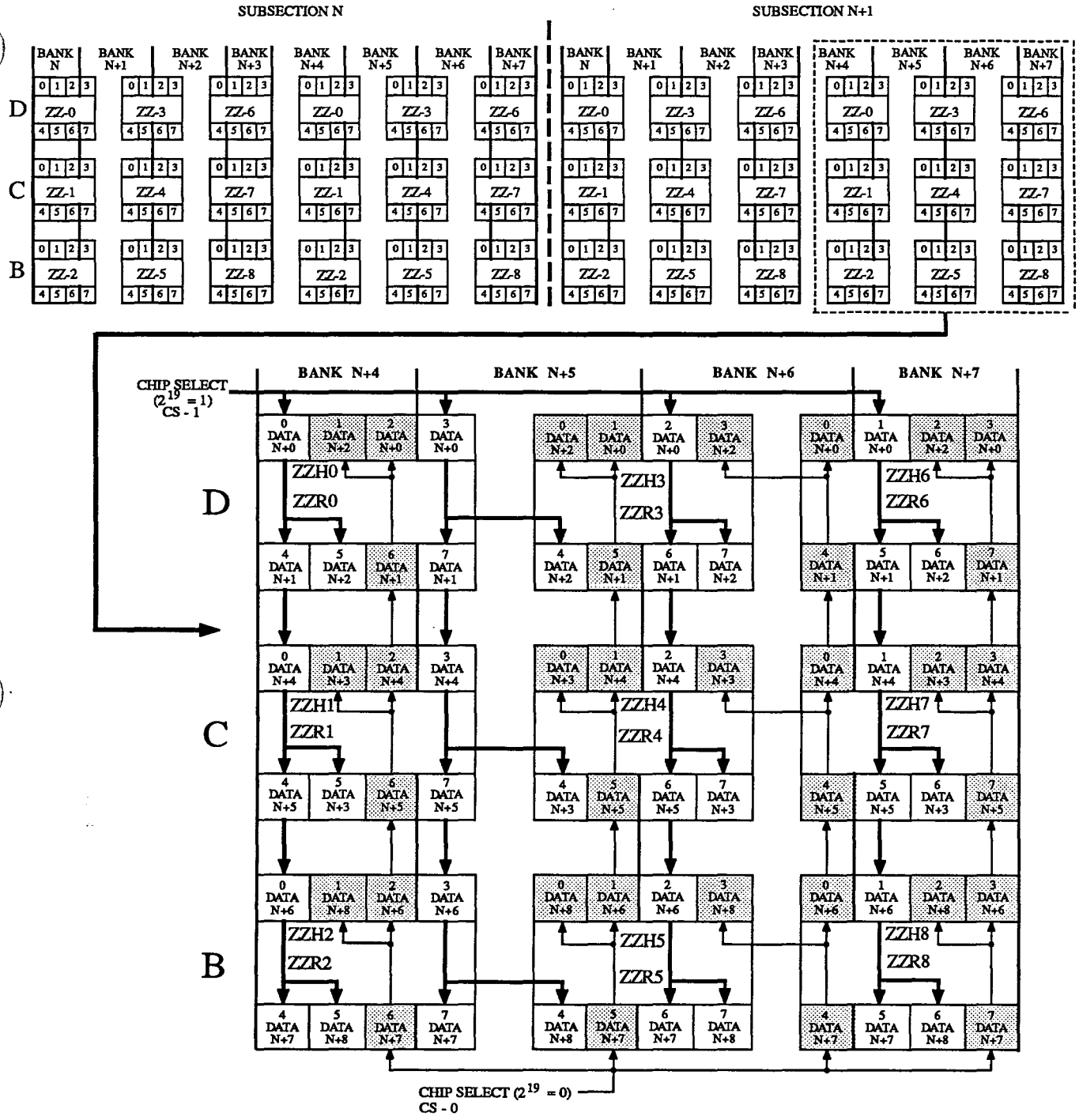
CRAY Y-MP MEMORY BOARD B/D SUBSECTION 2/6 BANKS (N + 4 - N + 7) (64K x 1) LOCATOR



NOTE: EACH BANK HAS 18 MEMORY CHIPS (64K x 1) WHICH IS DIVIDED INTO 9 DATA BITS PER MODULE (N+0 - N+8) AND TWO CHIP SELECTS (2^{19}= 0, 2 ^{19}= 1)

Hardware Trng. A-5916A J.E.S.

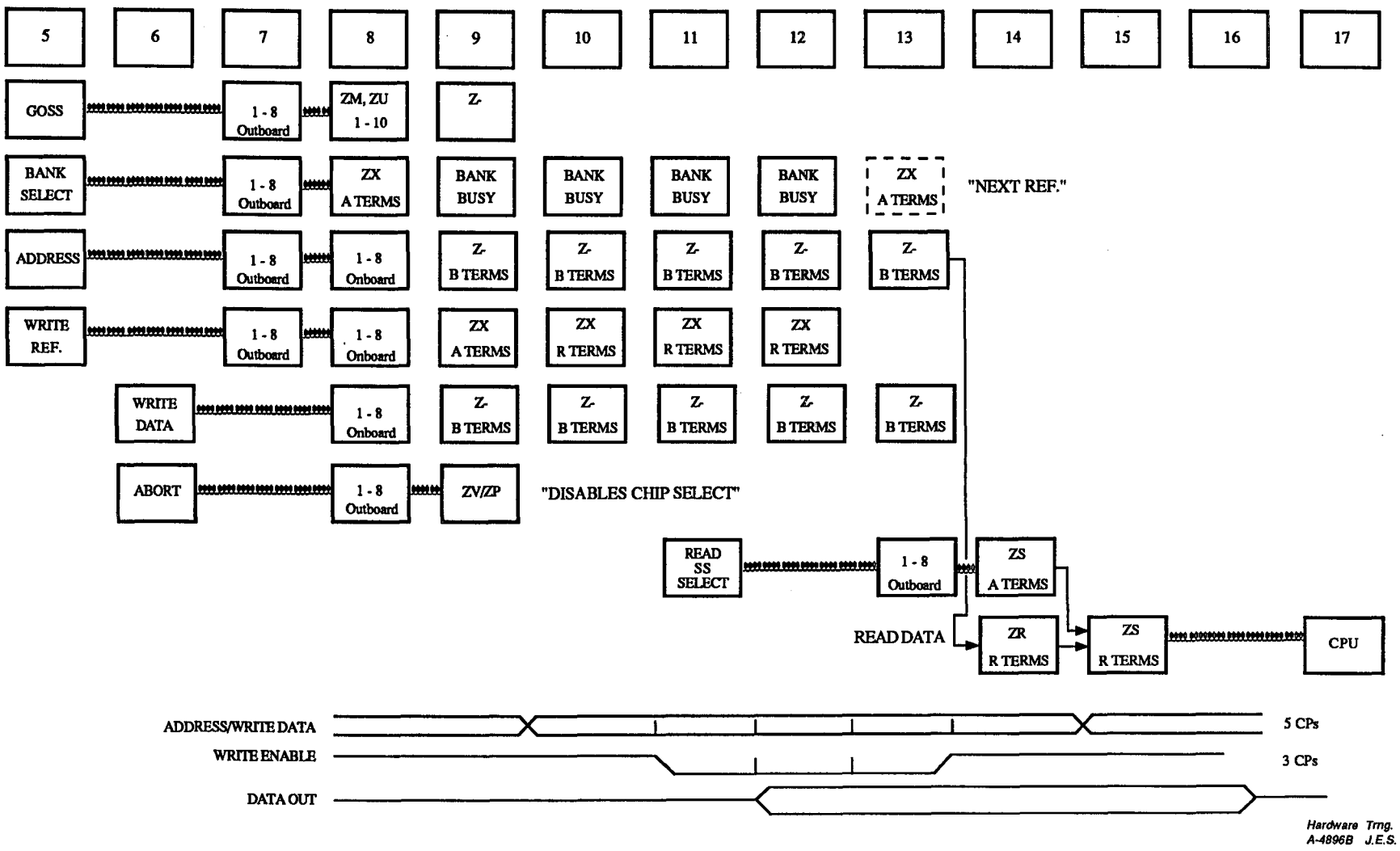
CRAY Y-MP MEMORY BOARD B/D SUBSECTION 3/7
BANKS (N - N + 3) (64K x 1) LOCATOR



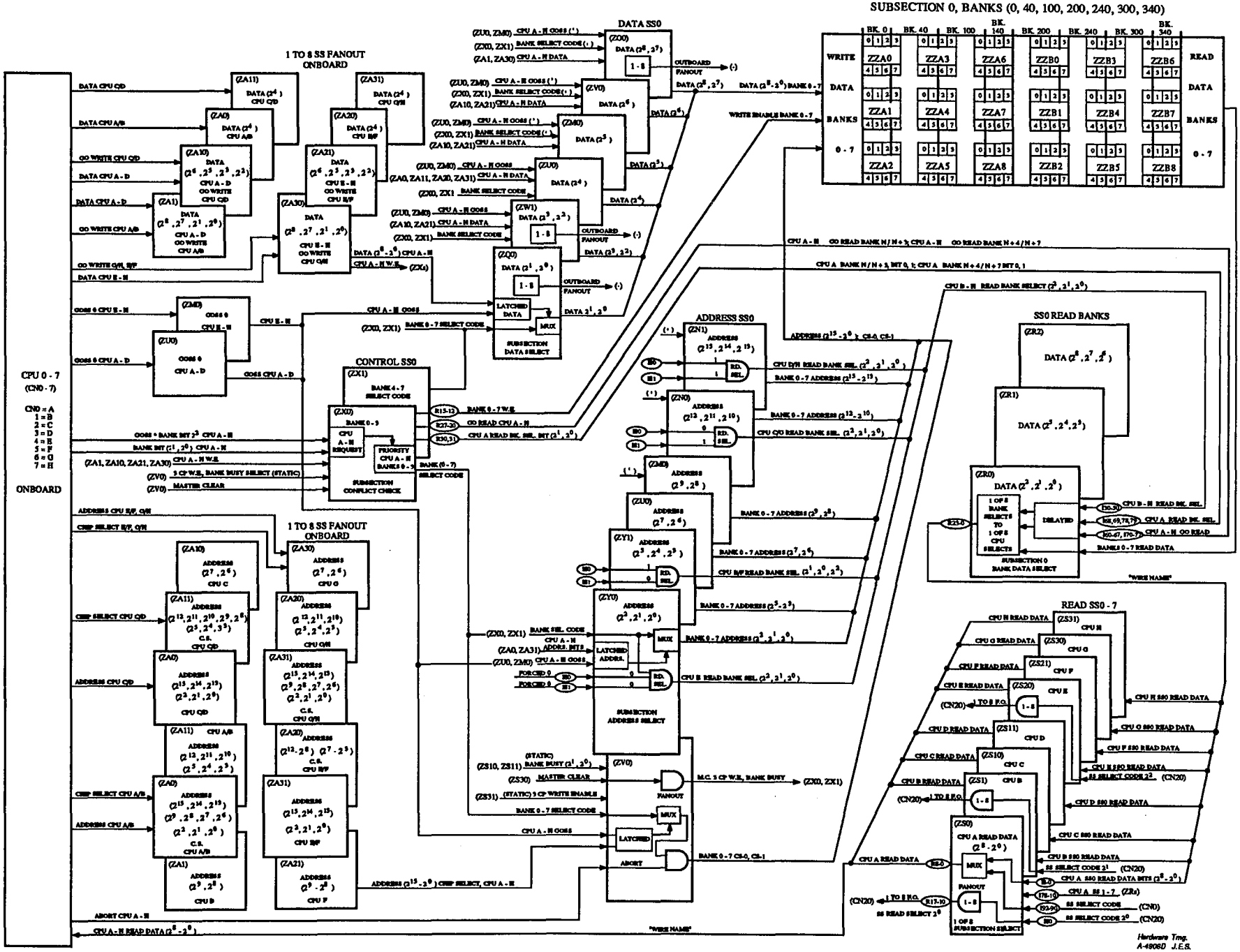
NOTE: EACH BANK HAS 18 MEMORY CHIPS (64K x 1) WHICH IS DIVIDED INTO 9 DATA BITS PER MODULE (N+0 - N+8) AND TWO CHIP SELECTS ($2^{19} = 0, 2^{19} = 1$)

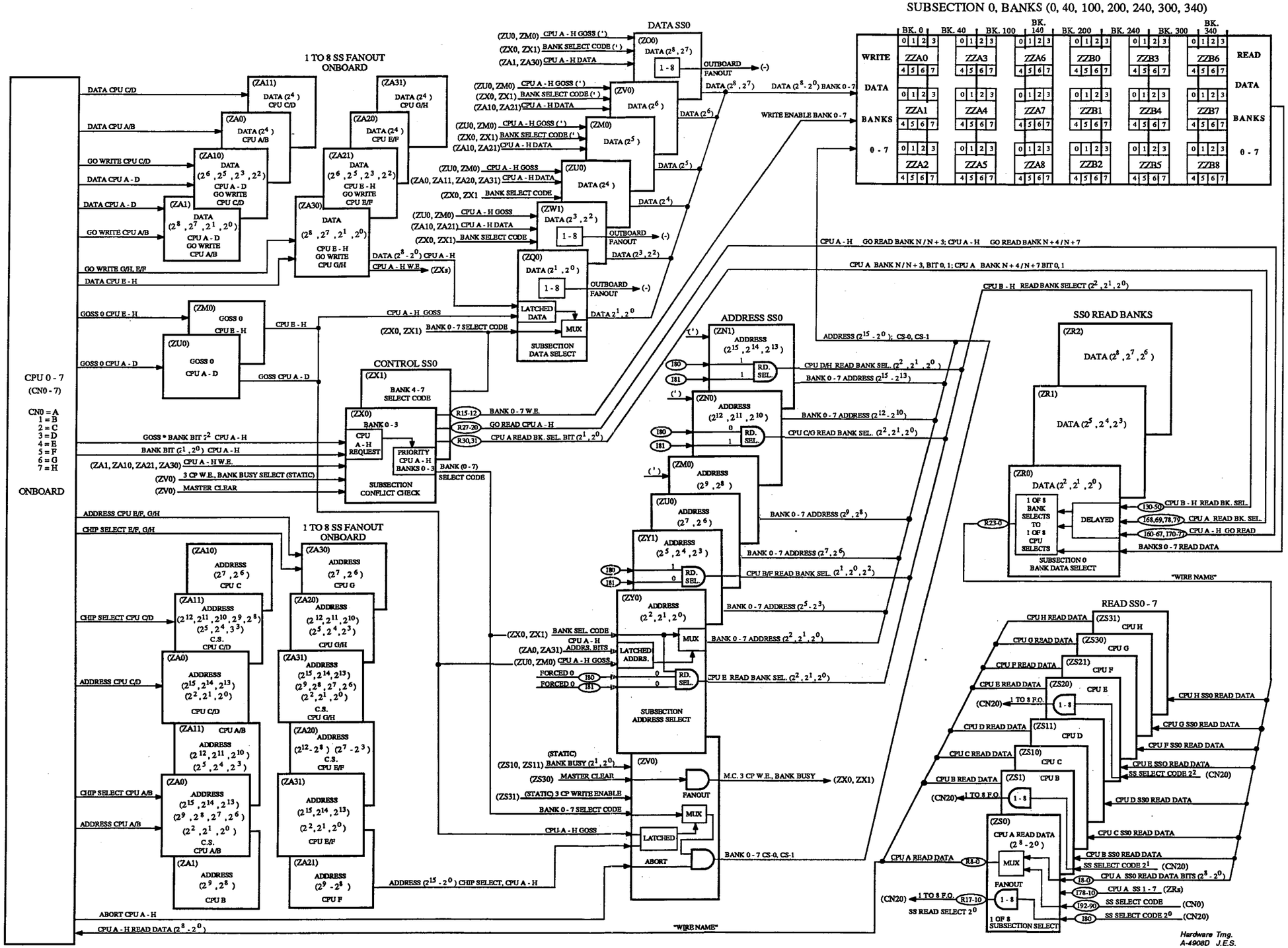
Hardware Tmg. A-5917 J.E.S.

CRAY Y-MP MEMORY BOARD B/D SUBSECTION 3/7 BANKS (N + 4 - N + 7) (64K x 1) LOCATOR



CRAY Y-MP MEMORY TIMING (64K x 1)


SUBSECTION 0, BANKS (0, 40, 100, 200, 240, 300, 340)
BK. 0
BK. 40
BK. 100
BK. 140
BK. 200
BK. 240
BK. 300
BK. 340
WRITE DATA BANKS 0 - 7
READ DATA BANKS 0 - 7
ZZA0
ZZA1
ZZA2
ZZA3
ZZA4
ZZA5
ZZA6
ZZA7
ZZA8
ZZB0
ZZB1
ZZB2
ZZB3
ZZB4
ZZB5
ZZB6
ZZB7
ZZB8
DATA SS0
1 TO 8 SS FANOUT ONBOARD
CONTROL SS0
ADDRESS SS0
SS0 READ BANKS
READ SS0 - 7
CPU 0 - 7 (CN0 - 7)
ONBOARD
CRAY Y-MP MEMORY BLOCK DIAGRAM (64k x 1) SUBSECTION 0 CPU A - H



CRAY Y-MP MEMORY BLOCK DIAGRAM (64K x 1) SUBSECTION 0 CPU A - H

WRITE DATA SELECT CPU 0 - 7

DATA	SS0	SS1	SS2	SS3	SS4	SS5	SS6	SS7
N + 0	ZQ0	ZO1	ZQ10	ZO11	ZQ20	ZO21	ZQ30	ZO31
N + 1	ZQ0	ZO1	ZQ10	ZO11	ZQ20	ZO21	ZQ30	ZO31
N + 2	ZW1	ZV1	ZW11	ZP11	ZW21	ZV21	ZW31	ZP31
N + 3	ZW1	ZM1	ZW11	ZM11	ZW21	ZM21	ZW31	ZM31
N + 4	ZU0	ZU1	ZU10	ZU11	ZU20	ZU21	ZU30	ZU31
N + 5	ZM0	ZW2	ZM10	ZW12	ZM20	ZW22	ZM30	ZW32
N + 6	ZV0	ZW2	ZP10	ZW12	ZV20	ZW22	ZP30	ZW32
N + 7	ZO0	ZQ3	ZO10	ZQ13	ZO20	ZQ23	ZO30	ZQ33
N + 8	ZO0	ZQ3	ZO10	ZQ13	ZO20	ZQ23	ZO30	ZQ33

ADDRESS SELECT CPU 0 - 7

ADDRS.	SS0	SS1	SS2	SS3	SS4	SS5	SS6	SS7
2^0	ZY0	ZN2	ZY10	ZY12	ZY20	ZN22	ZY30	ZN32
2^1	ZY0	ZN2	ZY10	ZY12	ZY20	ZN22	ZY30	ZN32
2^2	ZY0	ZN2	ZY10	ZY12	ZY20	ZN22	ZY30	ZN32
2^3	ZY1	ZN3	ZY11	ZN13	ZY21	ZN23	ZY31	ZN33
2^4	ZY1	ZN3	ZY11	ZN13	ZY21	ZN23	ZY31	ZN33
2^5	ZY1	ZN3	ZY11	ZN13	ZY21	ZN23	ZY31	ZN33
2^6	ZU0	ZM1	ZU10	ZM11	ZU20	ZM21	ZU30	ZM31
2^7	ZU0	ZM1	ZU10	ZM11	ZU20	ZM21	ZU30	ZM31
2^8	ZM0	ZU1	ZM10	ZU11	ZM20	ZU21	ZM30	ZU31
2^9	ZM0	ZU1	ZM10	ZU11	ZM20	ZU21	ZM30	ZU31
2^{10}	ZN0	ZY2	ZN10	ZY12	ZN20	ZY22	ZN30	ZY32
2^{11}	ZN0	ZY2	ZN10	ZY12	ZY20	ZY22	ZN30	ZY32
2^{12}	ZN0	ZY2	ZN10	ZY12	ZN20	ZY22	ZN30	ZY32
2^{13}	ZN1	ZY3	ZN11	ZY13	ZN21	ZY23	ZN31	ZY33
2^{14}	ZN1	ZY3	ZN11	ZY13	ZN21	ZY23	ZN31	ZY33
2^{15}	ZN1	ZY3	ZN11	ZY13	ZN21	ZY23	ZN31	ZY33

Hardware Trng.
A-4866B J.E.S.

CRAY Y-MP SUBSECTION 0 - 7 CROSS REFERENCE

SUBSECTION CONTROL

CPU 0 - 7

CONFLICT CHECKS	SS0	SS1	SS2	SS3	SS4	SS5	SS6	SS7
BANKS 0 - 3	ZX0	ZX2	ZX10	ZX12	ZX20	ZX22	ZX30	ZX32
BANKS 4 - 7	ZX1	ZX3	ZX11	ZX13	ZX21	ZX23	ZX31	ZX33

READ DATA (ZRs)

CPU 0 - 7

	SS0	SS1	SS2	SS3	SS4	SS5	SS6	SS7
DATA $2^2, 2^1, 2^0$	ZR0	ZR3	ZR10	ZR13	ZR20	ZR23	ZR30	ZR33
DATA $2^5, 2^4, 2^3$	ZR1	ZR4	ZR11	ZR14	ZR21	ZR24	ZR31	ZR34
DATA $2^8, 2^7, 2^6$	ZR2	ZR5	ZR12	ZR15	ZR22	ZR25	ZR32	ZR35

GO SUBSECTION GOSS

CPU A - H

CPUs	SS0	SS1	SS2	SS3	SS4	SS5	SS6	SS7
CPU A - D	ZU0	ZU1	ZM10	ZM11	ZU20	ZU21	ZM30	ZM31
CPU E - H	ZM0	ZM1	ZU10	ZU11	ZM20	ZM21	ZU30	ZU31

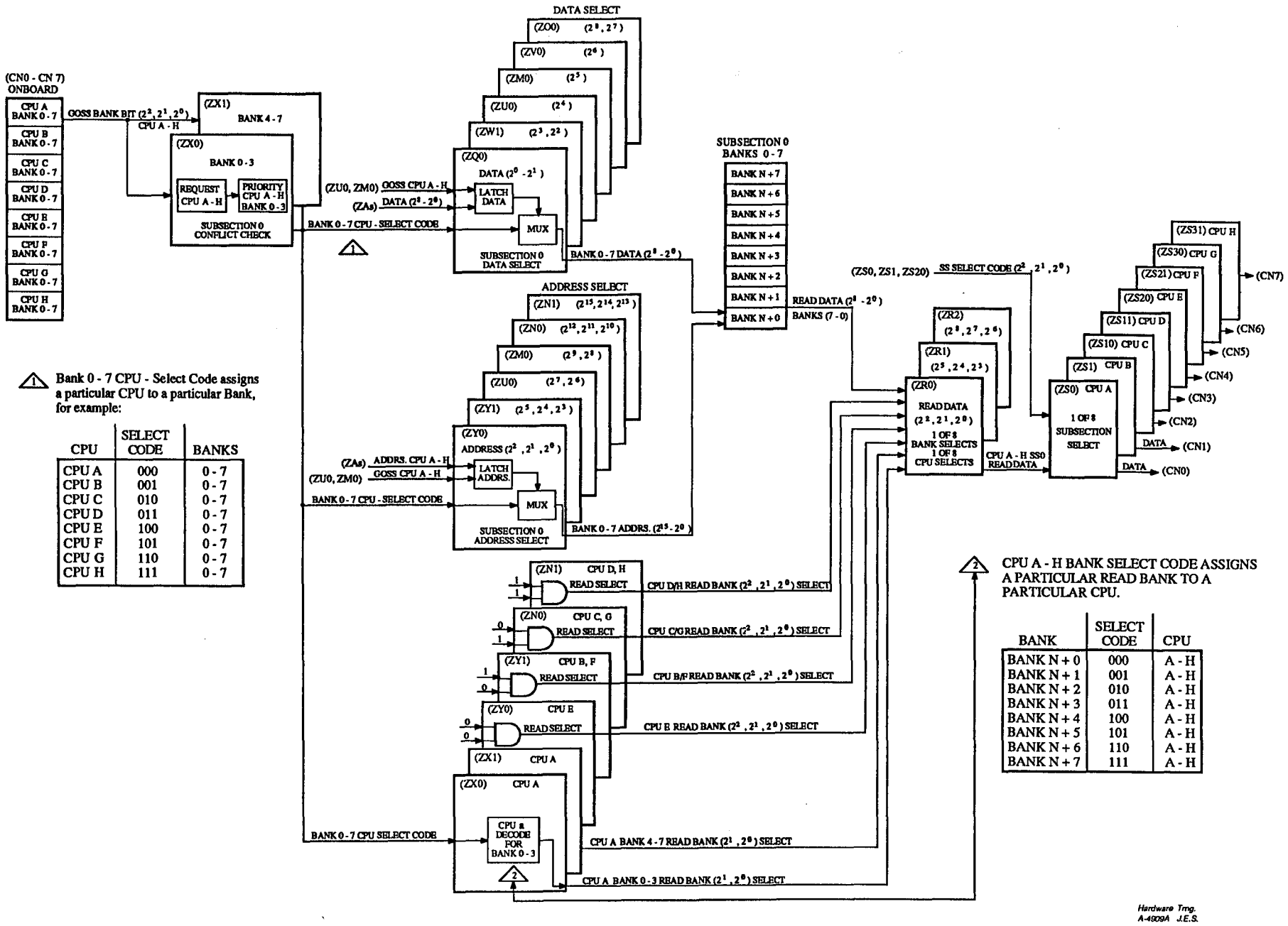
SUBSECTION CHIP SELECT/ABORT

CPU 0 - 7

CHIP SELECT	SS0	SS1	SS2	SS3	SS4	SS5	SS6	SS7
C.S.	ZV0	ZV1	ZP10	ZP11	ZV20	ZV21	ZP30	ZP31

Hardware Trng.
A-4865B J.E.S.

CRAY Y-MP
SUBSECTION 0 - 7 CROSS REFERENCE



1 Bank 0 - 7 CPU - Select Code assigns a particular CPU to a particular Bank, for example:

CPU	SELECT CODE	BANKS
CPU A	000	0 - 7
CPU B	001	0 - 7
CPU C	010	0 - 7
CPU D	011	0 - 7
CPU E	100	0 - 7
CPU F	101	0 - 7
CPU G	110	0 - 7
CPU H	111	0 - 7

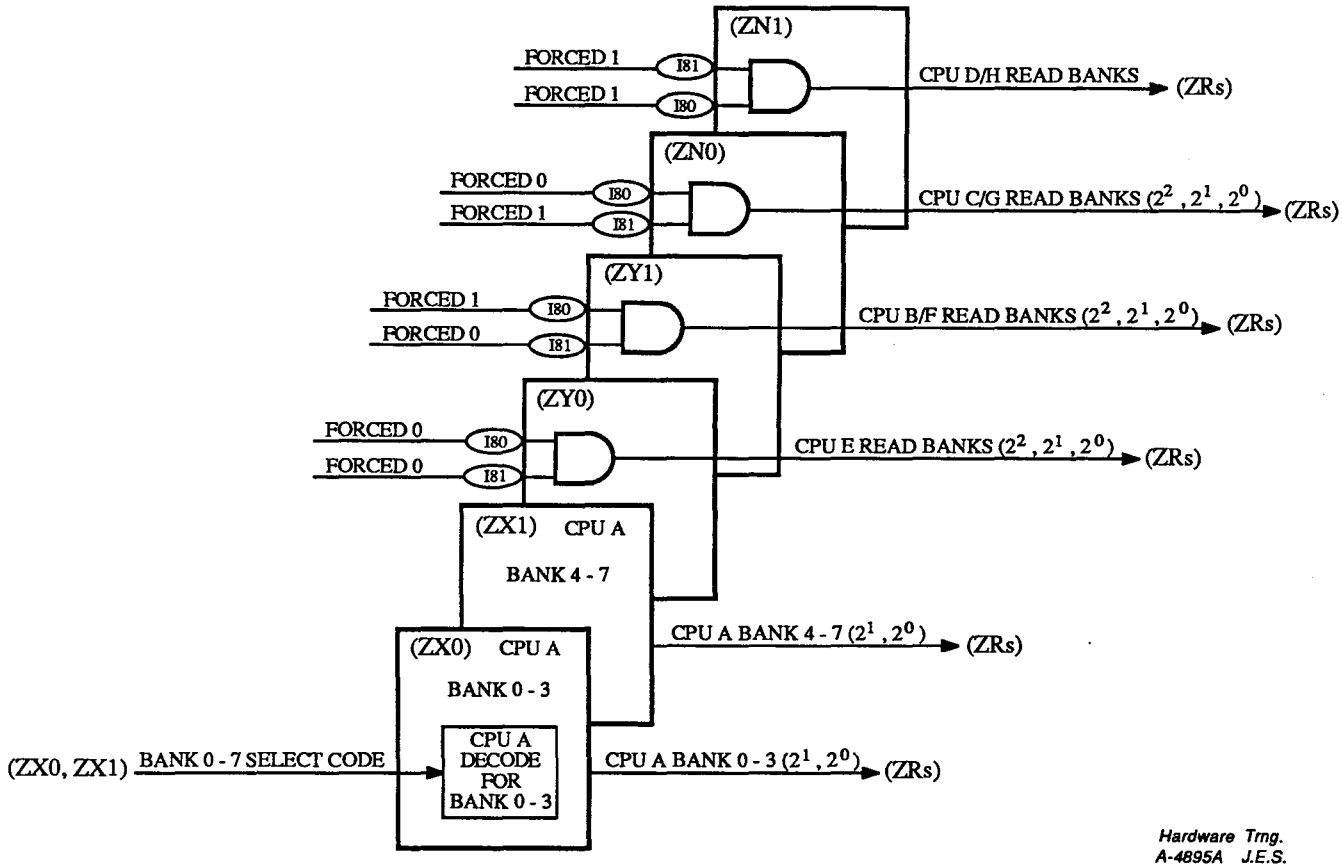
2 CPU A - H BANK SELECT CODE ASSIGNS A PARTICULAR READ BANK TO A PARTICULAR CPU.

BANK	SELECT CODE	CPU
BANK N + 0	000	A - H
BANK N + 1	001	A - H
BANK N + 2	010	A - H
BANK N + 3	011	A - H
BANK N + 4	100	A - H
BANK N + 5	101	A - H
BANK N + 6	110	A - H
BANK N + 7	111	A - H

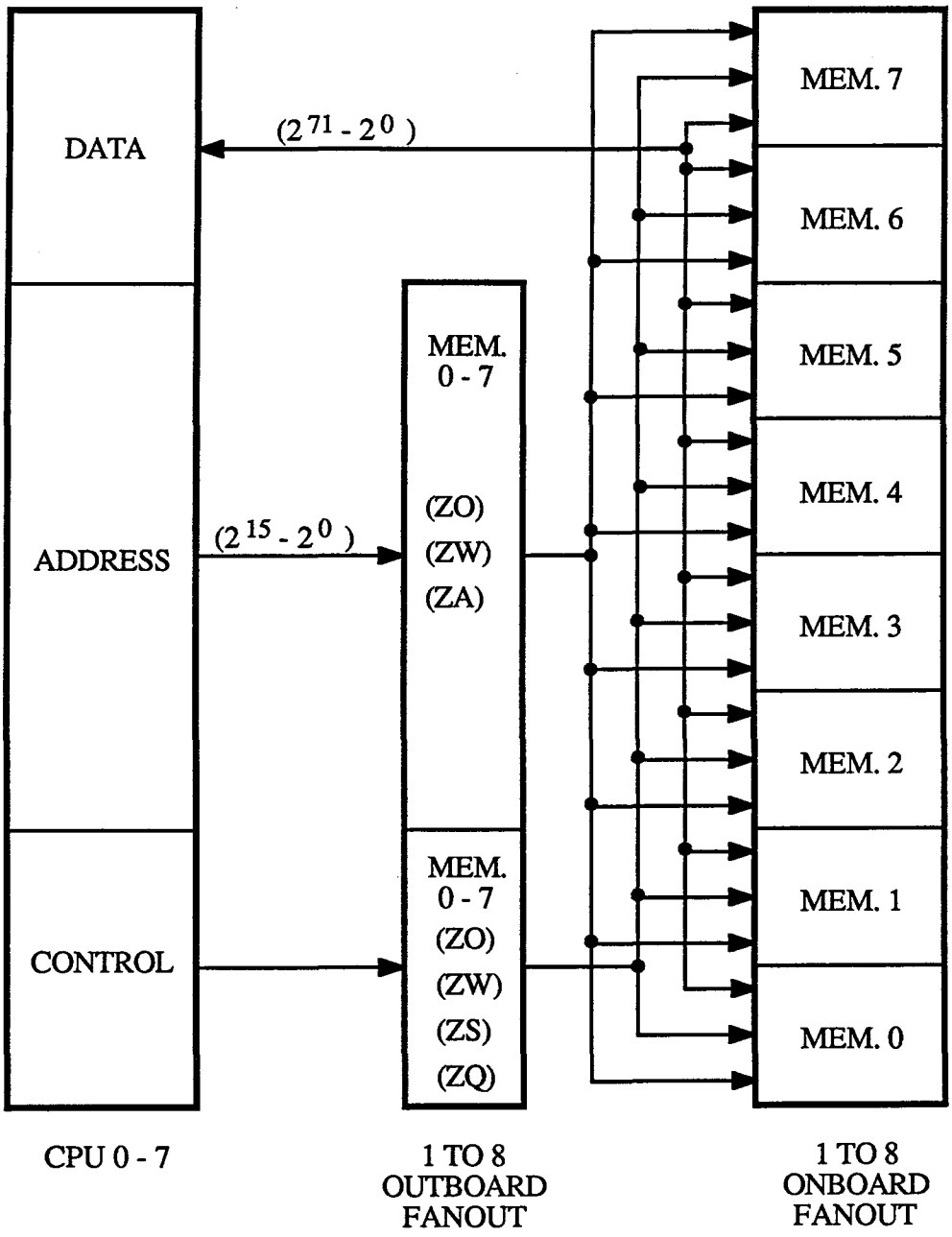
CRAY Y-MP MEMORY CPU SELECT CODES SUBSECTION 0

CPU A - H	SS0	SS1	SS2	SS3	SS4	SS5	SS6	SS7
CPU A	ZX0, ZX1	ZX2, ZX3	ZX10, ZX11	ZX12, ZX13	ZX20, ZX21	ZX22, ZX23	ZX30, ZX31	ZX32, ZX33
CPU B	ZY1	ZY2	ZY11	ZY12	ZY21	ZY22	ZY31	ZY32
CPU C	ZN0	ZN3	ZN10	ZN13	ZN20	ZN23	ZN30	ZN33
CPU D	ZN1	ZN2	ZN11	ZN12	ZN21	ZN22	ZN31	ZN32
CPU E	ZY0	ZY3	ZY10	ZY13	ZY20	ZY23	ZY30	ZY33
CPU F	ZY1	ZY2	ZY11	ZY12	ZY21	ZY22	ZY31	ZY32
CPU G	ZN0	ZN3	ZN10	ZN13	ZN20	ZN23	ZN30	ZN33
CPU H	ZN1	ZN2	ZN11	ZN12	ZN21	ZN22	ZN31	ZN32

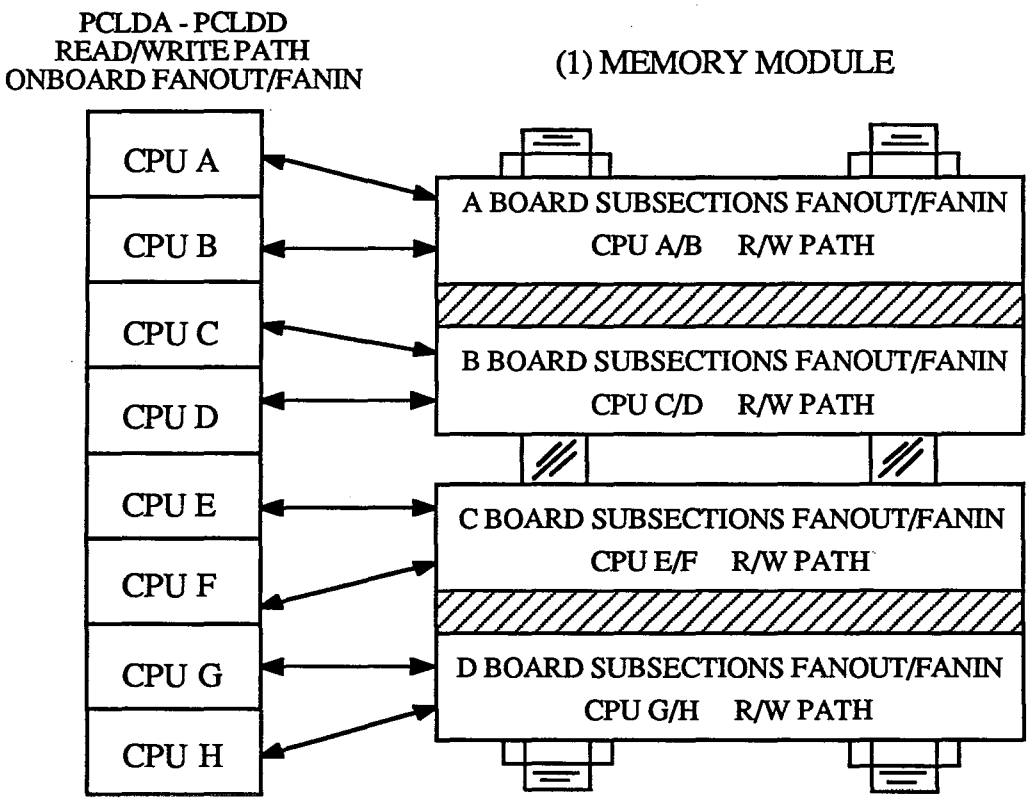
CRAY Y-MP READ BANK SELECTS (2^2, 2^1, 2^0) CROSS REFERENCE



CRAY Y-MP SUBSECTION 0 READ BANK SELECT (2^2, 2^1, 2^0)



MEMORY MODULE OUTBOARD FANOUT



CPU (A - H) PRIORITY SECTION 0

SUBSECTION ACCESSED	CPU NUMBER 0	1	2	3	7	6	5	4
	CPU LETTER A	B	C	D	E	F	G	H
0	(ZX-) I0-	I1-	I2-	I3-	I4-	I5-	I6-	I7-
1	(ZX-) I0-	I1-	I2-	I3-	I4-	I5-	I6-	I7-
2	(ZX-) I7-	I6-	I5-	I4-	I3-	I2-	I1-	I0-
3	(ZX-) I7-	I6-	I5-	I4-	I3-	I2-	I1-	I0-
4	(ZX-) I0-	I1-	I2-	I3-	I4-	I5-	I6-	I7-
5	(ZX-) I0-	I1-	I2-	I3-	I4-	I5-	I6-	I7-
6	(ZX-) I7-	I6-	I5-	I4-	I3-	I2-	I1-	I0-
7	(ZX-) I7-	I6-	I5-	I4-	I3-	I2-	I1-	I0-

A - highest

H - lowest

Hardware Trng.
A-4864B J.E.S.

CRAY Y-MP MEMORY FANOUT AND PRIORITY

LOC.	1	MEM. 0	1 - 8	BANK BUSY 2^0 (MEM.)
	2	1	1 - 8	BANK BUSY 2^1 (MEM.)
	3	2	1 - 8	I/O M.C.
	4	3	1 - 8	3 CP W.E.
	5	4	1 - 8	
	6	5	1 - 8	
	7	6	1 - 8	
	8	7	1 - 3	I/O M.C.
LOC.	9	MEM. 10	1 - 8	BANK BUSY 2^0 (MEM.)
	10	11	1 - 8	BANK BUSY 2^1 (MEM.)
	11	12	1 - 8	I/O M.C.
	12	13	1 - 8	3 CP W.E.
	13	14	1 - 8	CPU M.C.
	14	15	1 - 8	I/O M.C.
	15	16	1 - 8	
	16	17	1 - 8	
LOC.	17	CPU 0		
	18	1		
	19	2		
	20	3		
	21	4		
	22	5		
	23	6		
	24	7		
LOC.	25	MEM. 20	1 - 8	BANK BUSY 2^0 (MEM.)
	26	21	1 - 8	BANK BUSY 2^1 (MEM.)
	27	22	1 - 8	I/O M.C.
	28	23	1 - 8	3 CP W.E.
	29	24	1 - 8	
	30	25	1 - 8	
	31	26	1 - 2	I/O M.C.
	32	27	1 - 8	
LOC.	33	MEM. 30	1 - 8	BANK BUSY 2^0 (MEM.)
	34	31	1 - 8	BANK BUSY 2^1 (MEM.)
	35	32	1 - 8	I/O M.C.
	36	33	1 - 8	3 CP W.E.
	37	34	1 - 8	
	38	35	1 - 8	BANK BUSY BIT 0 (5 - 8) CPU
	39	36	1 - 8	BANK BUSY BIT 1 (5 - 8) CPU
	40	37	1 - 8	BANK BUSY SEL. (4 CP) CPU
	41	CLOCK		

A-6434

CRAY Y-MP 8/32 MODULE LOCATION

ADDRESS BIT	ADDRESS ONBOARD FANOUT							
	CPU A	CPU B	CPU C	CPU D	CPU E	CPU F	CPU G	CPU H
2^0	ZA0 R27	ZA0 R24	ZA0 R21	ZA0 R18	ZA31 R11	ZA31 R8	ZA31 R5	ZA31 R2
2^1	ZA0 R26	ZA0 R23	ZA0 R20	ZA0 R17	ZA31 R10	ZA31 R7	ZA31 R4	ZA31 R1
2^2	ZA0 R25	ZA0 R22	ZA0 R19	ZA0 R16	ZA31 R9	ZA31 R6	ZA31 R3	ZA31 R0
2^3	ZA11 R11	ZA11 R8	ZA11 R5	ZA11 R2	ZA20 R27	ZA20 R24	ZA20 R21	ZA20 R18
2^4	ZA11 R10	ZA11 R7	ZA11 R4	ZA11 R1	ZA20 R26	ZA20 R23	ZA20 R20	ZA20 R17
2^5	ZA11 R9	ZA11 R6	ZA11 R3	ZA11 R0	ZA20 R25	ZA20 R22	ZA20 R19	ZA20 R16
2^6	ZA0 R28	ZA0 R30	ZA10 R32	ZA11 R32	ZA20 R28	ZA20 R30	ZA30 R32	ZA31 R32
2^7	ZA0 R29	ZA0 R31	ZA10 R33	ZA11 R33	ZA20 R29	ZA20 R31	ZA30 R33	ZA31 R33
2^8	ZA0 R32	ZA1 R32	ZA11 R28	ZA11 R30	ZA20 R32	ZA21 R32	ZA31 R16	ZA31 R18
2^9	ZA0 R33	ZA1 R33	ZA11 R29	ZA11 R31	ZA20 R33	ZA21 R33	ZA31 R17	ZA31 R19
2^{10}	ZA11 R27	ZA11 R24	ZA11 R21	ZA11 R18	ZA20 R11	ZA20 R8	ZA20 R5	ZA20 R2
2^{11}	ZA11 R26	ZA11 R23	ZA11 R20	ZA11 R17	ZA20 R10	ZA20 R7	ZA20 R4	ZA20 R1
2^{12}	ZA11 R25	ZA11 R22	ZA11 R19	ZA11 R16	ZA20 R9	ZA20 R6	ZA20 R3	ZA20 R0
2^{13}	ZA0 R11	ZA0 R8	ZA0 R5	ZA0 R2	ZA31 R20	ZA31 R23	ZA31 R26	ZA31 R29
2^{14}	ZA0 R10	ZA0 R7	ZA0 R4	ZA0 R1	ZA31 R21	ZA31 R24	ZA31 R27	ZA31 R30
2^{15}	ZA0 R9	ZA0 R6	ZA0 R3	ZA0 R0	ZA31 R22	ZA31 R25	ZA31 R28	ZA31 R31
CHIP SELECT 2^0	ZA0 R14	ZA0 R15	ZA11 R14	ZA11 R15	ZA20 R14	ZA20 R15	ZA31 R14	ZA31 R15
GO WRITE	ZA1	ZA1	ZA10	ZA10	ZA21	ZA21	ZA30	ZA30

DATA BIT	DATA ONBOARD FANOUT							
	CPU A	CPU B	CPU C	CPU D	CPU E	CPU F	CPU G	CPU H
$N+2^0$	ZA1 R16	ZA1 R18	ZA1 R20	ZA1 R22	ZA30 R15	ZA30 R13	ZA30 R11	ZA30 R9
$N+2^1$	ZA1 R17	ZA1 R19	ZA1 R21	ZA1 R23	ZA30 R14	ZA30 R12	ZA30 R10	ZA30 R8
$N+2^2$	ZA10 R0	ZA10 R2	ZA10 R4	ZA10 R6	ZA21 R16	ZA21 R18	ZA21 R20	ZA21 R22
$N+2^3$	ZA10 R1	ZA10 R3	ZA10 R5	ZA10 R7	ZA21 R17	ZA21 R19	ZA21 R21	ZA21 R23
$N+2^4$	ZA0 R12	ZA0 R13	ZA11 R12	ZA13 R13	ZA20 R12	ZA20 R13	ZA31 R12	ZA31 R13
$N+2^5$	ZA10 R22	ZA10 R20	ZA10 R18	ZA10 R16	ZA21 R6	ZA21 R4	ZA21 R2	ZA21 R0
$N+2^6$	ZA10 R23	ZA10 R21	ZA10 R19	ZA10 R17	ZA21 R7	ZA21 R5	ZA21 R3	ZA21 R1
$N+2^7$	ZA1 R6	ZA1 R4	ZA1 R2	ZA1 R0	ZA30 R22	ZA30 R20	ZA30 R18	ZA30 R16
$N+2^8$	ZA1 R7	ZA1 R5	ZA1 R3	ZA1 R1	ZA30 R23	ZA30 R21	ZA30 R19	ZA30 R17

Hardware Trng.
A-6628A J.E.S.

CRAY Y-MP ONBOARD FANOUT ADDRESS/DATA

ADDRESS	CPU A	CPU B	CPU C	CPU D	CPU E	CPU F	CPU G	CPU H
2^0	ZW1 MEM. 0	ZW1 MEM. 1	ZO0 MEM. 0	ZO0 MEM. 1	ZO0 MEM. 6	ZO0 MEM. 7	ZW1 MEM. 6	ZW1 MEM. 7
2^1	ZW11 MEM. 0	ZW11 MEM. 1	ZO10 MEM. 0	ZO10 MEM. 1	ZO10 MEM. 6	ZO10 MEM. 7	ZW11 MEM. 6	ZW11 MEM. 7
2^2	ZW21 MEM. 0	ZW21 MEM. 1	ZO20 MEM. 0	ZO20 MEM. 1	ZO20 MEM. 6	ZO20 MEM. 7	ZW21 MEM. 6	ZW21 MEM. 7
2^3	ZW31 MEM. 0	ZW31 MEM. 1	ZO30 MEM. 0	ZO30 MEM. 1	ZO30 MEM. 6	ZO30 MEM. 7	ZW31 MEM. 6	ZW31 MEM. 7
2^4	ZO0 MEM. 0	ZO0 MEM. 1	ZO1 MEM. 0	ZO1 MEM. 1	ZO1 MEM. 6	ZO1 MEM. 7	ZO0 MEM. 6	ZO0 MEM. 7
2^5	ZO10 MEM. 0	ZO10 MEM. 1	ZO11 MEM. 0	ZO11 MEM. 1	ZO11 MEM. 6	ZO11 MEM. 7	ZO10 MEM. 6	ZO10 MEM. 7
2^6	ZO20 MEM. 0	ZO20 MEM. 1	ZO21 MEM. 0	ZO21 MEM. 1	ZO21 MEM. 6	ZO21 MEM. 7	ZO20 MEM. 6	ZO20 MEM. 7
2^7	ZO30 MEM. 0	ZO30 MEM. 1	ZO30 MEM. 2	ZO30 MEM. 3	ZO30 MEM. 4	ZO30 MEM. 5	ZO30 MEM. 6	ZO30 MEM. 7
2^8	ZA1 MEM. 0	ZA1 MEM. 1	ZA1 MEM. 2	ZA1 MEM. 3	ZA1 MEM. 4	ZA1 MEM. 5	ZA1 MEM. 6	ZA1 MEM. 7
2^9	ZA10 MEM. 0	ZA10 MEM. 1	ZA10 MEM. 2	ZA10 MEM. 3	ZA10 MEM. 4	ZA10 MEM. 5	ZA10 MEM. 6	ZA10 MEM. 7
2^{10}	ZA21 MEM. 0	ZA21 MEM. 1	ZA21 MEM. 2	ZA21 MEM. 3	ZA21 MEM. 4	ZA21 MEM. 5	ZA21 MEM. 6	ZA21 MEM. 7
2^{11}	ZA30 MEM. 0	ZA30 MEM. 1	ZA30 MEM. 2	ZA30 MEM. 3	ZA30 MEM. 4	ZA30 MEM. 5	ZA30 MEM. 6	ZA30 MEM. 7
2^{12}	ZO31 MEM. 0	ZO31 MEM. 1	ZO31 MEM. 2	ZO31 MEM. 3	ZO31 MEM. 4	ZO31 MEM. 5	ZO31 MEM. 6	ZO31 MEM. 7
2^{13}	ZO1 MEM. 0	ZO1 MEM. 1	ZW2 MEM. 0	ZW2 MEM. 1	ZW2 MEM. 6	ZW2 MEM. 7	ZO1 MEM. 6	ZO1 MEM. 7
2^{14}	ZO11 MEM. 0	ZO11 MEM. 1	ZW12 MEM. 0	ZW12 MEM. 1	ZW12 MEM. 6	ZW12 MEM. 7	ZO11 MEM. 6	ZO11 MEM. 7
2^{15}	ZO21 MEM. 0	ZO21 MEM. 1	ZW22 MEM. 0	ZW22 MEM. 1	ZW22 MEM. 6	ZW22 MEM. 7	ZO21 MEM. 6	ZO21 MEM. 7
CHIP SELECT 2^{16}	ZO31 MEM. 0	ZO31 MEM. 1	ZW32 MEM. 0	ZW32 MEM. 1	ZW32 MEM. 6	ZW32 MEM. 7	ZO31 MEM. 6	ZO31 MEM. 7
WRITE REFERENCE 2^{17}	ZO30 MEM. 2	ZO30 MEM. 3	ZO31 MEM. 2	ZO31 MEM.3	ZO31 MEM. 4	ZO31 MEM. 5	ZO3O MEM. 4	ZO30 MEM. 5

Hardware Trng.
A-4897A J.E.S.

1 TO 8 ADDRESS OUTBOARD FANOUT

ABORT FANOUT

ABORT	CPU A	CPU B	CPU C	CPU D	CPU E	CPU F	CPU G	CPU H
ABORT	ZO0 MEM. 2	ZO0 MEM. 3	ZO1 MEM. 2	ZO1 MEM. 3	ZO1 MEM. 4	ZO1 MEM. 5	ZO0 MEM. 4	ZO0 MEM. 5

GOSS FANOUT

GOSS	CPU A	CPU B	CPU C	CPU D	CPU E	CPU F	CPU G	CPU H
GOSS 0	ZQ0 MEM. 0	ZQ0 MEM. 1	ZQ0 MEM. 2	ZQ0 MEM. 3	ZQ0 MEM. 4	ZQ0 MEM. 5	ZQ0 MEM. 6	ZQ0 MEM. 7
GOSS 1	ZQ3 MEM. 0	ZQ3 MEM. 1	ZQ3 MEM. 2	ZQ3 MEM. 3	ZQ3 MEM. 4	ZQ3 MEM. 5	ZQ3 MEM. 6	ZQ3 MEM. 7
GOSS 2	ZQ10 MEM. 0	ZQ10 MEM. 1	ZQ10 MEM. 2	ZQ10 MEM. 3	ZQ10 MEM. 4	ZQ10 MEM. 5	ZQ10 MEM. 6	ZQ10 MEM. 7
GOSS 3	ZQ13 MEM. 0	ZQ13 MEM. 1	ZQ13 MEM. 2	ZQ13 MEM. 3	ZQ13 MEM. 4	ZQ13 MEM. 5	ZQ13 MEM. 6	ZQ13 MEM. 7
GOSS 4	ZQ20 MEM. 0	ZQ20 MEM. 1	ZQ20 MEM. 2	ZQ20 MEM. 3	ZQ20 MEM. 4	ZQ20 MEM. 5	ZQ20 MEM. 6	ZQ20 MEM. 7
GOSS 5	ZQ23 MEM. 0	ZQ23 MEM. 1	ZQ23 MEM. 2	ZQ23 MEM. 3	ZQ23 MEM. 4	ZQ23 MEM. 5	ZQ23 MEM. 6	ZQ23 MEM. 7
GOSS 6	ZQ30 MEM. 0	ZQ30 MEM. 1	ZQ30 MEM. 2	ZQ30 MEM. 3	ZQ30 MEM. 4	ZQ30 MEM. 5	ZQ30 MEM. 6	ZQ30 MEM. 7
GOSS 7	ZQ33 MEM. 0	ZQ33 MEM. 1	ZQ33 MEM. 2	ZQ33 MEM. 3	ZQ33 MEM. 4	ZQ33 MEM. 5	ZQ33 MEM. 6	ZQ33 MEM. 7

BANK BIT (2^2, 2^1, 2^0)

BANK BIT	CPU A	CPU B	CPU C	CPU D	CPU E	CPU F	CPU G	CPU H
2^0	ZW1, ZW11 MEM. 2	ZW1, ZW11 MEM. 3	ZO10 MEM. 2	ZO10 MEM. 3	ZO10 MEM. 4	ZO10 MEM. 5	ZW1, ZW11 MEM. 4	ZW1, ZW11 MEM. 5
2^0	ZW2, ZW12 MEM. 2	ZW2, ZW12 MEM. 3	ZO11 MEM. 2	ZO11 MEM. 3	ZO11 MEM. 4	ZO11 MEM. 5	ZW2, ZW12 MEM. 4	ZW2, ZW12 MEM. 5
2^1	ZW31, ZW21 MEM. 2	ZW31, ZW21 MEM. 3	ZO21 MEM. 2	ZO21 MEM. 3	ZO21 MEM. 4	ZO21 MEM. 5	ZW3, ZW21 MEM. 4	ZW3, ZW21 MEM. 5
2^1	ZW32, ZW22 MEM. 2	ZW32, ZW22 MEM. 3	ZO20 MEM. 2	ZO20 MEM. 3	ZO20 MEM. 4	ZO20 MEM. 5	ZW32, ZW22 MEM. 4	ZW32, ZW22 MEM. 5
2^2	ZQ0, ZQ10 ZQ20, ZQ30 MEM. 0	ZQ0, ZQ10 ZQ20, ZQ30 MEM. 1	ZQ0, ZQ10 ZQ20, ZQ30 MEM. 2	ZQ0, ZQ10 ZQ20, ZQ30 MEM. 3	ZQ0, ZQ10 ZQ20, ZQ30 MEM. 4	ZQ0, ZQ10 ZQ20, ZQ30 MEM. 5	ZQ0, ZQ10 ZQ20, ZQ30 MEM. 6	ZQ0, ZQ10 ZQ20, ZQ30 MEM. 7
2^2	ZQ3, ZQ13 ZQ23, ZQ33 MEM. 0	ZQ3, ZQ13 ZQ23, ZQ33 MEM. 1	ZQ3, ZQ13 ZQ23, ZQ33 MEM. 2	ZQ3, ZQ13 ZQ23, ZQ33 MEM. 3	ZQ3, ZQ13 ZQ23, ZQ33 MEM. 4	ZQ3, ZQ13 ZQ23, ZQ33 MEM. 5	ZQ3, ZQ13 ZQ23, ZQ33 MEM. 6	ZQ3, ZQ13 ZQ23, ZQ33 MEM. 7

SS READ SELECT (2^2, 2^1, 2^0)

SS	CPU A	CPU B	CPU C	CPU D	CPU E	CPU F	CPU G	CPU H
2^0	ZS0 MEM. 0	ZS0 MEM. 1	ZS0 MEM. 2	ZS0 MEM. 3	ZS0 MEM. 4	ZS0 MEM. 5	ZS0 MEM. 6	ZS0 MEM. 7
2^1	ZS1 MEM. 0	ZS1 MEM. 1	ZS1 MEM. 2	ZS1 MEM. 3	ZS1 MEM. 4	ZS1 MEM. 5	ZS1 MEM. 6	ZS1 MEM. 7
2^2	ZS20 MEM. 0	ZS20 MEM. 1	ZS20 MEM. 2	ZS20 MEM. 3	ZS20 MEM. 4	ZS20 MEM. 5	ZS20 MEM. 6	ZS20 MEM. 7

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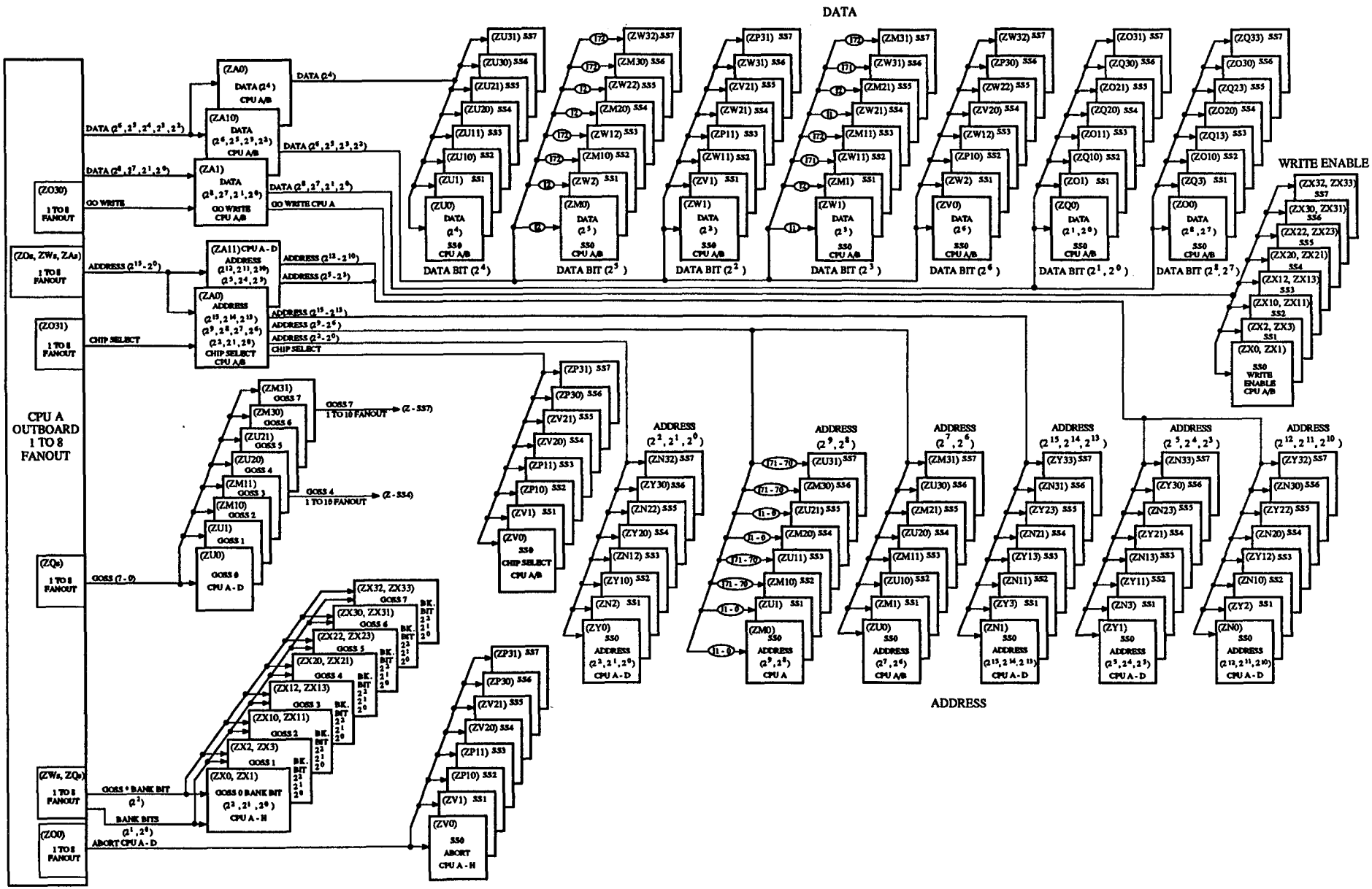
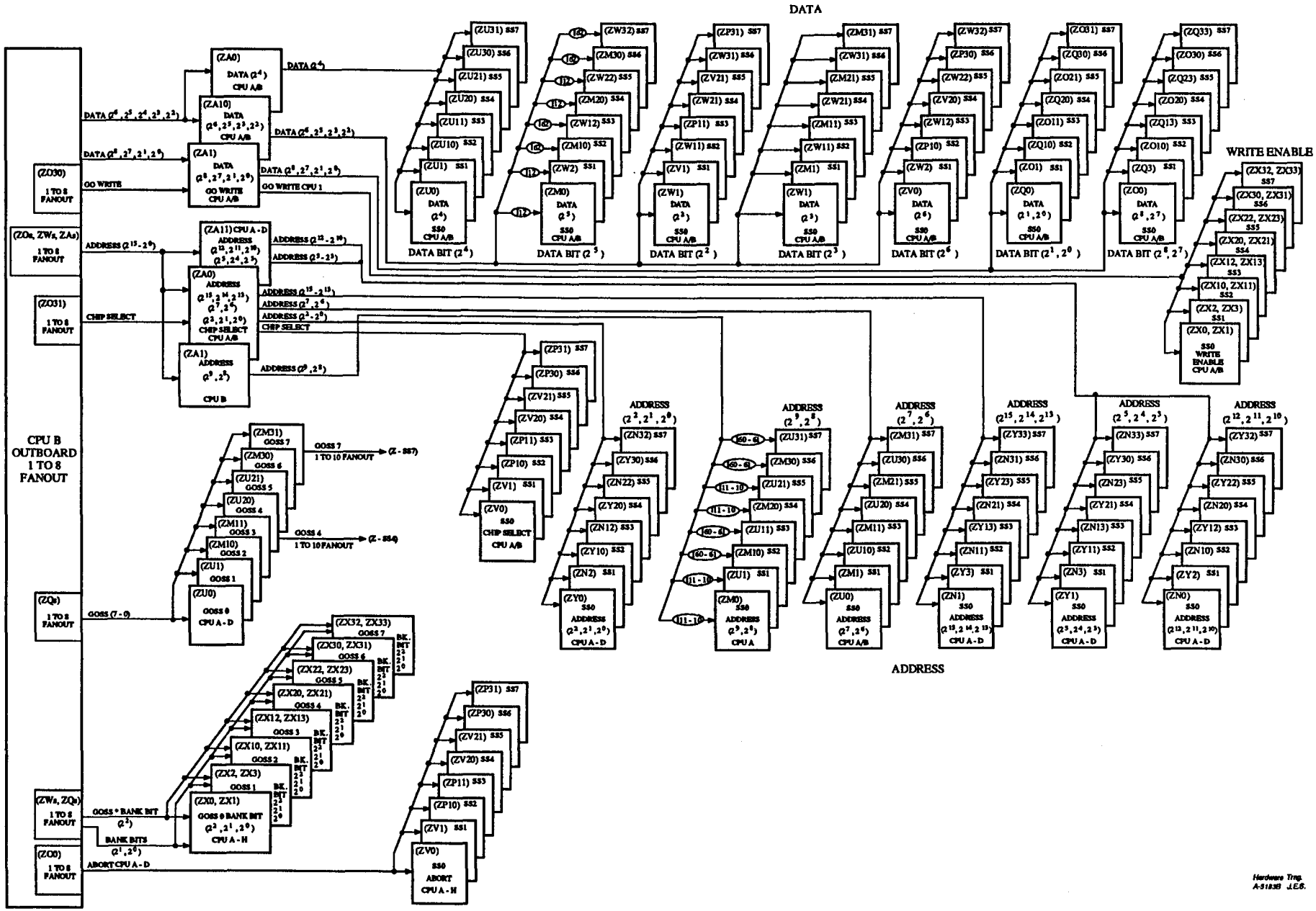
A-4898A J.E.S.

1 TO 8 CONTROL OUTBOARD FANOUT

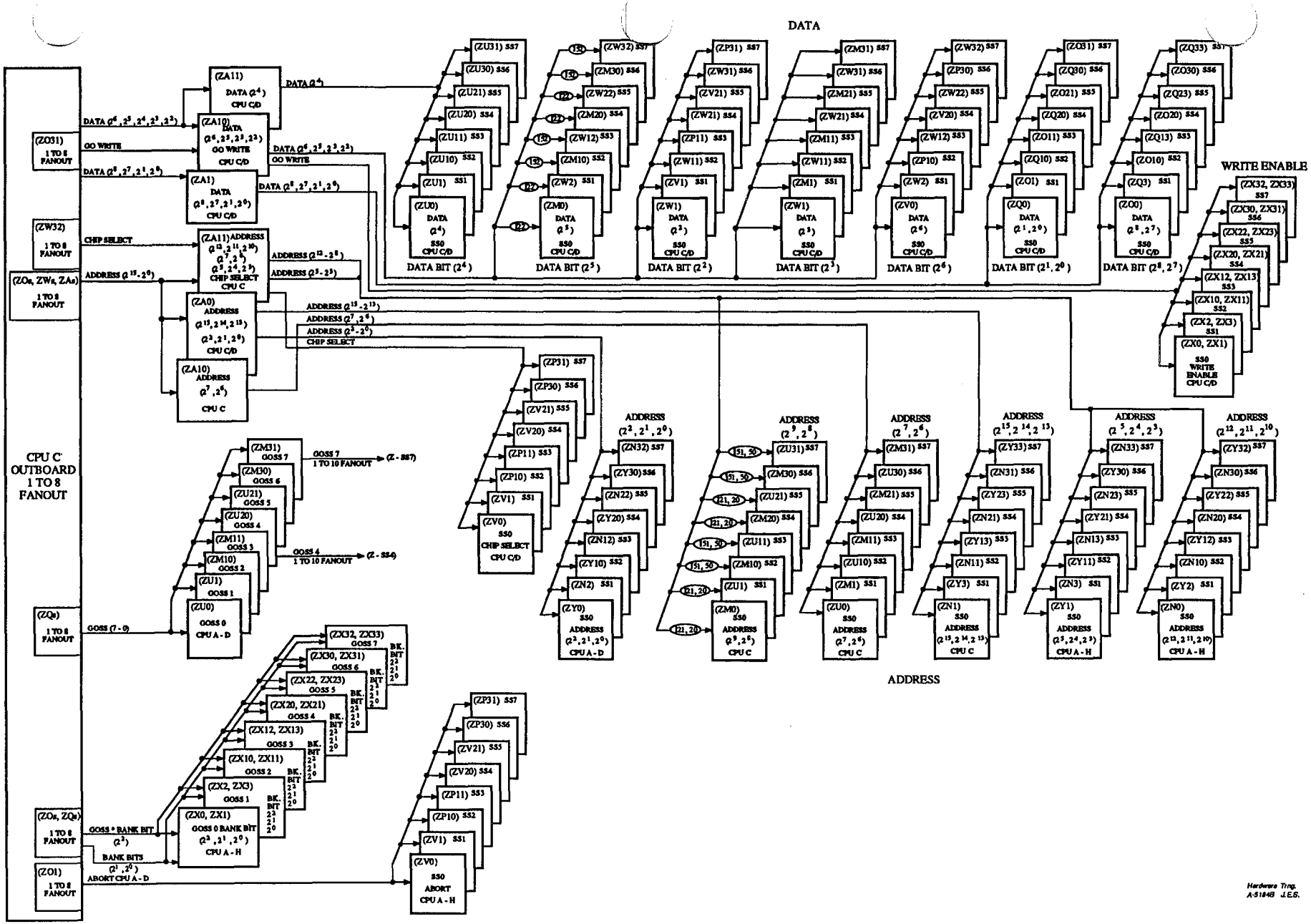


CRAY Y-MP MEMORY (64K x 1)
CPU A 1 TO 8 ONBOARD SUBSECTION FANOUT

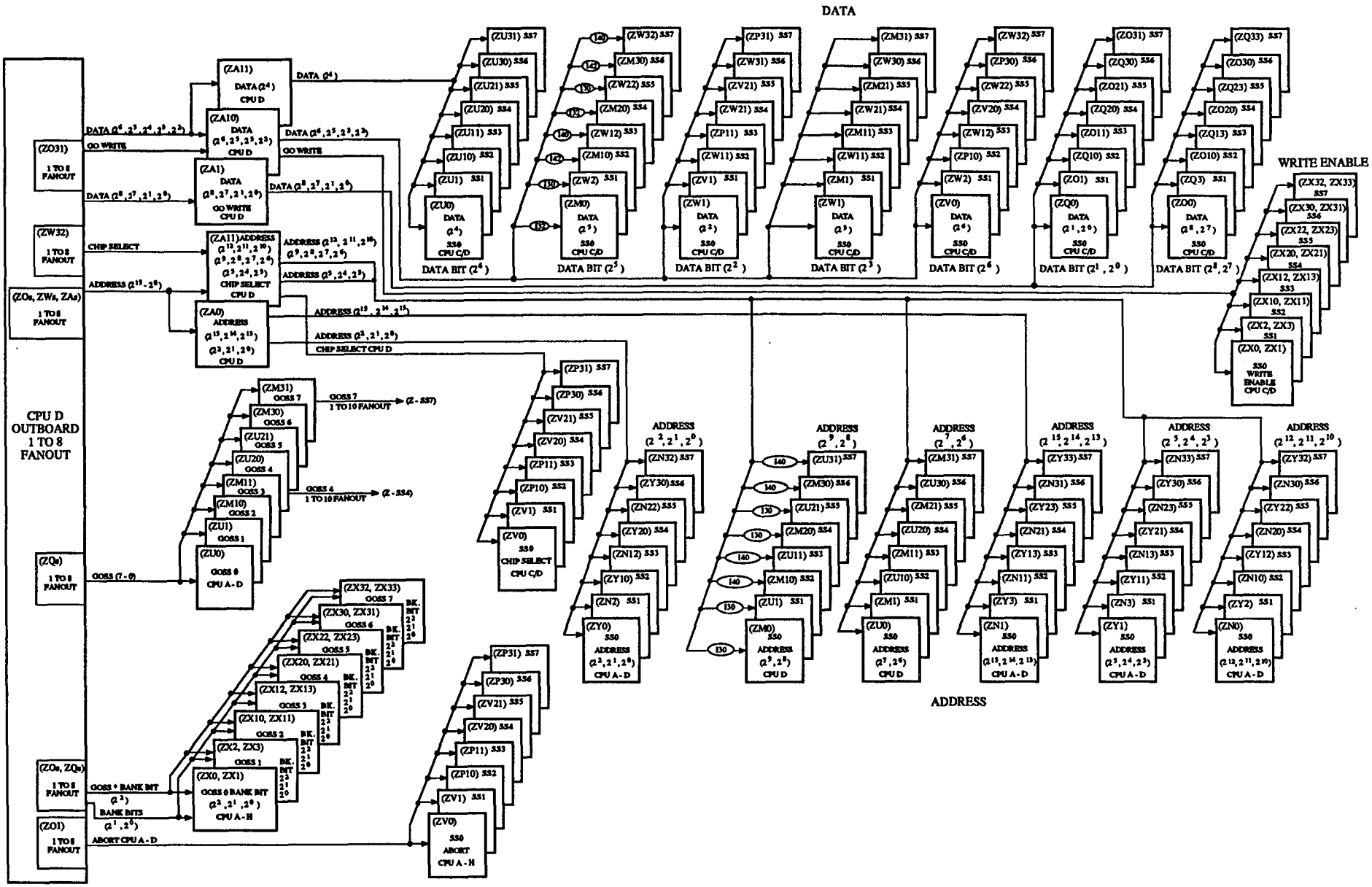
Hardware Trng.
A-51826 J.E.S.



CRAY Y-MP MEMORY (64K x 1)
CPU B 1 TO 8 ONBOARD SUBSECTION FANOUT

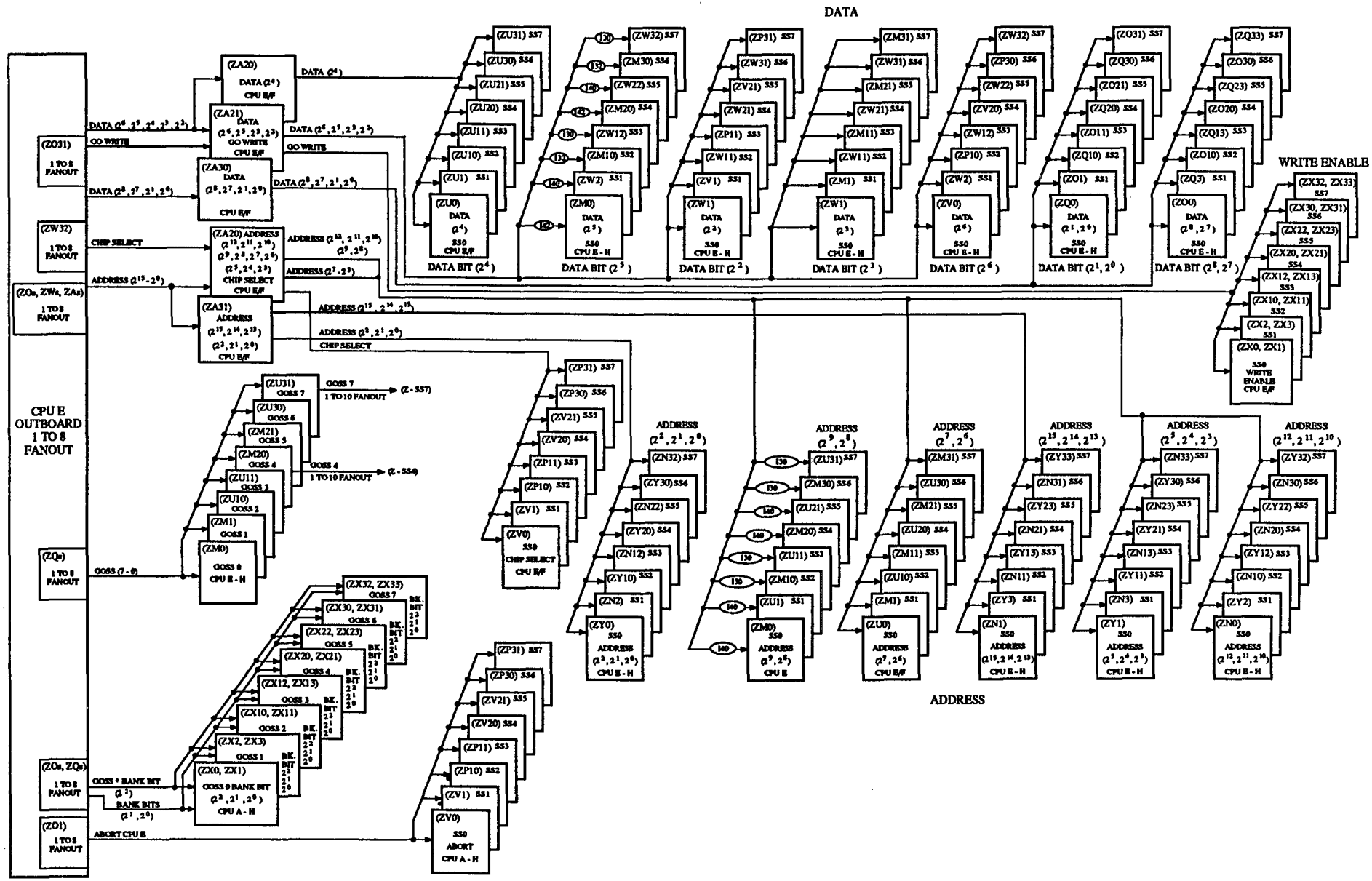


CRAY Y-MP MEMORY (64K x 1)
CPU C 1 TO 8 ONBOARD SUBSECTION FANOUT



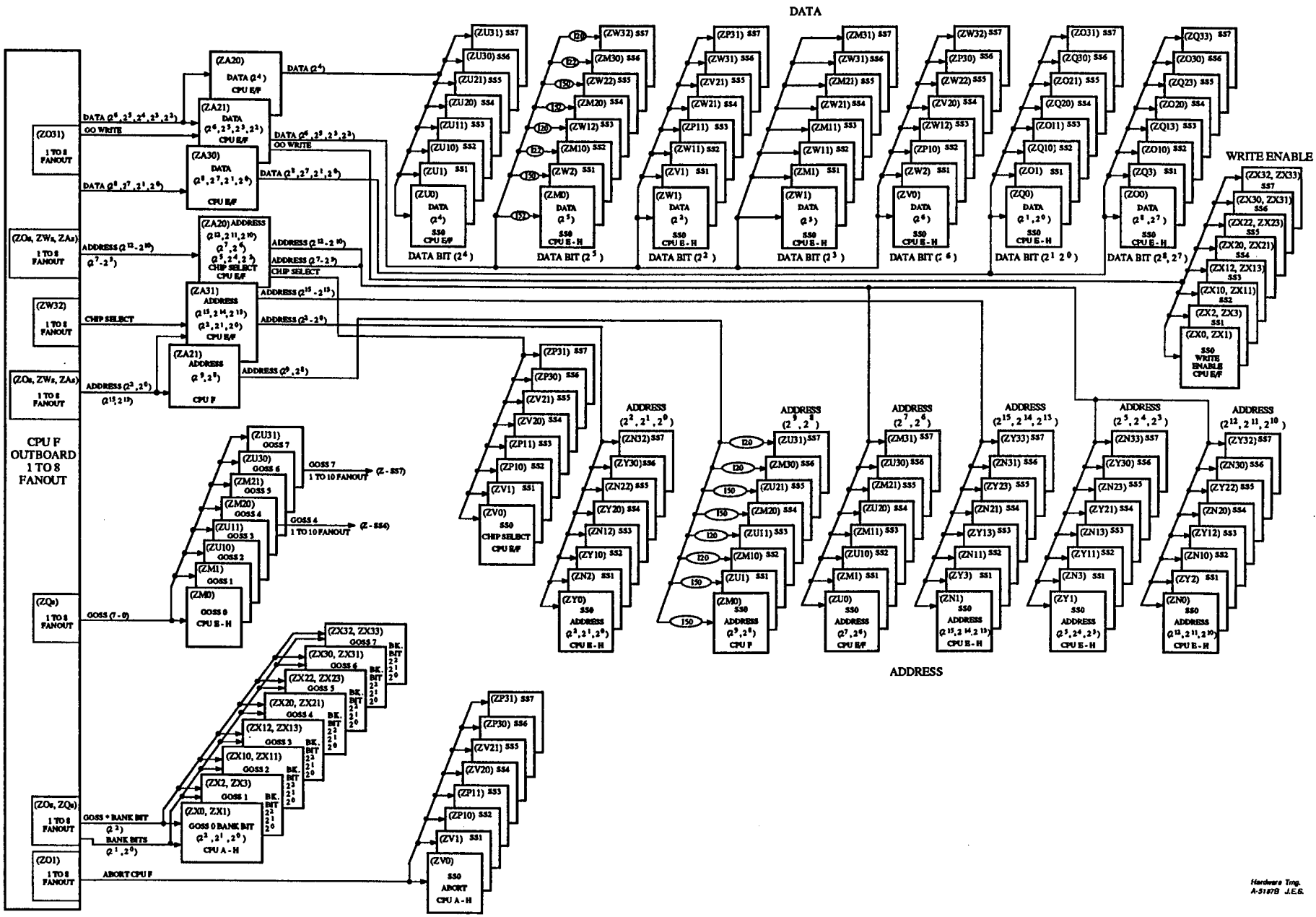
CRAY Y-MP MEMORY (64K x 1)
CPU D 1 TO 8 ONBOARD SUBSECTION FANOUT

Hardware Trng.
A-51858 J.E.S.

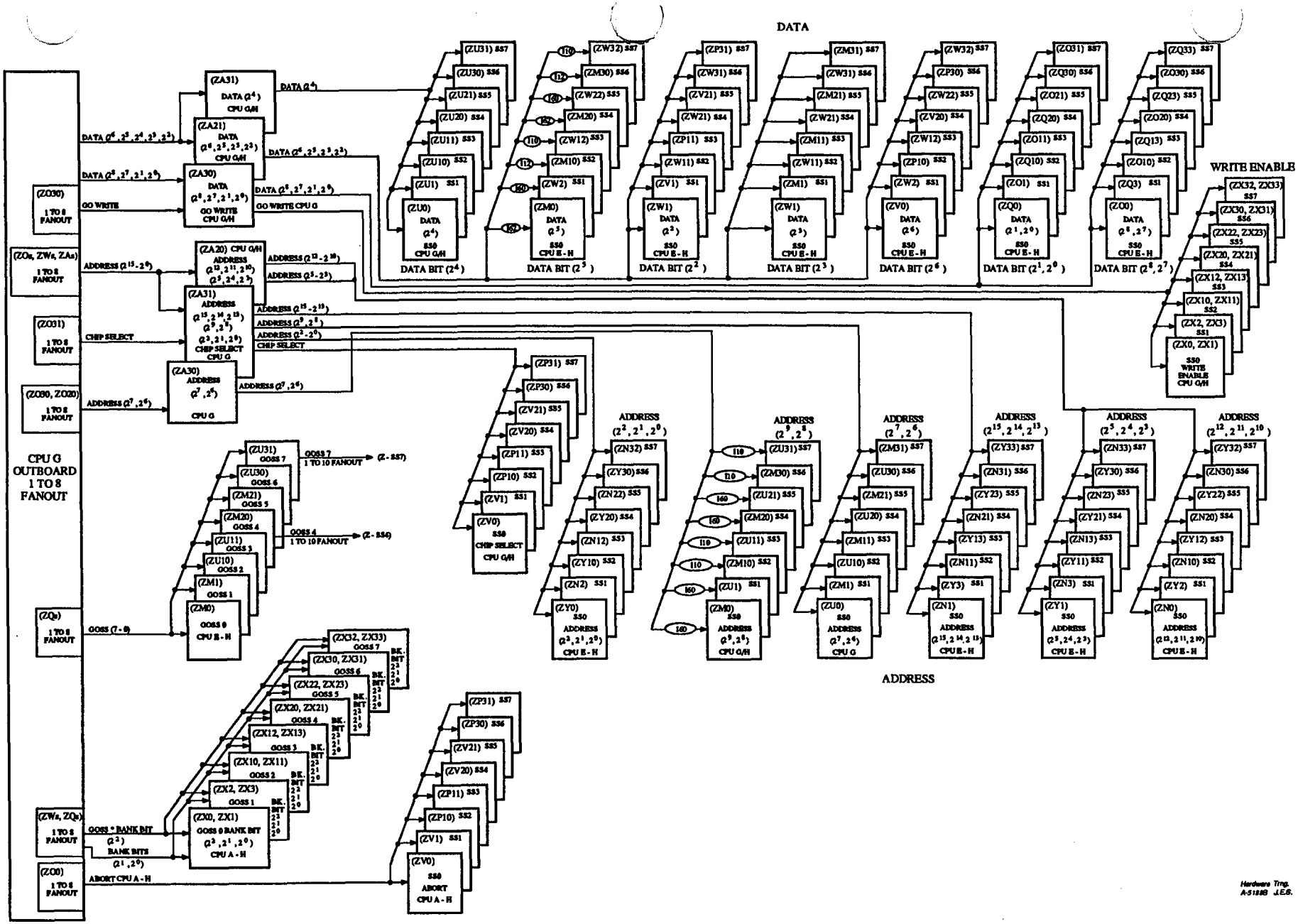


CRAY Y-MP MEMORY (64K x 1)
CPU E 1 TO 8 ONBOARD SUBSECTION FANOUT

Hardware Trng.
A-51988 J.E.S.



CRAY Y-MP MEMORY (64K x 1)
CPU F 1 TO 8 OUTBOARD SUBSECTION FANOUT



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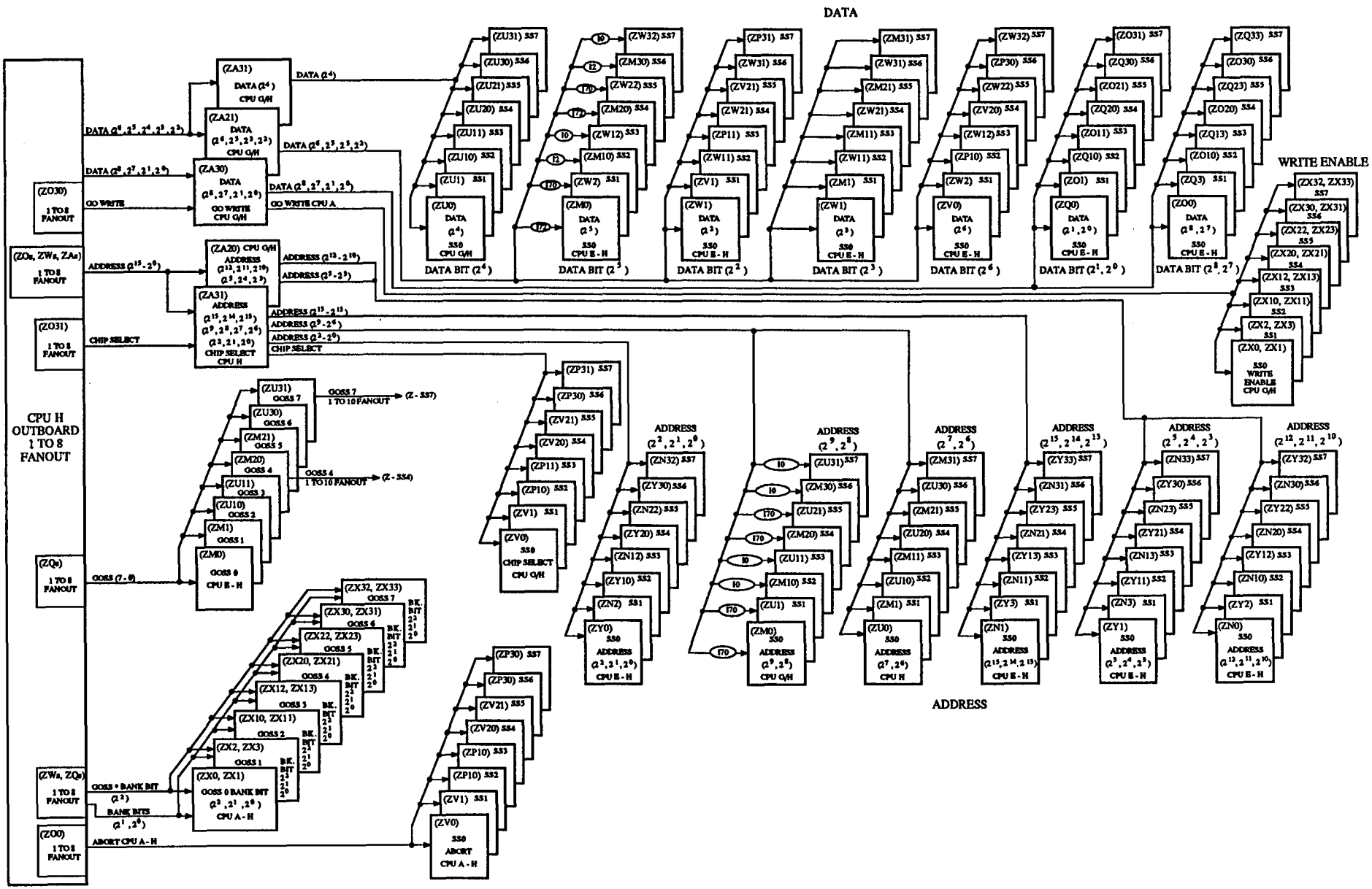
CRAY Y-MP MEMORY (64K x 1)
CPU G 1 TO 8 ONBOARD SUBSECTION FANOUT



CRAY Y-MP MEMORY (64K x 1)
CPU H 1 TO 8 ONBOARD SUBSECTION FANOUT

Hardware Trng.
A-5189A J.E.S.

OBJECTIVES - CRAY Y-MP Memory Hardware

Upon completion of the section, the student will be able to:

- Describe the overall specification of the memory including size, speed, data format, and address format
- Determine the failing memory module, option type, or memory chip given the failing address or data bit
- Interpret Memory Parity Error information
- Define with respect to time and use the Control signals
- Trace the Data, Address, and Control signals

CRAY Y-MP MEMORY (256K x 1) BIMOS

The CRAY Y-MP uses (256K x 1) BIMOS memory chips, which are organized into 256 banks, for a total of 64 million words of storage.

The CRAY Y-MP memory incorporates four sections, with each section containing eight subsections. Each subsection then contains 8 banks for a subsection total of 64 banks and a memory total of 256 banks.

Physically, there are eight modules per section, each module containing a 9-bit slice of the 72-bit word. Each module is also organized into eight subsections. Subsections 0 and 1 are located on the A Board of the module, Subsections 2 and 3 are on the B board, Subsections 4 and 5 are on the C board and Subsections 6 and 7 are located on the D board.

There are four ports per CPU, and all four ports can be accessing four different sections within the same clock period. All eight CPUs can go to the same subsection, as long as they are going to different banks within the subsection. Once a CPU has accessed a bank, that bank is held busy for 5 clock periods (CPs).

A 72-bit word is sent from the CPU module to the eight memory modules which make up a section. Data bits are divided into 9 bits per module. Memory module 0 or Memory 0 contains data bits (2^8 - 2^0). Memory 1 contains bits (2^{17} - 2^9), and so on. Controls and address which are sent from the CPUs must also be fanned out to the eight memory modules. This is called an Outboard fanout because they are done outside of the normal module's function. These Outboard fanouts are carried out by the (WW, WO, WB, WP, ZA, ZS) options. All memory modules assist in performing the 1 to 8 Outboard fanouts, some of the modules performing more fanouts than other memory modules. Once on the module, another fanout to the eight subsections takes place. This happens for the address, control and data and is referred to as an Onboard fanout, because this fanout happens only on a memory module.

Once a particular CPU has accessed a subsection, the controls Go Subsection (GOSS) and GOSS bank bits are routed to the (WT) option that controls the subsection. The (WT) option performs a subsection conflict check on the eight banks within the subsection among all CPUs. Only one CPU can access a bank at a time. Once the CPU has accessed a bank, that bank is held busy for 5 CPs. When a conflict occurs such that two or more CPUs want the same bank, called a Simultaneous Bank conflict, the CPU with the lowest number "i" term would have the highest priority to use the bank.

Read Operation To Subsection 0

During the Read operation, only the address and control are sent from the CPU module. The address is latched and held in the (WY0, WY1, WM0, WM1, WM2, WN0, WN1) options by the GOSS CPU (A - H). The (WT0) option for Subsection 0 will resolve any CPU conflict involving the particular bank. When the conflict is resolved, the (WT0) will supply the latched address on the (W-) option with a Bank (0 - 7) Select Code. The Select Code will assign a particular CPU to a bank. The address is presented to the Memory bank for 5 CPs.

To set up the appropriate Read paths back to a particular CPU, two things must be done: first, 1 of 8 banks needs to be selected from within Subsection 0, and secondly, 1 of 8 subsections needs to be selected for a particular CPU. Before the Read data will enter the (WR) option from the bank that was being addressed, the (WR0, WR1, WR2) options are sent a CPU (A - H) Read Bank Select Code, which assigns a Bank (0 - 7) to a particular CPU (A - H). The Read Select Code is generated by the (WL0) option for all CPUs. Read Bank Select Code is (000) for Bank 0 or (111) for Bank (N + 7).

Once the Read Bank Select Code is set up on the (WR) options, it is delayed while the address is being presented to the (256K x 1) chip. The words sent from Subsection 0's banks are routed to the (WR) options. The (WR) options will steer the data from Banks (0 - 7) to the appropriate CPU (A - H), performing a 1 of 8 Bank Select. CPU (A - H) data bits are then sent to the (ZS) options. The (ZS) options have been set up such that all Subsections (0 - 7) send their data to (ZS0) for CPU (A), (ZS1) for CPU (B), etc. The (ZS0) for CPU (A) would then have to select the 9 bits of data from 1 of 8 subsections. To do this the (ZS) options are supplied with a 3-bit SS Select code. The SS Select Code comes from the CPU modules through a 1-to-8 Outboard fanout on the (ZS0, ZS1, ZS20) options. The (ZS0) for CPU (A), or CPU 0, will then output the data to the CPU 0 module.

Write Operation To Subsection 0

On a Write operation to memory, the address, control, and data are sent from the CPU module to a particular section. The CPU module determines the section to which these signals are sent. Once sent to the section, the Control and Address signals undergo a 1 to 8 Outboard fanout to each module within the section. Data is not fanned out, but is split up into 9 bits per module. Memory module 0, or Memory 0, receives data bit (2^8 - 2^0) and so on. The 9 bits of data enter the (WB0, WW0, WM1, WV0, WO0) options for Subsection 0, along with GOSS 0 CPU (A - H). The GOSS 0 CPU (A - H) signals will latch and hold the data for the correct CPU. The same thing happens for the address, but this is performed on the (WY0, WY1, WM0, WM1, WN0, WN1, WM2) options for Subsection 0. Once the (WT0) option has resolved any conflicts among the CPUs, the (WT) will generate a Bank (0 - 7) Select Code, which is then sent to the latched data and address on the (W-) options. The Bank (0 - 7) Select Code will assign a particular CPU (A - H) to a specific Bank (0 - 7). The Select Code sent from the (WT) option is (000) for CPU 0, (001) for CPU 1, etc; however, on the address and data (W-) options, not all the options receive the true state of the Select Code. The (WM0, WM1, WV0, WO0) options for data and the (WM0, WM1, WM2, WN0, WN1) options for address receive the inverted state of the Select Code, while the (WB0, WW0) options for data and the (WY0, WY1) options for address receive the true Select Code.

The data is then steered to the correct bank within Subsection 0 for the CPU (A - H) that was requesting a Write reference. The Write Enable is supplied by the (WL0, WR0, WR1, WR2) options which are assigned to that bank. Banks (0 - 1) are controlled by (WL0) option, Banks (2 - 3) by the (WR0) option, Banks (4 - 5) by the (WR1) option, and Banks (6 - 7) by the (WR2) option. The address and data are held on the memory chip for 5 CPs by the (W-) options. The chip select is supplied by the (WV0) option, which is always enabled during a reference (selecting the nine memory chips in the bank) unless an abort occurs. The abort signal will disable the chip select which is sent to the memory chips. When an Abort occurs on a Write operation to memory, nothing is written; on a Read operation zeroes are read from memory.

CPU A - H Designators

On the memory module, the CPU is given a letter designator by the Subsection the CPU is trying to access to keep the interconnects between the boards as short as possible.

Section 0 CPU 0 is called CPU (A) in Subsection 0, 1, 4, and 5 and CPU (H) in Subsection 2, 3, 6, and 7. The table below shows the other combinations.

SECTION 0

Priorities	A	B	C	D	E	F	G	H	(A - highest, H - lowest)
SS0	CPU 0	CPU 1	CPU 2	CPU 3	CPU 7	CPU 6	CPU 5	CPU 4	* - wire name
SS1	CPU 0	CPU 1	CPU 2	CPU 3	CPU 7	CPU 6	CPU 5	CPU 4	*
SS2	CPU 4	CPU 5	CPU 6	CPU 7	CPU 3	CPU 2	CPU 1	CPU 0	
SS3	CPU 4	CPU 5	CPU 6	CPU 7	CPU 3	CPU 2	CPU 1	CPU 0	
SS4	CPU 0	CPU 1	CPU 2	CPU 3	CPU 7	CPU 6	CPU 5	CPU 4	*
SS5	CPU 0	CPU 1	CPU 2	CPU 3	CPU 7	CPU 6	CPU 5	CPU 4	*
SS6	CPU 4	CPU 5	CPU 6	CPU 7	CPU 3	CPU 2	CPU 1	CPU 0	
SS7	CPU 4	CPU 5	CPU 6	CPU 7	CPU 3	CPU 2	CPU 1	CPU 0	

SECTION 1

Priorities	A	B	C	D	E	F	G	H	(A - highest, H - lowest)
SS0	CPU 1	CPU 2	CPU 3	CPU 0	CPU 4	CPU 7	CPU 6	CPU 5	* - wire name
SS1	CPU 1	CPU 2	CPU 3	CPU 0	CPU 4	CPU 7	CPU 6	CPU 5	*
SS2	CPU 5	CPU 6	CPU 7	CPU 4	CPU 0	CPU 3	CPU 2	CPU 1	
SS3	CPU 5	CPU 6	CPU 7	CPU 4	CPU 0	CPU 3	CPU 2	CPU 1	
SS4	CPU 1	CPU 2	CPU 3	CPU 0	CPU 4	CPU 7	CPU 6	CPU 5	*
SS5	CPU 1	CPU 2	CPU 3	CPU 0	CPU 4	CPU 7	CPU 6	CPU 5	*
SS6	CPU 5	CPU 6	CPU 7	CPU 4	CPU 0	CPU 3	CPU 2	CPU 1	
SS7	CPU 5	CPU 6	CPU 7	CPU 4	CPU 0	CPU 3	CPU 2	CPU 1	

SECTION 2

Priorities	A	B	C	D	E	F	G	H	(A - highest, H - lowest)
SS0	CPU 2	CPU 3	CPU 0	CPU 1	CPU 5	CPU 4	CPU 7	CPU 6	* - wire name
SS1	CPU 2	CPU 3	CPU 0	CPU 1	CPU 5	CPU 4	CPU 7	CPU 6	*
SS2	CPU 6	CPU 7	CPU 4	CPU 5	CPU 1	CPU 0	CPU 3	CPU 2	
SS3	CPU 6	CPU 7	CPU 4	CPU 5	CPU 1	CPU 0	CPU 3	CPU 2	
SS4	CPU 2	CPU 3	CPU 0	CPU 1	CPU 5	CPU 4	CPU 7	CPU 6	*
SS5	CPU 2	CPU 3	CPU 0	CPU 1	CPU 5	CPU 4	CPU 7	CPU 6	*
SS6	CPU 6	CPU 7	CPU 4	CPU 5	CPU 1	CPU 0	CPU 3	CPU 2	
SS7	CPU 6	CPU 7	CPU 4	CPU 5	CPU 1	CPU 0	CPU 3	CPU 2	

SECTION 3

Priorities	A	B	C	D	E	F	G	H	(A - highest, H - lowest)
SS0	CPU 3	CPU 0	CPU 1	CPU 2	CPU 6	CPU 5	CPU 4	CPU 7	* - wire name
SS1	CPU 3	CPU 0	CPU 1	CPU 2	CPU 6	CPU 5	CPU 4	CPU 7	*
SS2	CPU 7	CPU 4	CPU 5	CPU 6	CPU 2	CPU 1	CPU 0	CPU 3	
SS3	CPU 7	CPU 4	CPU 5	CPU 6	CPU 2	CPU 1	CPU 0	CPU 3	
SS4	CPU 3	CPU 0	CPU 1	CPU 2	CPU 6	CPU 5	CPU 4	CPU 7	*
SS5	CPU 3	CPU 0	CPU 1	CPU 2	CPU 6	CPU 5	CPU 4	CPU 7	*
SS6	CPU 7	CPU 4	CPU 5	CPU 6	CPU 2	CPU 1	CPU 0	CPU 3	
SS7	CPU 7	CPU 4	CPU 5	CPU 6	CPU 2	CPU 1	CPU 0	CPU 3	

One of the advantages of lettering the CPUs is that when the (WT) option checks for Subsection conflicts and a decision needs to be made as to which CPU will get a particular bank, the lowest lettered CPU would have the highest priority. Because of the way the CPU letters are distributed among the Subsections, all CPUs are treated the same when using the law of averages.

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A-7824 J.E.S.

CRAY Y-MP MEMORY OPTIONS PER MODULE

OPTION TYPE	NUMBER USED	DESCRIPTION
WB	8	2 Data bits / two 1 - 8 F.O.
WL	8	Read bank selects / Bank n, n + 1 Write Enable
WM	24	3 Address bits / five 1 - 1 GOSS F.O.
WN	16	3 Address bits / 2 banks CPU Select F.O.
WO	8	2 Data bits / two 1 - 8 F.O.
WP	4	Chip Select / 1 Data bit
WR	24	Subsection Bank Data Select
WT	8	Subsection Conflict Check
WV	4	Chip Select / 1 Data bit
WW	8	2 Data bits / two 1 - 8 F.O.
WY	16	3 Address bits / 2 banks CPU Select F.O.
ZA	8	Fanout
ZS	8	CPU Read Data / one 1 - 8 F.O.
TO	4	Clock Distribution
	148 total options	

YM26/05

CRAY Y-MP MEMORY (OPTIONS INVOLVED) (256K x 1 BIMOS)

(WB) Option

There is one (WB) option in each subsection which is capable of handling 2 write data bits. The (WB) option receives a control signal called CPU A - H GOSS which allows the (WB) options to latch and hold the data bits until it is time to write the data to memory. When it is time to write to memory the (WB) option will decode the Bank 0 - 7 CPU Select Code, which will enable the (WB) option to steer the data to the appropriate bank. The (WB) options also perform a 1 to 8 outboard fanout on the address and control signals to the eight modules within a section for all CPUs.

(WL) Option

There is one (WL) option in each subsection which is used during both the read and write operations. During the write operation the (WL) options receive a control signal called Go Write n, n + 1. This signal produces the Write Enable which is sent to specific banks in memory for 3 CP. The timing of this signal is controlled by the Go Bank n, n + 1 and the 3 CP Write Enable Select signal. (WL0), (WL10), (WL20), and (WL30) generate the Write Enable for Banks 0 and 1 for their respective subsections. (WL1), (WL11), (WL21), and (WL31) generate the Write Enable for Banks 6 and 7.

During the read operation the (WL) options produce two control signals which are sent to the (WR) options, CPU A - H Read Bank Selects and Go Read CPU A - H. These signals are generated when there is no write reference. The CPU A - H Read Bank Select bits tell the (WR) options which bank in the subsection will be read from. The Go Read CPU A - H tells the (WR) option which CPU is requesting the read.

(WM) Option

The (WM) options are capable of handling 2 address bits and 1 data bit. There are three (WM) options in each subsection. The (WM) options receive a signal called CPU A - H GOSS, which is used to latch and hold the address and data bits. When the time is right for a particular CPU to reference a bank within a subsection the (WM) options will decode a Bank 0 - 7 CPU Select Code, which will allow the (WM) options to steer the address and data bits to the appropriate bank. The (WM) options also have a fanout which is used to assist in the GOSS.

(WN) Option

The (WN) options are capable of handling 3 address bits. There are two (WN) options in each subsection, each handling different address bits. The (WN) options receive a signal called CPU A - H GOSS. This signal latches and holds the address bits. When a CPU is allowed to reference a bank the (WN) options will decode a Bank 0 - 7 CPU Select Code, which will allow the (WN) options to steer the address to the appropriate bank. The (WN) options also have a fanout which is used to assist in the Bank 0 - 7 CPU Select Fanout. In Subsection 0, (WN0) fans out Bank 4 - 5 CPU select and (WN1) fans out bank 6 - 7 CPU select.

(WO) Option

There is one (WO) option in each subsection which is capable of handling two write data bits. The (WO) options receive the same control signals as the (WB) options for latching and steering the data bits, except these signals are inverted. The (WO) options also assist in the 1 to 8 Outboard fanout of address and controls from the various CPUs to the eight modules within a section.

(WP) Option

The (WP) options are capable of handling 1 data bit, chip select, and the Abort signal.There is one (WP) option in Subsections 2, 3, 6, and 7. The (WP) options receive the same control signals as the (WO) options to latch and steer the data bit to a bank in memory.

For the 64 million word machine the input to the (WP) options for the chip select is forced to a zero condition. This forced zero condition, along with a 64 million word select will enable both signals for chip select, (C.S. 0 and C.S. 0/1). Having both of these signals will enable the nine memory chips within the bank each time the bank is referenced.

When the Abort signal is sent to the (WP) options, the two signals for the chip select (C.S. 0 and C.S. 0/1) are both forced to zeroes, preventing a write operation from completing, or during a read causing zeroes to be read from memory.

(WR) Option

There are three (WR) options in each subsection which are used during both the read and write operations. During the write operation, the (WR) options receive a control signal called Go Write Bank n, n + 1. This signal produces the Write Enable which is sent to specific banks in memory for 3 CPs. The timing of this signal is controlled by the Go Bank n, n + 1 and the 3 CP Write Enable Select signal. (WR0), (WR4), (WR10), (WR14), (WR20), (WR24), (WR30), and (WR34) generate the Write Enable for Banks 2 and 3 for their respective subsections. (WR1), (WR5), (WR11), (WR15), (WR21), (WR25), (WR31), and (WR35) generate the Write Enable for Banks 4 and 5. (WR2), (WR12), (WR22), and (WR32) generate the Write Enable for Banks 6 and 7. (WR3), (WR13), (WR23), and (WR33) generate the Write Enable for Banks 0 and 1.

During the read operation each (WR) option will receive 3 data bits from each bank within the subsection. The control signals Go Read CPU A - H and CPU A - H Bank Bits select the proper data and will steer the data to the appropriate (ZS) option.

(WT) Option

There is one (WT) option in each subsection which will check for conflicts among all the banks within a subsection. The signals CPU A - H Bank Bits 0 and 1 along with GOSS anded with Bank Bit 2 or 2' tell the (WT) option there is a request of a bank by a particular CPU. When a request has been made the (WT) option will check to see if there is a conflict with the request. There are two conditions which can cause a conflict ; the bank is already busy or another CPU made a request for the same bank at the same time. If the first condition exists, the request will not be allowed until the bank busy is dropped. If the second condition exists, the (WT) has to decide which CPU has priority. The CPU with the lowest I term value has priority and will be allowed the request. Once the (WT) grants a request of a CPU, the bank is held busy for 5 CPs. The (WT) option then generates a Bank 0 - 7 Select Code which assigns a particular CPU to a specific bank and signal called Go Bank 0 - 7.

(WW) Option

There is one (WW) option in each subsection which is capable of handling 2 write data bits. The (WW) option receives a control signal called CPU A - H GOSS which allows the (WW) options to latch and hold the data bits until it is time to write the data to memory. When it is time to write to memory the (WW) option will decode the Bank 0 - 7 CPU Select Code, which will enable the (WW) option to steer the data to the appropriate bank. The (WW) options also perform a 1 to 8 Outboard fanout on the address and control signals to the eight modules within a section for all CPUs.

(WY) Option

The (WY) options are capable of handling 3 address bits. There are two (WY) options in each subsection, each handling different address bits. The (WY) options receive a signal called CPU A - H GOSS. This signal latches and holds the address bits. When a CPU is allowed to reference a bank the (WY) options will decode a Bank 0 - 7 CPU Select Code, which will allow the (WY) options to steer the address to the appropriate bank. The (WY) options also have a fanout which is used to assist in the Bank 0 - 7 CPU Select Fanout. In Subsection 0, (WY0) fans out Bank 4 - 5 CPU select and (WY1) fans out bank 6 - 7 CPU select.

(WV) Option

The (WV) options are capable of handling 1 data bit, chip select, and the Abort signal. There is one (WV) option in Subsections 0, 1, 4, and 5. The (WV) options receive the same control signals as the (WO) options to latch and steer the data bit to a bank in memory.

For the 64 million word machine the input to the (WV) options for the chip select is forced to a zero condition. This forced zero condition, along with a 64 million word select will enable both signals for chip select (C.S. 0, C.S. 0/1). Having both of these signals will enable the nine memory chips within the bank each time the bank is referenced.

When the Abort signal is sent to the (WV) options the two signals for chip select (C.S. 0, C.S. 0/1) are both forced to zeroes, preventing a write operation from completing, or during a read causing zeroes to be read from memory.

(ZA) Option

The (ZA) options are used to fanout memory information from the various CPUs. Since this fanout is done on the memory modules themselves, it is referred to as an Onboard fanout. In general, the (ZAs) fanout the Address, Chip Select, Data, and the Go Write to Subsections (0 - 7). The various (ZA) options can be differentiated by what data or address bits are being fanned out for the particular CPU. The (ZA) options also perform a 1 to 8 fanout to the eight memory modules within a section. (ZA1, ZA11) fanout address bits (2^{11}, 2^{10}, 2^{9}, 2^{8}) on memory modules (0 - 7) for all eight CPUs; this is called an Outboard fanout.

(ZS) Option

The (ZS) options are called the CPU Subsection Selects. There is one (ZS) per CPU per module. (ZS0) receives an SS Select Code from CPU 0 and selects 9 bits of data from 1 of 8 subsections. (ZS1) does the same for CPU 1, etc. The (ZSs) then send the 9 bits of read data to their particular CPU. The (ZSs) also perform a 1 to 8 Outboard fanout on subsection Read Select bits (2^{2}, 2^{1}, 2^{0}) for all CPUs.

CRAY Y-MP MEMORY
(256K x 1) BIMOS

GENERAL

SIZE:	64 million words
BANKS:	256 Banks
SECTIONS:	4 Sections
SUBSECTIONS:	8 per Section
BANK PER SECTION:	64 Banks
BANK PER SUBSECTION:	8 Banks
MEMORY CHIP:	256K x 1 BIMOS 15 nsec access, 100K compatible
CPU ACCESS:	4 ports per CPU These share one physical path into memory
MODULE PER SECTION:	8 modules per section each has a 9-bit slice, each has 8 CPU paths into memory
SECTION ACCESS:	The same CPU can go back to the same Subsection every 5 CPs or more. All 8 CPUs can go to the same Subsection as long as they are going to different Banks.

Hardware Trng.
YM26/09 J.E.S.

CRAY Y-MP MEMORY DOCUMENTATION

PCTAB Memory

PCTAB Memory documents option to option, option to edge connector, and option to memory chip connections on the memory module. The options and memory chips are listed in alphabetical and numerical order. The connectors are documented following the option/memory chip listing.

PCTAB Memory lists the source of the I terms and the destination of the R terms for each option, memory chip, and edge connector.

Memory Jumper Manual

The Memory Jumper manual documents the physical location of each jumper pin used on the memory module. It also documents the type of jumper pin used at each location.

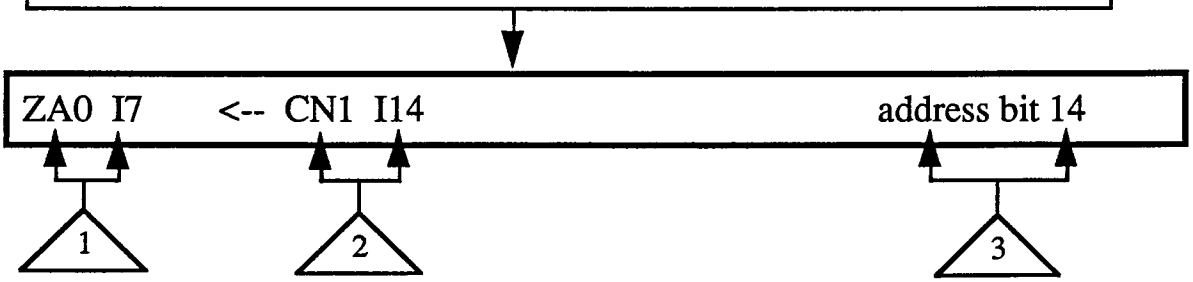
Wire Tabs

Wire tabs document the connections between modules in the mainframe. The modules are listed in numerical order dictated by their physical location in the mainframe. It also lists the source of the I terms and destination of the R terms for each connector used on a module.

PCTAB Memory

CHIP COPY: ZA0 LOCATION: AGE OPTION TYPE: ZA PCTAB P/N 31142015 09/06/88

ZA0 I0	<-- CN3 I15	address bit 15
ZA0 I1	<-- CN3 I14	address bit 14
ZA0 I2	<-- CN3 I13	address bit 13
ZA0 I3	<-- CN2 I15	address bit 15
ZA0 I4	<-- CN2 I14	address bit 14
ZA0 I5	<-- CN2 I13	address bit 13
ZA0 I6	<-- CN1 I15	address bit 15
ZA0 I7	<-- CN1 I14	address bit 14



1 OPTION INPUT - Address bit 2^{14} is sent to the option (ZA0). The signal arrives on the option as term I7.

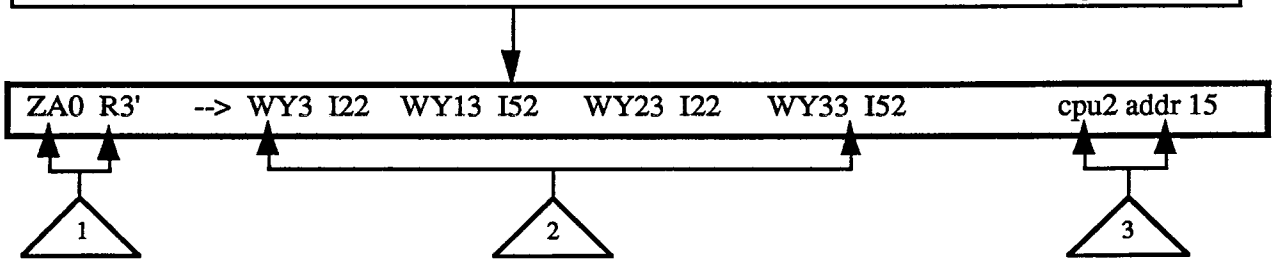
2 SOURCE OF THE SIGNAL - The signal comes from a connector called CN1. The signal leaves the connector as term I14.

3 DESCRIPTION OF THE SIGNAL

YM29/04

PCTAB Memory (continued)

ZA0	R0	--> WN1 I32	WN11 I42	WN21 I32	WN31 I42	cpu3 addr 15
ZA0	R0'	--> WY3 I32	WY13 I42	WY23 I32	WY33 I42	cpu3 addr 15
ZA0	R1	--> WN1 I31	WN11 I41	WN21 I31	WN31 I41	cpu3 addr14
ZA0	R1'	--> WY3 I31	WY13 I41	WY23 I31	WY33 I41	cpu3 addr14
ZA0	R2	--> WN1 I30	WN11 I40	WN21 I30	WN31 I40	cpu3 addr 13
ZA0	R2'	--> WY3 I30	WY13 I40	WY23 I30	WY33 I40	cpu3 addr 13
ZA0	R3	--> WN1 I22	WN11 I52	WN21 I22	WN31 I52	cpu2 addr 15
ZA0	R3'	--> WY3 I22	WY13 I52	WY23 I22	WY33 I52	cpu2 addr 15



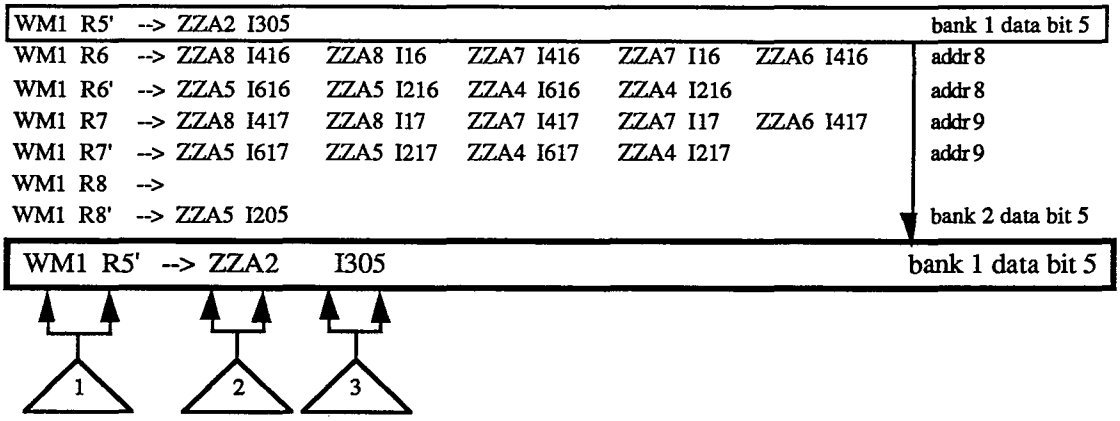
1 SOURCE OF THE SIGNAL - CPU 2 address bit 2^{15} leaves the option (ZA0) as term R3.

2 DESTINATION OF THE SIGNAL - This signal is sent to four different options: (WY3), (WY13), (WY23), and (WY33). This signal enters (WY3), and (WY23) as term I22 and on (WY13) and (WY33) it enters the option as term I52.

3 DESCRIPTION OF THE SIGNAL

YM29/05

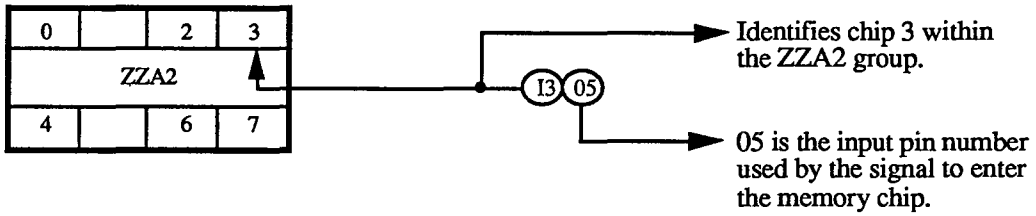
PCTAB Memory (continued)

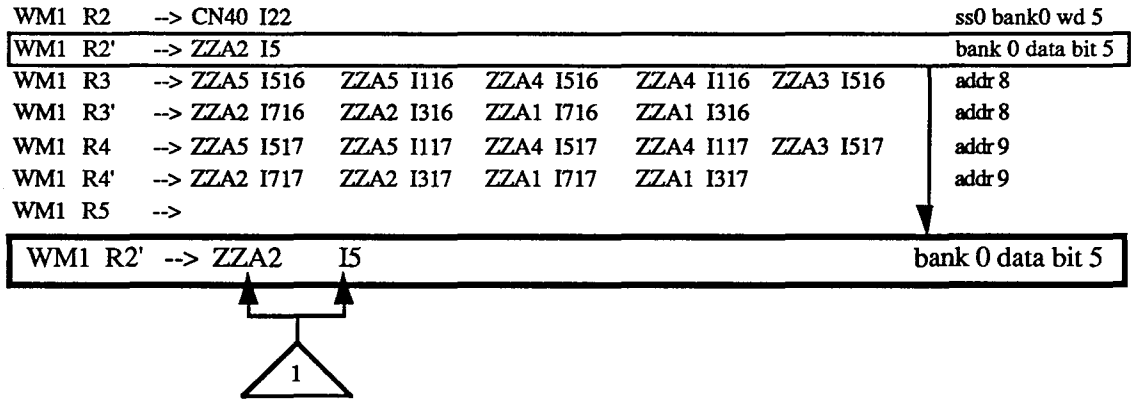


1 SOURCE OF THE SIGNAL - Bank 1 data bit 5 leaves option (WM1) as term R5'.

2 GROUP NAME - Bank 1 data bit 5 is sent to a group of memory chips called ZZA2. The ZZA2 group contains six memory chips.

3 CHIP AND INPUT DESIGNATOR - I305 can be broken into two parts:





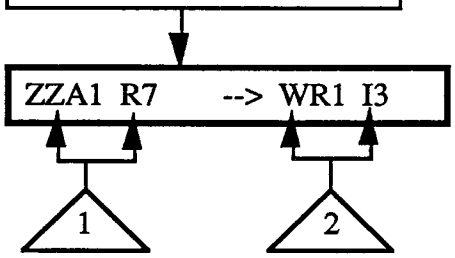
1 The memory chip is documented as ZZA2 I5. For this example, there are two leading zeroes missing. It should read ZZA2 I005, designating chip 0 of group ZZA2. The pin being used is pin 05.

YM29/06A

PCTAB Memory (continued)

CHIP COPY: ZZA1 LOCATION: AAC OPTION TYPE: ZZ PCTAB P/N 31209000 09/28/88

```
ZZA1 R0      --> WR0  I1
ZZA1 R1      -->
ZZA1 R2      --> WR0  I2
ZZA1 R3      --> WR0  I4
ZZA1 R4      --> WR1  I0
ZZA1 R5      -->
ZZA1 R6      --> WR1  I1
ZZA1 R7      --> WR1  I3
```



1 SOURCE OF THE SIGNAL - The read data bit leaves the group of memory chips called ZZA1. R7 specifies that chip 7 of the group is being used.

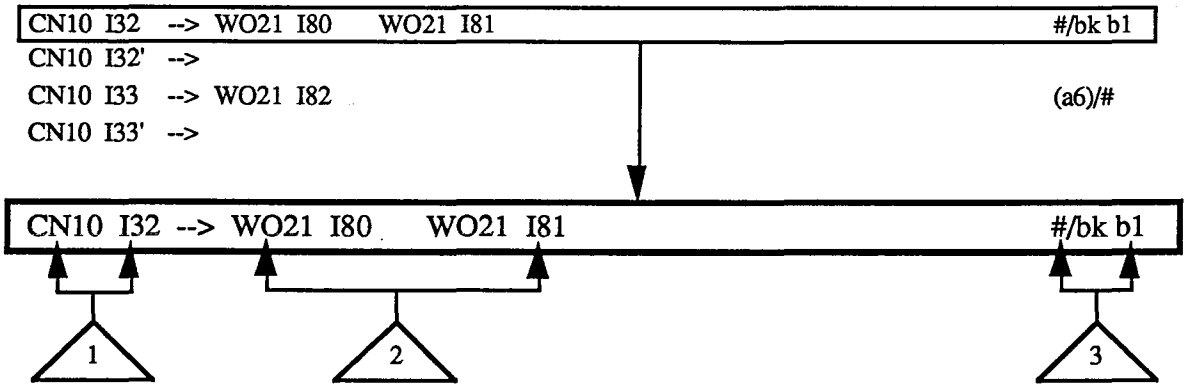
2 DESTINATION OF THE SIGNAL - ZZA1 R7 sends the read data bit to the option (WR1). The read data bit enters (WR1) as term I3.

YM29/07

PCTAB Memory (continued)

```
CONNECTOR: CN10                          PCTAB P/N 31209000   09/28/88  11:34:51  PAGE 978

CN10 I28  --> WO20 I80    WO20 I81                                        #/bk b1
CN10 I28' -->
CN10 I29  --> WO20 I82                                                    (a2)/#
CN10 I29' -->
CN10 I30  --> WO20 I83                                                    a6/#
CN10 I30' -->
CN10 I31  --> ZA21 I101                                                   a10
CN10 I31' -->
```



1 CONNECTOR - The connector CN10 is being used to bring Bank bit 2^1 on to the memory module. The term used for the signal is I32.

2 DESTINATION OF THE SIGNAL - Bank bit 2^1 is sent to option (WO21). The signals enter (WO21) as I80 and I81.

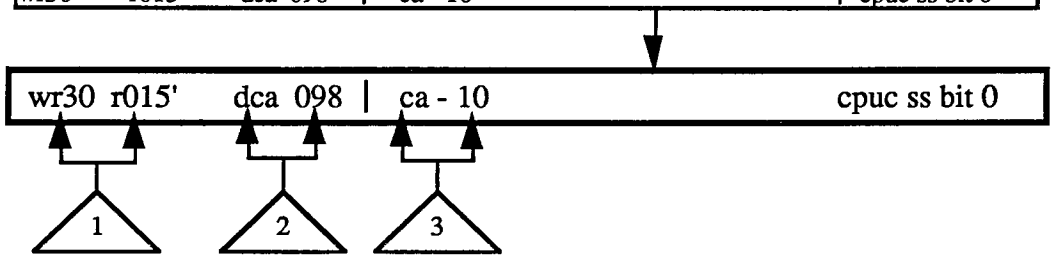
3 DESCRIPTION OF THE SIGNAL - #/bk b1
A / B

MEM0	A
MEM1	A
MEM2	B
MEM3	B
MEM4	B
MEM5	B
MEM6	A
MEM7	A

This comment can be used to describe two different signals. The "#" is the first comment which will be called "A". Bk b1 is the second comment which will be called "B". The "#" symbolizes an unused signal. CN10 I32 is not being used on MEM0, MEM1, MEM6, or MEM7. These four modules use the comment in the "A" position. CN10 I32 is being used by bk b1 on MEM2, MEM3, MEM4, and MEM5. These four modules use the comment in the "B" position.

YM29/08

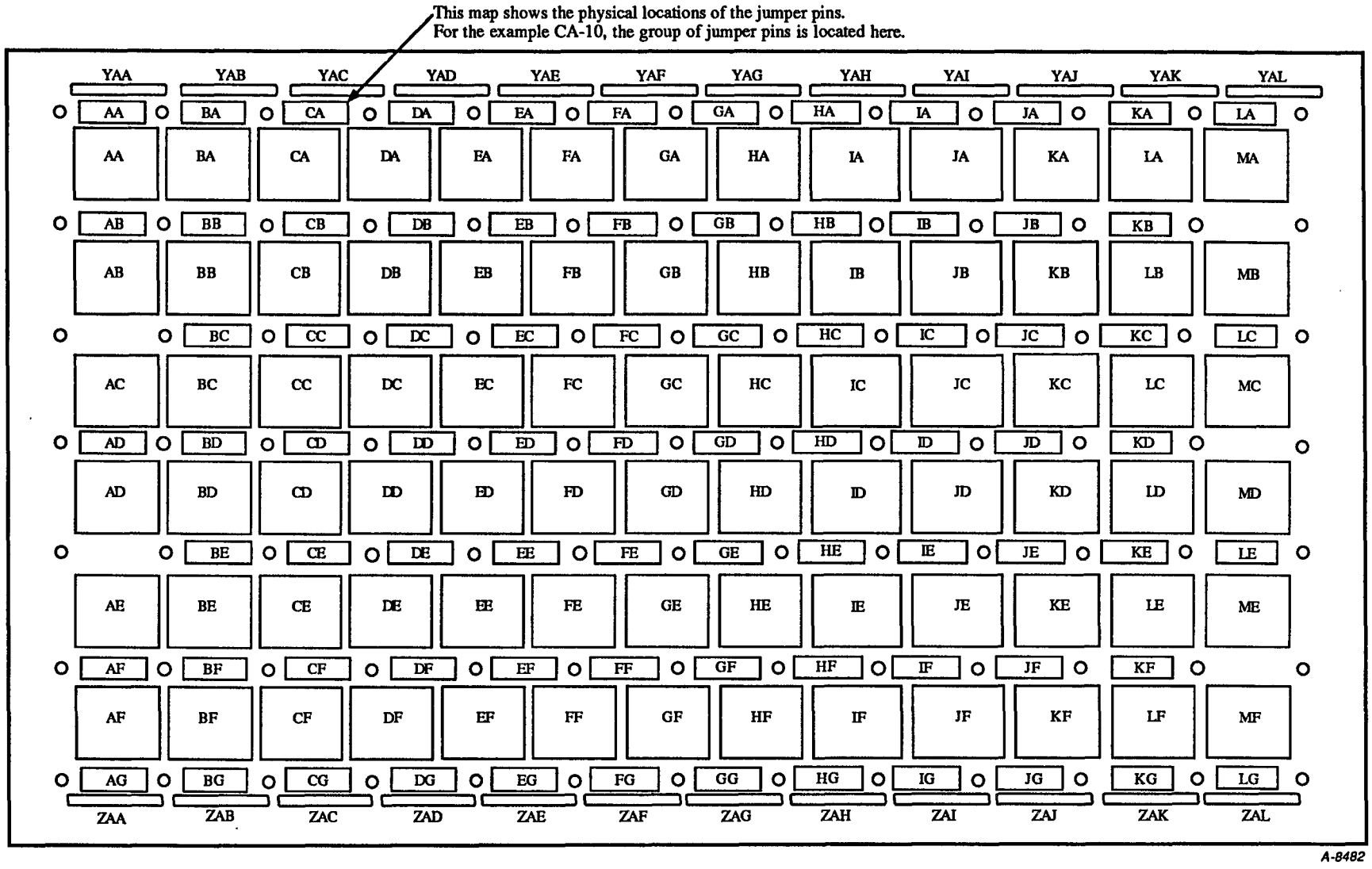
OPTION	TERM	LOC PIN	JUMPERS	DESCRIPTION
wr30	r008'	dca 011	cb - 04	cpuf ss bit 2
wr30	r009'	dca 009	ea - 35	cpue ss bit 0
wr30	r010'	dca 007	ea - 39	cpue ss bit 1
wr30	r011'	dca 148	bb - 44	cpue ss bit 2
wr30	r012'	dca 106	ca - 04	cpud ss bit 0
wr30	r013'	dca 103	ca - 06	cpud ss bit 1
wr30	r014'	dca 101	ca - 08	cpud ss bit 2
wr30	r015'	dca 098	ca - 10	cpuc ss bit 0



1 SOURCE OF THE SIGNALS - CPU C ss bit 2^0 leaves option (WR30) as term R015'.

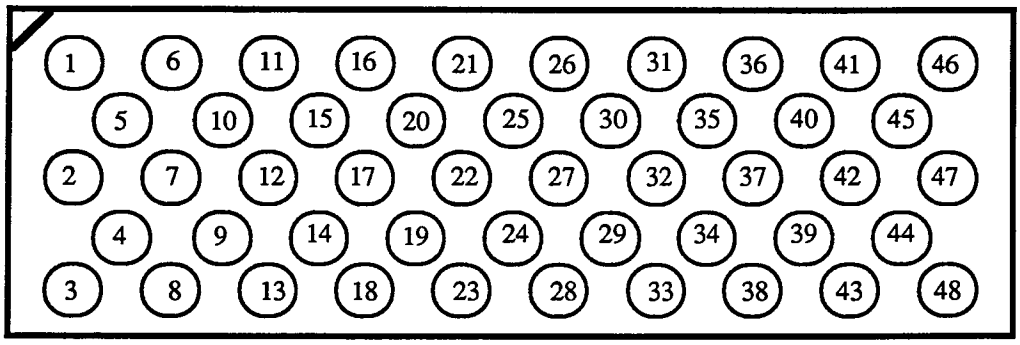
2 PHYSICAL LOCATION - (WR0) is physically located on board D, column C, row A. R015' leaves the option via pin 98.

3 JUMPER PIN LOCATION - The jumper pin used to transfer this signal to another printed circuit (PC) board is physically located at column C, row A, pin 10.

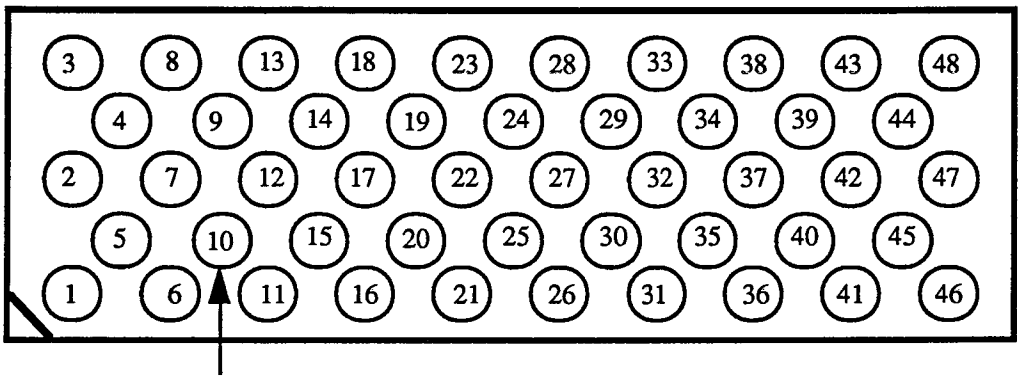


CRAY Y-MP PHYSICAL LOCATION MAP FOR A AND C BOARDS

CRAY Y-MP JUMPER BLOCK LAYOUT



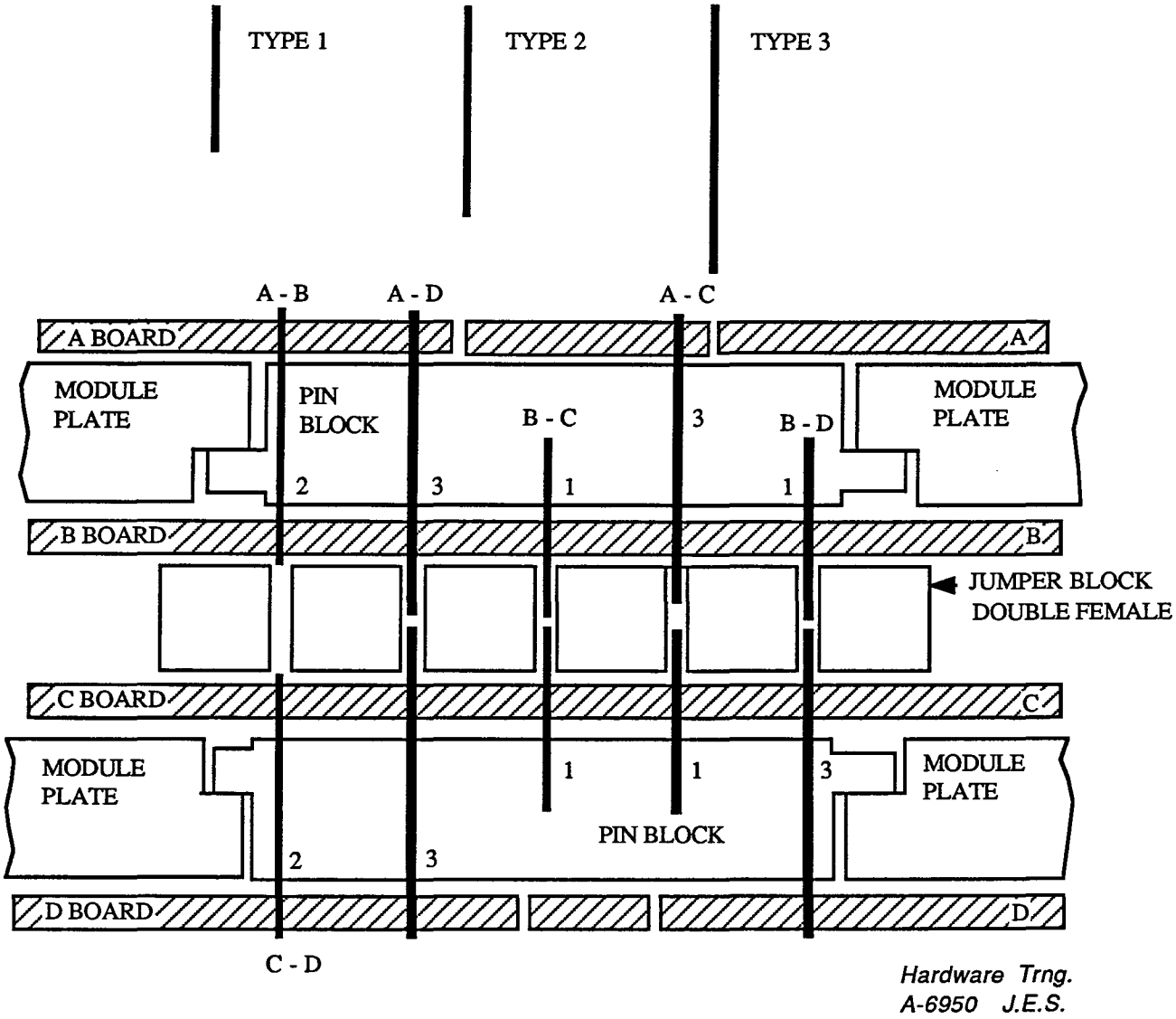
The jumper block layout shows the numbering scheme of the jumper pins within one group. The dark line at the top left hand corner designates pin 1. This placement of pin 1 is true if looking at the A or C board of the module. If looking at the B or D board of the module, pin 1 would be located at the lower left hand corner. The jumper layout of the B and D board looks like the diagram below.



For the example CA-10, pin 10 is located here if looking at the B or D boards.

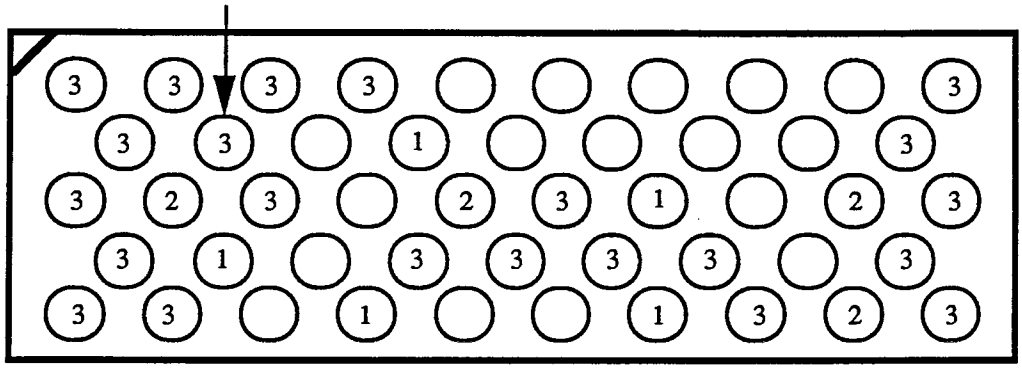
YM29/10

The next section of the jumper pin manual lists the type of jumper pins used at each location. There are three types of jumper pins: type 1, type 2, and type 3.

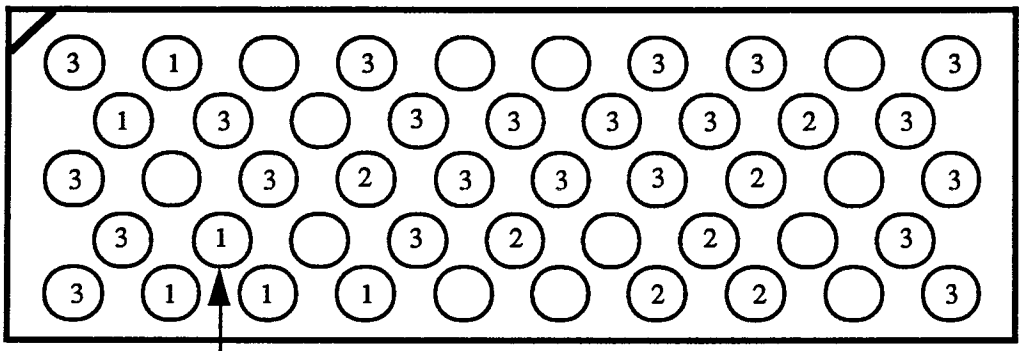


YM29/11

For the example CA-10, the type of jumper pin used for pin 10 on the C/D half of the module is type 3.



BOARD C
BLOCK CA



BOARD B
BLOCK CA

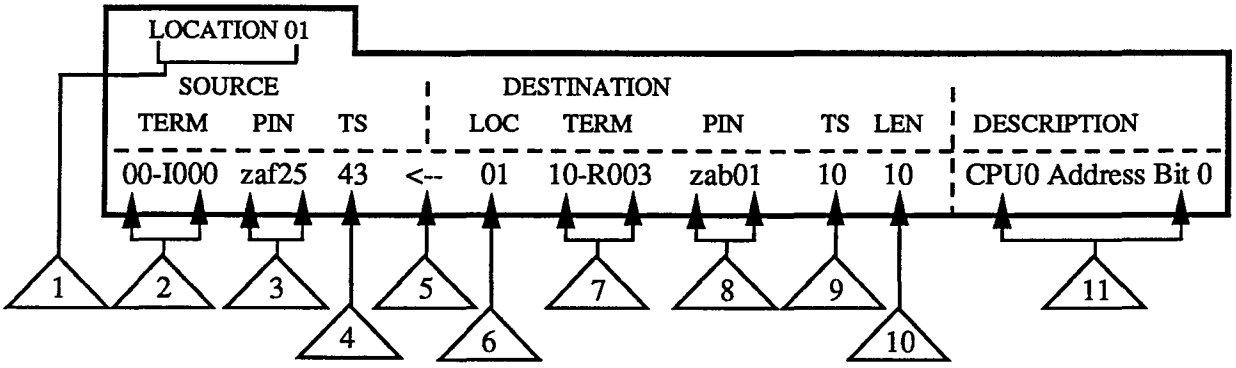
Pin 10 on the A/B half of the module is a type 1 jumper pin.

YM29/12

Wire Tabs

LOCATION 01 — CRAY Y-MP WIRE TABS S/N 1014 — PAGE 1

SOURCE				DESTINATION					
TERM	PIN	TS		LOC	TERM	PIN	TS	LEN	DESCRIPTION
00-I000	zaf25	43	<--	01	10-R003	zab01	10	10	CPU0 Address Bit 0
00-I001	zaf24	42	<--	01	10-R015	zbb27	10	11	CPU0 Address Bit 1
00-I002	zaf23	44	<--	01	10-R029	zcb01	10	12	CPU0 Address Bit 2
00-I003	zbg08	44	<--	01	10-R041	zdb27	11	12	CPU0 Address Bit 3
00-I004	zbg07	44	<--	01	10-R005	zaf12	10	12	CPU0 Address Bit 4
00-I005	zbg06	45	<--	01	10-R018	zbe18	10	12	CPU0 Address Bit 5
00-I006	zaf01	42	<--	01	10-R031	zcf12	10	10	CPU0 Address Bit 6
00-I007	zaf02	42	<--	01	10-R044	zde18	10	10	CPU0 Address Bit 7



1 MODULE LOCATION - Location 01 specifies the module seated at physical location 1 in the chassis of the mainframe. Location 1 in the CRAY Y-MP/832 mainframe seats MEM0 in Section 0 of the memory.

2 TERM - The term is the connector being used by the signal. For this example the connector is CN0. The term is I0.

3 PIN - The pin is the physical location of CN0 I0. CN0 I0 is located on the Z axis, board A, row F, pin 25.

4 TS - The time segment (TS) specifies when the signal arrives on the module. For this example, CPU0 address bit 2^0 arrives on the module at TS 43.

5 ARROW - The arrow designates the direction of the signal. The arrow always points to the destination of the signal.

NOTE

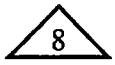
Ignore the source and destination comments of the heading because the comments are not always correct.

---

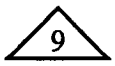
6 LOC. - Location (Loc.) specifies the physical location of the module in the mainframe where the signal came from.

A-8523

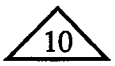
TERM - The term is the connector used on the module. For this example the connector is CN10 R3.



PIN - This is the physical location of CN10 R3. CN10 R3 is located on the Z axis, board A, row B, pin 1.



TS - This is the TS in which the signal CPU0 address bit 2^0 leaves the module. This signal leaves the module at TS 10.



LEN - LEN specifies the length of the wire used to transfer the signal. The wire used to transfer address bit 2^0 is 10 inches in length.

DESCRIPTION OF THE SIGNAL

A-8524

PCBDA, PCBDB, PCBDC, PCBDD

Documents where the memory options are located, called "chip map", and also contains a "connector map" which tells the loading on the "Z" and "Y" edge connectors. PCBDA loads board A, PCBDB loads board B, PCBDC loads board C and PCBDD loads board D.

PCLDA, PCLDB, PCLDC, PCLDD

Documents the loading of Data, Address and Control from the edge connectors to the logic chips. Each CPUs path into the memory module is documented. PCLDA handles CPU A/B; PCLDB handles CPU C/D; PCLDC handles CPU E/F; and PCLDD handles CPU G/H. PCLDA loads board A, PCLDB loads board B, PCLDC loads board C and PCLDD loads board D when looking at a particular option.

Subsection Data A-D

Documents the writing or reading of the data into each memory chip within the 8 banks per subsection. Subsection Data A contains subsection 0, 1; Subsection Data B contains subsection 2, 3; Subsection Data C contains subsection 4, 5 and Subsection Data D contains subsection 6, 7.

Bank Subsection 0-7

Documents the loading of the Address and Control into each memory chip within the 8 banks per subsection 0 - 7.

MPT WB-ZZ

Documents what comes into each pin of the 148-pin chip for options WB - WY, ZA, ZS.

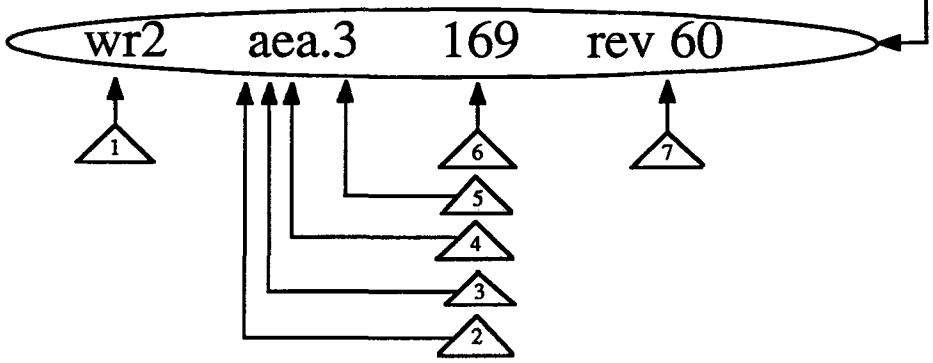
Options WB-WY, ZA, ZS Boolean

Documents the Boolean equation used inside the logic chips. The Boolean equations are translated into an arrangement of macro cells which perform logical functions for the computational process.

$pcbda 06-29-88

$chip map

wl0	aba.2	164	rev 60
wr0	aca.3	169	rev 60
wr1	ada.3	169	rev 60
wr2	aea.3	169	rev 60
zs0	afa.1	70	rev 61
to0	aga.2	02	rev 02
zs1	aha.1	70	rev 61
wr3	aia.3	169	rev 60
wr4	aja.3	169	rev 60
wr5	aka.3	169	rev 60
wl1	ala.2	164	rev 60



1 OPTION TYPE - In this example the option is a (wr2).

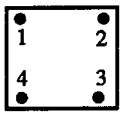
2 BOARD DESIGNATOR - The (wr2) option is found on the A board.

3 COLUMN DESIGNATOR - The (wr2) option is on the A board in Column E, or the longside of the module.

4 ROW DESIGNATOR - The (wr2) option is on the A board in Column E, Row A. Row A is on the short side of the module.

5 PIN ALIGNMENT - The (wr2) option has alignment .3. This puts alignment asterisk in the lower right corner on the memory module, if the coolant connections are to your left.

In general the placement is



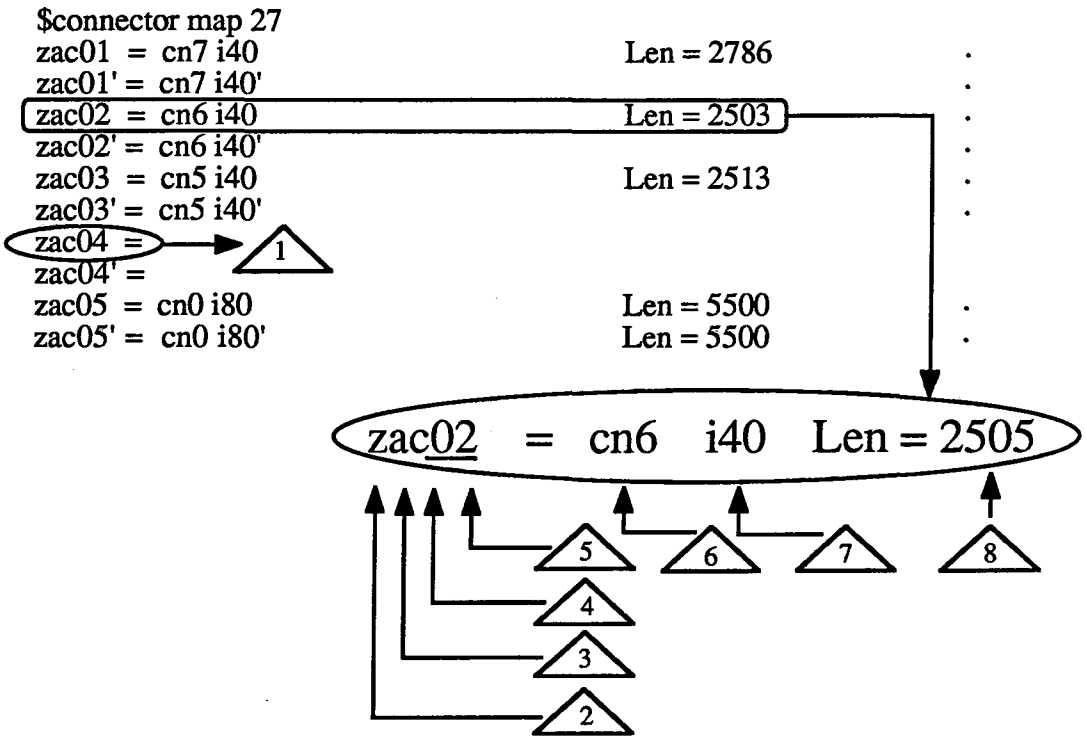
6 CHIP TYPE

7 REVISION OF THE CHIP

Hardware Trng.
A-7839 J.E.S.

CRAY Y-MP PCBDA $ CHIP MAP

PCBDA



1 CONNECTOR MAP 27 - Unused pin on the edge connector, the edge connector has 27 pins.

2 AXIS DESIGNATOR - The Edge Connector is located on the "z" axis or it can be the "y" axis.

3 BOARD DESIGNATOR - The Edge Connector is found on the A board. The letters would range from A to D for boards A through D.

4 COLUMN DESIGNATOR - Read as Board A, Column C. Identifing a 27-pin Edge Connector on the "z" axis of the memory module.

5 PIN DESIGNATOR - Board A, Column C, pin 02. Pin 02 is a true pin, pin 02' would be the false pin.

6 PINS LOGICAL VARIABLE - Identifies what the pin is being used for. In this case pin 02 is used by CPU 6.

7 PIN BOOLEAN TERM - Pin 02, on Edge Connector C, has an input Boolean term i40 from CPU 6.

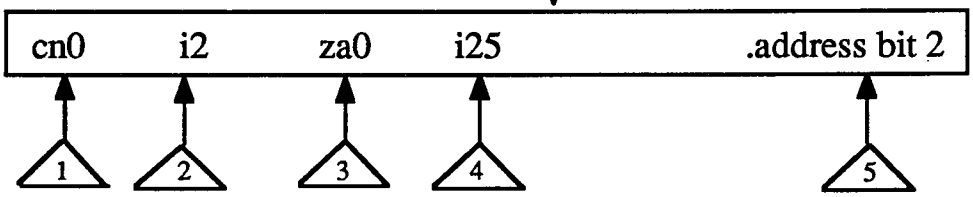
8 LENGTH

PCLDA - PC LOAD FILE

```
pcload:pclda
rev:   0
date:  09-19-86
title: pc load file for cpu0 , 1 and a board

$net list cn0  ************** cpu0 ************************

cn0 i0   za0  i27                                          .address bit 0
cn0 i0'                                                    .
cn0 i1   za0  i26                                          .address bit 1
cn0 i1'                                                    .
cn0 i2   za0  i25                                          .address bit 2
cn0 i2'                                                    .
```



CONNECTOR NUMBER - Connector Number 0 = cn0

Connector Number 7 = cn7

cn0 - cn7 for the 8 CPU load paths on to and off from the memory module.

EDGE CONNECTOR TERM - Input term into the module from CPU 0, which comes into the edge connector as term (i2). The letter "i" for input, or the letter "r" for output.

OPTION TYPE - CPU 0 will come into the (za0) option type.

OPTION INPUT TERM - I25 is the input term into the (za0) option.

PCLDA COMMENT - I2 coming in from the Edge Connector is Address bit 2 from CPU 0 goes into the (za0) option as i25.

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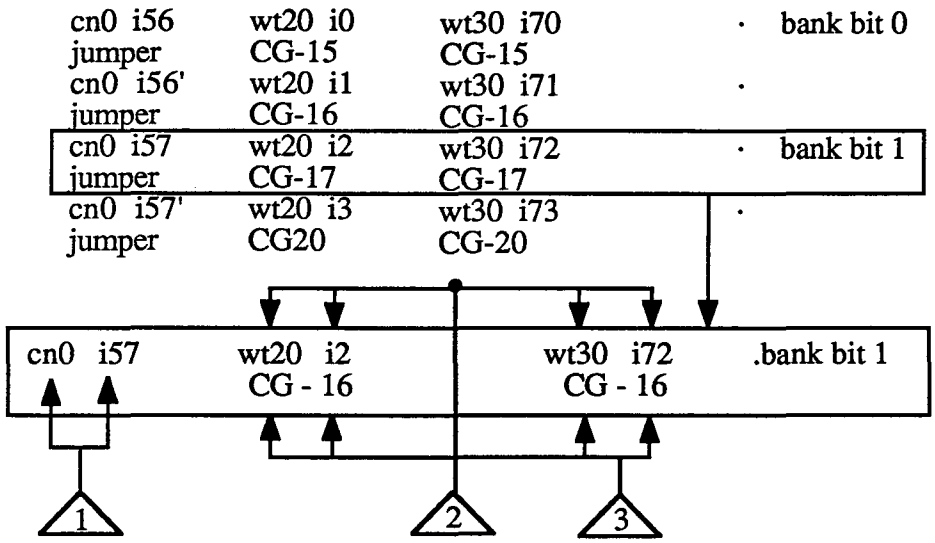
PCLDA - PC Load File (continued)



1 CPU INPUT - CPU 0 Bank Bit 1 signal comes into the memory module as i57.

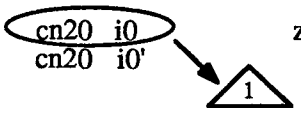
2 OPTION INPUT - The Bank Bit 1 signal is sent to (wt20) and (wt30) options. The signal comes into (wt20) as i2 and i72 on (wt30).

3 JUMPER LOCATION - The signal enters the A board via cn0. (wt20) and (wt30) are physically located on the C and D boards, respectively. To send the signal from the A board to the C and D boards a jumper pin is needed. This jumper is located in column C, Row G, pin number 16.

CG-16
- row - short side of module
- column - long side of module

PCLDA - D (continued)

$ y connector fan-out : master clear



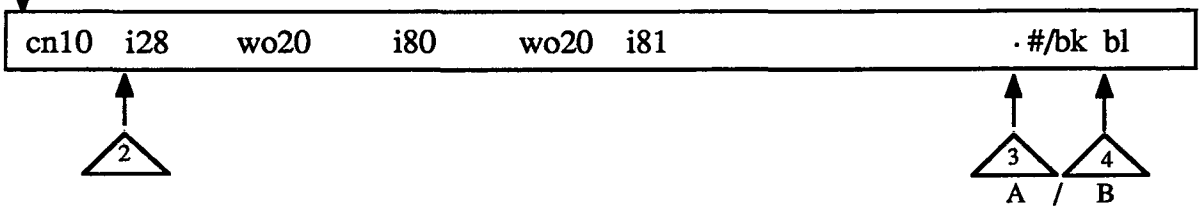
.master clear

$ z connector fan-out inputs

cn10 i26 wb20 i82
cn10 i26' ww20i80
cn10 i27 ww20i81
cn10 i27'
cn10 i28 wo20 i80
cn10 i28'
cn10 i29 wo20 i82
cn10 i29'

wb20 i83
wo20 i81

.goss
5 → .a2/#
.#/bk bl
6 → .(a2)/#



1 cn20 i0 - cn20 i0 comes in on the "y" connector denoted by cn20.

2 cn10 i28 - cn10 i28 comes in on the "z" connector denoted by cn10.

3 Not Used - # symbolizes that when in a particular slot of the machine the particular term is not used.

Mem. 0, A
Mem. 1, A
Mem. 2, B
Mem. 3, B
Mem. 4, B
Mem. 5, B
Mem. 6, A
Mem. 7, A

The first two and last two are the same configuration, as are the middle four.

4 #/bk bl - Abbreviated, Bank bit 1. When in A position, cn 10 i28 is not used. When in B position, cn 10 i28 is Bank bit 1.

5 a2/# - Abbreviate for address 2 or address bit 2 when used in A's position.

6 (a2)/# - (a2)/#, address bit 2 is used when in the A's position, a2 is in the inverted state shown by (a2).

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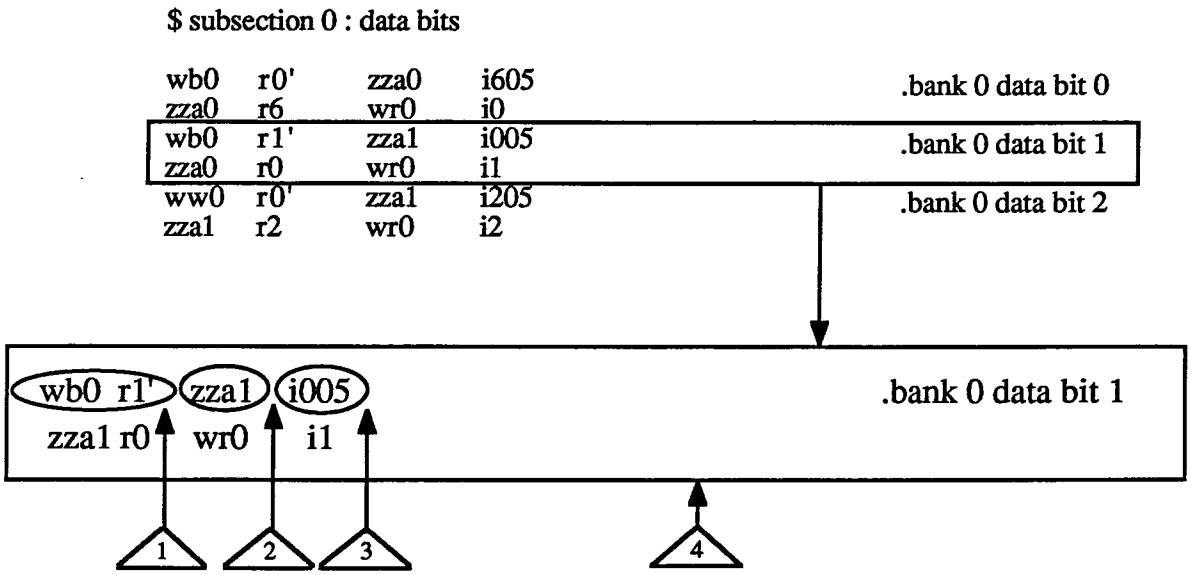
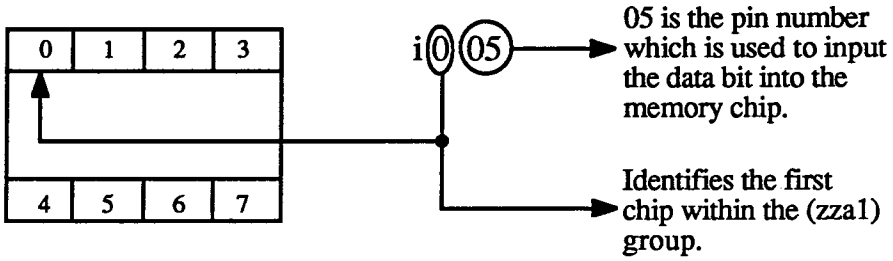
Subsection Data A - D



1 ORIGINATION - Bank 0 data bit 1 leaves the (wb0) option as term r1'.

2 GROUP DESCRIPTION - Bank 0 bit 1 is sent to a group of memory chips called zza1. The group zza1 can contain up to 8 memory chips.

3 CHIP AND INPUT DESIGNATOR - The i005 can be broken into two parts:



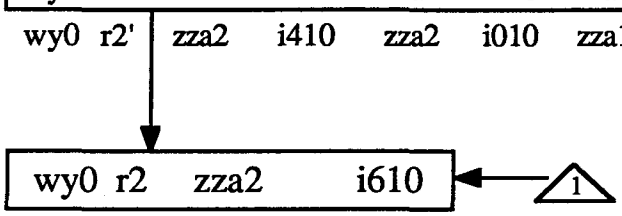
4 LINE READS AS - Bank 0 data bit 1 leaves the (wb0) option on r1'on a Write operation to the (zza1) group, chip 0, and comes into chip 0 on pin 05. Bank 0 data bit 1 will leave (zza1) chip 0 as r0 on a Read operation and come into (wr0) option as i1.

BANK SUBSECTION 0 - 7

$ fn: addrss0
$ rev: 0
$ date: 06-22-88
$ title: address fanout to ss0, bank n - n + 7

$ bank n

wy0	r0	zza2	i608	zza2	i208	zza1	i608	zza1	i208	zza0	i608	.addr0
wy0	r0'	zza2	i408	zza2	i008	zza1	i408	zza1	i008			
wy0	r1	zza2	i609	zza2	i209	zza1	i609	zza1	i209	zza0	i609	.addr1
wy0	r1'	zza2	i409	zza2	i009	zza1	i409	zza1	i009			
wy0	r2	zza2	i610	zza2	i210	zza1	i610	zza1	i210	zza0	i610	.addr2
wy0	r2'	zza2	i410	zza2	i010	zza1	i410	zza1	i010			

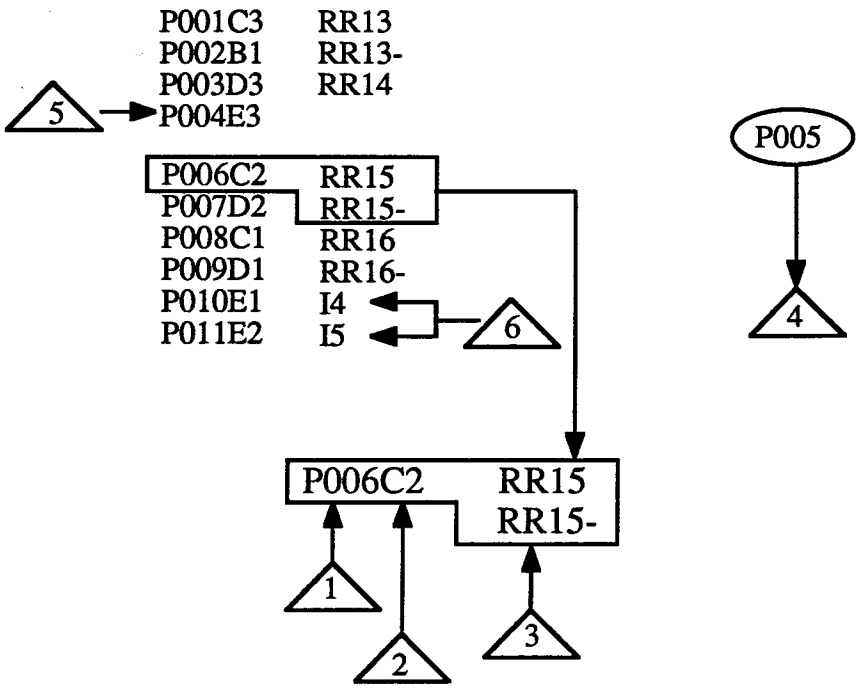


The Bank Subsection 0 - 7 reads the same as the Subsection Data A - D, except the Bank Subsection 0 - 7 documents Address and Control to the memory module as per Subsection 0 - 7. The Subsection Data A - D documents only the data per the module boards A - D.

1 This portion of Bank Subsection 0 would read as the (wy0) option outputs as r2, r2 is address bit 2^2 for bank n. Address bit 2^2 or r2 goes to the (zza2) group, chip 6 and comes into the memory chip on pin 10.

MPT ZM-ZZ MAP TABLE

```
$$$$ OPTION ZM * DATE 07-11-86 * MPTBL ****
$$$$ DATE OF LAST CHANGE  07-11-86 ****
```



1 PIN NUMBER - P006 calls out pin 6 of the 148 pin package.

2 INTERNAL PIN ASSIGNMENTS - Internal chip pad C2 is in Column C, Row 2.

3 PIN TERM - Pin 6 is an output term from the "R" term meaning output. The output term is R15 true. In the case with R15-, R15- is the false output.

4 POWER/GROUND - Power/ground is sometimes right justified. P005 happens to be VCC0.

5 UNUSED PIN - An unused pin is left blank.

6 INPUT PINS - Input pins are identified by the letter "I" as in I4 or I5.

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LOGICAL VARIABLES

Z AXIS

cn 0-7 (Connector Number) A - H on Memory Module	i0-16	Address
	i17	Go Write
	i18-19	Abort
	i20-28	Data in
	i30-37	GOSS 0-7
	i40-55	GOSS/Bank Bit 2^2
	i56-63	Bank bit 1, 0 (four copies)
cn 10	i0-47	Fanout
	r0-51	
	r100-151	
	r200-251	
	r700-751	

Y AXIS

cn 0-7 A-H	i70-72	Subsection Select Bit 2^0 - 2^2
cn 20	i0	Master Clear
	i1	3 CP Write Enable
	i2-3	Bank Busy Select
	i10-13	Clock Input
	i20-23	1-8 Fanout
	r0-8	Read Data
	r10-13	
	⋮	
	r70-73	

IN GENERAL

cn 30	I/O channels
cn 40	Deadstart Panel
cn 50	Test Points

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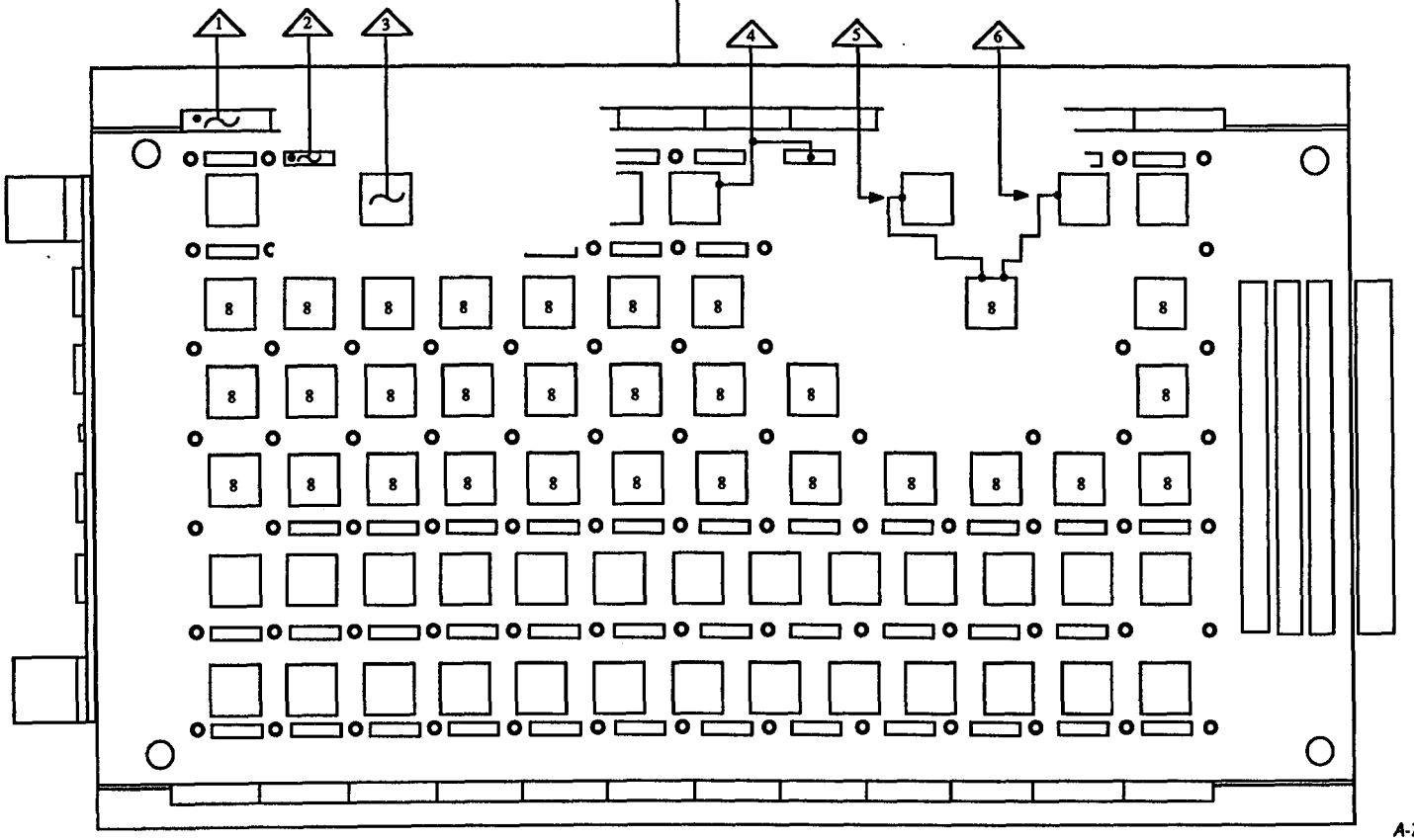
COMPONENTS PLACEMENT AND ASSIGNMENT DOCUMENTATION

1. EDGE CONNECTOR - PCBDA - PCBDD UNDER $ CONNECTOR MAP 27.
2. FEED THRU, JUMPERS - CALLED OUT WHEN USED IN PCLDA - PCLDD AS "JUMPER".
3. OPTION PLACEMENT AND TYPE - PCBDA - PCBDD UNDER $ CHIP MAP, ALSO GIVES THE CHIPS ROTATION.

LOGIC PATHS DOCUMENTATION

4. EDGE CONNECTOR USAGE - PCLDA - PCLDD TAKE THE SIGNAL FROM THE EDGE CONNECTOR TO AN OPTION TYPE OR "JUMPER".
5. DATA TO OR FROM THE MEMORY CHIP - SUBSECTION DATA A - D, SUBSECTION DATA A CONTAINS SUBSECTION 0, 1 DATA.
6. ADDRESS/CONTROL TO MEMORY CHIP - BANK SUBSECTION 0 - 7.



CRAY Y-MP MEMORY (64K x 1) DOCUMENT ASSIGNMENT

CRAY Y-MP MODULE LOCATIONS

MEMORY DATA	MEMORY MODULE LOCATION Section 0	Section 1	Section 2	Section 3
Bits 2^0 - 2^8	Location 1	9	25	33
Bits 2^9 - 2^{17}	Location 2	10	26	34
Bits 2^{18} - 2^{26}	Location 3	11	27	35
Bits 2^{27} - 2^{35}	Location 4	12	28	36
Bits 2^{36} - 2^{44}	Location 5	13	29	37
Bits 2^{45} - 2^{53}	Location 6	14	30	38
Bits 2^{54} - 2^{62}	Location 7	15	31	39
Bits 2^{63} - 2^{71}	Location 8	16	32	40

CPU NUMBER	LOCATION
0	Location 17
1	Location 18
2	Location 19
3	Location 20
4	Location 21
5	Location 22
6	Location 23
7	Location 24

MEMORY ADDRESS

2^{25} 2^{24} 2^{23} 2^{22} 2^{21} 2^{20}	2^{19}	2^{18} 2^{17} 2^{16} 2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^9 2^8	2^7 2^6 2^5	2^4 2^3 2^2	2^1 2^0
X X X X X X	X	X X X X X X X X X X X	X X X	X X X	X X
2^{16} 2^{15} 2^{14} 2^{13} 2^{12} 2^{11} (2^{17})	C.S. (2^{16})	2^{10} 2^9 2^8 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0	2^2 2^1 2^0	0 - 7 GOSS	0 - 3 Sec.

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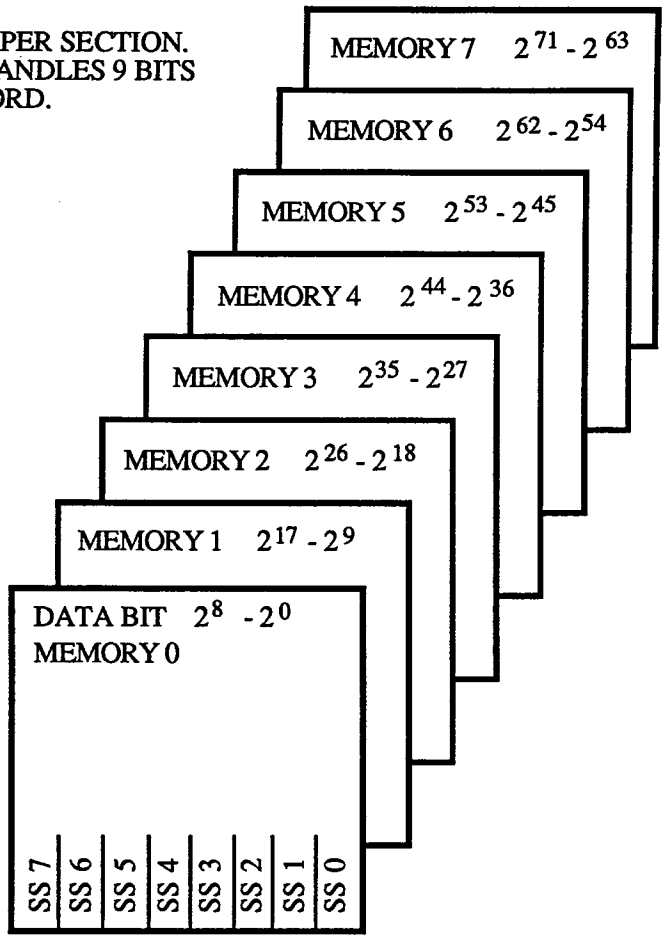
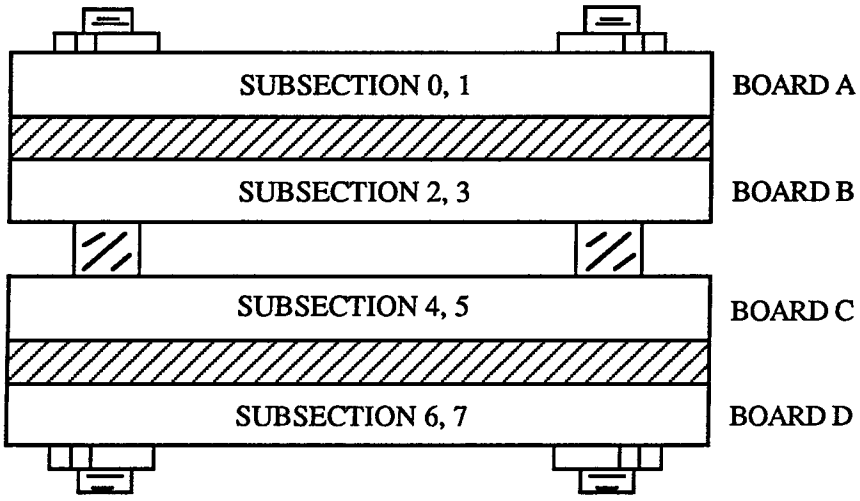
EIGHT MODULES PER SECTION.
EACH MODULE HANDLES 9 BITS
OF THE 72-BIT WORD.





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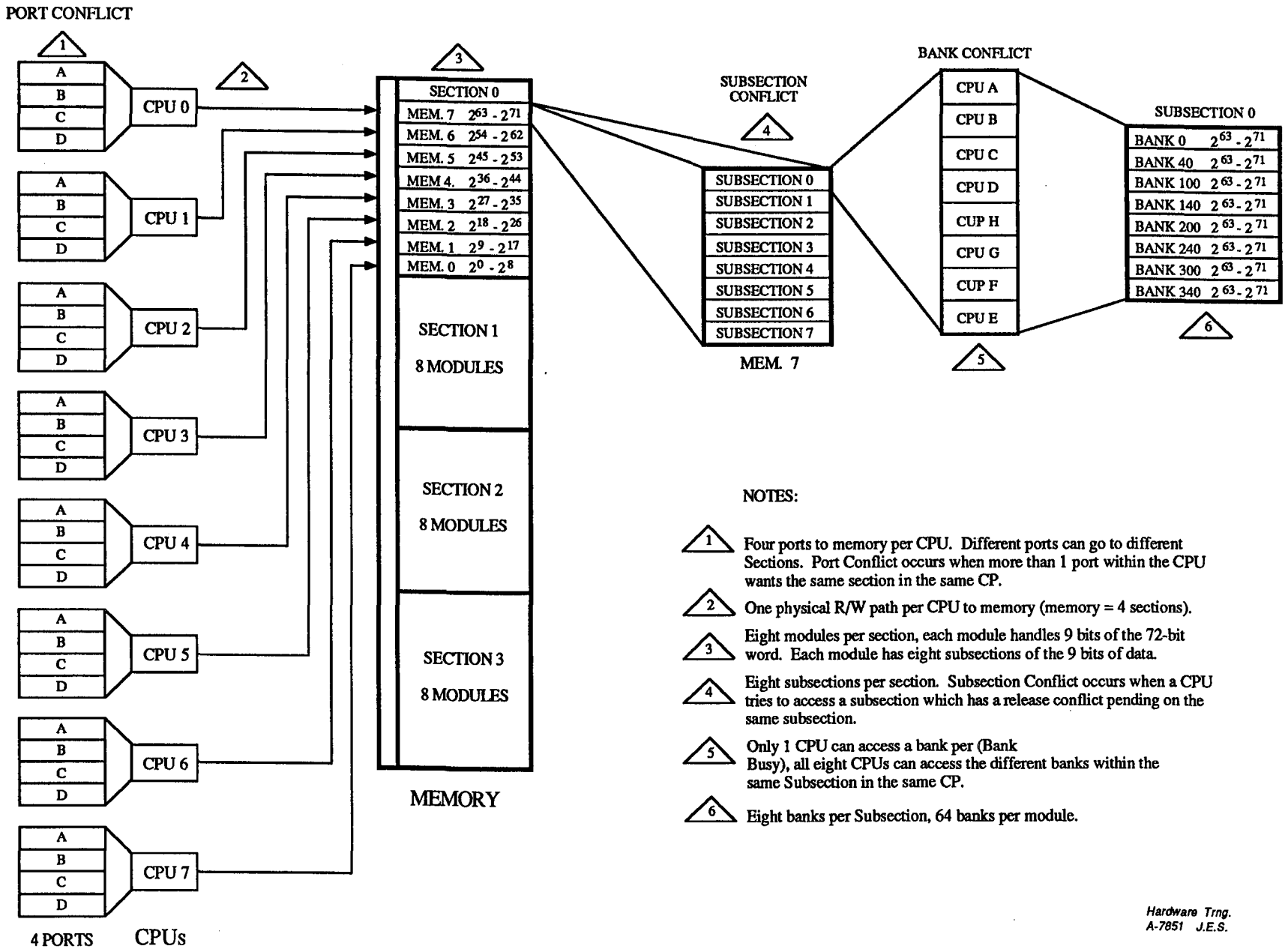
CRAY Y-MP MEMORY MODULE/SUBSECTION LAYOUT



NOTES:

1. Four ports to memory per CPU. Different ports can go to different Sections. Port Conflict occurs when more than 1 port within the CPU wants the same section in the same CP.
2. One physical R/W path per CPU to memory (memory = 4 sections).
3. Eight modules per section, each module handles 9 bits of the 72-bit word. Each module has eight subsections of the 9 bits of data.
4. Eight subsections per section. Subsection Conflict occurs when a CPU tries to access a subsection which has a release conflict pending on the same subsection.
5. Only 1 CPU can access a bank per (Bank Busy), all eight CPUs can access the different banks within the same Subsection in the same CP.
6. Eight banks per Subsection, 64 banks per module.

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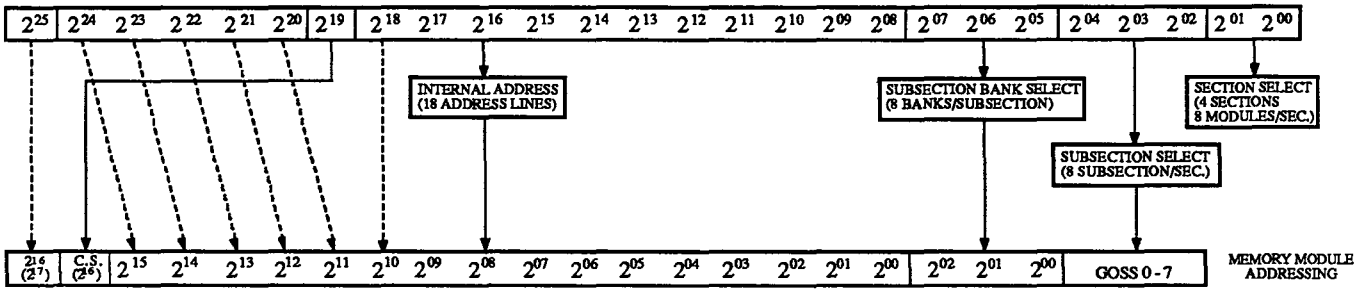
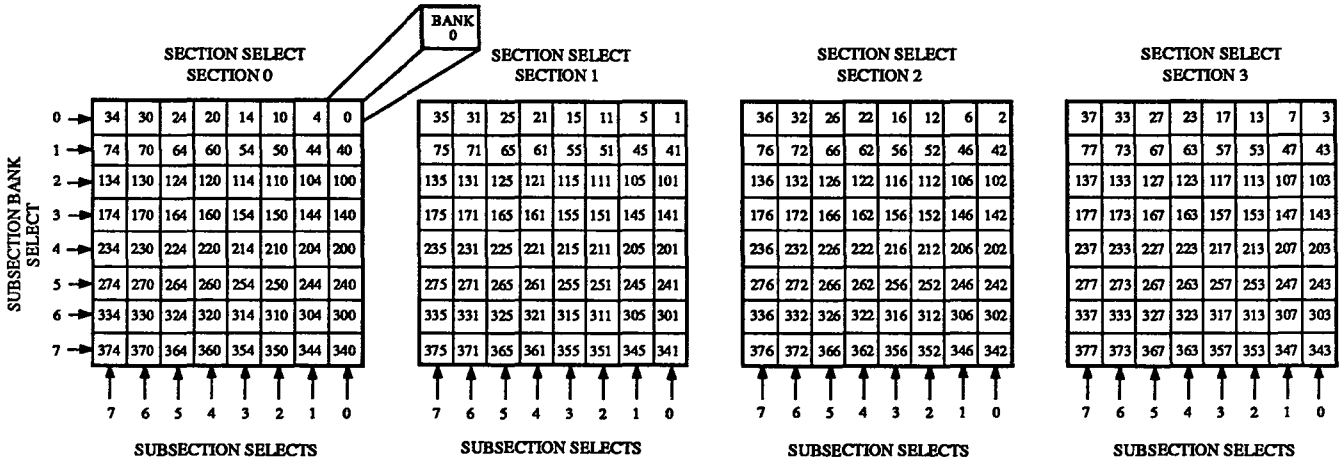
A-7851 J.E.S.

CRAY Y-MP MEMORY SUBSECTION

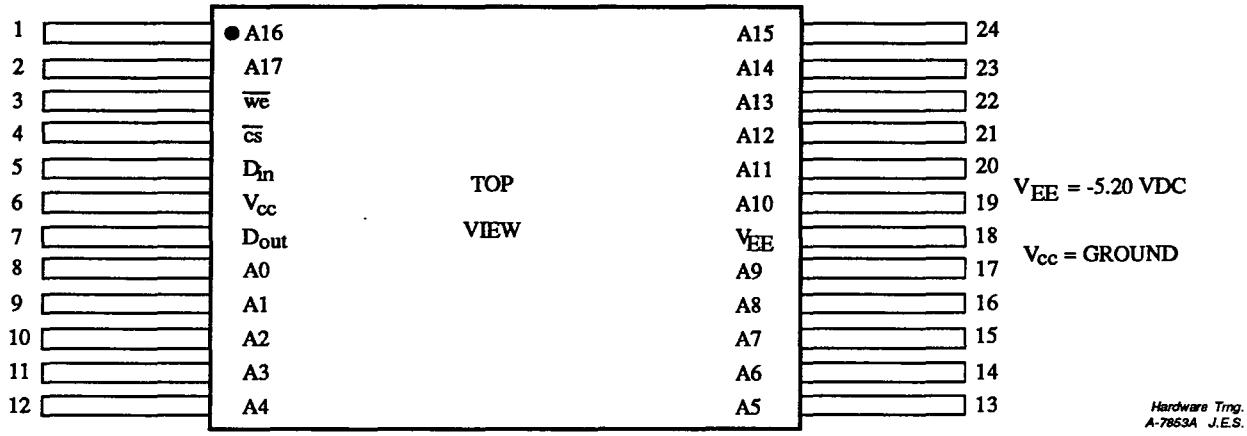
ADDRESS



BANK/SUBSECTION LAYOUT



256K x 1 BIMOS MEMORY CHIP



CRAY Y-MP MEMORY ADDRESSING

MEMORY MODULE

DATA BIT	MEM. 0	MEM. 1	MEM. 2	MEM. 3	MEM. 4	MEM. 5	MEM. 6	MEM. 7
N	2^0	2^9	2^{18}	2^{27}	2^{36}	2^{45}	2^{54}	2^{63}
N + 1	2^1	2^{10}	2^{19}	2^{28}	2^{37}	2^{46}	2^{55}	2^{64} CB0
N + 2	2^2	2^{11}	2^{20}	2^{29}	2^{38}	2^{47}	2^{56}	2^{65} CB1
N + 3	2^3	2^{12}	2^{21}	2^{30}	2^{39}	2^{48}	2^{57}	2^{66} CB2
N + 4	2^4	2^{13}	2^{22}	2^{31}	2^{40}	2^{49}	2^{58}	2^{67} CB3
N + 5	2^5	2^{14}	2^{23}	2^{32}	2^{41}	2^{50}	2^{59}	2^{68} CB4
N + 6	2^6	2^{15}	2^{24}	2^{33}	2^{42}	2^{51}	2^{60}	2^{69} CB5
N + 7	2^7	2^{16}	2^{25}	2^{34}	2^{43}	2^{52}	2^{61}	2^{70} CB6
N + 8	2^8	2^{17}	2^{26}	2^{35}	2^{44}	2^{53}	2^{62}	2^{71} CB7

NOTE: To locate the bad memory chip you need the failing Address and the failing bit.

From the failing address calculate:

1. Section _____
2. Subsection _____
3. Subsection Bank _____
4. Chip Select _____

Failing bit is associated to Data bits (N - N + 8).
Failing module is associated with the failing bit.

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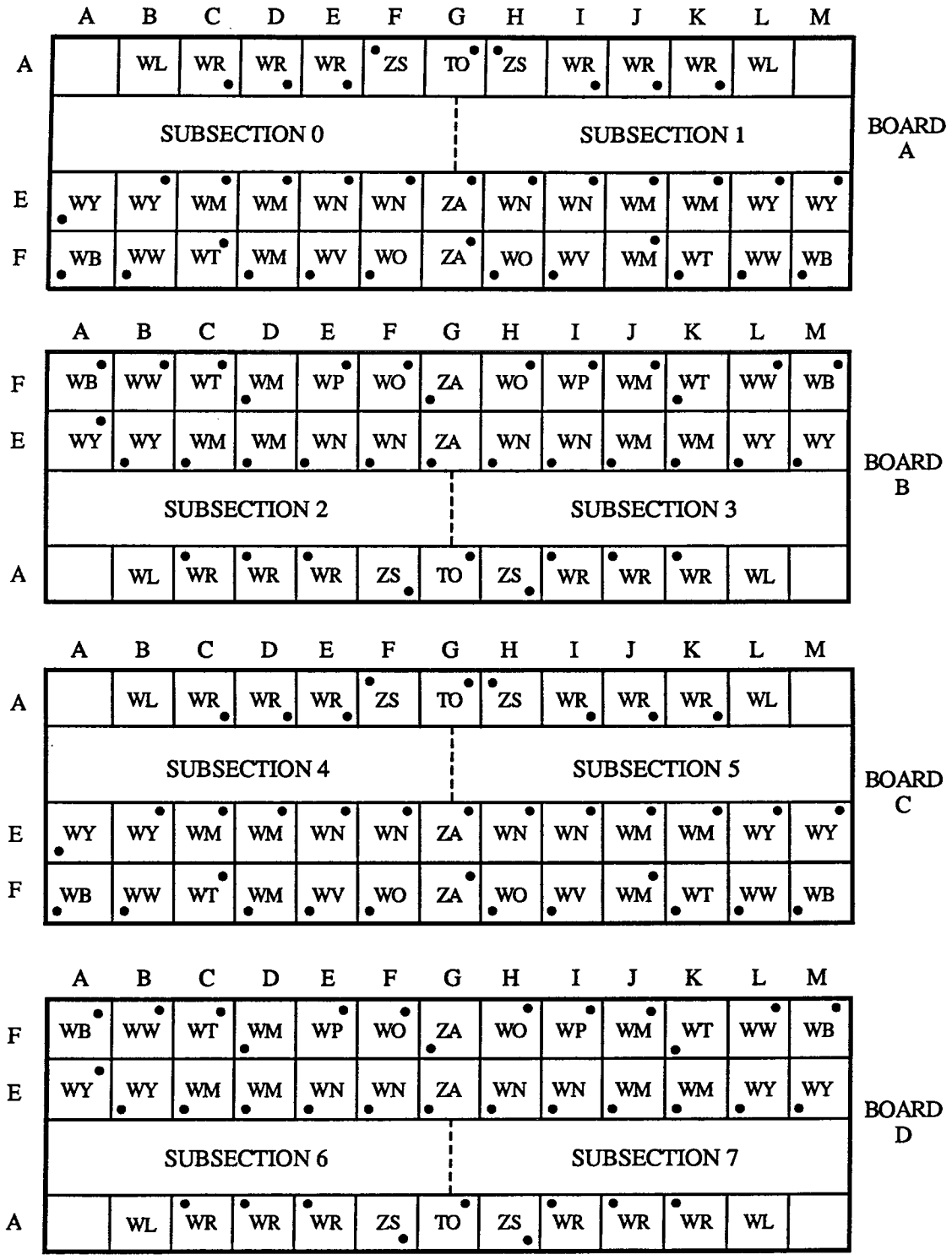
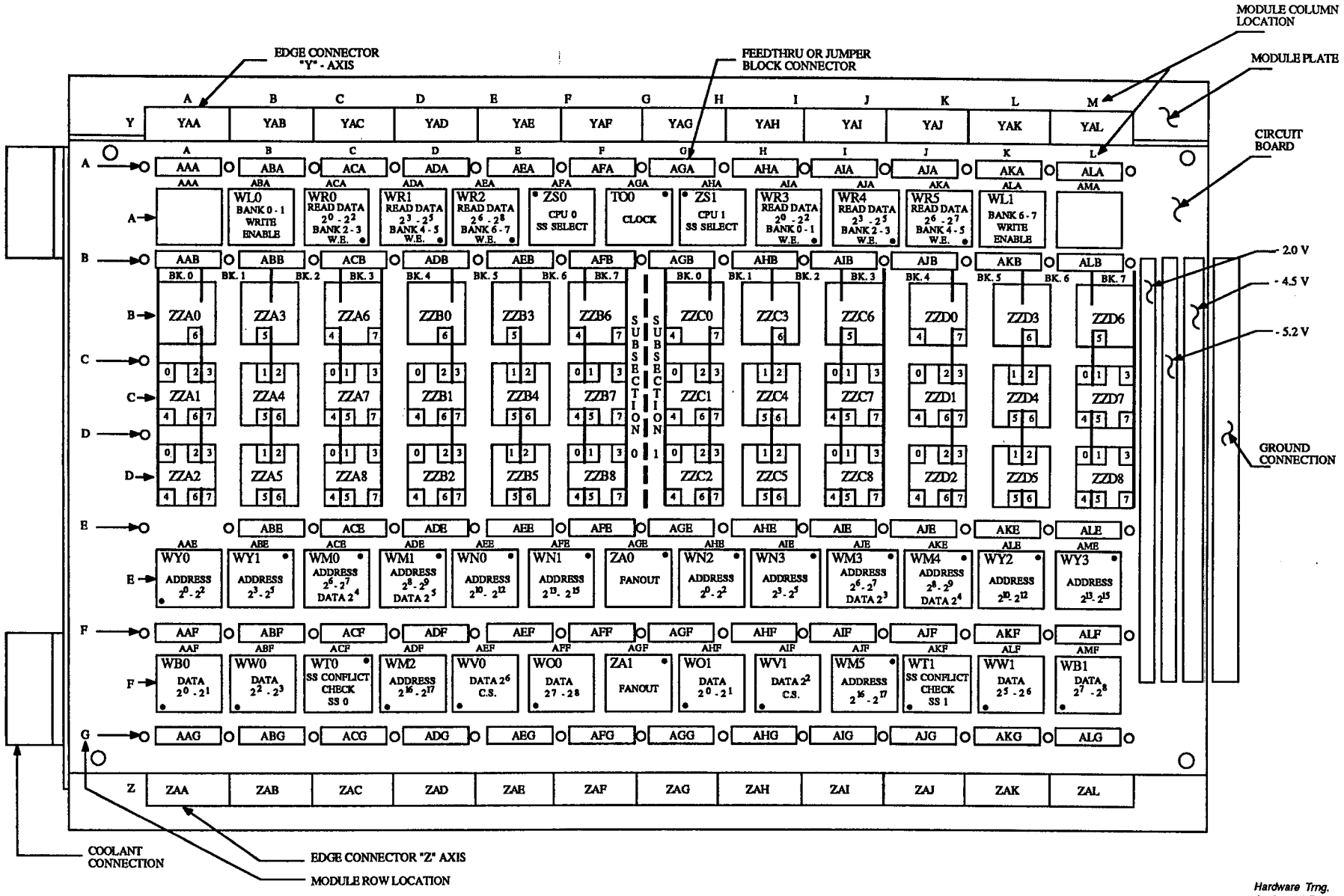
CRAY Y-MP MODULE BIT ASSOCIATION



CRAY Y-MP MODULE/SUBSECTION LAYOUT



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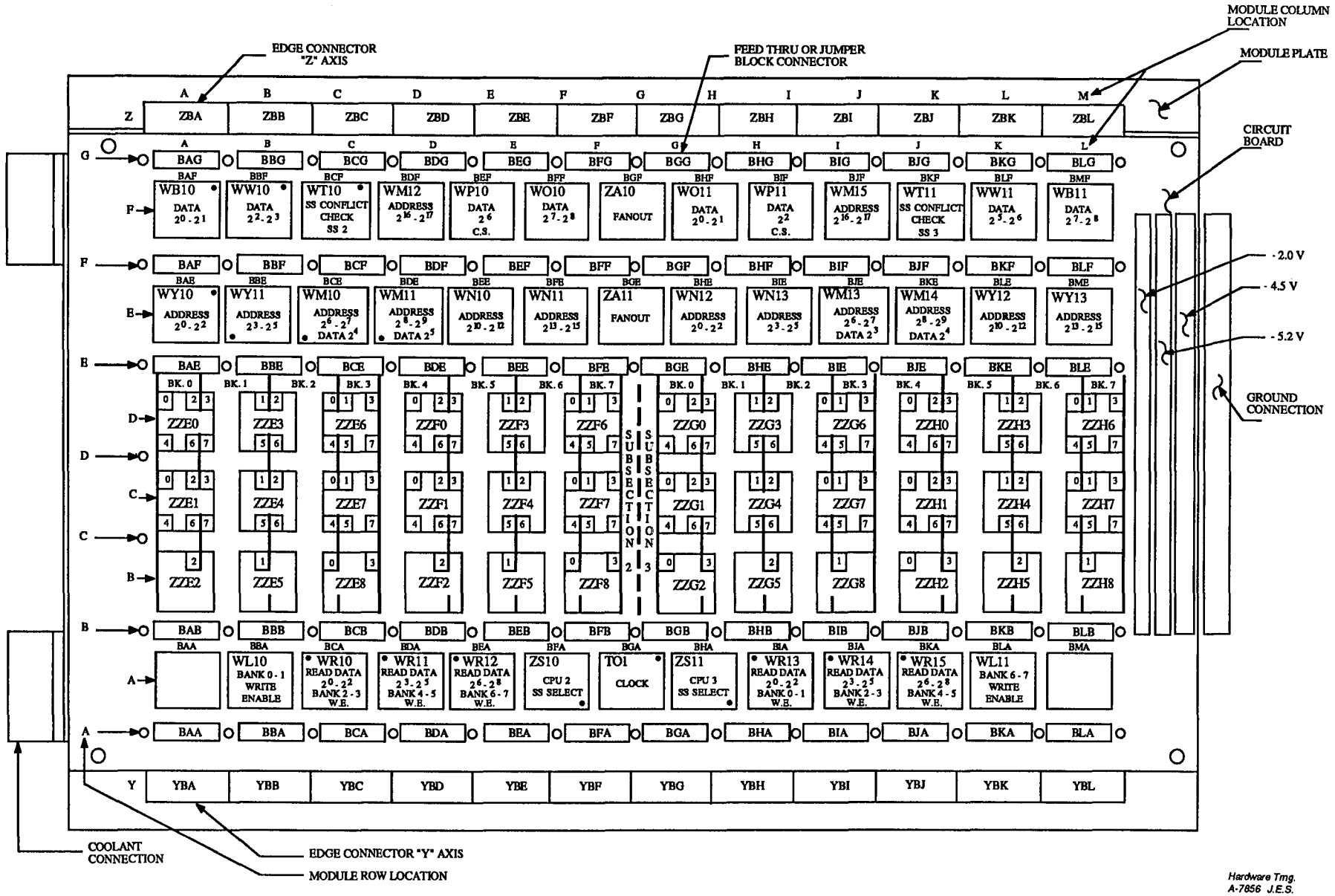
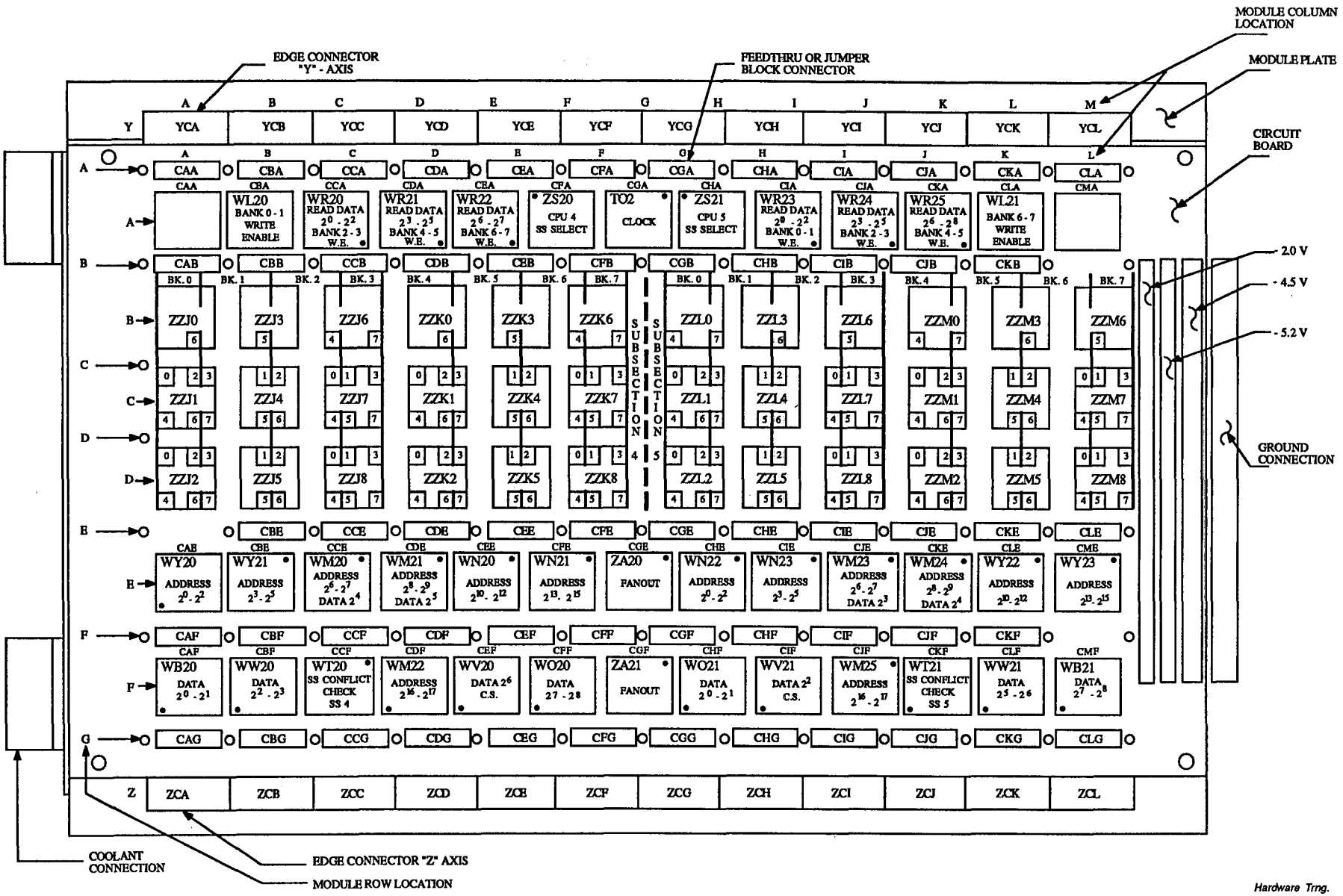
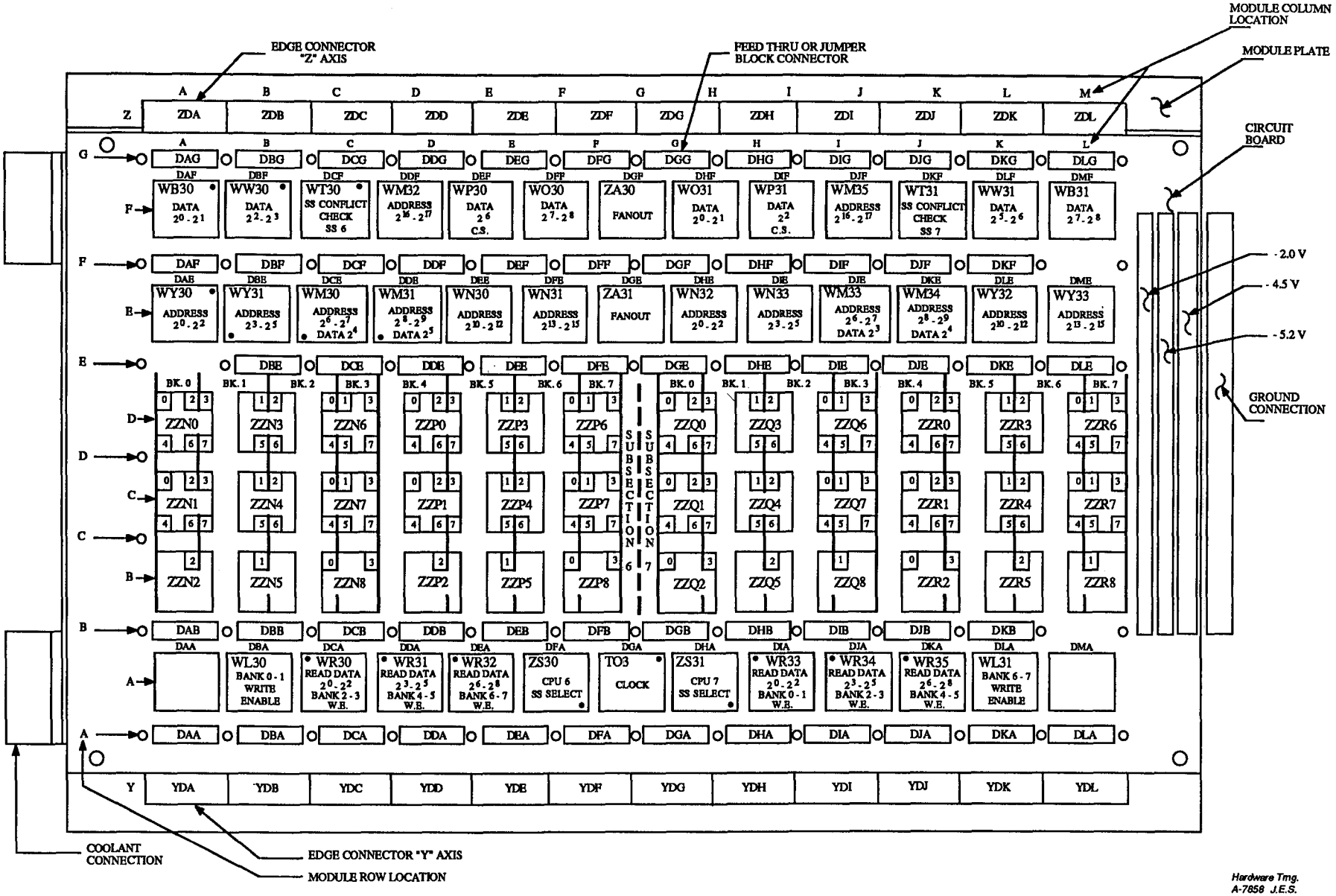
CRAY Y-MP MEMORY MAP
BOARD A



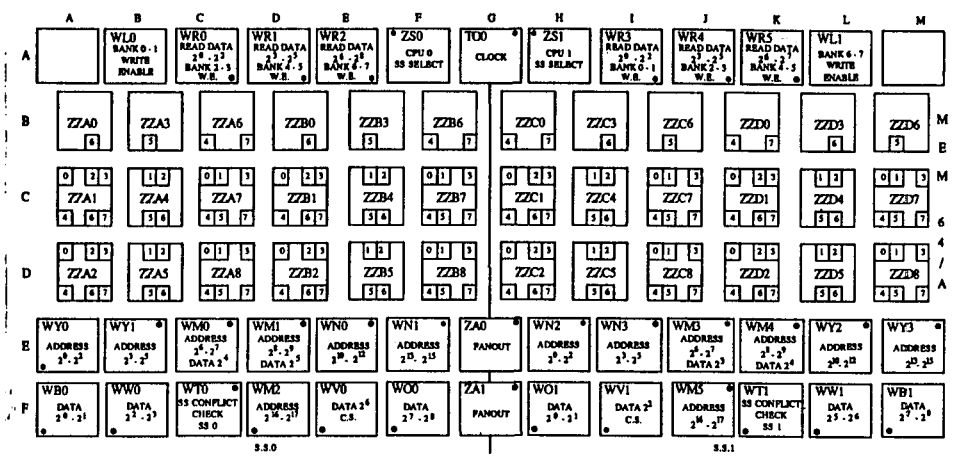
CRAY Y-MP MEMORY MAP
BOARD B

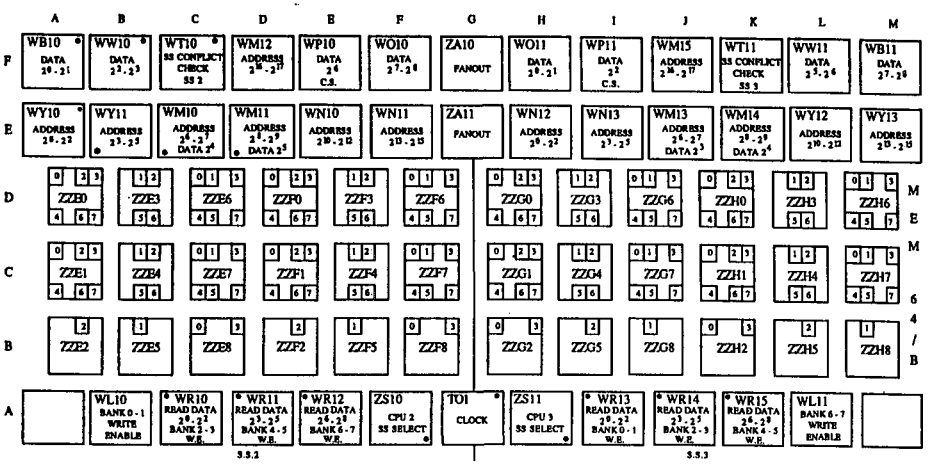


CRAY Y-MP MEMORY MAP
BOARD C



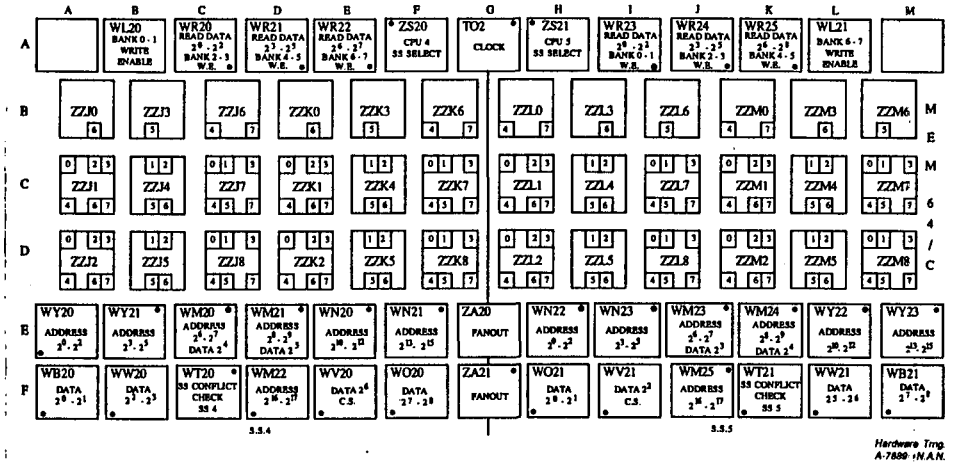
CRAY Y-MP MEMORY MAP
BOARD D

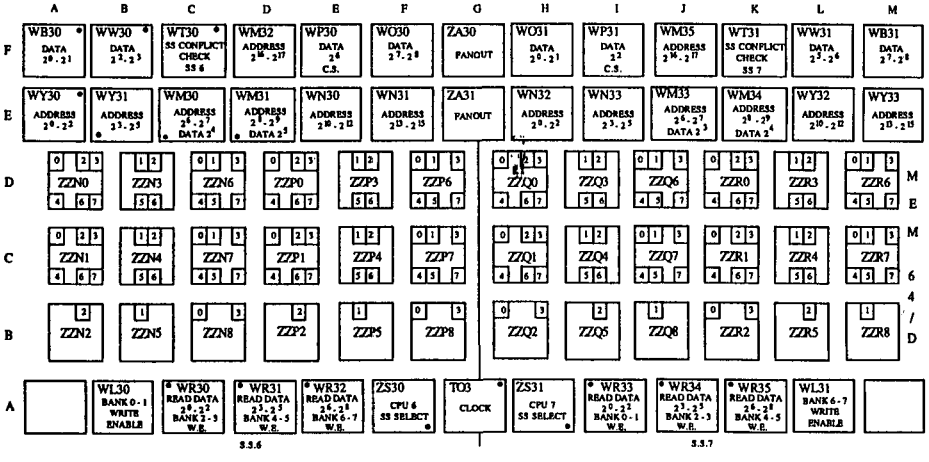




Hardware Trng. A-7887 N.A.N.

Hardware Trng. A-7888 N.A.N.

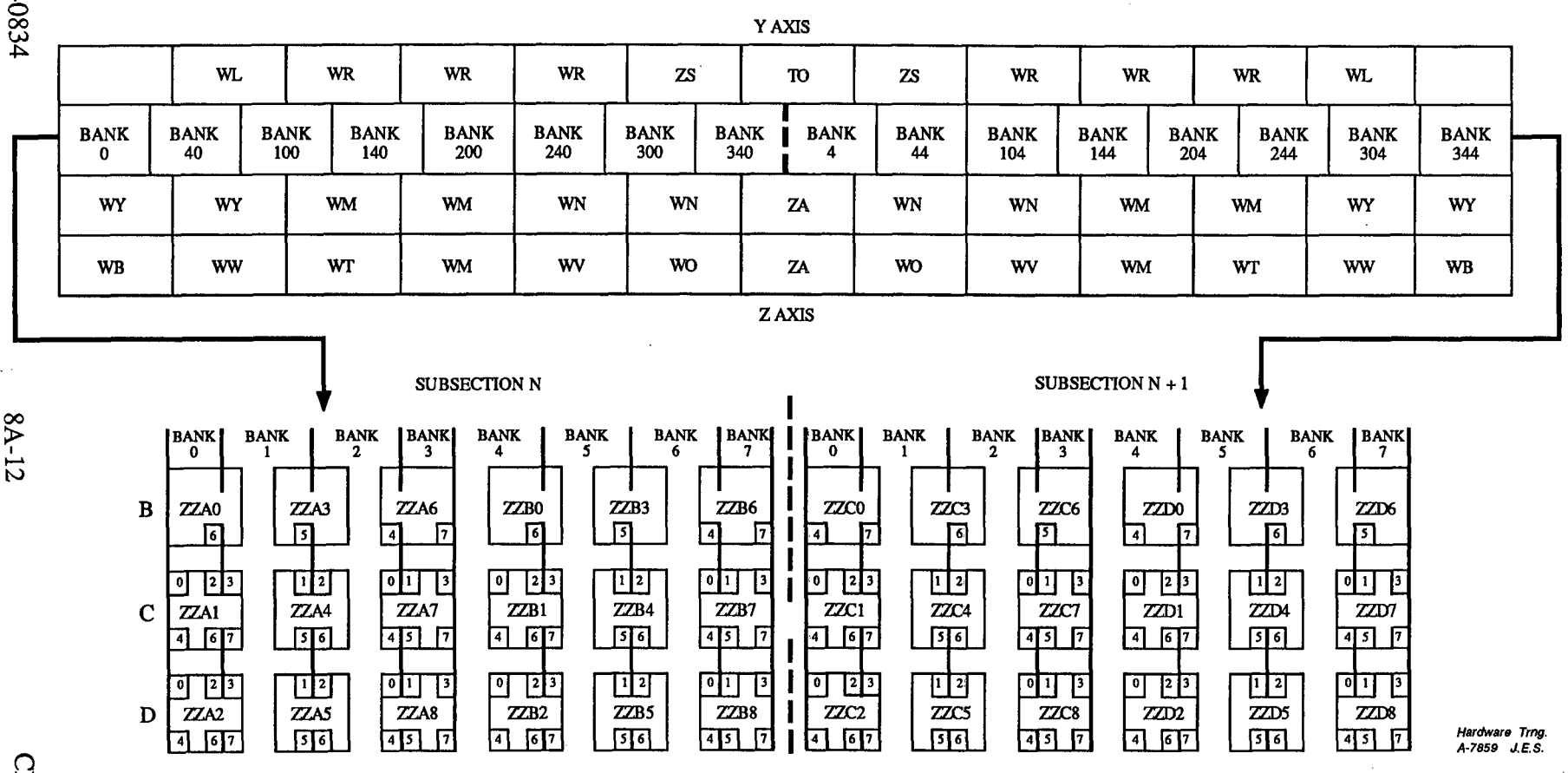




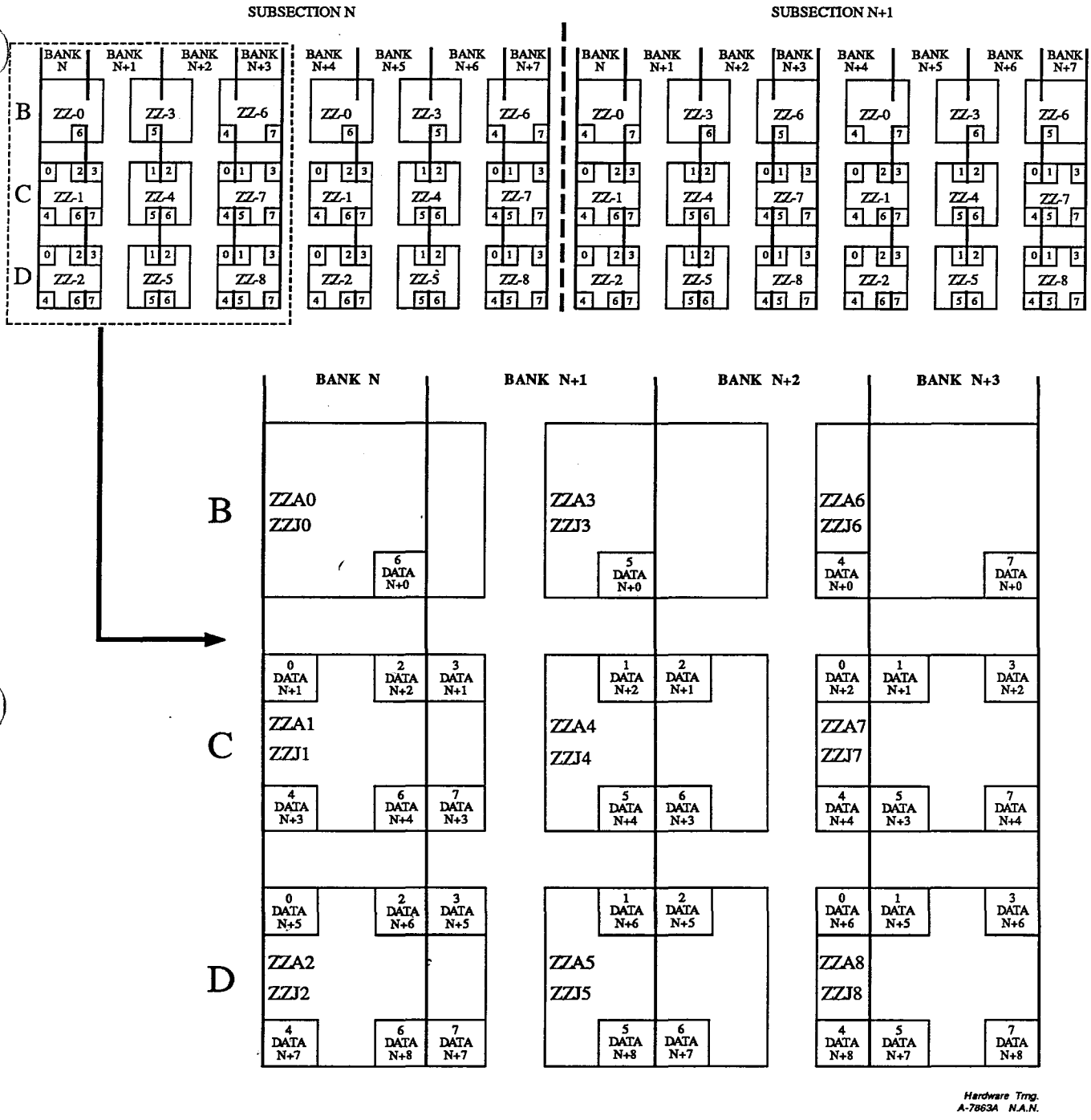
Hardware Trng. A-7889 N.A.N.

Hardware Trng. A-7890 N.A.N.

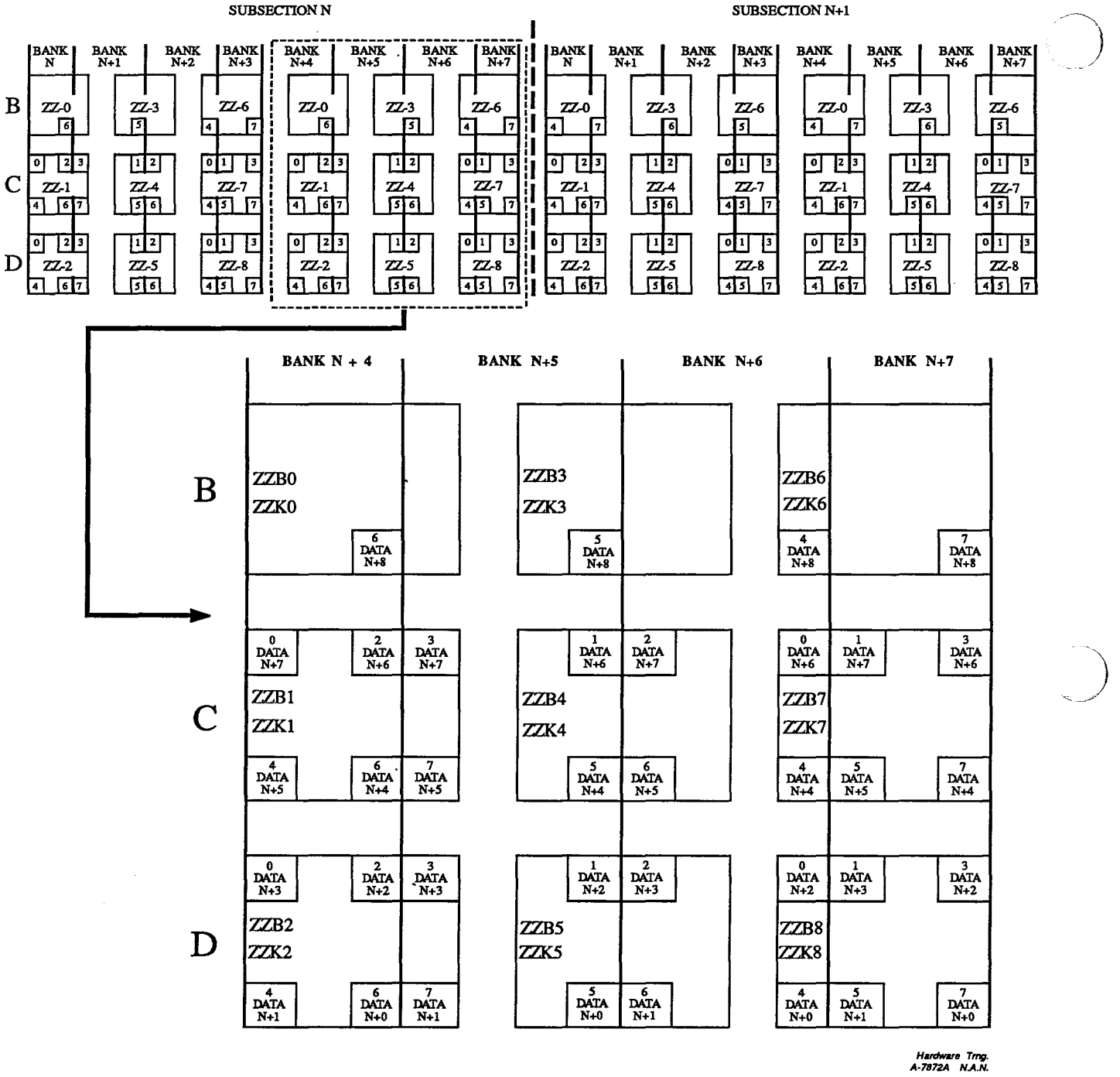
CRAY Y-MP 8/64 MEMORY - 256K x 1



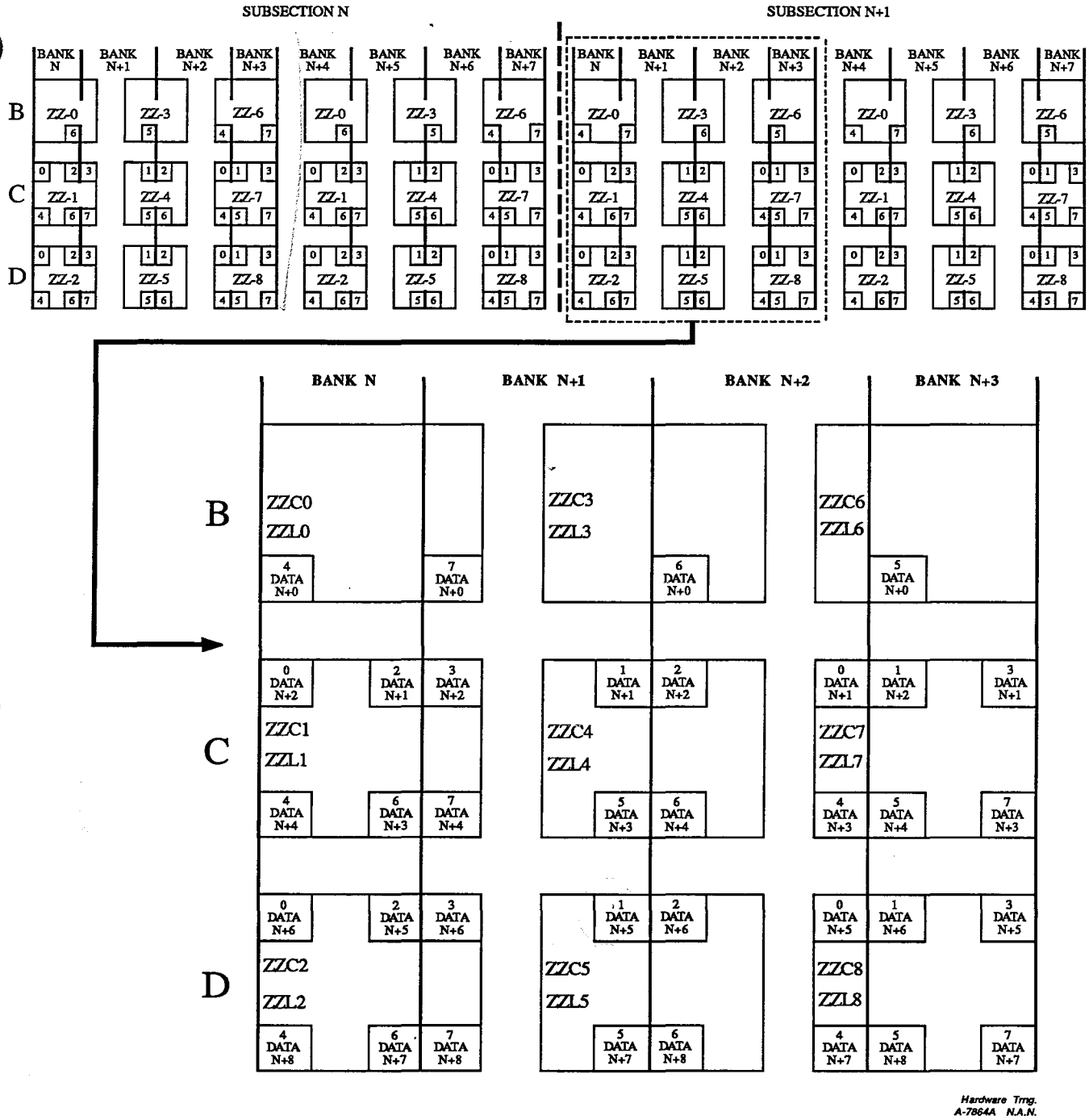
CRAY Y-MP BANK/SUBSECTION LAYOUT



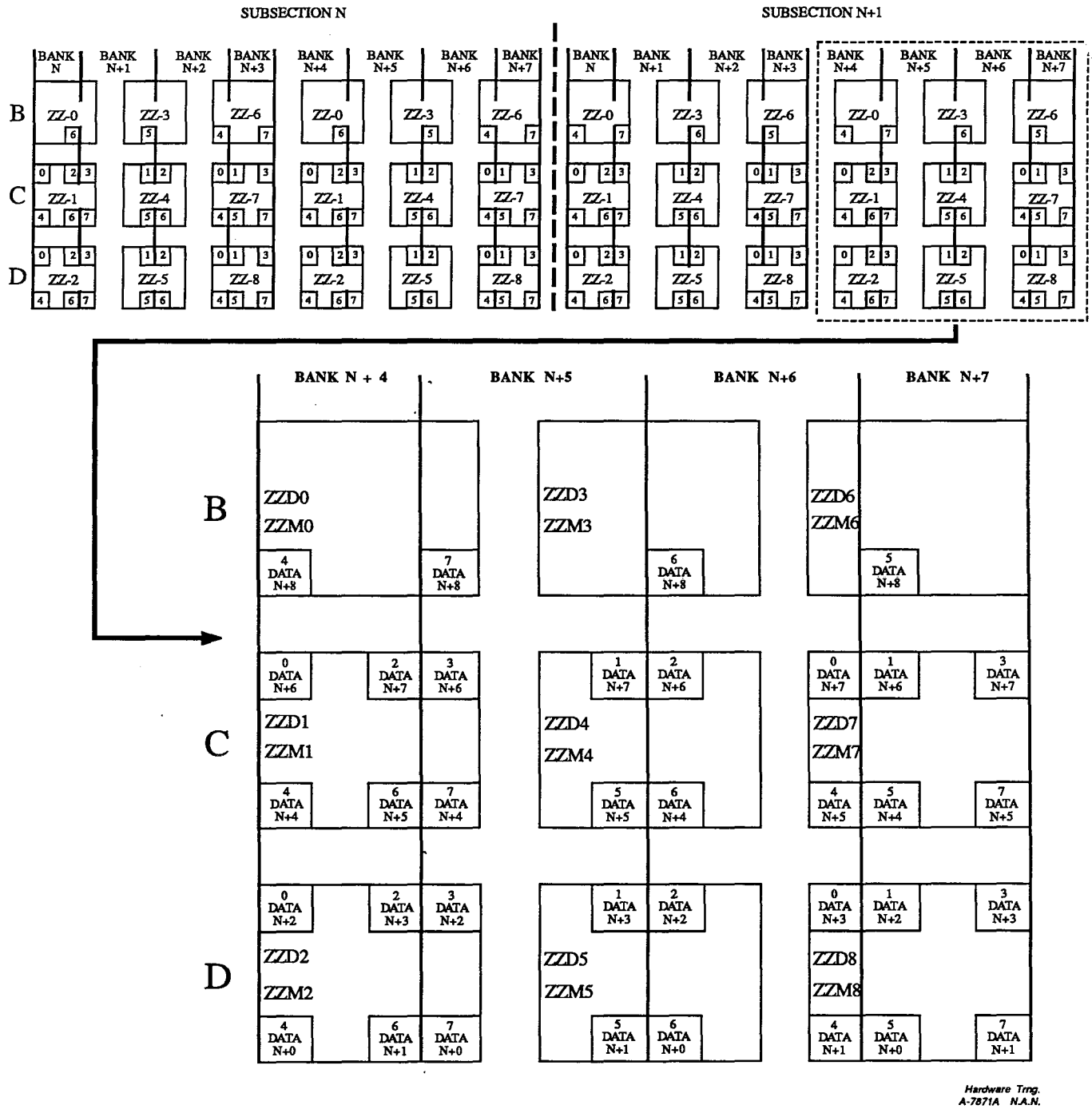
CRAY Y-MP MEMORY BOARD A/C SUBSECTION 0/4
BANKS (N - N + 3)



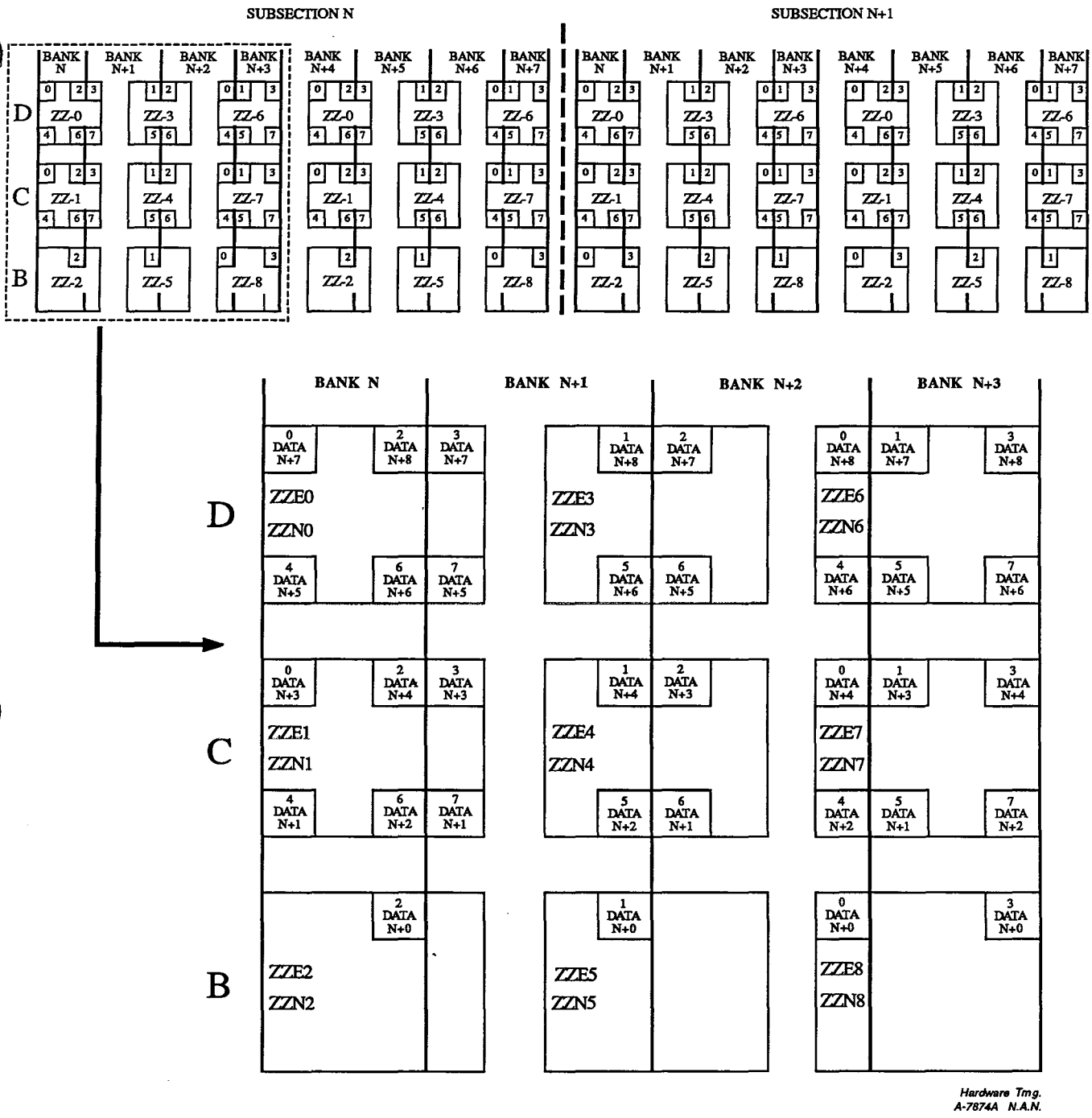
CRAY Y-MP MEMORY BOARD A/C SUBSECTION 0/4
BANKS (N + 4 - N + 7)



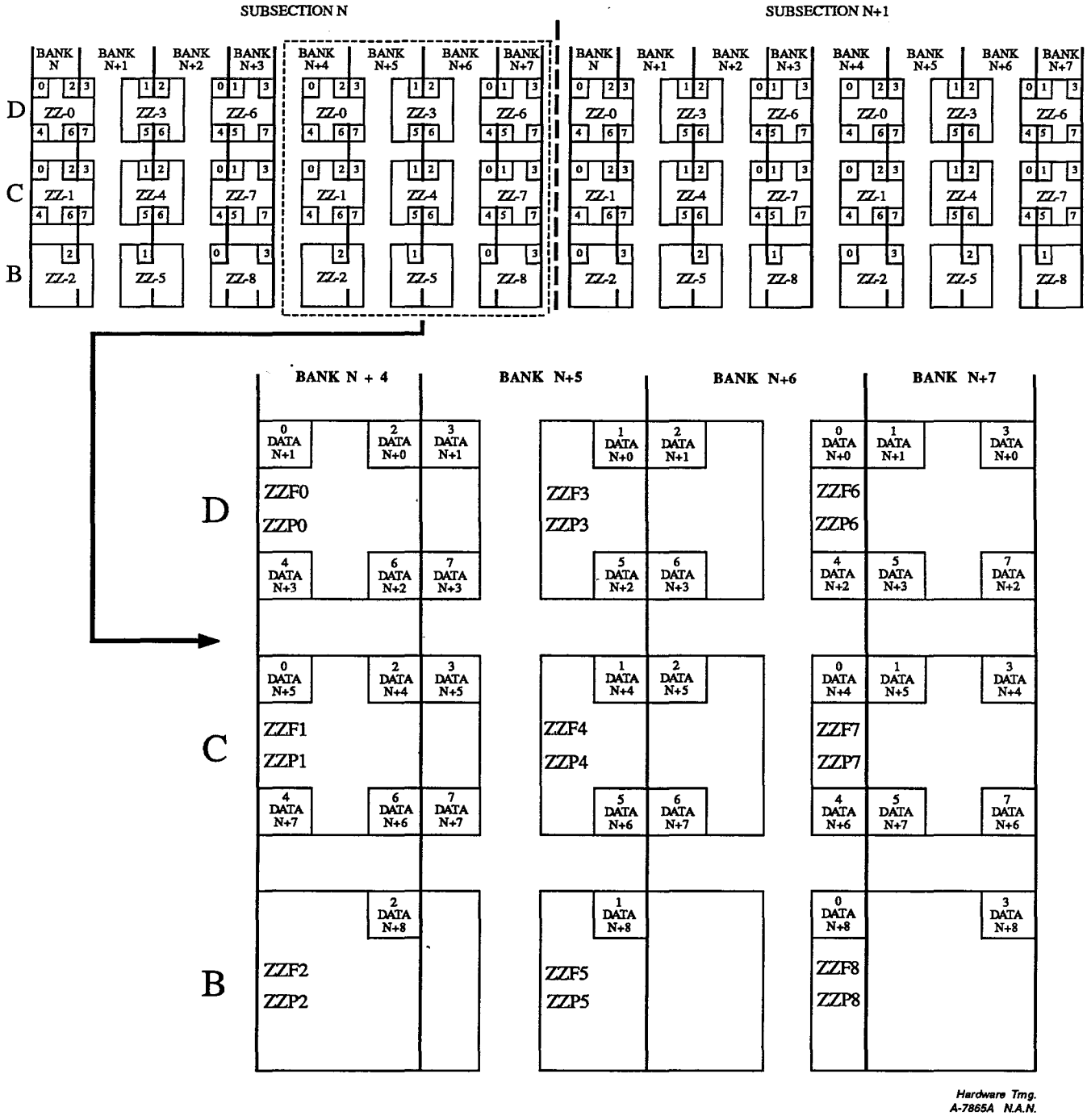
CRAY Y-MP MEMORY BOARD A/C SUBSECTION 1/5
BANKS (N - N + 3)



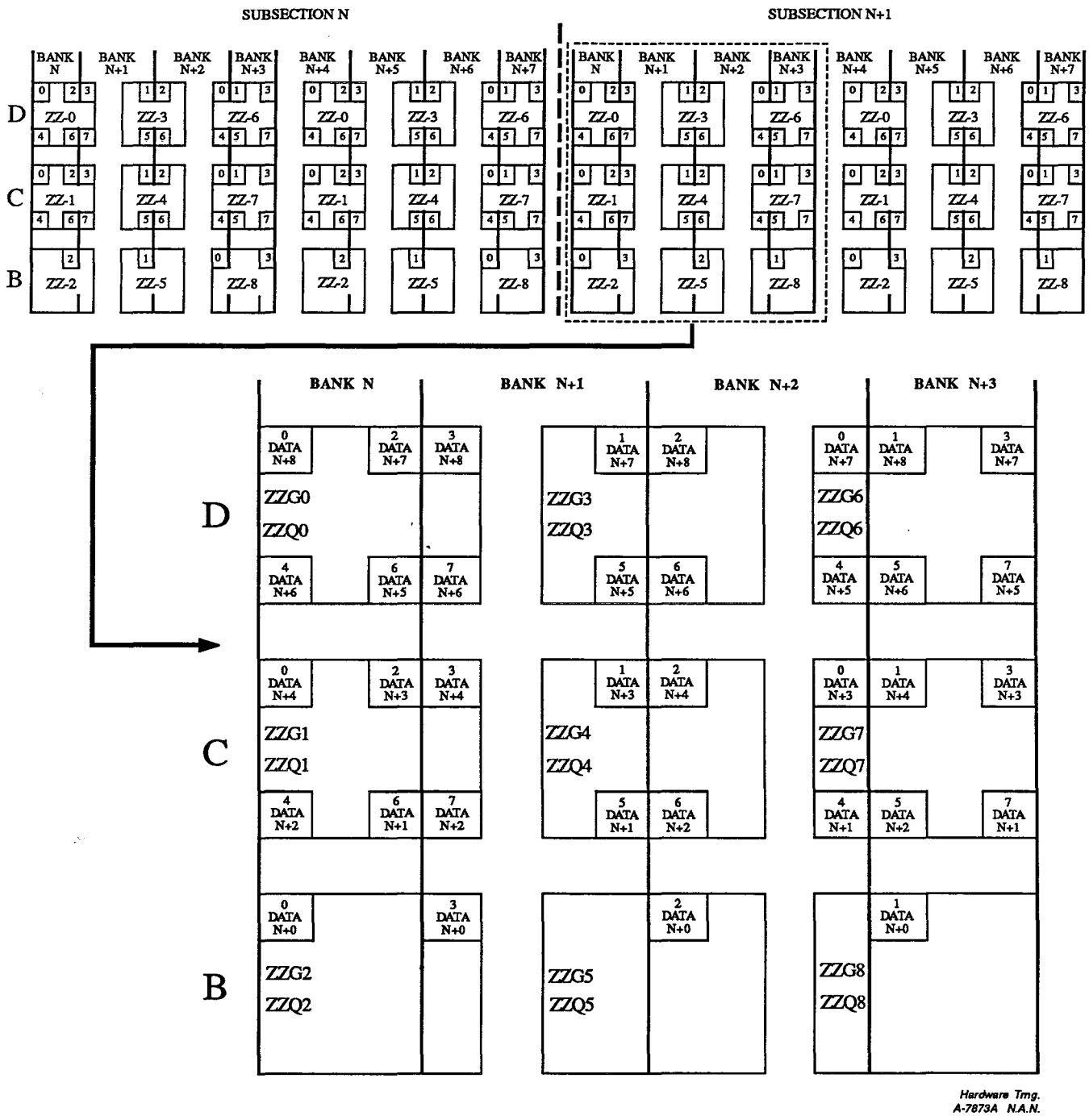
CRAY Y-MP MEMORY BOARD A/C SUBSECTION 1/5
BANKS (N + 4 - N + 7)



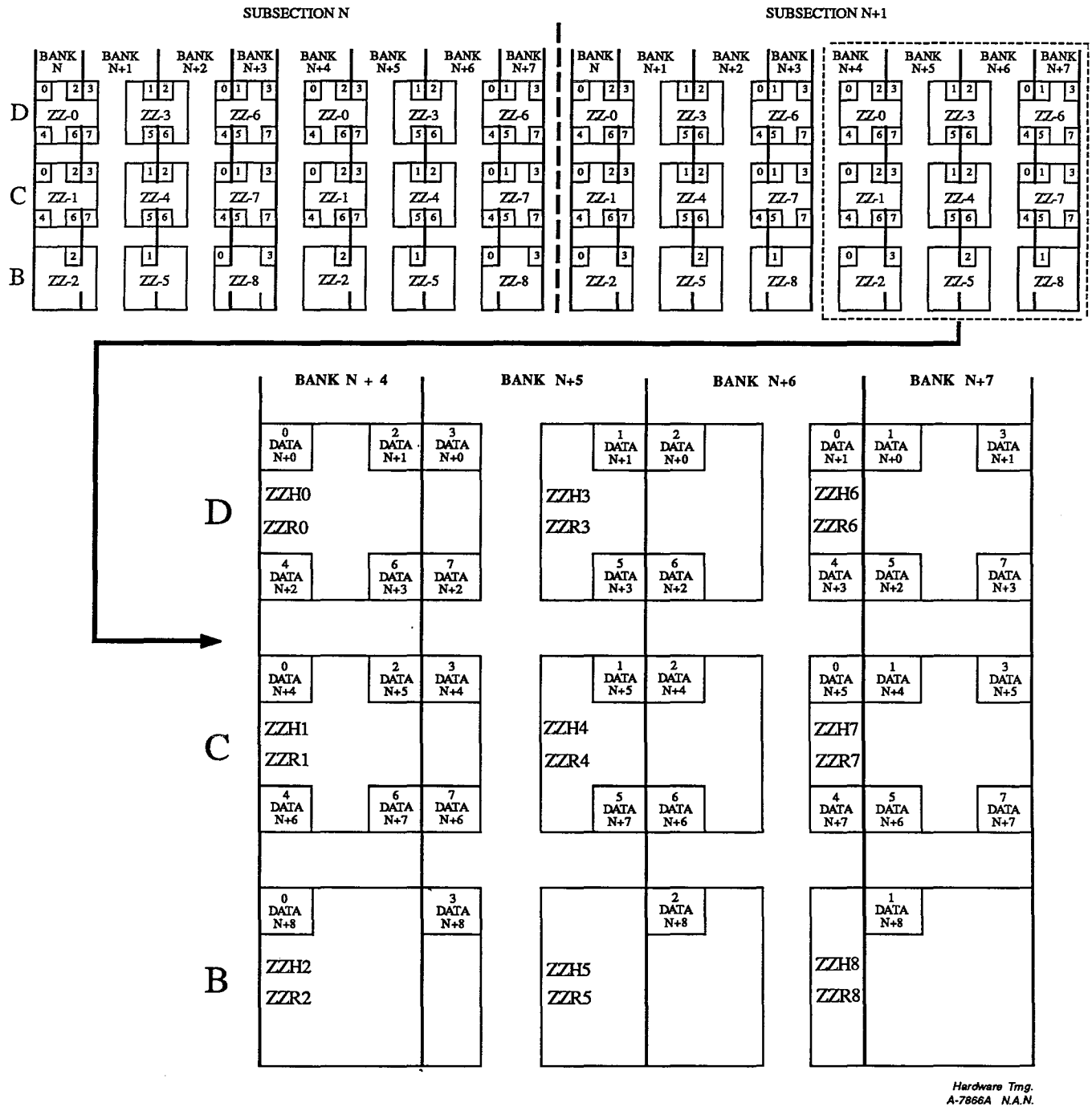
CRAY Y-MP MEMORY BOARD B/D SUBSECTION 2/6
BANKS (N - N + 3)



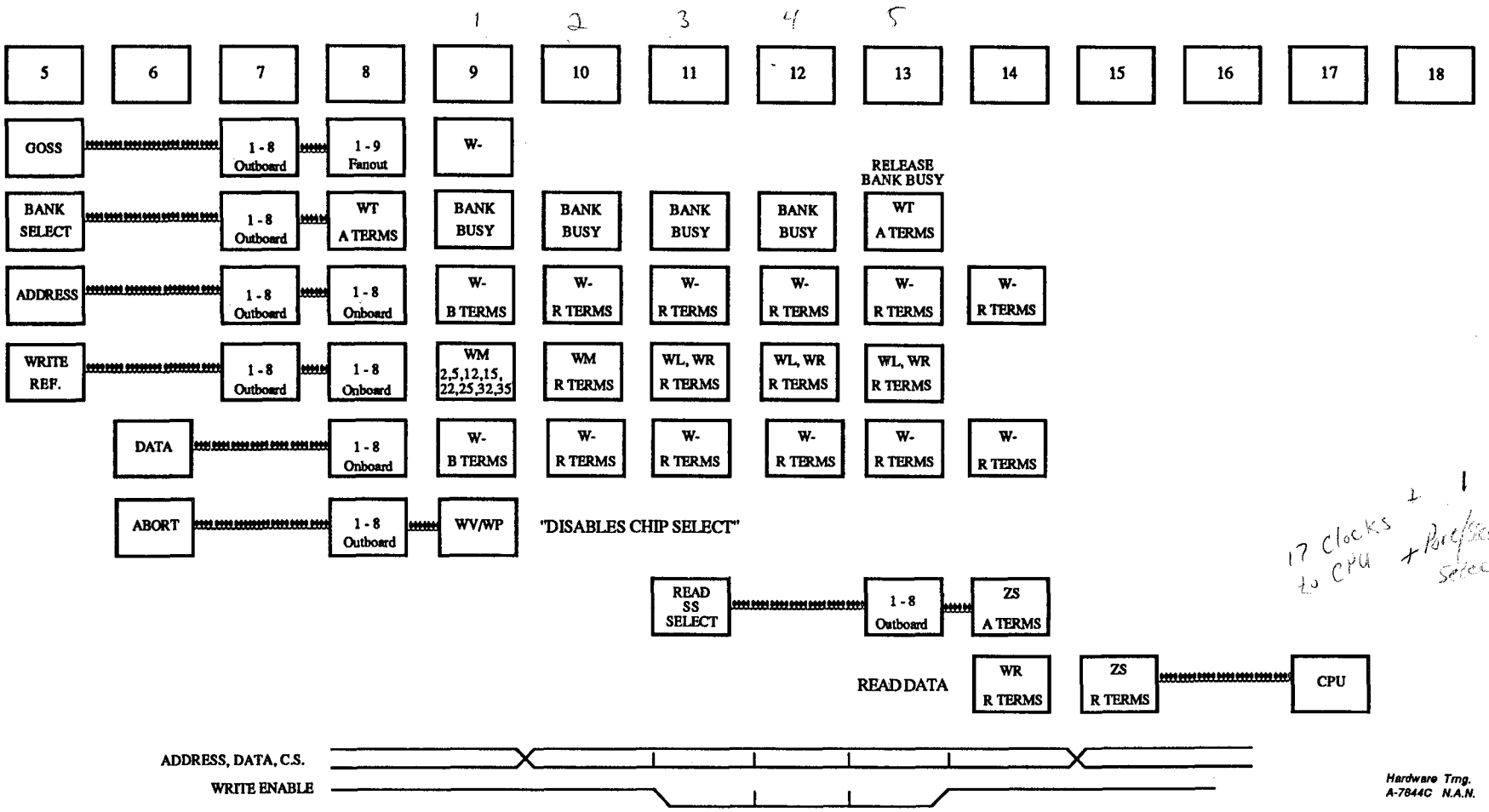
CRAY Y-MP MEMORY BOARD B/D SUBSECTION 2/6
BANKS (N + 4 - N + 7)



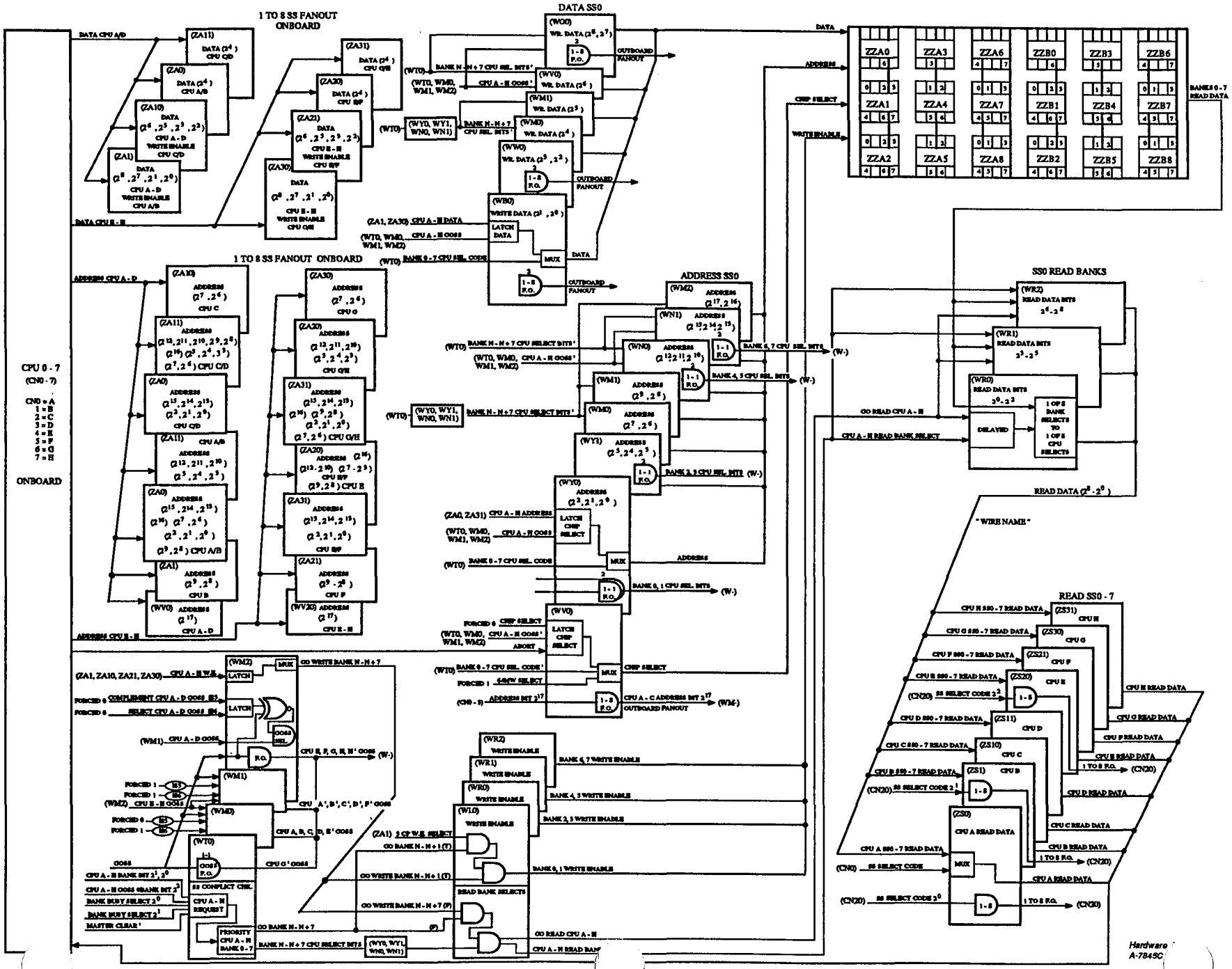
CRAY Y-MP MEMORY BOARD B/D SUBSECTION 3/7
BANKS (N - N + 3)



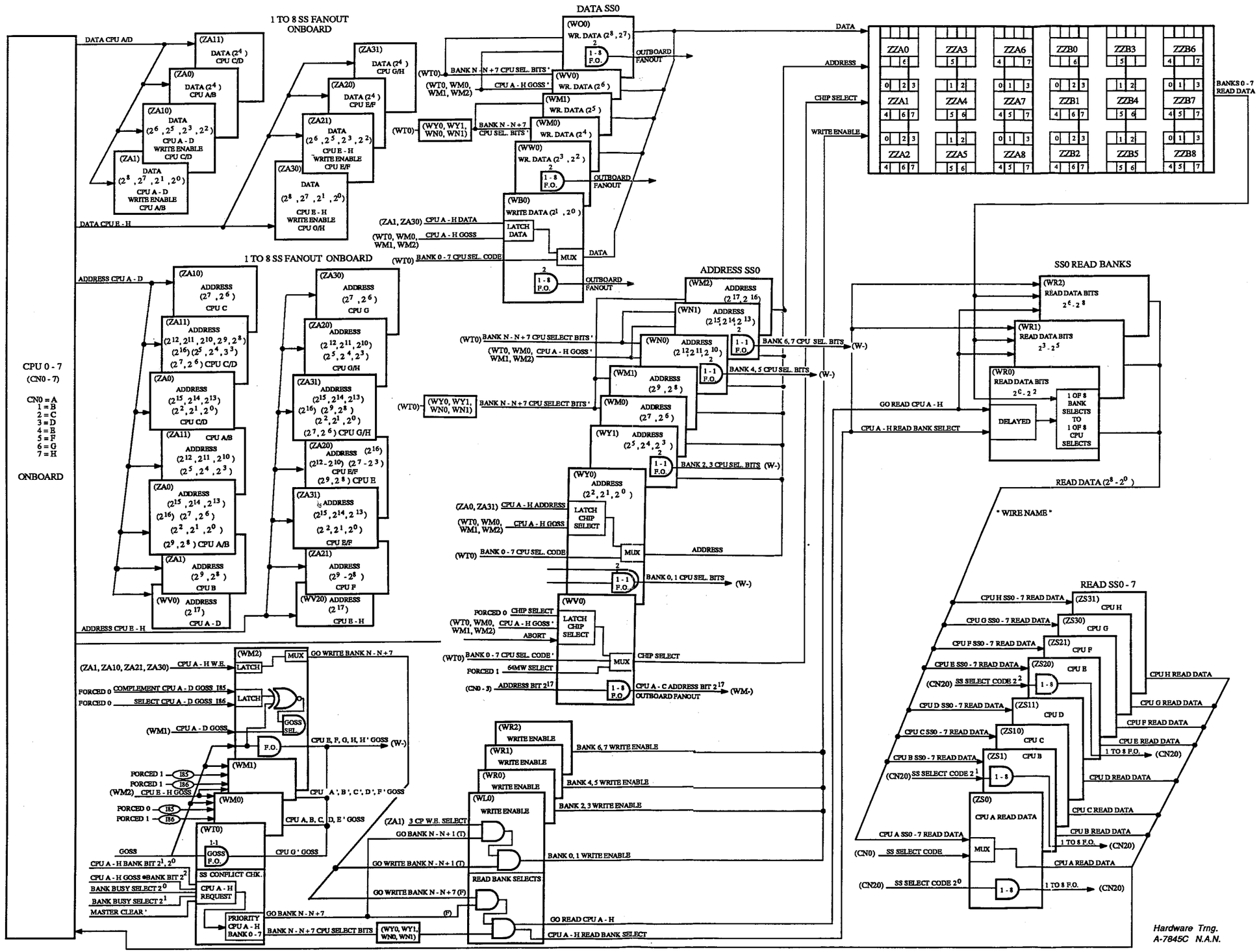
CRAY Y-MP MEMORY BOARD B/D SUBSECTION 3/7
BANKS (N + 4 - N + 7)



CRAY Y-MP MEMORY TIMING (256K x 1)



CRAY Y-MP MEMORY (64MW) BLOCK DIAGRAM (256K x 1) SUBSECTION 0 CPU A - H



CRAY Y-MP MEMORY (64MW) BLOCK DIAGRAM (256K x 1) SUBSECTION 0 CPU A - H

WRITE DATA SELECT CPU 0 - 7

DATA	SS0	SS1	SS2	SS3	SS4	SS5	SS6	SS7
N + 0	WB0	WO1	WB10	WO11	WB20	WO21	WB30	WO31
N + 1	WB0	WO1	WB10	WO11	WB20	WO21	WB30	WO31
N + 2	WW0	WV1	WW10	WP11	WW20	WV21	WW30	WP31
N + 3	WW0	WM3	WW10	WM13	WW20	WM23	WW30	WM33
N + 4	WM0	WM4	WM10	WM14	WM20	WM24	WM30	WM34
N + 5	WM1	WW1	WM11	WW11	WM21	WW21	WM31	WW31
N + 6	WV0	WW1	WP10	WW11	WV20	WW21	WP30	WW31
N + 7	WO0	WB1	WO10	WB11	WO20	WB21	WO30	WB31
N + 8	WO0	WB1	WO10	WB11	WO20	WB21	WO30	WB31

ADDRESS SELECT CPU 0 - 7

ADDRS.	SS0	SS1	SS2	SS3	SS4	SS5	SS6	SS7
2^0	WY0	WN2	WY10	WN12	WY20	WN22	WY30	WN32
2^1	WY0	WN2	WY10	WN12	WY20	WN22	WY30	WN32
2^2	WY0	WN2	WY10	WN12	WY20	WN22	WY30	WN32
2^3	WY1	WN3	WY11	WN13	WY21	WN23	WY31	WN33
2^4	WY1	WN3	WY11	WN13	WY21	WN23	WY31	WN33
2^5	WY1	WN3	WY11	WN13	WY21	WN23	WY31	WN33
2^6	WM0	WM3	WM10	WM13	WM20	WM23	WM30	WM33
2^7	WM0	WM3	WM10	WM13	WM20	WM23	WM30	WM33
2^8	WM1	WM4	WM11	WM14	WM21	WM24	WM31	WM34
2^9	WM1	WM4	WM11	WM14	WM21	WM24	WM31	WM34
2^{10}	WN0	WY2	WN10	WY12	WN20	WY22	WN30	WY32
2^{11}	WN0	WY2	WN10	WY12	WN20	WY22	WN30	WY32
2^{12}	WN0	WY2	WN10	WY12	WN20	WY22	WN30	WY32
2^{13}	WN1	WY3	WN11	WY13	WN21	WY23	WN31	WY33
2^{14}	WN1	WY3	WN11	WY13	WN21	WY23	WN31	WY33
2^{15}	WN1	WY3	WN11	WY13	WN21	WY23	WN31	WY33
2^{16}	WM2	WM5	WM12	WM15	WM22	WM25	WM32	WM35
2^{17}	WM2	WM5	WM12	WM15	WM22	WM25	WM32	WM35

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CRAY Y-MP SUBSECTION 0 - 7 CROSS REFERENCE

SUBSECTION CONTROL

CPU 0 - 7

CONFLICT CHECKS	SS0	SS1	SS2	SS3	SS4	SS5	SS6	SS7
BANKS 0 - 7	WT0	WT1	WT10	WT11	WT20	WT21	WT30	WT31

READ DATA (WRs)

CPU 0 - 7

	SS0	SS1	SS2	SS3	SS4	SS5	SS6	SS7
DATA $2^2, 2^1, 2^0$	WR0	WR3	WR10	WR13	WR20	WR23	WR30	WR33
DATA $2^5, 2^4, 2^3$	WR1	WR4	WR11	WR14	WR21	WR24	WR31	WR34
DATA $2^8, 2^7, 2^6$	WR2	WR5	WR12	WR15	WR22	WR25	WR32	WR35

GO SUBSECTION (GOSS)

CPU A - H

CPU	SS0	SS1	SS2	SS3	SS4	SS5	SS6	SS7
A	WM0 WM1	WM3 WM4	WM12	WM15	WM20 WM21	WM23 WM24	WM32	WM35
B	WM0 WM1	WM3 WM4	WM12 WT10	WM15 WT11	WM20 WM21	WM23 WM24	WM32 WT30	WM35 WT31
C	WM0 WM1	WM3 WM4	WM12 WM11	WM15 WM14	WM20 WM21	WM23 WM24	WM32 WM31	WM35 WM34
D	WM0 WM1	WM3 WM4	WM12 WM10	WM15 WM13	WM20 WM21	WM23 WM24	WM32 WM30	WM35 WM33
E	WM2 WM0	WM5 WM3	WM10 WM11	WM13 WM14	WM22 WM20	WM25 WM23	WM30 WM31	WM33 WM34
F	WM2 WM1	WM5 WM4	WM10 WM11	WM13 WM14	WM22 WM21	WM25 WM24	WM30 WM31	WM33 WM34
G	WM2 WT0	WM5 WT1	WM10 WM11	WM13 WM14	WM22 WT20	WM25 WT21	WM30 WM31	WM33 WM34
H	WM2	WM5	WM10 WM11	WM13 WM14	WM22	WM25	WM30 WM31	WM33 WM34

SUBSECTION CHIP SELECT/ABORT

CPU 0 - 7

CHIP SELECT	SS0	SS1	SS2	SS3	SS4	SS5	SS6	SS7
C.S.	WV0	WV1	WP10	WP11	WV20	WV21	WP30	WP31

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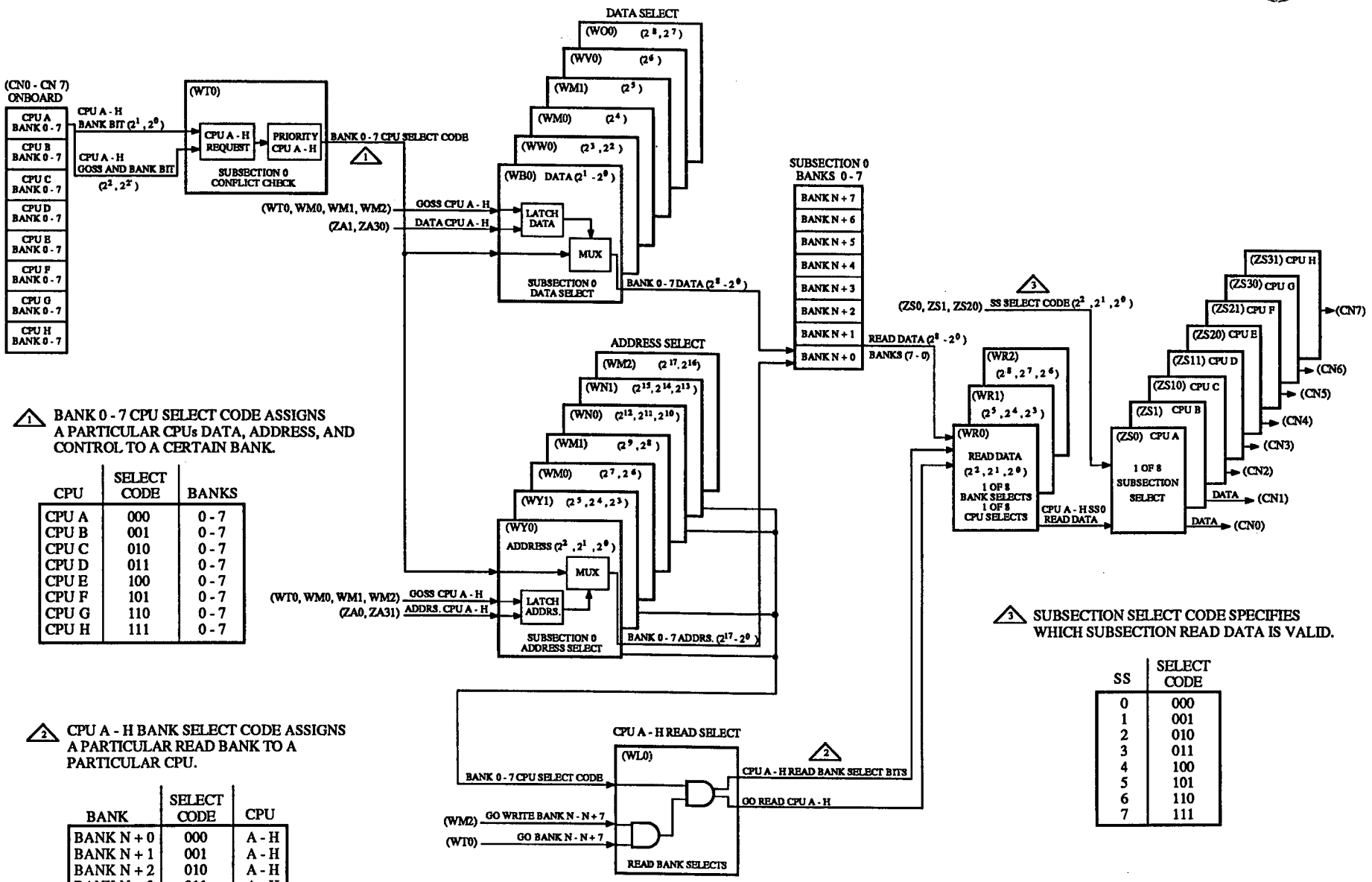
CRAY Y-MP
SUBSECTION 0 - 7 CROSS REFERENCE



1 BANK 0 - 7 CPU SELECT CODE ASSIGNS A PARTICULAR CPUs DATA, ADDRESS, AND CONTROL TO A CERTAIN BANK.

CPU	SELECT CODE	BANKS
CPU A	000	0 - 7
CPU B	001	0 - 7
CPU C	010	0 - 7
CPU D	011	0 - 7
CPU E	100	0 - 7
CPU F	101	0 - 7
CPU G	110	0 - 7
CPU H	111	0 - 7

2 CPU A - H BANK SELECT CODE ASSIGNS A PARTICULAR READ BANK TO A PARTICULAR CPU.

BANK	SELECT CODE	CPU
BANK N + 0	000	A - H
BANK N + 1	001	A - H
BANK N + 2	010	A - H
BANK N + 3	011	A - H
BANK N + 4	100	A - H
BANK N + 5	101	A - H
BANK N + 6	110	A - H
BANK N + 7	111	A - H

3 SUBSECTION SELECT CODE SPECIFIES WHICH SUBSECTION READ DATA IS VALID.

SS	SELECT CODE
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

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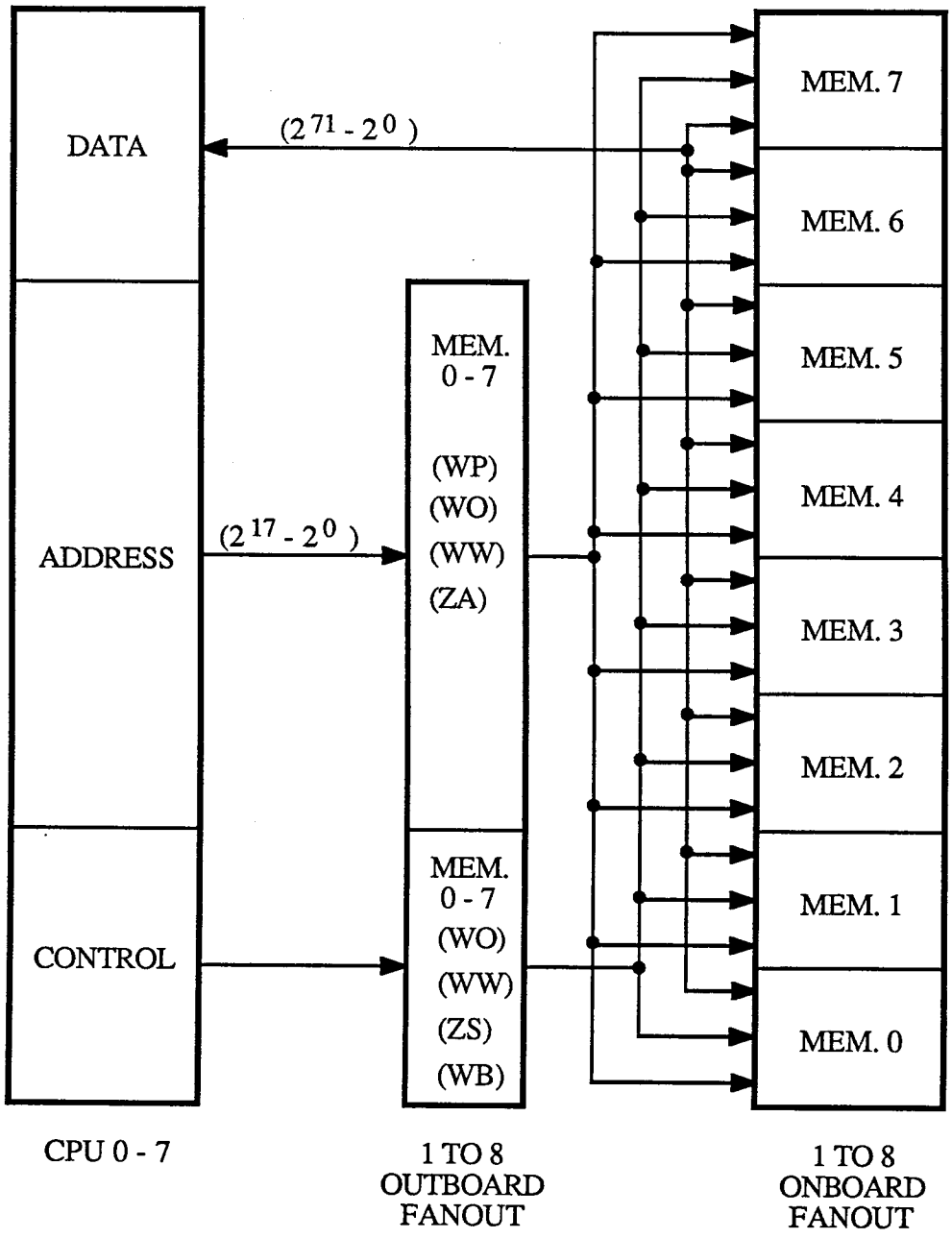
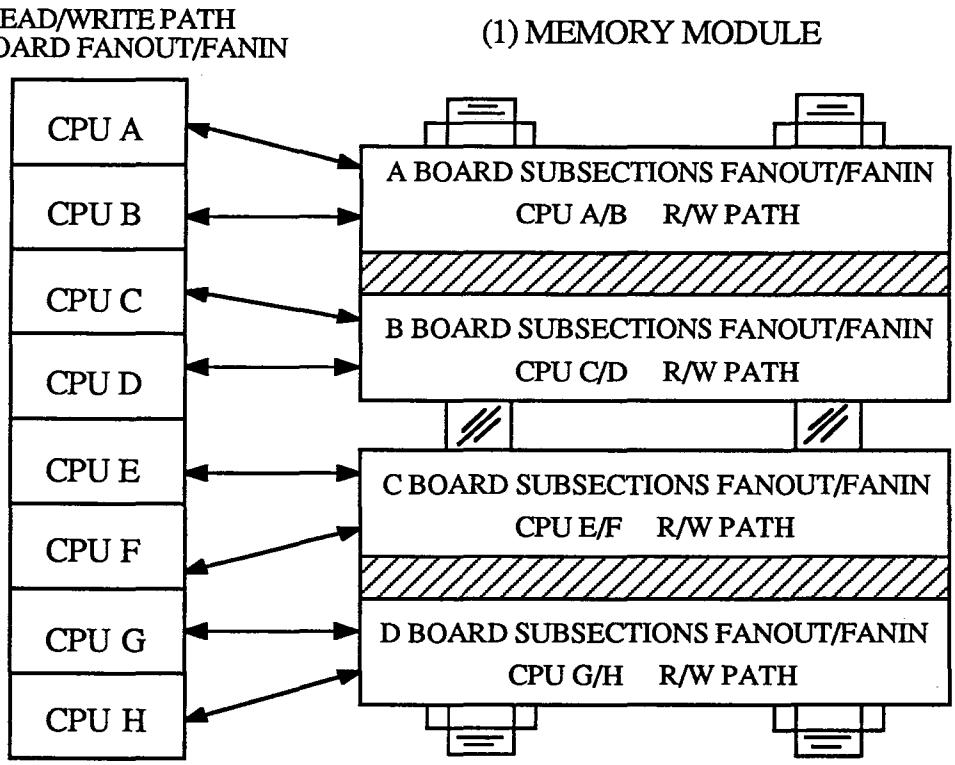
CRAY Y-MP MEMORY CPU SELECT CODES SUBSECTION 0

CRAY Y-MP Read Bank Selects Cross Reference

CPU A - H	SS0	SS1	SS2	SS3	SS4	SS5	SS6	SS7
CPU A	WL0	WL1	WL10	WL11	WL20	WL21	WL30	WL31
CPU B	WL0	WL1	WL10	WL11	WL20	WL21	WL30	WL31
CPU C	WL0	WL1	WL10	WL11	WL20	WL21	WL30	WL31
CPU D	WL0	WL1	WL10	WL11	WL20	WL21	WL30	WL31
CPU E	WL0	WL1	WL10	WL11	WL20	WL21	WL30	WL31
CPU F	WL0	WL1	WL10	WL11	WL20	WL21	WL30	WL31
CPU G	WL0	WL1	WL10	WL11	WL20	WL21	WL30	WL31
CPU H	WL0	WL1	WL10	WL11	WL20	WL21	WL30	WL31



CRAY Y-MP MEMORY MODULE OUTBOARD FANOUT



CPU (A - H) PRIORITY SECTION 0

SUBSECTION	CPU NUMBER	0	1	2	3	7	6	5	4
ACCESSED	CPU LETTER	A	B	C	D	E	F	G	H
0	(WT-)	I0-	I1-	I2-	I3-	I4-	I5-	I6-	I7-
1	(WT-)	I0-	I1-	I2-	I3-	I4-	I5-	I6-	I7-
2	(WT-)	I7-	I6-	I5-	I4-	I3-	I2-	I1-	I0-
3	(WT-)	I7-	I6-	I5-	I4-	I3-	I2-	I1-	I0-
4	(WT-)	I0-	I1-	I2-	I3-	I4-	I5-	I6-	I7-
5	(WT-)	I0-	I1-	I2-	I3-	I4-	I5-	I6-	I7-
6	(WT-)	I7-	I6-	I5-	I4-	I3-	I2-	I1-	I0-
7	(WT-)	I7-	I6-	I5-	I4-	I3-	I2-	I1-	I0-

A - highest

H - lowest

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CRAY Y-MP MEMORY FANOUT AND PRIORITY

LOC.	1	MEM. 0	1 - 8	BANK BUSY 2^0 (MEM.)
	2	1	1 - 8	BANK BUSY 2^1 (MEM.)
	3	2	1 - 8	I/O M.C.
	4	3	1 - 8	3 CP W.E.
	5	4	1 - 8	
	6	5	1 - 8	
	7	6	1 - 8	
	8	7	1 - 3	I/O M.C.
LOC.	9	MEM. 10	1 - 8	BANK BUSY 2^0 (MEM.)
	10	11	1 - 8	BANK BUSY 2^1 (MEM.)
	11	12	1 - 8	I/O M.C.
	12	13	1 - 8	3 CP W.E.
	13	14	1 - 8	CPU M.C.
	14	15	1 - 8	I/O M.C.
	15	16	1 - 8	
	16	17	1 - 8	
LOC.	17	CPU 0		
	18	1		
	19	2		
	20	3		
	21	4		
	22	5		
	23	6		
	24	7		
LOC.	25	MEM. 20	1 - 8	BANK BUSY 2^0 (MEM.)
	26	21	1 - 8	BANK BUSY 2^1 (MEM.)
	27	22	1 - 8	I/O M.C.
	28	23	1 - 8	3 CP W.E.
	29	24	1 - 8	
	30	25	1 - 8	
	31	26	1 - 2	I/O M.C.
	32	27	1 - 8	
LOC.	33	MEM. 30	1 - 8	BANK BUSY 2^0 (MEM.)
	34	31	1 - 8	BANK BUSY 2^1 (MEM.)
	35	32	1 - 8	I/O M.C.
	36	33	1 - 8	3 CP W.E.
	37	34	1 - 8	
	38	35	1 - 8	BANK BUSY BIT 0 (5 - 8) CPU
	39	36	1 - 8	BANK BUSY BIT 1 (5 - 8) CPU
	40	37	1 - 8	BANK BUSY SEL. (4 CP) CPU
	41	CLOCK		

A-7785

CRAY Y-MP 8/32 MODULE LOCATION

ADDRESS BIT	ADDRESS ONBOARD FANOUT							
	CPU A	CPU B	CPU C	CPU D	CPU E	CPU F	CPU G	CPU H
2^0	ZA0 R27	ZA0 R24	ZA0 R21	ZA0 R18	ZA31 R11	ZA31 R8	ZA31 R5	ZA31 R2
2^1	ZA0 R26	ZA0 R23	ZA0 R20	ZA0 R17	ZA31 R10	ZA31 R7	ZA31 R4	ZA31 R1
2^2	ZA0 R25	ZA0 R22	ZA0 R19	ZA0 R16	ZA31 R9	ZA31 R6	ZA31 R3	ZA31 R0
2^3	ZA11 R11	ZA11 R8	ZA11 R5	ZA11 R2	ZA20 R27	ZA20 R24	ZA20 R21	ZA20 R18
2^4	ZA11 R10	ZA11 R7	ZA11 R4	ZA11 R1	ZA20 R26	ZA20 R23	ZA20 R20	ZA20 R17
2^5	ZA11 R9	ZA11 R6	ZA11 R3	ZA11 R0	ZA20 R25	ZA20 R22	ZA20 R19	ZA20 R16
2^6	ZA0 R28	ZA0 R30	ZA10 R32	ZA11 R32	ZA20 R28	ZA20 R30	ZA30 R32	ZA31 R32
2^7	ZA0 R29	ZA0 R31	ZA10 R33	ZA11 R33	ZA20 R29	ZA20 R31	ZA30 R33	ZA31 R33
2^8	ZA0 R32	ZA1 R32	ZA11 R28	ZA11 R30	ZA20 R32	ZA21 R32	ZA31 R16	ZA31 R18
2^9	ZA0 R33	ZA1 R33	ZA11 R29	ZA11 R31	ZA20 R33	ZA21 R33	ZA31 R17	ZA31 R19
2^{10}	ZA11 R27	ZA11 R24	ZA11 R21	ZA11 R18	ZA20 R11	ZA20 R8	ZA20 R5	ZA20 R2
2^{11}	ZA11 R26	ZA11 R23	ZA11 R20	ZA11 R17	ZA20 R10	ZA20 R7	ZA20 R4	ZA20 R1
2^{12}	ZA11 R25	ZA11 R22	ZA11 R19	ZA11 R16	ZA20 R9	ZA20 R6	ZA20 R3	ZA20 R0
2^{13}	ZA0 R11	ZA0 R8	ZA0 R5	ZA0 R2	ZA31 R20	ZA31 R23	ZA31 R26	ZA31 R29
2^{14}	ZA0 R10	ZA0 R7	ZA0 R4	ZA0 R1	ZA31 R21	ZA31 R24	ZA31 R27	ZA31 R30
2^{15}	ZA0 R9	ZA0 R6	ZA0 R3	ZA0 R0	ZA31 R22	ZA31 R25	ZA31 R28	ZA31 R31
CHIP SELECT (2^{16})	ZA0 R14	ZA0 R15	ZA11 R14	ZA11 R15	ZA20 R14	ZA20 R15	ZA31 R14	ZA31 R15
2^{16} (2^{17})	WV0 R30	WV0 R31	WV0 R32	WV0 R33	WV20 R30	WV20 R31	WV20 R32	WV20 R33
GO WRITE	ZA1	ZA1	ZA10	ZA10	ZA21	ZA21	ZA30	ZA30

DATA BIT	DATA ONBOARD FANOUT							
	CPU A	CPU B	CPU C	CPU D	CPU E	CPU F	CPU G	CPU H
$N+2^0$	ZA1 R16	ZA1 R18	ZA1 R20	ZA1 R22	ZA30 R15	ZA30 R13	ZA30 R11	ZA30 R9
$N+2^1$	ZA1 R17	ZA1 R19	ZA1 R21	ZA1 R23	ZA30 R14	ZA30 R12	ZA30 R10	ZA30 R8
$N+2^2$	ZA10 R0	ZA10 R2	ZA10 R4	ZA10 R6	ZA21 R16	ZA21 R18	ZA21 R20	ZA21 R22
$N+2^3$	ZA10 R1	ZA10 R3	ZA10 R5	ZA10 R7	ZA21 R17	ZA21 R19	ZA21 R21	ZA21 R23
$N+2^4$	ZA0 R12	ZA0 R13	ZA11 R12	ZA11 R13	ZA20 R12	ZA20 R13	ZA31 R12	ZA31 R13
$N+2^5$	ZA10 R22	ZA10 R20	ZA10 R18	ZA10 R16	ZA21 R6	ZA21 R4	ZA21 R2	ZA21 R0
$N+2^6$	ZA10 R23	ZA10 R21	ZA10 R19	ZA10 R17	ZA21 R7	ZA21 R5	ZA21 R3	ZA21 R1
$N+2^7$	ZA1 R6	ZA1 R4	ZA1 R2	ZA1 R0	ZA30 R22	ZA30 R20	ZA30 R18	ZA30 R16
$N+2^8$	ZA1 R7	ZA1 R5	ZA1 R3	ZA1 R1	ZA30 R23	ZA30 R21	ZA30 R19	ZA30 R17

Hardware Trng.
A-7786A J.E.S.

CRAY Y-MP ONBOARD FANOUT ADDRESS/DATA

ADDRESS	CPU A	CPU B	CPU C	CPU D	CPU E	CPU F	CPU G	CPU H
2^0	WW0 MEM. 0	WW0 MEM. 1	WO0 MEM. 0	WO0 MEM. 1	WO0 MEM. 6	WO0 MEM. 7	WW0 MEM. 6	WW0 MEM. 7
2^1	WW10 MEM. 0	WW10 MEM. 1	WO10 MEM. 0	WO10 MEM. 1	WO10 MEM. 6	WO10 MEM. 7	WW10 MEM. 6	WW10 MEM. 7
2^2	WW20 MEM. 0	WW20 MEM. 1	WO20 MEM. 0	WO20 MEM. 1	WO20 MEM. 6	WO20 MEM. 7	WW20 MEM. 6	WW20 MEM. 7
2^3	WW30 MEM. 0	WW30 MEM. 1	WO30 MEM. 0	WO30 MEM. 1	WO30 MEM. 6	WO30 MEM. 7	WW30 MEM. 6	WW30 MEM. 7
2^4	WO0 MEM. 0	WO0 MEM. 1	WO1 MEM. 0	WO1 MEM. 1	WO1 MEM. 6	WO1 MEM. 7	WO0 MEM. 6	WO0 MEM. 7
2^5	WO10 MEM. 0	WO10 MEM. 1	WO11 MEM. 0	WO11 MEM. 1	WO11 MEM. 6	WO11 MEM. 7	WO10 MEM. 6	WO10 MEM. 7
2^6	WO20 MEM. 0	WO20 MEM. 1	WO21 MEM. 0	WO21 MEM. 1	WO21 MEM. 6	WO21 MEM. 7	WO20 MEM. 6	WO20 MEM. 7
2^7	WO30 MEM. 0	WO30 MEM. 1	WO30 MEM. 2	WO30 MEM. 3	WO30 MEM. 4	WO30 MEM. 5	WO30 MEM. 6	WO30 MEM. 7
2^8	ZA1 MEM. 0	ZA1 MEM. 1	ZA1 MEM. 2	ZA1 MEM. 3	ZA1 MEM. 4	ZA1 MEM. 5	ZA1 MEM. 6	ZA1 MEM. 7
2^9	ZA10 MEM. 0	ZA10 MEM. 1	ZA10 MEM. 2	ZA10 MEM. 3	ZA10 MEM. 4	ZA10 MEM. 5	ZA10 MEM. 6	ZA10 MEM. 7
2^{10}	ZA21 MEM. 0	ZA21 MEM. 1	ZA21 MEM. 2	ZA21 MEM. 3	ZA21 MEM. 4	ZA21 MEM. 5	ZA21 MEM. 6	ZA21 MEM. 7
2^{11}	ZA30 MEM. 0	ZA30 MEM. 1	ZA30 MEM. 2	ZA30 MEM. 3	ZA30 MEM. 4	ZA30 MEM. 5	ZA30 MEM. 6	ZA30 MEM. 7
2^{12}	WO31 MEM. 0	WO31 MEM. 1	WO31 MEM. 2	WO31 MEM. 3	WO31 MEM. 4	WO31 MEM. 5	WO31 MEM. 6	WO31 MEM. 7
2^{13}	WO1 MEM. 0	WO1 MEM. 1	WW1 MEM. 0	WW1 MEM. 1	WW1 MEM. 6	WW1 MEM. 7	WO1 MEM. 6	WO1 MEM. 7
2^{14}	WO11 MEM. 0	WO11 MEM. 1	WW11 MEM. 0	WW11 MEM. 1	WW11 MEM. 6	WW11 MEM. 7	WO11 MEM. 6	WO11 MEM. 7
2^{15}	WO21 MEM. 0	WO21 MEM. 1	WW21 MEM. 0	WW21 MEM. 1	WW21 MEM. 6	WW21 MEM. 7	WO21 MEM. 6	WO21 MEM. 7
CHIP SELECT (2^{16})	WO31 MEM. 0	WO31 MEM. 1	WW31 MEM. 0	WW31 MEM. 1	WW31 MEM. 6	WW31 MEM. 7	WO31 MEM. 6	WO31 MEM. 7
2^{16} (2^{17})	WP10, WP30 MEM. 0	WP10, WP30 MEM. 1	WP10, WP30 MEM. 2	WP10, WP30 MEM.3	WP10, WP30 MEM. 7	WP10, WP30 MEM. 6	WP10, WP30 MEM. 5	WP10, WP30 MEM. 4
WRITE REFERENCE	WO30 MEM. 2	WO30 MEM. 3	WO31 MEM. 2	WO31 MEM.3	WO31 MEM. 4	WO31 MEM. 5	WO3O MEM. 4	WO30 MEM. 5

Hardware Trng.
A-7787 N.A.N.

CRAY Y-MP 1 TO 8 ADDRESS OUTBOARD FANOUT

ABORT FANOUT

ABORT	CPU A	CPU B	CPU C	CPU D	CPU E	CPU F	CPU G	CPU H
ABORT	WO0	WO0	WO1	WO1	WO1	WO1	WO0	WO0
	MEM. 2	MEM. 3	MEM. 2	MEM. 3	MEM. 4	MEM. 5	MEM. 4	MEM. 5

GOSS FANOUT

GOSS	CPU A	CPU B	CPU C	CPU D	CPU E	CPU F	CPU G	CPU H
GOSS 0	WW0	WW0	WW0	WW0	WW0	WW0	WW0	WW0
	MEM. 0	MEM. 1	MEM. 2	MEM. 3	MEM. 4	MEM. 5	MEM. 6	MEM. 7
GOSS 1	WW1	WW1	WW1	WW1	WW1	WW1	WW1	WW1
	MEM. 0	MEM. 1	MEM. 2	MEM. 3	MEM. 4	MEM. 5	MEM. 6	MEM. 7
GOSS 2	WW10	WW10	WW10	WW10	WW10	WW10	WW10	WW10
	MEM. 0	MEM. 1	MEM. 2	MEM. 3	MEM. 4	MEM. 5	MEM. 6	MEM. 7
GOSS 3	WW11	WW11	WW11	WW11	WW11	WW11	WW11	WW11
	MEM. 0	MEM. 1	MEM. 2	MEM. 3	MEM. 4	MEM. 5	MEM. 6	MEM. 7
GOSS 4	WW20	WW20	WW20	WW20	WW20	WW20	WW20	WW20
	MEM. 0	MEM. 1	MEM. 2	MEM. 3	MEM. 4	MEM. 5	MEM. 6	MEM. 7
GOSS 5	WW21	WW21	WW21	WW21	WW21	WW21	WW21	WW21
	MEM. 0	MEM. 1	MEM. 2	MEM. 3	MEM. 4	MEM. 5	MEM. 6	MEM. 7
GOSS 6	WW30	WW30	WW30	WW30	WW30	WW30	WW30	WW30
	MEM. 0	MEM. 1	MEM. 2	MEM. 3	MEM. 4	MEM. 5	MEM. 6	MEM. 7
GOSS 7	WW31	WW31	WW31	WW31	WW31	WW31	WW31	WW31
	MEM. 0	MEM. 1	MEM. 2	MEM. 3	MEM. 4	MEM. 5	MEM. 6	MEM. 7

BANK BIT (2^2, 2^1, 2^0)

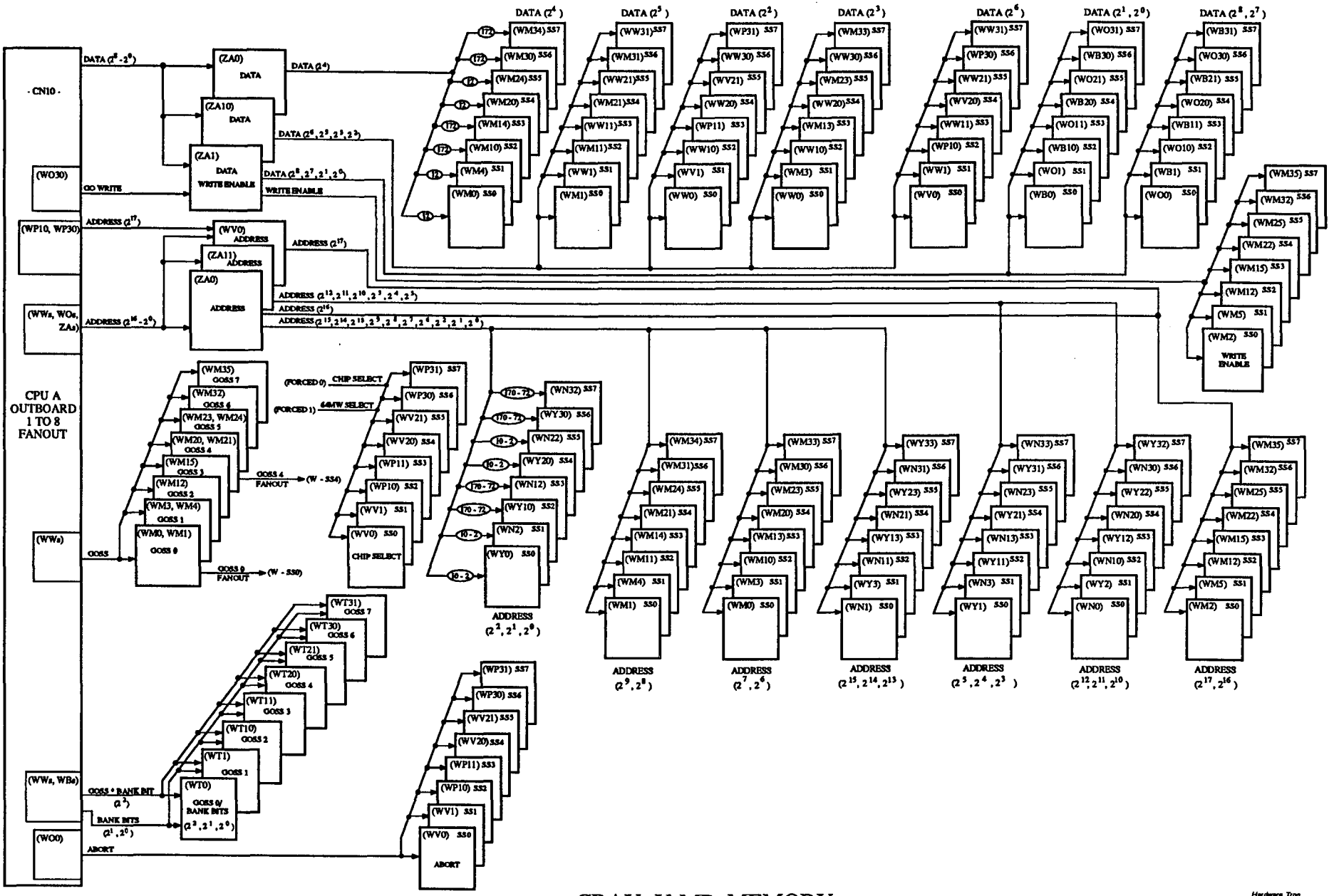
BANK BIT	CPU A	CPU B	CPU C	CPU D	CPU E	CPU F	CPU G	CPU H
2^0	WW0, WW10	WW0, WW10	WO10	WO10	WO10	WO10	WW0, WW10	WW0, WW10
	MEM. 2	MEM. 3	MEM. 2	MEM. 3	MEM. 4	MEM. 5	MEM. 4	MEM. 5
2^0	WW1, WW11	WW1, WW11	WO11	WO11	WO11	WO11	WW1, WW11	WW1, WW11
	MEM. 2	MEM. 3	MEM. 2	MEM. 3	MEM. 4	MEM. 5	MEM. 4	MEM. 5
2^1	WW30, WW20	WW30, WW20	WO21	WO21	WO21	WO21	WW30, WW20	WW30, WW20
	MEM. 2	MEM. 3	MEM. 2	MEM. 3	MEM. 4	MEM. 5	MEM. 4	MEM. 5
2^1	WW31, WW21	WW31, WW21	WO20	WO20	WO20	WO20	WW31, WW21	WW31, WW21
	MEM. 2	MEM. 3	MEM. 2	MEM. 3	MEM. 4	MEM. 5	MEM. 4	MEM. 5
2^2	WB0, WB10	WB0, WB10	WB0, WB10	WB0, WB10	WB0, WB10	WB0, WB10	WB0, WB10	WB0, WB10
	WB20, WB30	WB20, WB30	WB20, WB30	WB20, WB30	WB20, WB30	WB20, WB30	WB20, WB30	WB20, WB30
	MEM. 0	MEM. 1	MEM. 2	MEM. 3	MEM. 4	MEM. 5	MEM. 6	MEM. 7
2^2	WB1, WB11	WB1, WB11	WB1, WB11	WB1, WB11	WB1, WB11	WB1, WB11	WB1, WB11	WB1, WB11
	WB21, WB31	WB21, WB31	WB21, WB31	WB21, WB31	WB21, WB31	WB21, WB31	WB21, WB31	WB21, WB31
	MEM. 0	MEM. 1	MEM. 2	MEM. 3	MEM. 4	MEM. 5	MEM. 6	MEM. 7

SS READ SELECT (2^2, 2^1, 2^0)

SS	CPU A	CPU B	CPU C	CPU D	CPU E	CPU F	CPU G	CPU H
2^0	ZS0	ZS0	ZS0	ZS0	ZS0	ZS0	ZS0	ZS0
	MEM. 0	MEM. 1	MEM. 2	MEM. 3	MEM. 4	MEM. 5	MEM. 6	MEM. 7
2^1	ZS1	ZS1	ZS1	ZS1	ZS1	ZS1	ZS1	ZS1
	MEM. 0	MEM. 1	MEM. 2	MEM. 3	MEM. 4	MEM. 5	MEM. 6	MEM. 7
2^2	ZS20	ZS20	ZS20	ZS20	ZS20	ZS20	ZS20	ZS20
	MEM. 0	MEM. 1	MEM. 2	MEM. 3	MEM. 4	MEM. 5	MEM. 6	MEM. 7

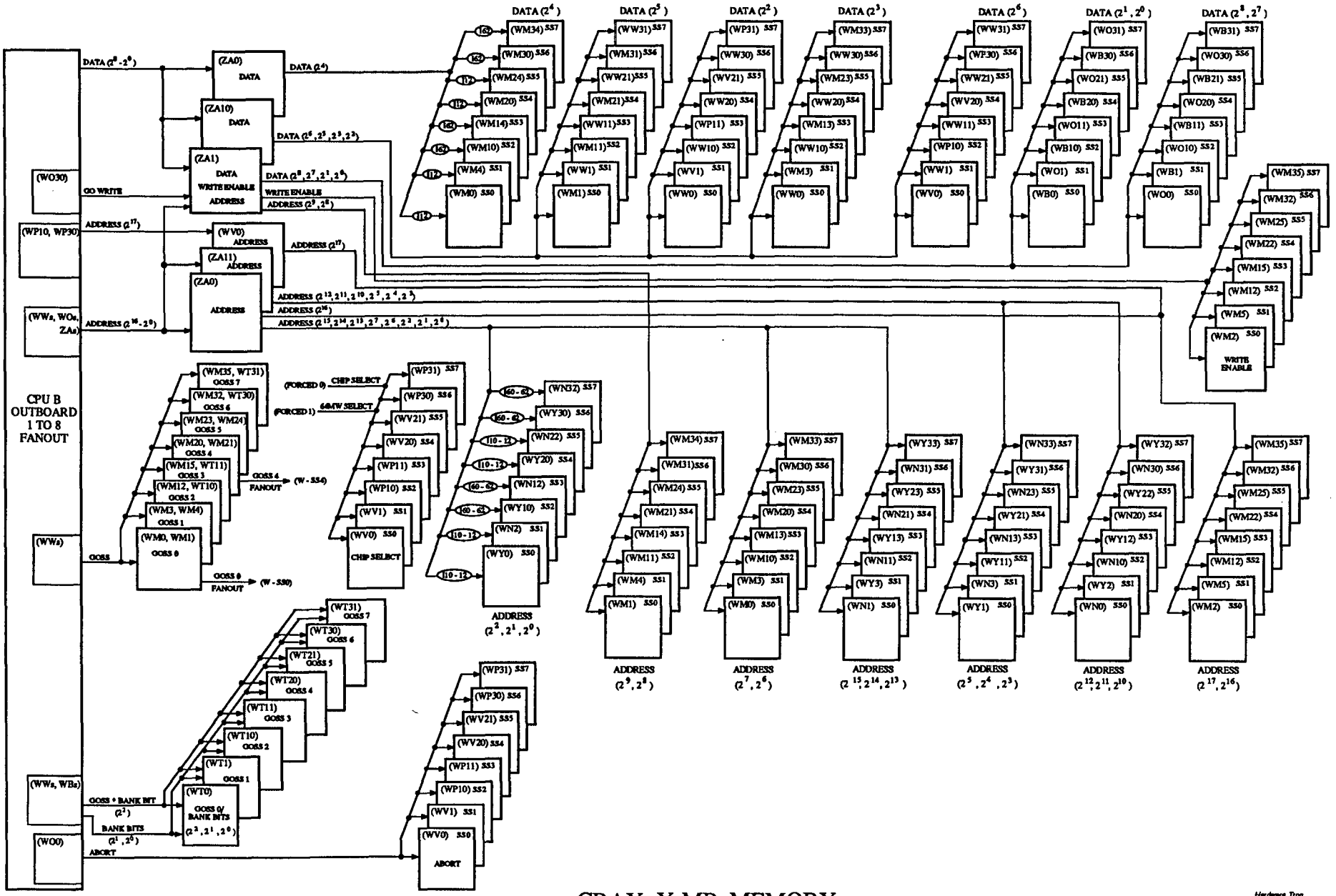
Hardware Trng.
A-7788 N.A.N.

CRAY Y-MP 1 TO 8 CONTROL OUTBOARD FANOUT



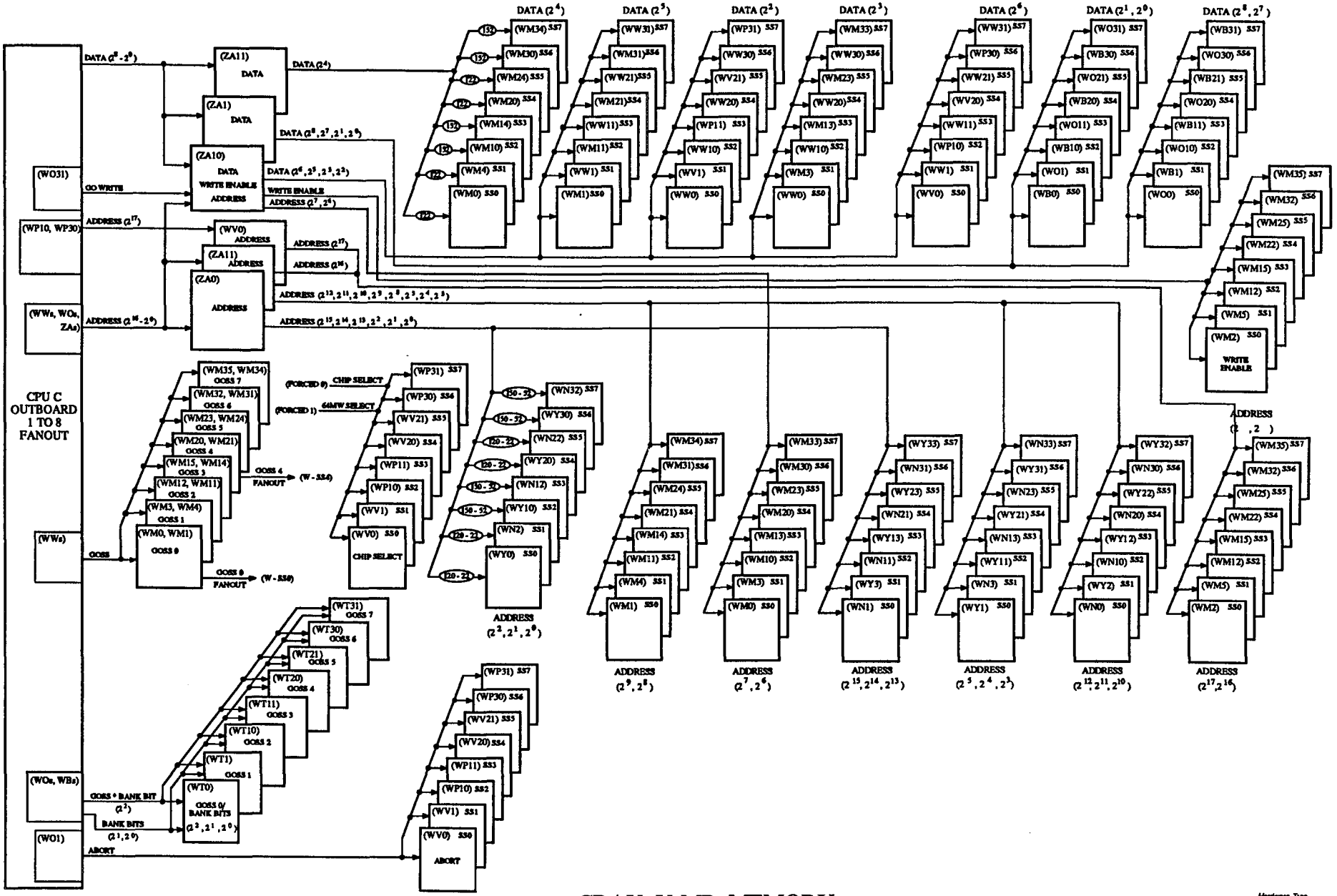
CRAY Y-MP MEMORY
CPU A 1 TO 8 ONBOARD SUBSECTION FANOUT

Hardware Trng.
A-7788A N.A.N.



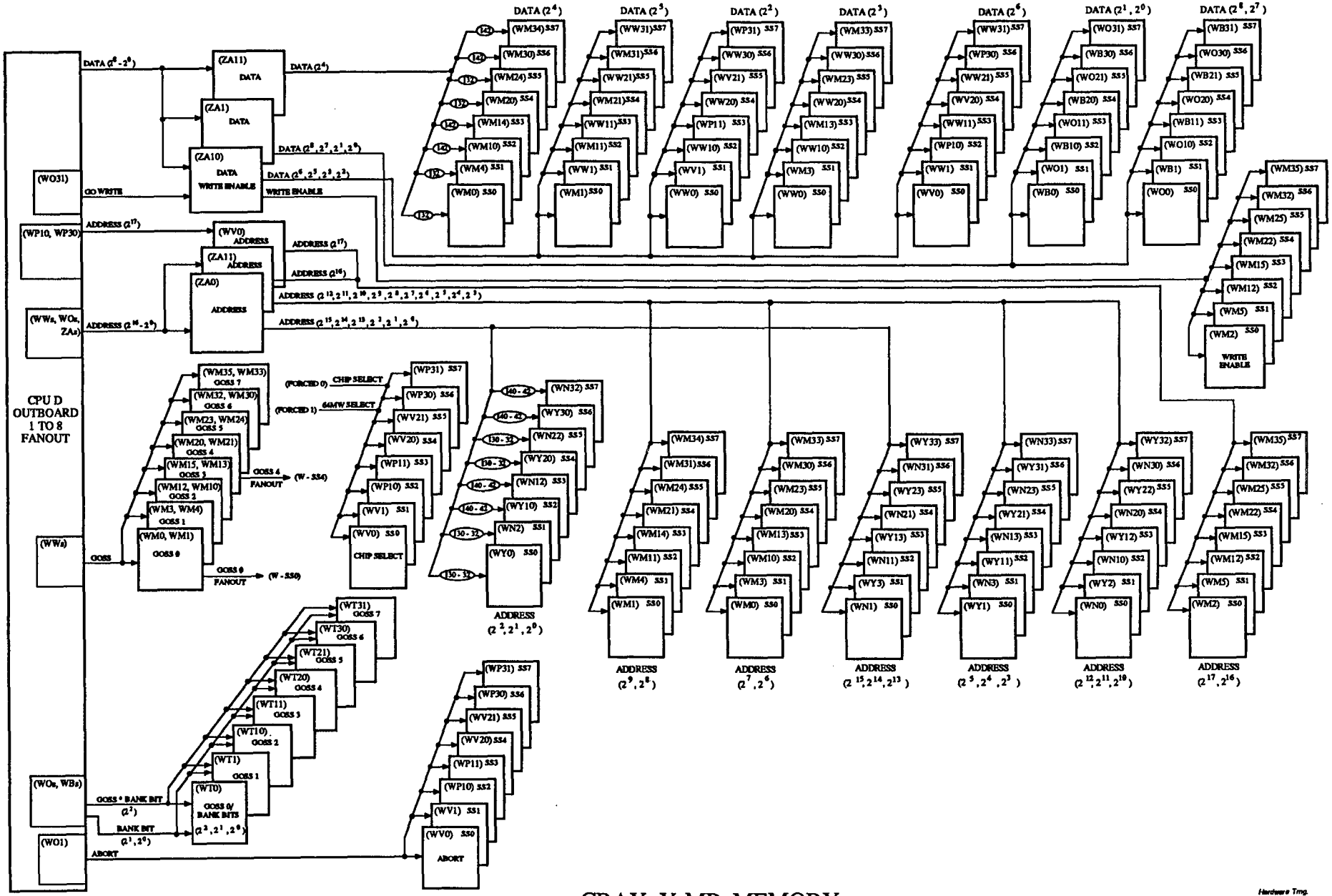
Hardware Trng. A-7790A M.A.N.

CRAY Y-MP MEMORY
CPU B 1 TO 8 ONBOARD SUBSECTION FANOUT



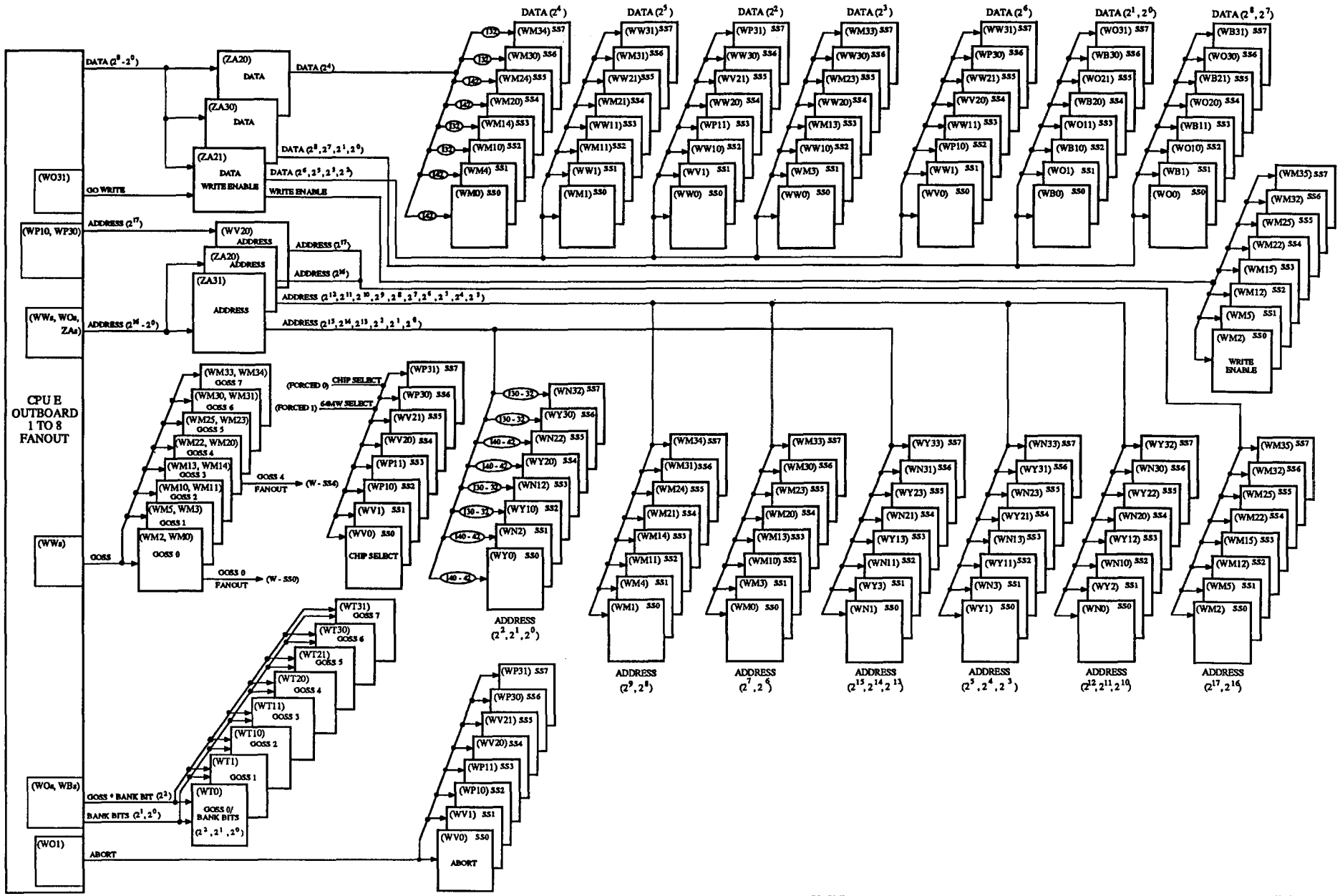
CRAY Y-MP MEMORY
CPU C 1 TO 8 ONBOARD SUBSECTION FANOUT

Hardware Trng.
A-7781A N.A.N.



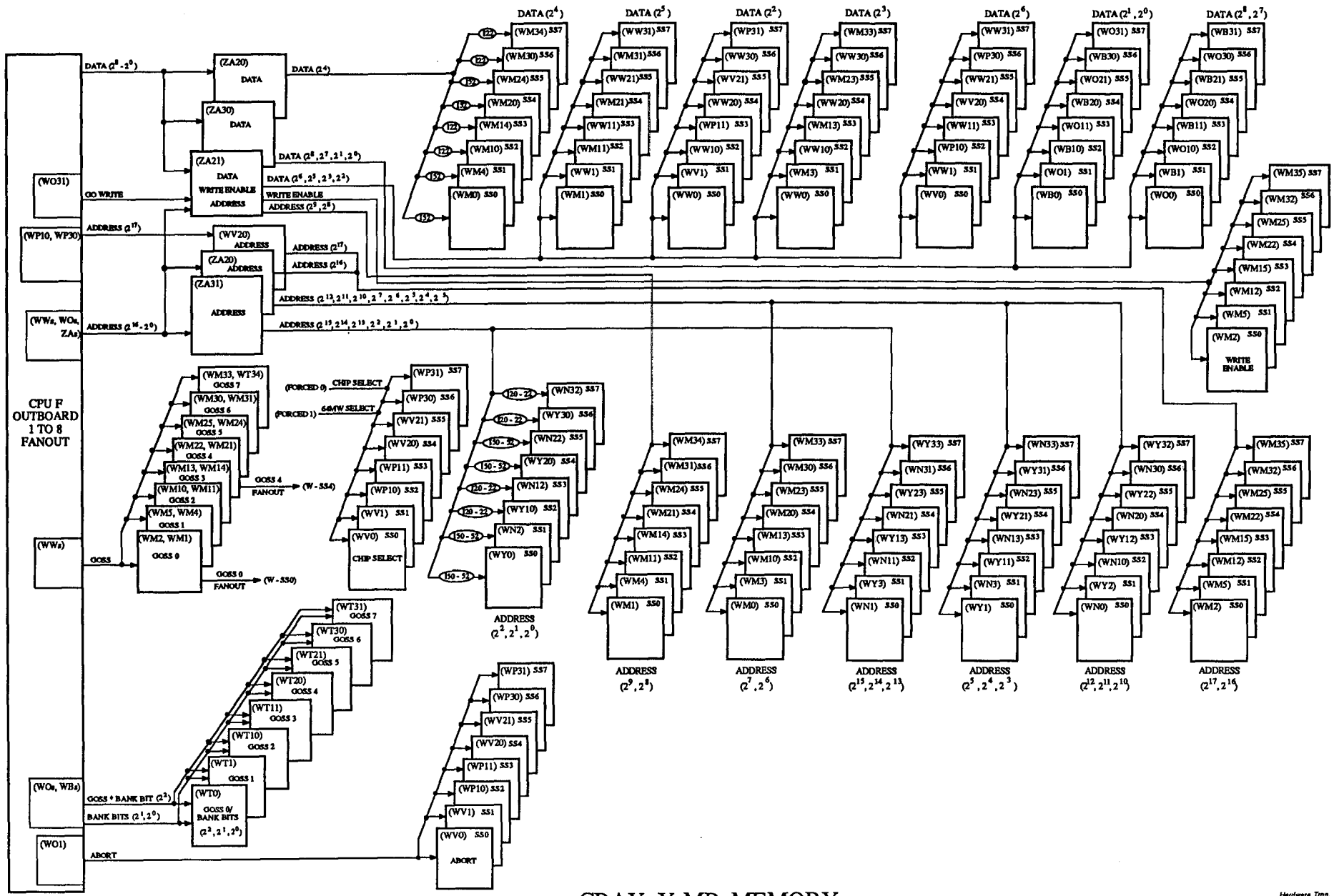
Hardware Trng.
A-7782A N.A.H.

CRAY Y-MP MEMORY
CPU D 1 TO 8 ONBOARD SUBSECTION FANOUT



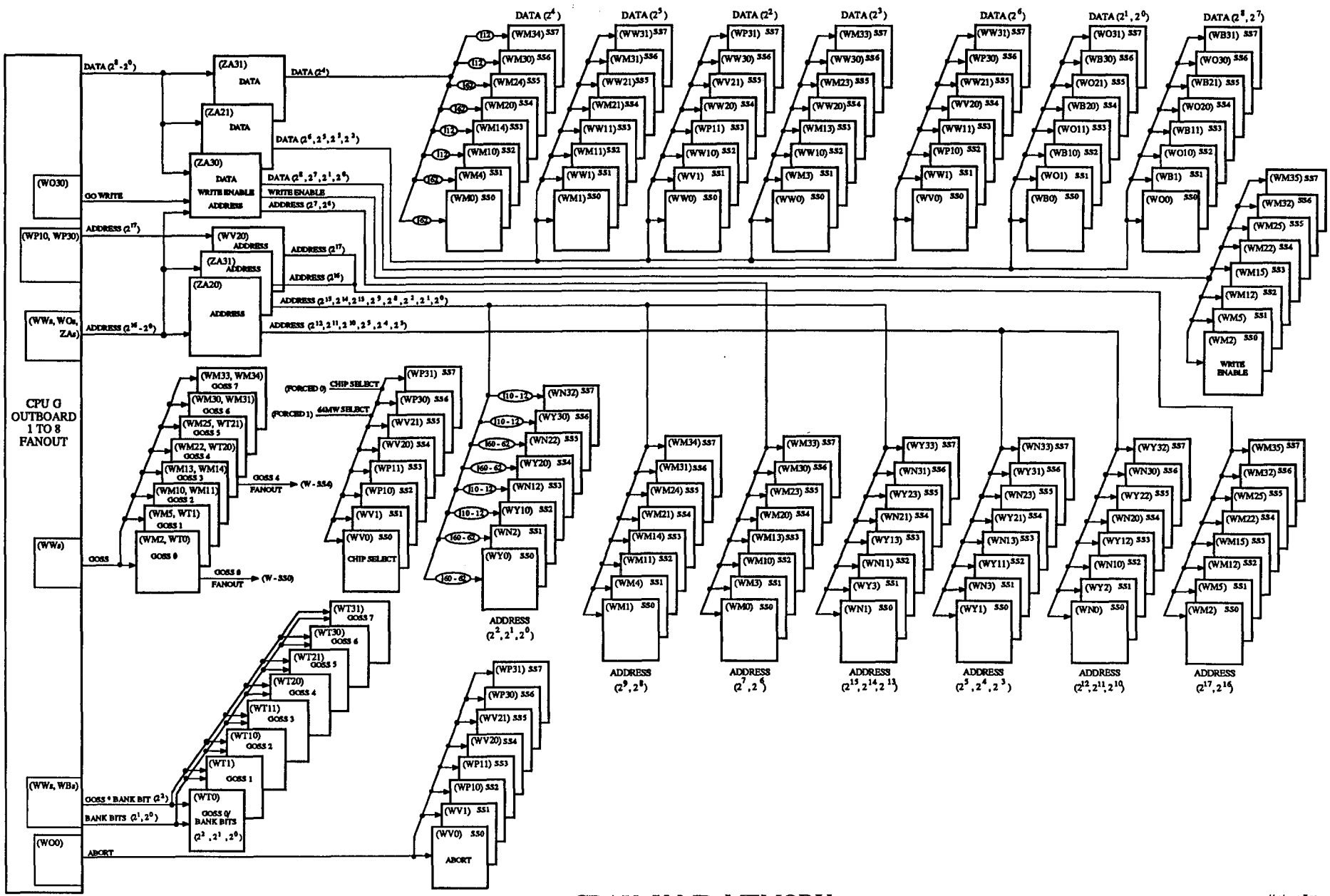
CRAY Y-MP MEMORY
CPU E 1 TO 8 ONBOARD SUBSECTION FANOUT

Hardware Trng.
A-7793A N.A.N.



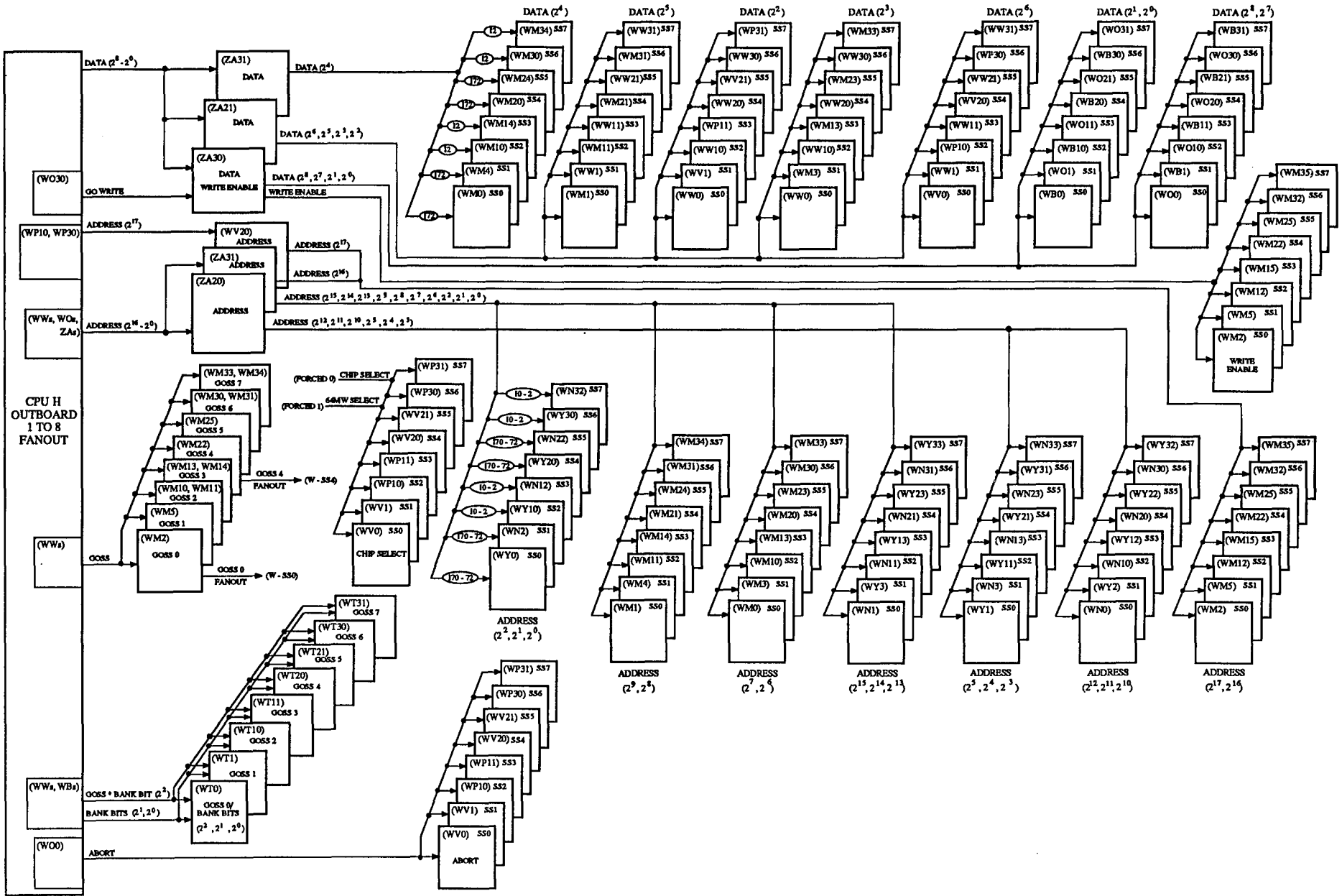
CRAY Y-MP MEMORY
CPU F 1 TO 8 ONBOARD SUBSECTION FANOUT

Hardware Tmg. A-77944 NAN



CRAY Y-MP MEMORY
CPU G 1 TO 8 ONBOARD SUBSECTION FANOUT

Hardware Trng.
A-7795A M.A.N.



CRAY Y-MP MEMORY
CPU H 1 TO 8 ONBOARD SUBSECTION FANOUT

Hardware Tmg.
A-7786A N.A.N.

128-Million Word Memory vs 64-Million Word Memory

The 128-million word memory utilizes the same options as the 64-million word memory so the basic theory of the two is the same. Basically, there are only two differences. First, the 128-million word memory is a fully populated module, meaning there are twice as many memory chips compared to the 64-million word memory. Doubling the amount of memory chips means there are two (256K x 1) memory chips per bit position. The second difference ties into the first. Since there are twice as many memory chips, the 128-million word memory needs one more address line. This address line (chip select) will select one of the two chips per bit position during a reference. Which chip is selected is dependent upon C.S. 0 and C.S. 1. Both C.S. 0 and C. S. 1 come from address bit 2^{18} on the memory module or address bit 2^{19} of the absolute address. If address bit 2^{19} equals a zero, C.S. 0 is enabled. If address bit 2^{19} equals a one, then C. S. 1 is enabled.

Most of the documented training material for the 64-million word memory can also be used for the 128-million word memory. The material which does differ can be found on the following pages.

(WN) Option

The (WN) options are capable of handling 3 address bits. There are two (WN) options in each subsection, each handling different address bits. The (WN) options receive a signal called CPU A - H GOSS. This signal latches and holds the address bits. When a CPU is allowed to reference a bank the (WN) options will decode a Bank 0 - 7 CPU Select Code, which will allow the (WN) options to steer the address to the appropriate bank. The (WN) options also have a fanout which is used to assist in the Bank 0 - 7 CPU Select Fanout. In Subsection 0, (WN0) fans out Bank 4 - 5 CPU select and (WN1) fans out bank 6 - 7 CPU select.

(WO) Option

There is one (WO) option in each subsection which is capable of handling two write data bits. The (WO) options receive the same control signals as the (WB) options for latching and steering the data bits, except these signals are inverted. The (WO) options also assist in the 1 to 8 Outboard fanout of address and controls from the various CPUs to the eight modules within a section.

(WP) Option

The (WP) options are capable of handling 1 data bit, chip select, and the Abort signal. There is one (WP) option in Subsections 2, 3, 6, and 7. The (WP) options receive the same control signals as the (WO) options to latch and steer the data bit to a bank in memory.

For the 128-million word memory there are two (256K x 1) memory chips per bit position or 144 chips per 72-bit word. Chip select 0 selects the lower 72 chips and chip select 1 selects the upper 72 chips. When the abort is present, the chip selects are forced to zeroes, preventing a write operation from completing or during a read, causing zeroes to be read from memory.

(WR) Option

There are three (WR) options in each subsection which are used during both the read and write operations. During the write operation, the (WR) options receive a control signal called Go Write Bank n, n + 1. This signal produces the Write Enable which is sent to specific banks in memory for 3 CPs. The timing of this signal is controlled by the Go Bank n, n + 1 and the 3 CP Write Enable Select signal. (WR0), (WR4), (WR10), (WR14), (WR20), (WR24), (WR30), and (WR34) generate the Write Enable for Banks 2 and 3 for their respective subsections. (WR1), (WR5), (WR11), (WR15), (WR21), (WR25), (WR31), and (WR35) generate the Write Enable for Banks 4 and 5. (WR2), (WR12), (WR22), and (WR32) generate the Write Enable for Banks 6 and 7. (WR3), (WR13), (WR23), and (WR33) generate the Write Enable for Banks 0 and 1.

Write Operation To Subsection 0

On a Write operation to memory, the address, control, and data are sent from the CPU module to a particular section. The CPU module determines the section to which these signals are sent. Once sent to the section, the Control and Address signals undergo a 1 to 8 Outboard fanout to each module within the section. Data is not fanned out, but is split up into 9 bits per module. Memory module 0, or Memory 0, receives data bit (2^8 - 2^0) and so on. The 9 bits of data enter the (WB0, WW0, WM1, WV0, WO0) options for Subsection 0, along with GOSS 0 CPU (A - H). The GOSS 0 CPU (A - H) signals will latch and hold the data for the correct CPU. The same thing happens for the address, but this is performed on the (WY0, WY1, WM0, WM1, WN0, WN1, WM2) options for Subsection 0. Once the (WT0) option has resolved any conflicts among the CPUs, the (WT) will generate a Bank (0 - 7) Select Code, which is then sent to the latched data and address on the(W-) options. The Bank (0 - 7) Select Code will assign a particular CPU (A - H) to a specific Bank (0 - 7). The Select Code sent from the (WT) option is (000) for CPU 0, (001) for CPU 1, etc; however, on the address and data (W-) options, not all the options receive the true state of the Select Code. The (WM0, WM1, WV0, WO0) options for data and the (WM0, WM1, WM2, WN0, WN1) options for address receive the inverted state of the Select Code, while the (WB0, WW0) options for data and the (WY0, WY1) options for address receive the true Select Code.

The data is then steered to the correct bank within Subsection 0 for the CPU (A - H) that was requesting a Write reference. The Write Enable is supplied by the (WL0, WR0, WR1, WR2) options which are assigned to that bank. Banks (0 - 1) are controlled by (WL0) option, Banks (2 - 3) by the (WR0) option, Banks (4 - 5) by the (WR1) option, and Banks (6 - 7) by the (WR2) option. The address and data are held on the memory chip for 5 CPs by the (W-) options. The chip select is supplied by the (WV0) option. For-64 million word memory, the chip select is always enabled during a reference (selecting the nine memory chips in the bank) unless an abort occurs. For 128-million word memory, there are two (256K x l) chips per bit position. The chip select will select one of the two chips during a reference. Which chip is selected is dependent on C.S. 0 or C.S. 1. Both C.S. 0 and C.S. 1 come from address bit (2^{18}) on the memory module or address bit (2^{19}) of the absolute address. If address bit (2^{19}) equals a zero, C.S. 0 is enabled. If address bit (2^{19}) equals a one, C.S. 1 is enabled. When a CPU sends an abort to the (WV/WP) options, the (WV/WP) will disable C.S. 0 and C.S. 1. When an abort occurs on a write operation to memory, nothing is written; on a read operation, zeroes are read from memory.

(WV) Option

The (WV) options are capable of handling 1 data bit, chip select, and the Abort signal. There is one (WV) option in Subsections 0, 1, 4, and 5. The (WV) options receive the same control signals as the (WO) options to latch and steer the data bit to a bank in memory.

For the 128-million word memory there are two (256K x 1) memory chips per bit position or 144 chips per 72-bit word. Chip select 0 selects the lower 72 chips and chip select 1 selects the upper 72 chips. When the abort is present, the chip selects are forced to zeroes, preventing a write operation from completing or during a read, causing zeroes to be read from memory.

(ZA) Option

The (ZA) options are used to fanout memory information from the various CPUs. Since this fanout is done on the memory modules themselves, it is referred to as an Onboard fanout. In general, the (ZAs) fanout the Address, Chip Select, Data, and the Go Write to Subsections (0 - 7). The various (ZA) options can be differentiated by what data or address bits are being fanned out for the particular CPU. The (ZA) options also perform a 1 to 8 fanout to the eight memory modules within a section. (ZA1, ZA11) fanout address bits (2^{11}, 2^{10}, 2^{9}, 2^{8}) on memory modules (0 - 7) for all eight CPUs; this is called an Outboard fanout.

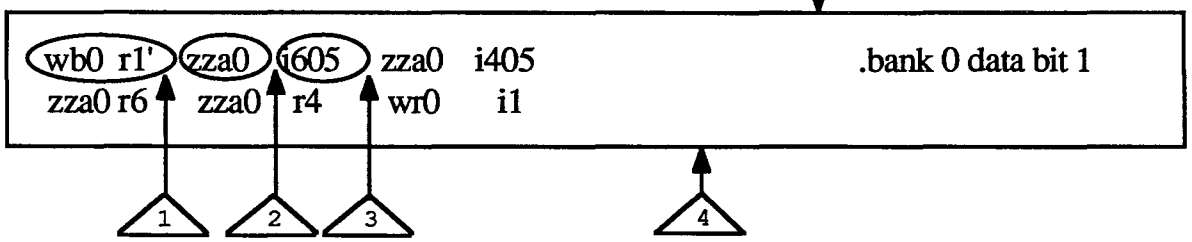
(ZS) Option

The (ZS) options are called the CPU Subsection Selects. There is one (ZS) per CPU per module. (ZS0) receives an SS Select Code from CPU 0 and selects 9 bits of data from 1 of 8 subsections. (ZS1) does the same for CPU 1, etc. The (ZSs) then send the 9 bits of read data to their particular CPU. The (ZSs) also perform a 1 to 8 Outboard fanout on subsection Read Select bits (2^{2}, 2^{1}, 2^{0}) for all CPUs.

Subsection Data A - D

$ subsection 0 : data bits

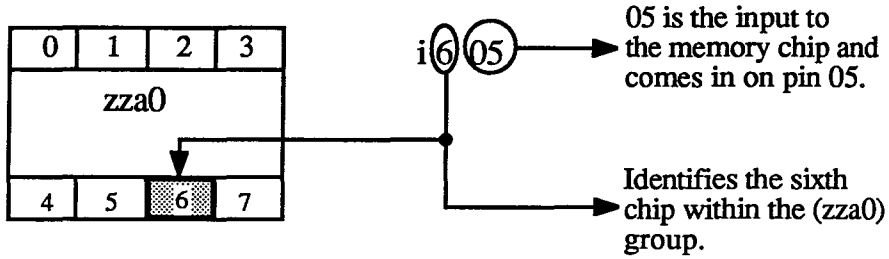
wb0	r0'	zza0	i205	zza0	i005	.bank 0 data bit 0
zza0	r2	zza0	r0	wr0	i0	
wb0	r1'	zza0	i605	zza0	i405	.bank 0 data bit 1
zza0	r6	zza0	r4	wr0	i1	
ww0	r0'	zza0	i105	zza0	i505	.bank 0 data bit 2
zza0	r1	zza0	r5	wr0	i2	



1 ORIGINATION - Bank 0 data bit 1 leaves the (wb0) option as term r1'.

2 GROUP DESCRIPTION - Bank 0 bit 1 is sent to a group of memory chips called zza0. The zza0 group contains 8 memory chips.

3 CHIP AND INPUT DESIGNATOR - The i605 can be broken into two parts:

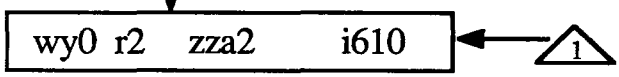


4 LINE READS AS - Bank 0 data bit 1 leaves the (wb0) option on r1'on a Write operation to the (zza0) group, chip 6, and (zza0) group, chip 4, and comes into chips 6 and 4 on pin 05. Bank 0 data bit 1 will leave (zza0) chip 6 as r6 on a Read operation and come into (zr0) option as i1. Bank 0 data bit 1 will leave (zza0) chip 4 as r4 and come into (wr0) option on i01. Depending on the chip selects, either r4 or r6 is Read but not both, same as on a Write operation.

BANK SUBSECTION 0 - 7

$ fn: addr 28a
$ rev: 0
$ date: 10-06-88
$ title: address fanout to ss0; bank N - N + 7
$ bank N

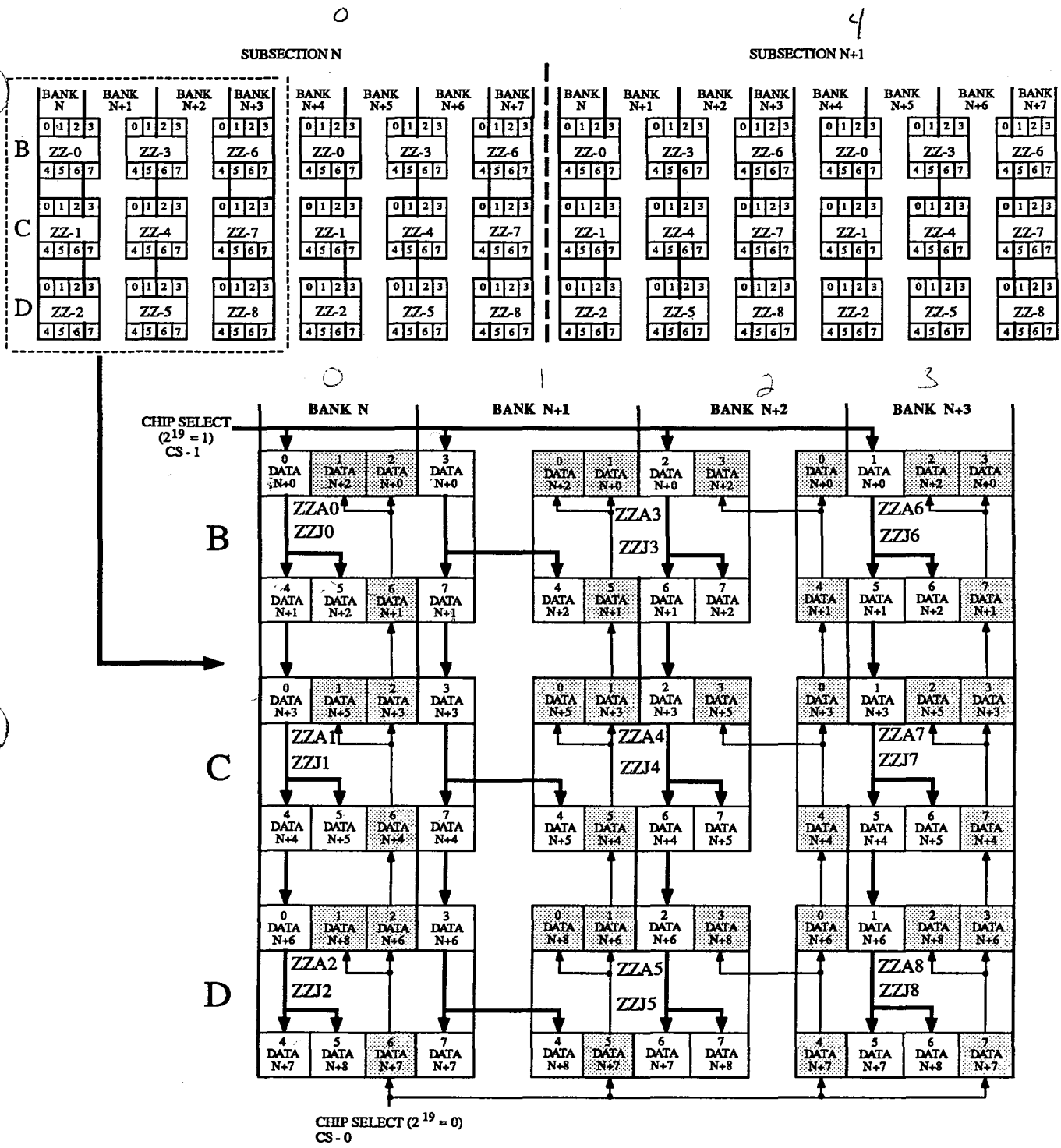
wy0	r0	zza2	i608	zza2	i208	zza2	i108	zza1	i608	zza1	i208 &
		zza1	i108	zza0	i608	zza0	i208	zza0	i108		
wy0	r0'	zza2	i508	zza2	i408	zza2	i008	zza1	i508	zza1	i408 &
		zza1	i008	zza0	i508	zza0	i408	zza0	i008		
wy0	r1	zza2	i609	zza2	i209	zza2	i109	zza1	i609	zza1	i209 &
		zza1	i109	zza0	i609	zza0	i209	zza0	i109		
wy0	r1'	zza2	i509	zza2	i409	zza2	i009	zza1	i509	zza1	i409 &
		zza1	i009	zza0	i509	zza0	i409	zza0	i009		
wy0	r2	zza2	i610	zza2	i210	zza2	i110	zza1	i610	zza1	i210 &
		zza1	i110	zza0	i610	zza0	i210	zza0	i110		
wy0	r2'	zza2	i510	zza2	i410	zza2	i010	zza1	i510	zza1	i410 &
		zza1	i010	zza0	i510	zza0	i410	zza0	i010		



The Bank Subsection 0 - 7 reads the same as the Subsection Data A - D, except the Bank Subsection 0 - 7 documents Address and Control to the memory module as per Subsection 0 - 7. The Subsection Data A - D documents only the data per the module boards A - D.

1 This portion of Bank Subsection 0 would read as the (wy0) option outputs as r2, r2 is address bit 2^2 for bank (N+0). Address bit 2^2 or r2 goes to the (zza2) group, chip 6 and comes into the memory chip on pin10.

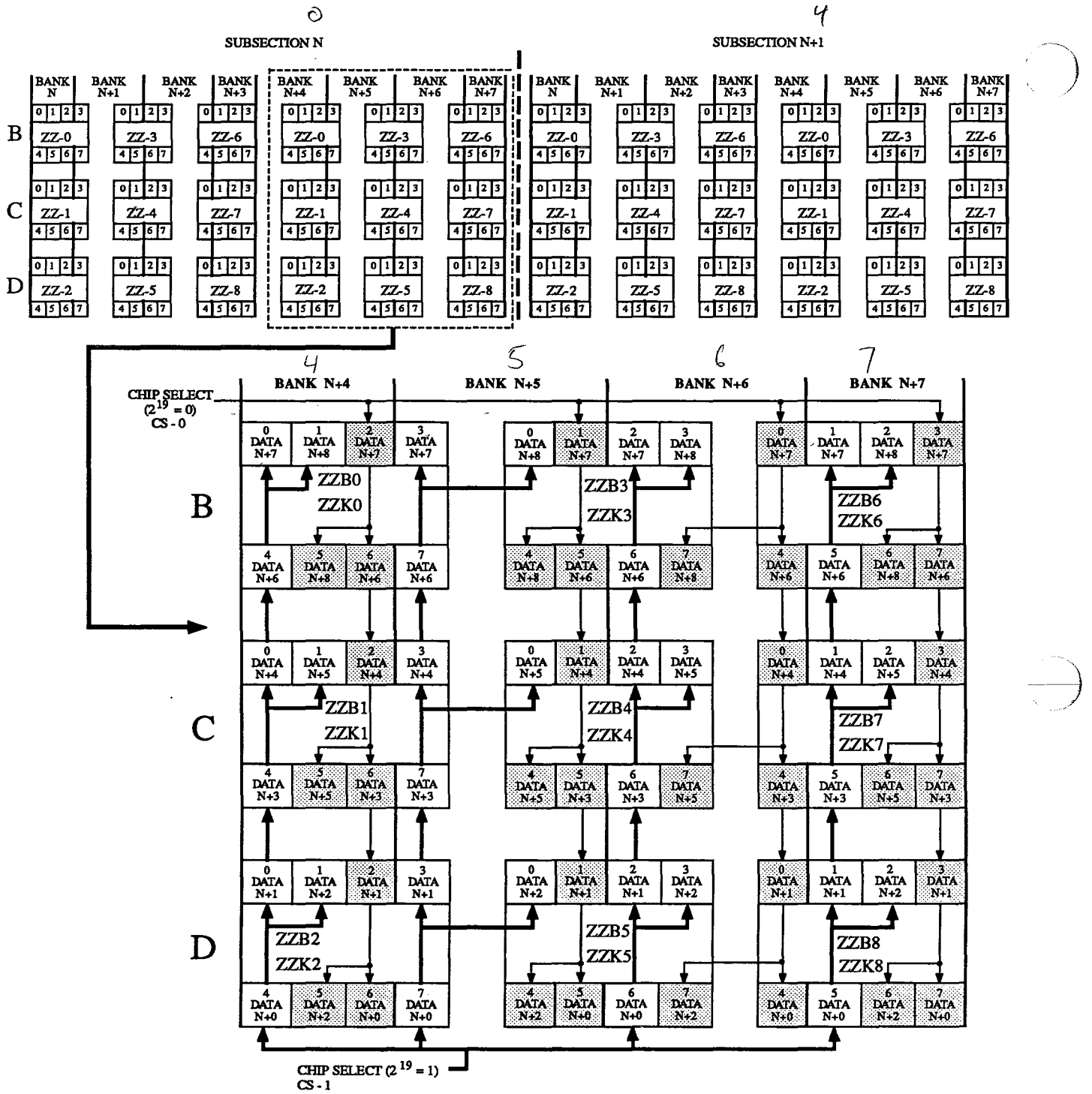
YM34/05



NOTE: EACH BANK HAS 18 MEMORY CHIPS (256K x 1) WHICH IS DIVIDED INTO 9 DATA BITS PER MODULE (N+0 - N+8) AND TWO CHIP SELECTS ($2^{19} = 0, 2^{19} = 1$)

Hardware Trng. A-6355 J.E.S.

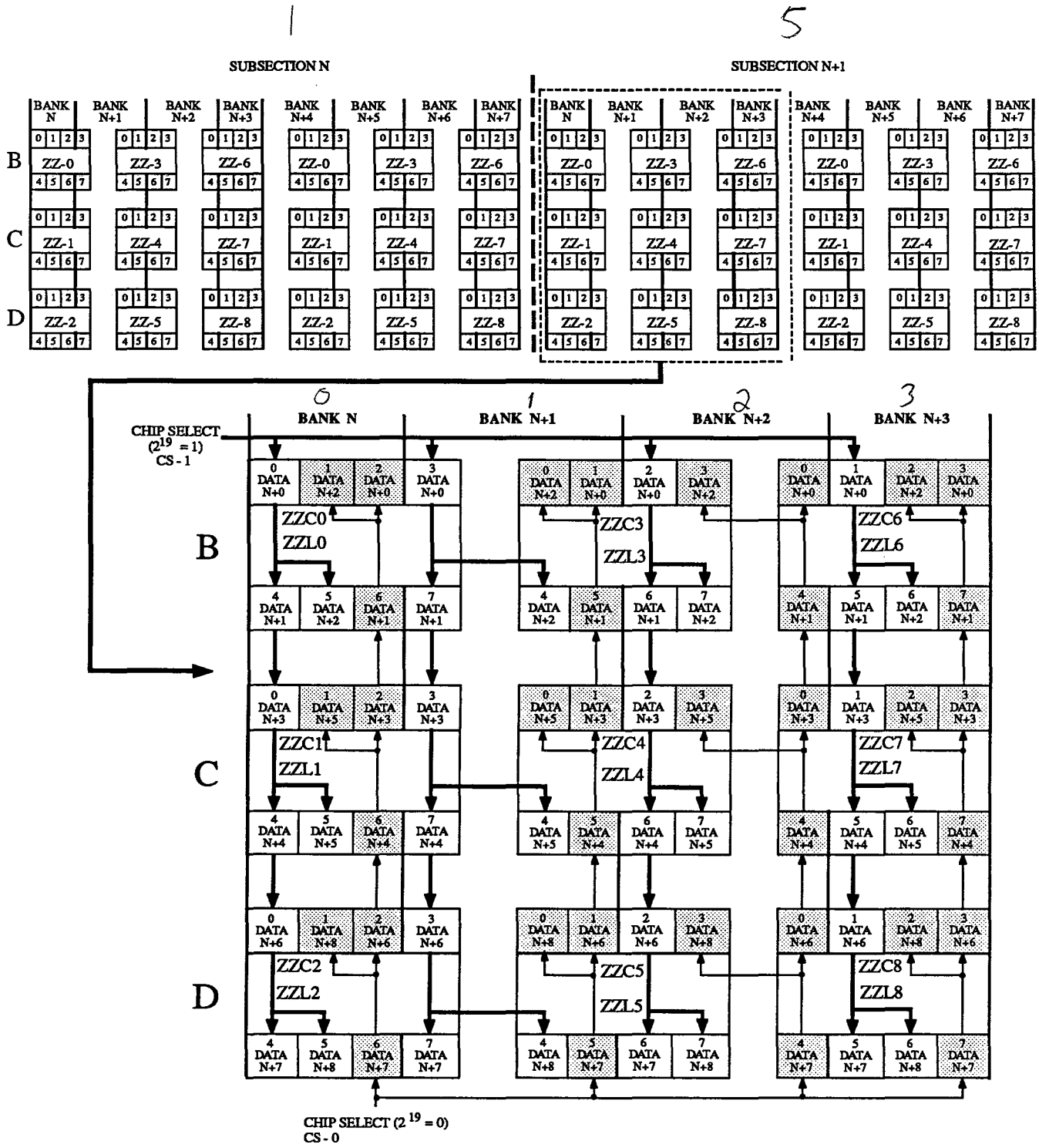
CRAY Y-MP MEMORY BOARD A/C SUBSECTION 0/4
BANKS (N - N + 3) (256K x 1) LOCATOR



NOTE: EACH BANK HAS 18 MEMORY CHIPS (256K x 1) WHICH IS DIVIDED INTO 9 DATA BITS PER MODULE (N+0 - N+8) AND TWO CHIP SELECTS ($2^{19} = 0$, $2^{19} = 1$)

Hardware Trng. A-8356 J.E.S.

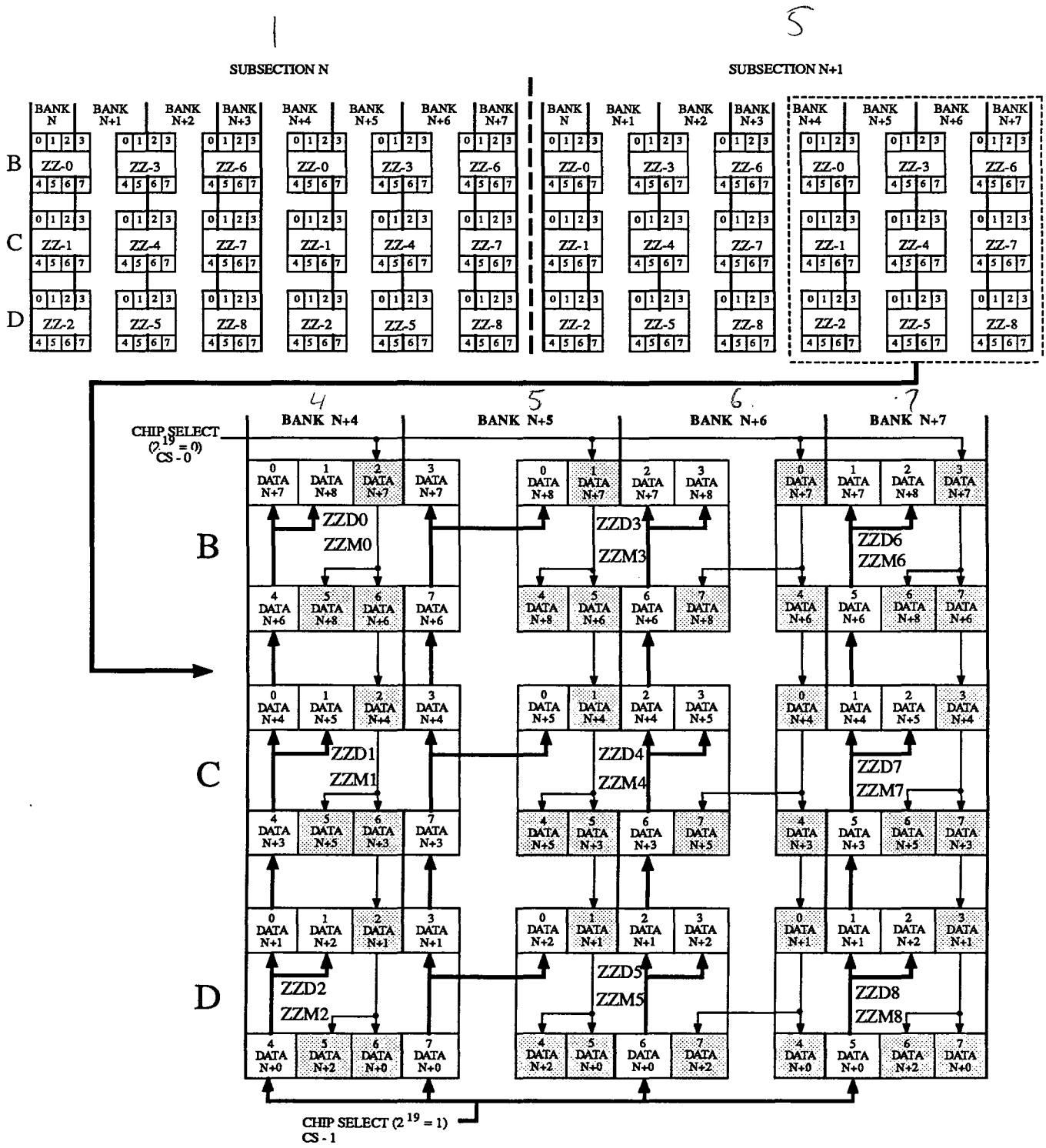
CRAY Y-MP MEMORY BOARD A/C SUBSECTION 0/4
BANKS (N + 4 - N + 7) (256K x 1) LOCATOR



NOTE: EACH BANK HAS 18 MEMORY CHIPS (256K x 1) WHICH IS DIVIDED INTO 9 DATA BITS PER MODULE (N+0 - N+8) AND TWO CHIP SELECTS (2^{19} = 0, 2^{19} = 1)

Hardware Trng. A-8357 J.E.S.

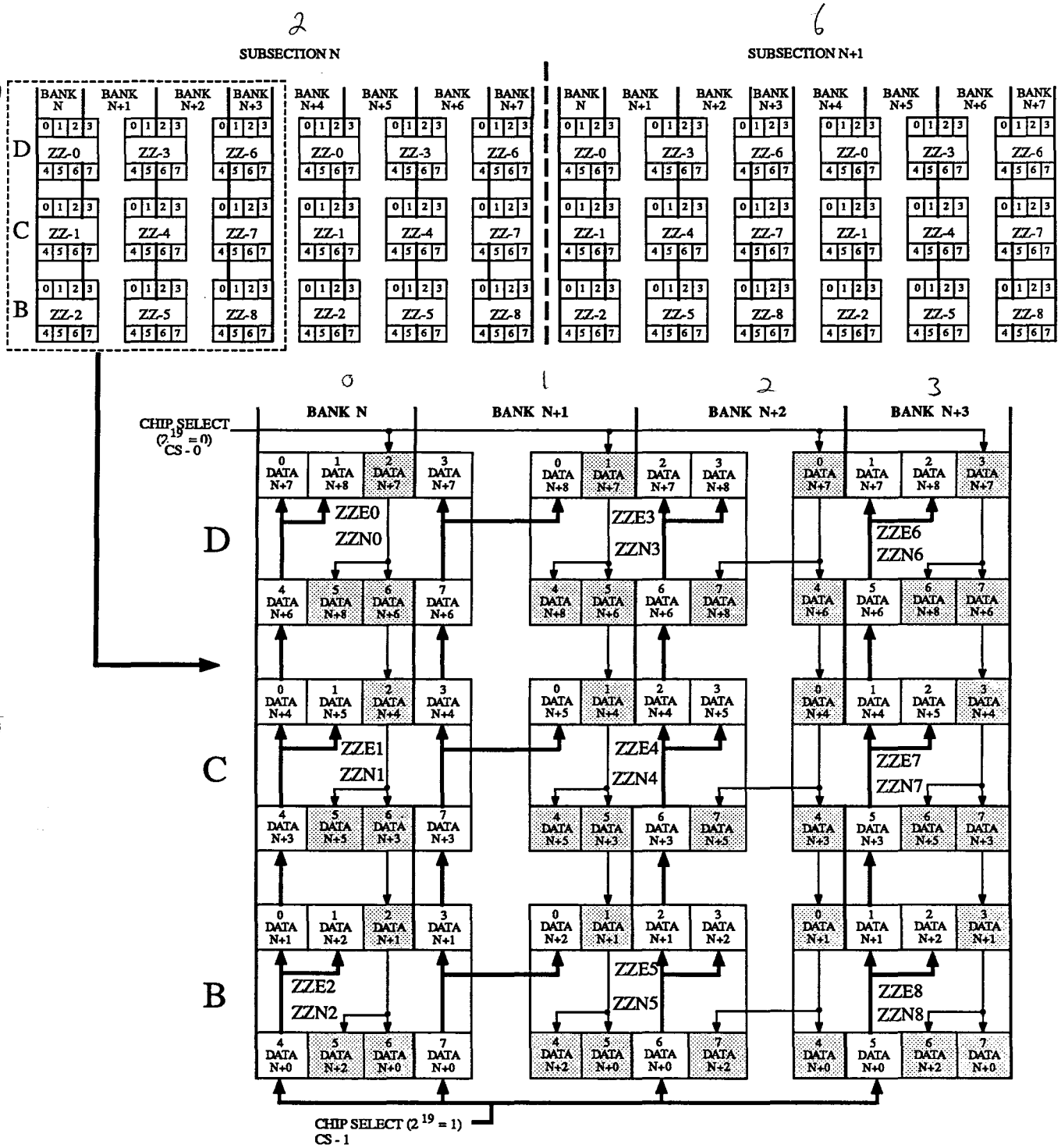
CRAY Y-MP MEMORY BOARD A/C SUBSECTION 1/5
BANKS (N - N + 3) (256K x 1) LOCATOR



NOTE: EACH BANK HAS 18 MEMORY CHIPS (256K x 1) WHICH IS DIVIDED INTO 9 DATA BITS PER MODULE (N+0 - N+8) AND TWO CHIP SELECTS ($2^{19} = 0$, $2^{19} = 1$)

Hardware Tmg. A-8358 J.E.S.

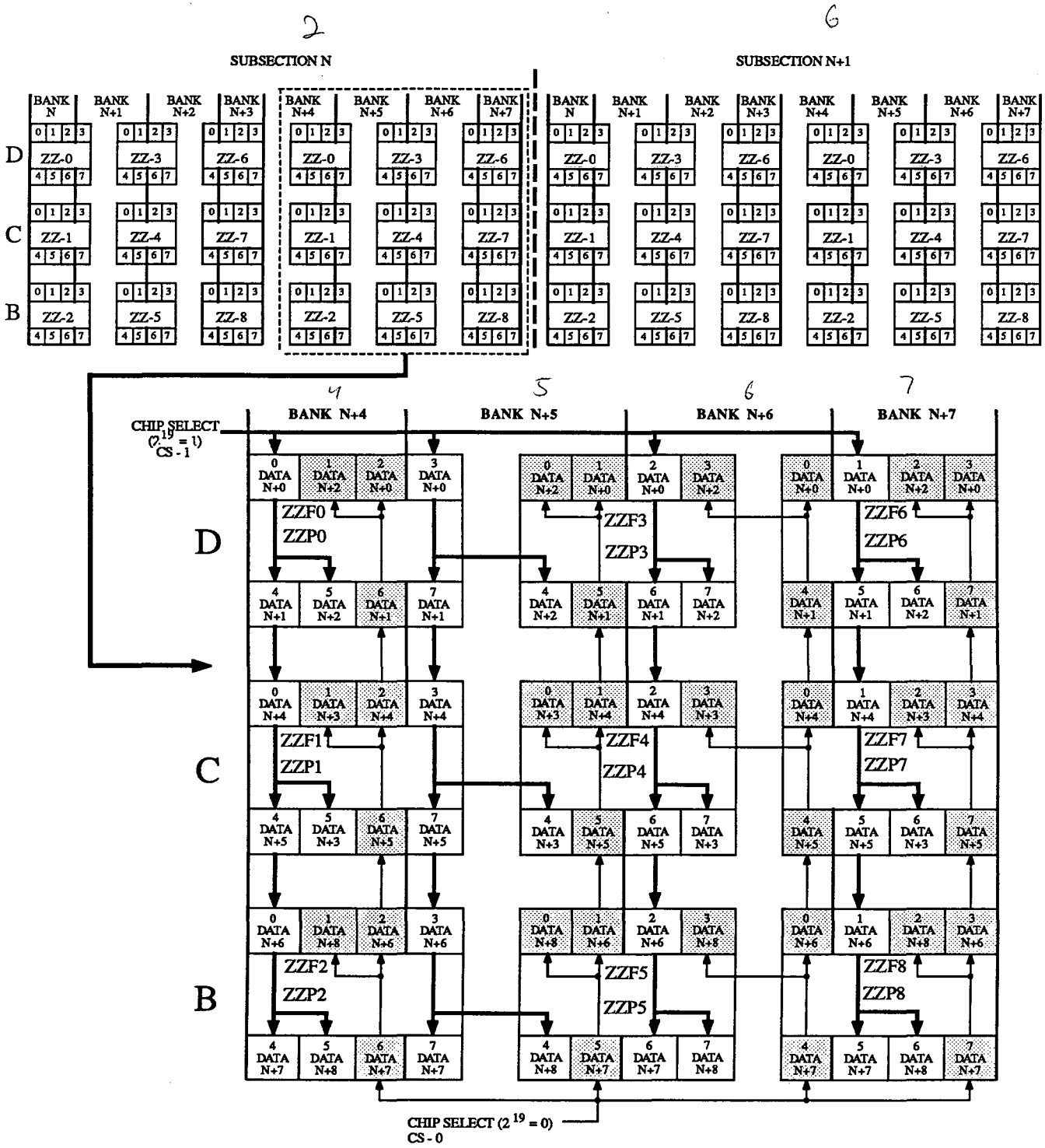
CRAY Y-MP MEMORY BOARD A/C SUBSECTION 1/5
BANKS (N + 4 - N + 7) (256K x 1) LOCATOR



NOTE: EACH BANK HAS 18 MEMORY CHIPS (256K x 1) WHICH IS DIVIDED INTO 9 DATA BITS PER MODULE (N+0 - N+8) AND TWO CHIP SELECTS (2 19= 0, 2 19= 1)

Hardware Trng.
A-8359 J.E.S.

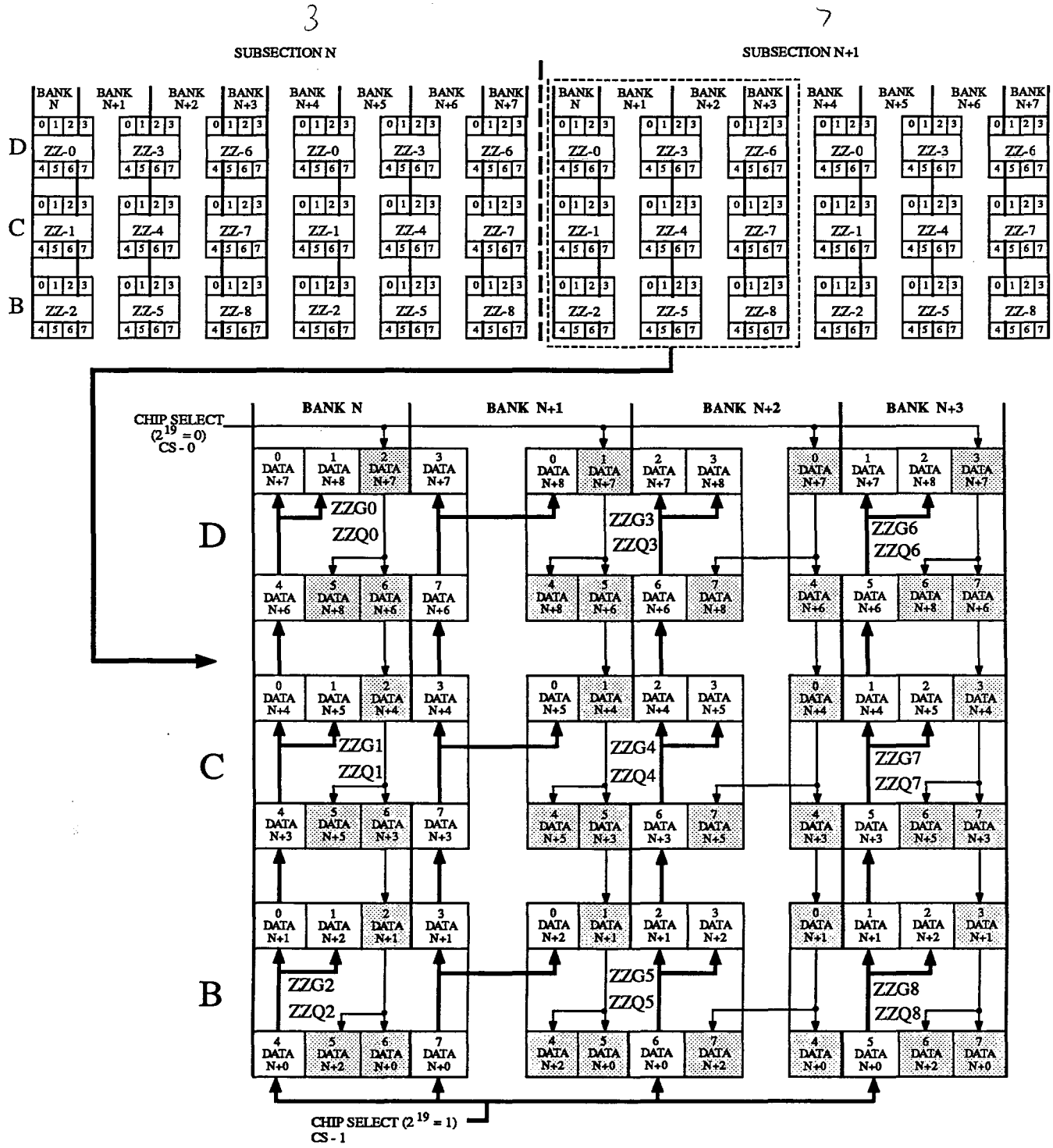
CRAY Y-MP MEMORY BOARD B/D SUBSECTION 2/6
BANKS (N - N + 3) (256K x 1) LOCATOR



NOTE: EACH BANK HAS 18 MEMORY CHIPS (256K x 1) WHICH IS DIVIDED INTO 9 DATA BITS PER MODULE (N+0 - N+8) AND TWO CHIP SELECTS ($2^{19} = 0, 2^{19} = 1$)

Hardware Trng. A-8360 J.E.S.

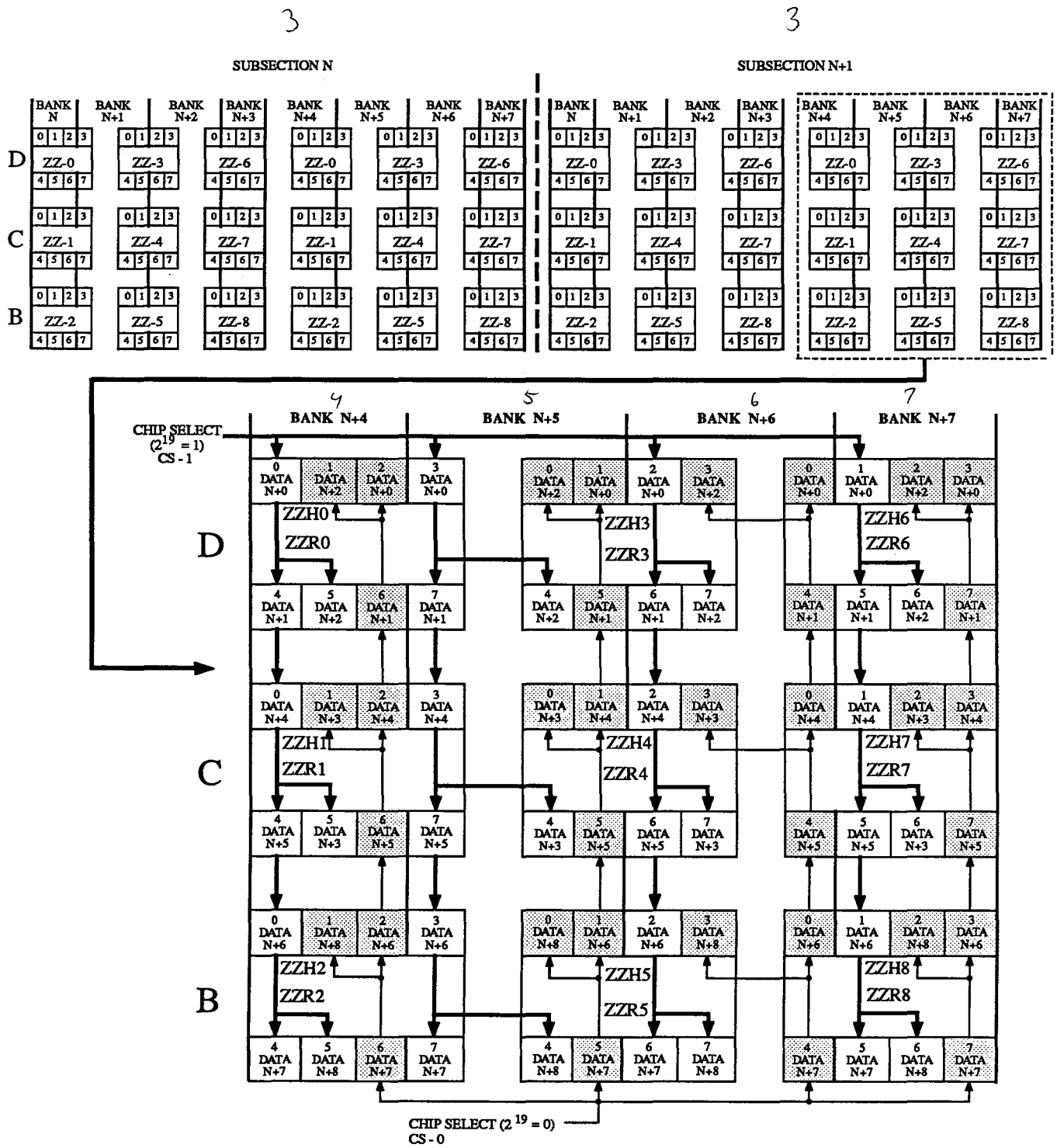
CRAY Y-MP MEMORY BOARD B/D SUBSECTION 2/6 BANKS (N + 4 - N + 7) (256K x 1) LOCATOR



NOTE: EACH BANK HAS 18 MEMORY CHIPS (256K x 1) WHICH IS DIVIDED INTO 9 DATA BITS PER MODULE (N+0 - N+8) AND TWO CHIP SELECTS ($2^{19} = 0$, $2^{19} = 1$)

Hardware Trng. A-8361 J.E.S.

CRAY Y-MP MEMORY BOARD B/D SUBSECTION 3/7
BANKS (N - N + 3) (256K x 1) LOCATOR



NOTE: EACH BANK HAS 18 MEMORY CHIPS (256K x 1) WHICH IS DIVIDED INTO 9 DATA BITS PER MODULE (N+0 - N+8) AND TWO CHIP SELECTS ($2^{19} = 0$, $2^{19} = 1$)

Hardware Trng. A-8362 J.E.S.

CRAY Y-MP MEMORY BOARD B/D SUBSECTION 3/7 BANKS (N + 4 - N + 7) (256K x 1) LOCATOR

CRAY Y-MP MODULE LOCATIONS

MEMORY DATA	MEMORY MODULE LOCATION Section 0	Section 1	Section 2	Section 3
Bits 2^0 - 2^8	Location 1	9	25	33
Bits 2^9 - 2^{17}	Location 2	10	26	34
Bits 2^{18} - 2^{26}	Location 3	11	27	35
Bits 2^{27} - 2^{35}	Location 4	12	28	36
Bits 2^{36} - 2^{44}	Location 5	13	29	37
Bits 2^{45} - 2^{53}	Location 6	14	30	38
Bits 2^{54} - 2^{62}	Location 7	15	31	39
Bits 2^{63} - 2^{71}	Location 8	16	32	40

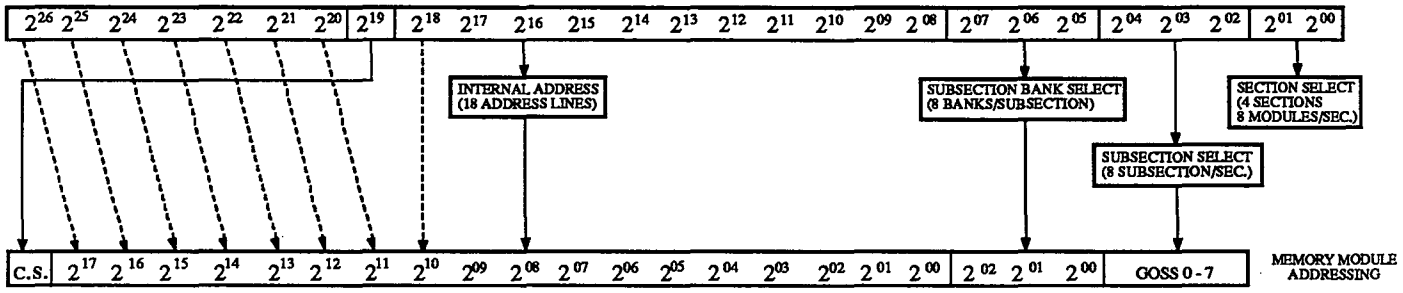
CPU NUMBER	LOCATION
0	Location 17
1	Location 18
2	Location 19
3	Location 20
4	Location 21
5	Location 22
6	Location 23
7	Location 24

MEMORY ADDRESS

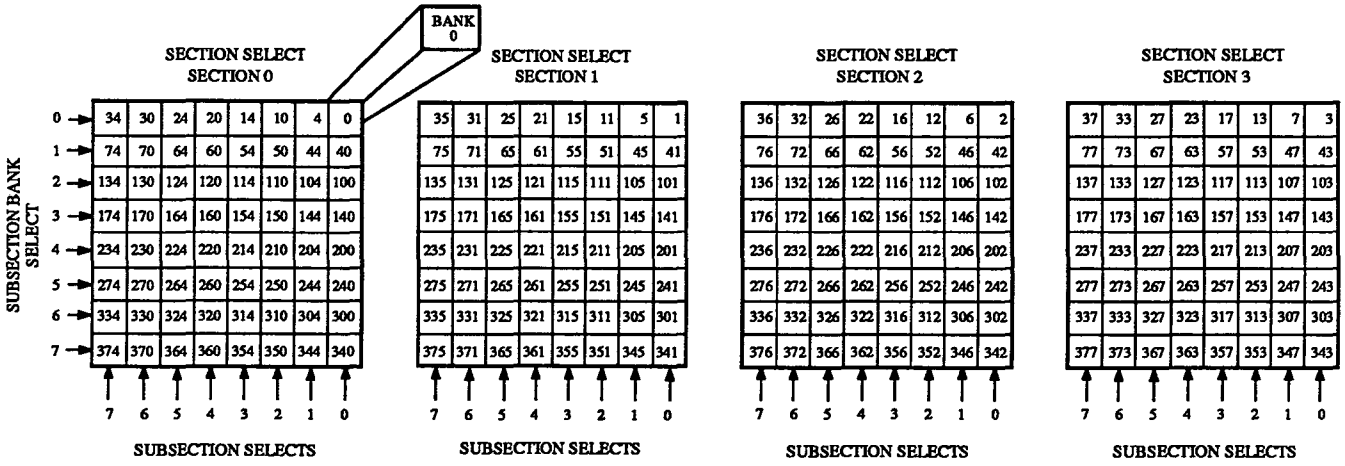
2^{26} 2^{25} 2^{24} 2^{23} 2^{22} 2^{21} 2^{20}	2^{19}	2^{18} 2^{17} 2^{16} 2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^9 2^8	2^7 2^6 2^5	2^4 2^3 2^2	2^1 2^0
X X X X X X X	X	X X X X X X X X X X X X	X X X	X X X	X X
2^{17} 2^{16} 2^{15} 2^{14} 2^{13} 2^{12} 2^{11}	C.S.	2^{10} 2^9 2^8 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0	2^2 2^1 2^0	0 - 7 GOSS	0 - 3 Sec.

Hardware Trng.
YM34/04 J.E.S.

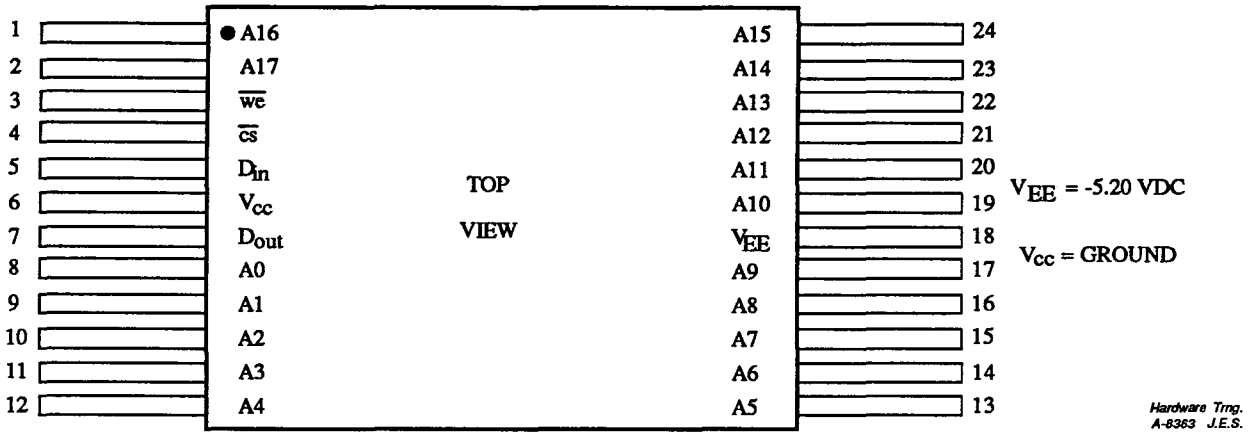
ADDRESS



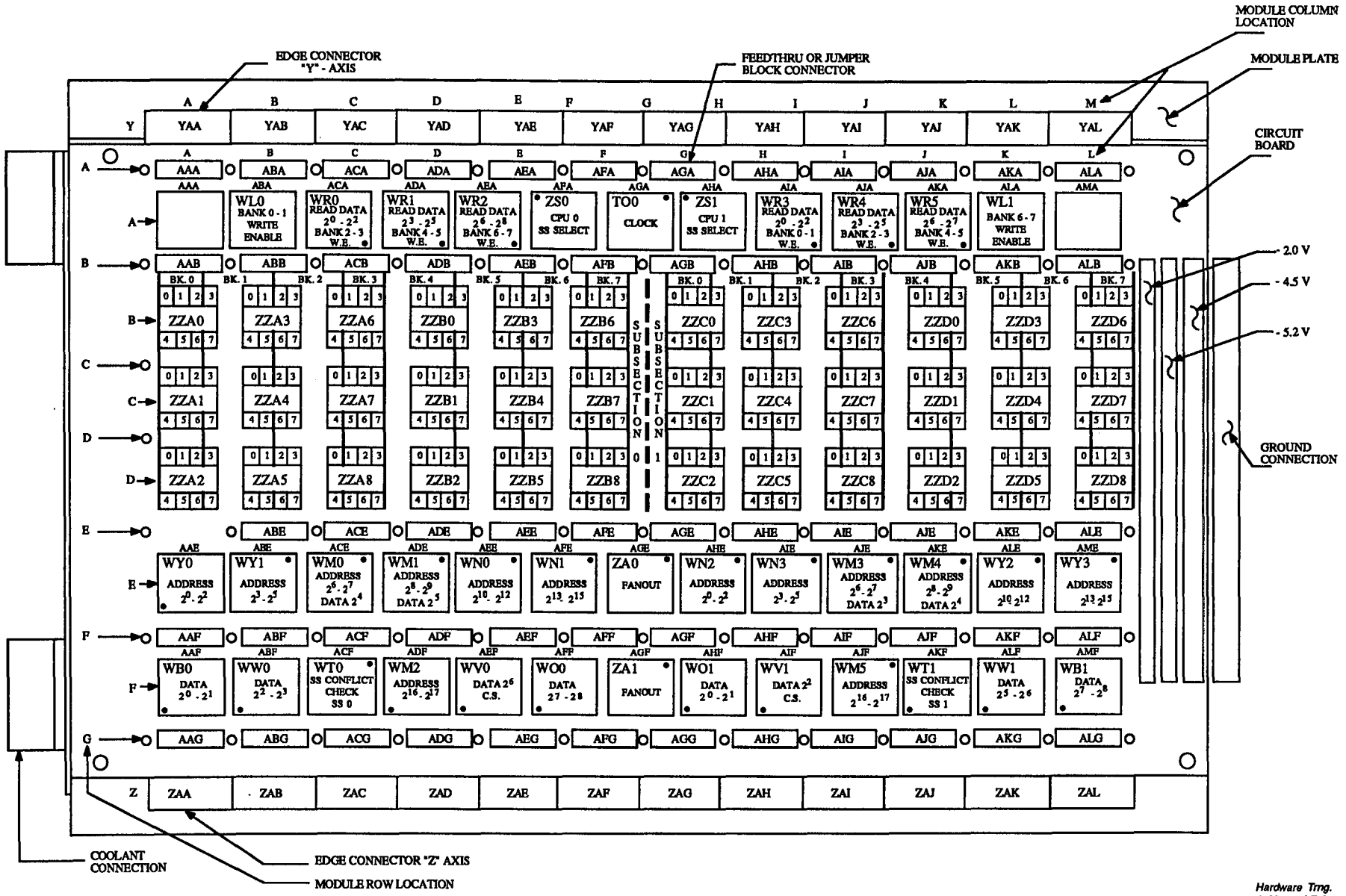
BANK/SUBSECTION LAYOUT



256K x 1 BIMOS MEMORY CHIP

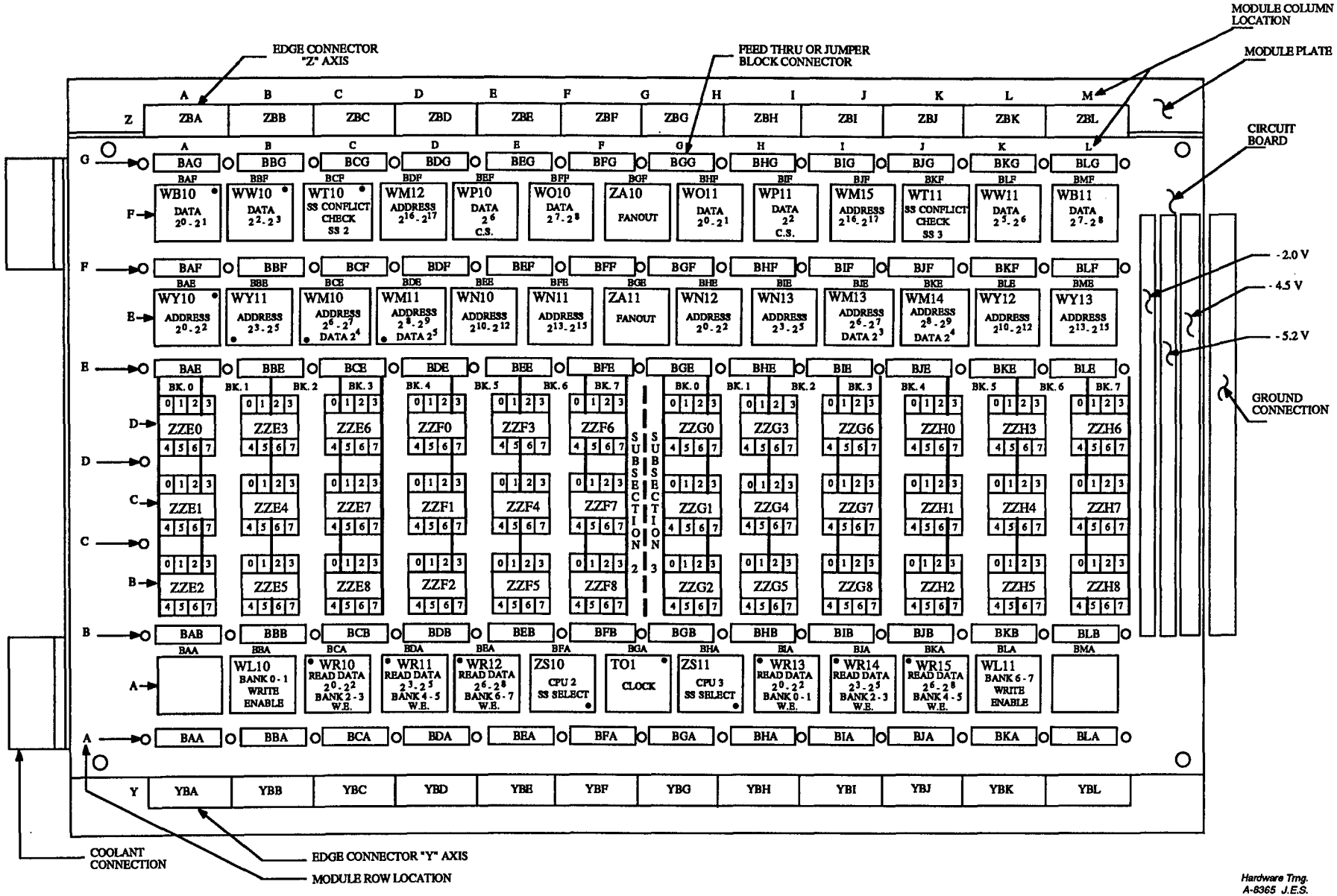


CRAY Y-MP MEMORY ADDRESSING

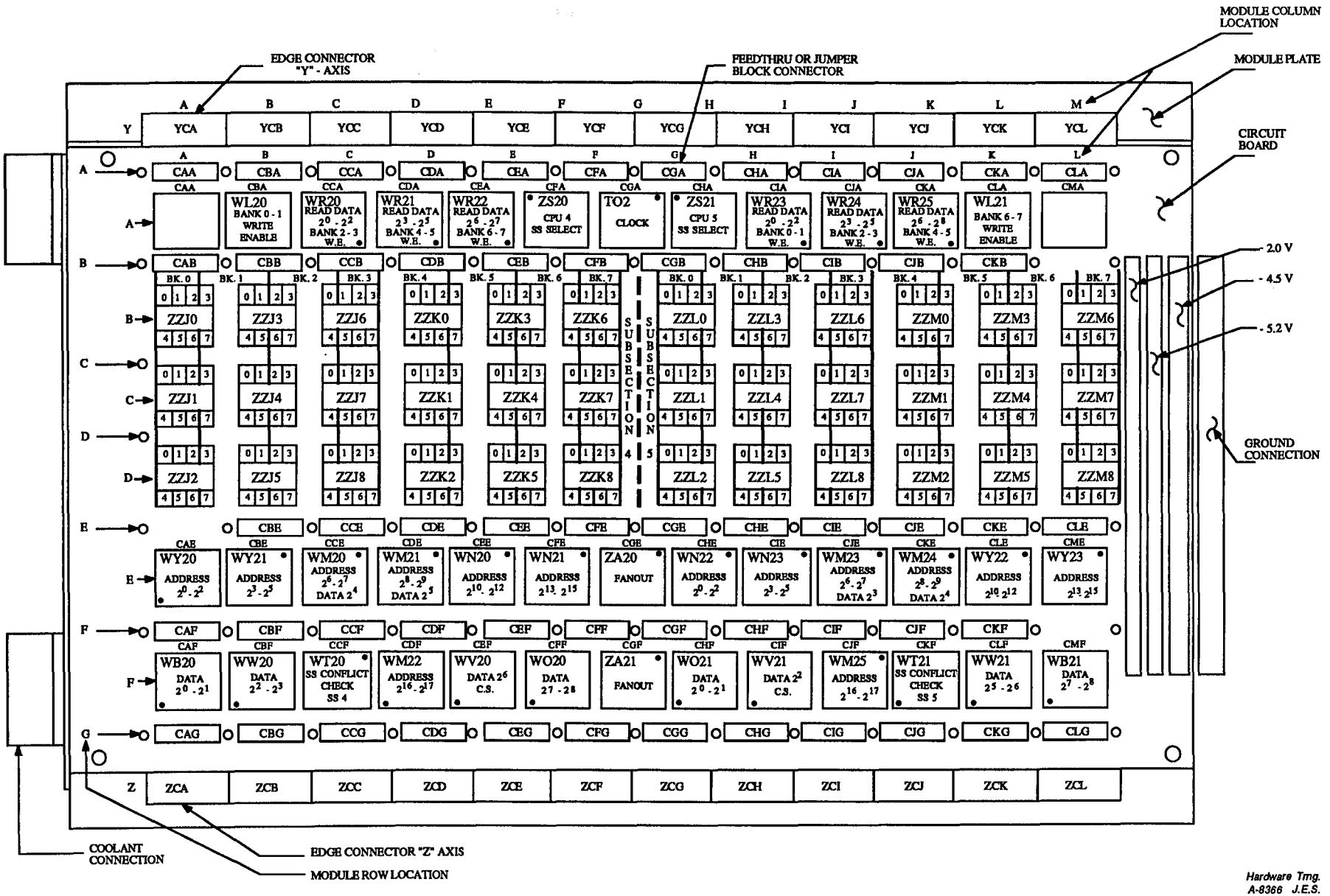


Hardware Trng.
A-8364 J.E.S.

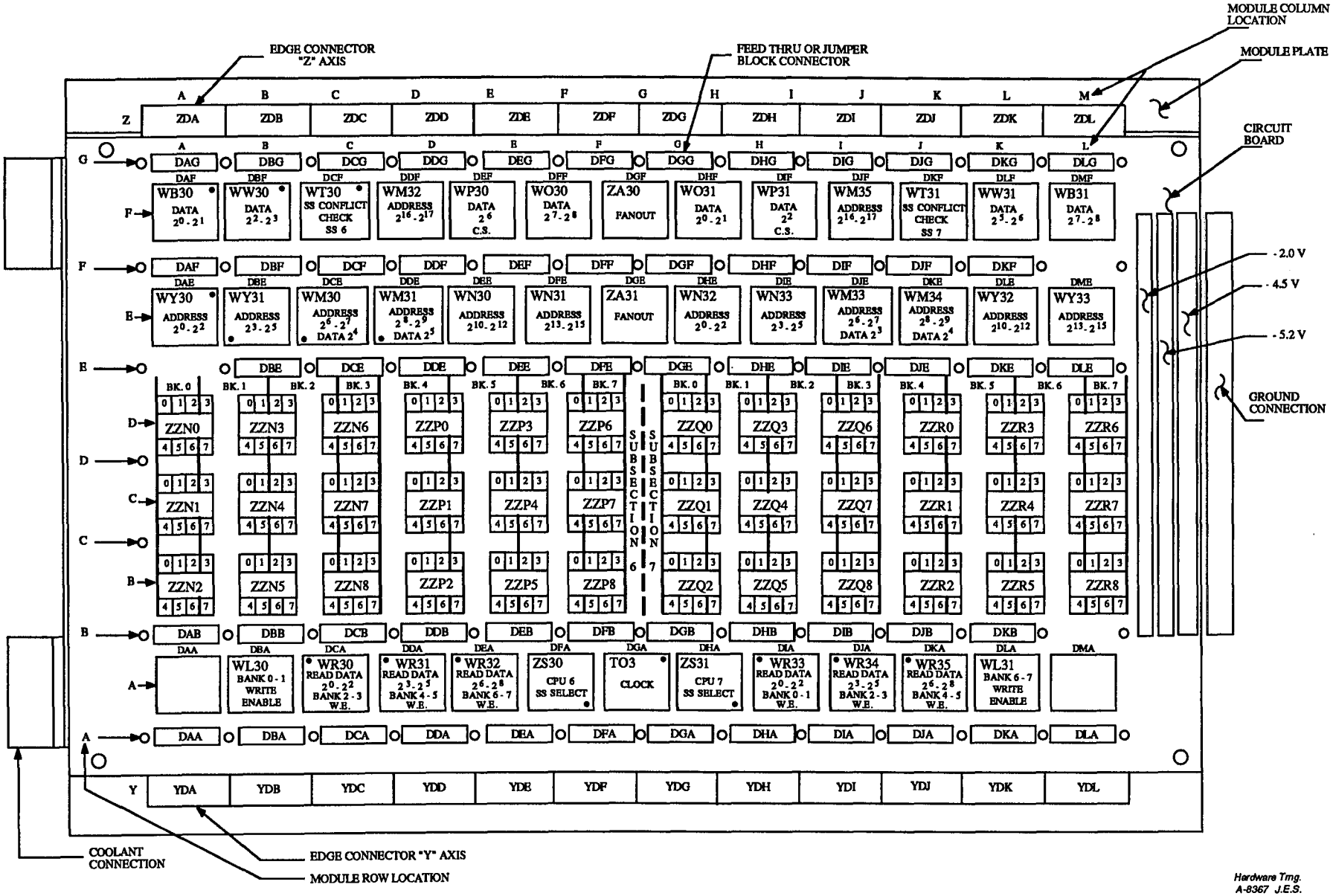
CRAY Y-MP 128MW MEMORY MAP
BOARD A



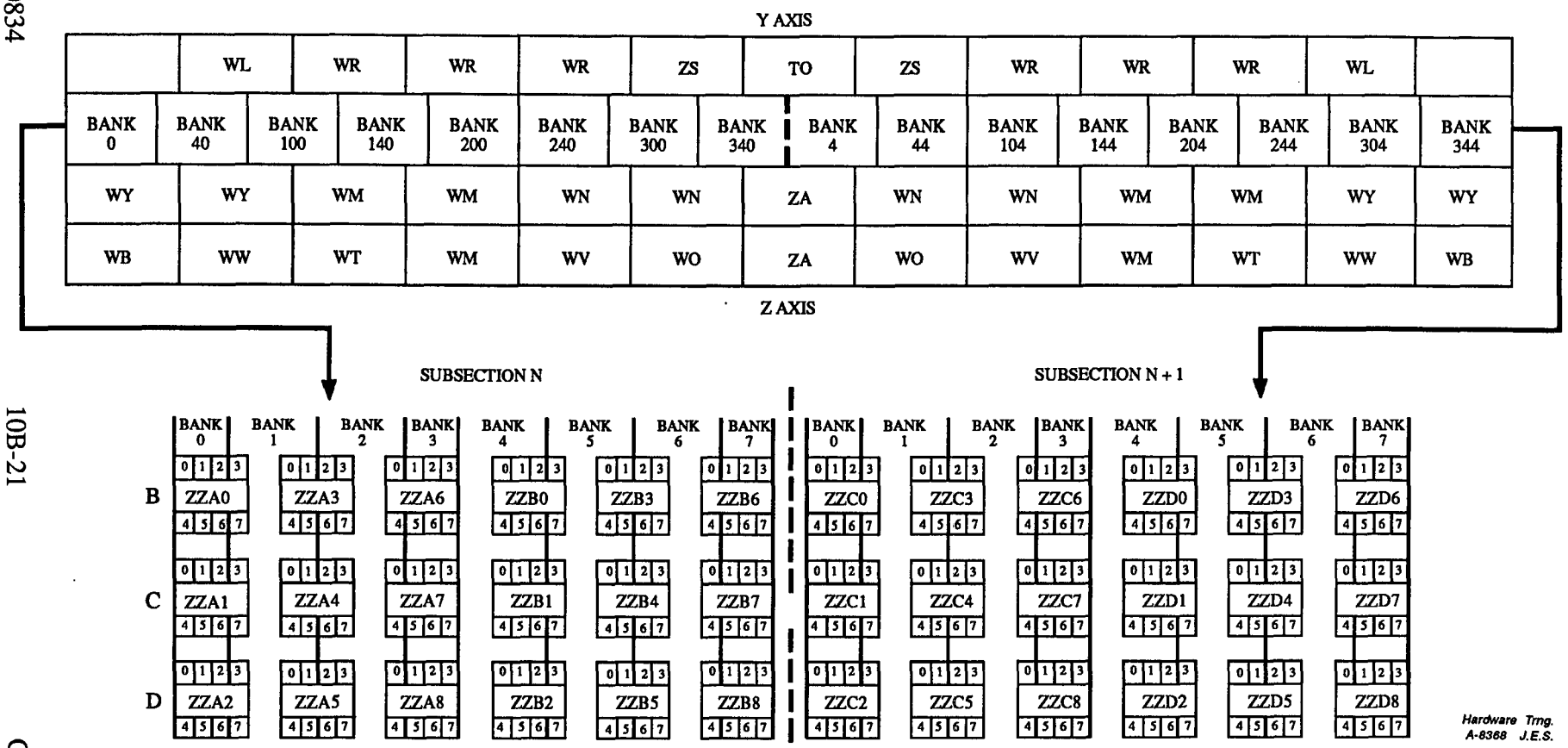
CRAY Y-MP 128MW MEMORY MAP
BOARD B



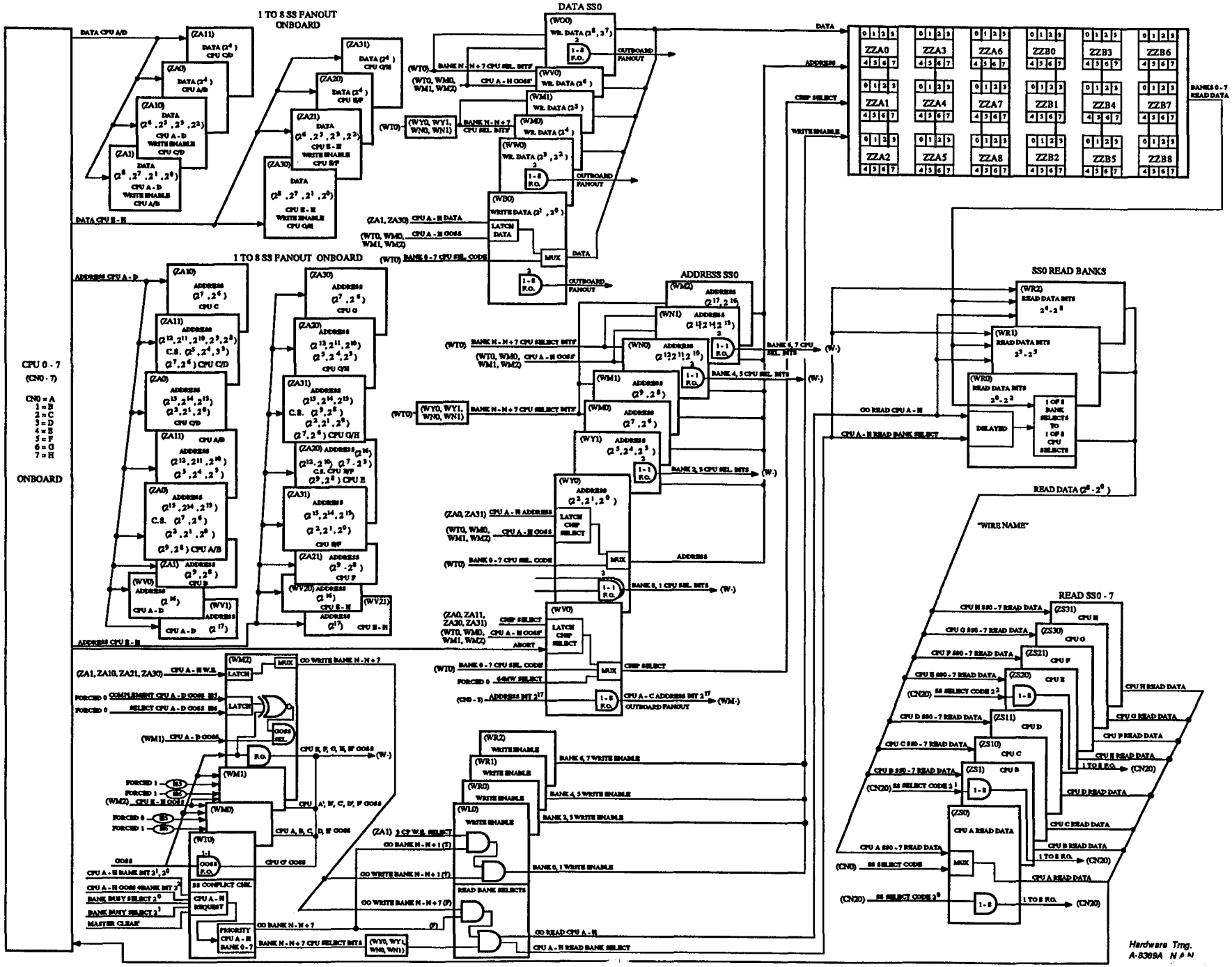
CRAY Y-MP 128MW MEMORY MAP
BOARD C



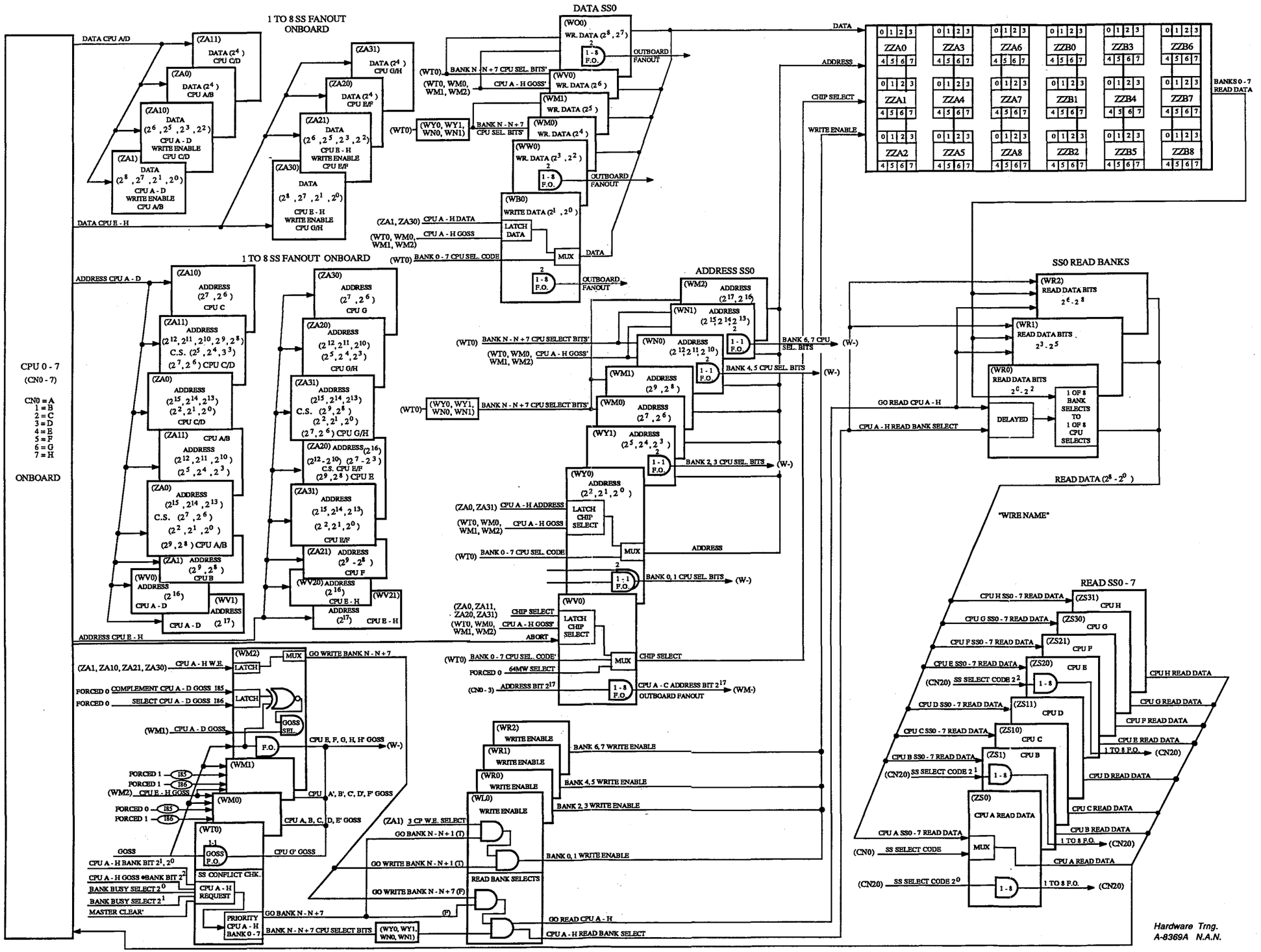
CRAY Y-MP 128MW MEMORY MAP
BOARD D



CRAY Y-MP BANK/SUBSECTION LAYOUT



CRAY Y-MP MEMORY (128MW) BLOCK DIAGRAM (256K x 1) SUBSECTION 0 CPU A - H



CRAY Y-MP MEMORY (128MW) BLOCK DIAGRAM (256K x 1) SUBSECTION 0 CPU A - H

ADDRESS BIT	ADDRESS ONBOARD FANOUT							
	CPU A	CPU B	CPU C	CPU D	CPU E	CPU F	CPU G	CPU H
2^0	ZA0 R27	ZA0 R24	ZA0 R21	ZA0 R18	ZA31 R11	ZA31 R8	ZA31 R5	ZA31 R2
2^1	ZA0 R26	ZA0 R23	ZA0 R20	ZA0 R17	ZA31 R10	ZA31 R7	ZA31 R4	ZA31 R1
2^2	ZA0 R25	ZA0 R22	ZA0 R19	ZA0 R16	ZA31 R9	ZA31 R6	ZA31 R3	ZA31 R0
2^3	ZA11 R11	ZA11 R8	ZA11 R5	ZA11 R2	ZA20 R27	ZA20 R24	ZA20 R21	ZA20 R18
2^4	ZA11 R10	ZA11 R7	ZA11 R4	ZA11 R1	ZA20 R26	ZA20 R23	ZA20 R20	ZA20 R17
2^5	ZA11 R9	ZA11 R6	ZA11 R3	ZA11 R0	ZA20 R25	ZA20 R22	ZA20 R19	ZA20 R16
2^6	ZA0 R28	ZA0 R30	ZA10 R32	ZA11 R32	ZA20 R28	ZA20 R30	ZA30 R32	ZA31 R32
2^7	ZA0 R29	ZA0 R31	ZA10 R33	ZA11 R33	ZA20 R29	ZA20 R31	ZA30 R33	ZA31 R33
2^8	ZA0 R32	ZA1 R32	ZA11 R28	ZA11 R30	ZA20 R32	ZA21 R32	ZA31 R16	ZA31 R18
2^9	ZA0 R33	ZA1 R33	ZA11 R29	ZA11 R31	ZA20 R33	ZA21 R33	ZA31 R17	ZA31 R19
2^{10}	ZA11 R27	ZA11 R24	ZA11 R21	ZA11 R18	ZA20 R11	ZA20 R8	ZA20 R5	ZA20 R2
2^{11}	ZA11 R26	ZA11 R23	ZA11 R20	ZA11 R17	ZA20 R10	ZA20 R7	ZA20 R4	ZA20 R1
2^{12}	ZA11 R25	ZA11 R22	ZA11 R19	ZA11 R16	ZA20 R9	ZA20 R6	ZA20 R3	ZA20 R0
2^{13}	ZA0 R11	ZA0 R8	ZA0 R5	ZA0 R2	ZA31 R20	ZA31 R23	ZA31 R26	ZA31 R29
2^{14}	ZA0 R10	ZA0 R7	ZA0 R4	ZA0 R1	ZA31 R21	ZA31 R24	ZA31 R27	ZA31 R30
2^{15}	ZA0 R9	ZA0 R6	ZA0 R3	ZA0 R0	ZA31 R22	ZA31 R25	ZA31 R28	ZA31 R31
2^{16}	WV0 R30	WV0 R31	WV0 R32	WV0 R33	WV20 R30	WV20 R31	WV20 R32	WV20 R33
2^{17}	WV1 R30	WV1 R31	WV1 R32	WV1 R33	WV21 R30	WV21 R31	WV21 R32	WV21 R33
CHIP SELECT	ZA0 R14	ZA0 R15	ZA11 R14	ZA11 R15	ZA20 R14	ZA20 R15	ZA31 R14	ZA31 R15
GO WRITE	ZA1	ZA1	ZA10	ZA10	ZA21	ZA21	ZA30	ZA30

DATA BIT	DATA ONBOARD FANOUT							
	CPU A	CPU B	CPU C	CPU D	CPU E	CPU F	CPU G	CPU H
$N+2^0$	ZA1 R16	ZA1 R18	ZA1 R20	ZA1 R22	ZA30 R15	ZA30 R13	ZA30 R11	ZA30 R9
$N+2^1$	ZA1 R17	ZA1 R19	ZA1 R21	ZA1 R23	ZA30 R14	ZA30 R12	ZA30 R10	ZA30 R8
$N+2^2$	ZA10 R0	ZA10 R2	ZA10 R4	ZA10 R6	ZA21 R16	ZA21 R18	ZA21 R20	ZA21 R22
$N+2^3$	ZA10 R1	ZA10 R3	ZA10 R5	ZA10 R7	ZA21 R17	ZA21 R19	ZA21 R21	ZA21 R23
$N+2^4$	ZA0 R12	ZA0 R13	ZA11 R12	ZA11 R13	ZA20 R12	ZA20 R13	ZA31 R12	ZA31 R13
$N+2^5$	ZA10 R22	ZA10 R20	ZA10 R18	ZA10 R16	ZA21 R6	ZA21 R4	ZA21 R2	ZA21 R0
$N+2^6$	ZA10 R23	ZA10 R21	ZA10 R19	ZA10 R17	ZA21 R7	ZA21 R5	ZA21 R3	ZA21 R1
$N+2^7$	ZA1 R6	ZA1 R4	ZA1 R2	ZA1 R0	ZA30 R22	ZA30 R20	ZA30 R18	ZA30 R16
$N+2^8$	ZA1 R7	ZA1 R5	ZA1 R3	ZA1 R1	ZA30 R23	ZA30 R21	ZA30 R19	ZA30 R17

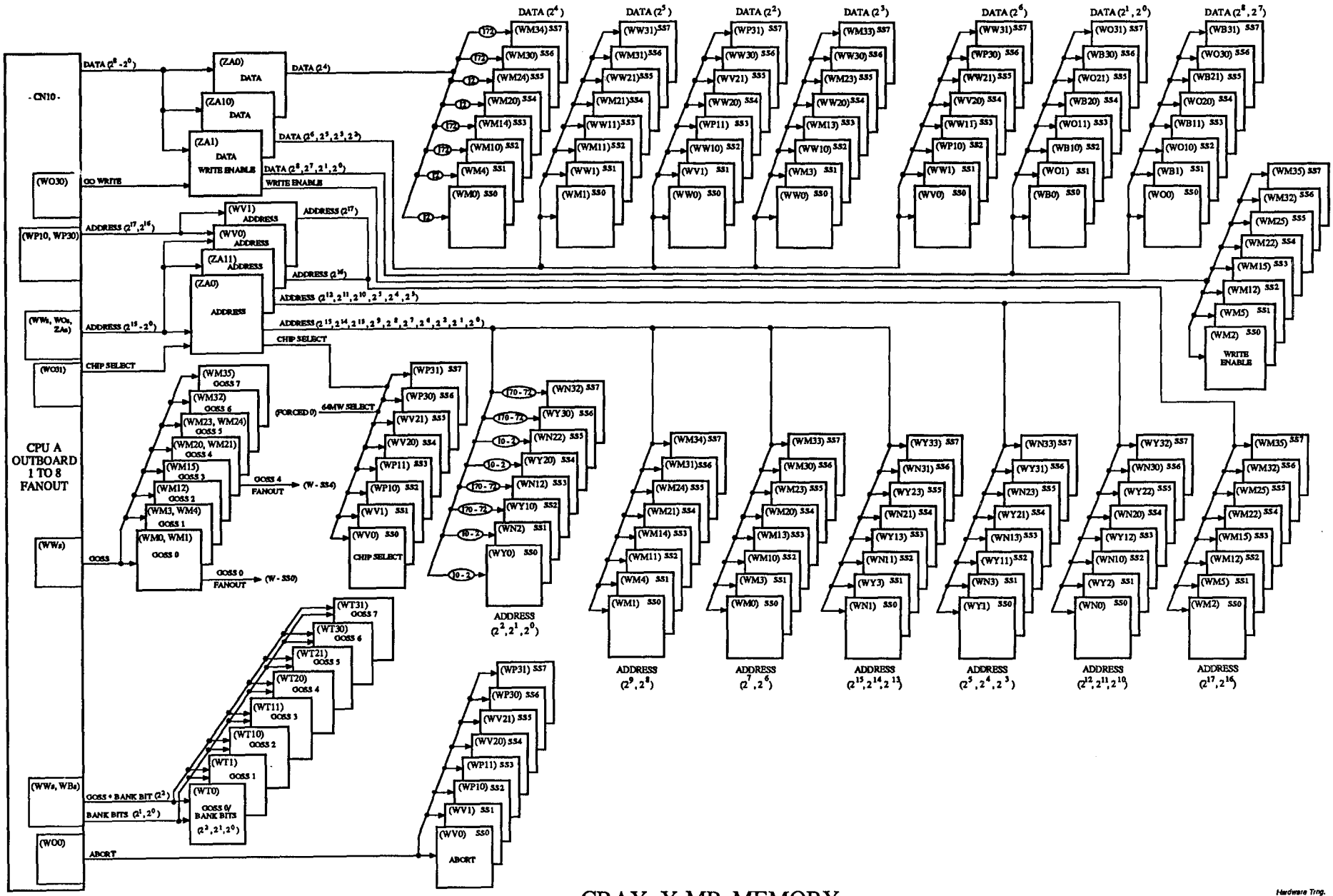
Hardware Trng.
A-8370A J.E.S.

CRAY Y-MP ONBOARD FANOUT ADDRESS/DATA

ADDRESS	CPU A	CPU B	CPU C	CPU D	CPU E	CPU F	CPU G	CPU H
2^0	WW0 MEM. 0	WW0 MEM. 1	WO0 MEM. 0	WO0 MEM. 1	WO0 MEM. 6	WO0 MEM. 7	WW0 MEM. 6	WW0 MEM. 7
2^1	WW10 MEM. 0	WW10 MEM. 1	WO10 MEM. 0	WO10 MEM. 1	WO10 MEM. 6	WO10 MEM. 7	WW10 MEM. 6	WW10 MEM. 7
2^2	WW20 MEM. 0	WW20 MEM. 1	WO20 MEM. 0	WO20 MEM. 1	WO20 MEM. 6	WO20 MEM. 7	WW20 MEM. 6	WW20 MEM. 7
2^3	WW30 MEM. 0	WW30 MEM. 1	WO30 MEM. 0	WO30 MEM. 1	WO30 MEM. 6	WO30 MEM. 7	WW30 MEM. 6	WW30 MEM. 7
2^4	WO0 MEM. 0	WO0 MEM. 1	WO1 MEM. 0	WO1 MEM. 1	WO1 MEM. 6	WO1 MEM. 7	WO0 MEM. 6	WO0 MEM. 7
2^5	WO10 MEM. 0	WO10 MEM. 1	WO11 MEM. 0	WO11 MEM. 1	WO11 MEM. 6	WO11 MEM. 7	WO10 MEM. 6	WO10 MEM. 7
2^6	WO20 MEM. 0	WO20 MEM. 1	WO21 MEM. 0	WO21 MEM. 1	WO21 MEM. 6	WO21 MEM. 7	WO20 MEM. 6	WO20 MEM. 7
2^7	WO30 MEM. 0	WO30 MEM. 1	WO30 MEM. 2	WO30 MEM. 3	WO30 MEM. 4	WO30 MEM. 5	WO30 MEM. 6	WO30 MEM. 7
2^8	ZA1 MEM. 0	ZA1 MEM. 1	ZA1 MEM. 2	ZA1 MEM. 3	ZA1 MEM. 4	ZA1 MEM. 5	ZA1 MEM. 6	ZA1 MEM. 7
2^9	ZA10 MEM. 0	ZA10 MEM. 1	ZA10 MEM. 2	ZA10 MEM. 3	ZA10 MEM. 4	ZA10 MEM. 5	ZA10 MEM. 6	ZA10 MEM. 7
2^{10}	ZA21 MEM. 0	ZA21 MEM. 1	ZA21 MEM. 2	ZA21 MEM. 3	ZA21 MEM. 4	ZA21 MEM. 5	ZA21 MEM. 6	ZA21 MEM. 7
2^{11}	ZA30 MEM. 0	ZA30 MEM. 1	ZA30 MEM. 2	ZA30 MEM. 3	ZA30 MEM. 4	ZA30 MEM. 5	ZA30 MEM. 6	ZA30 MEM. 7
2^{12}	WO31 MEM. 0	WO31 MEM. 1	WO31 MEM. 2	WO31 MEM. 3	WO31 MEM. 4	WO31 MEM. 5	WO31 MEM. 6	WO31 MEM. 7
2^{13}	WO1 MEM. 0	WO1 MEM. 1	WW1 MEM. 0	WW1 MEM. 1	WW1 MEM. 6	WW1 MEM. 7	WO1 MEM. 6	WO1 MEM. 7
2^{14}	WO11 MEM. 0	WO11 MEM. 1	WW11 MEM. 0	WW11 MEM. 1	WW11 MEM. 6	WW11 MEM. 7	WO11 MEM. 6	WO11 MEM. 7
2^{15}	WO21 MEM. 0	WO21 MEM. 1	WW21 MEM. 0	WW21 MEM. 1	WW21 MEM. 6	WW21 MEM. 7	WO21 MEM. 6	WO21 MEM. 7
2^{16}	WP10, WP30 MEM. 0	WP10, WP30 MEM. 1	WP10, WP30 MEM. 2	WP10, WP30 MEM.3	WP10, WP30 MEM. 7	WP10, WP30 MEM. 6	WP10, WP30 MEM. 5	WP10, WP30 MEM. 4
2^{17}	WP11, WP31 MEM. 0	WP11, WP31 MEM. 1	WP11, WP31 MEM. 2	WP11, WP31 MEM.3	WP11, WP31 MEM. 7	WP11, WP31 MEM. 6	WP11, WP31 MEM. 5	WP11, WP31 MEM. 4
CHIP SELECT	WO31 MEM. 0	WO31 MEM. 1	WW31 MEM. 0	WW31 MEM. 1	WW31 MEM. 6	WW31 MEM. 7	WO31 MEM. 6	WO31 MEM. 7
WRITE REFERENCE	WO30 MEM. 2	WO30 MEM. 3	WO31 MEM. 2	WO31 MEM.3	WO31 MEM. 4	WO31 MEM. 5	WO3O MEM. 4	WO30 MEM. 5

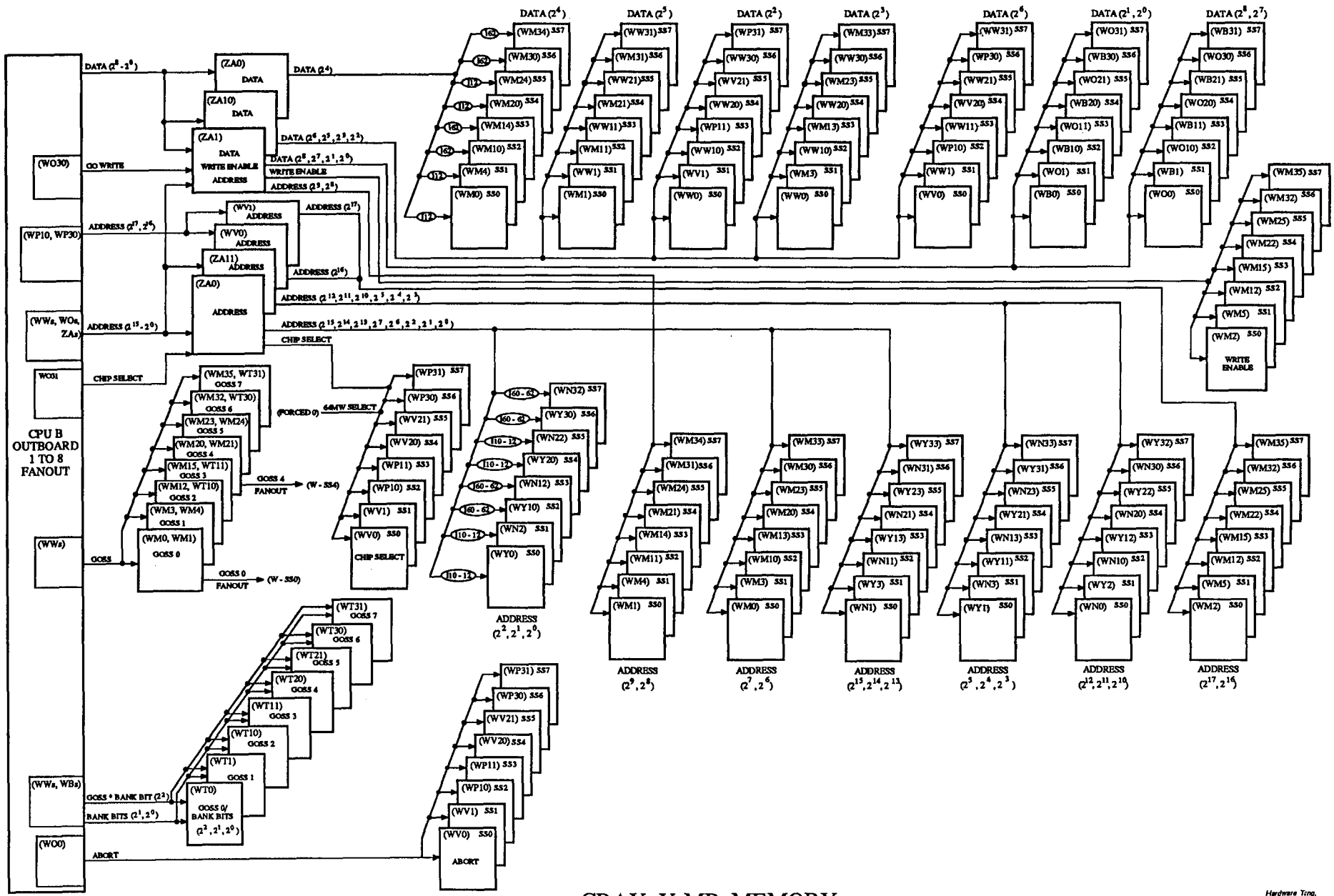
Hardware Trng.
A-8371 N.A.N.

CRAY Y-MP 1 TO 8 ADDRESS OUTBOARD FANOUT



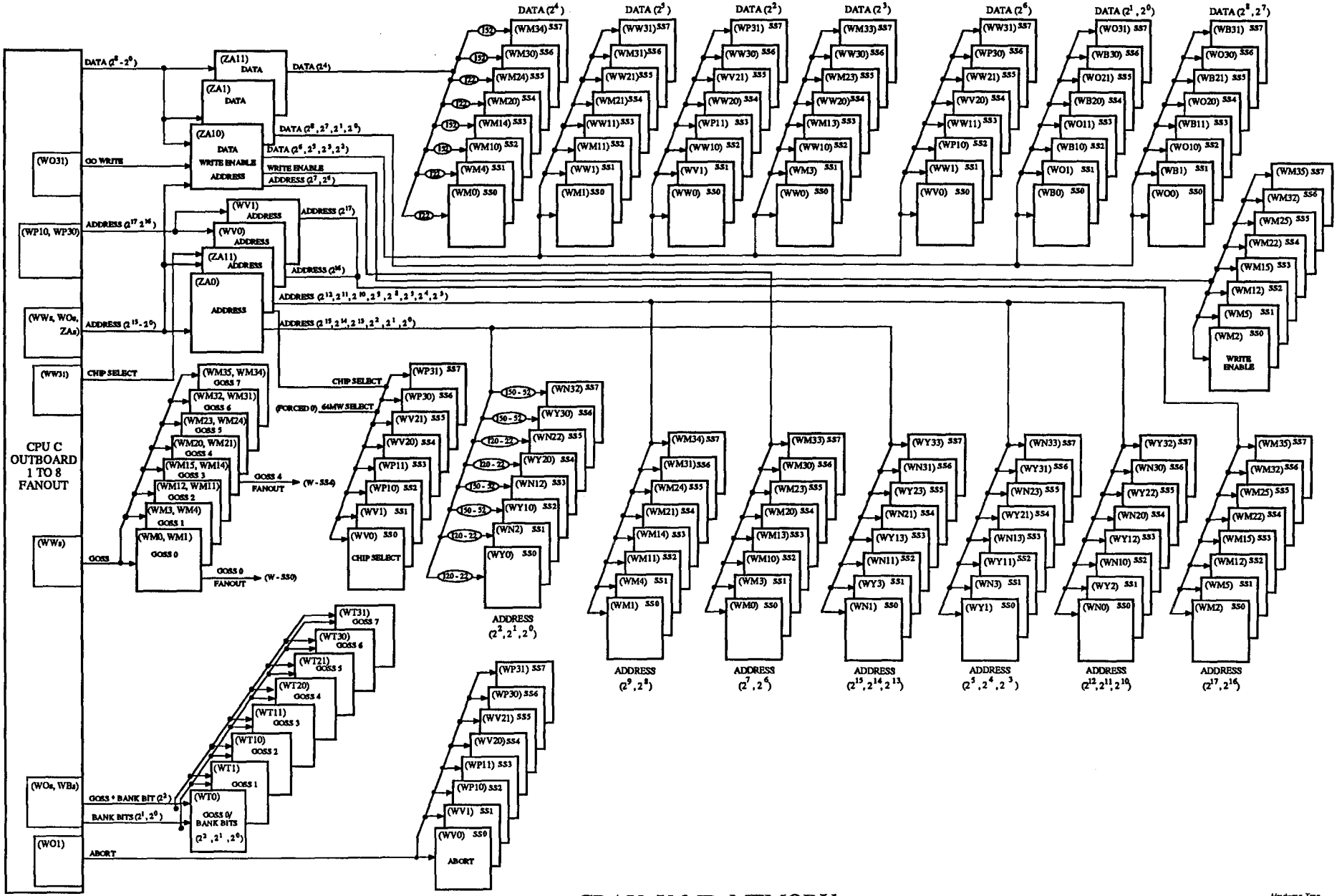
CRAY Y-MP MEMORY
CPU A 1 TO 8 ONBOARD SUBSECTION FANOUT

Hardware Trng.
A-8372A N.A.N.



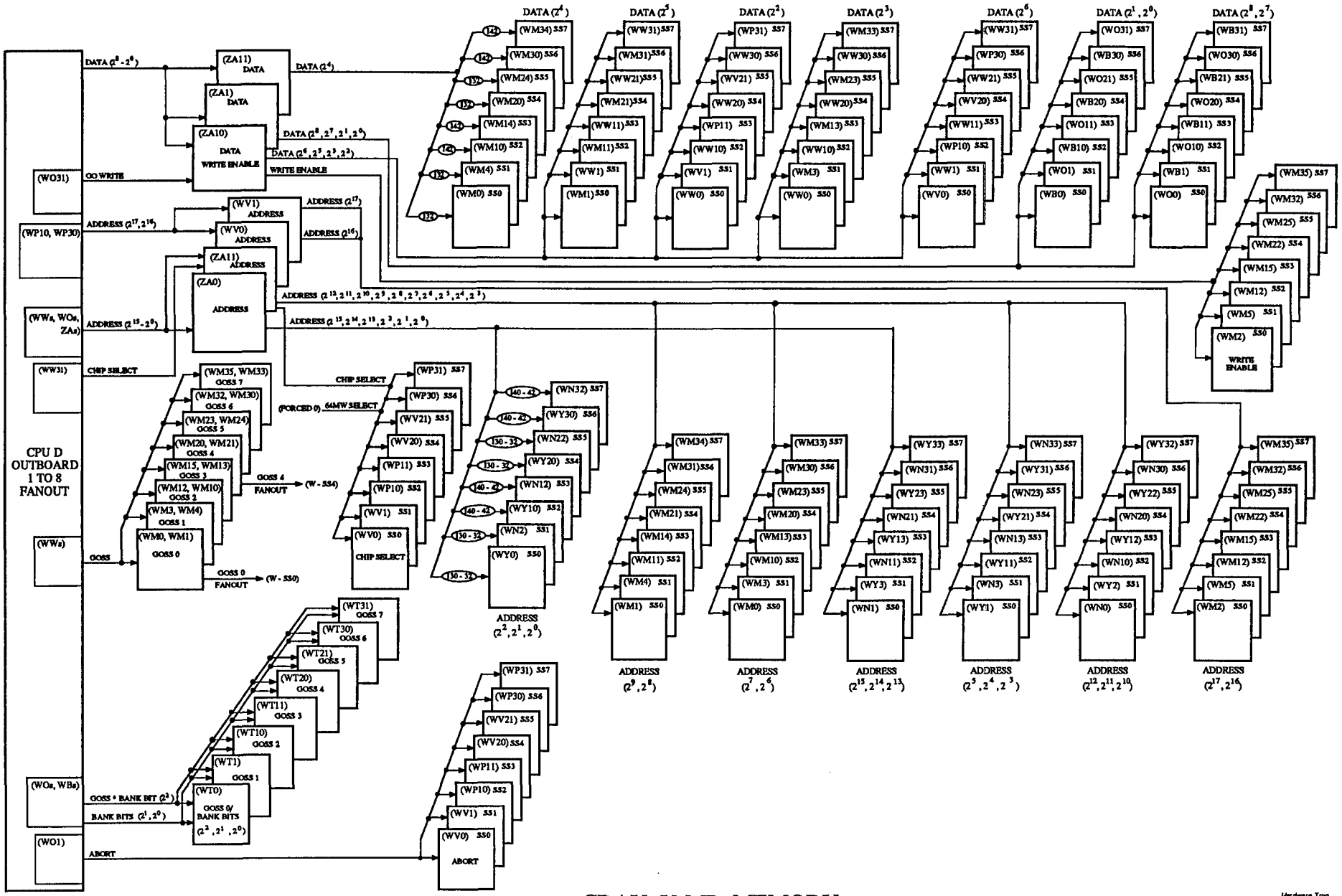
CRAY Y-MP MEMORY
CPU B 1 TO 8 ONBOARD SUBSECTION FANOUT

Hardware Trng.
A-8373A N.A.N.



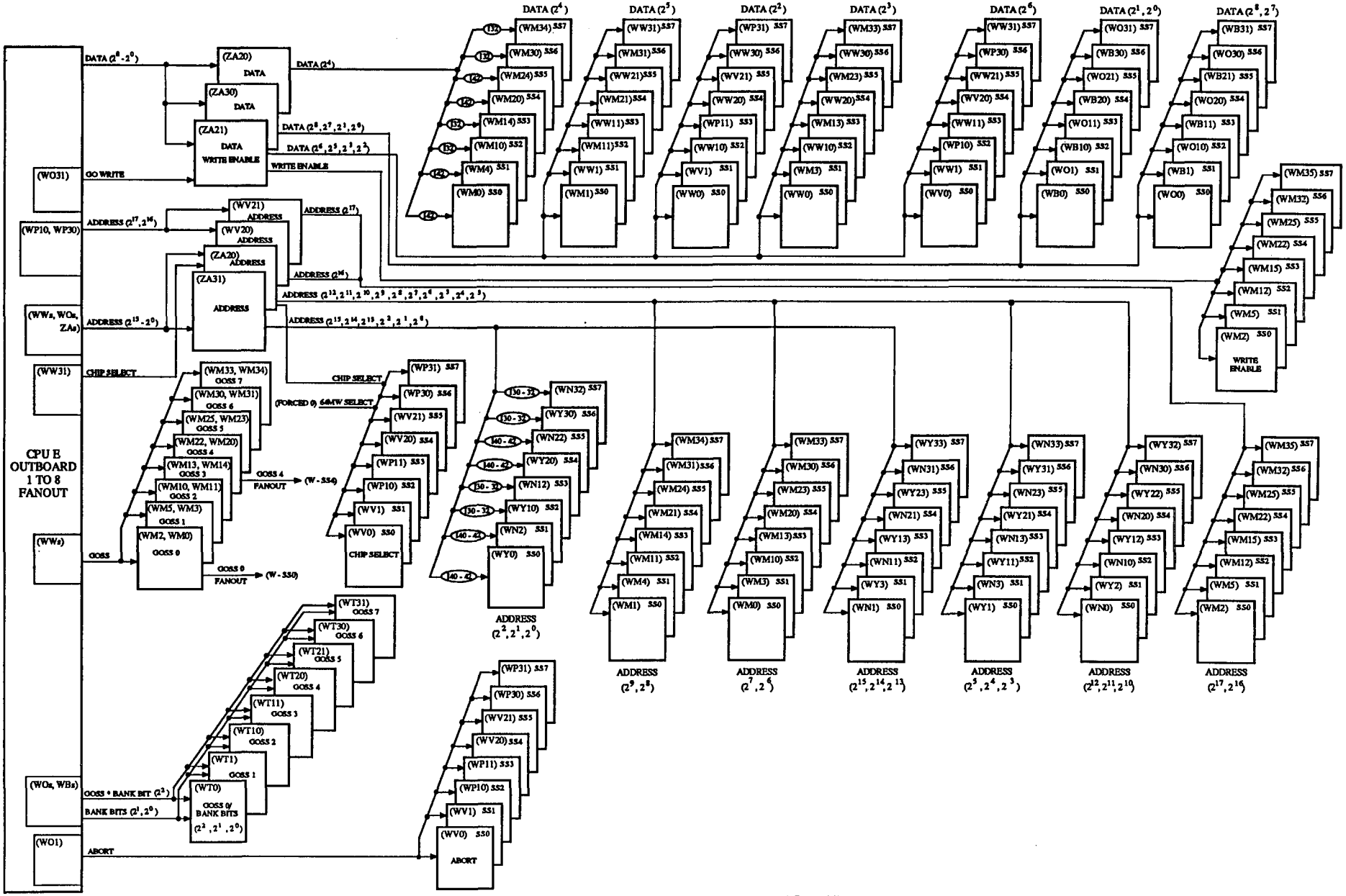
CRAY Y-MP MEMORY
CPU C 1 TO 8 ONBOARD SUBSECTION FANOUT

Hardware Trng.
A-8374A N.A.N.



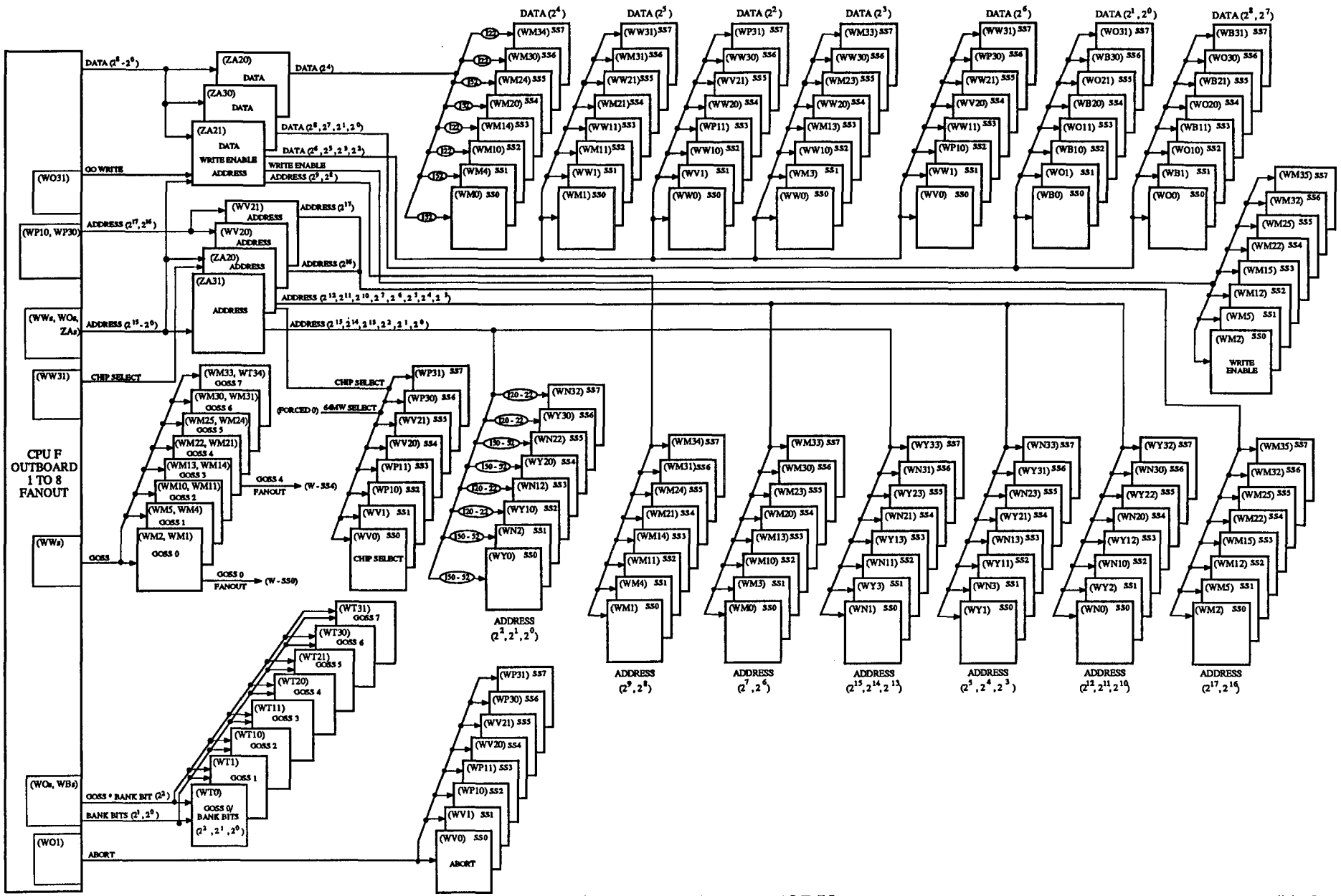
CRAY Y-MP MEMORY
CPU D 1 TO 8 ONBOARD SUBSECTION FANOUT

Hardware Tmg.
A-8375A N.A.N.



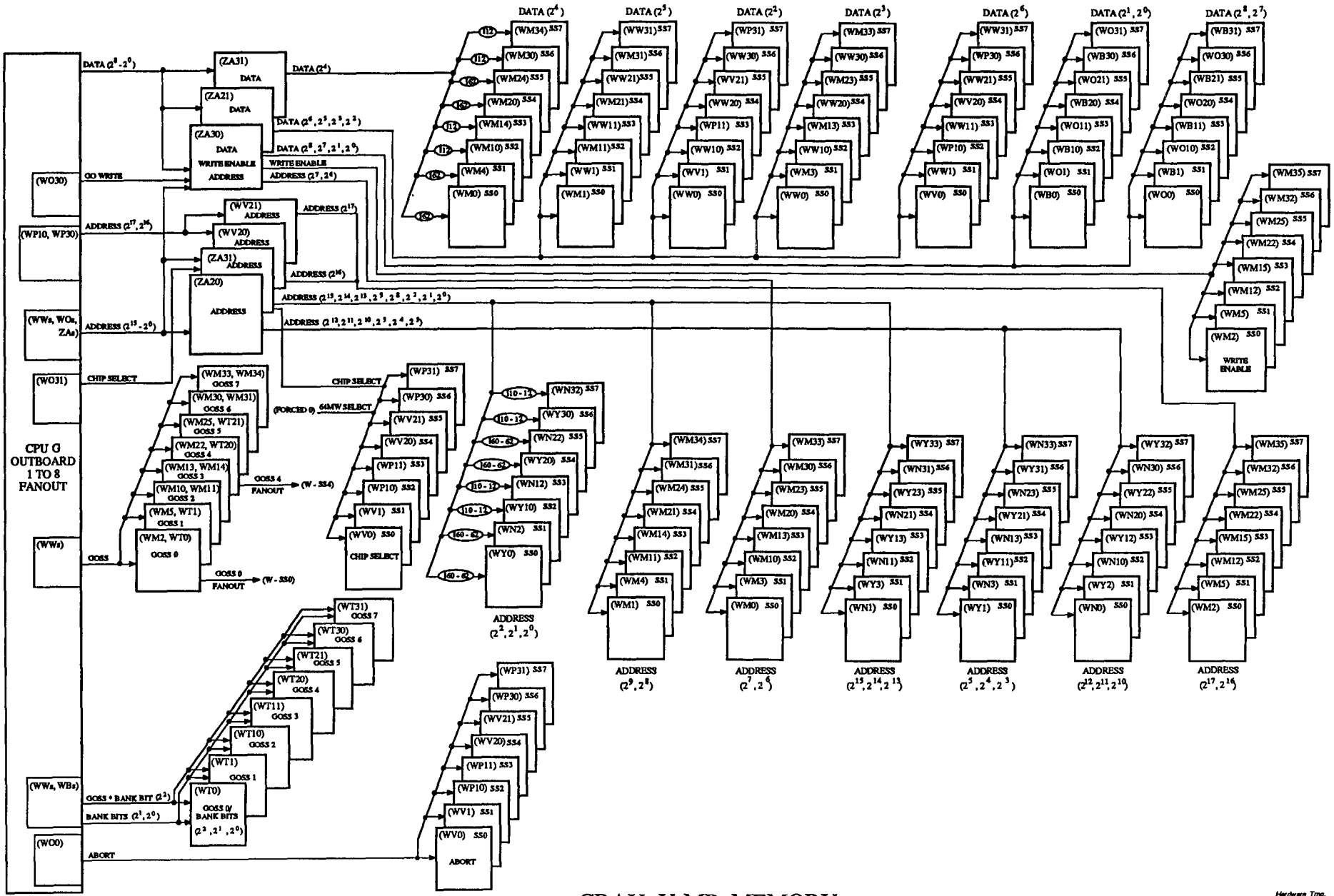
CRAY Y-MP MEMORY
CPU E 1 TO 8 ONBOARD SUBSECTION FANOUT

Hardware Trng.
A-8376A N.A.N.



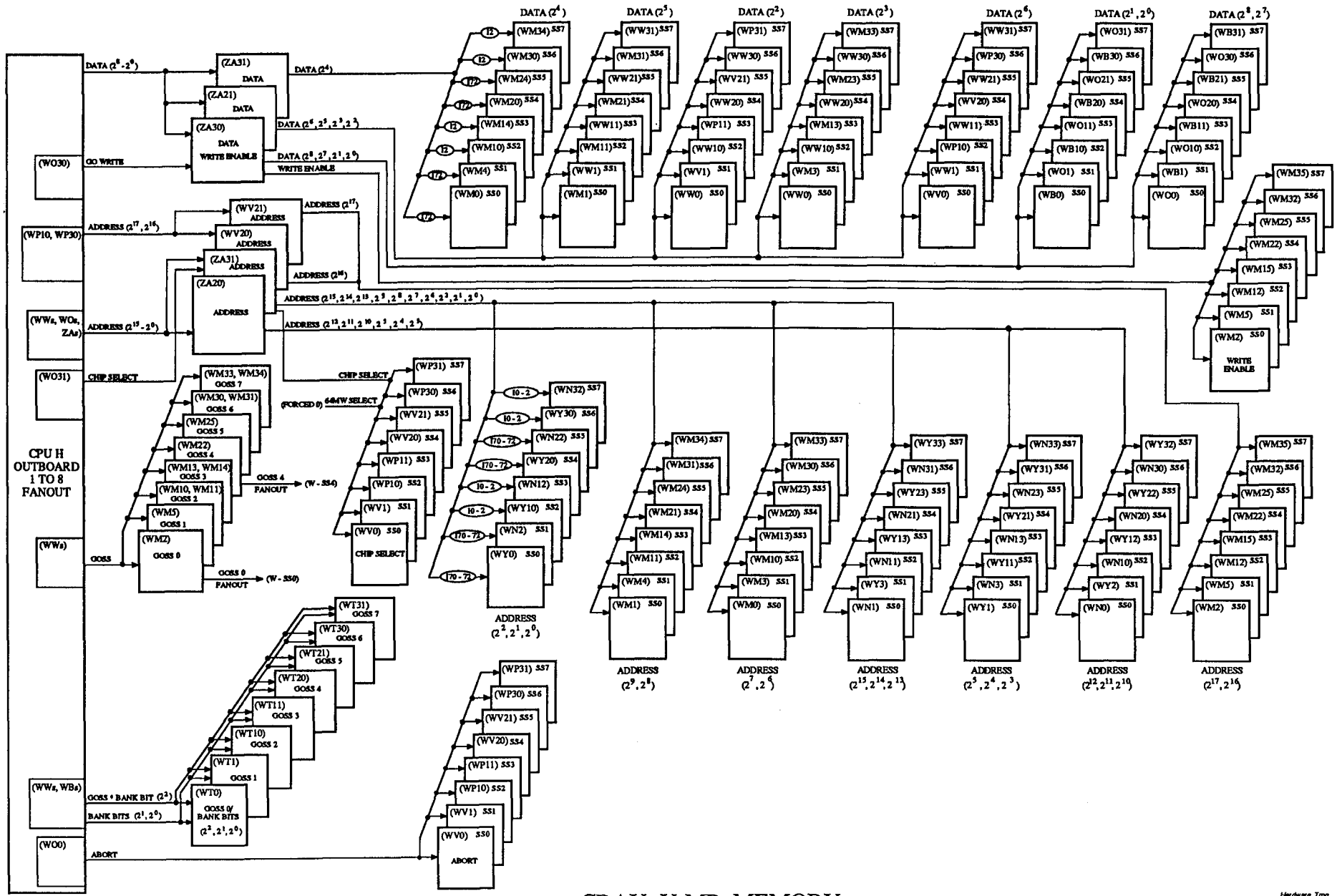
CRAY Y-MP MEMORY
CPU F 1 TO 8 ONBOARD SUBSECTION FANOUT

Hardware Tmg.
A-8377A N.A.N.



CRAY Y-MP MEMORY
CPU G 1 TO 8 ONBOARD SUBSECTION FANOUT

Hardware Trng.
A-8378A N.A.N.



CRAY Y-MP MEMORY
CPU H 1 TO 8 ONBOARD SUBSECTION FANOUT

Hardware Trng.
A-8375A N.A.N.

OBJECTIVES - Cray Y-MP CPU Hardware

Upon completion of this unit the student will be able to:

- Describe the overall specifications of the CPU module
- Determine the failing CPU module location, and option type, given the failing instruction or operation
- Describe the main function and differences of each specific unit of the CPU module
- Define with respect to time, utilize the control signals, and know where they are used
- Trace operands or data through the various units of the CPU module to generate the specific Boolean terms

CRAY Y-MP 8/32 MEMORY CONTROL

The CRAY Y-MP memory control is performed on the (Y-) options. There are 60 (Y-) options per CPU module, some of which are shared across all of the CPUs modules.

The memory control function is to resolve Subsection conflicts on the CPU level and Simultaneous Bank conflicts among the CPUs. Another function of the memory control is to pass the address and data along with the controls to the proper section in memory. The memory control requires so much logic because of the number of places that any given reference can go to. For example, CPU 0 could go to 1 of 4 sections, and within each section to 1 of 8 subsections, and within each subsection to 1 of 8 banks.

Each CPU has its own path to memory. However, this path can be separated into the four sections and not cause a conflict. When more than one port wants the same section, it is referred to as Subsection conflict and is resolved by the Port A, B, C, and D priorities. Port D is used by Fetch and has the highest priority. Ports A, B, and C with and odd increment would go first. I/O uses Port D when there are no Subsection conflicts or when an I/O Timeout occurs. I/O Timeout occurs when a counter has been enabled for a count of 37_8; a Subsection conflict will Enable the counter.

Once the CPU reference has determined the section, the subsection is then selected. Within the subsection the CPU can run into a conflict or competition for a specific bank. This occurrence is called a Simultaneous Bank conflict. A preset priority scheme determines which CPU will get to use the bank. The priority scheme allows each CPU to be first somewhere in memory, depending upon which section and subsection is being accessed.

The priorities are broken into CPU letters (A - H) where CPU (A) has highest priority and CPU (H) has the lowest priority. This priority is created by wiring the CPU module into the memory module such that depending on the reference to memory, CPU 0 can become CPU (A - H). For example, if CPU 0 were to go to Section 0, Subsection 0, it would become CPU (A) or if CPU 0 were to go to Section 0, Subsection 2, it would become CPU (H) , or last priority. The diagram below shows all combinations.

SECTION 0

PRIORITIES	a	b	c	d	e	f	g	h
	CPU	CPU	CPU	CPU	CPU	CPU	CPU	CPU
SS0	0	1	2	3	7	6	5	4
SS1	0	1	2	3	7	6	5	4
SS2	4	5	6	7	3	2	1	0
SS3	4	5	6	7	3	2	1	0
SS4	0	1	2	3	7	6	5	4
SS5	0	1	2	3	7	6	5	4
SS6	4	5	6	7	3	2	1	0
SS7	4	5	6	7	3	2	1	0

SECTION 1

PRIORITIES	a	b	c	d	e	f	g	h
	CPU	CPU	CPU	CPU	CPU	CPU	CPU	CPU
SS0	1	2	3	0	4	7	6	5
SS1	1	2	3	0	4	7	6	5
SS2	5	6	7	4	0	3	2	1
SS3	5	6	7	4	0	3	2	1
SS4	1	2	3	0	4	7	6	5
SS5	1	2	3	0	4	7	6	5
SS6	5	6	7	4	0	3	2	1
SS7	5	6	7	4	0	3	2	1

SECTION 2

PRIORITIES	a	b	c	d	e	f	g	h
	CPU	CPU	CPU	CPU	CPU	CPU	CPU	CPU
SS0	2	3	0	1	5	4	7	6
SS1	2	3	0	1	5	4	7	6
SS2	6	7	4	5	1	0	3	2
SS3	6	7	4	5	1	0	3	2
SS4	2	3	0	1	5	4	7	6
SS5	2	3	0	1	5	4	7	6
SS6	6	7	4	5	1	0	3	2
SS7	6	7	4	5	1	0	3	2

SECTION 3

PRIORITIES	a	b	c	d	e	f	g	h
	CPU	CPU	CPU	CPU	CPU	CPU	CPU	CPU
SS0	3	0	1	2	6	5	4	7
SS1	3	0	1	2	6	5	4	7
SS2	7	4	5	6	2	1	0	3
SS3	7	4	5	6	2	1	0	3
SS4	3	0	1	2	6	5	4	7
SS5	3	0	1	2	6	5	4	7
SS6	7	4	5	6	2	1	0	3
SS7	7	4	5	6	2	1	0	3

A-6464

Hardware Trng.
YM11/02 J.E.S.

One of the unique aspects of the memory control is the way in which bank conflicts are determined and resolved. Both the CPU and memory module check for memory bank conflicts. The CPU module will determine if a bank conflict occurs and resolve the conflict using the priority scheme described previously. The memory module must also determine if a bank conflict will occur and resolve the conflict using the same priority scheme as the CPU used. On a read reference both the CPU and memory module must come up with the same answer in order for the read data to be selected properly within the CPU module.

The section conflict resolves conflicts between the ports and the sections. If Port A wants Section 0 and Port B also wants Section 0, we have a section conflict. To resolve a section conflict, the rules are as follows:

- When Port D is being used by fetch, or by I/O during an I/O timeout condition, it has the highest priority. Port D with I/O and no I/O timeout would have the lowest priority.
- Odd increment has the next highest priority. If Port A has an odd increment and Port B has an even increment, then Port A would have the higher priority.
- If more than one port has an even or odd stride or increment, the first port issued has the highest priority. To determine which port has first issued is dependent upon what ports have reservations. If Port A was reserved first, then Port A would be first issued, so Port A would have higher priority over Port C or B. If Port C was reserved next, then Port C would have higher priority over Port B.
- A Gather/Scatter instruction defaults to an odd increment.
- Scalar reference will go active only after the block references run to completion.

Ports A and B are used for a read operation of memory. Port A is used by B registers, Address and Scalar registers, and Vector registers. Port B is used by vector T. Port C is used by vectors, B/T registers and A/S registers on a write to memory. Port D is used for both reads and writes to memory by fetch and I/O. A fetch write can occur on a control dump after a deadstart.

Write Data Sequence

Data is written to memory using Port C or Port D. Before the data is sent to memory, it must have 8 check bits appended to the 64-bit word. Data arrives to the (YC, YD) options from the Vector register, Scalar register, Address register, B/T registers, instruction buffers, and from I/O. I/O data would have previously generated check bits on the (YR12 - YR15) options on a LOSP channel, or performed SECDED on a HISP or VHISP channel. If a subsection conflict occurs, the previously read data would get stacked. There are eight stacks 0 - 7, that are addressed by a Write pointer or a Read pointer. When the Read pointer is equal to the Write pointer, the stack is not used. When the Read pointer is not equal to the Write pointer the stack is used. Port D bypasses the check bit generation on the (YC) options and supplies its own check bit on the (YC) options R terms. Port D also bypasses the stacks. The (YC -YD) option steers the data and check bits to the proper section, supplied by the (YK) section Enable terms.

Address Sequence Generation

In order to address memory, all references must be added to the DBA or IBA, except for I/O and Exchange which are absolute. The Port A, B, or C Address Add is performed on the (YE, YF) options. Generally what gets added is (Ah + DBA + Ak), (Ah + DBA + Vk), (Ah + DBA + 1) for a Vector reference, or (Ah + DBA + jkm) or (Ah + DBA + nm) for a Scalar reference.

When adding (Ah + DBA + Vk) for a Vector Memory reference, and the Port receives a Subsection conflict, the (VK) operand previously read out of the Vector register must be stacked. The (VK) operand is stacked on the (YI, YJ) option which are also used to multiplex data into the A registers. There are four stacks 0 - 3 for (VK) operand. The stacks operate similarly to the (YD, YC) stacks.

During a Fetch operation (IBA + P) is added and this is performed on the (YZ, YH) options. The (YZ, YH) will also compare (P + IBA) against ILA. If the (P + IBA) is equal to or above the ILA, the (YH) option will generate a Program Range Error to the (YB) option.

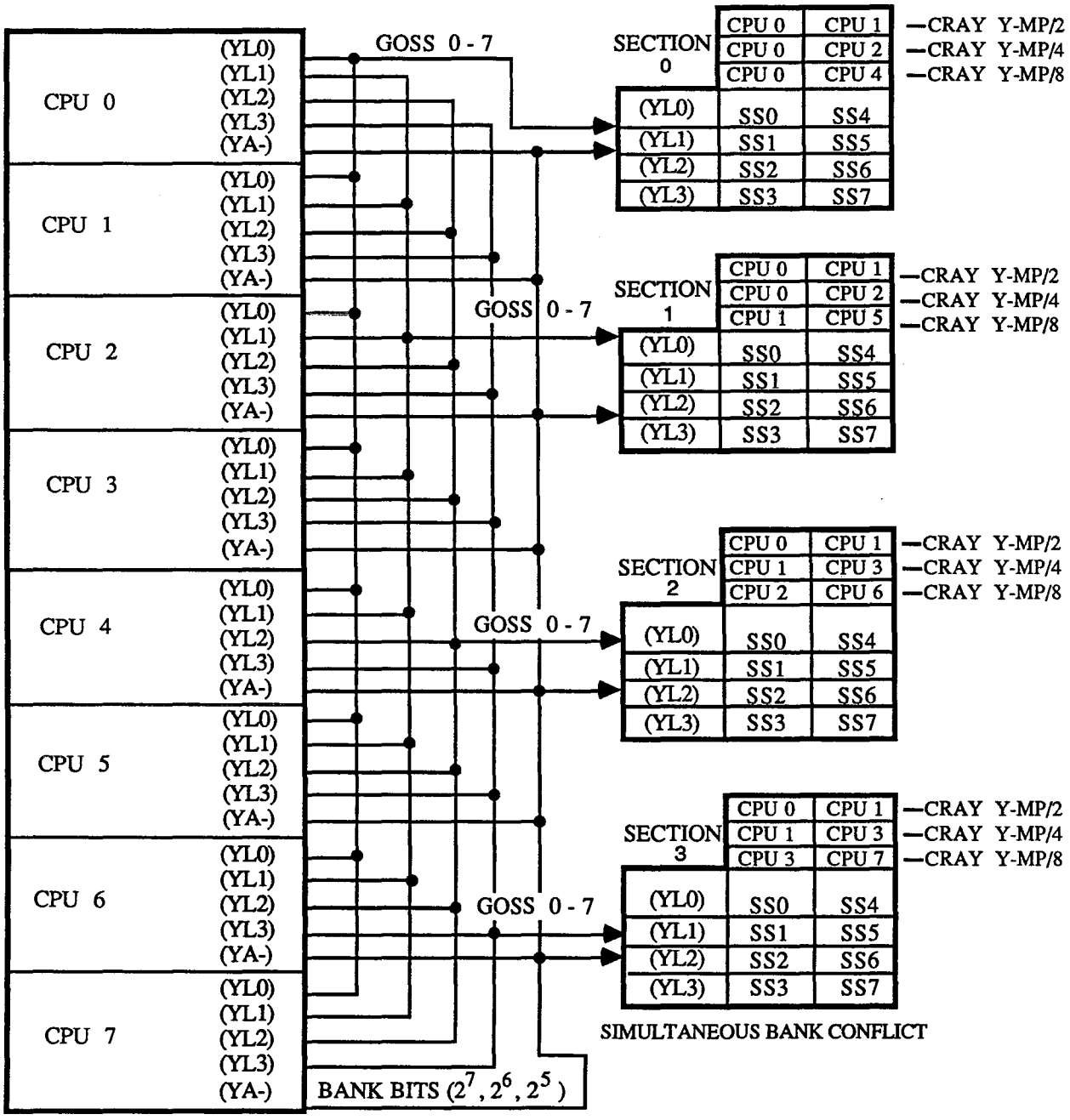
The (YB) option is used to check Ports A, B, or C Absolute address against the DLA. If the Absolute address is equal to or greater than the DLA, an Abort signal is sent to the appropriate section to stop the reference. The Program Range Error sent from the (YH) option will also generate an ABORT signal to a particular section in memory.

The (YA) options are used to multiplex the address from Ports A, B, C, or D to Sections 0 - 3 in memory. The (YA) will send address bits (2^5 - 2^7) to the CPU modules and to the memory modules to determine a Bank conflict amongst the CPUs.

Control Sequence

The port references A, B, C, or D come into the (YK) options from the (YE, YZ) options. Before a port can make a request, it must first check to see if the requesting subsection is busy or if the port is holding on a conflict. When the port runs into a conflict, the (YK) will send out a Subsection conflict to the (YC, YD, YI, YJ). This will stack the data which is to be written into memory or address and stop the reads of the data and address. When the port is released, the (YK) will send its section Enable and SS0, SS1, SS2, SS3, Go Subsection (GOSS) 0 - 3, GOSS 4 - 7 bits to the (YL). The (YL) will decode the GOSS bits and send a GOSS 0 - 7 to memory and to the CPU modules. The (YAs) will send the address to the memory modules and the Bank address bits (2^5, 2^6, 2^7) to the CPU modules. The CPUs receive the GOSS back into the (YLs) along with address bits (2^5, 2^6, 2^7). The (YL) option will now check for a Simultaneous Bank conflict, or a conflict between CPUs wanting the same bank. The diagram on the next page memory module will also be checking for the same bank conflicts on the (ZX) options. The (YLs) will check for CPU (A - H) having similar banks, and then will release the subsection if no conflict, or will release the highest priority CPU (A - H) when conflict occurs. The subsection released is then sent out to the proper CPU (A - H) (YM) options.

The (YM) option within the CPUs will decode the release subsection and determine which Port A/B/D can be released from the release Subsection 0 - 7. The (YM) option will generate the Port A/B/D release conflict to the (YM, YN, YK) options. The Port A/B/D release conflict will then generate the release Subsection 0 - 7 which is sent to the (YK) option. The (YK) option upon receiving the Port A/B/D release will release the port Subsection conflict which allows another reference with that port. The release Subsection 0 - 7 allows the section to be used again by any Port A/B/C/D.



CRAY Y-MP GOSS 0 - 7 EXTERNAL FANOUT

When a Port Section conflict occurs, the (YM) will prioritize Ports A, B, D such that A has highest priority, then B, then D. Basically, there is a three clock period (CP) window in which the data must be selected from the memory module before another Read Reference to memory would over write the data so that Ports A, B, and D must select their data within this time. The Release Subsection sent to the (YK) clears the section busy, allowing any ports to access the section while the Release conflict A, B, D sent to the (YK) will continue to hold the release until the Release conflict goes away.

When a conflict occurs, the (YM) generates a Release conflict, which means the release has a conflict on Ports A, B, D or that the port is unable to release. The Release conflict could be generated if it is not the highest priority or if the SS Release is not present for the (YL) option.

Prior to getting the SS Release from the (YLs), the (YM) option will asume that a conflict exists, causing the (YK, YO, YN) to latch and hold its information. Once the SS Release arrives, the information is advanced. The (YO, YH) option could have four references backed up at one time.

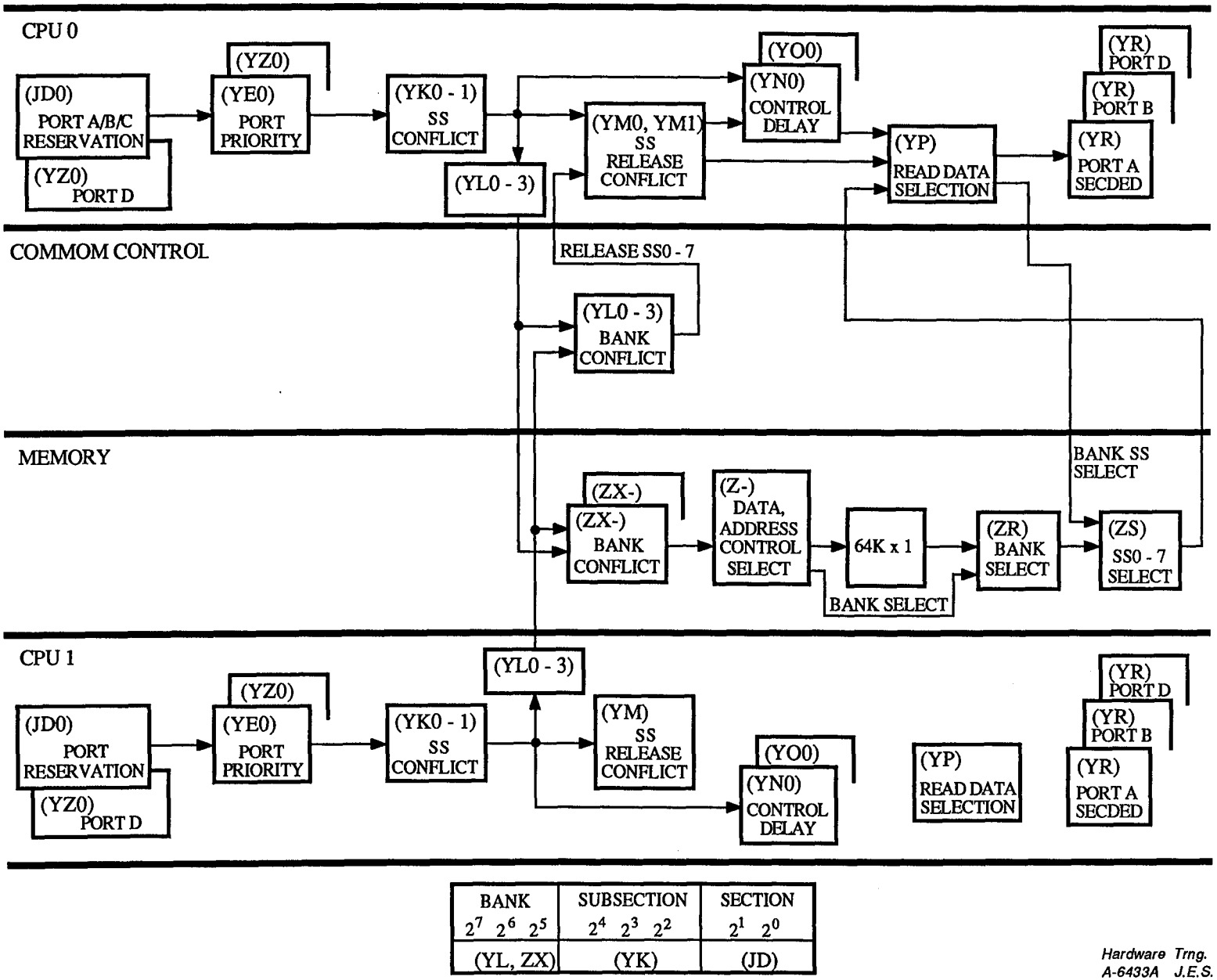
After the (YM) has gone through Bank Busy which was spent on the (YO, YN) option and the Bank conflicts, it will supply the (YP) option with the section selects for the Read data. The port selects are supplied from the (YN) option at RCON + 2 time to the (YP) option for Port Select A/B/D.

The data is then sent to the appropriate (YR) options where SECDED is performed before the data is sent to the A registers, S registers, V registers, B/T registers, or instruction buffers.

Subsection Conflict

The Subsection conflict is determined on the (YK) option, and will prevent a reference to a subsection which has been previously referenced within the same section. The reference which was held on a Subsection conflict is allowed to procede once that subsection receives a Release Subsection from the (YM) option.

A Subsection conflict is caused by two or more references to the same subsection within the same section for a particular CPU.



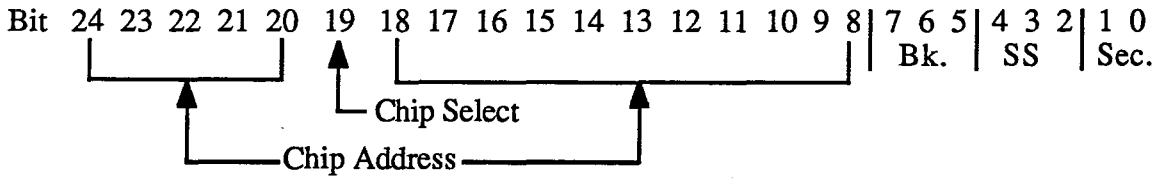
BANK	SUBSECTION	SECTION
2^7 2^6 2^5	2^4 2^3 2^2	2^1 2^0
(YL, ZX)	(YK)	(JD)

Hardware Trng.
A-6433A J.E.S.

CRAY Y-MP MEMORY CONTROL

Addressing

The memory uses a 25-bit address which consists of Section Select, Subsection Select, Bank Select, Chip Address, and Chip Select bits. The figure below shows the memory address bits.

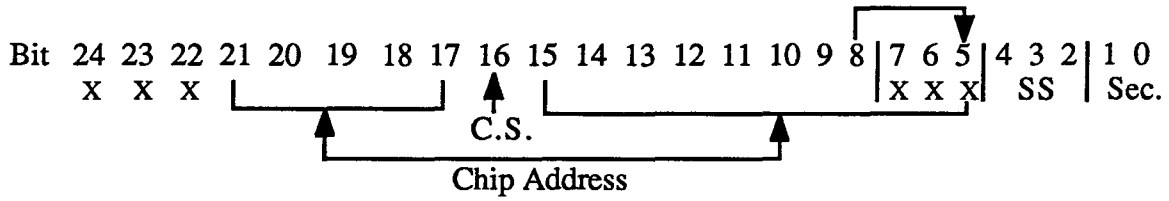


Memory Address Bits Using 64K Storage Chip

As the address increments sequentially, first the selection steps through the four sections in turn, then it starts toggling through the eight subsections, and eventually steps through the banks. The chip address is used within the storage chip. The Chip Select signal selects one of the two physical groups of storage chips on the module.

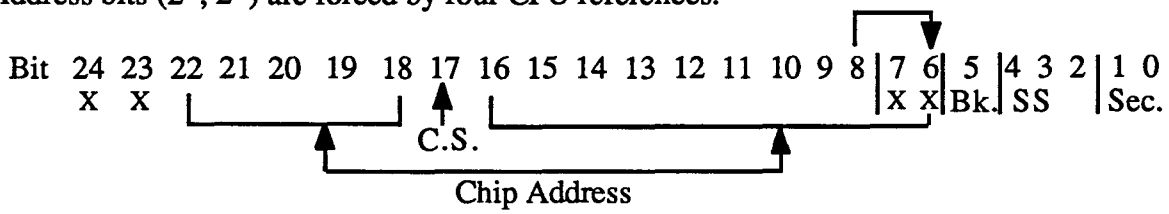
Addressing on CRAY Y-MP/1 Mainframe

On a CRAY Y-MP/14 address bits (2^5 - 2^7) are forced by the eight CPU references, so that an internal address (2^8) becomes internal address (2^5), and every other bit moves down three positions.



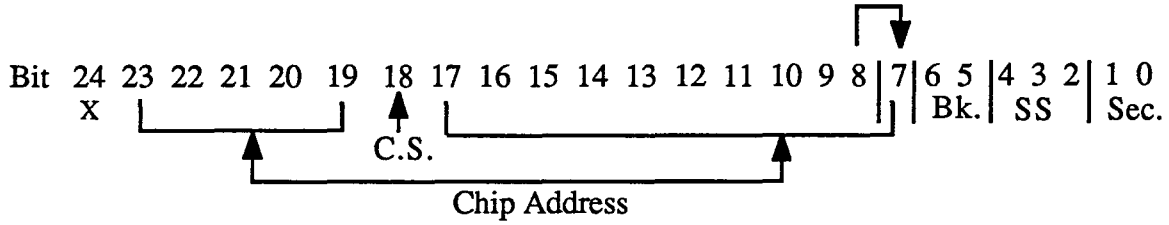
Addressing on CRAY Y-MP/28 Mainframe

Address bits (2^6, 2^7) are forced by four CPU references.



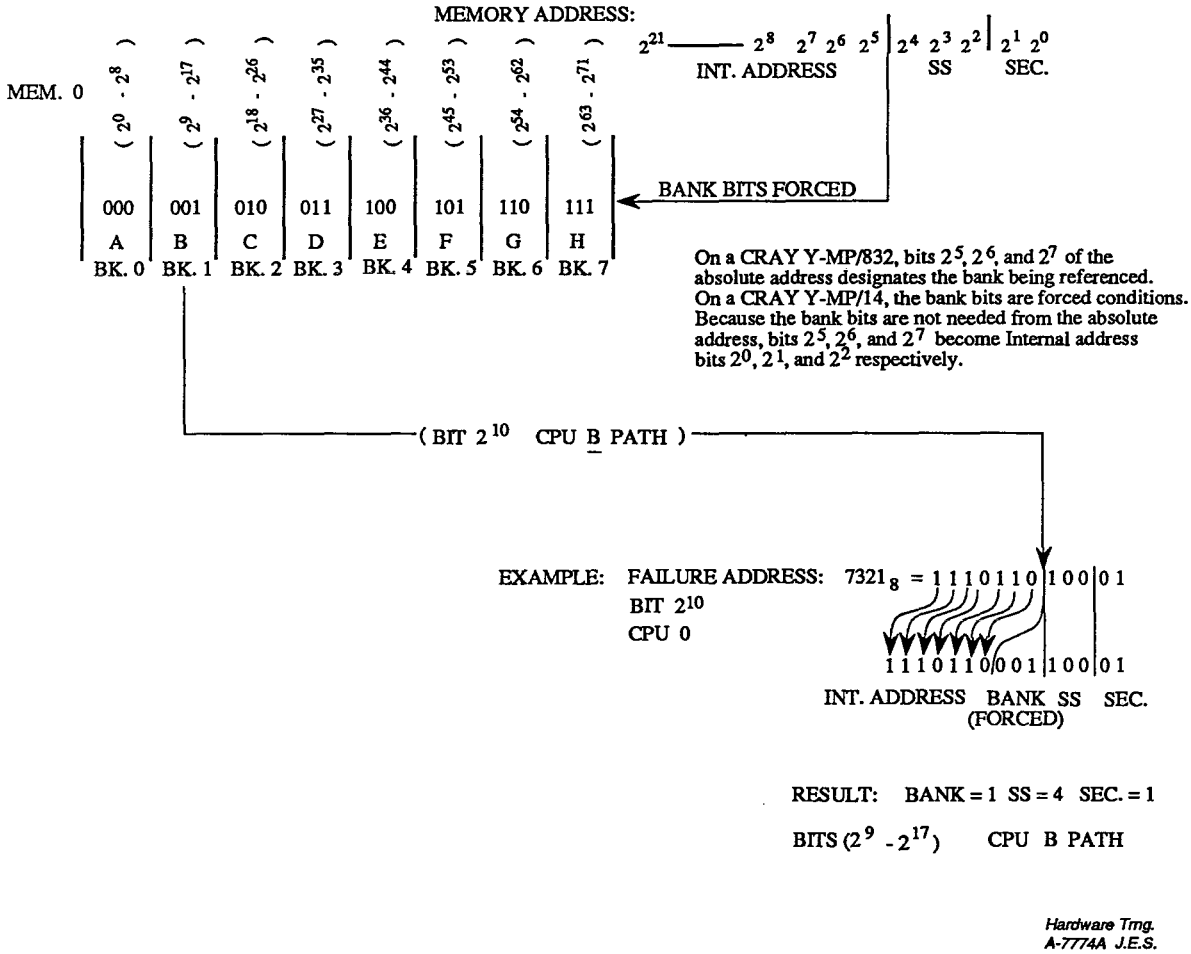
Addressing on CRAY Y-MP/416 Mainframe

Address bit (2^7) is forced by two CPU references.



Hardware Trng.
YM11/06B J.E.S.

- 1 MODULE PER SECTION; 72 BITS PER MODULE
- 4 TOTAL MEMORY MODULES
- 32 BANK MACHINE
- 1 BANK PER SUBSECTION
- MEMORY ADDRESS



CRAY Y-MP/14 MEMORY LAYOUT

	SS0	SS1	SS2	SS3	SS4	SS5	SS6	SS7	
SECTION 0	0	4	10	14	20	24	30	34	
	40	44	50	54	60	64	70	74	
	100	104	110	114	120	124	130	134	
	140	144	150	154	160	164	170	174	
	200	204	210	214	220	224	230	234	
	240	244	250	254	260	264	270	274	
	300	304	310	314	320	324	330	334	
	340	344	350	354	360	364	370	374	
	CPU 0	CPU 0	CPU 0	CPU 0	CPU 4	CPU 4	CPU 4	CPU 4	– CRAY Y-MP/8
	CPU 0	CPU 0	CPU 0	CPU 0	CPU 2	CPU 2	CPU 2	CPU 2	– CRAY Y-MP/4
	CPU 0	CPU 0	CPU 0	CPU 0	CPU 1	CPU 1	CPU 1	CPU 1	– CRAY Y-MP/2
	(YL0)	(YL1)	(YL2)	(YL3)	(YL0)	(YL1)	(YL2)	(YL3)	

	SS0	SS1	SS2	SS3	SS4	SS5	SS6	SS7	
SECTION 1	1	5	11	15	21	25	31	35	
	41	45	51	55	61	65	71	75	
	101	105	111	115	121	125	131	135	
	141	145	151	155	161	165	171	175	
	201	205	211	215	221	225	231	235	
	241	245	251	255	261	265	271	275	
	301	305	311	315	321	325	331	335	
	341	345	351	355	361	365	371	375	
	CPU 1	CPU 1	CPU 1	CPU 1	CPU 5	CPU 5	CPU 5	CPU 5	– CRAY Y-MP/8
	CPU 0	CPU 0	CPU 0	CPU 0	CPU 2	CPU 2	CPU 2	CPU 2	– CRAY Y-MP/4
	CPU 0	CPU 0	CPU 0	CPU 0	CPU 1	CPU 1	CPU 1	CPU 1	– CRAY Y-MP/2
	(YL0)	(YL1)	(YL2)	(YL3)	(YL0)	(YL1)	(YL2)	(YL3)	

CPU 0	(YL0 - YL3)	GO SUBSECTION 0 - 7 TO SECTION 0 - 3
CPU 1	(YL0 - YL3)	GO SUBSECTION 0 - 7 TO SECTION 0 - 3
CPU 2	(YL0 - YL3)	GO SUBSECTION 0 - 7 TO SECTION 0 - 3
CPU 3	(YL0 - YL3)	GO SUBSECTION 0 - 7 TO SECTION 0 - 3
CPU 4	(YL0 - YL3)	GO SUBSECTION 0 - 7 TO SECTION 0 - 3
CPU 5	(YL0 - YL3)	GO SUBSECTION 0 - 7 TO SECTION 0 - 3
CPU 6	(YL0 - YL3)	GO SUBSECTION 0 - 7 TO SECTION 0 - 3
CPU 7	(YL0 - YL3)	GO SUBSECTION 0 - 7 TO SECTION 0 - 3

	SS0	SS1	SS2	SS3	SS4	SS5	SS6	SS7	
SECTION 2	2	6	12	16	22	26	32	36	
	42	46	52	56	62	66	72	76	
	102	106	112	116	122	126	132	136	
	142	146	152	156	162	166	172	176	
	202	206	212	216	222	226	232	236	
	242	246	252	256	262	266	272	276	
	302	306	312	316	322	326	332	336	
	342	346	352	356	362	366	372	376	
	CPU 2	CPU 2	CPU 2	CPU 2	CPU 6	CPU 6	CPU 6	CPU 6	– CRAY Y-MP/8
	CPU 1	CPU 1	CPU 1	CPU 1	CPU 3	CPU 3	CPU 3	CPU 3	– CRAY Y-MP/4
	CPU 0	CPU 0	CPU 0	CPU 0	CPU 1	CPU 1	CPU 1	CPU 1	– CRAY Y-MP/2
	(YL0)	(YL1)	(YL2)	(YL3)	(YL0)	(YL1)	(YL2)	(YL3)	

	SS0	SS1	SS2	SS3	SS4	SS5	SS6	SS7	
SECTION 3	3	7	13	17	23	27	33	37	
	43	47	53	57	63	67	73	77	
	103	107	113	117	123	127	133	137	
	143	147	153	157	163	167	173	177	
	203	207	213	217	223	227	233	237	
	243	247	253	257	263	267	273	277	
	303	307	313	317	323	327	333	337	
	343	347	353	357	363	367	373	377	
	CPU 3	CPU 3	CPU 3	CPU 3	CPU 7	CPU 7	CPU 7	CPU 7	– CRAY Y-MP/8
	CPU 1	CPU 1	CPU 1	CPU 1	CPU 3	CPU 3	CPU 3	CPU 3	– CRAY Y-MP/4
	CPU 0	CPU 0	CPU 0	CPU 0	CPU 1	CPU 1	CPU 1	CPU 1	– CRAY Y-MP/2
	(YL0)	(YL1)	(YL2)	(YL3)	(YL0)	(YL1)	(YL2)	(YL3)	

Hardware Trng.
A-6221A J.E.S.

CRAY Y-MP SIMULTANEOUS BANK CONFLICT (YL)

- 4 MODULES PER SECTION; 18 BITS PER MODULE
- 16 TOTAL MEMORY MODULES
- 128 BANK MACHINE
- 4 BANKS PER SUBSECTION
- MEMORY ADDRESS

		MEM 0 (2^0-2^8) MEM 1 (2^{18}-2^{26}) MEM 2 (2^{36}-2^{44}) MEM 3 (2^{54}-2^{62})								MEM 0 (2^9-2^{17}) MEM 1 (2^{27}-2^{35}) MEM 2 (2^{45}-2^{53}) MEM 3 (2^{63}-2^{71})							
SECTION		BITS 0 - 8, 18 - 26, 36 - 44, 54 - 62								BITS 9 - 17, 27 - 35, 45 - 53, 63 - 71							
		0		1		2		3		0		1		2		3	
SUBSECTION		0145	2367	0145	2367	0145	2367	0145	2367	0145	2367	0145	2367	0145	2367	0145	2367
CPU PATH		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	0	A	H	G	B	E	D	C	F	B	G	H	A	F	C	D	E
	1	C	F	A	H	G	B	E	D	D	E	B	G	H	A	F	C
	2	E	D	C	F	A	H	G	B	F	C	D	E	B	G	H	A
	3	G	B	E	D	C	F	A	H	H	A	F	C	D	E	B	G

2^{23} —— 2^8 2^7 | 2^6 2^5 | 2^4 2^3 2^2 | 2^1 2^0
INT. ADDR. | BK. | SS | SEC.
2^1 2^0

BANK BIT (2^2) FORCED

Bits (2^5) and (2^6) of the Absolute address are bank bits (2^0) and (2^1) respectively. On a CRAY Y-MP8 bit (2^7) of the Absolute address is bank bit (2^2). On a CRAY Y-MP4 bank bit (2^2) is forced. Because bank bit (2^2) does not come from bit (2^7) of the Absolute address, bit (2^7) becomes Internal address bit (2^0).

(BIT (2^{10}) CPU H PATH)

YL CONFLICT CHECKS

SEC.		0		1		2		3	
SS		0145	2367	0145	2367	0145	2367	0145	2367
CPU PATH	0	A	H	G	B	F	C	D	E
	1	C	F	B	G	H	A	E	D
	2	F	C	D	E	A	H	G	B
	3	H	A	E	D	C	F	B	G

EXAMPLE: FAILURE ADDRESS: 7321_8 = 1 1 1 0 1 1 0 1 0 0 0 0 1
BIT (2^{10})
CPU 0

1 1 1 0 1 | 1 0 | 1 0 0 | 0 1
INT. ADDR. | BK. | SS | SEC.

RESULT: BANK 6, SS 4, SEC. 1
BITS (2^9 - 2^{17}) CPU H PATH MEM 0

Hardware Trng.
A-7781B J.E.S.

CRAY Y-MP4/xy

- 2 MODULES PER SECTION; 36 BITS PER MODULE
- 8 TOTAL MEMORY MODULES
- 64 BANK MACHINE
- 2 BANKS PER SUBSECTION
- MEMORY ADDRESS

MEMORY ADDRESS:

2^{22} —— 2^8 2^7 2^6 | 2^5 | 2^4 2^3 2^2 | 2^1 2^0

INT. ADDRESS | BANK 2^0 | SS | SEC.

	MEM0 (2^0 - 2^8) MEM1 (2^{36} - 2^{44})								MEM0 (2^9 - 2^{17}) MEM1 (2^{45} - 2^{53})								MEM0 (2^{18} - 2^{26}) MEM1 (2^{54} - 2^{62})								MEM0 (2^{27} - 2^{35}) MEM1 (2^{63} - 2^{71})							
SECTION	0		1		2		3		0		1		2		3		0		1		2		3		0		1		2		3	
SUBSECTION	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7
	00X		00X		00X		00X		01X		01X		01X		01X		10X		10X		10X		10X		11X		11X		11X		11X	
CPU 0	A	H	H	A	A	H	H	A	B	G	G	B	B	G	G	B	C	F	F	C	C	F	F	C	D	E	E	D	D	E	E	D
PATH 1	H	A	A	H	H	A	A	H	G	B	B	G	G	B	B	G	F	C	C	F	F	C	C	F	E	D	D	E	E	D	D	E

(BIT 2^{10} CPU B PATH)

Bit 2^5 of the absolute address is bank bit 2^0. On a CRAY Y-MP8, bits 2^6 and 2^7 of the absolute address are bank bits 2^1 and 2^2 respectively. On a CRAY Y-MP2, bank bits 2^1 and 2^2 are forced. Because bank bits 2^1 and 2^2 do not come from the absolute address, bits 2^6 and 2^7 become part of the Internal address. Bit 2^6 becomes Internal address bit 2^0. Bit 2^7 becomes Internal address bit 2^1.

YL CONFLICT CHECK

SEC.		0		1		2		3	
SS		0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7	0 1 4 5	2 3 6 7
CPU PATH	0	A	H	G	B	C	F	E	D
	1	H	A	B	G	F	C	D	E

EXAMPLE: FAILURE ADDRESS: 7321_8 = 1 1 1 0 1 1 0 1 0 0 0 1

BIT 2^{10}

CPU 1

1 1 1 0 1 1 0 1 0 0 0 1

INT. ADDRESS BANK SS SEC.

(2^1, 2^2 FORCED)

RESULT: BANK = 2 SS = 4 SEC. = 1

BITS (2^9 - 2^{17}) CPU B PATH MEM 0

Hardware Trng A-7782C J.E.S.

CRAY Y-MP2/XY MEMORY LAYOUT

CRAY X-MP MEMORY REFERENCE INSTRUCTIONS X-MODE

SCALAR REFERENCE

10hijkm - Read from Memory address specified by ((Ah)+(jkm)+(DBA)) to Ai (Ah ≠ 0)
100ijkm - Read from Memory address specified by ((jkm)+(DBA)) to Ai (Ah = 0)
10hi000 - Read from Memory address specified by ((Ah)+(DBA)) to Ai (Ah ≠ 0)

11hijkm - Write (Ai) to Memory address specified by ((Ah)+(jkm)+(DBA))(Ah ≠0)

110ijkm - Write (Ai) to Memory address specified by ((jkm)+(DBA)) (Ah = 0)
11hi000 - Write (Ai) to Memory address specified by ((Ah)+(DBA)) (Ah ≠ 0)

12hijkm - Read from Memory address specified by ((Ah)+(jkm)+(DBA)) to Si (Ah ≠ 0)
120ijkm - Read from Memory address specified by ((jkm)+(DBA)) to Si (Ah = 0)
12hi000 - Read from Memory address specified by ((Ah)+(DBA)) to Si (Ah ≠ 0)

13hijkm - Write (Si) to Memory address specified by ((Ah)+(jkm)+(DBA)) (Ah ≠0)
130ijkm - Write (Si) to Memory address specified by ((jkm)+(DBA)) (Ah = 0)
13hi000 - Write (Si) to Memory address specified by ((Ah)+(DBA)) (Ah ≠ 0)

B/T REGISTER BLOCK REFERENCE

034ijk - Read (Ai) word from starting Memory address ((A0)+(DBA)) to Bjk
035ijk - Write (Ai) words to starting Memory address ((A0)+(DBA)) from Bjk

036ijk - Read (Ai) words from starting Memory address ((A0)+(DBA)) to Tjk
037ijk - Write (Ai) words to starting Memory address ((A0)+(DBA)) from Tjk

VECTOR REGISTER BLOCK REFERENCE

176i0k - Read (VL) words into Vi from Memory address specified by ((A0)+(DBA)) incremented by (Ak)
176i00 - Read (VL) words into Vi from Memory address specified by ((A0)+(DBA)) incremented by one

176ilk - Read (VL) words from Memory address specified by ((A0)+(Vk)+(DBA)) to Vi (Gather)

1770jk - Write (VL) words from Vj to Memory address specified by ((A0)+(DBA)) incremented by (Ak)
1770j0 - Write (VL) words from Vj to Memory address specified by ((A0)+(DBA)) incremented by one

177ljk - Write (VL) words from Vj to Memory address specified by ((A0)+(Vk)+(DBA)) (Scatter)

YM11/07

CRAY Y-MP MEMORY REFERENCE INSTRUCTIONS Y-MODE

SCALAR REFERENCE

10hijkmn - Read from Memory address specified by ((Ah)+(nm)+(DBA)) to Ai (Ah ≠ 0)
100ijkmn - Read from Memory address specified by ((nm)+(DBA)) to Ai (Ah = 0)
10hi0000 - Read from Memory address specified by ((Ah)+(DBA)) to Ai (Ah ≠ 0)

11hijkmn - Write (Ai) to Memory address specified by ((Ah)+(nm)+(DBA)) (Ah ≠ 0)
110ijkmn - Write (Ai) to Memory address specified by ((nm)+(DBA)) (Ah = 0)
11hi0000 - Write (Ai) to Memory address specified by ((Ah)+(DBA)) (Ah ≠ 0)

12hijkmn - Read from Memory address specified by ((Ah)+(nm)+(DBA)) to Si (Ah ≠ 0)
120ijkmn - Read from Memory address specified by ((nm)+(DBA)) to Si (Ah = 0)
12hi0000 - Read from Memory address specified by ((Ah)+(DBA)) to Si (Ah ≠ 0)

13hijkmn - Write (Si) to Memory address specified by ((Ah)+(nm)+(DBA)) (Ah ≠ 0)
130ijkmn - Write (Si) to Memory address specified by ((nm)+(DBA)) (Ah = 0)
13hi0000 - Write (Si) to Memory address specified by ((Ah)+(DBA)) (Ah ≠ 0)

B/T REGISTER BLOCK REFERENCE

034ijk - Read (Ai) word from starting Memory address ((A0)+(DBA)) to Bjk
035ijk - Write (Ai) words tostarting Memory address ((A0)+(DBA)) from Bjk

036ijk - Read (Ai) words from starting Memory address ((A0)+(DBA)) to Tjk
037ijk - Write (Ai) words to starting Memory address ((A0)+(DBA)) from Tjk

VECTOR REGISTER BLOCK REFERENCE

176i0k - Read (VL) words into Vi from Memory address specified by ((A0)+(DBA)) incremented by (Ak)
176i00 - Read (VL) words into Vi from Memory address specified by ((A0)+(DBA)) incremented by one

176ilk - Read (VL) words from Memory address specified by ((A0)+(Vk)+(DBA)) to Vi (Gather)

1770jk - Write (VL) words from Vj to Memory address specified by ((A0)+(DBA)) incremented by (Ak)
1770j0 - Write (VL) words from Vj to Memory address specified by ((A0)+(DBA)) incremented by one
177ljk - Write (VL) words from Vj to Memory address specified by ((A0)+(Vk)+(DBA)) (Scatter)

YM11/08

CRAY Y-MP MEMORY CONTROL

OPTION TYPE	NUMBER USED	DESCRIPTION
YA	4	Address Section Select
YB	1	Data Address Range Check
YC	4	Memory Check Byte Generation
YD	8	Memory Write Data Selection
YE	1	Port A, B, and C Lower Address
YF	3	Port A, B, and C Upper Address
YH	1	Port D Upper Address
YI	1	Gather/Scatter Lower
YJ	1	Gather/Scatter Upper
YK	2	Subsection Conflict
YL	4	Bank Conflict
YM	2	Subsection Release Conflict
YN	2	Reference Address Delay
YO	1	Read Reference Control Delay
YP	8	Memory Read Data Selection
YR	16	Error Correction, Disable SECDED
YZ	1	Port D Lower Address - I/O, Fetch
	68	Total Options

Hardware Trng.
YM11/09A J.E.S.

CRAY Y-MP MEMORY CONTROL (OPTIONS INVOLVED)

(YA0 - YA3) Options

The (YA) options are used to multiplex the address from Ports A, B, C, and D to Sections 0 - 3. They also send address bits (2^5, 2^6, 2^7) to the CPU module (YL) options to assist in the Simultaneous Bank conflicts. The (YA0) handles address bits (2^5, 2^8, 2^{12}, 2^{16}, 2^{20}). The (YA1) handles address bits (2^6, 2^9, 2^{13}, 2^{17}, 2^{21}). The (YA2) handles address bits (2^7, 2^{10}, 2^{14}, 2^{18}, 2^{22}) while the (YA3) handles address bits (2^{24} - 2^{27}, 2^{11}, 2^{15}, 2^{19}, 2^{23}).

(YB0) Option

The (YB0) option is used to determine if the Absolute Memory reference is within the DBA/DLA for Port A, B, or C. For Port D, the (YH, YZ) determine if the Fetch address is within range of the ILA. If not, the (YH0) will send over a Program Range Error to the (YB0) option. When a Operand Range Error occurs on Port A, B, or C, an Abort signal is sent to the memory section being requested. This stops the reference to memory, by preventing the chip select from being generated on the (ZV) option. Program Range Errors will abort all sections as long as there are no Port A, B, or C section Enables.

(YC0 - YC3) Options

The (YC) option is used to generate the 8 check bytes (CB) which are appended to the Memory Write reference. The (YC) options, however, do not generate the CB for an I/O reference, but instead pass the I/O CB on through to the proper section. The I/O CB are generated on the (YR12 - YR15) options which perform SECDED on a HISP or VHISP channel. In order for the (YC) options to generate the CBs, it must receive all 64 bits of the data word. The (YC0) receives data bits (2^0 - 2^7) and (2^{32} - 2^{39}); the (YC1) receives data bits (2^8 - 2^{15}) and (2^{40} - 2^{47}); the (YC2) receives data bits (2^{16} - 2^{31}) and (2^{56} - 2^{63}), while the (YC3) receives data bits (2^{24} - 2^{31}) and (2^{56} - 2^{63}). When the parity for CB 0 - 7 has been determined, the CB is set to make the parity even for the associated CB. Check bits (2^{64}, 2^{68}) are sent from the (YC0), CB (2^{65}, 2^{69}) are sent from (YC1), CB (2^{66}, 2^{70}) are sent from the (YC2), and CB (2^{67}, 2^{71}) are sent from the (YC3) option to the appropriate section. When a Subsection conflict occurs, the (YC) option will stack the data. The (YC) contains eight stacks 0 - 7. The stacks are addressed by a read pointer and a write pointer. When R = W the stack is bypassed. When R $\neq$ W the Read stack is used. The (YK) option controls the stacks from the Subsection conflicts and Bank conflicts.

Hardware Trng.
YM11/10A J.E.S.

(YD0 - YD7) Options

The (YD) options handle the write data to memory for Port C and Port D. The (YD) options will steer the data to the proper section when the section Enables are sent by the (YK) option. The (YD) will also stack the data similar to the (YC) option when a Subsection conflict or Bank conflict occurs with the Memory address.

(YE0) Option

The (YE) option contains the Port A, B, and C lower block address bits (2^0 - 2^4). The address bits (2^0 - 2^4) contain the section and subsection of the Memory address. The (YE0) will add to the lower bits the ports increment value of (+1, Vk, Ak) depending upon the type of Memory reference. The (YE0) also contains the Block Length (BL) and Vector Length (VL) registers which are loaded on start-up of the instruction. The BL is loaded from the (Ai) field of a 034 - 037 instruction, from the (AR) option, while the VL is loaded from the (HE0) option on a 176 - 177 instruction. The BL or VL registers are decremented by one each time an address is passed to memory. When the VL/BL is equal to zero, the (YE) option will generate a release to the (J-) options to release the port reservation. The (YE0) will determine the Port A, B, or C priority, and pass this information to the (YK) option. When the (YE0) receives a Subsection conflict from the (YK), the (YE) will stop sending address to memory and stop the decrement of the BL/VL registers.

(YF0 - YF2) Options

There are three (YF) options, each handling the upper address bits of a port. The (YF0) handles address bits (2^5 - 2^{27}) for Port A. (YF1) handles Port B and (YF2) handles Port C. The (YF) will add (A0+DBA+Ak), or (A0+DBA+VB), or (A0+DBA+1), or (A0+DBA+jkm), or (Ah+DBA+jkm), or (A0+DBA+nm) depending on the type of memory reference. A Subsection conflict will stop the adders. When there is no conflict, the (YF) will pass the absolute address to the (YA) options for a port and section select to memory. Address bits (2^5 - 2^7) are also passed to the (YN) options for a Reference Address Delay, which then passes the address to the (YM) for a Subsection Release.

(YZ0) Options

The (YZ0) contains the lower 5 bits (2^0 - 2^4) of the I/O address and Fetch address for Port D. The (YZ0) will determine the Port D priority over A, B, or C. Port D has the highest priority when being used by a Fetch request, or Port D is the lowest when used by I/O. I/O is allowed after the I/O time-out occurs. An I/O time-out occurs when the Fetch reference has a Subsection (SS) conflict for more than 37_8 clock periods. The (YZ) controls the Fetch operation by checking for no coincidence and for generating the Fetch request. It also times the arrival of words at the instruction buffers and generates the control dump after a deadstart. This writes the instruction buffer back into memory using the issue path LIP 0 and LIP 1 along with the P register.

(YH0) Option

The (YH0) option handles the upper address bit of Port D. The (YD) will add the (P+IBA) from a Fetch and check the final add against the ILA. If (P+IBA) is equal to or greater than IBA, the (YH) will generate a Program Range Error to the (YB) to abort the reference. An SS conflict will stop the add similar to the (YE, YF) options.

(YI0, YJ0) Options

The (YI, YJ) options are used to stack (Vk) when a SS conflict occurs from Port A, B, or C on a Gather/Scatter instruction. The (VK) can be stacked four deep, (0 - 3). The stack works similarly to the (YD, YC) options stacks. The (YI0, YJ0) are also used to multiplex the A register data into the (AR) option, and also pass the (nm) or (jkm) instruction field to the (YE, YF) option. The (YI0) handles data bits (2^0 - 2^7) while the (YJ0) handles data bits (2^8 - 2^{27}).

(YK0, YK1) Options

The two (YK) options solve the SS conflicts between Port A, B, C, and D. The (YK0) solves the Subsection conflicts for Sections (0, 2), while (YK1) solves Subsection conflicts for Sections (1, 3). The (YK) checks the requesting reference against the previously reserved subsection to prevent a Subsection conflict on the (ZS) options for read Ports A/B/D. When a port makes a reference request to the (YK), the (YK) must check to see if the requesting subsection is busy. If the port is in conflict with another port for the same section, the port priority would resolve the conflict. The port that is held will generate an SS Conflict to the (YC, YD) to stack the data on a write operation and to the (YE, YF) to hold the address or to the (YI, YJ) to stack (VK) if it is being used on a Gather/Scatter instruction. The (YK) is also used to stop the address and data when a Bank conflict occurs on the (YL) option. The (YK) receives the port priorities from the (YE, YZ) options. The (YK) originates the section Enables for the (YA, YB) options.

(YL0 - YL3) Options

Each (YL) option handles a section in memory. The (YLs) check for Simultaneous Bank conflict within a section. When a Simultaneous Bank conflict occurs, the (YL) resolves the conflict by a CPU (A - H) priority. CPU (A) has the highest priority and CPU (H) would have the lowest priority. Where the CPU comes in as CPU (A - H) is dependent upon where in memory the CPU has requested. Each CPU has a chance to be first somewhere in memory. Once the CPU has gone through the (YL) which has the highest priority, the (YL) will "advertise" which CPU went through, by generating a SS Release for that CPU. The SS Release will allow the previously held reference to proceed. To determine what section and subsection is going to be used, the (YL) option will generate a Go Subsection (GOSS) for Section N. The GOSS is sent to the eight memory modules within that section and to the one CPU module. This allows the memory and CPU to know what subsection is being accessed. The (YLs) will also receive the bank bits (2^5 - 2^7) from the

(YA) options from the CPU module that sent the GOSS. The GOSS and bank bits are then compared on one of the (YLs) for a particular section and subsection to determine if a Simultaneous Bank conflict will occur. The SS Release is fanned out to all the CPUs by the (YL) option.

(YM0, YM1) Options

The (YL) option generates the SS Release and the (YM) option will release the SS conflict and send the Release Subsection to the (YK) option which was waiting for the release to allow Port A, B, C, and D to continue on. The (YM0) handles Subsection 0 - 7 for Sections 0 and 2, while (YM1) handles Subsection 0 - 7 for Sections 1 and 3. The (YM) receives its control from the (YO, YN) options. The (YO0) sends the (YM) the Port A, B, D, reads, while the (YN0, YN1) sends the Port A, B, C, and D Go Reference address bits (2^1 - 2^5) which contain the section and subsection selects. The (YM) options intercommunicate like the (YK) option so as not to let a port reference get ahead of itself with a Release conflict Port A, B, C, D where the (YK) uses a Subsection conflict Port A, B, C, D. When the (YM) has generated the Release Subsection, the (YM) option will send the section select bits to the (YP) options at RCON+2 time to select the proper section data from memory. The (YM) option will generate a Port C Empty for a Complete Memory Reference (CMR) instruction.

(YN0, YN1, YO0) Options

The (YN) option will delay the Bank Busy for 5 to 8 CPs for Ports A, B, C, and D, and then hold the Go Reference Section 0 - 3 and address bits (2^0 - 2^7 and 2^{19}) for Port A, B, and D until the Bank conflict has been resolved on the (YM) option. The (YN) will send a Port A, B, D port select to the (YP) option to select the correct read data port. The (YO0) option performs the same operations as the (YN) options except the (YO0) contains the memory reference controls, for example, what port is being used and what port has a release.

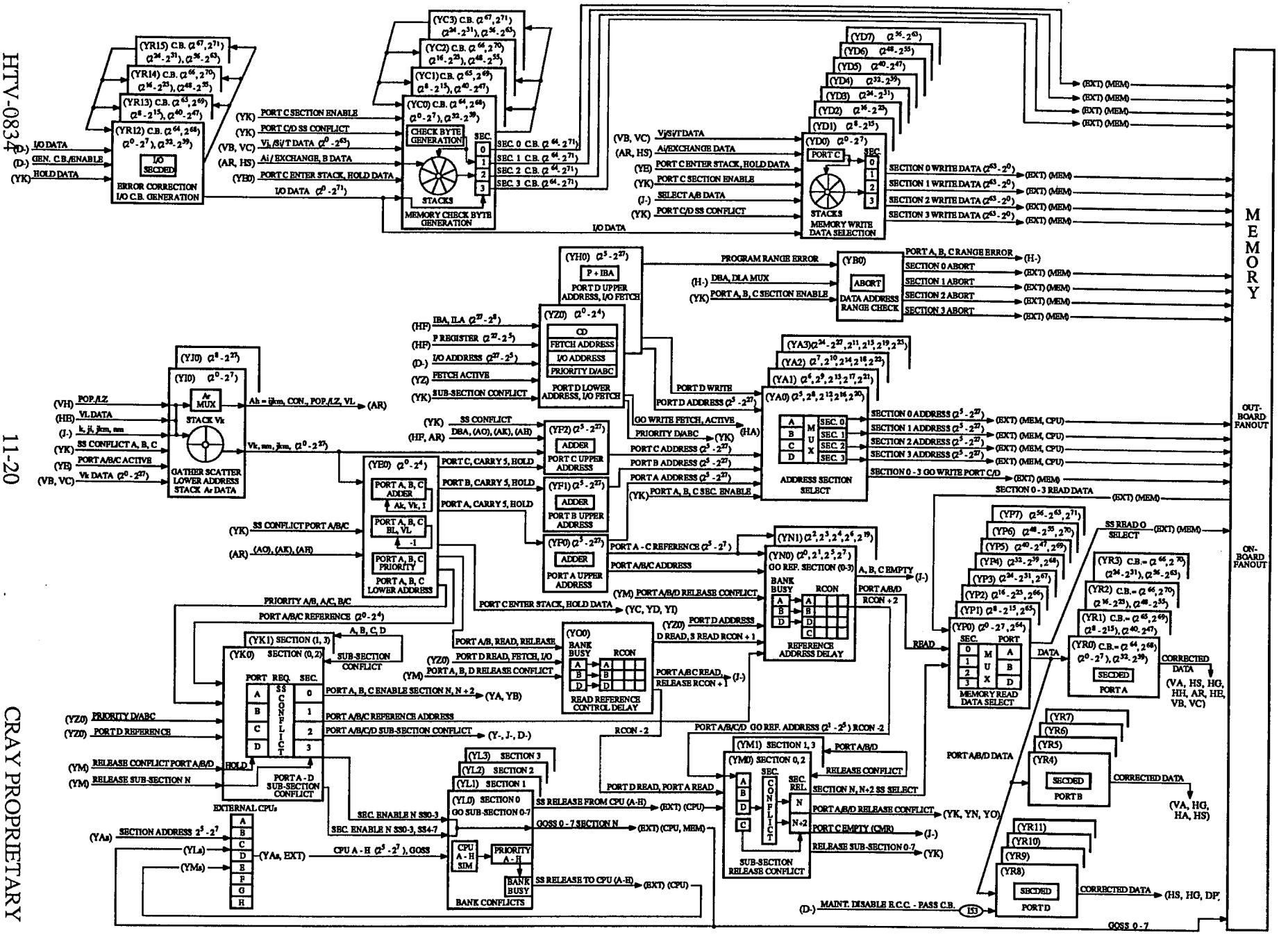
(YP0 - YP7) Options

The (YP) option will select the data from the correct section and steer the data to the correct Port A, B, or D. Each (YP) option handles 8 bits and 1 check bit of the 72-bit word which was read from memory.

(YR0 - YR15) Options

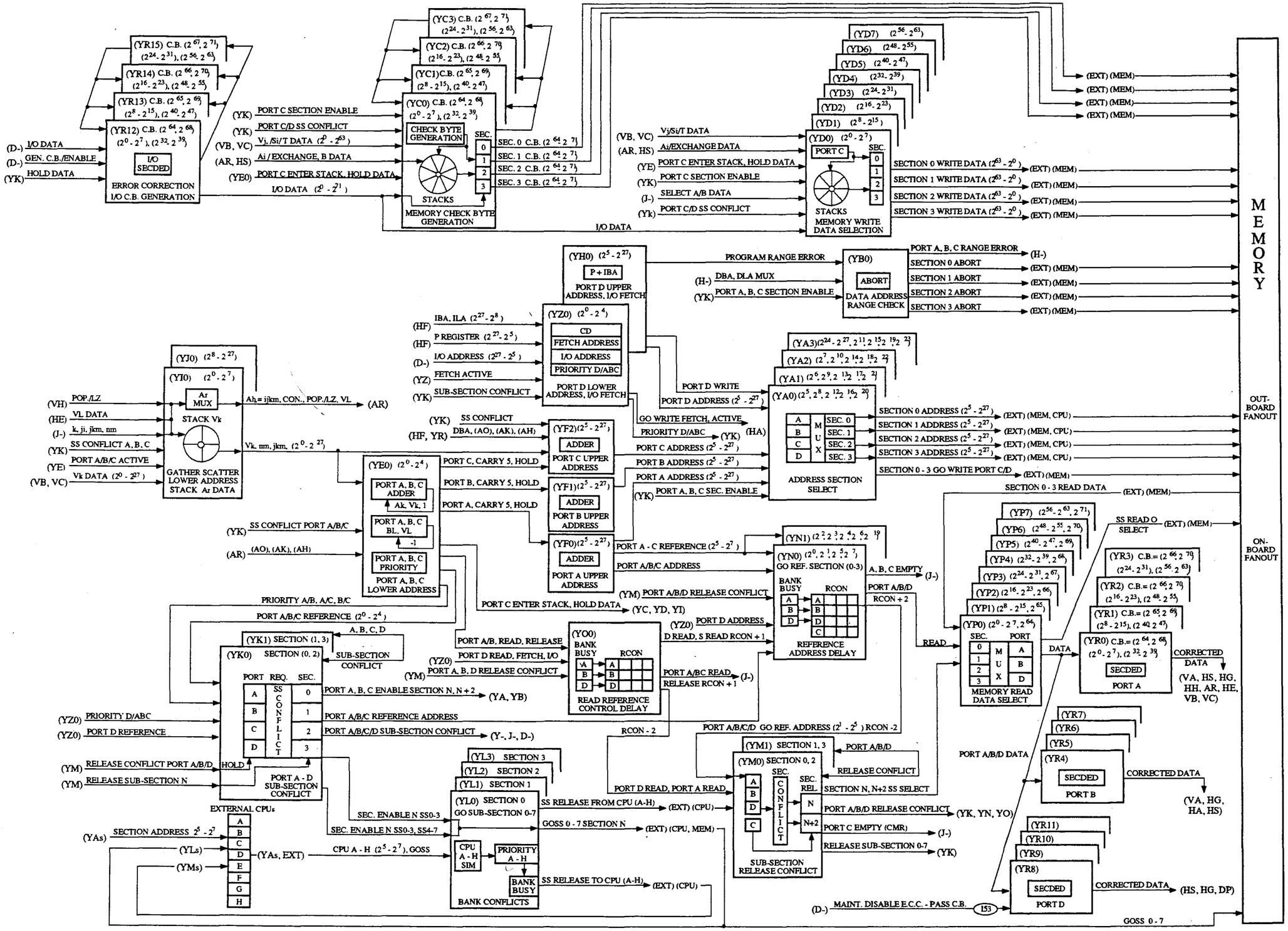
The 16 (YR) options are broken into four groups of four options. (YR0 - YR3) options perform SECDED for Port A and send the corrected data to (VA, HS, AR, HE, VB, VC, HG, HH) options. The (YR4 - YR7) perform SECDED for Port Bs read data and send the corrected data to (VA, HS, HG, HA) option. The (YR8 - YR11) options perform SECDED for Port D and send the corrected data to the (HS, H-) options. The (YR12 - YR15) options are used by the LOSP and HISP/VHISP channels. The LOSP channels use the (YR12 - YR15) to generate check bits on a I/O write to memory, while the HISP/VHISP uses the (YR12 - YR15) to perform SECDED on a write to memory. This allows SECDED on an input to Cray memory from the input HISP/VHISP channels.

Hardware Trng.
YM11/13A J.E.S.



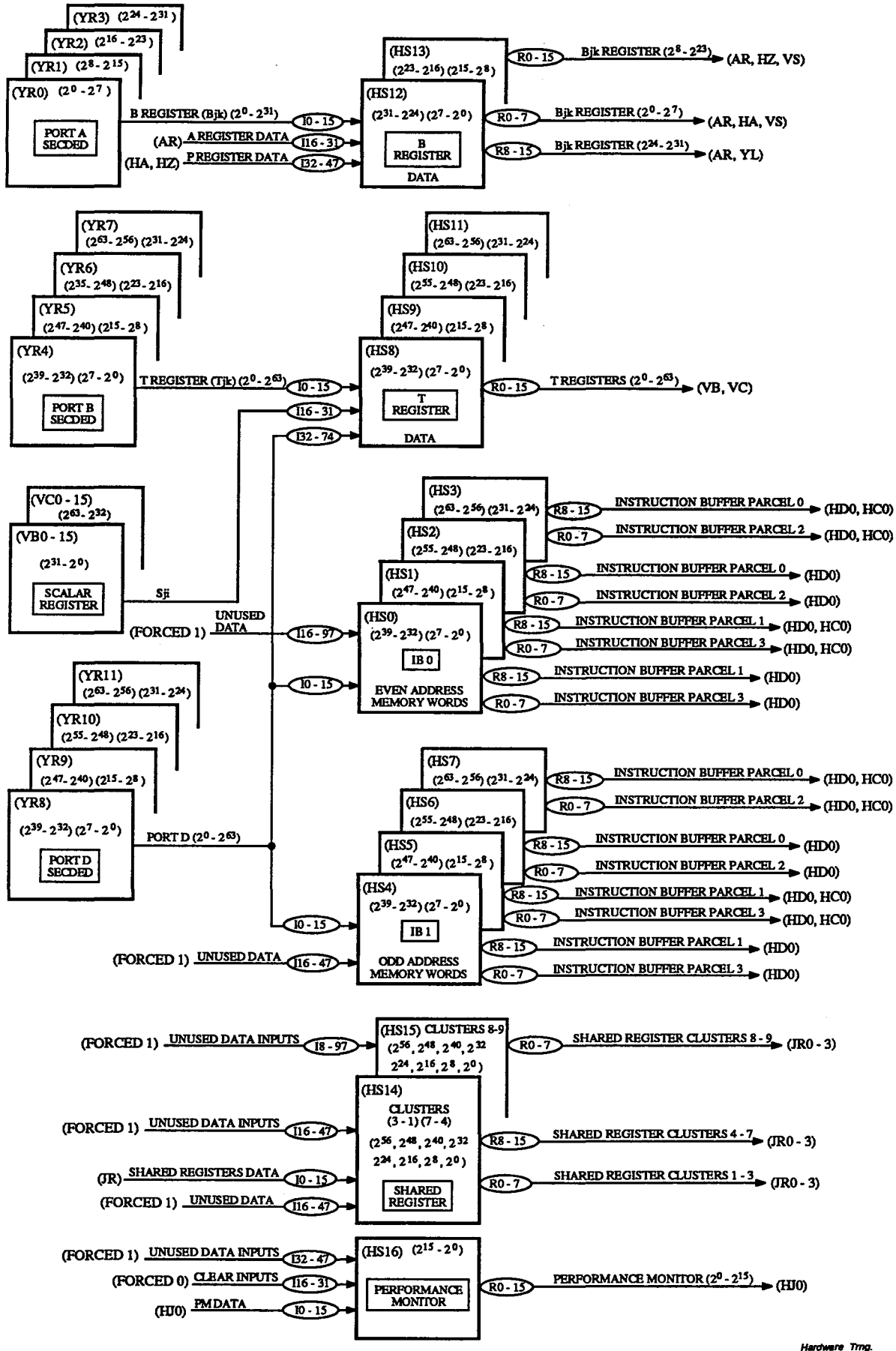
CRAY Y-MP CPU MEMORY CONTROL BLOCK DIAGRAM

Hardware Tmg.
A-6230B J.E.S.



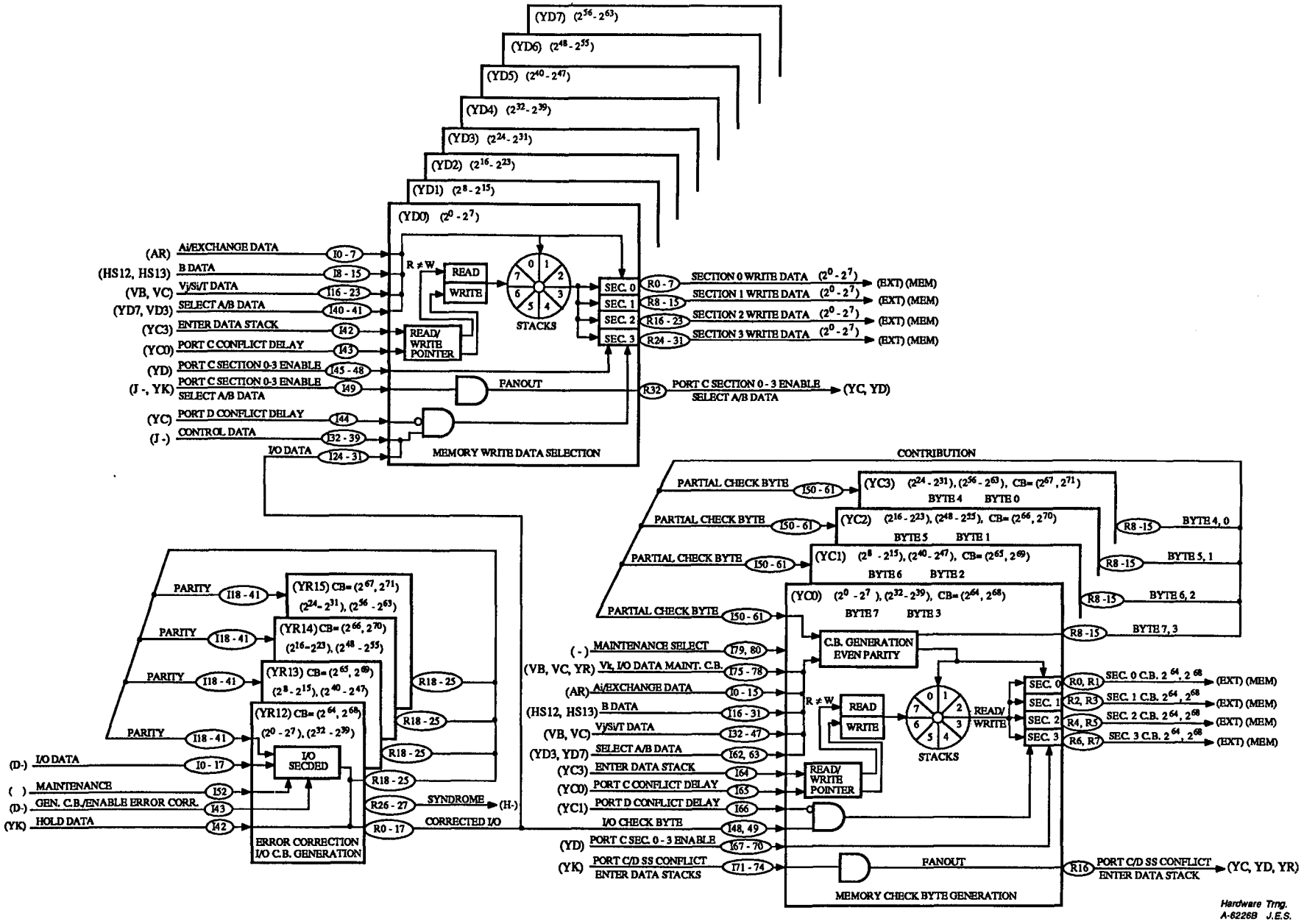
CRAY Y-MP CPU MEMORY CONTROL BLOCK DIAGRAM

Hardware Trng.
A-6230B J.E.S.



CRAY Y-MP (HS) STORAGE USAGE

Hardware Trng.
A-6279A J.E.S.



CRAY Y-MP MEMORY CONTROL BLOCK DIAGRAM
DATA SELECTION AND CHECK BYTE GENERATION

CRAY Y-MP (YC0 - YC3) OPTION FANOUTS

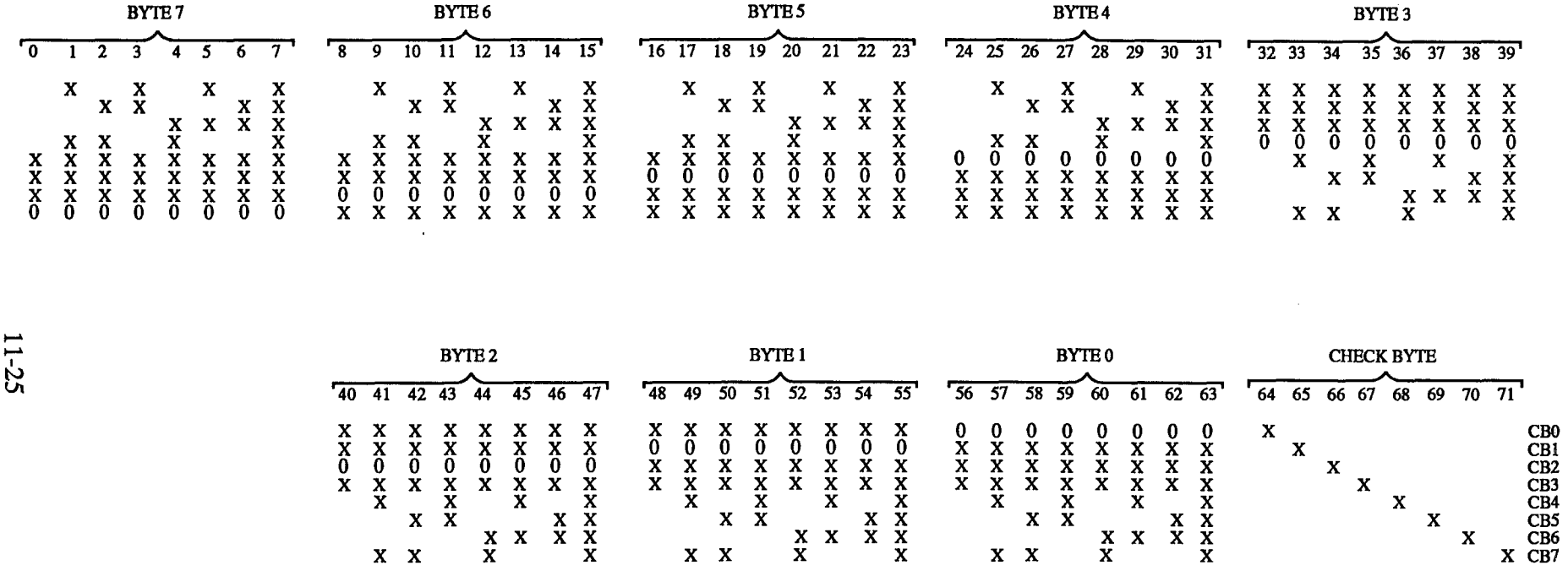
OPTION	(TERM)	DESCRIPTION	DESTINATION
(YC0)	R16	4 - 2 PORT C SSCON	(YD6 - YD3) I43
(YC0)	R16'	4 - 2 PORT C SSCON'	(YC6 - YC3) I65
(YC0)	R16A	4 - 2 PORT C SSCON	(YD4 - YD7) I43
(YC1)	R16	4 - 2 PORT D SSCON	(YD0 - YD3) I44
(YC1)	R16'	4 - 2 PORT D SSCON'	(YC6 - YC3) I66
(YC1)	R16A	4 - 2 PORT D SSCON	(YD4 - YD7) I44
(YC1)	R16A'	4 - 2 PORT D SSCON'	(YR12 - YR15) I42
(YC3)	R16	4 - 2 ENTER DATA STACK	(YD0 - YD3) I42
(YC3)	R16'	4 - 2 ENTER DATA STACK'	(YC0 - YC3) I64
(YC3)	R16A	4 - 2 ENTER DATA STACK	(YD4 - YD7) I42

A-8420

CRAY Y-MP (YD0 - YD5) OPTION FANOUTS

OPTION	TERM	DESCRIPTION	DESTINATION
(YD0)	R32	PORT C SEC. 0 ENABLE	(YD0 - YD3) I45
(YD0)	R32'	PORT C SEC. 0 ENABLE'	(YC0 - YC3) I67
(YD0)	R32A	PORT C SEC. 0 ENABLE	(YD4 - YD7) I45
(YD1)	R32	PORT C SEC. 2 ENABLE	(YD0 - YD3) I47
(YD1)	R32'	PORT C SEC. 2 ENABLE'	(YC0 - YC3) I69
(YD1)	R32A	PORT C SEC. 2 ENABLE	(YD4 - YD7) I47
(YD2)	R32	FETCH ACTIVE, HOLD I/O	(HI0) I5
(YD4)	R32	PORT C SEC. 1 ENABLE	(YD0 - YD3) I46
(YD4)	R32'	PORT C SEC. 1 ENABLE'	(YC0 - YC3) I68
(YD4)	R32A	PORT C SEC. 1 ENABLE	(YD4 - YD7) I46
(YD5)	R32	PORT C SEC. 3 ENABLE	(YD0 - YD3) I48
(YD5)	R32'	PORT C SEC. 3 ENABLE'	(YC0 - YC3) I76
(YD5)	R32A	PORT C SEC. 3 ENABLE	(YD4 - YD7) I48

A-8421



A-5911

CRAY Y-MP
ERROR CORRECTION CODE

0 - OK	40 - 69	100 - 70	140 - D	200 - 71	240 - D	300 - D	340 - 24
1 - 64	41 - D	101 - D	141 - M	201 - D	241 - M	301 - M	341 - D
2 - 65	42 - D	102 - D	142 - M	202 - D	242 - M	302 - M	242 - D
3 - D	43 - M	103 - M	143 - D	203 - M	243 - D	303 - D	343 - 27
4 - 66	44 - D	104 - D	144 - M	204 - D	244 - M	304 - M	344 - D
5 - D	45 - M	105 - M	145 - D	205 - M	245 - D	305 - D	345 - 29
6 - D	46 - M	106 - M	146 - D	206 - M	246 - D	306 - D	346 - 30
7 - 32	47 - D	107 - D	147 - 38	207 - D	247 - 34	307 - 36	347 - D
10 - 67	50 - D	110 - D	150 - M	210 - D	250 - M	310 - M	350 - D
11 - D	51 - M	111 - M	151 - M	211 - M	251 - D	311 - D	351 - 25
12 - D	52 - M	112 - M	152 - D	212 - M	252 - D	312 - D	352 - 26
13 - 40	53 - D	113 - D	153 - 46	213 - D	253 - 42	313 - 44	353 - D
14 - D	54 - M	114 - M	154 - D	214 - M	254 - D	314 - D	354 - 28
15 - 48	55 - D	115 - D	155 - 54	215 - D	255 - 50	315 - 52	355 - D
16 - 56	56 - D	116 - D	156 - 62	216 - D	256 - 58	316 - 60	356 - D
17 - D	57 - M	117 - M	157 - D	217 - M	257 - D	317 - D	357 - 31
20 - 68	60 - D	120 - D	160 - 00	220 - D	260 - 08	320 - 16	360 - D
21 - D	61 - M	121 - M	161 - D	221 - M	261 - D	321 - D	361 - M
22 - D	62 - M	122 - M	162 - D	222 - M	262 - D	322 - D	362 - M
23 - M	63 - D	123 - D	163 - 03	223 - D	263 - 11	323 - 19	363 - D
24 - D	64 - M	124 - M	164 - D	224 - M	264 - D	324 - D	364 - M
25 - M	65 - D	125 - D	165 - 05	225 - D	265 - 13	325 - 21	365 - D
26 - M	66 - D	126 - D	166 - 06	226 - D	266 - 14	326 - 22	366 - D
27 - D	67 - 35	127 - 37	167 - D	227 - 33	267 - D	327 - D	367 - 39
30 - D	70 - M	130 - M	170 - D	230 - M	270 - D	330 - D	370 - M
31 - M	71 - D	131 - D	171 - 01	231 - D	271 - 09	331 - 17	371 - D
32 - M	72 - D	132 - D	172 - 02	232 - D	272 - 10	332 - 18	372 - D
33 - D	73 - 43	133 - 45	173 - D	233 - 41	273 - D	333 - D	373 - 47
34 - M	74 - D	134 - D	174 - 04	234 - D	274 - 12	334 - 20	374 - D
35 - D	75 - 51	135 - 53	175 - D	235 - 49	275 - D	335 - D	375 - 55
36 - D	76 - 59	136 - 61	176 - D	236 - 57	276 - D	336 - D	376 - 63
37 - M	77 - D	137 - D	177 - 07	237 - D	277 - 15	337 - 23	377 - D

D - Double Error
M - Multiple Error

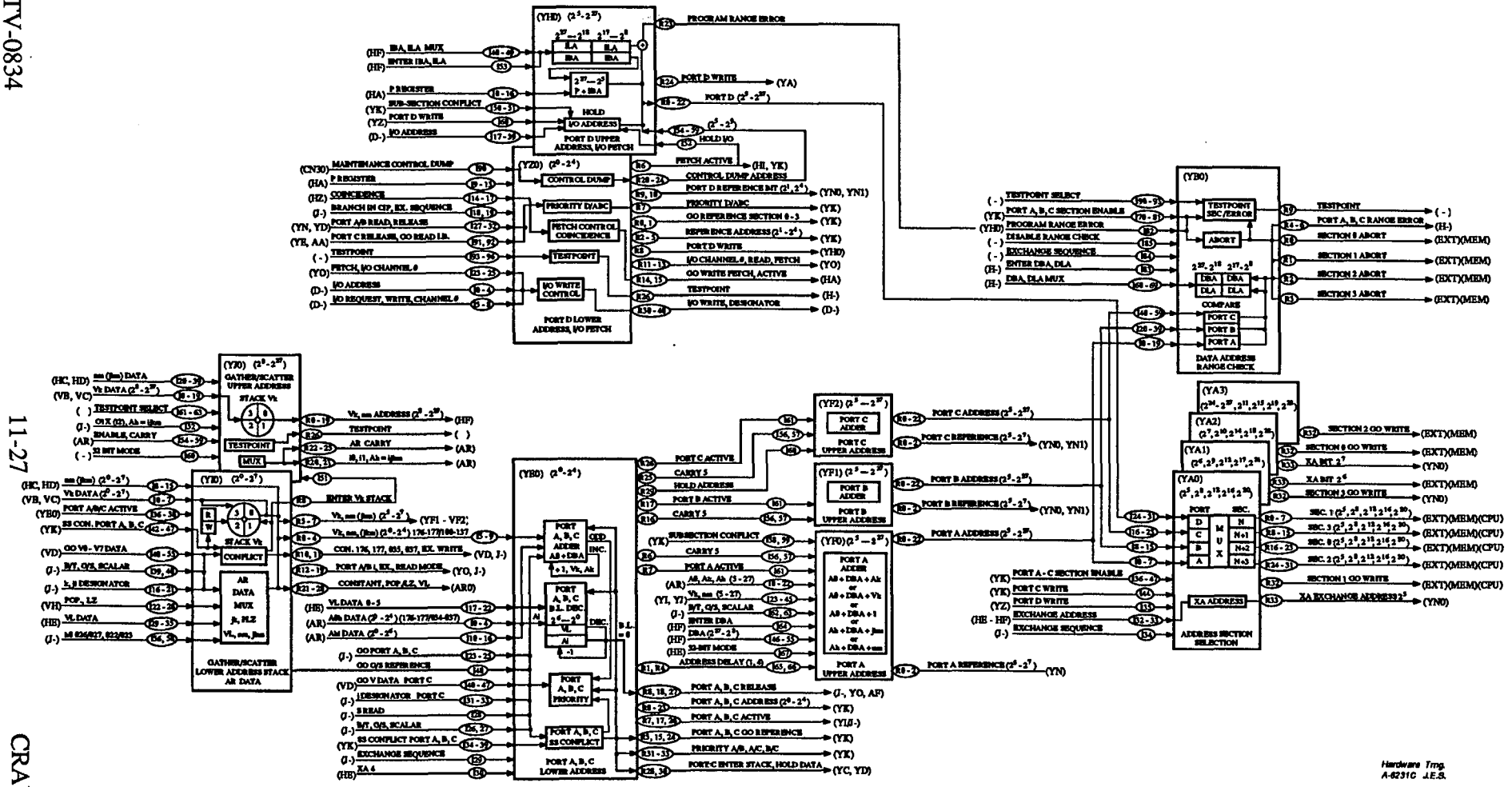
Any change of state of a single bit in memory causes an odd number of syndrome bits to be set to 1. A double error (an error in 2 bits) appears as an even number of syndrome bits set to 1.

The matrix is designed so that:

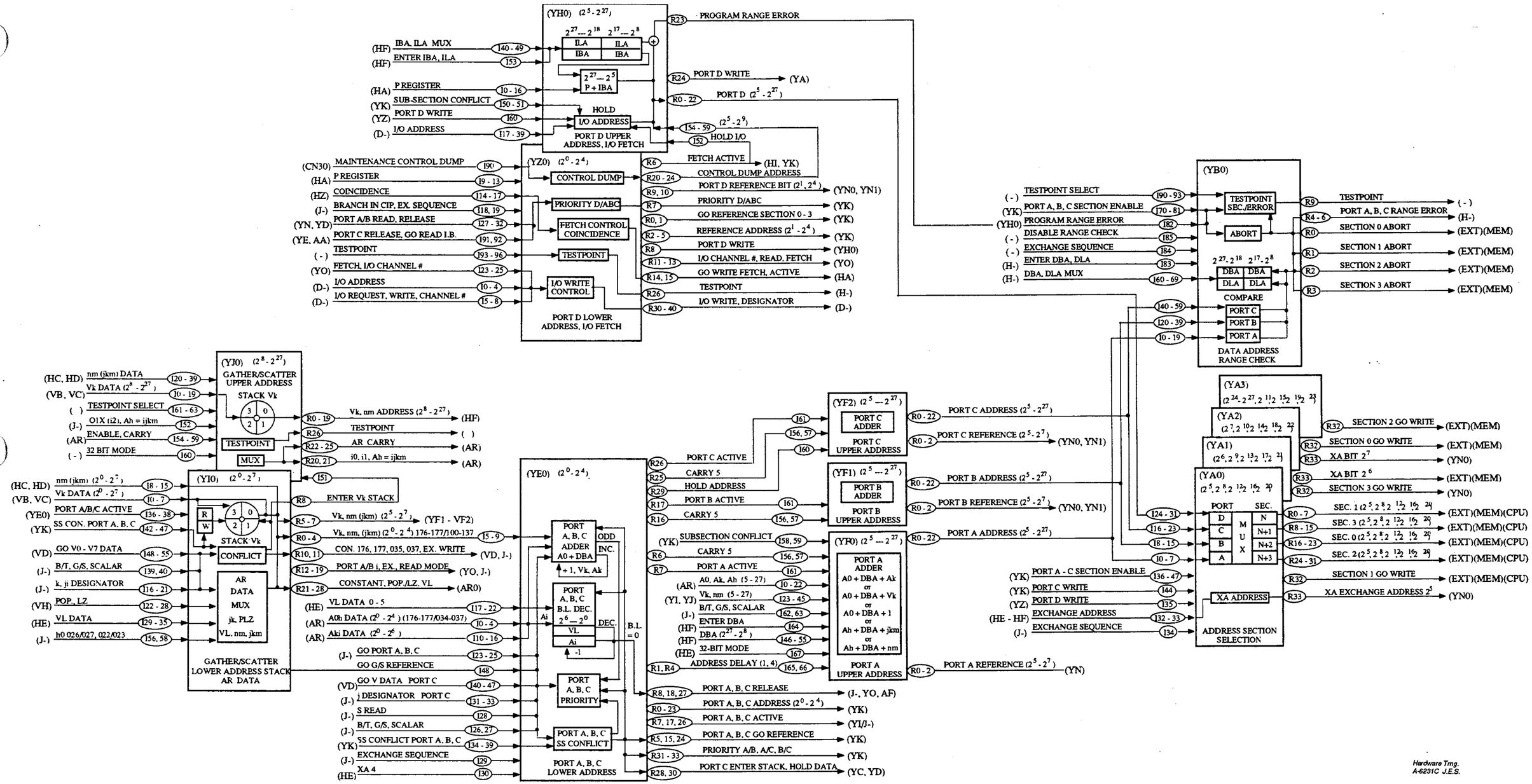
- If all syndrome bits are 0, no error is assumed.
- If only 1 syndrome bit is 1, the associated check bit is in error.
- If more than 1 syndrome bit is 1 and the parity of syndrome bits S0 through S7 is even, then a double error (or an even number of bit errors) occurred within the data bits or check bits.
- If more than 1 syndrome bit is 1 and the parity of all syndrome bits is odd, then a single and correctable error is assumed to have occurred. The syndrome bits can be decoded to identify the bit in error.
- If 3 or more memory bits are in error, the parity of all syndrome bits is odd and results are ambiguous.

CRAY Y-MP SYNDROME CODES

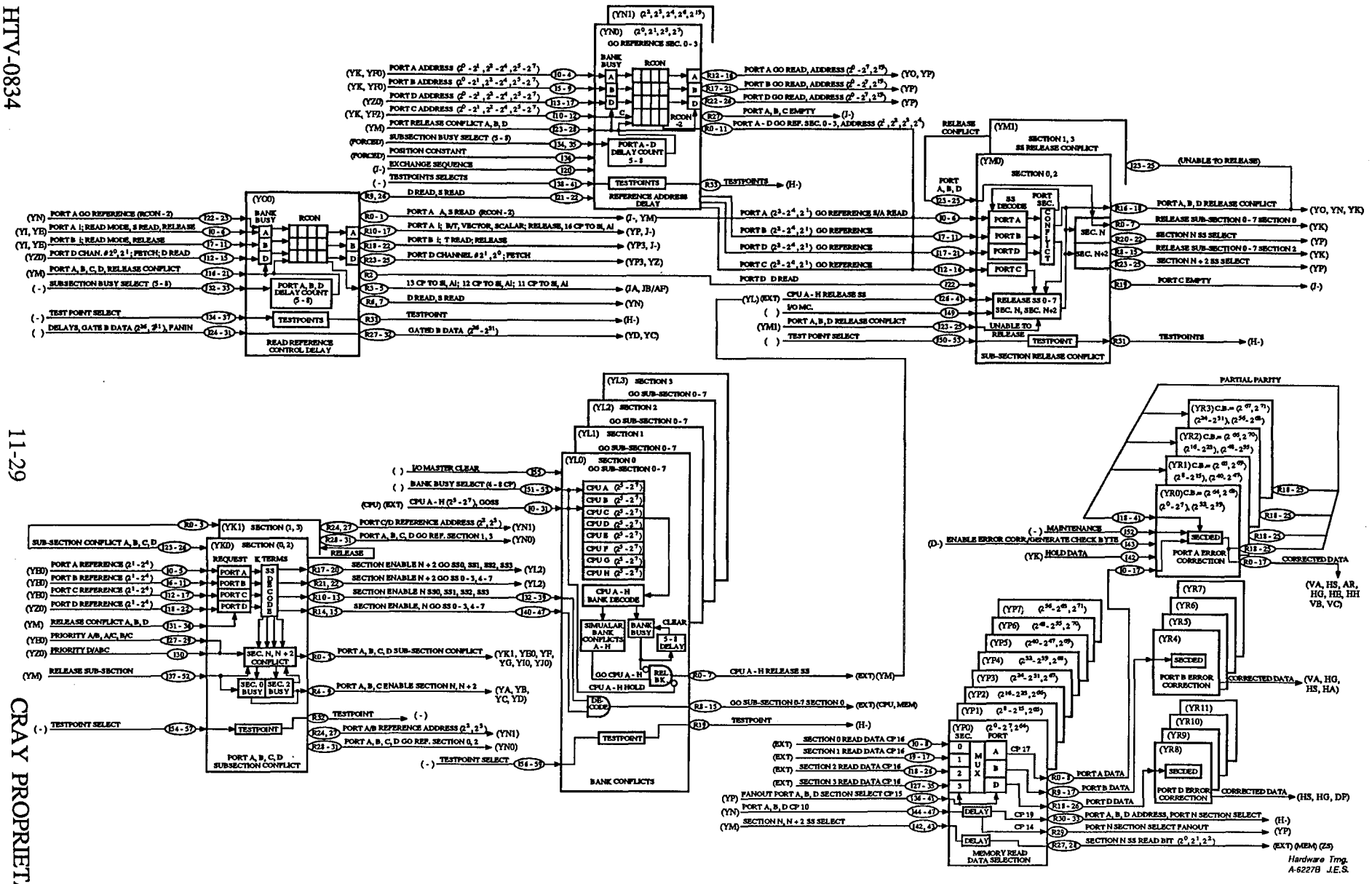
YM11/14A



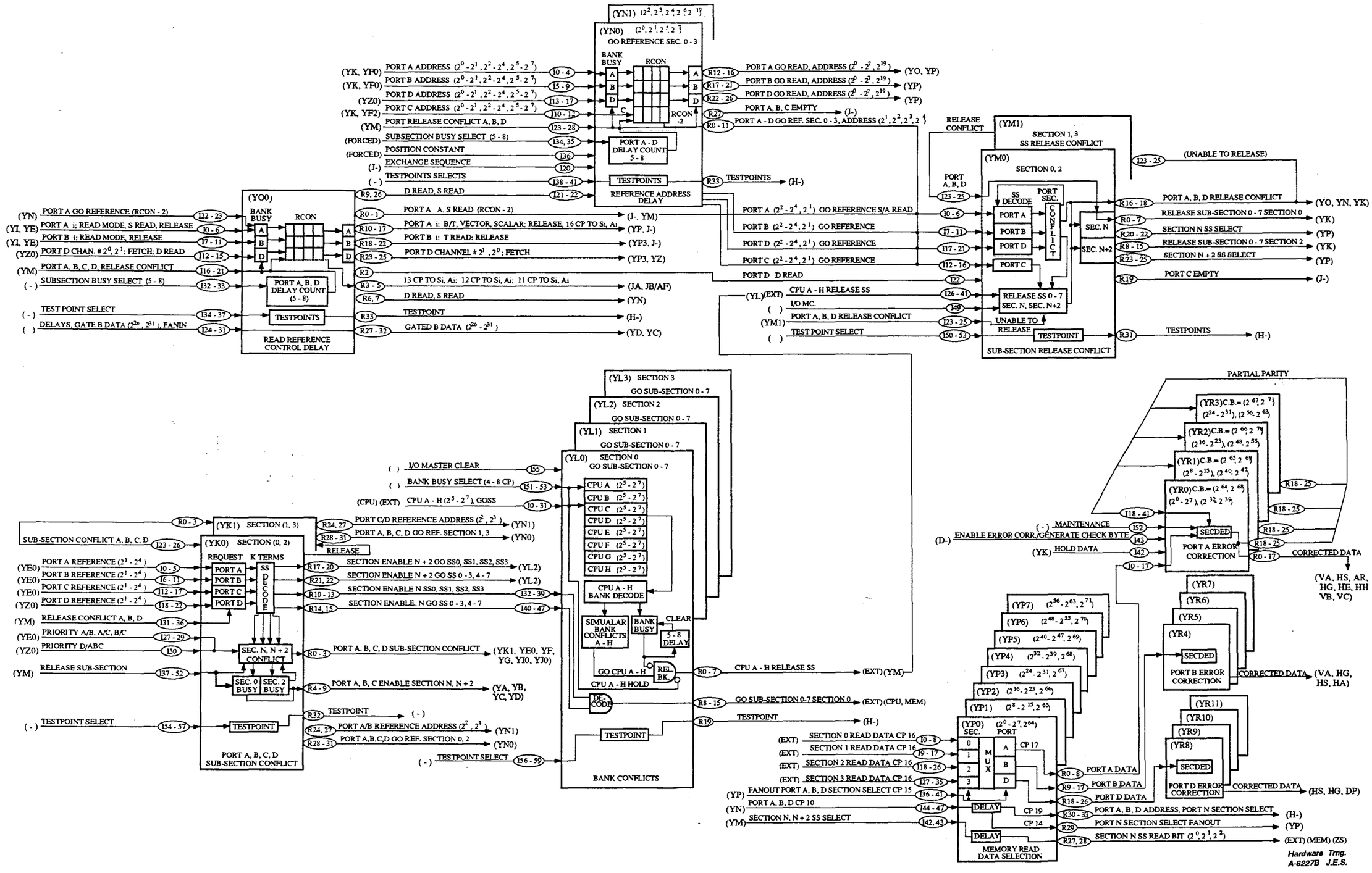
CRAY Y-MP MEMORY CONTROL BLOCK DIAGRAM
ADDRESS SUMMATION PORT A, B, C, D SECTION SELECTION



CRAY Y-MP MEMORY CONTROL BLOCK DIAGRAM
ADDRESS SUMMATION PORT A, B, C, D SECTION SELECTION



CRAY Y-MP PORT A - D REFERENCE CONTROL



CRAY Y-MP PORT A - D REFERENCE CONTROL

(YP0-YP7) OPTION FANOUTS

Section 0 - 3 Subsection Readout Select

OPTION	TERM	DESCRIPTION	DESTINATION
(YP0)	R27	Section 0 Readout 2^0 Select	(EXT) (MEM.) (ZS)
(YP1)	R27	Section 0 Readout 2^1 Select	(EXT) (MEM.) (ZS)
(YP2)	R27	Section 0 Readout 2^2 Select	(EXT) (MEM.) (ZS)
(YP4)	R27	Section 1 Readout 2^0 Select	(EXT) (MEM.) (ZS)
(YP5)	R27	Section 1 Readout 2^1 Select	(EXT) (MEM.) (ZS)
(YP6)	R27	Section 1 Readout 2^2 Select	(EXT) (MEM.) (ZS)
(YP0)	R28	Section 2 Readout 2^0 Select	(EXT) (MEM.) (ZS)
(YP1)	R28	Section 2 Readout 2^1 Select	(EXT) (MEM.) (ZS)
(YP2)	R28	Section 2 Readout 2^2 Select	(EXT) (MEM.) (ZS)
(YP4)	R28	Section 3 Readout 2^0 Select	(EXT) (MEM.) (ZS)
(YP5)	R28	Section 3 Readout 2^1 Select	(EXT) (MEM.) (ZS)
(YP6)	R28	Section 3 Readout 2^2 Select	(EXT) (MEM.) (ZS)

Port A/B/D Section Select

OPTION	TERM	DESCRIPTION	DESTINATION
(YP0)	R29	Port A Section Select 2^0	(YP0 - YP7)
(YP1)	R29	Port A Section Select 2^1	(YP0 - YP7)
(YP4)	R29	Port B Section Select 2^0	(YP0 - YP7)
(YP5)	R29	Port B Section Select 2^1	(YP0 - YP7)
(YP3)	R29	Port D Section Select 2^0	(YP0 - YP7)
(YP7)	R29	Port D Section Select 2^1	(YP0 - YP7)

Port A/B/D Address to Exchange Package

OPTION	TERM	DESCRIPTION	DESTINATION
(YP0)	R30	Port A Address bit 2^0	(HG0)
(YP1)	R30	Port A Address bit 2^1	(HG0)
(YP4)	R30	Port B Address bit 2^0	(HG0)
(YP5)	R30	Port B Address bit 2^1	(HG0)
(YP3)	R30	Port D Address bit 2^0	(HG0)
(YP7)	R30	Port D Address bit 2^1	(HG0)

Hardware Trng.
YM16/01 J.E.S.

BOARD A MUX. TEST POINTS

(T.P. 83) (YZ0)

0 0 0 0	Q10	Port D Conflict
0 0 0 1	B6	I/O Write
0 0 1 0	B7	I/O Channel Numbers 2^0
0 0 1 1	B8	I/O Channel Numbers 2^1
0 1 0 0	A10	Coincidence
0 1 0 1	A11	Coincidence
0 1 1 0	A12	Coincidence
0 1 1 1	A13	Coincidence
1 0 0 0	A14	Branch in CIP + Ex. Seq. + Fetch + MC + CD
1 0 0 1	A116	Exchange Sequence
1 0 1 0	D2	Fetch Active
1 0 1 1	A100	P Data 2^2 (Register Bit 0)
1 1 0 0	A101	P Data 2^3 (Register Bit 1)
1 1 0 1	A102	P Data 2^4 (Register Bit 2)
1 1 1 0	A103	P Data 2^5 (Register Bit 3)
1 1 1 1	A104	P Data 2^6 (Register Bit 4)

(T.P. 94) (YK0)

0 0 0 0	J0	Section 0 SS0 Busy
0 0 0 1	J1	Section 0 SS1 Busy
0 0 1 0	J2	Section 0 SS2 Busy
0 0 1 1	J3	Section 0 SS3 Busy
0 1 0 0	J4	Section 0 SS4 Busy
0 1 0 1	J5	Section 0 SS5 Busy
0 1 1 0	J6	Section 0 SS6 Busy
0 1 1 1	J7	Section 0 SS7 Busy
1 0 0 0	J8	Section 2 SS0 Busy
1 0 0 1	J9	Section 2 SS1 Busy
1 0 1 0	J10	Section 2 SS2 Busy
1 0 1 1	J11	Section 2 SS3 Busy
1 1 0 0	J12	Section 2 SS4 Busy
1 1 0 1	J13	Section 2 SS5 Busy
1 1 1 0	J14	Section 2 SS6 Busy
1 1 1 1	J15	Section 2 SS7 Busy

(T.P. 96) (YK1)

0 0 0 0	J0	Section 1 SS0 Busy
0 0 0 1	J1	Section 1 SS1 Busy
0 0 1 0	J2	Section 1 SS2 Busy
0 0 1 1	J3	Section 1 SS3 Busy
0 1 0 0	J4	Section 1 SS4 Busy
0 1 0 1	J5	Section 1 SS5 Busy
0 1 1 0	J6	Section 1 SS6 Busy
0 1 1 1	J1	Section 1 SS7 Busy
1 0 0 0	J2	Section 3 SS0 Busy
1 0 0 1	J3	Section 3 SS1 Busy
1 0 1 0	J4	Section 3 SS2 Busy
1 0 1 1	J5	Section 3 SS3 Busy
1 1 0 0	J12	Section 3 SS4 Busy
1 1 0 1	J13	Section 3 SS5 Busy
1 1 1 0	J14	Section 3 SS6 Busy
1 1 1 1	J15	Section 3 SS7 Busy

(T.P. 99) (YM0)

0 0 0 0	R0	Release SS0 Sec. 0
0 0 0 1	R1	Release SS1 Sec. 0
0 0 1 0	R2	Release SS2 Sec. 0
0 0 1 1	R3	Release SS3 Sec. 0
0 1 0 0	R4	Release SS4 Sec. 0
0 1 0 1	R5	Release SS5 Sec. 0
0 1 1 0	R6	Release SS6 Sec. 0
0 1 1 1	R7	Release SS7 Sec. 0
1 0 0 0	R8	Release SS0 Sec. 2
1 0 0 1	R9	Release SS1 Sec. 2
1 0 1 0	R10	Release SS2 Sec. 2
1 0 1 1	R11	Release SS3 Sec. 2
1 1 0 0	R12	Release SS4 Sec. 2
1 1 0 1	R13	Release SS5 Sec. 2
1 1 1 0	R14	Release SS6 Sec. 2
1 1 1 1	R15	Release SS7 Sec. 2

(T.P. 120) (YM1)

0 0 0 0	R0	Release SS0 Sec. 1
0 0 0 1	R1	Release SS1 Sec. 1
0 0 1 0	R2	Release SS2 Sec. 1
0 0 1 1	R3	Release SS3 Sec. 1
0 1 0 0	R4	Release SS4 Sec. 1
0 1 0 1	R5	Release SS5 Sec. 1
0 1 1 0	R6	Release SS6 Sec. 1
0 1 1 1	R7	Release SS7 Sec. 1
1 0 0 0	R8	Release SS0 Sec. 3
1 0 0 1	R9	Release SS1 Sec. 3
1 0 1 0	R10	Release SS2 Sec. 3
1 0 1 1	R11	Release SS3 Sec. 3
1 1 0 0	R12	Release SS4 Sec. 3
1 1 0 1	R13	Release SS5 Sec. 3
1 1 1 0	R14	Release SS6 Sec. 3
1 1 1 1	R15	Release SS7 Sec. 3

Hardware Trng.
YM31/01 D.H.

BOARD B MUX. TEST POINTS

(T.P. 01) (YB0)

0 0 0 0	Q0	Port A Section 0 Enable
0 0 0 1	Q1	Port A Section 1 Enable
0 0 1 0	Q2	Port A Section 2 Enable
0 0 1 1	Q3	Port A Section 3 Enable
0 1 0 0	Q10	Port B Section 0 Enable
0 1 0 1	Q11	Port B Section 1 Enable
0 1 1 0	Q12	Port B Section 2 Enable
0 1 1 1	Q13	Port B Section 3 Enable
1 0 0 0	Q20	Port C Section 0 Enable
1 0 0 1	Q21	Port C Section 1 Enable
1 0 1 0	Q22	Port C Section 2 Enable
1 0 1 1	Q23	Port C Section 3 Enable
1 1 0 0	R4	Port A Data Range Error
1 1 0 1	R5	Port B Data Range Error
1 1 1 0	R6	Port C Data Range Error
1 1 1 1	W0	Program Range Error

(T.P. 82) (YJ0)

0 0 0	X11	Port A Active
0 0 1	X12	Port B Active
0 1 0	X13	Port C Active
0 1 1	G6	Go Vk Data
1 0 0	X14	Port A Conflice
1 0 1	X15	Port B Conflict
1 1 0	X16	Port C Conflict
1 1 1	X17	G/S Active

(T.P. 03) (YN0)

0 0 0 0	R12	Port A Reference Go Read
0 0 0 1	R13	Port A Address 2^0
0 0 1 0	R14	Port A Address 2^1
0 0 1 1	R15	Port A Address 2^5
0 1 0 0	R17	Port B Reference Go Read
0 1 0 1	R18	Port B Address 2^0
0 1 1 0	R19	Port B Address 2^1
0 1 1 1	R20	Port B Address 2^5
1 0 0 0	C140	Port C Reference Go Section 0/2
1 0 0 1	C141	Port C Reference Go Section 1/3
1 0 1 0	C142	Port C Reference Address 2^1
1 0 1 1	R27	Port A/B/C Empty
1 1 0 0	R22	Port D Reference Go Read
1 1 0 1	R23	Port D Address 2^0
1 1 1 0	R24	Port D Address 2^1
1 1 1 1	R25	Port D Address 2^5

(T.P. 04) (YN1)

0 0 0 0	R12	Port A Reference Address 2^2
0 0 0 1	R13	Port A Reference Address 2^3
0 0 1 0	R14	Port A Reference Address 2^4
0 0 1 1	R15	Port A Reference Address 2^6
0 1 0 0	R17	Port B Reference Address 2^2
0 1 0 1	R18	Port B Reference Address 2^3
0 1 1 0	R19	Port B Reference Address 2^4
0 1 1 1	R20	Port B Reference Address 2^6
1 0 0 0	C140	Port C Reference Address 2^2
1 0 0 1	C141	Port C Reference Address 2^3
1 0 1 0	C142	Port C Reference Address 2^4
1 0 1 1	R27	
1 1 0 0	R22	Port D Reference Address 2^2
1 1 0 1	R23	Port D Reference Address 2^3
1 1 1 0	R24	Port D Reference Address 2^4
1 1 1 1	R25	Port D Reference Address 2^6

Hardware Trng.
YM31/02 D.H.

BOARD C MUX. TEST POINTS

(T.P. 120) (YL0)

0 0 0 0	K0	CPU A - H Request Bank 0
0 0 0 1	K1	CPU A - H Request Bank 1
0 0 1 0	K2	CPU A - H Request Bank 2
0 0 1 1	K3	CPU A - H Request Bank 3
0 1 0 0	K4	CPU A - H Request Bank 4
0 1 0 1	K5	CPU A - H Request Bank 5
0 1 1 0	K6	CPU A - H Request Bank 6
0 1 1 1	K7	CPU A - H Request Bank 7
1 0 0 0	A3'	CPU A Go SS
1 0 0 1	A13'	CPU B Go SS
1 0 1 0	A23'	CPU C Go SS
1 0 1 1	A33'	CPU D Go SS
1 1 0 0	A43'	CPU E Go SS
1 1 0 1	A53'	CPU F Go SS
1 1 1 0	A63'	CPU G Go SS
1 1 1 1	A73'	CPU H Go SS

(T.P. 121) (YL2)

0 0 0 0	K0	CPU A - H Request Bank 0
0 0 0 1	K1	CPU A - H Request Bank 1
0 0 1 0	K2	CPU A - H Request Bank 2
0 0 1 1	K3	CPU A - H Request Bank 3
0 1 0 0	K4	CPU A - H Request Bank 4
0 1 0 1	K5	CPU A - H Request Bank 5
0 1 1 0	K6	CPU A - H Request Bank 6
0 1 1 1	K7	CPU A - H Request Bank 7
1 0 0 0	A3'	CPU A Go SS
1 0 0 1	A13'	CPU B Go SS
1 0 1 0	A23'	CPU C Go SS
1 0 1 1	A33'	CPU D Go SS
1 1 0 0	A43'	CPU E Go SS
1 1 0 1	A53'	CPU F Go SS
1 1 1 0	A63'	CPU G Go SS
1 1 1 1	A73'	CPU H Go SS

Hardware Trng.
YM31/03 D.H.

BOARD D MUX. TEST POINTS

(T.P. 66) (JG0)

0 0 0 0	P0	CIP k 2^0
0 0 0 1	P1	CIP k 2^1
0 0 1 0	P2	CIP k 2^2
0 0 1 1	P103	CIP j 2^0
0 1 0 0	P104	CIP j 2^1
0 1 0 1	P105	CIP j 2^2
0 1 1 0	P6	CIP i 2^0
0 1 1 1	P7	CIP i 2^1
1 0 0 0	P8	CIP i 2^2
1 0 0 1	P9	CIP h 2^0
1 0 1 0	P10	CIP h 2^1
1 0 1 1	P11	CIP h 2^2
1 1 0 0	P12	CIP g 2^0
1 1 0 1	P13	CIP g 2^1
1 1 1 0	P14	CIP g 2^2
1 1 1 1	R25	CIP g 2^3

(T.P. 01) (YL1)

0 0 0 0	K0	CPU A - H Request Bank 0
0 0 0 1	K1	CPU A - H Request Bank 1
0 0 1 0	K2	CPU A - H Request Bank 2
0 0 1 1	K3	CPU A - H Request Bank 3
0 1 0 0	K4	CPU A - H Request Bank 4
0 1 0 1	K5	CPU A - H Request Bank 5
0 1 1 0	K6	CPU A - H Request Bank 6
0 1 1 1	K7	CPU A - H Request Bank 7
1 0 0 0	A3'	CPU A Go SS
1 0 0 1	A13'	CPU B Go SS
1 0 1 0	A23'	CPU C Go SS
1 0 1 1	A33'	CPU D Go SS
1 1 0 0	A43'	CPU E Go SS
1 1 0 1	A53'	CPU F Go SS
1 1 1 0	A63'	CPU G Go SS
1 1 1 1	A73'	CPU H Go SS

(T.P. 02) (YL3)

0 0 0 0	K0	CPU A - H Request Bank 0
0 0 0 1	K1	CPU A - H Request Bank 1
0 0 1 0	K2	CPU A - H Request Bank 2
0 0 1 1	K3	CPU A - H Request Bank 3
0 1 0 0	K4	CPU A - H Request Bank 4
0 1 0 1	K5	CPU A - H Request Bank 5
0 1 1 0	K6	CPU A - H Request Bank 6
0 1 1 1	K7	CPU A - H Request Bank 7
1 0 0 0	A3'	CPU A Go SS
1 0 0 1	A13'	CPU B Go SS
1 0 1 0	A23'	CPU C Go SS
1 0 1 1	A33'	CPU D Go SS
1 1 0 0	A43'	CPU E Go SS
1 1 0 1	A53'	CPU F Go SS
1 1 1 0	A63'	CPU G Go SS
1 1 1 1	A73'	CPU H Go SS

(T.P. 06) (YO0)

0 0 0 0	A92	Port A Release Conflict
0 0 0 1	B92	Port B Release Conflict
0 0 1 0	C92	Port D Release Conflict
0 0 1 1	R10	Port A i2
0 1 0 0	R11	Port A B/T, Scalar
0 1 0 1	R12	Port A V, Scalar
0 1 1 0	R13	Port A Release
0 1 1 1	R14	Port A 10 CP to Ai
1 0 0 0	R15	Port A 10 CP to Si
1 0 0 1	R8	Port A i0
1 0 1 0	R9	Port A i1
1 0 1 1	R18	Port B i0
1 1 0 0	R19	Port B i1
1 1 0 1	R20	Port B i2
1 1 1 0	R21	Port B Read T
1 1 1 1	R23	Port B Release

Hardware Trng.
YM31/04 D.H.

EXCHANGE MECHANISM

- Means of switching execution from program to program.
- Exchange Package - Block (16 words) of program parameters.

  Any program to be executed must have an Exchange Package defining where and how it is to be run.

  Exchange Package is 20_8 words in length.

  Must reside in lower 4096 memory locations.

  Must start on a 20_8 word boundary.

- Exchange Sequence - The process which deactivates the current Exchange Package and puts it into memory. It then loads from memory, a new Exchange Package and activates it.
- Conditions that cause an Exchange Sequence.

  Deadstart Sequence

  Interrupt Flag Set (F register)

  Program Exit (004, 000 instruction)

Deadstart Sequence - Setting and dropping I/O M.C. causes input channel 20 to go active. The MWS can transfer 20000_8 words into memory or 20000_8 words from the IOS.

Setting and dropping CPU M.C. forces an exchange with Exchange address 0. XA register is set to zero by setting the CPU M.C.

Deadstarting processor 0 - 7, processor 0 performs the exchange when CPU M.C. drops. Processor 0 could set up the Deadstart Exchange Package 00 and issues a 0014j1 instruction to processor 1. Processor 0 will then set up the Deadstart Exchange Package 00, then issue a 0014j1 to processor 2. Processor 0 will set up Deadstart Exchange Package 00 and issue an 0014j1 to processor 3, and so on. All processors have now been deadstarted, and processor 0 could exchange on itself.

Interrupt Flag Set - The following interrupts can be set while in user mode: Programmable clock, MCU, Floating-point Error, Operand range, Program range, Memory Error, I/O interrupt, Error exit and Normal exit. While in monitor mode, all interrupts other than Memory Error are disabled. If the IMM (Interrupt Monitor Mode) bit is set, all interrupts except PCI, MCU, I/O and Deadlock are Enabled in monitor mode.

Program Exit - Program exit occurs from the decode of instruction (000, 004). Instruction (000) is an Error Exit instruction, instruction (004) is a normal exit.

After an exchange has occurred and the program is in monitor mode, the monitor needs to save the B register and T registers, Shared registers and Vector registers. If the Vector Not Used bit (VNU) is equal to a one, the Vector registers do not need to be saved.

Hardware Trng.
YM10/31A J.E.S.

Exchange Sequence

Before an exchange can take place, everything must run to completion in the processor that wants to perform the exchange. If a Test and Set instruction (0034) is waiting on semaphore, the P register is decremented by two or by one if the Test and Set is in NIP. The (HF) decrements the P register before it is loaded into memory.

The processor doing the exchange clears out the Buffer Valid bits and Buffer counter. Clearing the Buffer Valid bit causes a Fetch to occur after the exchange has completed. Clearing the IBAR counter causes the data which was fetched from memory to be loaded into Instruction Buffer 0 first.

Exchange R/W Sequence

Words Read From Memory using Port A

0	
1	
2	
3	
4	Words Written to Memory using Port C
5	0
6	1
7	2
10	3
11	4
12	5
13	6
14	7
15	10
16	11
17	12
	13
	14
	15
	16
	17

The Exchange Sequence functions as a block reference to memory. Port C is used on the write to memory while Port A is used for the read of memory. The read starts up 5 CPs ahead of the write to prevent Bank conflicts within the same CPU. However, Bank conflicts among the other CPUs is unavoidable and must be handled when they occur by the memory controls.

Exchange Write Sequence

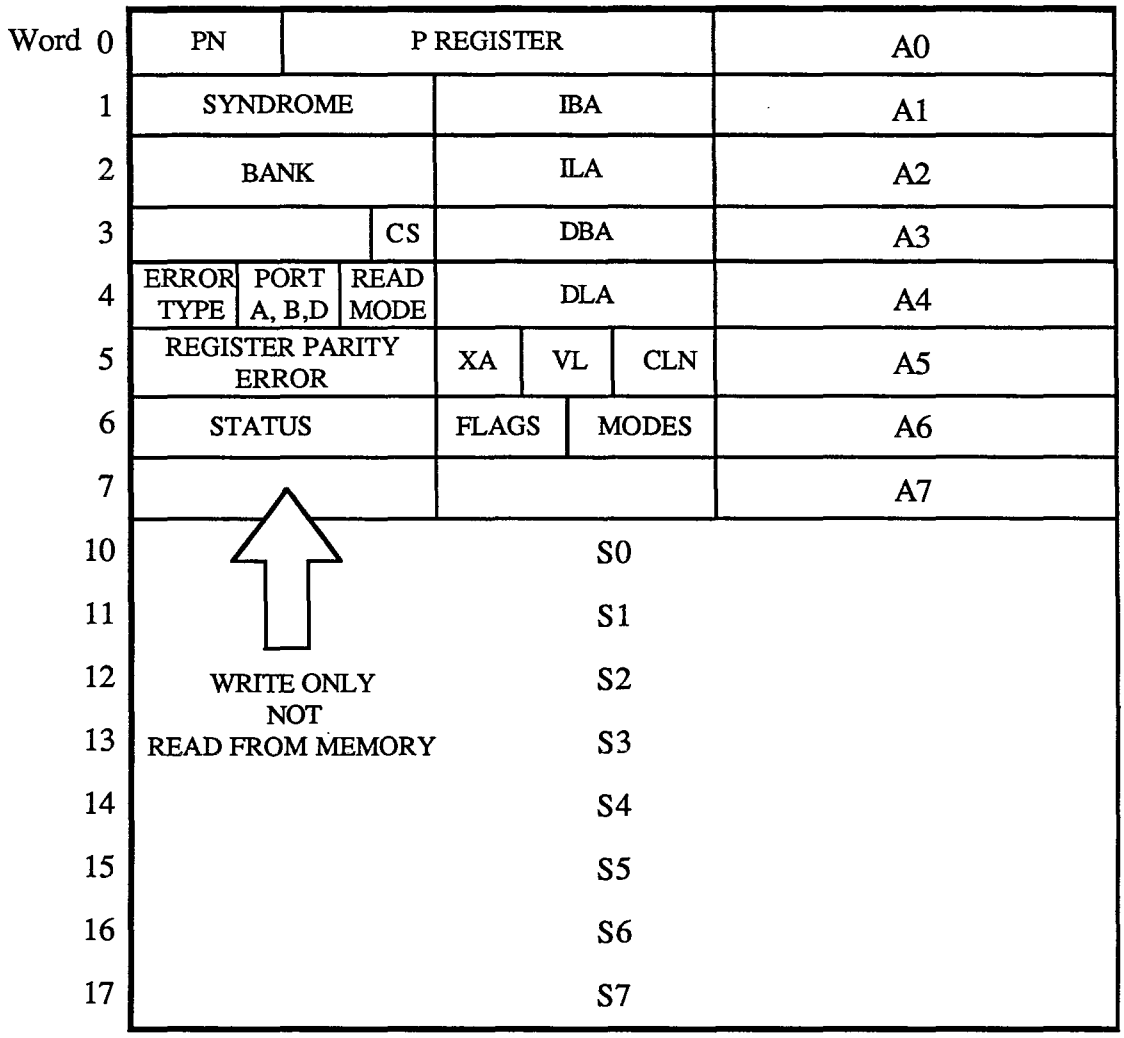
Assuming that an interrupt is set on the (HE) option which will initiate the Exchange Sequence, the interrupt is passed to the (HC) option which will set the Wait Exchange. The Wait Exchange is sent to the (HA, HZ) options to stop the P register from incrementing and also generate blank NIP, which will keep the issue circuits quiet. The Wait Exchange is held until the (JD) sends a Release

Exchange which occurs when the Exchange Sequence has completed. The (JD) option, upon receiving the Wait Exchange signal, will generate an Exchange Request as long as the A/S/V registers are quiet and Fetch is quiet. The (JD) option will generate an Exchange Sequence which is sent to various options to initiate their Exchange Sequence counts or timers. The (YI) option, upon receiving the Exchange Sequence, will start up a Write pointer to memory which uses the Port B path to the (JG) option to address the A and S registers. The (JG) option will generate a (j and k) operand equivalent to the Write pointer values and cause a read of A0 followed by A1 - A7, then the (JG) will start over with the Write pointer equal to zero, only this time addressing S0 - S7.

The first word to be sent to memory contains A0 plus the P register and the Processor Number (PN). The P register is held on the (HA, HZ) options prior to sending the P register to memory . The P register is decremented by -1 or -2 on the (HF) option if a Test and Set were in NIP or CIP. The (HF), which is the Exchange Parameters for DLA, DBA, ILA, IBA, P register, XA, VL, CLN, Flags and Modes, will check for P-1 or P-2 signals and decrement the P register accordingly before sending the P register to the (YC, YD) options. The P register, along with A0, arrive on the (YC, YD) option at the same time. The (YC, YD) options will select the proper section to send the data to memory.

The Write Exchange address is set from the Absolute XA address which contains bit (2^{11} - 2^4), the lower 4 bits being zeroes to put the Exchange Package on 20 word boundaries. The Absolute XA address is held on the (HE) option when the Exchange Sequence starts. The XA address bit (2^4) is sent to the (YE) for the upper subsection select. Exchange address bits (2^5 - 2^{11}) are sent to the (YA) option where the proper section is selected. The (YE) will increment the Exchange address from (0 - 17), and supply the (YK) option with the section and subsection selects. The (YK) will then generate the GOSS 0 - 7 to the (YL) options which will be distributed to memory and the CPU modules to assist in determining a Bank conflict. The (YA) receives its section Enables from the (YK) option. The (YA) will send the address bits (2^5 - 2^{11}) to the proper section in memory, along with sending bank bits (2^5 - 2^7) to the CPU modules to be checked for Bank conflicts on the (YL) option among the other CPU references. Because of the sequence counters and controls, up to eight references can be stacked on the (YC/D) options prior to stopping on a Bank conflict.

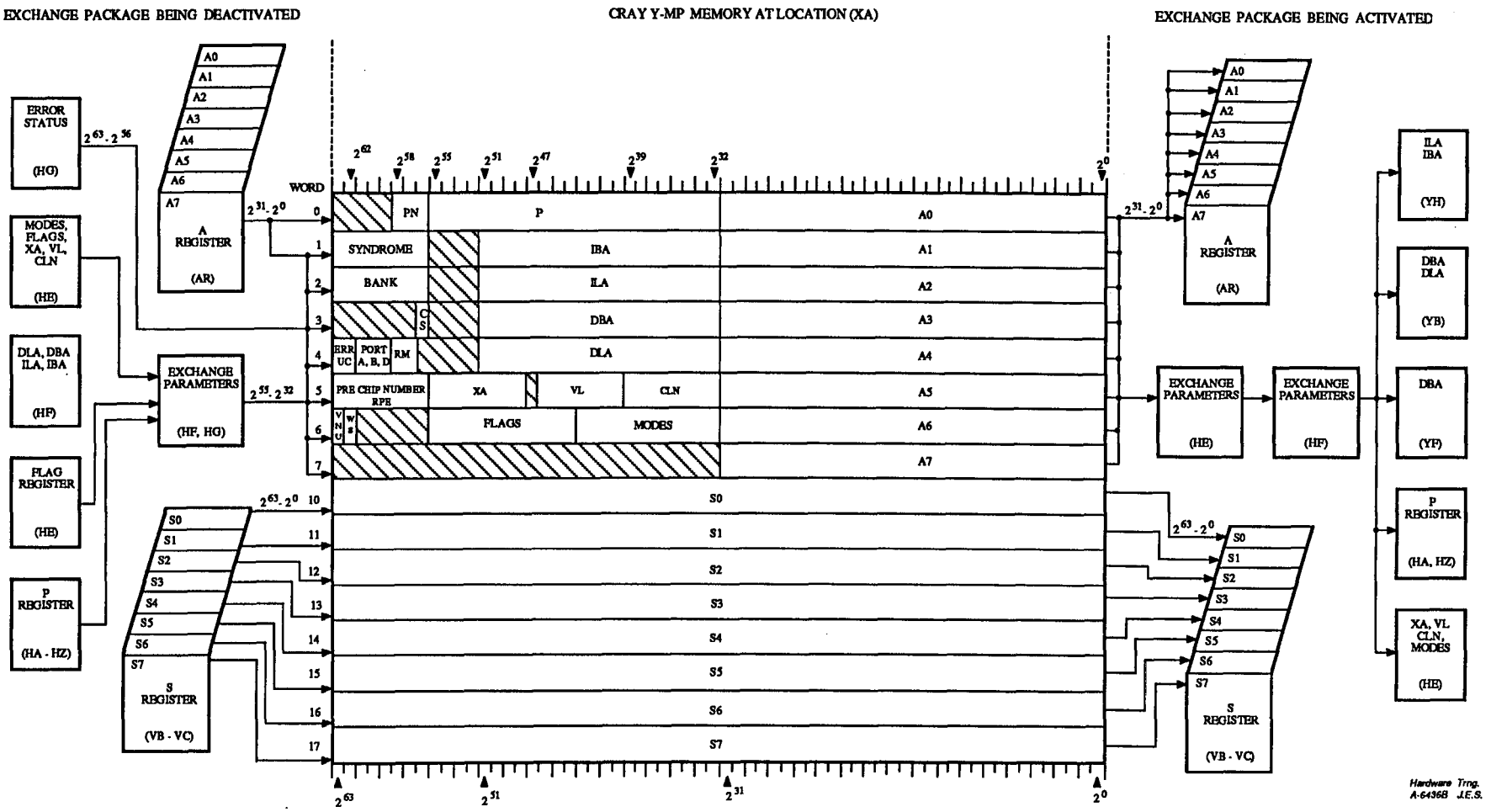
The write exchange parameters are passed from the (HE) option to the (HF) option . The (HF) has an Exchange Sequence counter which will send off the appropriate exchange parameters to the (YC, YD) to be joined with the A register data to make up a 64-bit word write to memory. The figure on the following page shows what is in words 0 - 17.



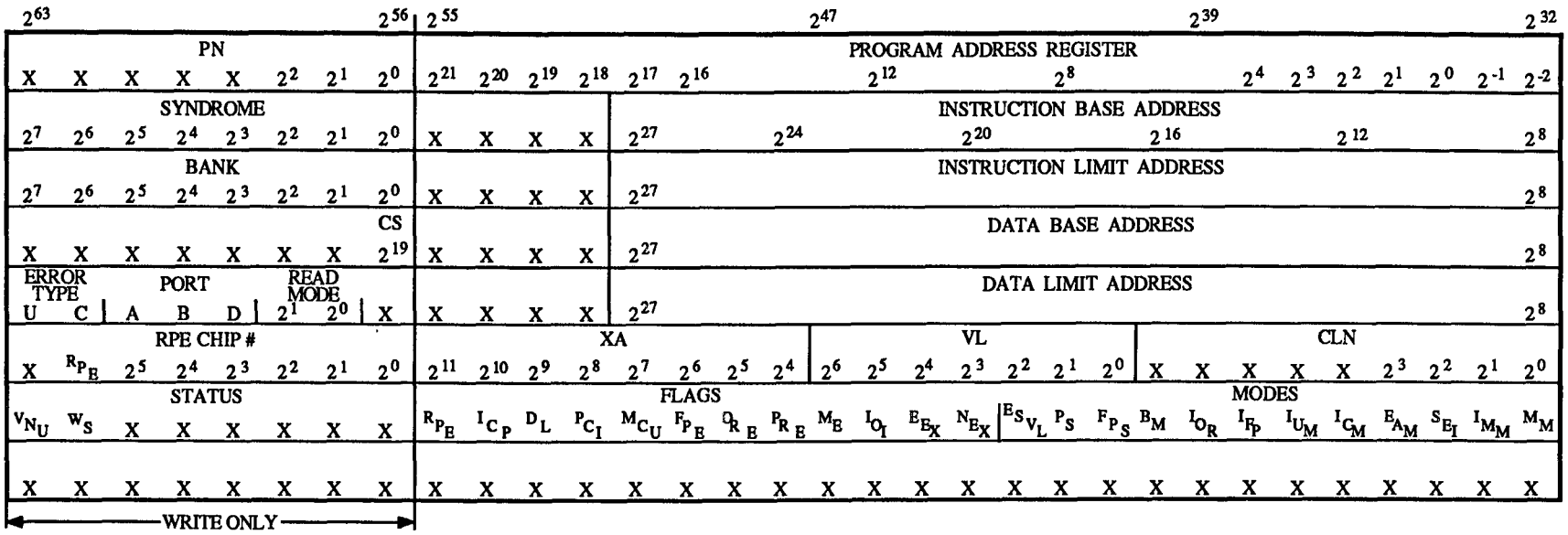
Exchange Read Sequence

The Exchange Read Sequence of memory is ahead of the write sequence by 5 CPs to prevent Bank conflicts within the same CPU. The 5 CPs happen to be the access time of the 64K x 1 memory chips. The read sequence is initiated similar to the write sequence by a flag being set, instruction (000000, 004000) or CPU M.C. starting the Exchange Sequence. The Exchange address is passed to memory from the (HE) to the (YA) option and then to memory. The read control is initiated on the (YI) option by receiving the Exchange Sequence from the (JD). The (YI) will start up a Read pointer which is passed to the (YN/O) options to time the writing of the A/S registers taking into account any Bank conflict which could occur among the CPUs. The read parameters along with A register data will first start arriving at CP 19 from memory, on the (YP) option. The P register is sent from the (YQ) to the (HE) option and then to the (HF) were the P register is muxed out 6 bits at a time to the (HA/Z). The entire P register is loaded into the (HA/Z) at CP 27. Next to arrive from

memory, is the IBA and A1. The IBA is routed from the (HE) to the (HF) where the (HF) will divide the IBA in half and send out the lower half first to the (YH) and then the next clock period to the upper half. The ILA, DBA, DLA will follow the same sequence of events. The XA, VL and Modes arriving from memory are sent to the (HE) option and not passed to the (HF). Following the Exchange Sequence is the fetch operation caused by the Exchange Sequence clearing the buffer valid bits. The combined exchange and fetch would take 52 CPs if no Bank conflict had occurred. The (JD) will generate a Release Exchange which is sent to the (HC) option which will drop Wait Exchange. The (JD) Release Exchange is caused by Port C being released on the (YE) option at CP 27.



CRAY Y-MP EXCHANGE DATA PATHS



READ MODE

2^1 2^0	PORT A	PORT B	PORT D
0 0	EX		FETCH
0 1	B	T	LOSP
1 0	VECTOR	VECTOR	HISP
1 1	A/S		SSD

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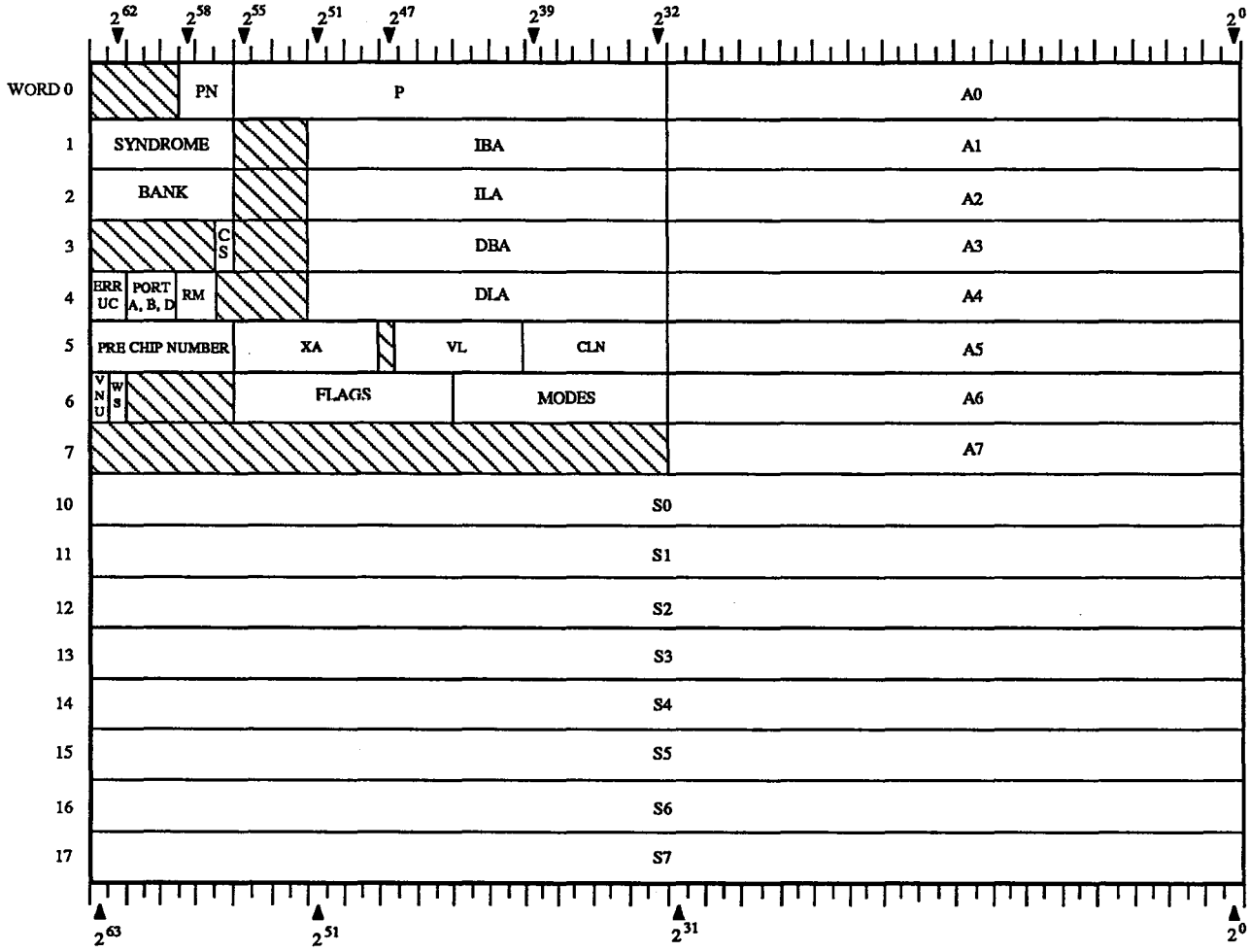
CRAY Y-MP EXCHANGE PACKAGE



FIELD	WORD	BIT
PROCESSOR NUMBER (PN)	0	$2^{58}-2^{56}$
SYNDROME (S)	1	$2^{63}-2^{56}$
READ ADDRESS BANK (BANK)	2	$2^{63}-2^{56}$
READ ADDRESS CHIP SELECT (CS)	3	2^{56}
READ ERROR TYPE (ERR)	4	$2^{68}-2^{62}$
PORT (PORT)	4	$2^{61}-2^{59}$
READ MODE (RM)	4	$2^{58}-2^{57}$
REGISTER PARITY ERROR CHIP (RPE)	5	$2^{61}-2^{56}$
VECTOR NOT USED (VNU)	6	2^{63}
WAIT ON SEMAPHORE (WS)	6	2^{62}
PROGRAM ADDRESS REGISTER (P)	0	$2^{55}-2^{32}$
INSTRUCTION BASE ADDRESS (IBA)	1	$2^{51}-2^{32}$

FIELD	WORD	BIT
INSTRUCTION LIMIT ADDRESS (ILA)	2	$2^{51}-2^{32}$
DATA BASE ADDRESS (DBA)	3	$2^{51}-2^{32}$
DATA LIMIT ADDRESS (DLA)	4	$2^{51}-2^{32}$
EXCHANGE ADDRESS REGISTER (XA)	5	$2^{55}-2^{48}$
VECTOR LENGTH REGISTER (VL)	5	$2^{47}-2^{41}$
CLUSTER NUMBER (CLN)	5	$2^{35}-2^{32}$
FLAG REGISTER (FLAGS)	6	$2^{55}-2^{44}$
MODE REGISTER (MODES)	6	$2^{43}-2^{32}$
EIGHT A REGISTER CONTENTS	0-7	$2^{31}-2^{0}$
EIGHT S REGISTER CONTENTS	0-7	$2^{63}-2^{0}$

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CRAY Y-MP EXCHANGE PACKAGE

EXCHANGE PACKAGE DESCRIPTION

PN - Processor Number

Word 0, bit (2^{58} - 2^{56})
The contents of the 3-bit PN field in the Exchange Package shows the CPU in which the exchange executed. This value is not read into the CPU; it is a constant inserted only into a package being stored.

S - Syndrome Bits

Word 1, bit (2^{63} - 2^{56})
If a SECDED Error occurred on a memory read or on an I/O channel, the 8 Syndrome bits are stored in this field of the Exchange Package.

BANK - Read Address Bank

Word 2, bit (2^{63} - 2^{56})
If an error was detected during a Memory Read operation, the number of the bank from which the error came is kept in this 8-bit field. The bank number is considered to be bits (2^{0}) through (2^{7}) of the Read address.

CS - Read Address Chip Select

Word 3, bit (2^{56})
If an error was detected during a Memory Read operation, the chip select value of the Read address is filed in this location. This CS bit is considered to be bit (2^{19}) of the Memory Read address.

ERR - Read Error Type

Word 4, bits (2^{63} - 2^{62})
The I/O or Memory Error can be either correctable or uncorrectable. Bit (2^{63}) (U) is set if the error is uncorrectable. Bit (2^{62}) (C) is set if the error is correctable.

PORT - Read Port A, B and D

Word 4, bits (2^{61} - 2^{59})
If an error is detected on a memory read, the port that was active at the time is shown in this 3-bit field. Ports A, B and D are represented by bits (2^{61}, 2^{60} and 2^{59}) respectively. These bits are used in conjunction with the Read Mode Field bits to identify the operation that had the error.

RM - Read Mode

Word 4, bits (2^{58} - 2^{57})
The two Read Mode bits, (2^{58}) and (2^{57}) of word four, are used along with the PORT field bits to determine what kind of a transfer occurred when the error was detected. The table on the following page shows the interpretations of the Port and Mode field bits.

READ MODE

2^1 2^0	PORT A	PORT B	PORT D
0 0	EX		Fetch
0 1	B	T	LOSP
1 0	Vector	Vector	HISP
1 1	A/S		SSD

XA - Exchange Address

Word 5, bits (2^{48} - 2^{55})
The 8-bit XA field specifies the address of the first word of the next Exchange Package. When the current execution interval ends, the Exchange Package read from memory will be the package starting at the XA address. The XA field contains bits (2^{11}) through (2^4) of the address. The lower four address bits are not needed because the Exchange Package can only begin on a 16-word boundary. The address size requires that the Absolute address be in the lower 4,096 ($10{,}000_8$) words of memory.

VL - Vector Length

Word 5, bits (2^{47} - 2^{41})
The VL field holds the contents of the Vector Length register. The 7-bit field contains the number of elements to be operated on in the Vector register. If VL = 000 or VL = 100_8, all vector elements are used within the vector instructions.

CLN - Cluster Number

Word 5, bits (2^{35} - 2^{32})
The CLN field has a 4-bit Cluster Number to be loaded into the Cluster Number register. The number selects the group, or cluster, of shared registers (SB, ST and SM) the CPU can access. The remaining 4 bits in the CLN field are reserved for future use. The CRAY Y-MP uses nine clusters.

Flags

Word 5, bits (2^{55} - 2^{44})
The table below lists the bit assignments for the flags field in the Exchange Package. Meanings for these bits are similar to the meanings for the CRAY X-MP/48. The following flags being set will cause the hardware to perform an exchange.

Flag register bit assignments

Word	Binary Exponent	Name
6	2^{55}	Register Parity Error (RPE) (Not used)
6	2^{54}	Interrupt From Internal CPU (ICP)
6	2^{53}	Deadlock (DL)
6	2^{52}	Programmable Clock Interrupt (PCI)
6	2^{51}	MCU Interrupt (MCU)
6	2^{50}	Floating-point Error (FPE)
6	2^{49}	Operand Range Error (ORE)
6	2^{48}	Program Range Error (PRE)
6	2^{47}	Memory Error (ME)
6	2^{46}	I/O Interrupt (IOI)
6	2^{45}	Error Exit (EEX)
6	2^{44}	Normal Exit (NEX)

RPE - Register Parity Error:

Word 6, bit (2^{55}) - Flags a parity error from the (VS) or (HS) options, which includes Vector registers, Instruction buffers, T- registers, B- registers, and SB/ST registers.

ICP - Interrupt from Internal CPU

Word 6, bit (2^{54}) - Occurs when another CPU issues a 0014jl (j = 0 - 7) instruction.

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DL - Dead Lock

Word 6, bit (2^{53})
Occurs when all CPUs in the same cluster are holding issue on a test and set instruction (0034). Cluster numbers are not equal in at least two CPUs, and a CPU is a Hold Issue on a test and set instruction.

PCI - Programmable Clock Interrupt

Word 6, bit (2^{52})
Occurs when the interrupt countdown counter in the programmable clock equals zero. Thirty-two-bit register loaded from (Sj).

MCU - MCU Interrupt

Word 6, bit (2^{51})
Occurs when the MIOP sends this signal.

FPE - Floating-point Error

Word 6, bit (2^{50})
Occurs when a Floating-point Range Error occurs in any of the Floating-point units, and the Enable Floating-point Interrupt flag is set.

ORE - Operand Range Error

Word 6, bit (2^{49})
Occurs when a data reference is made outside the boundaries of the Data Base address and Data Limit address and the Enable Operand Range Interrupt flag is set.

PRE - Program Range Error

Word 6, bit (2^{48})
Occurs when a Fetch is made outside the boundaries of the Instruction Base and Instruction Limit address.

ME - Memory Error

Word 6, bit (2^{47})
Occurs when a correctable or uncorrectable Memory Error and the corresponding Memory Error mode bit is set.

IOI - I/O Interrupt

Word 6, bit (2^{46})
Occurs when a Low-speed channel or the SSD channel completes a transfer.

EEX - Error Exit

Word 6, bit (2^{45})
Occurs when an 000000 instruction is issued.

NEX - Normal Exit

Word 6, bit (2^{44})
Occurs when an 004000 instruction has issued.

Status Register

The Status register contains bits that reflect the operating modes of the CPU. Instruction 073i01 transmits the status bits to the high-order bit positions of a selected S register. The table below lists the status bits and the S register bit positions assigned to each status bit.

Status register bit assignments in Si

Si Bit	Status When Bit = 1
2^{63}	Clustered, CLN not zero (CL)
2^{57}	Program state (PS)
2^{51}	Floating-point error occurred (FPS)
2^{50}	Floating-point interrupt enabled (IFP)
2^{49}	Operand range interrupt enabled (IOR)
2^{48}	Bidirectional memory enabled (BDM)
2^{42}	Processor number bit 2 (PN2)
2^{41}	Processor number bit 1 (PN1)
2^{40}	Processor number bit 0 (PN0)
2^{35}	Cluster number bit 3 (CLN3)
2^{34}	Cluster number bit 2 (CLN2)
2^{33}	Cluster number bit 1 (CLN1)
2^{32}	Cluster number bit 0 (CLN0)

Register Parity Error Test

Register chips are capable of reporting parity errors and self-testing the parity error detection and reporting logic.

Parity on a register chip is handled in groups of 8 data bits and 1 parity bit. The diagram below shows a 64-bit register with parity bits mixed in with data bits.

BYTE 7		BYTE 6		BYTE 5		BYTE 4		BYTE 3		BYTE 2		BYTE 1		BYTE 0	
P 7	D63 - 56	P6	D55 - 48	P5	D47 - 40	P4	D39 - 32	P3	D31 - 24	P2	D23 - 16	P1	D15 - 8	P0	D7 - 0

Parity Bits in 64-bit Operating Register

Each parity bit gives the whole byte odd parity. As data bits enter the operating register, the parity bits for each group of 8 bits are generated and loaded. When the data bits are read from the register, parity checking is done on each byte. If the whole byte does not have odd parity, a Register Parity error is generated.

The parity generation, checking and reporting logic is tested in maintenance mode by setting bit 6 in the Maintenance Mode register. With bit 6 set to one, the value of Maintenance Mode register bit 5 becomes the value of all parity bits.

Exchange Package

Word 5 bits

2^{63}	2^{62}	2^{61}	2^{60}	2^{59}	2^{58}	2^{57}	2^{56}
N/A	R_{PE}	2^5	2^4	2^3	2^2	2^1	2^0
	Flag	Chip Function			Chip Number		

Chip Number Bits - Meaning

CHIP FUNCTION	$2^5\,2^4\,2^3$	CHIP NUMBER $2^2\,2^1\,2^0$						
No Parity Error	0 0 0	N/A						
V Register A Board	0 0 1	0 = (VS0)	1 = (VS10)	2 = (VS20)	3 = (VS30)	4 = (VS40)	5 = (VS50)	6 = (VS60) 7 = (VS70)
V Register B Board	0 1 0	0 = (VS1)	1 = (VS11)	2 = (VS21)	3 = (VS31)	4 = (VS41)	5 = (VS51)	6 = (VS61) 7 = (VS71)
V Register C Board	0 1 1	0 = (VS2)	1 = (VS12)	2 = (VS22)	3 = (VS32)	4 = (VS42)	5 = (VS52)	6 = (VS62) 7 = (VS72)
V Register D Board	1 0 0	0 = (VS3)	1 = (VS13)	2 = (VS23)	3 = (VS33)	4 = (VS43)	5 = (VS53)	6 = (VS63) 7 = (VS73)
IB Register	1 0 1	0 = (HS0)	1 = (HS1)	2 = (HS2)	3 = (HS3)	4 = (HS4)	5 = (HS5)	6 = (HS6) 7 = (HS7)
T/B SR Register	1 1 0	0 = (HS8)	1 = (HS9)	2 = (HS10)	3 = (HS11)	4 = (HS12)	5 = (HS13)	6 = (HS14) 7 = (HS15)

10_8 - 17_8 = V Register A Board
20_8 - 27_8 = V Register B Board
30_8 - 37_8 = V Register C Board
40_8 - 47_8 = V Register D Board
50_8 - 57_8 = Instruction Buffer
60_8 - 63_8 = T Register
64_8 - 65_8 = B Register
66_8 - 67_8 = SB/ST Register

YR INPUTS

(YR0)	(YR1)	(YR2)	(YR3)	(YR10)	(YR9)	
(VS0)	(VS1)	(VS2)	(VS3)	(HS0)	(HS8)	→ I44
(VS10)	(VS11)	(VS12)	(VS13)	(HS1)	(HS9)	→ I45
(VS20)	(VS21)	(VS22)	(VS23)	(HS2)	(HS10)	→ I46
(VS30)	(VS31)	(VS32)	(VS33)	(HS3)	(HS11)	→ I47
(VS40)	(VS41)	(VS42)	(VS43)	(HS4)	(HS12)	→ I48
(VS50)	(VS51)	(VS52)	(VS53)	(HS5)	(HS13)	→ I49
(VS60)	(VS61)	(VS62)	(VS63)	(HS6)	(HS14)	→ I50
(VS70)	(VS71)	(VS72)	(VS73)	(HS7)	(HS15)	→ I51

CRAY Y-MP REGISTER PARITY ERROR

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Modes

Word 6, Bit (2^{43} - 2^{32})
The Modes field of the Exchange Package contains 12 bits that govern execution. The table below lists the Mode bit assignments. Most of the bits retain their CRAY X-MP meanings. The Extended Addressing Mode bit is explained following the table.

Mode Register bit assignments

Word	Binary Exponent	Name
6	2^{43}	Enable Second Vector Logical (ESVL)
6	2^{42}	Program State (PS)
6	2^{41}	Floating-point Error Status (FPS)
6	2^{40}	Bidirectional Memory (BM)
6	2^{39}	Interrupt on Operand Range Error (IOR)
6	2^{38}	Interrupt on Floating-point Error (IFP)
6	2^{37}	Interrupt on Uncorrectable Memory Error (IUM)
6	2^{36}	Interrupt on Correctable Memory Error (ICM)
6	2^{35}	Extended Addressing Mode (EAM)
6	2^{34}	Selected for External Interrupts (SEI)
6	2^{33}	Interrupt Monitor Mode (IMM)
6	2^{32}	Monitor Mode (MM)

ESVL - Enable Second Vector Logical

Word 6, bit (2^{43})
If ESVL = 1, then 140 - 145 instructions will attempt to use the Second Vector Logical functional unit first. If ESVL = 0, the Second Vector Logical is not used.

PS - Program State

Word 6, bit (2^{42})
The contents of this 1-bit register is manipulated by the operating system (software) to represent different program states among the CPUs which are currently processing a single program.

FPS - Floating-point Error Status

Word 6, bit (2^{41})
When this bit is set, a Floating-point Error has occurred regardless of the state of the Floating-point Error Mode flag.

BM - Bidirectional Memory

Word 6, bit (2^{40})
When this bit is set, block reads and writes may operate concurrently.

IOR - Interrupt on Operand Range Error

Word 6, bit (2^{39})
When this bit is set, interrupts on Operand Range Errors are Enabled.

IFP - Interrupt on Floating-point

Word 6, bit (2^{38})
When this bit is set, interrupts on Floating-point Errors are Enabled.

IUM - Interrupts on Uncorrectable Memory Error

Word 6, bit (2^{37})
When this bit is set, interrupts on uncorrectable Memory Data Errors are Enabled.

ICM - Interrupt on Correctable Memory Error

Word 6, bit (2^{36})
When this bit is set, interrupts on correctable Memory Data Errors are Enabled.

EAM - Extended Addressing Mode

Word 6, bit (2^{35})
The Extended Addressing Mode bit is set to allow full 32-bit addressing. This bit shows which mode the machine uses with the program. If the bit equals a one, then the program is in Y-mode; if it equals a zero, then it is in X-mode with 24-bit addressing.

SEI - Selected for External Interrupt

Word 6, bit (2^{34})
When this bit is set, this CPU is preferred for I/O interrupts.

IMM - Interrupt Monitor Mode

Word 6, bit (2^{33})
When the Interrupt Monitor Mode bit is set in the Modes register, certain interrupts will be recognized while in monitor mode. Other interrupts will not be enabled. The table below shows the interrupts and their recognition when the IMM bit is a one.

Interrupt Monitor Mode Interrupt Handling

Interrupt Abbreviation	Interrupt Name	Condition When IMM = 1
ICP	Interrupt from internal CPU	Disabled
DL	Deadlock Interrupt	Enabled
PCI	Programmable Clock Interrupt	Disabled
MCU	MCU Interrupt	Disabled
FPE	Floating-point Error Interrupt	Enabled
ORE	Operand Range Error Interrupt	Enabled
PRE	Program Range Error Interrupt	Enabled
ME	Memory Error Interrupt	Enabled
IOI	I/O Interrupt	Disabled
EEX	Error Exit Interrupt	Enabled
NEX	Normal Error Exit Interrupt	Enabled

MM - Monitor Mode

Word 6, bit (2^{32})
When this bit is set, all interrupts other than Memory errors are disabled.

CRAY Y-MP EXCHANGE CONTROL INSTRUCTIONS

000000 - Error Exit

004000 - Normal Exit

** 0013j0 - Enter XA Register With (Aj)

** 0014j1 - Set Interprocessor Interrupt Request of CPU (Aj) (Aj = 0 - 7)

** 0014j2 - Clear Interprocessor Interrupt (ICP)

** 0014j3 - Select CLN Register to (Aj) (Aj = 0 - 11)

** 001405 - Clear Programmable Clock Interrupt (PCI) Request

** 001406 - Enable PCI Request

** 001407 - Disable PCI Request

002100 - Enable Interrupt in Floating-point Error

002200 - Disable Interrupt on Floating-point Error

002300 - Enable Operand Range Error Interrupts

002400 - Disable Operand Range Error Interrupts

002500 - Disable Bi-directional Memory Transfers

002600 - Enable Bi-directional Memory Transfers

** Privileged to Monitor Mode

YM10/40

CRAY Y-MP EXCHANGE SEQUENCE (OPTIONS INVOLVED)

(AR0 - AR3) Options

The (AR) option contains the A registers which are controlled by the (JG) options for the write to memory and controlled by the (JE) option for the read of memory to the A registers.

(HA0 - HZ0) Options

The (HA/Z) options contain the P register which stops incrementing upon receiving the Wait Exchange from the (HC) option. The (HA/Z) will then pass the P register to the (HF) option where the P register is sent to memory or decremented by minus one or minus two prior to being sent to memory. The (HA) option will also generate the blank NIP upon receiving the Wait Exchange which will keep issue circuits quiet.

(HC0 - HD0) Options

The (HC/D) options contain the NIP/LIP registers which must be issued before an Exchange Sequence can take place. The (HC) option will set the Wait Exchange for the entire Exchange Sequence and drop the Wait Exchange upon receiving the Release Exchange from the (JD) option.

(HE0) Option

The (HE) option contains the VL, XA, CLN, Modes and Flag registers for the program in execution. The VL, XA, CLN and Flags are kept up-to-date as the program modifies those registers. When the (HE) receives the Exchange Sequence from the (JD), the (He) will send out the XA address to the (YE, YA) for the starting Memory address. The (HE) will then sequence out the VL, XA, CLN, Modes and Flag values out to the (HF) for a write to memory. On the read from memory, all the exchange parameters are routed first through the (HE) and some to the (HF). The (HE) can cause an exchange to take place by having an Interrupt flag set. The interrupt is sent to the (HC) and sets the Wait Exchange.

(HF0) Option

The (HF) option contains the exchange parameters that are written to memory and also read back from memory, which are the DBA, DLA, ILA, ILB and P register. The P register on a write to memory is received from the (HA/Z) options and are passed to the (YC/D) option all bits at a time, while on a read of memory the P register is received from the (HE) and then multiplex out to the (HA/Z) 6 bits at a time. The Flags, Modes, XA, VL and CLN are received from the (HE) option on a write to memory, but on a read of memory they are not received until another exchange takes place. The (HF) will also subtract minus one from P register if a Test and Set (T & S) instruction is in NIP or P - 2 if the T & S instruction is in CIP.

(HG0) Option

The (HG) option contains the exchange parameters for the PN, Syndrome, Bank, C.S., Read Mode register and parity error, VNU and WS, those values are written to memory only. The (HG0) exchange parameters are sequenced out by the Sequence Counters located on the (HG), what initiates the counters is the (HG) receiving the Exchange Sequence from the (JD) option. The (HG) exchange parameters contain the memory error information, except for VNU and WS, that the program experienced while in execution .

(JB0) Option

The (JB) option simply passes the control select j/i to the (VB/C) option during an Exchange Sequence.

(JC0) Option

The (JC) options purpose in the exchange process is to clear the waiting on the Semaphore flag (WS) and send a signal to the (HG) option if the vector is not used (VNU). The (JC) will pass a signal T & S and holding to the (JD) option which will be decoded on the (JD) for P - 1 or P - 2. This in turn will cause the WS flag to all be set on the (HG) option.

(JD0) Option

The (JD) option is responsible for generating the exchange request, which cannot occur until NIP/CIP have issued and A/S/V are quiet along with a Fetch operation being quiet. The (JD) is also responsible for receiving the Ports A and C reservation which are used by the Exchange Sequence. Port A is used by the read of memory, while Port C is used by the write of memory. The Exchange Sequence is treated as a Block reference. The (JD) will also generate P - 1 and P - 2, depending on whether the Test and Set instruction (0034) is in NIP or CIP.

(JE0) Option

The (JE) option is used on an Exchange Read Sequence to write the value of A0 - A7 into (AR0 - AR3) options.

(JG0) Option

The (JG0) option is used on an Exchange Write Sequence to read A0 - A7 and S0 - S7 registers which are passed to the (YC/D) options. Also, on an Exchange Read Sequence to generate the controls to load S0 - S7 from memory.

(VB - VC) Options

The (VB - VC) options contain the Scalar registers S0 - S7 which are controlled by the (JG) option. On an Exchange Write, S0 - S7 are sent to the (YC/D) options. On an Exchange Read, the (VB/C) receive their data from the (YQ) options from Port A.

(VS) Option

The (VS) option is used to fanout the controls to the 16 (VB) options and the 16 (VC) options which make up the S registers.

(YA0 - YA3) Options

The (YA) option is responsible for passing the XA address to the memory module. The (YA) will also select the proper section of memory from the section Enables sent from the (YK) option. Exchange address bits (2^8 -2^{11}) are passed to memory as an Internal Memory address, while address bits (2^5, 2^6, 2^7) are passed to the memory and CPU modules as the bank selects. The bank selects are checked against the other Bank references to determine any conflicts on the (YL) options.

(YE0) Option

The (YE) option generates the Port A/C reference, along with the Port A/C release when the Exchange R/W is completed. The (YE) receives XA bit (2^4) and also contains a Port A/C Exchange Adder for the lower XA bits (2^0 - 2^3). Exchange address bits (2^1 - 2^4) are then passed to the (YK) option where a Bank conflict could stop the reference.

(YI0) Option

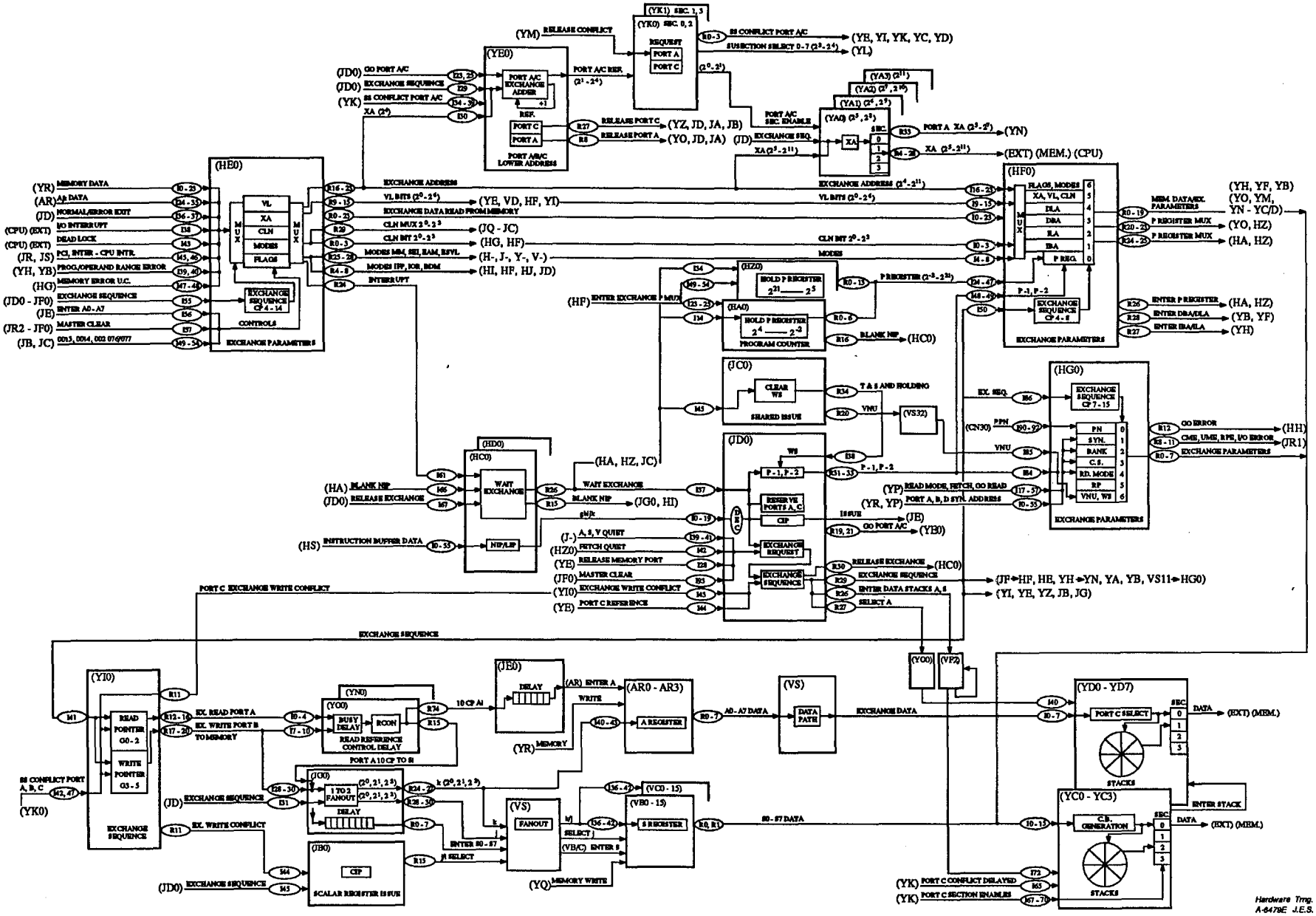
The (YI0) option, upon receiving the Exchange Sequence from the (JD) option, will start the Read pointers and the Write pointers which are used to select the proper A0 - A7 or S0 - S7 register. The Write pointer which is used on an Exchange Write to memory uses Port B path to the A/S registers on the (YI) option. While the Read pointer uses Port A read path to load the A0 - A7 registers and S0 - S7 registers taking into account any Bank conflicts amongst the other CPUs.

(YK0, YK1) Options

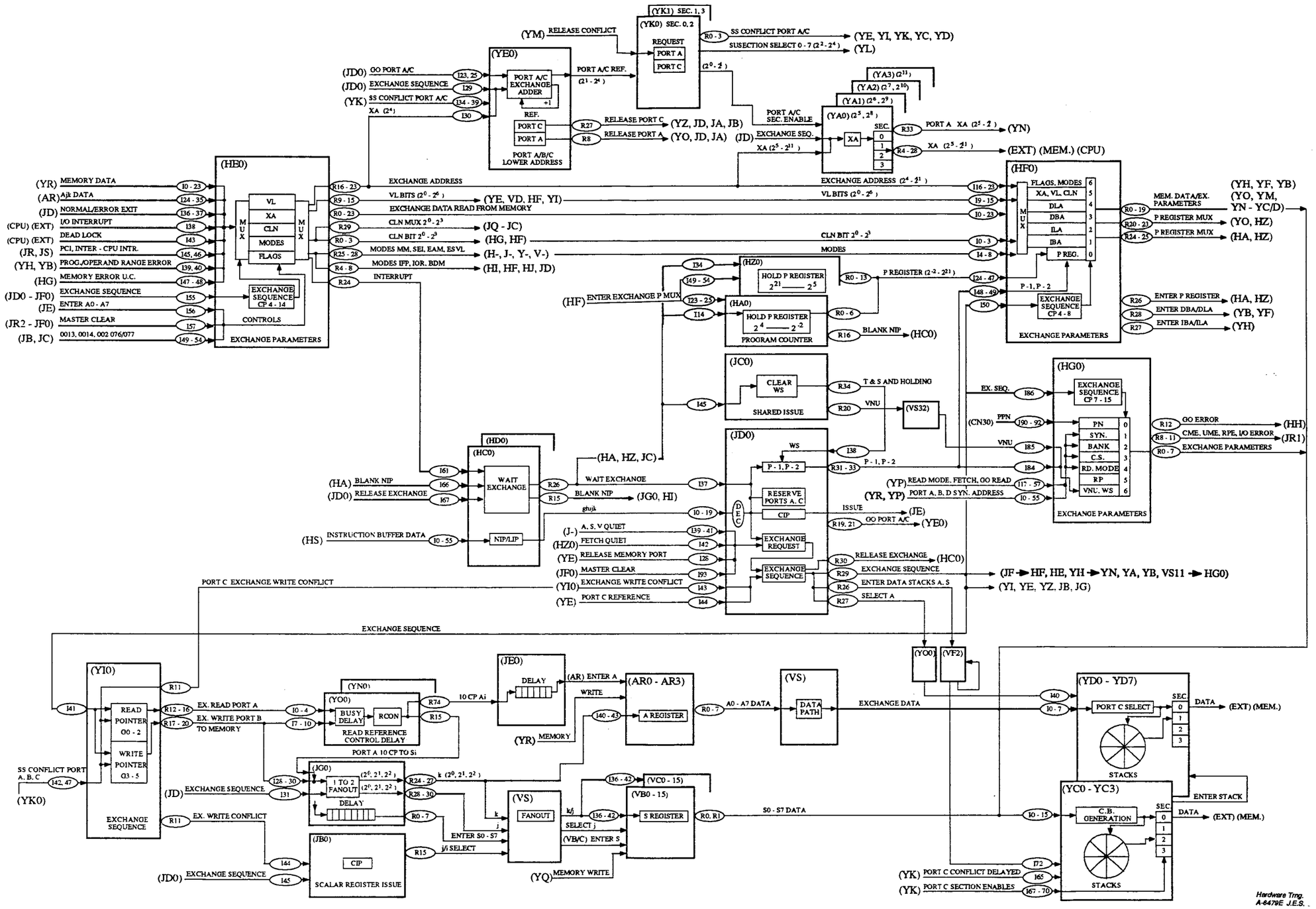
The (YK) option is used by the Exchange Sequence to select the proper section for the XA address to memory and also the proper Subsection (SS) SS0 - SS7. The (YK) will also stop the Exchange R/W Sequence upon receiving a Release conflict from the (YM) option. The (YK) will send out a SS conflict Port A/C to the (YE, YI, YK) option to stop the sequence counters and to the (YC/D) options to stack the data which was read from the A or S registers. The (YK0) option is used to control Sections 0 and 2 while (YK1) option controls Sections 1 and 3.

(YO0, YN0) Options

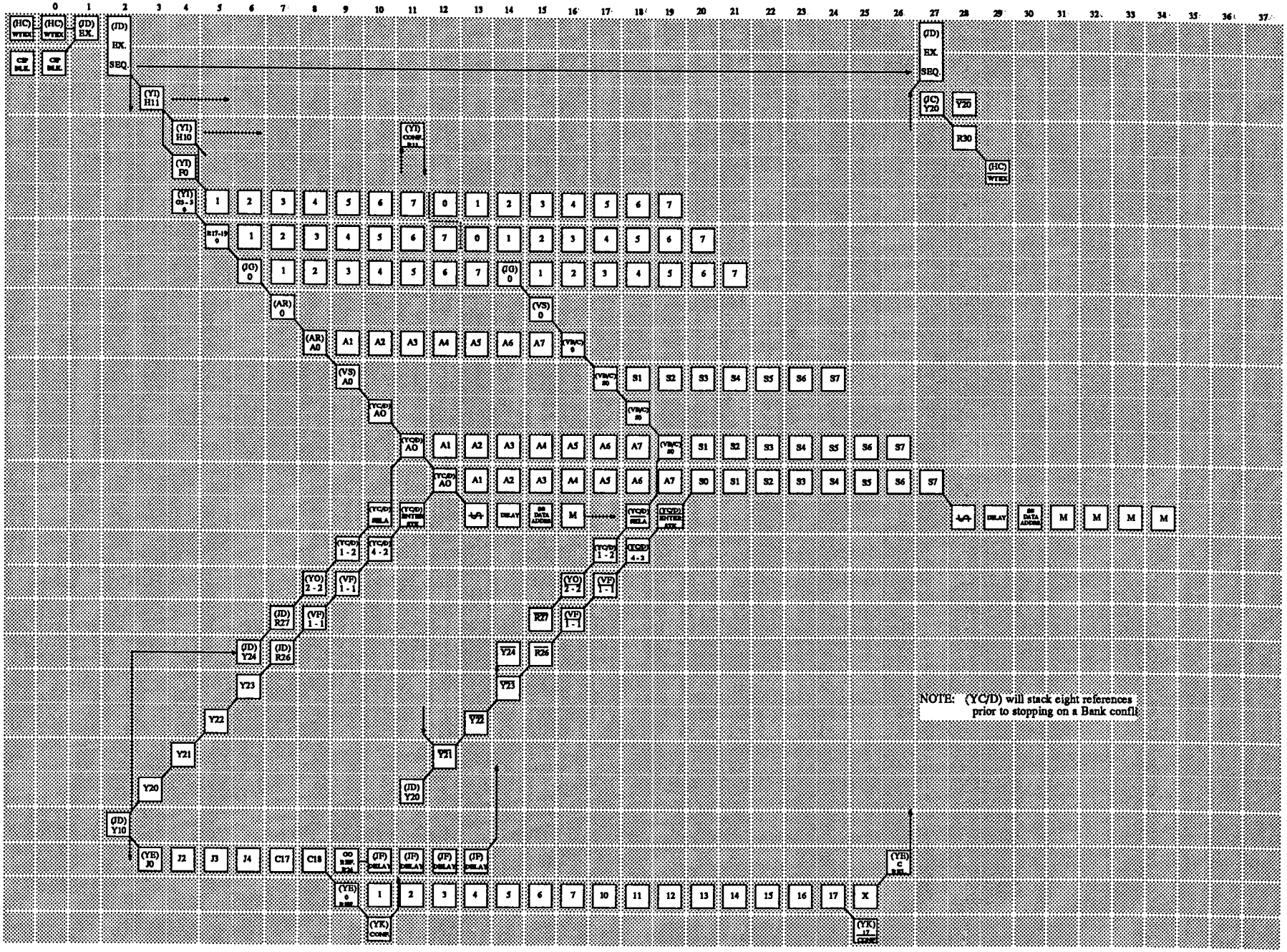
The (YO, YN) options are used to time the read references from memory taking into account any Bank conflicts that the Exchange Read experienced.



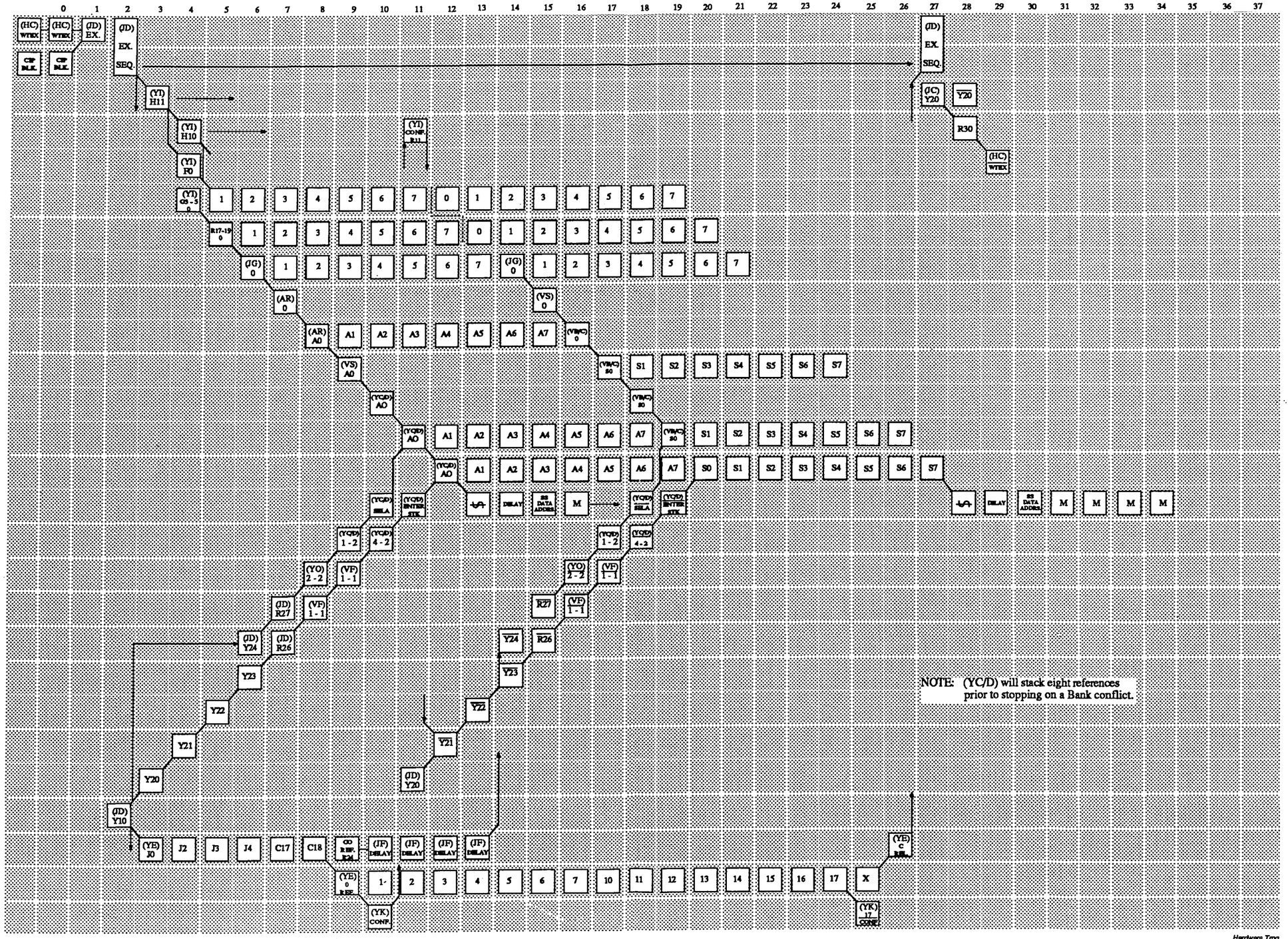
CRAY Y-MP EXCHANGE SEQUENCE BLOCK DIAGRAM



CRAY Y-MP EXCHANGE SEQUENCE BLOCK DIAGRAM

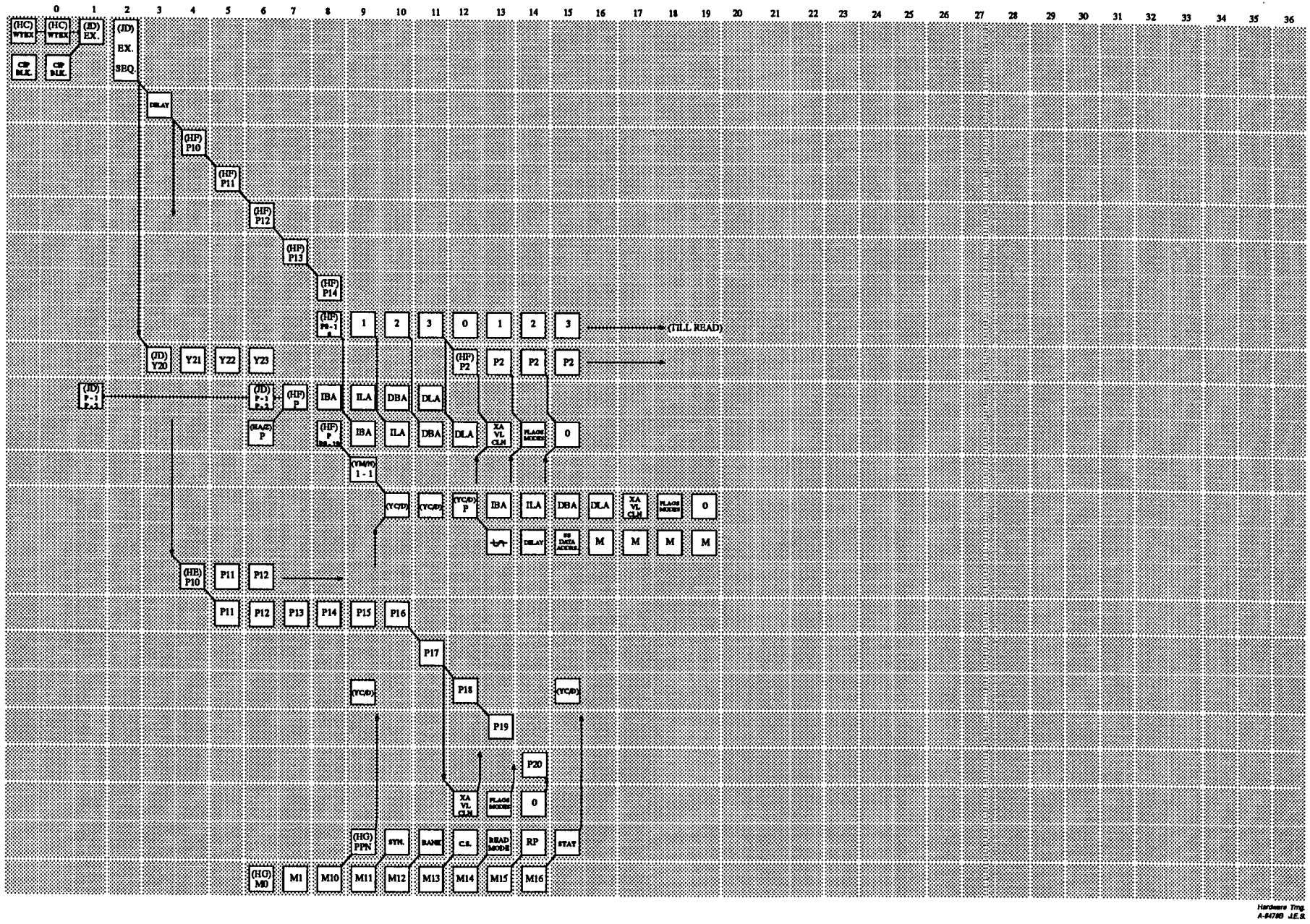


CRAY Y-MP EXCHANGE WRITE SEQUENCE A, S DATA



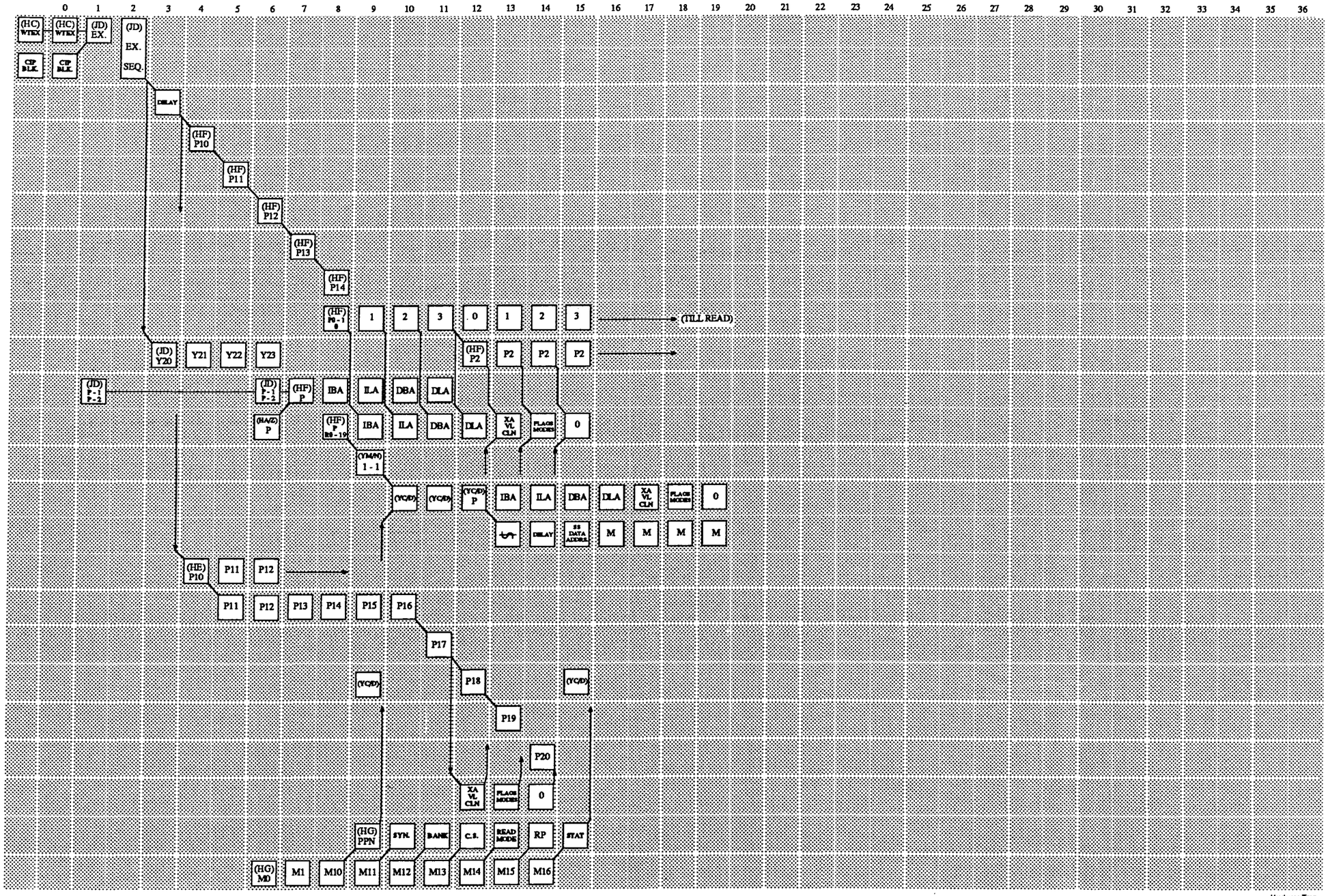
Hardware Trng.
A-6476B J.E.S.

CRAY Y-MP EXCHANGE WRITE SEQUENCE A, S DATA



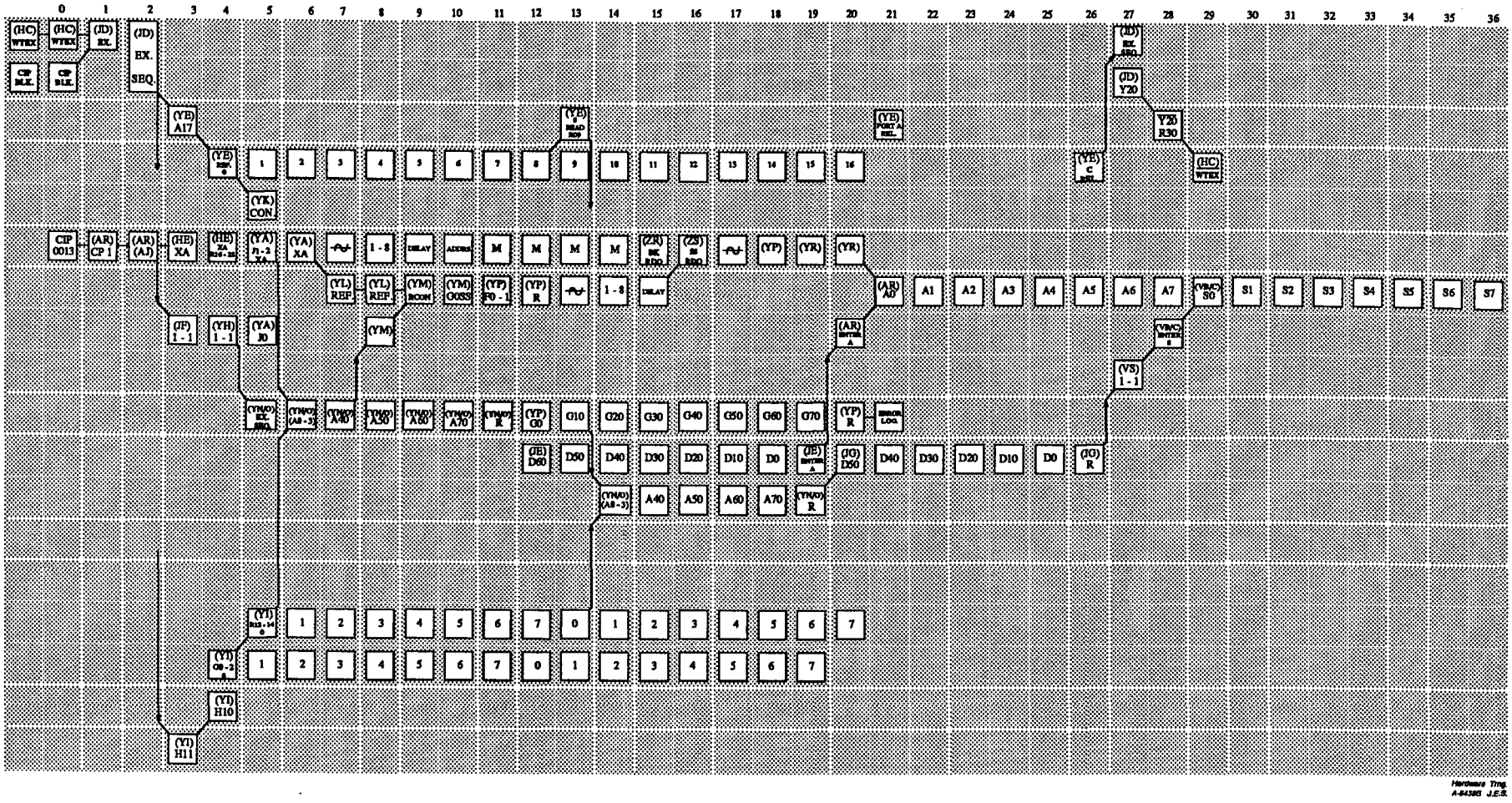
Hardware Trng.
A-84788 J.E.S.

CRAY Y-MP EXCHANGE WRITE SEQUENCE PARAMETERS

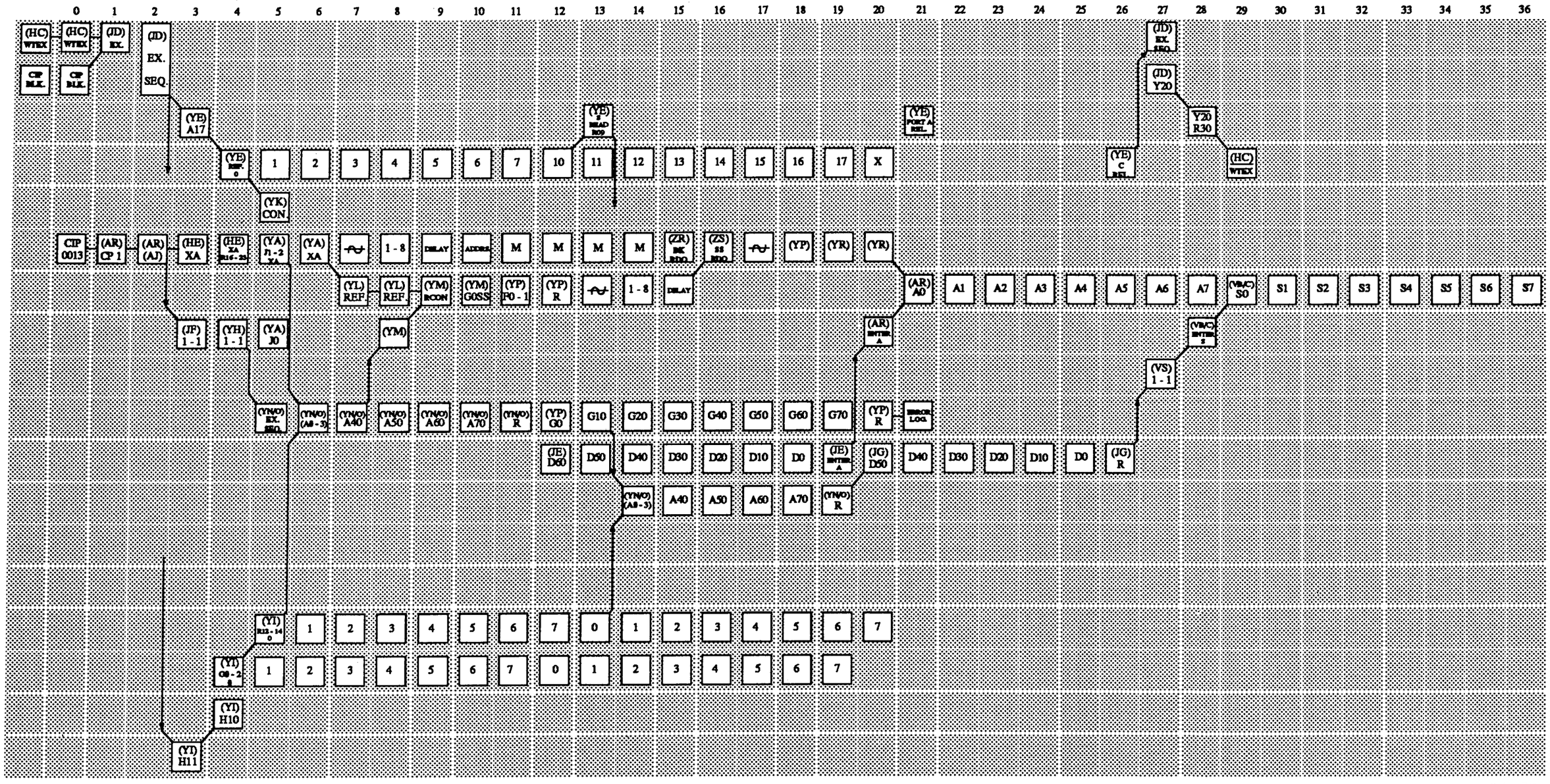


Hardware Trng.
A-6478B J.E.S.

CRAY Y-MP EXCHANGE WRITE SEQUENCE PARAMETERS

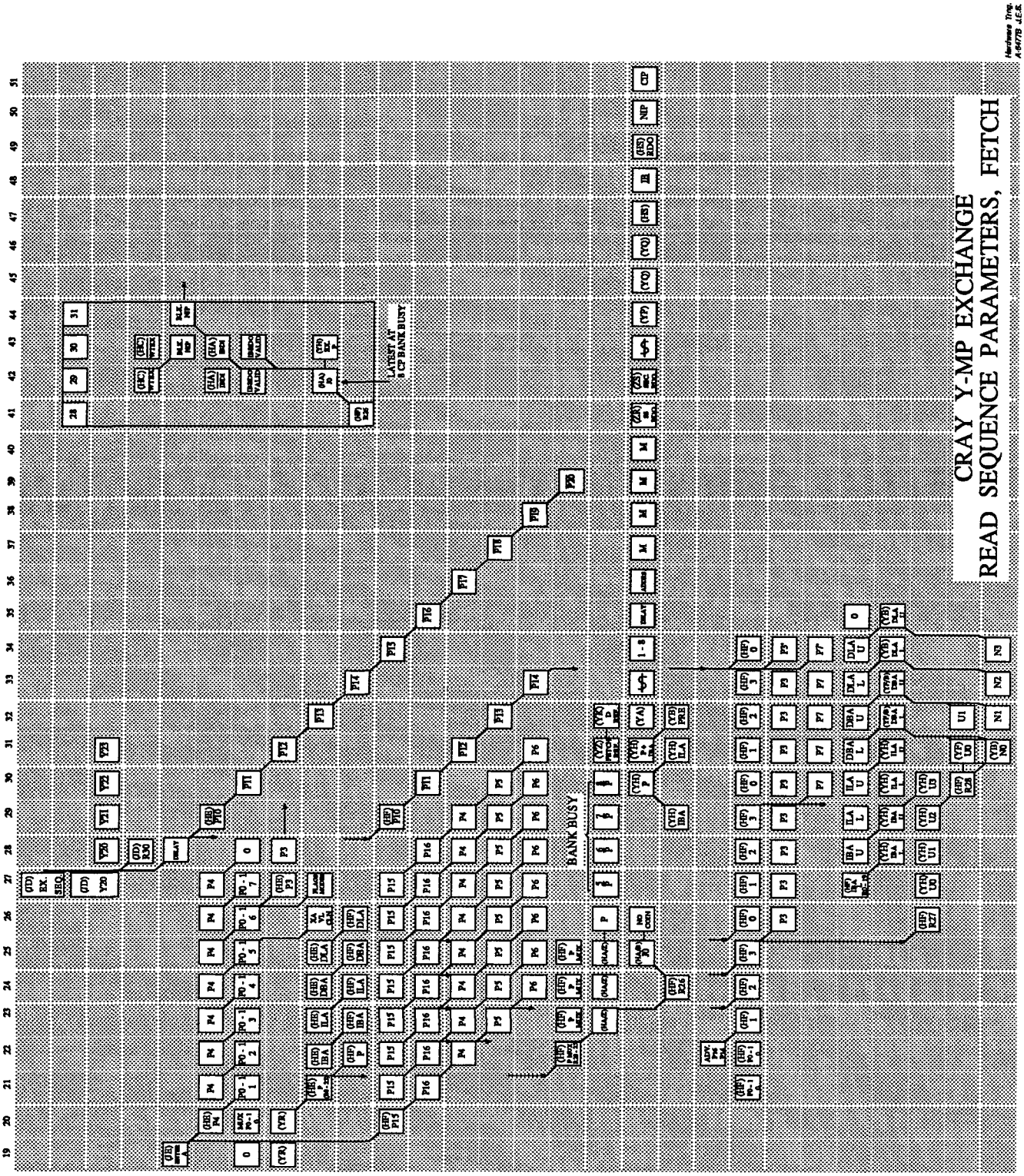


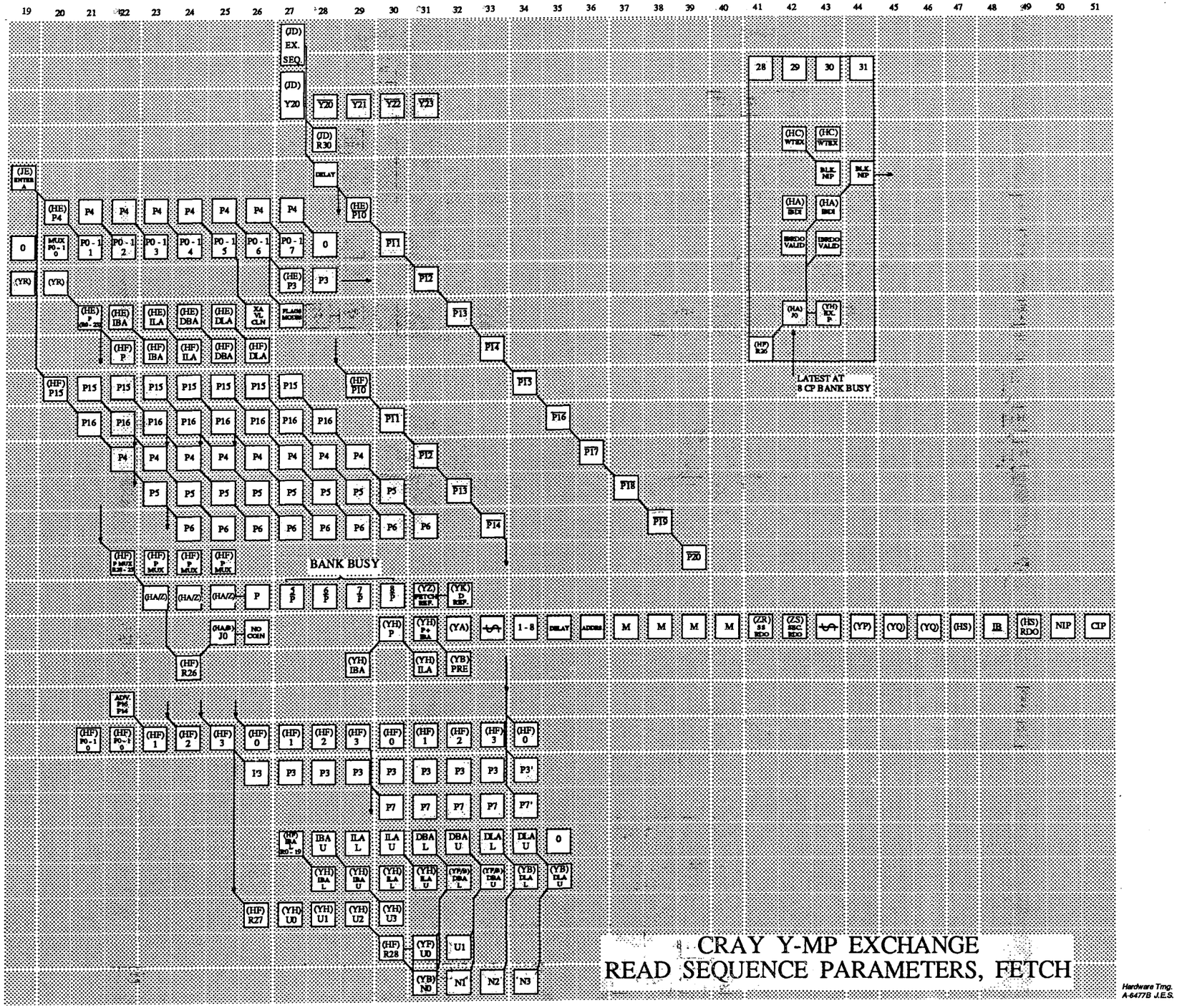
CRAY Y-MP EXCHANGE READ SEQUENCE A, S DATA

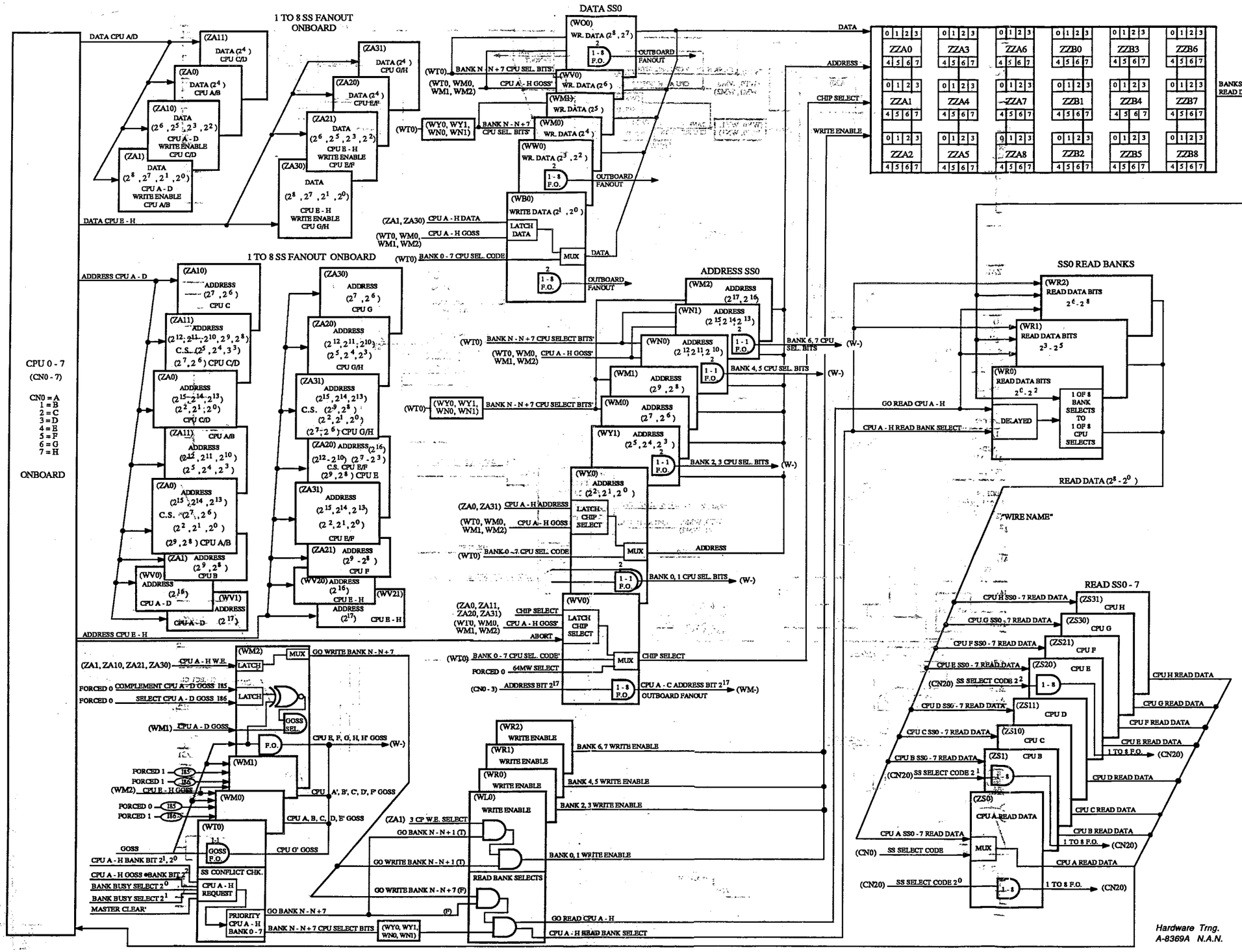


Hardware Trng.
A-6438B J.E.S.

CRAY Y-MP EXCHANGE READ SEQUENCE A, S DATA


CRAY Y-MP EXCHANGE
READ SEQUENCE PARAMETERS, FETCH
BANK BUSY





HTV-0834

CRAY Y-MP MEMORY (128MW) BLOCK DIAGRAM (256K x 1) SUBSECTION 0 CPU A - H

CRAY PROPRIETARY

Date: 11 September 1989

From: HTS, Chippewa Falls

Subject: Troubleshooting Y-MP Double / Multiple Bit Errors in a Y-MP.

Possible causes:

1) Any module and most wires in the Y-MP.

Failure Mode:

1) Solid or offline diagnostic recreatable failures.
2) Intermittent failures under customer loading, not recreatable under diagnostics.

Troubleshooting:

1) The solid or offline diagnostic recreatable failures, are usually straight forward; but are not the norm in the present Y-MP field environment.
2) The intermittent problems (Failure Modes) are the ones addressed in this paper.
3) Try to avoid "shot-gunning" a module for each double / multiple bit occurrance. If necessary, accumulate information from more than one error before making a BEST GUESS module replacement. (This will help minimize the number of power cycles taken to locate the failing module, give the Repair Center additional information to help them make a good repair, and yield a higher percentage of first time fixes).
4) Of primary importance is to document all errors, and look for patterns:

Patterns:

1) All double / multiple bit errors need to be documented and researched. This includes DBEs / MBEs that do or do not crash the system. Ensure a record is kept of all information recorded on the Error Logger, particularily CPU involved, BANK, SYNDRONE, READ MODE, and I/O bit.
2) On job aborts, try to identify the user and job involved. One useful troubleshooting technique is to have the failed job rerun several times to look for problem repeats. An additional troubleshooting aid is to have this job targeted to a specific CPU each time it is run.
3) On system crashes, scan the memory before OS or Diagnostics are started, and identify all occurrences of single and double bit errors.
   a) An official yscan routine has been requested from the offline diagnostics department. In the interim, sites should write their own scan routine. This may be a routine which records the address of any DBE / MBE found and allows the engineer to look at that memory location possibly via a HISP channel, or a routine which will record the address and data pattern received for all SBEs, DBEs and MBEs seen while scanning memory.

b) Review the information recorded to see if there are any patterns such as:
   1) address similarities except for 1 or 2 address bits. (Indicating an address fan-out failure).
   2) data pattern irregularities such as a 9-bit grouping in a field of zeros or a group of 9-zero bits in a field of random data. (Indicating an address or control fan-out failure).
   3) A single word reported in error. (Indicating a possible go-write failure).
   4) No errors recorded in memory. (Indicating a possible go-read or address failure).
   5) Data patterns that appear as a 16-bit or 32-bit possible problem. (Indicating a possible CPU related problem).
   6) Data inconsistancies when comparred with the memory words immediately prior to and following the failing location.

4) After a system abort, or during a PM period following a DBE / MBE that did not crash the system, run ypave and MX8 under margins to see if the error is recreatable. Then check the site logs to see if any module movement activity was done in that area of the system recently (possibly a recently installed module failed, or a voltage buss was not torqued properly on the rear of this or an adjacent module).
5) Module Ground Drops should not exceed 30mv. A module in excess of 30mv, or one that has recently increased noticeably can be the cause of SBEs, DBEs and MBEs.
6) Random MBEs, DBEs and SBEs in one section, may indicate a power supply or failing diode problem.
7) After a couple of DBEs / MBEs, a pattern should develop which may point to a probable CPU path or fan-out. The lack of a pattern may even help to isolate the problem.
8) SBEs on the logger with identical or similar BANK addresses may help isolate to the failing memory module.
9) Increased I/O traffic may bring the problem out. (ie: swapping data in and out of the SSD to create more frequent memory conflicts).
10) Attached is a chart developed by Scott Emery indicating the probability of a particular module as causing the DBE / MBE. Remember; the DBE / MBE is seen as the result of data bits being in error. The true cause may actually be on another module which fans out a control or address signal to this module.
11) Don't forget the CLOCK module. To-date there has been one field CLOCK module failure. This failure appeared as both subsections on the same PCB of a module recording the majority of the double bits, while the remaining were traceable to fanouts located on that same PCB. Running under clock margins may help to identify this cause, but a short or poor electrical contact is more prone to voltage isolation.

Examples:

1) In the best case; several jobs fail due to DBEs / MBEs at the same BANK address and were logged by multiple CPUs, followed by a system crash. A memory scan identifies two words in error at the same BANK address, with the same 9-bits hosed in each word, and the real memory addresses has only one address bit toggled to create the other address. This problem should be immediately identifiable as the module which stores the data bits as being in error. (The attached chart should isolate).

2) In another case; intermittent jobs fail due to DBEs / MBEs at various bank and subsection addresses, always in the same memory section and reported usually by the same CPU. This problem should be identifiable as a probable fanout of an address or control line from the CPU normally reporting the problem. One way to help isolate is to idle that CPU. The attached chart may help isolate the failing bits, though the actual failure may end up being a module containing the outboard fanouts for the effected CPU.

Basically:

AN INTERMITTANT MEMORY FAILURE MAY CAUSE TWO OR MORE INCIDENTS BEFORE THE FIRST INTELLIGENT MEMORY REPLACEMENT CAN BE MADE.

AN INTERMITTENT MEMORY FAILURE MAY ACTUALLY CAUSE MULTIPLE INCIDENTS BEFORE THE REAL PROBLEM IS IDENTIFIED AND FIXED.

****

Scott Emery Single, Double and Multiple Bit isolation chart (Attached)

x = a primary suspect module based on DATA BITS in error.
null indicates this syndrone should not be creatable by a failure of DATA BITS on this module.

Y-MP8: Each memory module contains 09-bits of data / C.B.s. These bits are mapped into the standard 8-banks of a subsection.

Bits:	00-08	09-17	18-26	27-35	36-44	45-53	54-62	63-CBs
Y-MP8 Memory Module Location:								
SEC-0:	01	02	03	04	05	06	07	08
SEC-1:	09	10	11	12	13	14	15	16
SEC-2:	25	26	27	28	29	30	31	32
SEC-3:	33	34	35	36	37	38	39	40

Y-MP4: Each memory module contains 18-bits of data / C.B.s. These bits are mapped into the standard 8-banks of a subsection by forcing each group of 9-bits into a different physical module bank. Data bits 0-8, 18-26, 36-44, and 54-62 will always be stored in physical banks 0, 1, 2 and 3. Data bits 9-17, 27-35, 45-53, and 63 plus CBs will always be stored in physical banks 4, 5, 6 and 7. Physical banks 0 and 4 are selected if logical bank 0 is addressed by the CPU. Physical banks 1 and 5 are selected if logical bank 1 is addressed by the CPU. Physical banks 2 and 6 are selected if logical bank 2 is addressed by the CPU. Physical banks 3 and 7 are selected if logical bank 3 is addressed by the CPU. A physical bank mapping of data bits to logical bank accessed is provided below.

Bits:	00-08	09-17	18-26	27-35	36-44	45-53	54-62	63-CBs
Bank: (Physical Bank on Module mapped to Logical Bank Address)								
Physical:	0-3	4-7	0-3	4-7	0-3	4-7	0-3	4-7
Logical:	0-3	0-3	0-3	0-3	0-3	0-3	0-3	0-3

The Y-MP4 is able to map multiple groups of 9-bit data simultaneously onto a memory module by using more than 1 path. The paths used by CPU-0 to access a single memory module are listed below.

Y-MP4 Memory Module Data Paths used by CPU-0:

Bits:	00-08	09-17	18-26	27-35	36-44	45-53	54-62	63-CBs
SEC-0 Path:	cpu-a	cpu-b	cpu-a	cpu-b	cpu-a	cpu-b	cpu-a	cpu-b
SEC-1 Path:	cpu-g	cpu-h	cpu-g	cpu-h	cpu-g	cpu-h	cpu-g	cpu-h
SEC-2 Path:	cpu-e	cpu-f	cpu-e	cpu-f	cpu-e	cpu-f	cpu-e	cpu-f
SEC-3 Path:	cpu-c	cpu-d	cpu-c	cpu-d	cpu-c	cpu-d	cpu-c	cpu-d

Y-MP2: Each memory module contains 36-bits of data / C.B.s. These bits are mapped into the standard 8-banks of a subsection by forcing each group of 9-bits into a different physical module bank. Data bits 0-8 and 36-44 will always be stored in physical banks 0 and 1. Data bits 9-17 and 45-53 will always be stored in physical banks 2 and 3. Data bits 18-26 and 54-62 will always be stored in physical banks 4 and 5. Data bits 27-35 and 63 plus CBs will always be stored in banks 6 and 7. The set of even physical banks is selected if logical bank 0 is addressed by the CPU. The set of odd physical banks is selected if logical bank 1 is addressed by the CPU. A physical bank mapping of data bits to logical bank accessed is provided below.

Bits:	00-08	09-17	18-26	27-35	36-44	45-53	54-62	63-CBs
Bank : (Physical Bank on Module mapped to Logical Bank Address)								
Physical:	0/1	2/3	4/5	6/7	0/1	2/3	4/5	6/7
Logical:	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

The Y-MP2 is able to map multiple groups of 9-bit data simultaneously onto a memory module by using more than 1 path. The paths used by CPU-0 to access a single memory module are listed below.

Y-MP2 Memory Module Data Paths used by CPU-0:

Bits:	00-08	09-17	18-26	27-35	36-44	45-53	54-62	63-CBs
SEC-0 Path:	cpu-a	cpu-b	cpu-c	cpu-d	cpu-a	cpu-b	cpu-c	cpu-d
SEC-1 Path:	cpu-h	cpu-g	cpu-f	cpu-e	cpu-h	cpu-g	cpu-f	cpu-e
SEC-2 Path:	cpu-a	cpu-b	cpu-c	cpu-d	cpu-a	cpu-b	cpu-c	cpu-d
SEC-3 Path:	cpu-h	cpu-g	cpu-f	cpu-e	cpu-h	cpu-g	cpu-f	cpu-e

Y-MP2 Memory Module Location:

SEC-0:	05	05	05	05	06	06	06	06
SEC-1:	07	07	07	07	08	08	08	08
SEC-2:	09	09	09	09	10	10	10	10
SEC-3:	11	11	11	11	12	12	12	12

Y-MP4 Memory Module Location:

SEC-0:	09	09	10	10	11	11	12	12
SEC-1:	13	13	14	14	15	15	16	16
SEC-2:	25	25	26	26	27	27	28	28
SEC-3:	29	29	30	30	31	31	32	32

Y-MP8 Memory Module Location:

SEC-0:	01	02	03	04	05	06	07	08
SEC-1:	09	10	11	12	13	14	15	16
SEC-2:	25	26	27	28	29	30	31	32
SEC-3:	33	34	35	36	37	38	39	40

Bits: Synd;	00-08	09-17	18-26	27-35	36-44	45-53	54-62	63-CBs
001				x				x
002				x				x
003	x	x	x	x			x	x
---	-	-	-	-	-	-	-	-
004				x				x
005	x	x	x	x				x
006	x	x	x	x		x		x
007				x	x			x
---	-	-	-	-	-	-	-	-
010				x				x
011	x	x	x	x				x
012	x	x	x	x				x
013				x	x	x		x
---	-	-	-	-	-	-	-	-
014	x	x	x	x	x			x
015				x		x	x	x
016				x			x	x
017	x	x	x	x				x

:	00-08	09-17	18-26	27-35	36-44	45-53	54-62	63-CBs
020								x
021								x
022								x
023								x
---	-	-	-	-	-	-	-	-
024								x
025								x
026								x
027								x
---	-	-	-	-	-	-	-	-
030								x
031								x
032								x
033								x
---	-	-	-	-	-	-	-	-
034								x
035								x
036								x
037								x

Y-MP2 Memory Module Location:

SEC-0:	05	05	05	05	06	06	06	06
SEC-1:	07	07	07	07	08	08	08	08
SEC-2:	09	09	09	09	10	10	10	10
SEC-3:	11	11	11	11	12	12	12	12

Y-MP4 Memory Module Location:

SEC-0:	09	09	10	10	11	11	12	12
SEC-1:	13	13	14	14	15	15	16	16
SEC-2:	25	25	26	26	27	27	28	28
SEC-3:	29	29	30	30	31	31	32	32

Y-MP8 Memory Module Location:

SEC-0:	01	02	03	04	05	06	07	08
SEC-1:	09	10	11	12	13	14	15	16
SEC-2:	25	26	27	28	29	30	31	32
SEC-3:	33	34	35	36	37	38	39	40

:	00-08	09-17	18-26	27-35	36-44	45-53	54-62	63-CBs
040								x
041								x
042								x
043								x
---	-	-	-	-	-	-	-	-
044								x
045								x
046								x
047								x
---	-	-	-	-	-	-	-	-
050								x
051								x
052								x
053								x
---	-	-	-	-	-	-	-	-
054								x
055								x
056								x
057								x

:	00-08	09-17	18-26	27-35	36-44	45-53	54-62	63-CBs
060			x	x	x		x	x
061				x		x		x
062				x				x
063			x	x			x	x
---	-	-	-	-	-	-	-	-
064				x				x
065			x	x				x
066			x	x		x		x
067				x	x			x
---	-	-	-	-	-	-	-	-
070				x				x
071			x	x				x
072			x	x				x
073				x	x	x		x
---	-	-	-	-	-	-	-	-
074			x	x	x			x
075				x		x	x	x
076				x			x	x
077			x	x				x

Y-MP2 Memory Module Location:

SEC-0:	05	05	05	05	06	06	06	06
SEC-1:	07	07	07	07	08	08	08	08
SEC-2:	09	09	09	09	10	10	10	10
SEC-3:	11	11	11	11	12	12	12	12

Y-MP4 Memory Module Location:

SEC-0:	09	09	10	10	11	11	12	12
SEC-1:	13	13	14	14	15	15	16	16
SEC-2:	25	25	26	26	27	27	28	28
SEC-3:	29	29	30	30	31	31	32	32

Y-MP8 Memory Module Location:

SEC-0:	01	02	03	04	05	06	07	08
SEC-1:	09	10	11	12	13	14	15	16
SEC-2:	25	26	27	28	29	30	31	32
SEC-3:	33	34	35	36	37	38	39	40

:	00-08	09-17	18-26	27-35	36-44	45-53	54-62	63-CBs
100				x				x
101				x				x
102				x				x
103				x				x
---	-	-	-	-	-	-	-	-
104				x				x
105				x				x
106				x				x
107				x				x
---	-	-	-	-	-	-	-	-
110				x				x
111				x				x
112				x				x
113				x				x
---	-	-	-	-	-	-	-	-
114				x				x
115				x				x
116				x				x
117				x				x

:	00-08	09-17	18-26	27-35	36-44	45-53	54-62	63-CBs
120					x	x	x	x
121								x
122								x
123							x	x
---	-	-	-	-	-	-	-	-
124								x
125								x
126						x		x
127					x			x
---	-	-	-	-	-	-	-	-
130								x
131								x
132								x
133					x	x		x
---	-	-	-	-	-	-	-	-
134					x			x
135						x	x	x
136							x	x
137								x

Y-MP2 Memory Module Location:

SEC-0:	05	05	05	05	06	06	06	06
SEC-1:	07	07	07	07	08	08	08	08
SEC-2:	09	09	09	09	10	10	10	10
SEC-3:	11	11	11	11	12	12	12	12

Y-MP4 Memory Module Location:

SEC-0:	09	09	10	10	11	11	12	12
SEC-1:	13	13	14	14	15	15	16	16
SEC-2:	25	25	26	26	27	27	28	28
SEC-3:	29	29	30	30	31	31	32	32

Y-MP8 Memory Module Location:

SEC-0:	01	02	03	04	05	06	07	08
SEC-1:	09	10	11	12	13	14	15	16
SEC-2:	25	26	27	28	29	30	31	32
SEC-3:	33	34	35	36	37	38	39	40

:	00-08	09-17	18-26	27-35	36-44	45-53	54-62	63-CBs
200								x
201								x
202								x
203								x
---	-	-	-	-	-	-	-	-
204								x
205								x
206								x
207								x
---	-	-	-	-	-	-	-	-
210								x
211								x
212								x
213								x
---	-	-	-	-	-	-	-	-
214								x
215								x
216								x
217								x

:	00-08	09-17	18-26	27-35	36-44	45-53	54-62	63-CBs
220				x	x	x	x	x
221				x				x
222				x				x
223				x			x	x
---	-	-	-	-	-	-	-	-
224				x				x
225				x				x
226				x		x		x
227				x	x			x
---	-	-	-	-	-	-	-	-
230				x				x
231				x				x
232				x				x
233				x	x	x		x
---	-	-	-	-	-	-	-	-
234				x	x			x
235				x		x	x	x
236				x			x	x
237				x				x

Y-MP2 Memory Module Location:

SEC-0:	05	05	05	05	06	06	06	06
SEC-1:	07	07	07	07	08	08	08	08
SEC-2:	09	09	09	09	10	10	10	10
SEC-3:	11	11	11	11	12	12	12	12

Y-MP4 Memory Module Location:

SEC-0:	09	09	10	10	11	11	12	12
SEC-1:	13	13	14	14	15	15	16	16
SEC-2:	25	25	26	26	27	27	28	28
SEC-3:	29	29	30	30	31	31	32	32

Y-MP8 Memory Module Location:

SEC-0:	01	02	03	04	05	06	07	08
SEC-1:	09	10	11	12	13	14	15	16
SEC-2:	25	26	27	28	29	30	31	32
SEC-3:	33	34	35	36	37	38	39	40

:	00-08	09-17	18-26	27-35	36-44	45-53	54-62	63-CBs
240				x	x	x	x	x
241				x				x
242				x				x
243				x			x	x
---	-	-	-	-	-	-	-	-
244				x				x
245				x				x
246				x		x		x
247				x	x			x
---	-	-	-	-	-	-	-	-
250				x				x
251				x				x
252				x				x
253				x	x	x		x
---	-	-	-	-	-	-	-	-
254				x	x			x
255				x		x	x	x
256				x			x	x
257				x				x

:	00-08	09-17	18-26	27-35	36-44	45-53	54-62	63-CBs
260	x	x						x
261								x
262								x
263	x	x						x
---	-	-	-	-	-	-	-	-
264								x
265	x	x						x
266	x	x						x
267								x
---	-	-	-	-	-	-	-	-
270								x
271	x	x						x
272	x	x						x
273								x
---	-	-	-	-	-	-	-	-
274	x	x						x
275								x
276								x
277	x	x						x

Y-MP2 Memory Module Location:

SEC-0:	05	05	05	05	06	06	06	06
SEC-1:	07	07	07	07	08	08	08	08
SEC-2:	09	09	09	09	10	10	10	10
SEC-3:	11	11	11	11	12	12	12	12

Y-MP4 Memory Module Location:

SEC-0:	09	09	10	10	11	11	12	12
SEC-1:	13	13	14	14	15	15	16	16
SEC-2:	25	25	26	26	27	27	28	28
SEC-3:	29	29	30	30	31	31	32	32

Y-MP8 Memory Module Location:

SEC-0:	01	02	03	04	05	06	07	08
SEC-1:	09	10	11	12	13	14	15	16
SEC-2:	25	26	27	28	29	30	31	32
SEC-3:	33	34	35	36	37	38	39	40

:	00-08	09-17	18-26	27-35	36-44	45-53	54-62	63-CBs
300	x				x	x	x	x
301								x
302								x
303	x						x	x
---	-	-	-	-	-	-	-	-
304								x
305	x							x
306	x					x		x
307					x			x
---	-	-	-	-	-	-	-	-
310								x
311	x							x
312	x							x
313					x	x		x
---	-	-	-	-	-	-	-	-
314	x				x			x
315						x	x	x
316							x	x
317	x							x

:	00-08	09-17	18-26	27-35	36-44	45-53	54-62	63-CBs
320		x	x	x				x
321				x				x
322				x				x
323		x	x	x				x
---	-	-	-	-	-	-	-	-
324				x				x
325		x	x	x				x
326		x	x	x				x
327				x				x
---	-	-	-	-	-	-	-	-
330				x				x
331		x	x	x				x
332		x	x	x				x
333				x				x
---	-	-	-	-	-	-	-	-
334		x	x	x				x
335				x				x
336				x				x
337		x	x	x				x

Y-MP2 Memory Module Location:

SEC-0:	05	05	05	05	06	06	06	06
SEC-1:	07	07	07	07	08	08	08	08
SEC-2:	09	09	09	09	10	10	10	10
SEC-3:	11	11	11	11	12	12	12	12

Y-MP4 Memory Module Location:

SEC-0:	09	09	10	10	11	11	12	12
SEC-1:	13	13	14	14	15	15	16	16
SEC-2:	25	25	26	26	27	27	28	28
SEC-3:	29	29	30	30	31	31	32	32

Y-MP8 Memory Module Location:

SEC-0:	01	02	03	04	05	06	07	08
SEC-1:	09	10	11	12	13	14	15	16
SEC-2:	25	26	27	28	29	30	31	32
SEC-3:	33	34	35	36	37	38	39	40

:	00-08	09-17	18-26	27-35	36-44	45-53	54-62	63-CBs
340			x	x				x
341				x				x
342				x				x
343			x	x				x
---	-	-	-	-	-	-	-	-
344				x				x
345			x	x				x
346			x	x				x
347				x				x
---	-	-	-	-	-	-	-	-
350				x				x
351			x	x				x
352			x	x				x
353				x				x
---	-	-	-	-	-	-	-	-
354			x	x				x
355				x				x
356				x				x
357			x	x				x

:	00-08	09-17	18-26	27-35	36-44	45-53	54-62	63-CBs
360					x	x	x	x
361								x
362								x
363							x	x
---	-	-	-	-	-	-	-	-
364								x
365								x
366						x		x
367					x			x
---	-	-	-	-	-	-	-	-
370								x
371								x
372								x
373					x	x		x
---	-	-	-	-	-	-	-	-
374					x			x
375						x	x	x
376								x
377								x
:	00-08	09-17	18-26	27-35	36-44	45-53	54-62	63-CBs

EXERCISE

EXERCISE NAME: CRAY Y-MP Memory Control No. 2 REVISION: 3/14/89

STUDENT NAME: _____ DATE: _____

INSTRUCTOR: _____

EXERCISE TYPE: Take home, In class _____ TIME ALLOTTED: _____

The following exercise is to determine if you can correctly go through the conflicts that a particular memory reference will experience and make the correct decisions based on the given information.

PTS.

7372 111 00 111 010 7 6 2

1. Given the following absolute address 7372_8 from Ports A, B (with odd increments), and D for fetch within the same clock period for CPUs 0 and 3, answer the following questions.

3 a. For CPU 0, which port would go first?

D

2 b. Which CPU and port would go next on the (YL) for bank conflicts?

CPU Ø FIRST PORT ISSUING

2 c. What option types solved the port conflict?

YK YM

3 d. What option type fanned out the GOSS 0 - 7 Section N to the CPU modules and to the memory modules?

YL

2 e. What option type solves the simultaneous bank conflict? In which CPU?

YL

3 f. To determine the bank conflicts, what option type fanned out address bit 2^5 to CPU 3 and to all other CPUs?

YA

Hardware Trng.
Y12EX20B J.E.S.

EXERCISE (Continued)

EXERCISE NAME: CRAY Y-MP Memory Control No. 2 REVISION: 3/14/89

STUDENT NAME: _____

PTS.

5 g. What CPU letters are CPU 0 and 3 being represented when solving the simultaneous bank conflicts?

F + 6

5 h. Which CPU, 0 or 3, has the higher priority?

Ø

5 i. What signal is generated from the (YL) option to the (YM) option when the bank is released?

5 j. Which (YM) option releases the SS conflict?

5 k. Why would Port D be released first on the (YM) option?

5 l. What option types perform the SECDED for this word being read from memory?

2. Given the following absolute address 13331 with the increment even from Port A, B, C within the same clock period for CPU 1 and CPU 3 and CPU 5, answer the following :

5 a. Which port would go first?

5 b. Which port would go next?

5 c. What option type solves the port conflict?

Hardware Trng.
Y12EX21B J.E.S.

EXERCISE (Continued)

EXERCISE NAME: CRAY Y-MP Memory Control No. 2 REVISION: 3/14/89

STUDENT NAME: _____

PTS.

5 d. For Port C, where is the write data stacked when a subsection conflict occurs?

5 e. What option type and location solves the simultaneous bank conflict?

5 f. What CPU letters are CPU 1, 3, 5, being represented as when solving the simultaneous bank conflict?

5 g. Which CPU has the higher priority?

5 h. What option type and location will generate Release Subsection 0 - 7?

5 3. What is the port priority on the (YM) option?

10 4. Upon issuing the following instruction, answer the questions below.

176100 176200 176300 177040 in CPU 4 and VL = 100

a. Which port has the highest priority?

b. Which port has the next highest priority?

c. Is there a Hold Issue? If yes, why? If no, why not?

EXERCISE

EXERCISE NAME: CRAY Y-MP Memory Control No. 2 REVISION: 09/09/88

STUDENT NAME: _____ DATE: _____

INSTRUCTOR: _____

EXERCISE TYPE: Take home, In class TIME ALLOTTED: _____

The following exercise is to determine if you can correctly go through the conflicts that a particular memory reference will experience and make the correct decisions based on the given information.

PTS.

1. Given the following absolute address 7372_8 from Ports A, B, and D for Fetch within the same clock period for CPU's 0 and 3, answer the following questions.

5 a. For CPU 0, which port would go first?

5 b. Which port would go next?

5 c. What option types solved the Port Conflict?

5 d. What option type fanned out the GOSS 0-7 Section N to the CPU modules and to the memory modules?

5 e. What option type solves the Simultaneous Bank Conflict? In which CPU?

5 f. To determine the Bank Conflicts, what option type fanned out address bit 2^5 to CPU 3 and to all other CPUs?

Hardware Trng.
Y12EX20M J.E.S.

EXERCISE (Continued)

EXERCISE NAME: CRAY Y-MP Memory Control No.2 REVISION: 09/09/88

STUDENT NAME: _____

PTS.

5 g. What CPU letters are CPU 0 and 3 being represented when solving the Simultaneous Bank Conflicts?

5 h. Which CPU, 0 or 3, has the higher priority?

5 i. What signal is generated from the (Yl) option to the (Ym) option when the Bank is released?

5 j. Which (Ym) option releases the SS conflict?

5 k. Why would Port D be released first on the (Ym) option?

5 l. What option types perform the SECDED for this word being read from memory?

2. Given the following absolute address 13331 with the increment even from Port A, B, C within the same clock period for CPU 1 and CPU 3 and CPU 5, answer the following :

5 a. Which Port would go first?

5 b. Which Port would go next?

5 c. What option type solves the Port Conflict?

Hardware Trng.
Y12EX21M J.E.S.

EXERCISE (Continued)

EXERCISE NAME: CRAY Y-MP Memory Control No. 2 REVISION: 09/09/88

STUDENT NAME: _____

PTS.

5 d. For Port C, where is the Write Data stacked when a Subsection Conflict occurs?

5 e. What option type and location solves the Simultaneous Bank Conflict?

5 f. What CPU letters are CPU 1, 3, 5, being represented as when solving the Simultaneous Bank Conflict?

5 g. Which CPU has the higher priority?

5 h. What option type and location will generate Release Subsection 0 - 7?

3. What is the port priority on the (Ym) option?