	1	Empty												
	2	WINs	A3	PINT	(F)	A2	WIN 1	(N)	A1	WIN 0	(F)	A0	Blank	
			B3	Blank		B2	MCUI	(N)	B1	Dummy		B0	Blank	
Memory Section 0	3	Data Bits 0 - 35	CPU 0 A6 - 24 Bank Bits 0 - 2 Go SS: 0 - 7 SS Read-out Selects Abort Go Write											
	4													
	5	Data Bits 36 - 71	CPU 1 A6 - 24 Bank Bits 0 - 2 Go SS: 0 - 7 SS Read-out Selects Abort Go Write											
	6													
Memory Section 1	7	Data Bits 0 - 35	CPU 0 A6 - 24 Bank Bits 0 - 2 Go SS: 0 - 7 SS Read-out Selects Abort Go Write											
	8													
	9	Data Bits 36 - 71	CPU 1 A6 - 24 Bank Bits 0 - 2 Go SS: 0 - 7 SS Read-out Selects Abort Go Write											
	10													
	11	Crossover												
	12	Shared Clock	Shared (JR) 2 - 7, 10 - 15, 18 - 23, 26 - 31, 34 - 39, 42 - 47, 50 - 55, 58 - 63 CPU 0 - 1 D.L. W.S. (HH)											
CPUs	13	CPU 0	Conflict Resolution (YL) Section 0 - 3 SS: 0 - 3			Shared (JR) 0, 8, 16, 24, 32, 40, 48, 56			LOSP 20/21		VHISP 1	(HH) Error Logger CPU 0		
	14													
	15	CPU 1	Conflict Resolution (YL) Section 0 - 3 SS: 4 - 7			Shared (JR) 1, 9, 17, 25, 33, 41, 49, 57			LOSP 22/23		VHISP 1	Priority (HH) Error Logger LOSP 20 - 23 CPU 1		
	16													
Memory Section 2	17	Data Bits 0 - 35	CPU 0 A6 - 24 Bank Bits 0 - 2 Go SS: 0 - 7 SS Read-out Selects Abort Go Write											
	18													
	19	Data Bits 36 - 71	CPU 1 A6 - 24 Bank Bits 0 - 2 Go SS: 0 - 7 SS Read-out Selects Abort Go Write											
	20													
Memory Section 3	21	Data Bits 0 - 35	CPU 0 A6 - 24 Bank Bits 0 - 2 Go SS: 0 - 7 SS Read-out Selects Abort Go Write											
	22													
	23	Data Bits 36 - 71	CPU 1 A6 - 24 Bank Bits 0 - 2 Go SS: 0 - 7 SS Read-out Selects Abort Go Write											
	24													
I/O Cluster 0	25	I/O Processors	A3	HCM	(F)	A2	CIN 0	(N)	A1	IOP MUX	(F)	A0	HCM	(N)
			B3	EIOP 3	(F)	B2	EIOP 2	(N)	B1	EIOP 1	(F)	B0	EIOP 0	(N)
	26	Buffer Board	HISP 0 Data ↔ All Buffers			EIOP 0 Data ↔ Buffers 0-3					EIOP 2 Data ↔ Buffers 10-13			
			HISP 1 Data ↔ All Buffers			EIOP 1 Data ↔ Buffers 4-7					EIOP 3 Data ↔ Buffers 14-17			
	27	Channel Adapters	A3	CA 12	(N)	A2	CA 10	(N)	A1	CA 2	(N)	A0	CA 0	(N)
			B3	CA 13	(N)	B2	CA 11	(N)	B1	CA 3	(N)	B0	CA 1	(N)
	28	Channel Adapters	A3	CA 17	(N)	A2	CA 15	(N)	A1	CA 7	(F)	A0	CA 5	(N)
			B3	CA 16	(N)	B2	CA 14	(N)	B1	CA 6	(F)	B0	CA 4	(N)
I/O Cluster 1	29	I/O Processors	A3	HCM	(F)	A2	CIN 1	(N)	A1	IOP MUX	(F)	A0	HCM	(N)
			B3	EIOP 3	(F)	B2	EIOP 2	(N)	B1	EIOP 1	(F)	B0	EIOP 0	(N)
	30	Buffer Board	HISP 0 Data ↔ All Buffers			EIOP 0 Data ↔ Buffers 0-3					EIOP 2 Data ↔ Buffers 10-13			
			HISP 1 Data ↔ All Buffers			EIOP 1 Data ↔ Buffers 4-7					EIOP 3 Data ↔ Buffers 14-17			
	31	Channel Adapters	A3	CA 12	(N)	A2	CA 10	(N)	A1	CA 2	(N)	A0	CA 0	(N)
			B3	CA 13	(N)	B2	CA 11	(N)	B1	CA 3	(N)	B0	CA 1	(N)
	32	Channel Adapters	A3	CA 17	(N)	A2	CA 15	(N)	A1	CA 7	(F)	A0	CA 5	(N)
			B3	CA 16	(N)	B2	CA 14	(N)	B1	CA 6	(F)	B0	CA 4	(N)

NOTE: All CPUs listed are physical CPUs, and all address bits are absolute bits.

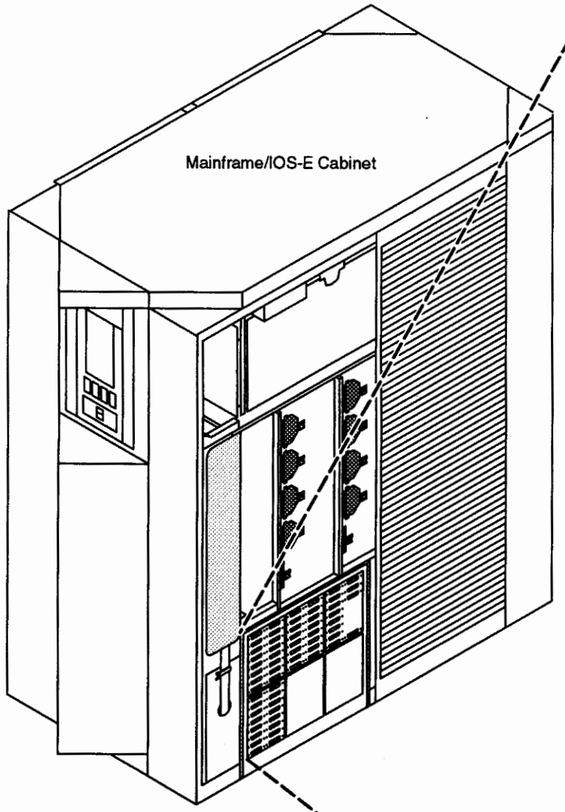
A-10027

Figure 2-29. Mainframe/IOS-E Cabinet Chassis Map (Y Side View)

		Group / Section / Module		Data Storage	Word 0 Data Steering		Word 1 Data Steering	
SSD-E Memory Section 0	1	Memory 000	A Board	Bits 0-11	Read 0: 22, 03, 00	Write 0: 00, 01, 02	Read 1: 03, 00, 07	Write 1: 06, 07, 08
			B Board	Bits 12-23	Read 0: 08, 13, 20	Write 0: 06, 07, 03	Read 1: 06, 09, 02	Write 1: 00, 01, 03
	2	Memory 010	A Board	Bits 0-11	Read 0: 23, 01, 11	Write 0: 08, 10, 04	Read 1: 04, 01, 08	Write 1: 09, 10, 11
			B Board	Bits 12-23	Read 0: 12, 17, 19	Write 0: 09, 11, 05	Read 1: 10, 11, 12	Write 1: 02, 05, 04
	3	Memory 020	A Board	Bits 0-11	Read 0: 02, 18, 09	Write 0: 12, 13, 18	Read 1: 18, 05, 16	Write 1: 12, 13, 14
			B Board	Bits 12-23	Read 0: 06, 07, 04	Write 0: 14, 15, 19	Read 1: 13, 14, 15	Write 1: 20, 21, 18
	4	Memory 030	A Board	Bits 0-11	Read 0: 21, 14, 10	Write 0: 16, 17, 20	Read 1: 19, 20, 17	Write 1: 15, 16, 17
			B Board	Bits 12-23	Read 0: 15, 16, 05	Write 0: 21, 22, 23	Read 1: 21, 22, 23	Write 1: 22, 23, 19
	5	Memory 001	A Board	Bits 24-35	Read 0: 46, 27, 24	Write 0: 24, 25, 26	Read 1: 27, 24, 31	Write 1: 30, 31, 32
			B Board	Bits 36-47	Read 0: 32, 37, 44	Write 0: 30, 31, 27	Read 1: 30, 33, 26	Write 1: 24, 25, 27
	6	Memory 011	A Board	Bits 24-35	Read 0: 47, 25, 35	Write 0: 32, 34, 28	Read 1: 28, 25, 32	Write 1: 33, 34, 35
			B Board	Bits 36-47	Read 0: 36, 41, 43	Write 0: 33, 35, 29	Read 1: 34, 35, 36	Write 1: 26, 29, 28
	7	Memory 021	A Board	Bits 24-35	Read 0: 26, 42, 33	Write 0: 36, 37, 42	Read 1: 42, 29, 40	Write 1: 36, 37, 38
			B Board	Bits 36-47	Read 0: 30, 31, 28	Write 0: 38, 39, 43	Read 1: 37, 38, 39	Write 1: 44, 45, 42
	8	Memory 031	A Board	Bits 24-35	Read 0: 45, 38, 34	Write 0: 40, 41, 44	Read 1: 43, 44, 41	Write 1: 39, 40, 41
			B Board	Bits 36-47	Read 0: 39, 40, 29	Write 0: 45, 46, 47	Read 1: 45, 46, 47	Write 1: 46, 47, 43
	9	Memory 002	A Board	Bits 48-59	Read 0: 70, 51, 48	Write 0: 48, 49, 50	Read 1: 51, 48, 55	Write 1: 54, 55, 56
			B Board	Bits 60-71	Read 0: 56, 61, 68	Write 0: 54, 55, 51	Read 1: 54, 57, 50	Write 1: 48, 49, 51
	10	Memory 012	A Board	Bits 48-59	Read 0: 71, 49, 59	Write 0: 56, 58, 52	Read 1: 52, 49, 56	Write 1: 57, 58, 59
			B Board	Bits 60-71	Read 0: 60, 65, 67	Write 0: 57, 59, 53	Read 1: 58, 59, 60	Write 1: 50, 53, 52
	11	Memory 022	A Board	Bits 48-59	Read 0: 50, 66, 57	Write 0: 60, 61, 66	Read 1: 66, 53, 64	Write 1: 60, 61, 62
			B Board	Bits 60-71	Read 0: 54, 55, 52	Write 0: 62, 63, 67	Read 1: 61, 62, 63	Write 1: 68, 69, 66
	12	Memory 032	A Board	Bits 48-59	Read 0: 69, 62, 58	Write 0: 64, 65, 68	Read 1: 67, 68, 65	Write 1: 63, 64, 65
			B Board	Bits 60-71	Read 0: 63, 64, 53	Write 0: 69, 70, 71	Read 1: 69, 70, 71	Write 1: 70, 71, 67
	13	Crossover						
	14	SSD-E Clock						
	15	SSD-E Control	Maintenance Channel ↔ MWS-E or OWS-E			SSD-E Error Logger ↔ MWS-E		
	16	SSD-E Port/Buffer 0/1	HISP 0 Data ↔ IOS-E			VHISP 0 Data ↔ Mainframe		
	17		HISP 1 Data ↔ IOS-E			Data Test 0 ↔ SSD-E Control		
	18	Empty						
	19	Empty						
	20	Empty						
	21	Empty						
	22	Empty						
	23	Empty						
	24	Empty						
	25	Empty						
	26	Empty						
	27	Empty						
	28	Empty						
	29	Empty						
	30	Empty						
	31	Empty						
	32	Empty						

A-10029

Figure 2-30. SSD-E Cabinet Chassis Map (Y Side View)



NOTE: This configuration may include cabinets with serial numbers 1610 - 1612, 1614 - 1644, 1648 - 1650, 1652 - 1654, 1656, 1658, 1660, and 1661. However, due to system modifications, some cabinets may no longer correspond to this arrangement.

† Some cabinets contain a real-time interrupt 0 connector.

I/O Cluster 0 Channel Adapters

ZA

IOC 0 CA-0 __CA__ IN EIOP 0 30 _____	IOC 0 CA-10 __CA__ IN EIOP 2 30 _____
IOC 0 CA-0 __CA__ OUT EIOP 0 31 _____	IOC 0 CA-10 __CA__ OUT EIOP 2 31 _____
IOC 0 CA-2 __CA__ IN EIOP 0 34 _____	IOC 0 CA-12 __CA__ IN EIOP 2 34 _____
IOC 0 CA-2 __CA__ OUT EIOP 0 35 _____	IOC 0 CA-12 __CA__ OUT EIOP 2 35 _____
IOC 0 CA-5 __CA__ IN EIOP 1 32 _____	IOC 0 CA-15 __CA__ IN EIOP 3 32 _____
IOC 0 CA-5 __CA__ OUT EIOP 1 33 _____	IOC 0 CA-15 __CA__ OUT EIOP 3 33 _____
IOC 0 CA-7 __CA__ IN EIOP 1 36 _____	IOC 0 CA-17 __CA__ IN EIOP 3 36 _____
IOC 0 CA-7 __CA__ OUT EIOP 1 37 _____	IOC 0 CA-17 __CA__ OUT EIOP 3 37 _____

I/O Cluster 1 Channel Adapters

ZB

IOC 1 CA-0 __CA__ IN EIOP 0 30 _____	IOC 1 CA-10 __CA__ IN EIOP 2 30 _____
IOC 1 CA-0 __CA__ OUT EIOP 0 31 _____	IOC 1 CA-10 __CA__ OUT EIOP 2 31 _____
IOC 1 CA-2 __CA__ IN EIOP 0 34 _____	IOC 1 CA-12 __CA__ IN EIOP 2 34 _____
IOC 1 CA-2 __CA__ OUT EIOP 0 35 _____	IOC 1 CA-12 __CA__ OUT EIOP 2 35 _____
IOC 1 CA-5 __CA__ IN EIOP 1 32 _____	IOC 1 CA-15 __CA__ IN EIOP 3 32 _____
IOC 1 CA-5 __CA__ OUT EIOP 1 33 _____	IOC 1 CA-15 __CA__ OUT EIOP 3 33 _____
IOC 1 CA-7 __CA__ IN EIOP 1 36 _____	IOC 1 CA-17 __CA__ IN EIOP 3 36 _____
IOC 1 CA-7 __CA__ OUT EIOP 1 37 _____	IOC 1 CA-17 __CA__ OUT EIOP 3 37 _____

ZC

IOS-E TO ZIF IN HISP 0–23	ZIF TO CPU LOSP IN
IOS-E TO ZIF IN HISP 24–47	ZIF TO CPU LOSP OUT
IOS-E TO ZIF IN HISP 48–71	ZIF TO CPU LOSP CONTROL
IOS-E TO ZIF OUT HISP 0–23	
IOS-E TO ZIF OUT HISP 24–47	
IOS-E TO ZIF OUT HISP 48–71	
IOS-E TO ZIF IN HISP CONTROL	
IOS-E TO ZIF OUT HISP CONTROL	IOSE TO ZIF HISP ADDRESS EXPANSION

ZD

IOC 0 CA-14 __CA__ 200MB (P3) _____

IOC 0 CA-14 __CA__ 200MB (P2) _____

ZE

REAL-TIME INTERRUPT 0 †

ZF

A-10064

Figure 3-41. Mainframe/IOS-E CINCH Connector Worksheet for Z Side of Some Cabinets

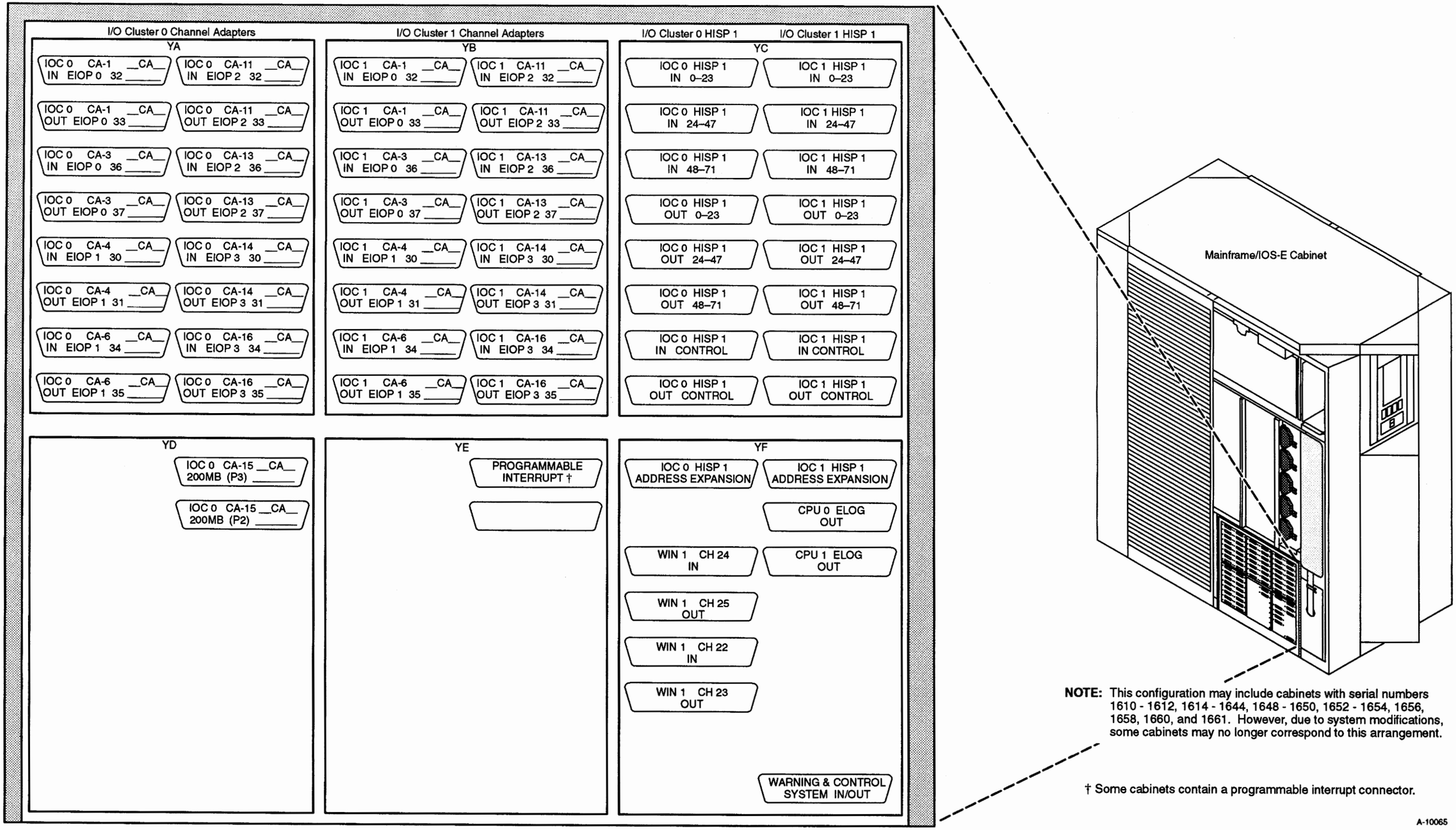
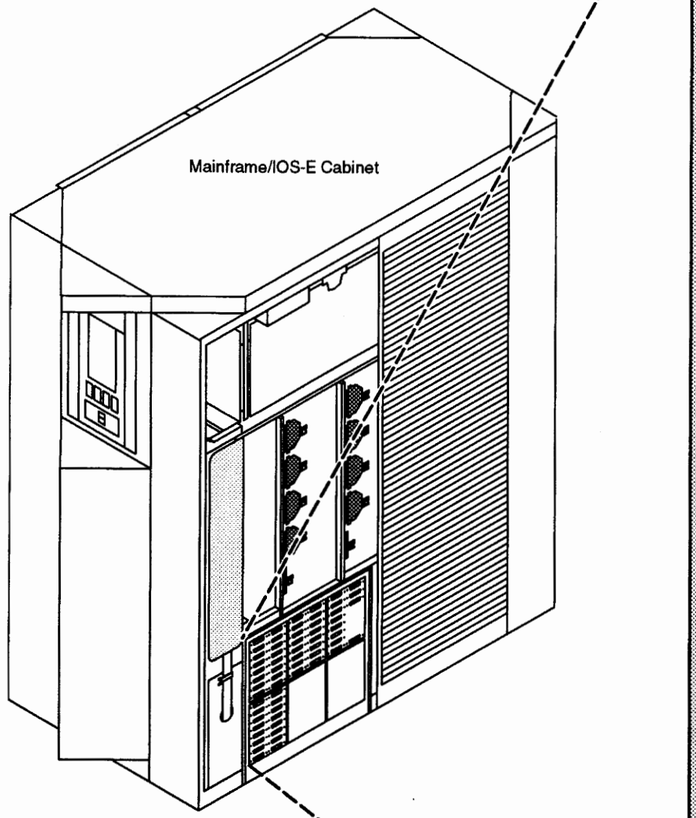


Figure 3-42. Mainframe/IOS-E CINCH Connector Worksheet for Y Side of Some Cabinets



NOTE: This configuration may include cabinets with serial numbers 1613, 1645 - 1647, 1651, 1655, 1657, 1659, 1662, and greater.

I/O Cluster 0 Channel Adapters

ZA

IOC 0 CA-0 __CA__ IN EIOP 0 30 _____	IOC 0 CA-10 __CA__ IN EIOP 2 30 _____
IOC 0 CA-0 __CA__ OUT EIOP 0 31 _____	IOC 0 CA-10 __CA__ OUT EIOP 2 31 _____
IOC 0 CA-2 __CA__ IN EIOP 0 34 _____	IOC 0 CA-12 __CA__ IN EIOP 2 34 _____
IOC 0 CA-2 __CA__ OUT EIOP 0 35 _____	IOC 0 CA-12 __CA__ OUT EIOP 2 35 _____
IOC 0 CA-5 __CA__ IN EIOP 1 32 _____	IOC 0 CA-15 __CA__ IN EIOP 3 32 _____
IOC 0 CA-5 __CA__ OUT EIOP 1 33 _____	IOC 0 CA-15 __CA__ OUT EIOP 3 33 _____
IOC 0 CA-7 __CA__ IN EIOP 1 36 _____	IOC 0 CA-17 __CA__ IN EIOP 3 36 _____
IOC 0 CA-7 __CA__ OUT EIOP 1 37 _____	IOC 0 CA-17 __CA__ OUT EIOP 3 37 _____

I/O Cluster 1 Channel Adapters

ZB

IOC 1 CA-0 __CA__ IN EIOP 0 30 _____	IOC 1 CA-10 __CA__ IN EIOP 2 30 _____
IOC 1 CA-0 __CA__ OUT EIOP 0 31 _____	IOC 1 CA-10 __CA__ OUT EIOP 2 31 _____
IOC 1 CA-2 __CA__ IN EIOP 0 34 _____	IOC 1 CA-12 __CA__ IN EIOP 2 34 _____
IOC 1 CA-2 __CA__ OUT EIOP 0 35 _____	IOC 1 CA-12 __CA__ OUT EIOP 2 35 _____
IOC 1 CA-5 __CA__ IN EIOP 1 32 _____	IOC 1 CA-15 __CA__ IN EIOP 3 32 _____
IOC 1 CA-5 __CA__ OUT EIOP 1 33 _____	IOC 1 CA-15 __CA__ OUT EIOP 3 33 _____
IOC 1 CA-7 __CA__ IN EIOP 1 36 _____	IOC 1 CA-17 __CA__ IN EIOP 3 36 _____
IOC 1 CA-7 __CA__ OUT EIOP 1 37 _____	IOC 1 CA-17 __CA__ OUT EIOP 3 37 _____

ZC

IOS-E TO ZIF IN HISP 0–23	ZIF TO CPU LOSP IN
IOS-E TO ZIF IN HISP 24–47	ZIF TO CPU LOSP OUT
IOS–E TO ZIF IN HISP 48–71	ZIF TO CPU LOSP CONTROL
IOS-E TO ZIF OUT HISP 0–23	SSD ELOG (some systems)
IOS-E TO ZIF OUT HISP 24–47	
IOS-E TO ZIF OUT HISP 48–71	
IOS-E TO ZIF IN HISP CONTROL	
IOS-E TO ZIF OUT HISP CONTROL	IOS-E TO ZIF HISP ADDRESS EXPANSION

ZD

IOC 0 CA-1 __CA__ DRIVE 4 (P3) _____	IOC 0 CA-11 __CA__ DRIVE 4 (P3) _____
IOC 0 CA-4 __CA__ DRIVE 4 (P3) _____	IOC 0 CA-14 __CA__ DRIVE 4 (P3) _____
	IOC 0 CA-14 __CA__ 200MB (P2) _____

ZE

IOC 1 CA-1 __CA__ DRIVE 4 (P3) _____	IOC 1 CA-11 __CA__ DRIVE 4 (P3) _____
IOC 1 CA-4 __CA__ DRIVE 4 (P3) _____	IOC 1 CA-14 __CA__ DRIVE 4 (P3) _____

ZF

REAL-TIME INTERRUPT 0

A-11402

Figure 3-43. Mainframe/IOS-E CINCH Connector Worksheet for Z Side of Cabinets with Drive 4 Connectors

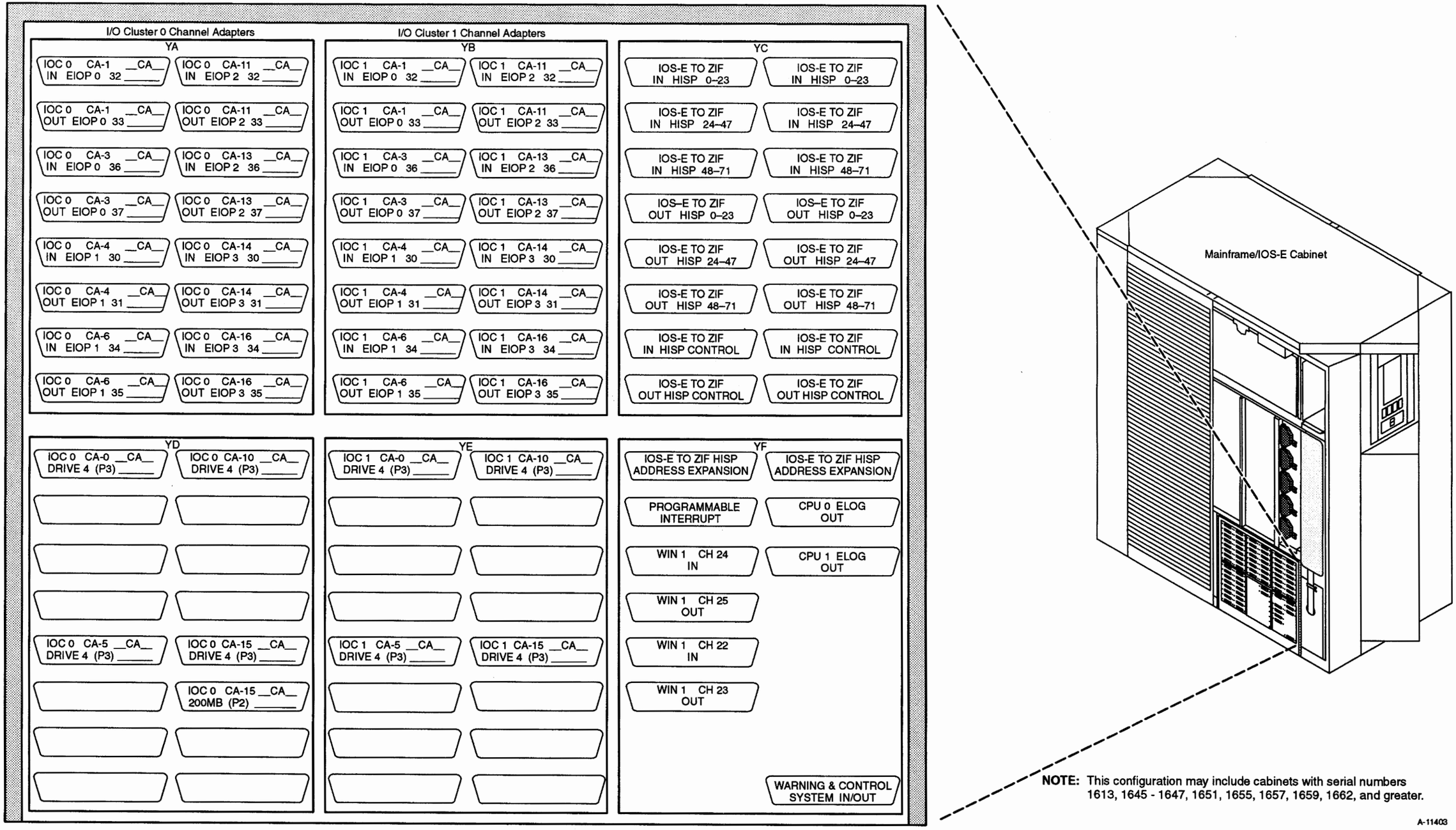
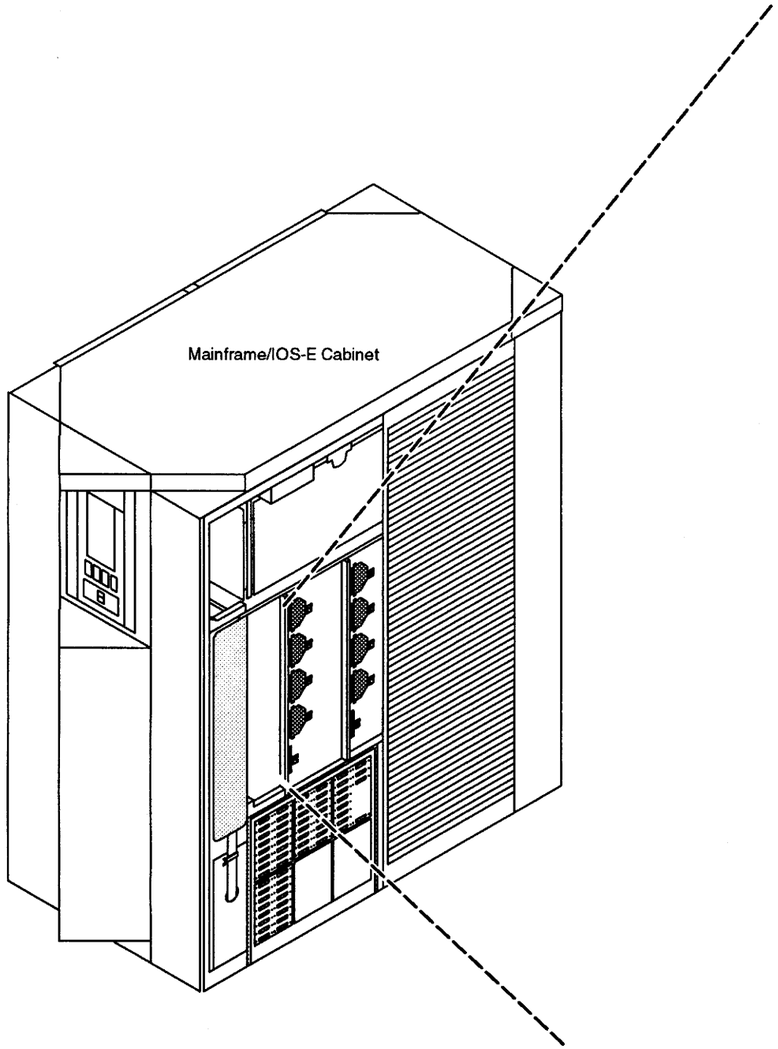


Figure 3-44. Mainframe/IOS-E CINCH Connector Worksheet for Y Side of Cabinets with Drive 4 Connectors

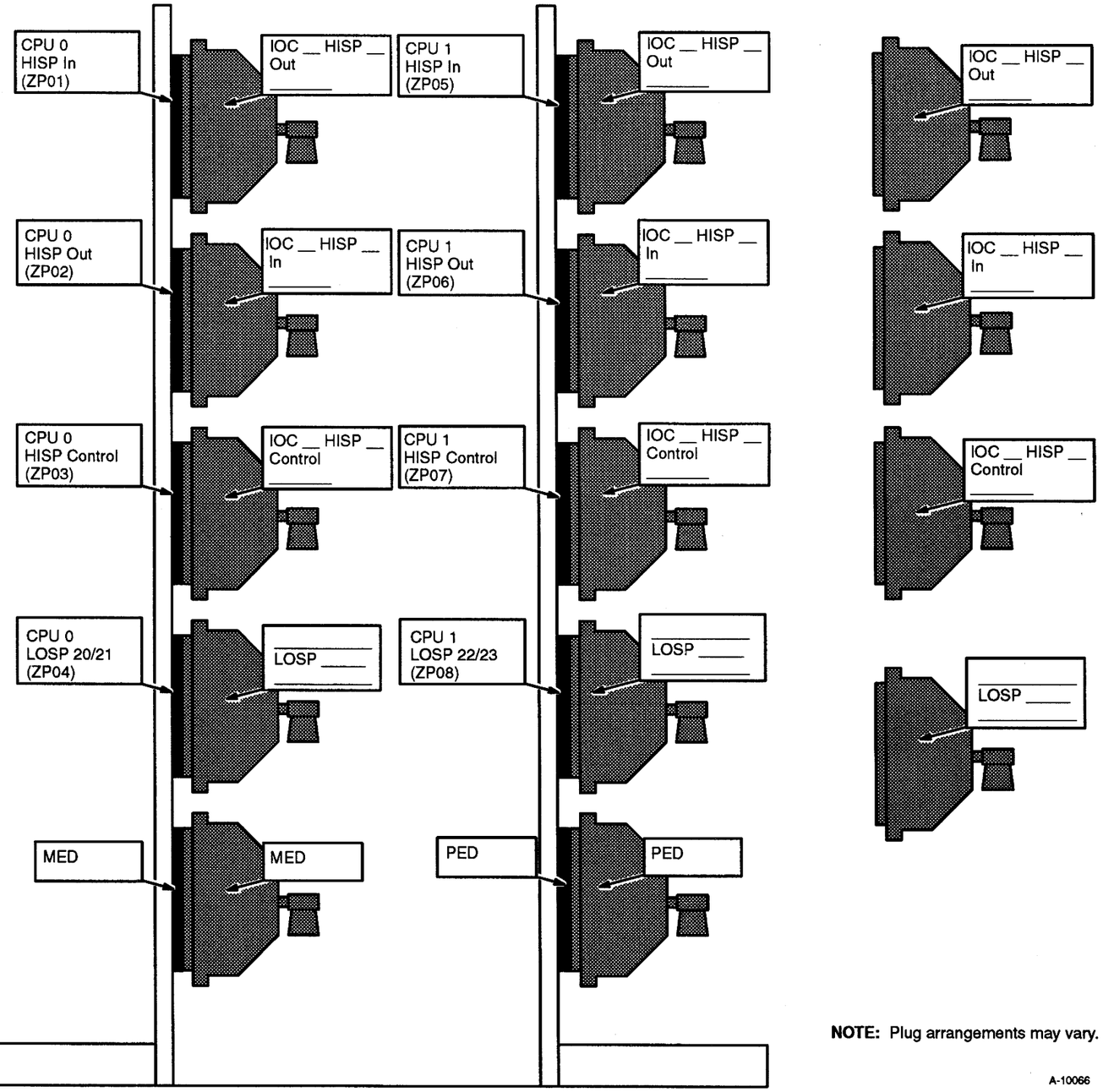


NOTE: Plug for ZP01 can be ZP02 IOC 0 HISP 0 Out or IOS-E to ZIF HISP 1 Out

Plug for ZP02 can be ZP01 IOC 0 HISP 0 In or IOS-E to ZIF HISP 1 In

Plug for ZP03 can be ZP03 IOC 0 HISP 0 Control or IOS-E to ZIF HISP 1 Control

Plug for ZP04 can be ZP04 IOC 0 LOSP 20/21 or IOS-E to ZIF LOSP 20/21



NOTE: Plug arrangements may vary.

A-10066

Figure 3-45. Mainframe/IOS-E ZIF Connector Worksheet for Z Side of Cabinet (Serial Numbers 1600 and Greater)

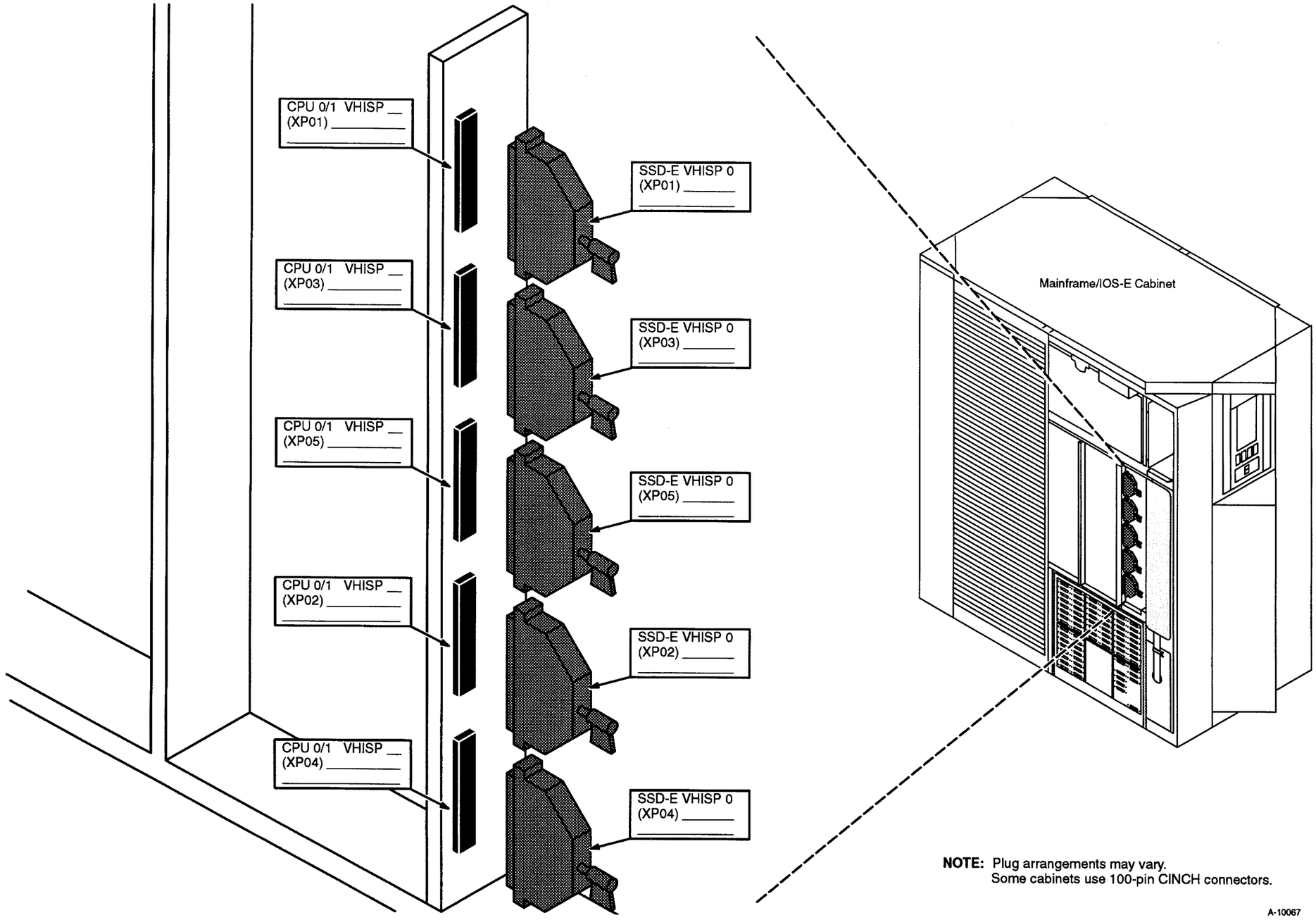


Figure 3-46. Mainframe/IOS-E VHISP ZIF Connector Worksheet for Y Side of Cabinet (Serial Numbers 1600 through 1662)

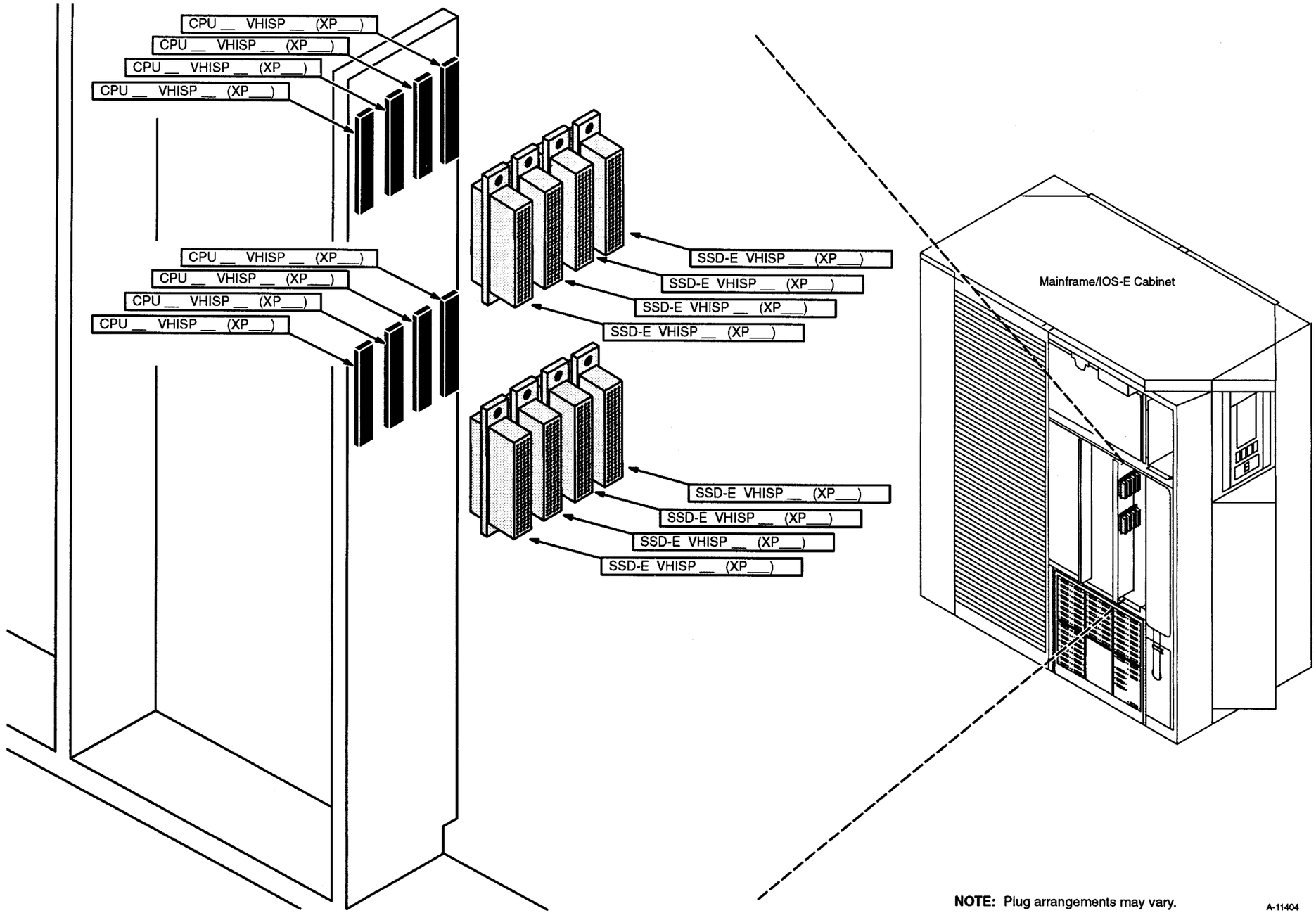
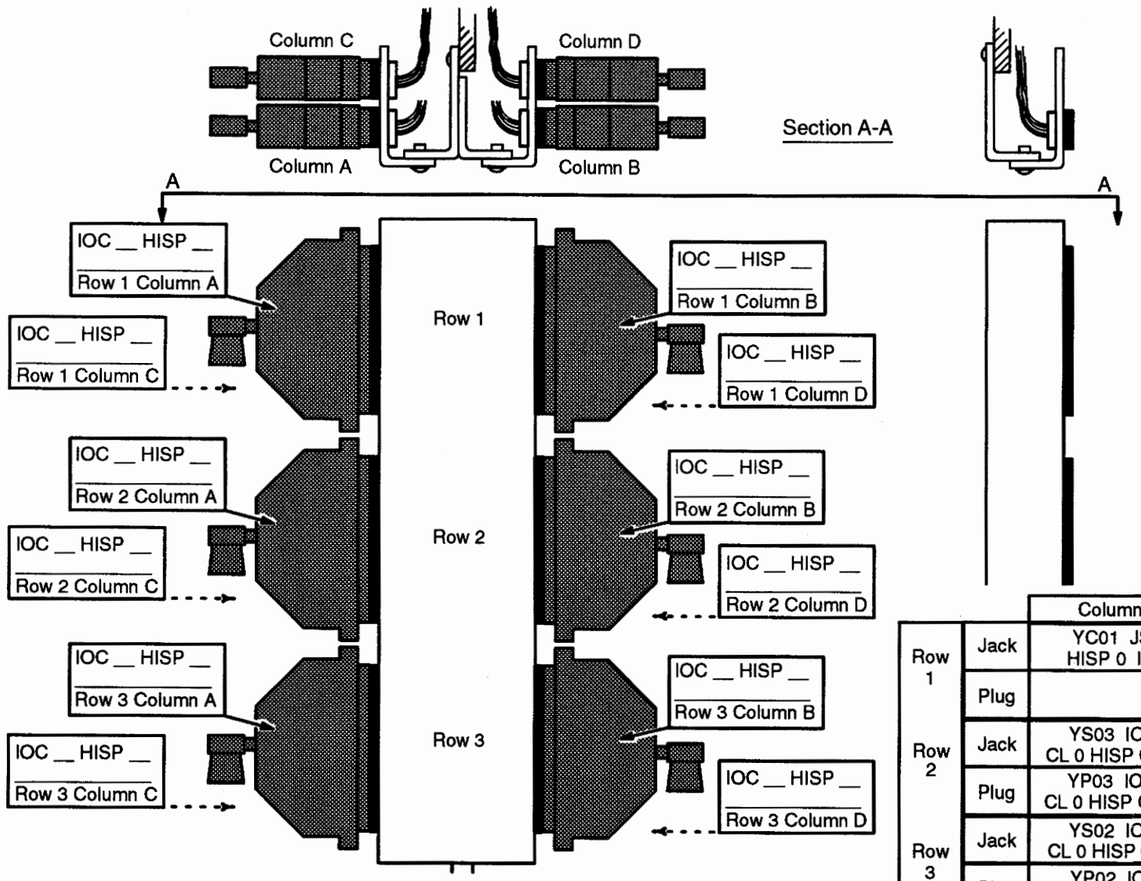


Figure 3-47. Mainframe/IOS-E 100-pin CINCH Connector Worksheet for Y Side of Cabinet (Serial Numbers 1663 and Greater)

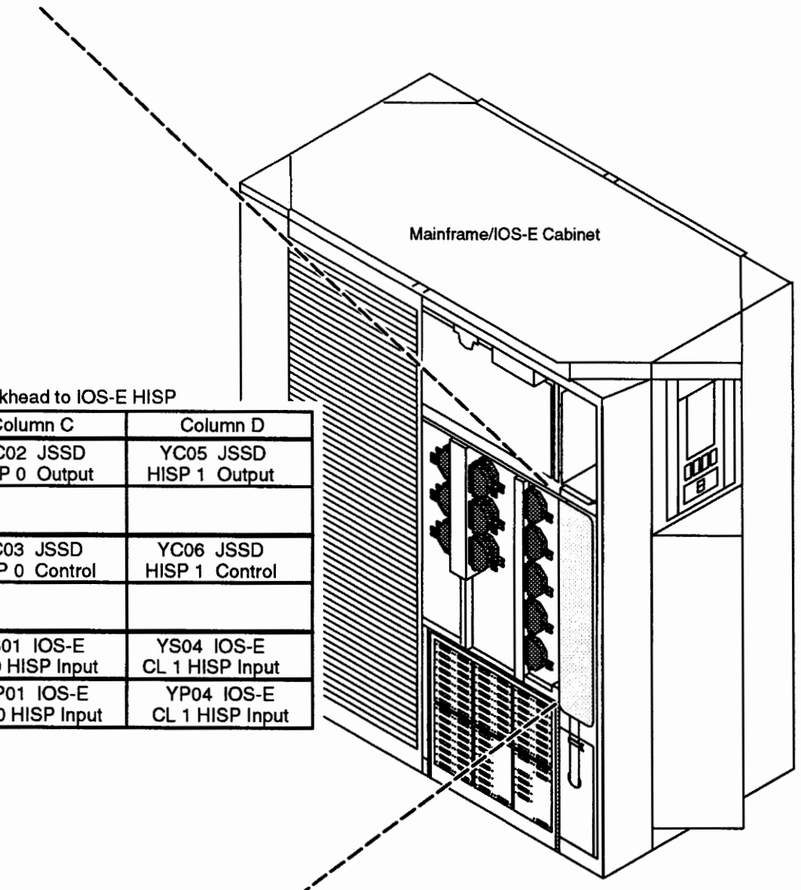


Y Side ZIF Plug Connection for SSD-E/32i HISP

		Column A	Column B	Column C	Column D
Row 1	Jack	YC01 JSSD HISP 0 Input	YC04 JSSD HISP 1 Input	YC02 JSSD HISP 0 Output	YC05 JSSD HISP 1 Output
	Plug	YP02 IOS-E CL 0 HISP Output	YP05 IOS-E CL 1 HISP Output	YP01 IOS-E CL 0 HISP Input	YP04 IOS-E CL 1 HISP Input
Row 2	Jack	YS03 IOS-E CL 0 HISP Control	YS06 IOS-E CL 1 HISP Control	YC03 JSSD HISP 0 Control	YC06 JSSD HISP 1 Control
	Plug			YP03 IOS-E CL 0 HISP Control	YP06 IOS-E CL 1 HISP Control
Row 3	Jack	YS02 IOS-E CL 0 HISP Output	YS05 IOS-E CL 1 HISP Output	YS01 IOS-E CL 0 HISP Input	YS04 IOS-E CL 1 HISP Input
	Plug				

Y Side ZIF Plug Connection for Bulkhead to IOS-E HISP

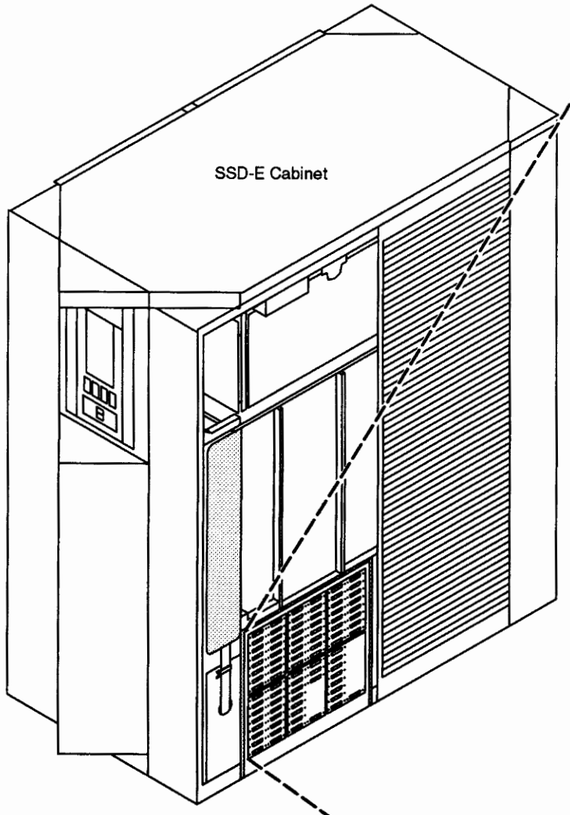
		Column A	Column B	Column C	Column D
Row 1	Jack	YC01 JSSD HISP 0 Input	YC04 JSSD HISP 1 Input	YC02 JSSD HISP 0 Output	YC05 JSSD HISP 1 Output
	Plug				
Row 2	Jack	YS03 IOS-E CL 0 HISP Control	YS06 IOS-E CL 1 HISP Control	YC03 JSSD HISP 0 Control	YC06 JSSD HISP 1 Control
	Plug	YP03 IOS-E CL 0 HISP Control	YP06 IOS-E CL 1 HISP Control		
Row 3	Jack	YS02 IOS-E CL 0 HISP Output	YS05 IOS-E CL 1 HISP Output	YS01 IOS-E CL 0 HISP Input	YS04 IOS-E CL 1 HISP Input
	Plug	YP02 IOS-E CL 0 HISP Output	YP05 IOS-E CL 1 HISP Output	YP01 IOS-E CL 0 HISP Input	YP04 IOS-E CL 1 HISP Input



NOTE: Jacks YCxx = SSD-E/32i HISP from Z-side crossover.
Jacks YSxx = adapter cable from ZIF to bulkhead.
Plugs for YPxx are from IOS-E section of machine.
Only six ZIF connectors are used in either configuration.
Plug arrangements may vary.
Some cabinets have 100-pin CINCH connectors for VHISP channels.

A-11405

Figure 3-48. Mainframe/IOS-E ZIF Connector Worksheet for Y Side of Cabinets Configured for SSD-E/32i (JSSD)



I/O Cluster 0 Channel Adapters — ZA

IOC 0 CA-0 __CA__ IN EIOP 0 30	IOC 0 CA-10 __CA__ IN EIOP 2 30
IOC 0 CA-0 __CA__ OUT EIOP 0 31	IOC 0 CA-10 __CA__ OUT EIOP 2 31
IOC 0 CA-2 __CA__ IN EIOP 0 34	IOC 0 CA-12 __CA__ IN EIOP 2 34
IOC 0 CA-2 __CA__ OUT EIOP 0 35	IOC 0 CA-12 __CA__ OUT EIOP 2 35
IOC 0 CA-5 __CA__ IN EIOP 1 32	IOC 0 CA-15 __CA__ IN EIOP 3 32
IOC 0 CA-5 __CA__ OUT EIOP 1 33	IOC 0 CA-15 __CA__ OUT EIOP 3 33
IOC 0 CA-7 __CA__ IN EIOP 1 36	IOC 0 CA-17 __CA__ IN EIOP 3 36
IOC 0 CA-7 __CA__ OUT EIOP 1 37	IOC 0 CA-17 __CA__ OUT EIOP 3 37

I/O Cluster 1 Channel Adapters — ZB

IOC 1 CA-0 __CA__ IN EIOP 0 30	IOC 1 CA-10 __CA__ IN EIOP 2 30
IOC 1 CA-0 __CA__ OUT EIOP 0 31	IOC 1 CA-10 __CA__ OUT EIOP 2 31
IOC 1 CA-2 __CA__ IN EIOP 0 34	IOC 1 CA-12 __CA__ IN EIOP 2 34
IOC 1 CA-2 __CA__ OUT EIOP 0 35	IOC 1 CA-12 __CA__ OUT EIOP 2 35
IOC 1 CA-5 __CA__ IN EIOP 1 32	IOC 1 CA-15 __CA__ IN EIOP 3 32
IOC 1 CA-5 __CA__ OUT EIOP 1 33	IOC 1 CA-15 __CA__ OUT EIOP 3 33
IOC 1 CA-7 __CA__ IN EIOP 1 36	IOC 1 CA-17 __CA__ IN EIOP 3 36
IOC 1 CA-7 __CA__ OUT EIOP 1 37	IOC 1 CA-17 __CA__ OUT EIOP 3 37

I/O Cluster 2 Channel Adapters — ZC

IOC 2 CA-0 __CA__ IN EIOP 0 30	IOC 2 CA-10 __CA__ IN EIOP 2 30
IOC 2 CA-0 __CA__ OUT EIOP 0 31	IOC 2 CA-10 __CA__ OUT EIOP 2 31
IOC 2 CA-2 __CA__ IN EIOP 0 34	IOC 2 CA-12 __CA__ IN EIOP 2 34
IOC 2 CA-2 __CA__ OUT EIOP 0 35	IOC 2 CA-12 __CA__ OUT EIOP 2 35
IOC 2 CA-5 __CA__ IN EIOP 1 32	IOC 2 CA-15 __CA__ IN EIOP 3 32
IOC 2 CA-5 __CA__ OUT EIOP 1 33	IOC 2 CA-15 __CA__ OUT EIOP 3 33
IOC 2 CA-7 __CA__ IN EIOP 1 36	IOC 2 CA-17 __CA__ IN EIOP 3 36
IOC 2 CA-7 __CA__ OUT EIOP 1 37	IOC 2 CA-17 __CA__ OUT EIOP 3 37

ZD

IOC 0 HISP 0 IN 0–23	IOC 0 CA-1 __CA__ DRIVE 4 (P3)
IOC 0 HISP 0 IN 24–47	IOC 0 CA-4 __CA__ DRIVE 4 (P3)
IOC 0 HISP 0 IN 48–71	IOC 0 CA-11 __CA__ DRIVE 4 (P3)
IOC 0 HISP 0 OUT 0–23	IOC 0 CA-14 __CA__ DRIVE 4 (P3)
IOC 0 HISP 0 OUT 24–47	IOC 0 CA-14 __CA__ 200MB (P2)
IOC 0 HISP 0 OUT 48–71	IOC 0 IN LOSP
IOC 0 HISP 0 IN CONTROL	IOC 0 OUT LOSP
IOC 0 HISP 0 OUT CONTROL	IOC 0 CONTROL LOSP
IOC 0 HISP 0 ADDRESS EXPANSION	

ZE

IOC 1 HISP 0 IN 0–23	IOC 1 CA-1 __CA__ DRIVE 4 (P3)
IOC 1 HISP 0 IN 24–47	IOC 1 CA-4 __CA__ DRIVE 4 (P3)
IOC 1 HISP 0 IN 48–71	IOC 1 CA-11 __CA__ DRIVE 4 (P3)
IOC 1 HISP 0 OUT 0–23	IOC 1 CA-14 __CA__ DRIVE 4 (P3)
IOC 1 HISP 0 OUT 24–47	
IOC 1 HISP 0 OUT 48–71	IOC 1 IN LOSP
IOC 1 HISP 0 IN CONTROL	IOC 1 OUT LOSP
IOC 1 HISP 0 OUT CONTROL	IOC 1 CONTROL LOSP
IOC 1 HISP 0 ADDRESS EXPANSION	

ZF

IOC 2 HISP 0 IN 0–23	IOC 2 CA-1 __CA__ DRIVE 4 (P3)
IOC 2 HISP 0 IN 24–47	IOC 2 CA-4 __CA__ DRIVE 4 (P3)
IOC 2 HISP 0 IN 48–71	IOC 2 CA-11 __CA__ DRIVE 4 (P3)
IOC 2 HISP 0 OUT 0–23	IOC 2 CA-14 __CA__ DRIVE 4 (P3)
IOC 2 HISP 0 OUT 24–47	
IOC 2 HISP 0 OUT 48–71	IOC 2 IN LOSP
IOC 2 HISP 0 IN CONTROL	IOC 2 OUT LOSP
IOC 2 HISP 0 OUT CONTROL	IOC 2 CONTROL LOSP
IOC 2 HISP 0 ADDRESS EXPANSION	

A-10068

Figure 3-49. SSD-E CINCH Connector Worksheet for Z Side of Cabinet (Serial Numbers 815, 816, 822, and Greater)

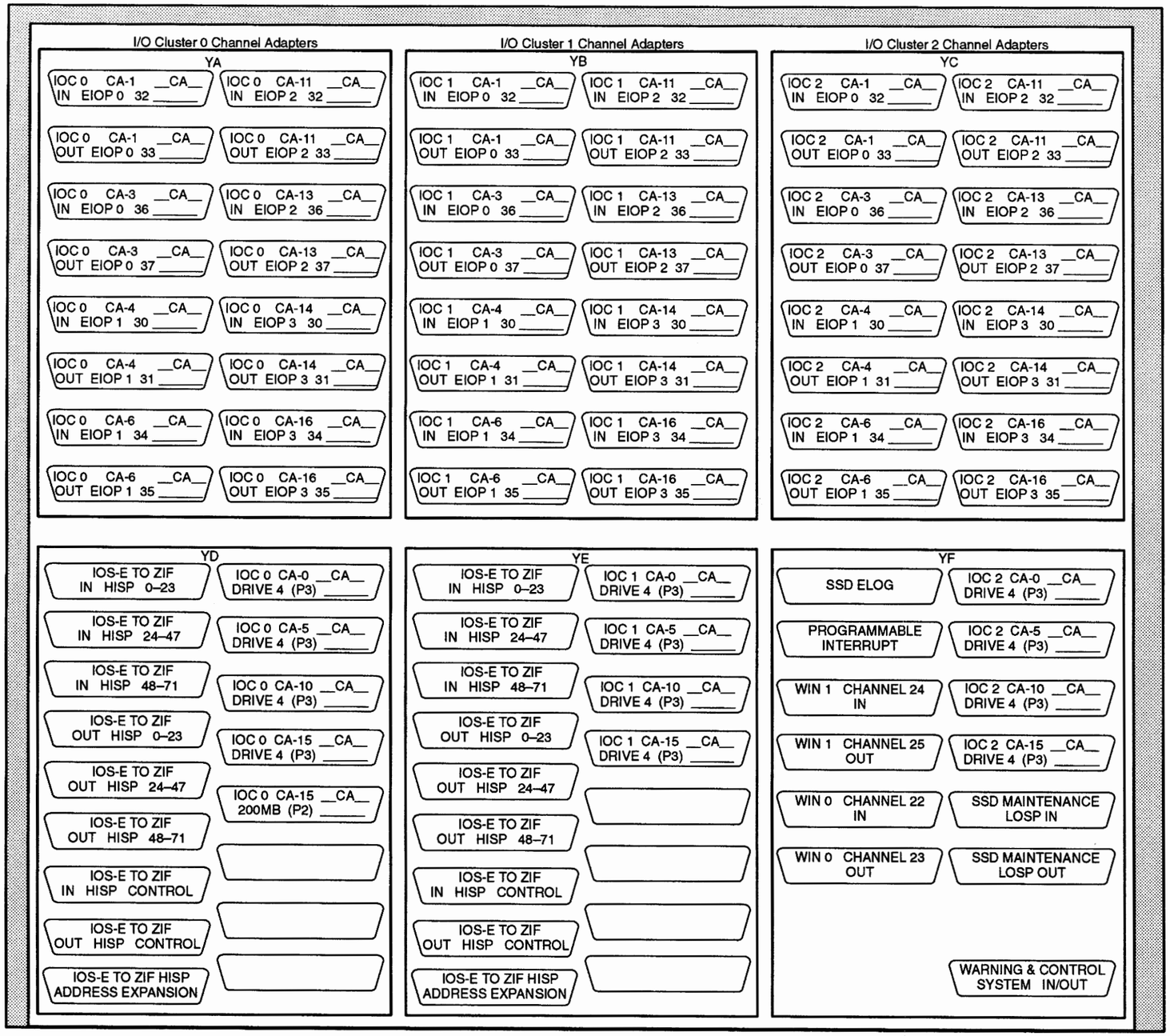
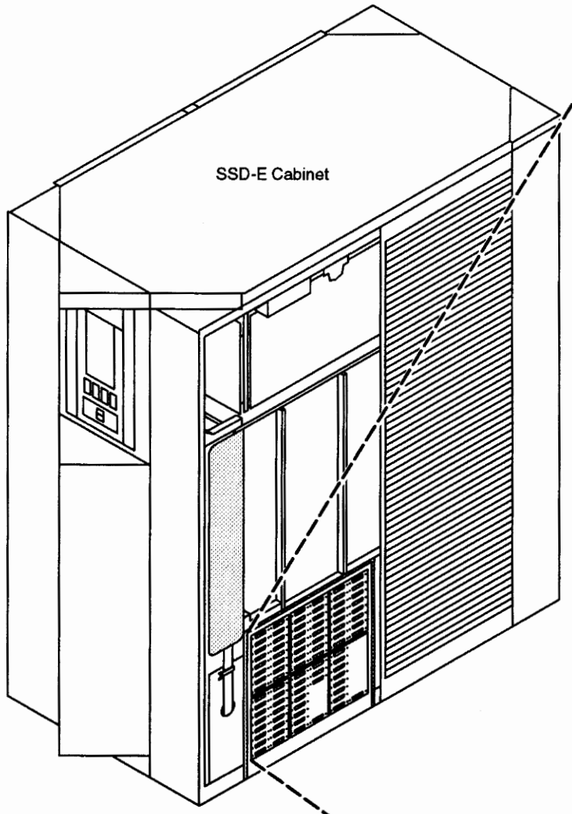


Figure 3-50. SSD-E CINCH Connector Worksheet for Y Side of Cabinet (Serial Numbers 815, 816, 822, and Greater)



I/O Cluster 0 Channel Adapters

ZA

IOC 0 CA-0 __CA__ IN EIOP 0 30	IOC 0 CA-10 __CA__ IN EIOP 2 30
IOC 0 CA-0 __CA__ OUT EIOP 0 31	IOC 0 CA-10 __CA__ OUT EIOP 2 31
IOC 0 CA-2 __CA__ IN EIOP 0 34	IOC 0 CA-12 __CA__ IN EIOP 2 34
IOC 0 CA-2 __CA__ OUT EIOP 0 35	IOC 0 CA-12 __CA__ OUT EIOP 2 35
IOC 0 CA-5 __CA__ IN EIOP 1 32	IOC 0 CA-15 __CA__ IN EIOP 3 32
IOC 0 CA-5 __CA__ OUT EIOP 1 33	IOC 0 CA-15 __CA__ OUT EIOP 3 33
IOC 0 CA-7 __CA__ IN EIOP 1 36	IOC 0 CA-17 __CA__ IN EIOP 3 36
IOC 0 CA-7 __CA__ OUT EIOP 1 37	IOC 0 CA-17 __CA__ OUT EIOP 3 37

I/O Cluster 1 Channel Adapters

ZB

IOC 1 CA-0 __CA__ IN EIOP 0 30	IOC 1 CA-10 __CA__ IN EIOP 2 30
IOC 1 CA-0 __CA__ OUT EIOP 0 31	IOC 1 CA-10 __CA__ OUT EIOP 2 31
IOC 1 CA-2 __CA__ IN EIOP 0 34	IOC 1 CA-12 __CA__ IN EIOP 2 34
IOC 1 CA-2 __CA__ OUT EIOP 0 35	IOC 1 CA-12 __CA__ OUT EIOP 2 35
IOC 1 CA-5 __CA__ IN EIOP 1 32	IOC 1 CA-15 __CA__ IN EIOP 3 32
IOC 1 CA-5 __CA__ OUT EIOP 1 33	IOC 1 CA-15 __CA__ OUT EIOP 3 33
IOC 1 CA-7 __CA__ IN EIOP 1 36	IOC 1 CA-17 __CA__ IN EIOP 3 36
IOC 1 CA-7 __CA__ OUT EIOP 1 37	IOC 1 CA-17 __CA__ OUT EIOP 3 37

I/O Cluster 2 Channel Adapters

ZC

IOC 2 CA-0 __CA__ IN EIOP 0 30	IOC 2 CA-10 __CA__ IN EIOP 2 30
IOC 2 CA-0 __CA__ OUT EIOP 0 31	IOC 2 CA-10 __CA__ OUT EIOP 2 31
IOC 2 CA-2 __CA__ IN EIOP 0 34	IOC 2 CA-12 __CA__ IN EIOP 2 34
IOC 2 CA-2 __CA__ OUT EIOP 0 35	IOC 2 CA-12 __CA__ OUT EIOP 2 35
IOC 2 CA-5 __CA__ IN EIOP 1 32	IOC 2 CA-15 __CA__ IN EIOP 3 32
IOC 2 CA-5 __CA__ OUT EIOP 1 33	IOC 2 CA-15 __CA__ OUT EIOP 3 33
IOC 2 CA-7 __CA__ IN EIOP 1 36	IOC 2 CA-17 __CA__ IN EIOP 3 36
IOC 2 CA-7 __CA__ OUT EIOP 1 37	IOC 2 CA-17 __CA__ OUT EIOP 3 37

ZD

IOC 0 HISP 0 IN 0–23	IOC 0 CA-14 __CA__ 200MB (P3)
IOC 0 HISP 0 IN 24–47	IOC 0 CA-14 __CA__ 200MB (P2)
IOC 0 HISP 0 IN 48–71	
IOC 0 HISP 0 OUT 0–23	
IOC 0 HISP 0 OUT 24–47	IOC 0 IN LOSP
IOC 0 HISP 0 OUT 48–71	IOC 0 OUT LOSP
IOC 0 HISP 0 IN CONTROL	IOC 0 CONTROL LOSP
IOC 0 HISP 0 OUT CONTROL	IOC 0 HISP 0 ADDRESS EXPANSION

ZE

IOC 1 HISP 0 IN 0–23	IOC 1 IN LOSP
IOC 1 HISP 0 IN 24–47	IOC 1 OUT LOSP
IOC 1 HISP 0 IN 48–71	IOC 1 CONTROL LOSP
IOC 1 HISP 0 OUT 0–23	
IOC 1 HISP 0 OUT 24–47	
IOC 1 HISP 0 OUT 48–71	
IOC 1 HISP 0 IN CONTROL	
IOC 1 HISP 0 OUT CONTROL	IOC 1 HISP 0 ADDRESS EXPANSION

ZF

IOC 2 HISP 0 IN 0–23	IOC 2 IN LOSP
IOC 2 HISP 0 IN 24–47	IOC 2 OUT LOSP
IOC 2 HISP 0 IN 48–71	IOC 2 CONTROL LOSP
IOC 2 HISP 0 OUT 0–23	
IOC 2 HISP 0 OUT 24–47	
IOC 2 HISP 0 OUT 48–71	
IOC 2 HISP 0 IN CONTROL	
IOC 2 HISP 0 OUT CONTROL	IOC 2 HISP 0 ADDRESS EXPANSION

A-10073

Figure 3-51. SSD-E CINCH Connector Worksheet for Z Side of Cabinet (Serial Numbers 817 through 821)

I/O Cluster 0 Channel Adapters
YA

IOC 0 CA-1 __CA__ IN EIOP 0 32 _____	IOC 0 CA-11 __CA__ IN EIOP 2 32 _____
IOC 0 CA-1 __CA__ OUT EIOP 0 33 _____	IOC 0 CA-11 __CA__ OUT EIOP 2 33 _____
IOC 0 CA-3 __CA__ IN EIOP 0 36 _____	IOC 0 CA-13 __CA__ IN EIOP 2 36 _____
IOC 0 CA-3 __CA__ OUT EIOP 0 37 _____	IOC 0 CA-13 __CA__ OUT EIOP 2 37 _____
IOC 0 CA-4 __CA__ IN EIOP 1 30 _____	IOC 0 CA-14 __CA__ IN EIOP 3 30 _____
IOC 0 CA-4 __CA__ OUT EIOP 1 31 _____	IOC 0 CA-14 __CA__ OUT EIOP 3 31 _____
IOC 0 CA-6 __CA__ IN EIOP 1 34 _____	IOC 0 CA-16 __CA__ IN EIOP 3 34 _____
IOC 0 CA-6 __CA__ OUT EIOP 1 35 _____	IOC 0 CA-16 __CA__ OUT EIOP 3 35 _____

I/O Cluster 1 Channel Adapters
YB

IOC 1 CA-1 __CA__ IN EIOP 0 32 _____	IOC 1 CA-11 __CA__ IN EIOP 2 32 _____
IOC 1 CA-1 __CA__ OUT EIOP 0 33 _____	IOC 1 CA-11 __CA__ OUT EIOP 2 33 _____
IOC 1 CA-3 __CA__ IN EIOP 0 36 _____	IOC 1 CA-13 __CA__ IN EIOP 2 36 _____
IOC 1 CA-3 __CA__ OUT EIOP 0 37 _____	IOC 1 CA-13 __CA__ OUT EIOP 2 37 _____
IOC 1 CA-4 __CA__ IN EIOP 1 30 _____	IOC 1 CA-14 __CA__ IN EIOP 3 30 _____
IOC 1 CA-4 __CA__ OUT EIOP 1 31 _____	IOC 1 CA-14 __CA__ OUT EIOP 3 31 _____
IOC 1 CA-6 __CA__ IN EIOP 1 34 _____	IOC 1 CA-16 __CA__ IN EIOP 3 34 _____
IOC 1 CA-6 __CA__ OUT EIOP 1 35 _____	IOC 1 CA-16 __CA__ OUT EIOP 3 35 _____

I/O Cluster 2 Channel Adapters
YC

IOC 2 CA-1 __CA__ IN EIOP 0 32 _____	IOC 2 CA-11 __CA__ IN EIOP 2 32 _____
IOC 2 CA-1 __CA__ OUT EIOP 0 33 _____	IOC 2 CA-11 __CA__ OUT EIOP 2 33 _____
IOC 2 CA-3 __CA__ IN EIOP 0 36 _____	IOC 2 CA-13 __CA__ IN EIOP 2 36 _____
IOC 2 CA-3 __CA__ OUT EIOP 0 37 _____	IOC 2 CA-13 __CA__ OUT EIOP 2 37 _____
IOC 2 CA-4 __CA__ IN EIOP 1 30 _____	IOC 2 CA-14 __CA__ IN EIOP 3 30 _____
IOC 2 CA-4 __CA__ OUT EIOP 1 31 _____	IOC 2 CA-14 __CA__ OUT EIOP 3 31 _____
IOC 2 CA-6 __CA__ IN EIOP 1 34 _____	IOC 2 CA-16 __CA__ IN EIOP 3 34 _____
IOC 2 CA-6 __CA__ OUT EIOP 1 35 _____	IOC 2 CA-16 __CA__ OUT EIOP 3 35 _____

YD

IOS-E TO ZIF IN HISP 0–23	IOC 0 CA-15 __CA__ 200MB (P3) _____
IOS-E TO ZIF IN HISP 24–47	IOC 0 CA-15 __CA__ 200MB (P2) _____
IOS-E TO ZIF IN HISP 48–71	
IOS-E TO ZIF OUT HISP 0–23	
IOS-E TO ZIF OUT HISP 24–47	
IOS-E TO ZIF OUT HISP 48–71	
IOS-E TO ZIF IN HISP CONTROL	
IOS-E TO ZIF OUT HISP CONTROL	IOS-E TO ZIF HISP ADDRESS EXPANSION

YE

IOS-E TO ZIF IN HISP 0–23	PROGRAMMABLE INTERRUPT
IOS-E TO ZIF IN HISP 24–47	
IOS-E TO ZIF IN HISP 48–71	
IOS-E TO ZIF OUT HISP 0–23	
IOS-E TO ZIF OUT HISP 24–47	
IOS-E TO ZIF OUT HISP 48–71	
IOS-E TO ZIF IN HISP CONTROL	
IOS-E TO ZIF OUT HISP CONTROL	IOS-E TO ZIF HISP ADDRESS EXPANSION

YF

SSD ELOG	SSD MAINTENANCE LOSP IN
	SSD MAINTENANCE LOSP OUT
WIN 1 CHANNEL 24 IN	
WIN 1 CHANNEL 25 OUT	
WIN 0 CHANNEL 22 IN	
WIN 0 CHANNEL 23 OUT	
	WARNING & CONTROL SYSTEM IN/OUT

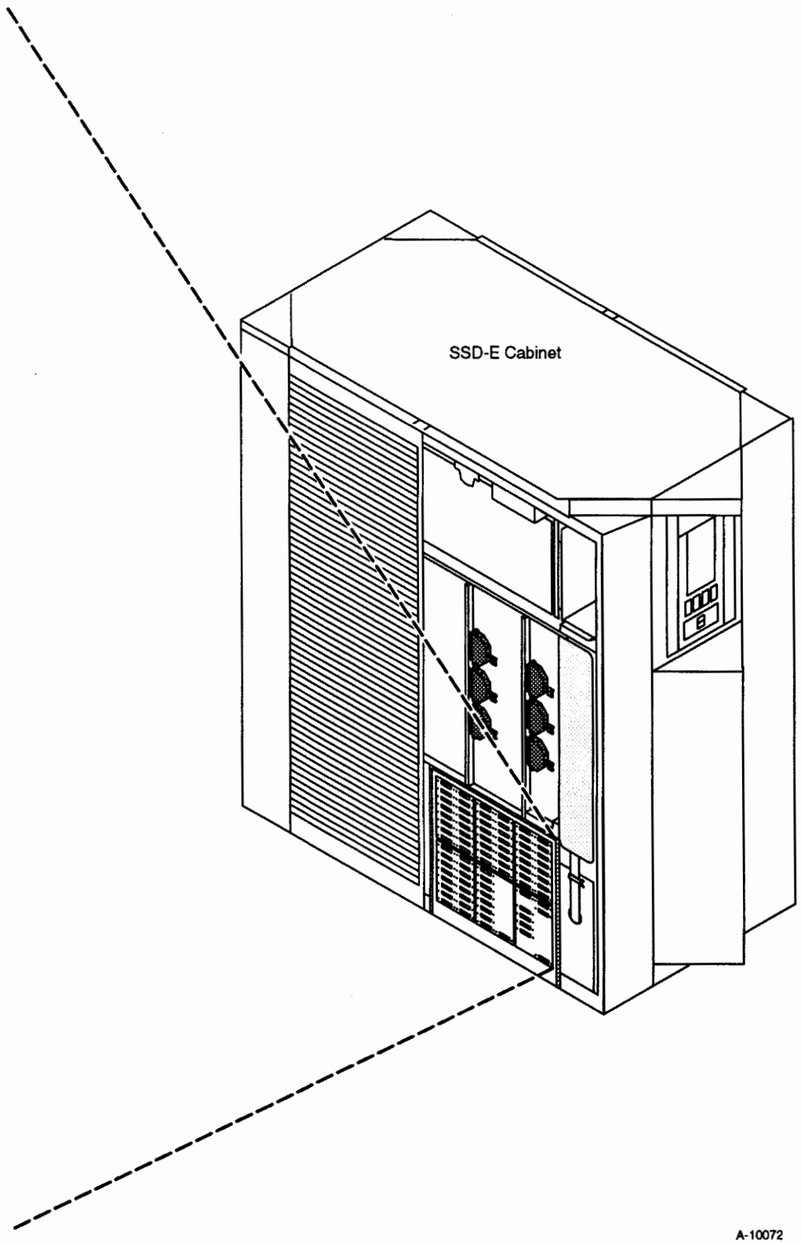


Figure 3-52. SSD-E CINCH Connector Worksheet for Y Side of Cabinet (Serial Numbers 817 through 821)

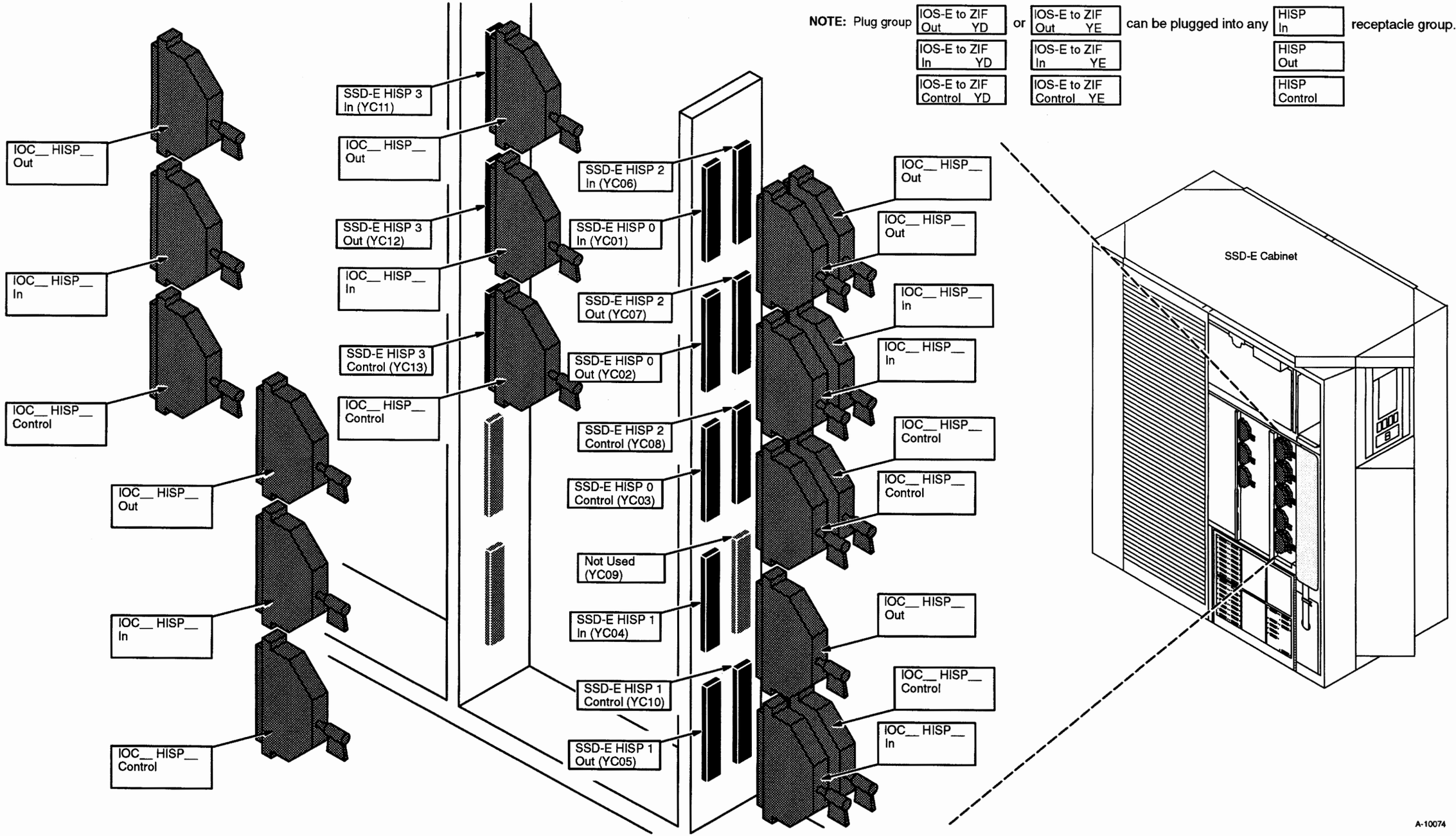


Figure 3-53. SSD-E ZIF Connector Worksheet for Y Side of Cabinet (Serial Numbers 815 through 899)

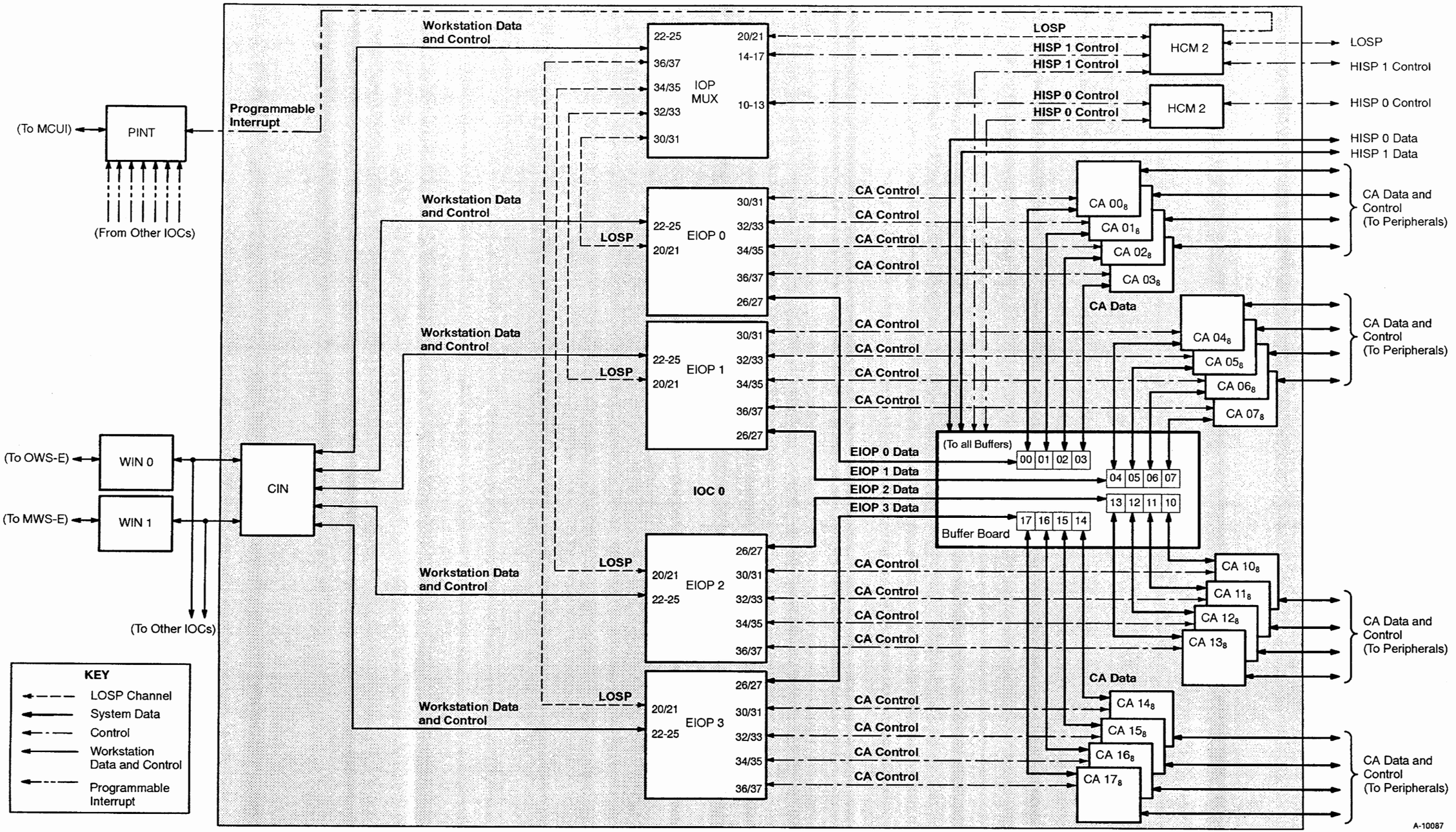


Figure 5-3. IOS-E Control and Data

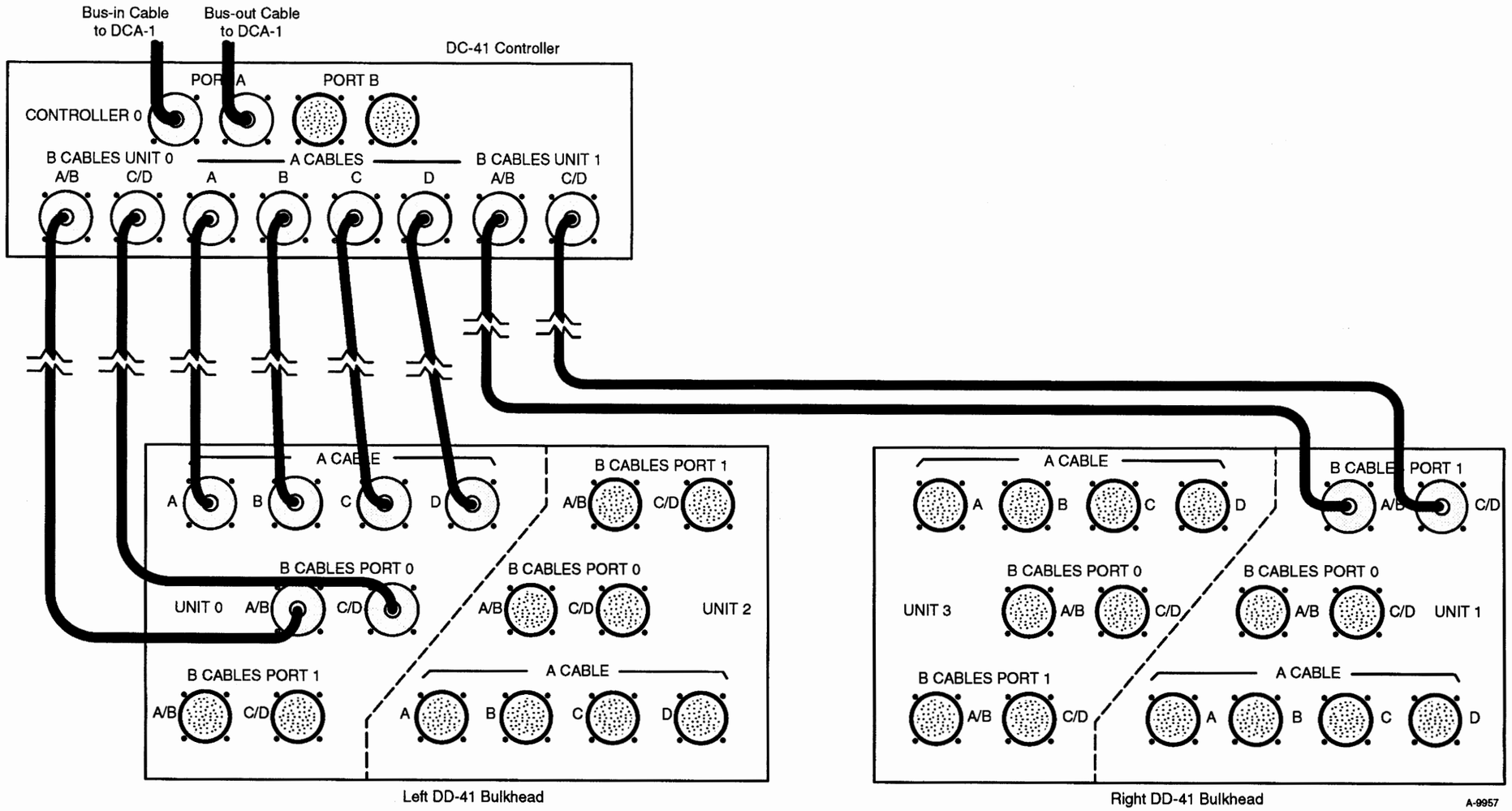


Figure 8-34. DD-41 Daisy Chain Configuration Cabling

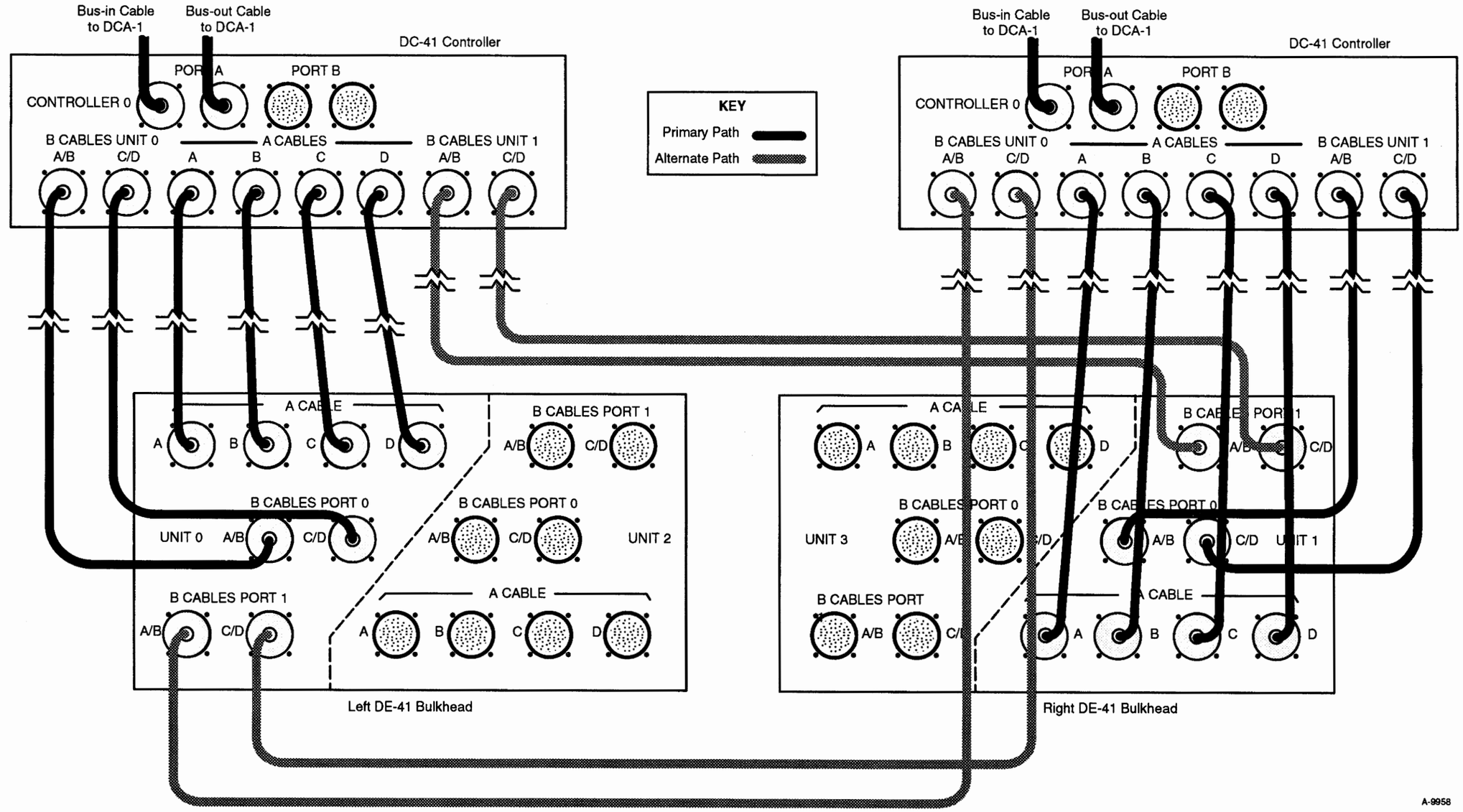


Figure 8-35. Alternate-path Configuration Cabling