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Cray Research, Inc.

CRAY Y-MP EL Computer Systems Hardware Troubleshooting and Maintenance Manual

CMM-xxxx-PR2

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REVISION	DESCRIPTION
PR1	Preliminary manual for classroom use only
PR2	Preliminary manual for classroom use only

PREFACE

To be provided.

CONTENTS

1 SYSTEM OVERVIEW

The CRAY Y-MP EL computer system is a completely self-contained system. This means that the central processing unit (CPU), input/output subsystem (IOS), and all peripherals are contained in one easily moved cabinet. The cabinet can be moved easily to most general office environments equipped with a 200- to 250-Vac power source and be operational.

One to four CPU boards can be installed in the CRAY Y-MP EL system cabinet. This cabinet also holds four memory boards, an IOS contained within a VMEbus-based assembly, and the optional peripherals requested by the customer. Another area in the frame contains the small computer system interface (SCSI) subsystem. The SCSI subsystem consists of a cartridge-type streaming tape drive, a 780-Mbyte hard disk drive, and an optional 8-mm helical scan tape drive. This SCSI subsystem is analogous to the expander chassis that formed part of the CRAY X-MP computer system. The SCSI is used to install any new releases of software as they become available. It also has the capability of performing data transfers and being the system backup and boot device.

The primary frame is constructed so that another standard frame can be bolted to the primary frame to expand the system. It is possible to connect as many as three secondary frames to the primary frame; thus, the CRAY Y-MP EL system can contain as many as 16 IOSs and additional peripheral devices.

Figure 1-1 and Figure 1-2 can be used to locate the four cabinets that can be configured and the various subassemblies within the CRAY Y-MP EL system.

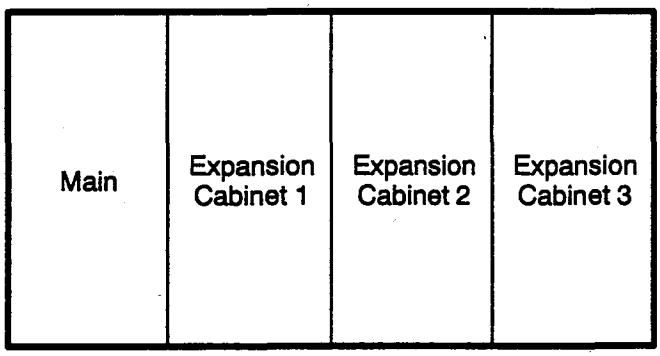


Figure 1-1. Left Side View (Maximum configuration)

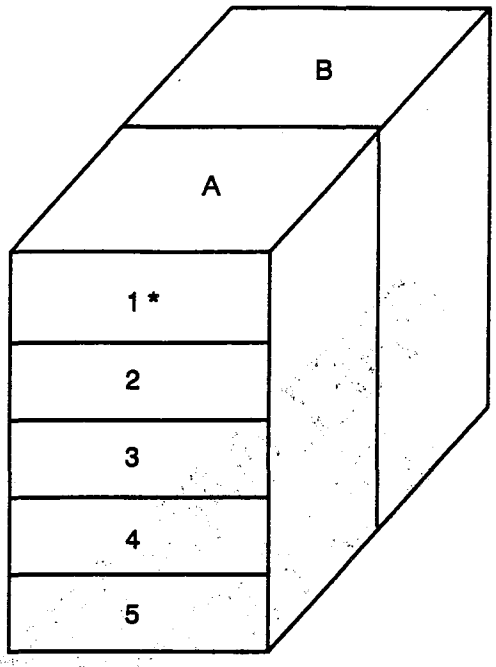


Figure 1-2. Front-Right View, Cabinet A

All of the frames forming the CRAY Y-MP EL system are air cooled by integrated fans at both the top and bottom of the frame. This form of cooling is referred to as vertical cooling.

The peripheral devices available on the CRAY Y-MP EL system and their characteristics are listed below.

- DS-3 Disk Storage System
  - 5.25-inch format Winchester disk drive
  - Holds 1.5 Gbytes of unformatted data per drive
  - Transfer rates are between 1 and 1.75 Mbytes/s
  - Average seek time is 15 milliseconds
  - Mean time between failures (MTBF) is estimated at 150,000 hours
  - DC-3 controller controls up to four enhanced serial drive interface (ESDI) disk drives
  - Each disk controller provides error correction code (ECC) and media defect management

- DD-3 low performance disk unit
  - 1.5 Gbytes; 5.25 inch ESDI drive
  - 2.75-Mbyte/s transfer rate
  - Packaged ten drives per drawer with a shared power supply
- DS-4 disk storage system
  - DD-4 medium performance disk unit
  - 3.0 Gbyte 8-inch two-head IPI dual port disk drives
  - 9.34 Mbytes/s transfer rate
  - Packaged two disk drives per drawer with one per drive
  - DC-4 controller controls intelligent peripheral interface (IPI-2) containing two IPI channels; each channel can handle two DD-4 drives
- DAS-2 disk array subsystem
  - Intelligent disk array controller
  - Bank of eight 1.5-Gbyte ESDIs for storage plus one for parity and one spare
  - Hardware striping used to distribute data evenly across all drives
  - Sustained transfer rate of 13 Mbytes/s
  - Has 12-Gbyte unformatted capacity
- Tape units
- 9-track tape drive subsystem
  - One TCU-2 tape controller unit
  - One TD-2800 bpi (NRZI), 1600 bpi (PE), 6250 bpi (GCR) 9-track low profile tape drive, 125 ips
- Cartridge tape drive (EXABYTE) models
  - EX-1 2.3 Gbyte, EXB-200 246K/s 8-mm tape drive
  - EX-2 5.0 Gbyte, EXB-850 500K/s 8-mm tape drive

- TD-3 .5-inch cartridge tape drive; 3480-type tape
- DR-1 removable disk system
  - Dual 5.25-inch disks in easily removable cartridges designed to protect data from damage during transport
- DR-2 removable IOS disk drive
- TD-2 autoloading low profile 9-track tape drive
- TD-3 .5 inch cartridge; 3480-type tape drive

Customers select peripheral devices according to their requirements, some of which are dictated by the system requirements.

System Configurations

Three system configuration examples are offered to fill the specific needs of the customer. In many cases, the configuration defines the peripheral options selected. The three configurations are: remote seismic option, departmental system, and file server system. The characteristics of each of these configurations are listed below.

- Remote seismic system (refer to Figure 1-3).
  - Low overall system cost
  - 9-track tape capability
  - 2 to 4 VMEbus channels
  - Minimum disk space required (10 to 20 Gbytes)
  - Single 19-inch frame
- Departmental supercomputer system (refer to Figure 1-4).
  - Compatible with office environment
  - Compact size
  - Low power consumption
  - Minimal heat dissipation
  - Quiet operation
  - Easy to network
  - 4 to 8 VMEbus channels
  - Customer-specified disk capacity
  - 32 to 64 Gbytes of ESDI disk drive storage
  - Higher performance DAS or IPI drives
  - Tape backup system
  - 1 or 2 19-inch frames

- File server system (refer to Figure 1-5).
  - Computer room environment
  - Significant disk storage space (200 to 400 Gbytes)
  - 8 to 16 VMEbus channels
  - Up to 4 racks per system

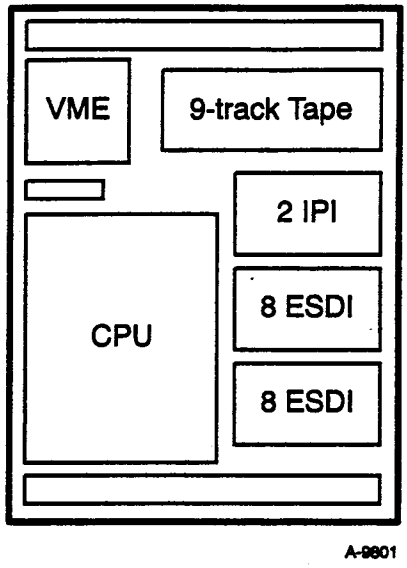


Figure 1-3. Remote Seismic System

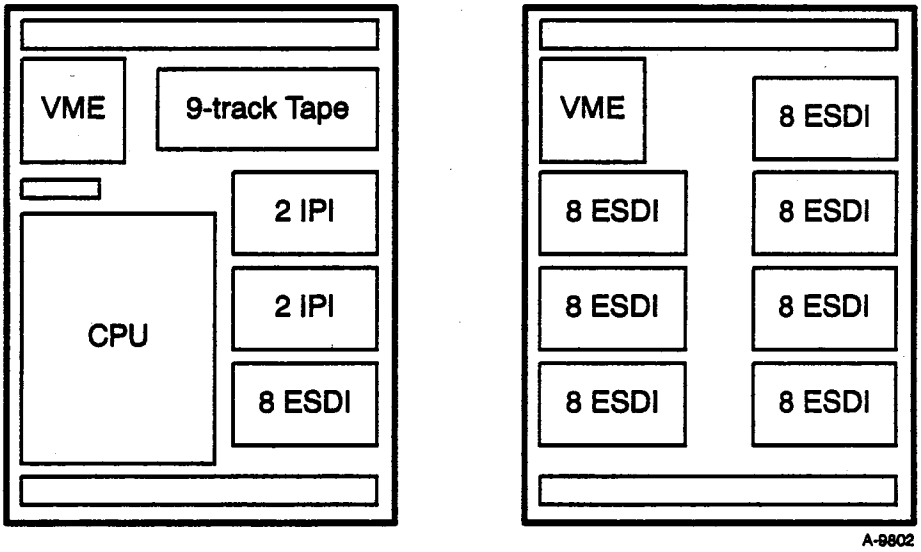


Figure 1-4. Departmental System

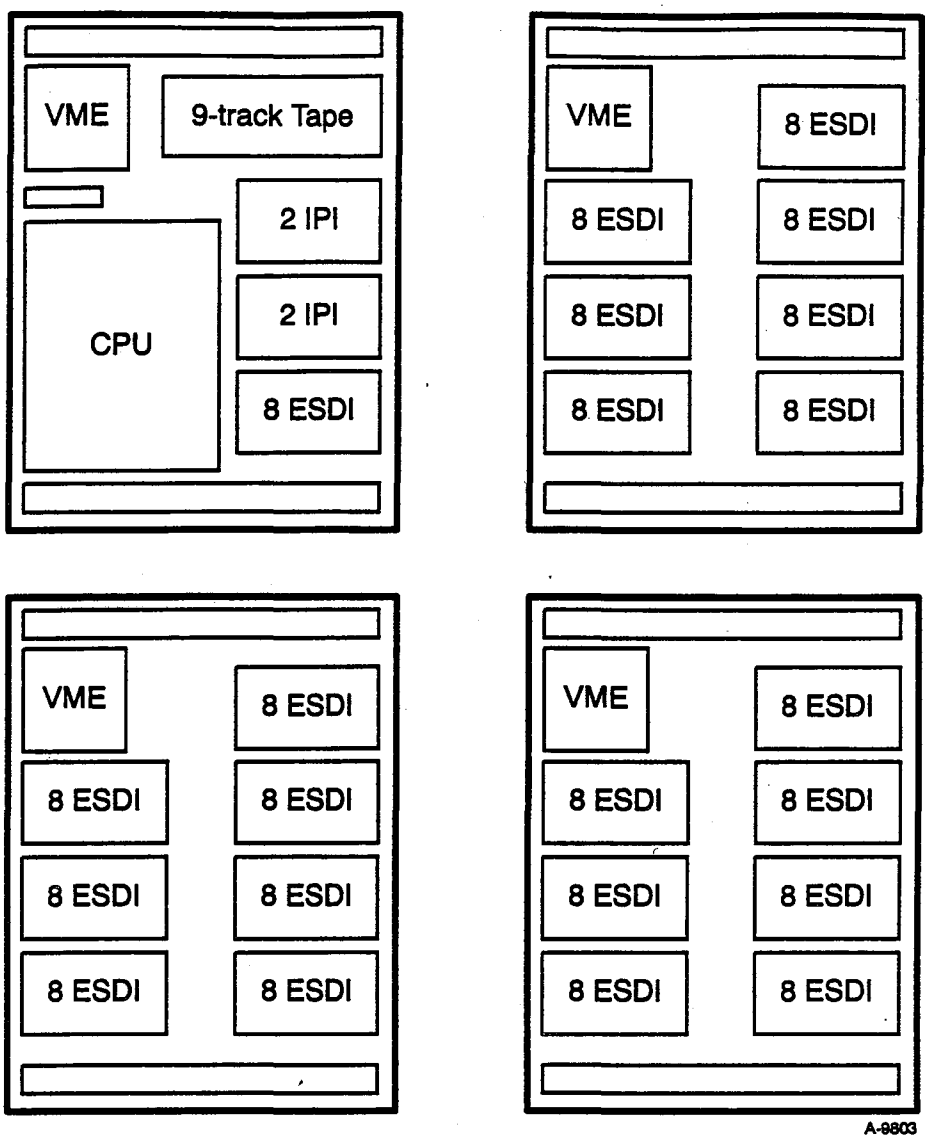


Figure 1-5. File Server System

CPU Overview

The CPU in the CRAY Y-MP EL computer system is constructed on a single 16 x 22 inch printed circuit (PC) board. This PC board contains all of the logic associated with the CRAY Y-MP EL system CPU. Very large scale integration (VLSI) solid-state technology enables a relatively small PC board to contain an entire CPU.

The VLSI chips used in the CPU are application-specific integrated circuits (ASICs). They are constructed using complementary metal oxide semiconductors (CMOS). The ASICs are available in two package sizes; one has 299 pins and one has 223 pins. The internal construction

of the ASIC forms 100,000 undefined gates. This massive number of gates is contained in a 2 x 2 inch or a 1.88 x 1.88 inch package, which consumes an average of 5 watts at + 5 volts.

The CPU contains nine ASIC chip types; there are 23 ASIC chips per CPU. Figure 1-6 shows the chip layout for the CPU of the CRAY Y-MP EL system.

The nine types of ASICs that form the CPU are:

- 1 arbiter (AR) ASIC, used for memory access control and for inter-CPU synchronization.
- 1 address and scalar (AS) ASIC, containing the address registers and address functional units and the scalar registers and scalar functional units.
- 2 channel control (CC) ASICs. Each CC supports two Y1 channels, which are the 40 Mbyte/s channels that connect to the VMEbus sybsystem. The CC option is also used for control support.
- 8 data switch (DS) ASICs, which perform the major data steering between memory, channel, and functional units; they contain the vector registers and B/T registers.
- 4 execution unit (EU) ASICs. Each EU contains all of the vector and floating-point functional units, except the floating-point reciprocal. All of these functional units are fully pipelined, but only one functional unit can be active per EU at any one time. Vector mask (VM) operations can only be performed on EU3.
- 1 memory control (MC) ASIC, which provides memory address generation for a maximum of 512 Mwords of memory. The MC also performs operand and program range error detection.
- 4 memory data (MD) ASICs, which perform single-error correction/double-error detection (SECDED †) and generate check bits. The MDs also support any memory maintenance instructions.
- 1 processor control (PC) ASIC. This device contains eight 32-word instruction buffers(IB), performs shared register (SR) access control, and supports 7 shared register clusters. Also included are the instruction issue control circuits, including the instruction and functional unit scoreboard, and I/O interrupt handling circuits.

† Hamming, R. W. "Error Detection and Correcting Codes." Bell System Technical Journal. 29.2 (1950): 147–160.

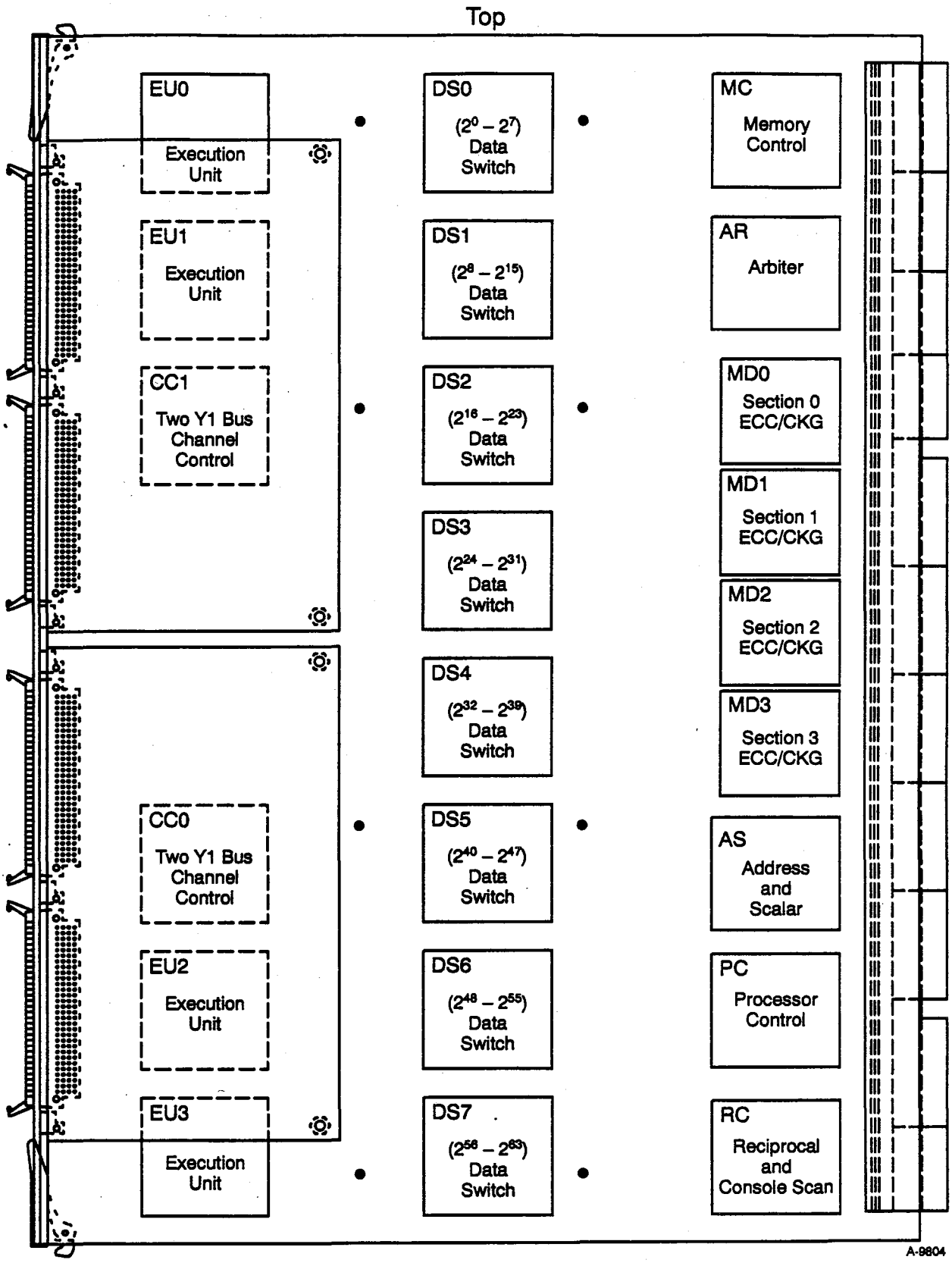


Figure 1-6. CPU/Channel Module

- 1 reciprocal and console (RC) ASIC. The RC performs floating-point reciprocal approximations and contains CONBUS interfaces, scan control and clock control hardware, and console registers.

The interconnection of these CPU components is shown by the block diagram in Figure 1-7.

The CRAY Y-MP EL system is designed to contain up to four independent CPUs. However, the four CPUs can work in conjunction by using shared registers. The CPU runs on a 30 nanosecond (ns) clock. Each CPU connects to the system backplane using 1230 signal pins.

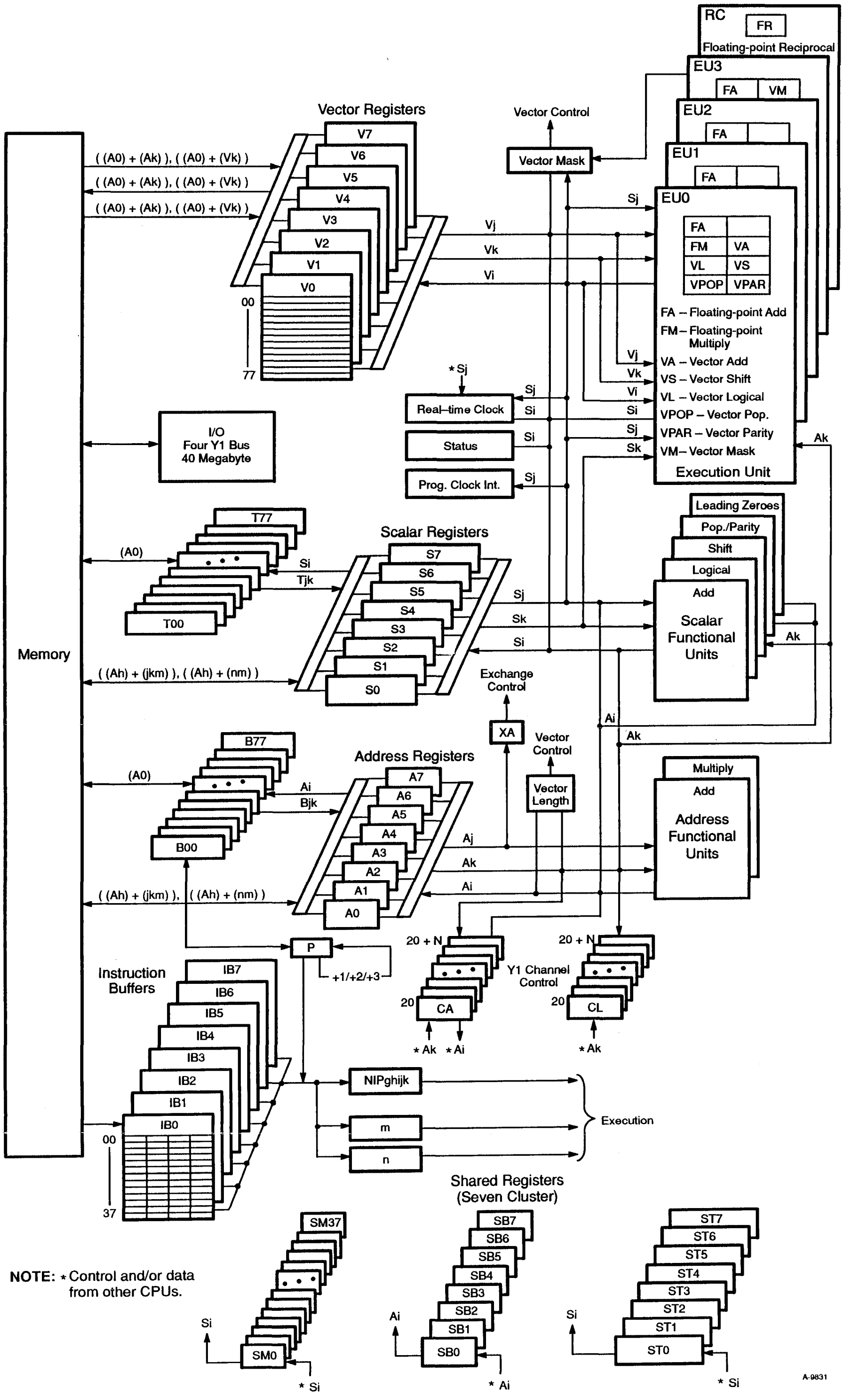


Figure 1-7. CRAY Y-MP EL Block Diagram

Memory Overview

Central memory within the CRAY Y-MP EL system is contained on four PC boards. Each of these boards is 16 x 22 inches (the same size as the CPU board) and is composed of two ASIC types, with a total of nine ASICs per board and a specific number of 1M x 4 dynamic random access memory (DRAM) integrated circuits. The number of DRAMs depends upon the customer's choice of available memory options. The CRAY Y-MP EL system can be ordered with either 64 Mwords or 128 Mwords of central memory. When the 64 Mword option is selected, the memory module contains 16 Mwords of memory supplied by 288 DRAMs. This is a half-populated module. The larger memory, 128 Mwords, consists of 576 DRAMs mounted on each module, creating 32 Mwords per module and 128 Mwords per system. This option uses fully populated modules.

The layout of the memory board is shown in Figure 1-8. The two ASIC types used on the memory board are:

- 2 memory array control (MAC) ASICs support the four memory functions. These ASICs contain an address crossbar which allows access to memory from each of the four CPUs as well as refresh address counters for the local refresh function. The MAC ASIC also contain DRAM address and control circuitry, which provides control to all MADs.

- 7 memory array data (MAD) ASICs. These contain a data crossbar that connects the four CPUs to the 16 banks contained on each memory board. The MAD ASICs handle a portion of the 72-bit memory data word.

The CRAY Y-MP EL system central memory contains a total of 64 banks spread across the four modules. Each module contains 16 banks and is considered a memory section. These 16 banks are separated into lower and upper banks on each board. Thus, a half-populated memory board uses only the lower bank, but still retains the full 16 banks of memory. This means that a fully populated memory module uses both upper and lower banks.

Figure 1-9 shows the chassis locations of the eight boards that form the CRAY Y-MP EL computer system. Note that this represents a top view, with the front of the chassis at the bottom of the diagram.

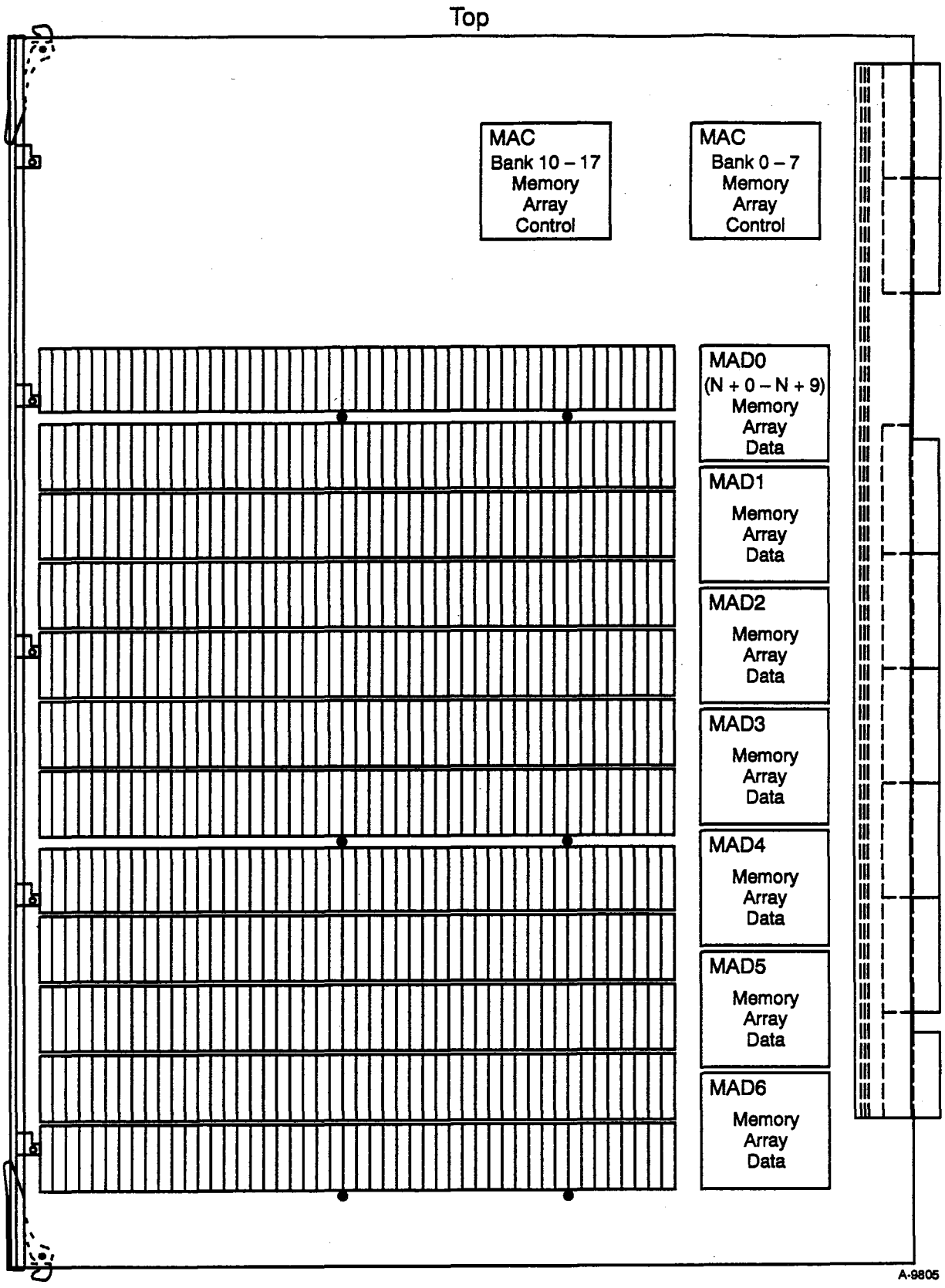


Figure 1-8. Memory Module

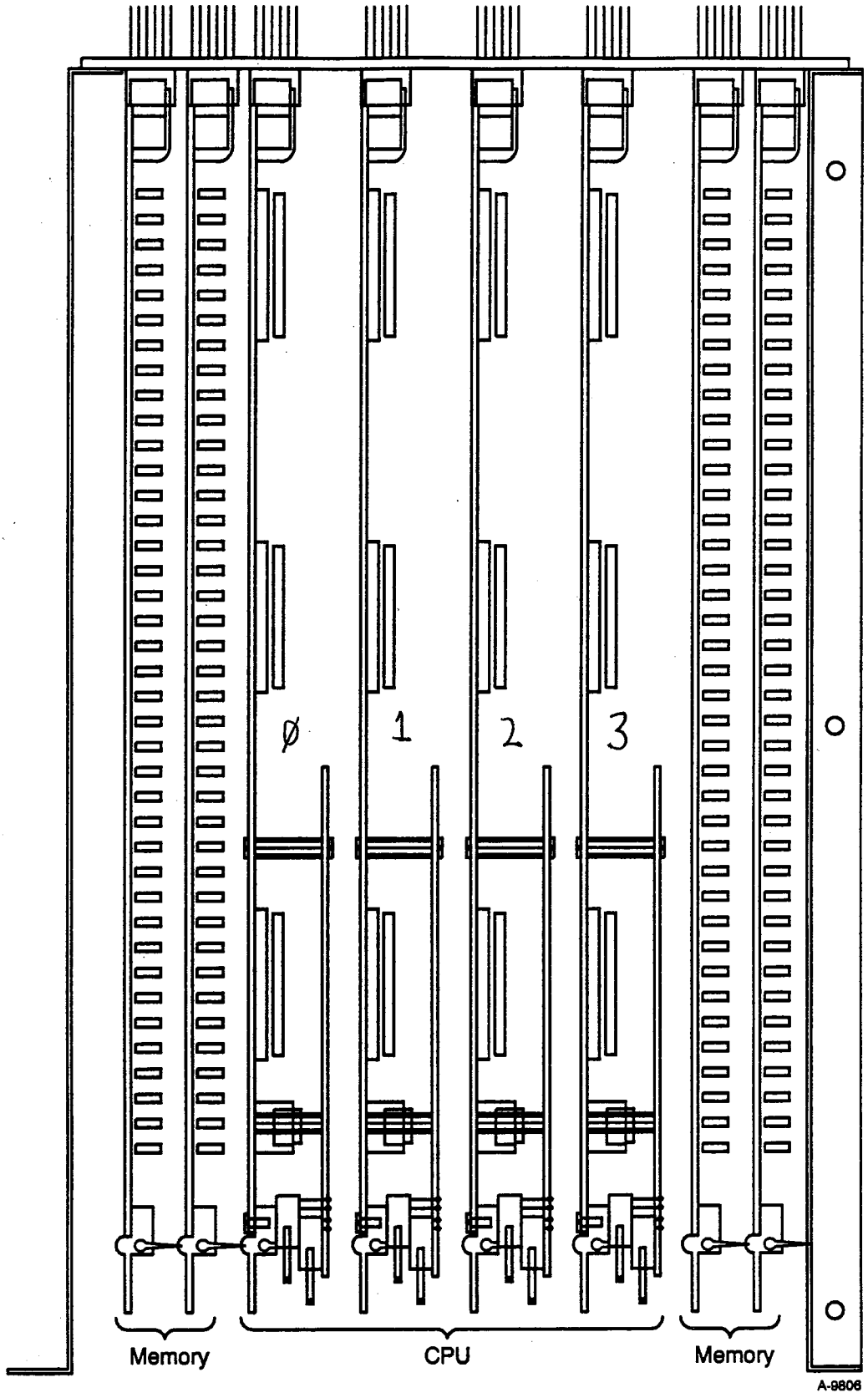


Figure 1-9. Chassis, Top View

Input/Output Subsystem Overview

The IOS for the CRAY Y-MP EL system was selected to provide customers with the maximum choice of peripheral equipment. The IOS is a VME-based system that communicates with the CPU via the Y1 bus (a 40-Mbyte/s channel) using a Cray Research, Inc. (CRI) proprietary module, the input/output buffer board (IOBB). The IOBB is the only CRI proprietary board within the IOS. All other functions within the IOS are performed using vendor-supplied VME boards.

The restrictions of the IOS configuration require use of a 68030-type processor that is capable of processing 32 bits, and as many as eight peripheral controllers to handle data transfers. A possible IOS configuration is represented in Figure 1-10. The types of controllers used are defined by the customer's choice of system peripherals.

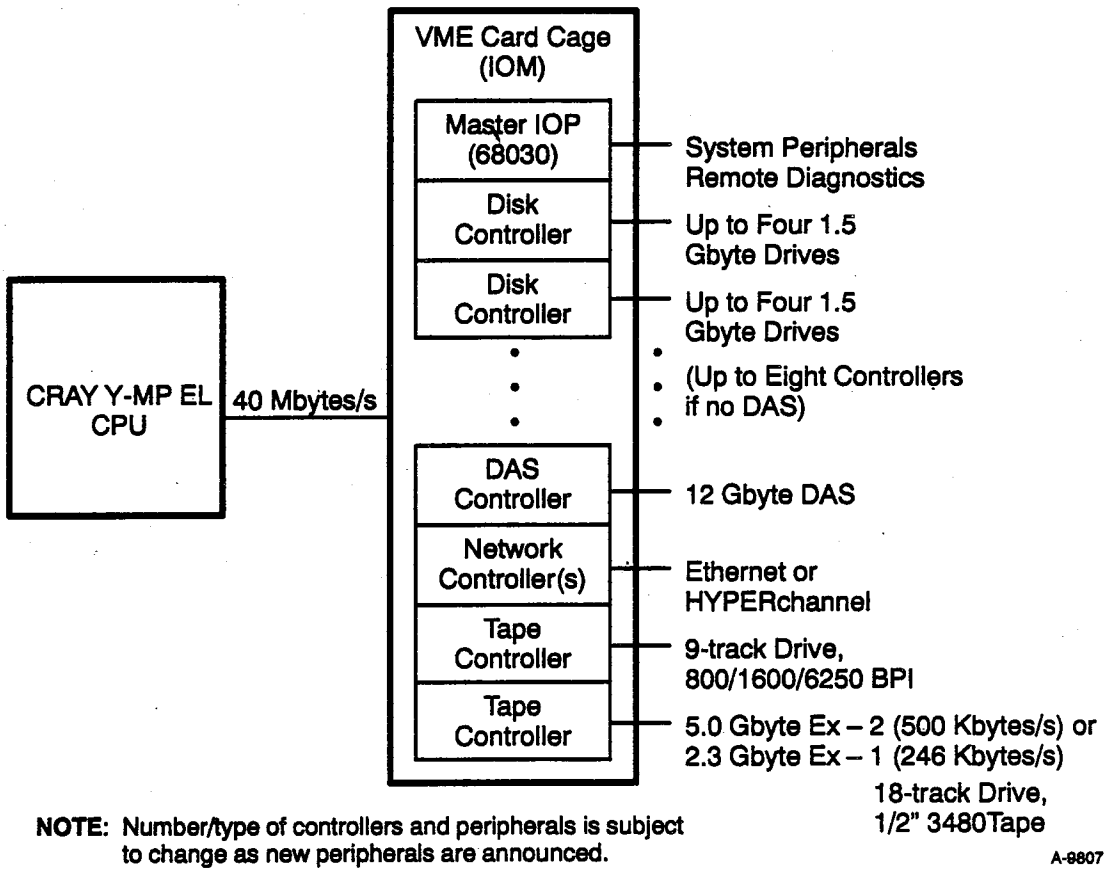


Figure 1-10. IOS Configuration

There are several other considerations pertaining to the VMEbus system. The standard VME mechanical chassis is a 19-inch rack mount chassis that is air cooled, supports standard 64 x 160 mm VME boards, and requires a 750-watt power supply. The backplane is a modular design based on a 10-slot system. The backplane configurations include:

- 10-slot, 10-slot option
- 10-slot, 6-slot, 4-slot option
- 6-slot, 4-slot, 6-slot, 4-slot option

2 MEMORY

The memory portion of the CRAY Y-MP EL computer system consists of four modules. These modules currently are provided in two types: a fully populated module and a half populated module. Both module types are constructed on 16 x 22 x .093 inch printed circuit (PC) boards consisting of 16 circuit layers. These 16 layers are:

- 1 top pad
- 1 bottom pad
- 4 ground (Vss) layers
- 4 power layers: 5-volt application-specific integrated circuit (ASIC); 6-volt dynamic random access memory (DRAM)
- 6 signal layers

The logic portion of a memory PC board comprises two types of ASICs and a group of DRAM chips. There are nine ASICs on each memory board: two memory array control (MAC) ASICs and seven memory array data (MAD) ASICs. The number of DRAM chips on each memory PC board is determined by the memory size selected by the customer. Currently, the CRAY Y-MP EL system can be supplied with either a 64-Mword memory or a 128-Mword memory.

The 64-Mword memory option is a half-populated memory board that contains 288 DRAM chips. Each of these DRAM chips is a 1M x 4 memory chip with a 70 nanosecond (ns) access time. The same DRAM chip is used with the 128-Mword memory, but there are 576 memory chips mounted on the fully populated memory board. Refer to Figure 2-1 for a diagram of a fully populated memory module.

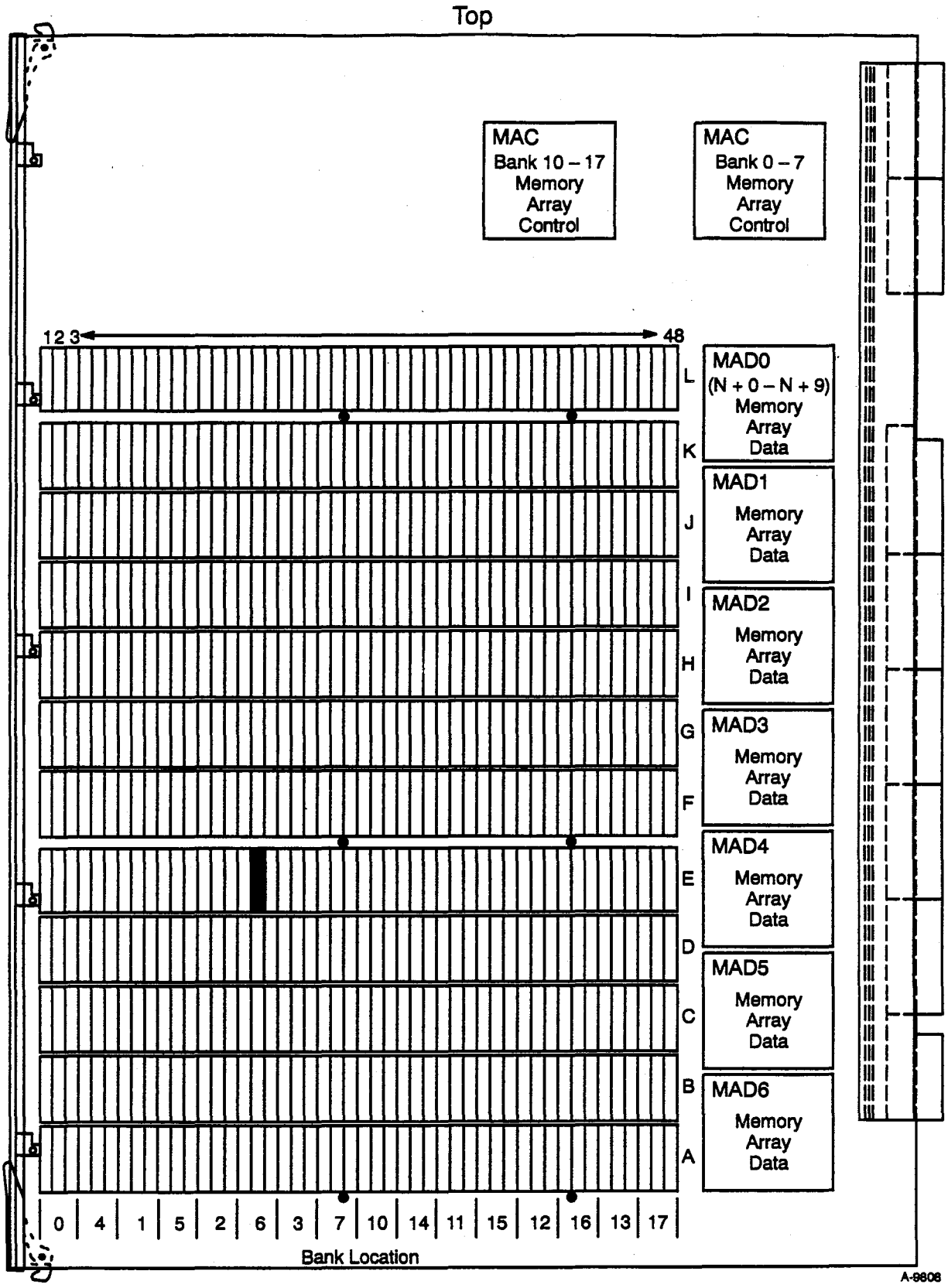


Figure 2-1. Memory Module

Memory is divided into 16-banks for addressing whether the module is half populated or fully populated. The fully populated module contains an upper 16 banks and a lower 16 banks of addressable memory; the half populated module uses only the lower 16 banks. There are 16 banks of memory on each memory module, providing the mainframe with a total of 64 banks of memory. The memory is also separated into sections; each memory module is one section. This arrangement provides the mainframe with four memory sections, each consisting of 16 banks.

The addressing method used by the CRAY Y-MP EL system is a 32-bit address scheme, of which 27 bits (0 through 26) are used. The bits are assigned as shown in Figure 2-2. Bits 2^0 and 2^1 are used to select the appropriate section and bits 2^2 through 2^5 are used for bank selection.

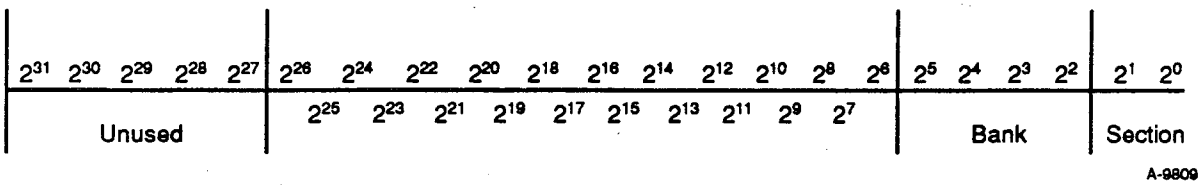


Figure 2-2. Address Bit Assignments

The remainder of the address bits, with one exception, are used to select the actual memory location. The exception is bit 2^{26}, which is used as the upper/lower bank select bit. This bit is only necessary on a fully populated 128-Mword memory module. The internal addressing scheme, represented by bits 2^6 through 2^{25}, uses a row and column scheme. The odd numbered bits are used to count the rows of memory, while the even numbered bits are used to locate the column. It is possible to determine the exact DRAM chip that contains a failing bit by first decoding bits 2^0 and 2^1 to determine which section is in error. This corresponds to a specific memory module. The locations of the memory sections is shown in Figure 2-3, which is a representation of the eight-slot mainframe card cage. All of the memory modules are interchangeable, so swapping the suspected failing module with a good module can help isolate the failure.

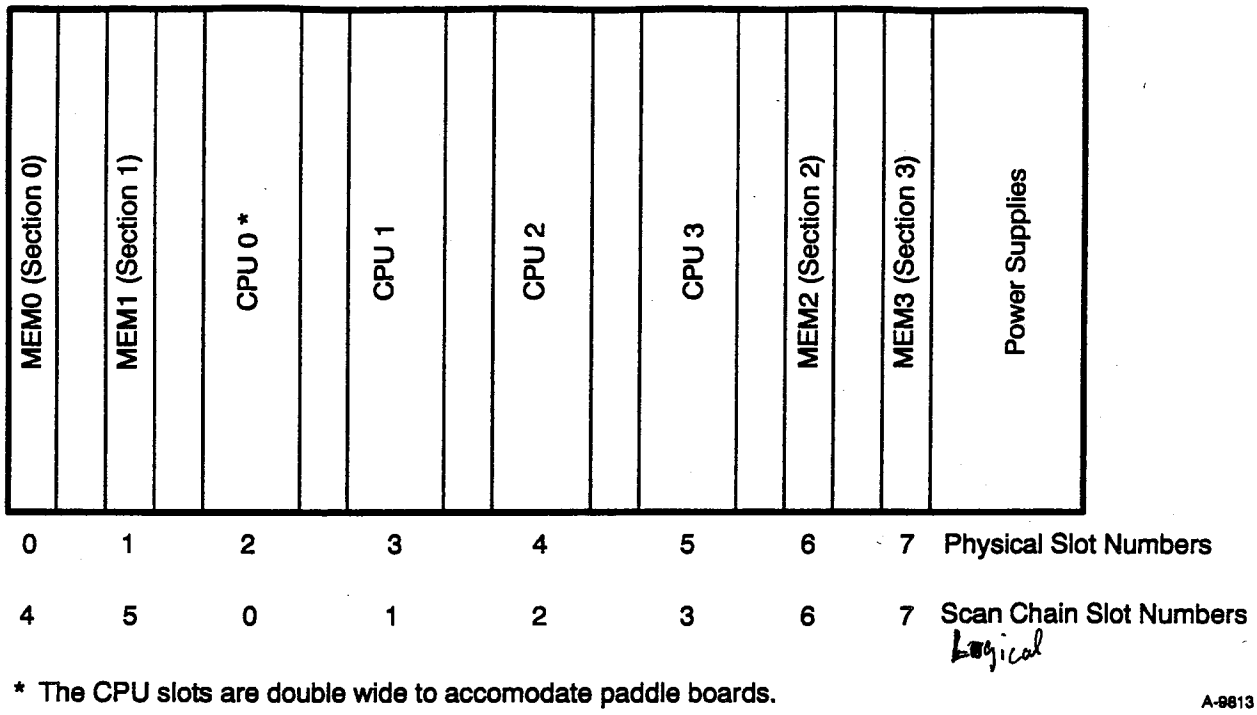


Figure 2-3. Mainframe Chassis, Front View

The next step in the failure isolation procedure is to decode bits 2^2 through 2^5 from the failing address. Once the failing bank has been identified, use Figure 2-1 to identify the location of the failing bank on the PC board. Next, locate the failing data bit in the center section of Table 2-1 as well as the column representing the failing bank. The bank selection will partially depend on the condition of address bit 2^{26}. If 2^{26} is zero, the failing bank is located to the right of center. When 2^{26} is one, the failing bank is located to the left of center. Once the two starting coordinates have been located, draw lines to the left or right from the failing data bit and down under the failing bank. The point at which these two lines intersect represents the board coordinates of the failing chip.

In Figure 2-1, representing the actual PC board, it is possible to locate the chip that requires replacement. In this figure, note that at the right side of the chip locations are labeled positions A through L, moving bottom to top. Along the top, the chips are numbered left to right from 1 to 48. Finally, along the bottom of the chips, the bank locations are indicated. Each bank contains three chips in each of the rows A through L, and the banks are **not** numbered consecutively. Using these locator coordinates, apply the board coordinate determined on Table 2-1 , and the physical location of the failing chip is defined.

As an example, if data bit 2^{43} is reported as failing with an address of 312764132_8, locate the failing DRAM chip.

Table 2-1. DRAM Locator Chart

Banks H A26 = 1																DRAM				Banks L A26 = 0															
17	16	15	14	13	12	11	10	7	6	5	4	3	2	1	0	1M x 4				0	1	2	3	4	5	6	7	10	11	12	13	14	15	16	17
L 46	L 40	L 34	L 28	L 43	L 37	L 31	L 25	L 22	L 16	L 10	L 4	L 19	L 13	L 7	L 1	0	9	23	28	K 1	K 7	K 13	K 19	K 4	K 10	K 16	K 22	K 25	K 31	K 37	K 43	K 28	K 34	K 40	K 46
L 47	L 41	L 35	L 29	L 44	L 38	L 32	L 26	L 23	L 17	L 11	L 5	L 20	L 14	L 8	L 2	1	10	21	30	K 2	K 8	K 14	K 20	K 5	K 11	K 17	K 23	K 26	K 32	K 38	K 44	K 29	K 35	K 41	K 47
L 48	L 42	L 36	L 30	L 45	L 39	L 33	L 27	L 24	L 18	L 12	L 6	L 21	L 15	L 9	L 3	2	11	22	31	K 3	K 9	K 15	K 21	K 6	K 12	K 18	K 24	K 27	K 33	K 39	K 45	K 30	K 36	K 42	K 48
J 46	J 40	J 34	J 28	J 43	J 37	J 31	J 25	J 22	J 16	J 7	J 4	J 19	J 13	J 7	J 1	3	8	20	29	I 1	I 7	I 13	I 19	I 4	I 10	I 16	I 22	I 25	I 31	I 37	I 43	I 28	I 34	I 40	I 46
J 47	J 41	J 35	J 29	J 44	J 38	J 32	J 26	J 23	J 17	J 8	J 5	J 20	J 14	J 8	J 2	4	13	19	24	I 2	I 8	I 14	I 20	I 5	I 11	I 17	I 23	I 26	I 32	I 38	I 44	I 29	I 35	I 41	I 47
J 48	J 42	J 36	J 30	J 45	J 39	J 33	J 27	J 24	J 18	J 9	J 6	J 21	J 15	J 9	J 3	5	14	17	26	I 3	I 9	I 15	I 21	I 6	I 12	I 18	I 24	I 27	I 33	I 39	I 45	I 30	I 36	I 42	I 48
H 46	H 40	H 34	H 28	H 43	H 37	H 31	H 25	H 22	H 16	H 10	H 4	H 19	H 13	H 7	H 1	6	15	18	27	G 1	G 7	G 13	G 19	G 4	G 10	G 16	G 22	G 25	G 31	G 37	G 43	G 28	G 34	G 40	G 46
H 47	H 41	H 35	H 29	H 44	H 38	H 32	H 26	H 23	H 17	H 11	H 5	H 20	H 14	H 8	H 2	7	12	16	25	G 2	G 8	G 14	G 20	G 5	G 11	G 17	G 23	G 26	G 32	G 38	G 44	G 29	G 35	G 41	G 47
H 48	H 42	H 36	H 30	H 45	H 39	H 33	H 27	H 24	H 18	H 12	H 6	H 21	H 15	H 9	H 3	32	41	55	60	G 3	G 9	G 15	G 21	G 6	G 12	G 18	G 24	G 27	G 33	G 39	G 45	G 30	G 36	G 42	G 48
F 46	F 40	F 34	F 28	F 43	F 37	F 31	F 25	F 22	F 16	F 10	F 4	F 19	F 13	F 7	F 1	33	42	53	62	E 1	E 7	E 13	E 19	E 4	E 10	E 16	E 22	E 25	E 31	E 37	E 43	E 28	E 34	E 40	E 46
F 47	F 41	F 35	F 29	F 44	F 38	F 32	F 26	F 23	F 17	F 11	F 5	F 20	F 14	F 8	F 2	34	43	54	63	E 2	E 8	E 14	E 20	E 5	E 11	E 17	E 23	E 26	E 32	E 38	E 44	E 29	E 35	E 41	E 47
F 48	F 42	F 36	F 30	F 45	F 39	F 33	F 27	F 24	F 18	F 12	F 6	F 21	F 15	F 9	F 3	35	40	52	61	E 3	E 9	E 15	E 21	E 6	E 12	E 18	E 24	E 27	E 33	E 39	E 45	E 30	E 36	E 42	E 48
D 46	D 40	D 34	D 28	D 43	D 37	D 31	D 25	D 22	D 16	D 10	D 4	D 19	D 13	D 7	D 1	36	45	51	56	C 1	C 7	C 13	C 19	C 4	C 10	C 16	C 22	C 25	C 31	C 37	C 43	C 28	C 34	C 40	C 46
D 47	D 41	D 35	D 29	D 44	D 38	D 32	D 26	D 23	D 17	D 11	D 5	D 20	D 14	D 8	D 2	37	46	49	58	C 2	C 8	C 14	C 20	C 5	C 11	C 17	C 23	C 26	C 32	C 38	C 44	C 29	C 35	C 41	C 47
D 48	D 42	D 36	D 30	D 45	D 39	D 33	D 27	D 24	D 18	D 12	D 6	D 21	D 15	D 9	D 3	38	47	50	59	C 3	C 9	C 15	C 21	C 6	C 12	C 18	C 24	C 27	C 33	C 39	C 45	C 30	C 36	C 42	C 48
B 46	B 40	B 34	B 28	B 43	B 37	B 31	B 25	B 22	B 16	B 10	B 4	B 19	B 13	B 7	B 1	39	44	48	57	A 1	A 7	A 13	A 19	A 4	A 10	A 16	A 22	A 25	A 31	A 37	A 43	A 28	A 34	A 40	A 46
B 47	B 41	B 35	B 29	B 44	B 38	B 32	B 26	B 23	B 17	B 11	B 5	B 20	B 14	B 8	B 2	64	66	68	70	A 2	A 8	A 14	A 20	A 5	A 11	A 17	A 23	A 26	A 32	A 38	A 44	A 29	A 35	A 41	A 47
B 48	B 42	B 36	B 30	B 45	B 39	B 33	B 27	B 24	B 18	B 12	B 6	B 21	B 15	B 9	B 3	65	67	69	71	A 3	A 9	A 15	A 21	A 6	A 12	A 18	A 24	A 27	A 33	A 39	A 45	A 30	A 36	A 42	A 48

1. Decode the address. Refer to Figure 2-4.

   The reported error is in section 2, lower bank 6.

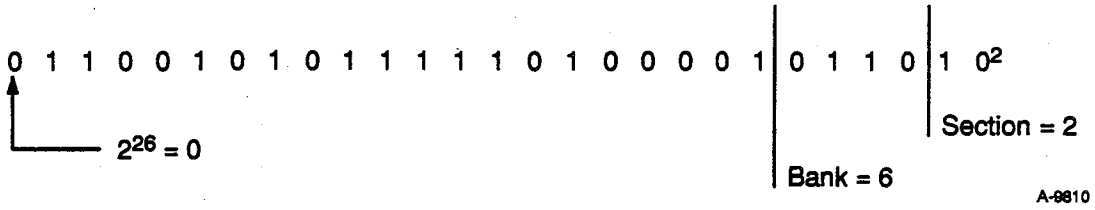


Figure 2-4. Example of Address Decode

2. Locate the failing module. Refer to Figure 2-3; section 2 is in slot 6.

3. Using Table 2-1, locate data bit 2^{43} in the center section and lower bank 6 in the top row. Draw lines to the right from bit 2^{43} and down from bank 6. These two lines should intersect at a point labeled E17.

4. Using Figure 2-1, locate point E17. To the right of the DRAM chips, locate row E. From the left end of row E, count to the seventeenth DRAM chip (shaded on the diagram). To check, follow column 17 down and verify that the failing chip is in bank 6.

Because the DRAM chip used in the CRAY Y-MP EL system memory is a 1M x 4 chip, it is expected that a single-bit error will rapidly escalate into a multiple-bit error. For this reason, it is important to repair single-bit errors as soon as possible.

Other specifications pertaining to the DRAM chip are:

- ZIP package .4 x 1.03 inch
- 5 clock period bank access time
- Standby power = 5 milliwatts at 5 volts
- Active power = 550 milliwatts at 5 volts

The rest of the memory PC board is made up of two types of MAC and MAD ASICs. The MAC ASIC chip supports four memory operations:

- Read, a normal DRAM read operation, lasts 5 clock periods.

- Write, a normal DRAM write operation, lasts 5 clock periods.

- Refresh, which uses row address strobe (RAS) to refresh data, lasts 5 clock periods.

- Read/Modify/Write (RMW) is used during an exchange, and uses normal DRAM read operations followed by a normal DRAM write operation to the same address. RMW lasts 10 clock periods.

The refresh control for the DRAM chips is located on the CPU and memory PC boards.

Other functions of the MAC ASIC include:

- Connects any of the four processors to any of the 16 banks through an address crossbar

- Controls both address and control signals

- Holds a refresh address counter

- Controls all of the MAD ASICs

The MAD ASICs perform the following functions:

- Each handles a specific portion of the 72-bit memory data word

- Each contains a data crossbar which connects any of the four processors to any of the 16 banks

The interconnection between the MAD, MAC, and DRAM chips is represented in Figure 2-5. Note that MAC 0 controls operations for banks 0 through 7, and MAC 1 controls banks 10 through 17. The content of the entire data bus is presented to the seven MAD ASICs and each receives its assigned bits. The bits assigned to each MAD ASIC are in no specific order. If a group of 10 or 11 bits of data are reported as failing, it could in fact be a single MAD that is failing. Included in this section are Figure 2-6, the internal block diagram of a MAD ASIC, and Figure 2-7, the internal block diagram of the MAC ASIC, indicate how an ASIC is designed. When an ASIC fails, the failing chip is removed from the PC board, discarded, and replaced by a new ASIC. No internal repairs are possible.

Other important characteristics of CRAY Y-MP EL system memory modules are:

- Each memory module contains 16 Mwords of memory if half populated and 32 Mwords if fully populated

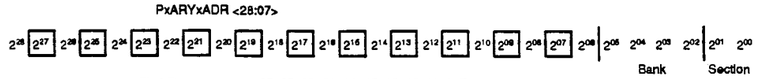
- Operates with a 30 ns clock period

- Air cooled
- Connected to the backplane by two types of connectors:

  120 pins x 7 connectors = 840 pins
  90 pins x 1 connector = 90 pins
  930 pins

- Connected to the individual CPUs using one port per CPU; all ports are read/write ports
- There is no hardware error logger. Single and double bit errors are reported to the operating system by bits being set within the exchange package.
- 270 watts per module = 1080 watts per system
- Voltage = + 6 volts

2^2	2^1	2^0	Command	Action
0	0	x	No Command	None
0	1	0	Read-modify-write	DRAM Read Cycle Followed by Write Cycle to Same Location (Exchange)
0	1	1	Refresh	DRAM Read Cycle with Address from Refresh Address Counter
1	0	0	Write	DRAM Write Cycle
1	0	1	Range Error Write	None
1	1	0	Read	DRAM Read Cycle
1	1	1	Range Error Read	None



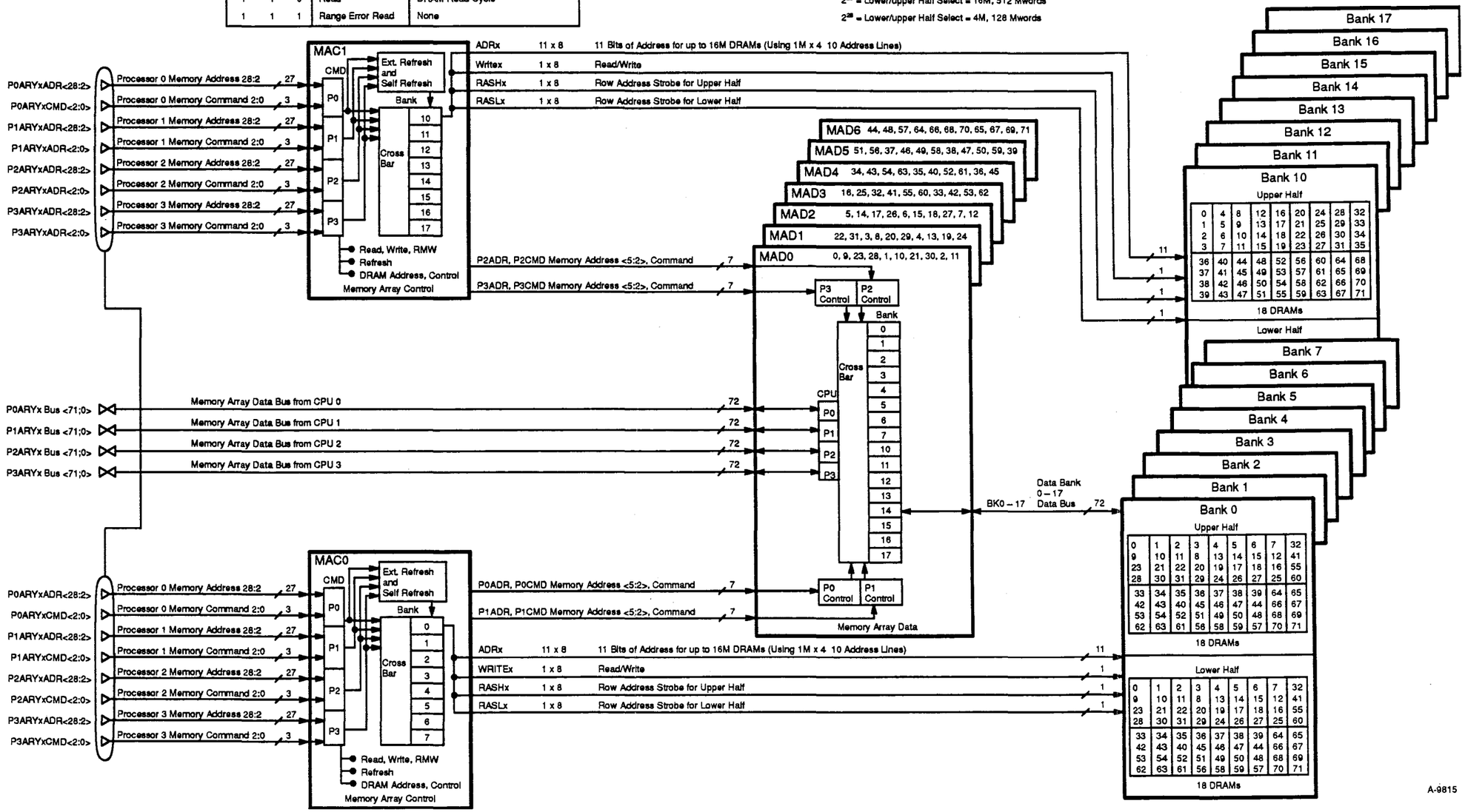


Figure 2-5. Memory Block Diagram

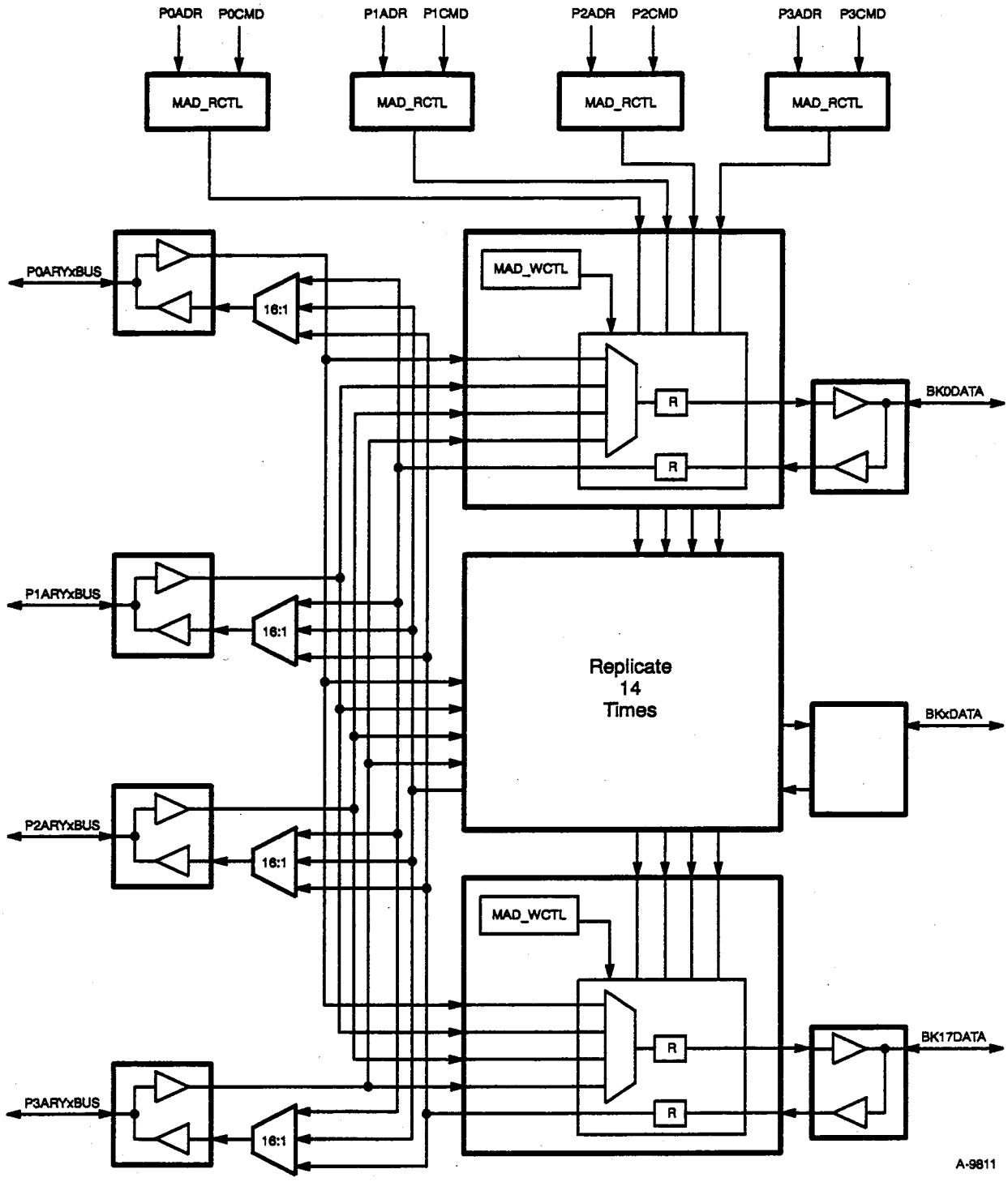


Figure 2-6. Memory Array Data Block Diagram

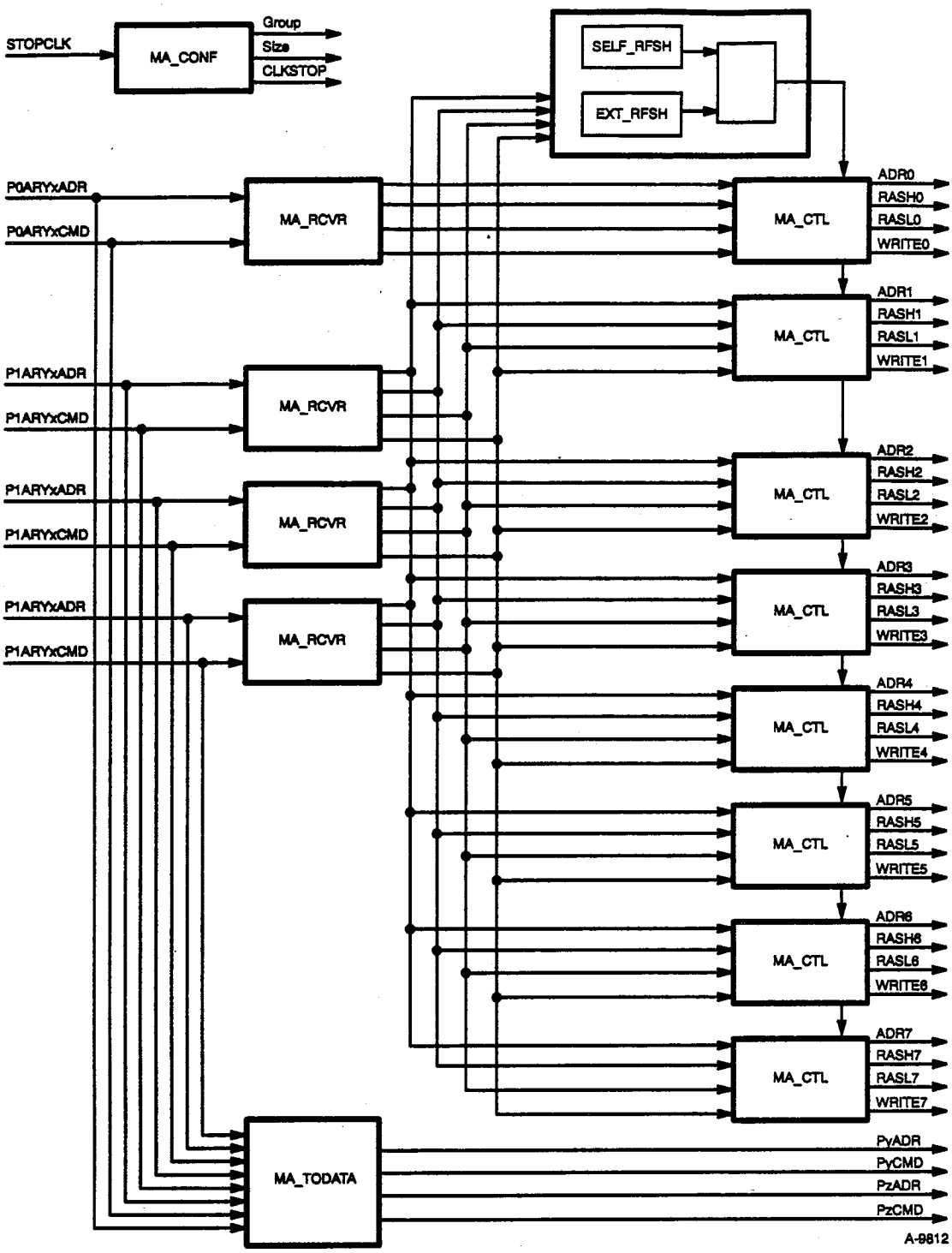


Figure 2-7. Memory Array Control Block Diagram

3 CPU

The CRAY Y-MP EL computer system central processing unit (CPU) is a single printed circuit (PC) board module that contains all the registers and functional units normally used in a computer mainframe. This miniturization is made possible by using very large-scale integration (VLSI) complimentary metal oxide semiconductive (CMOS) application-specific integrated circuits (ASICs). Twenty-three of these ASICs are mounted on a single 16 x 22 x .093 inch PC board.

The CMOS ASICs are provided in two sizes, both 1-micron, two-layer devices with 100,000 undefined gates:

- 2.08 x 2.08 inch chip with 299 pins
- 1.88 x 1.88 inch chip with 233 pins

The power consumed by these chips averages less than 5 watts per ASIC, operating at + 6 volts.

The PC board used to form the CPU module is manufactured of 16 separate layers:

- 1 top pad
- 1 bottom pad
- 4 ground (Vss) layers
- 4 power (Vdd) layers
- 6 signal layers

This module uses an average of 160 watts of power per CPU module. Therefore, the maximum of four CPU modules in a system consumes 640 watts. The CPU, like the entire CRAY Y-MP EL system, is an air cooled device.

The following nine types of ASIC chips reside on the CPU module:

- 1 arbiter (AR) ASIC controls memory access and arbitrates all memory conflicts. It also provides inter-CPU synchronization.

- 1 address and scalar (AS) ASIC contains all of the address registers and the address functional units (FUs), as well as the scalar (S) registers and scalar FUs.

- 2 channel control (CC) ASICs control or support the functions of two Y1 channels. Each of the Y1 channels is capable of 40-Mbyte/s transfers and each connects to a VME subsystem. It is also possible to use two Y1 channels in conjunction to provide one high performance parallel interface (HIPPI) channel for 100-Mbyte/s transfers). One other function of the CC chip is console support.

- 8 data switch (DS) ASICs steer data between memory, the selected channel, and the required FUs.

- 4 execution unit (EU) ASICs contain all of the vector and floating-point FUs, with the exception of the floating-point reciprocal FU. This format provides full pipelining to the EU chips and allows each to work on a different problem independently of the others. The restrictions which pertain to the EU chips are:

  - Only one FU in each EU chip can be operating at any one time

  - Only the EU3 ASIC is capable of executing vector mask (VM) instructions (146 – 147, 175 instructions)

- 1 memory control (MC) ASIC provides address generation, which can support up to 512 Mwords of memory. The other function of the MC chip is to provide both operand and program range error detection.

- 4 memory data (MD) ASICs perform single-error correction, double-error detection (SECDED) functions, including check bit generation on the read and write memory data. The MD chips are also used to support all of the memory maintenance instructions.

- 1 processor control (PC) ASIC contains the CPU instruction buffers. The CRAY Y-MP EL system CPU uses eight instruction buffers, each of which is 32 words wide. Instruction issue control and I/O interrupt handling control also reside on the PC chip. Part of the issue control function is a resource scoreboard, also resident on the PC. Shared register access control is also performed on the PC ASIC; the CRAY Y-MP EL system supports seven shared register clusters.

- 1 reciprocal and control (RC) ASIC contains the floating-point reciprocal FU, the CONBUS interfaces, the scan and clock control, and the control registers.

These units interconnect in the way shown on the the CRAY Y-MP EL system block diagram, Figure 3-1. A more specific diagram showing some of the signal paths can be found in Figure 3-2, a block diagram of the CPU bus. This diagram also shows the internal contents of each of the ASICs located on the CPU module. Another diagram of interest is shown in Figure 3-3, which shows the actual location of the various ASICs.

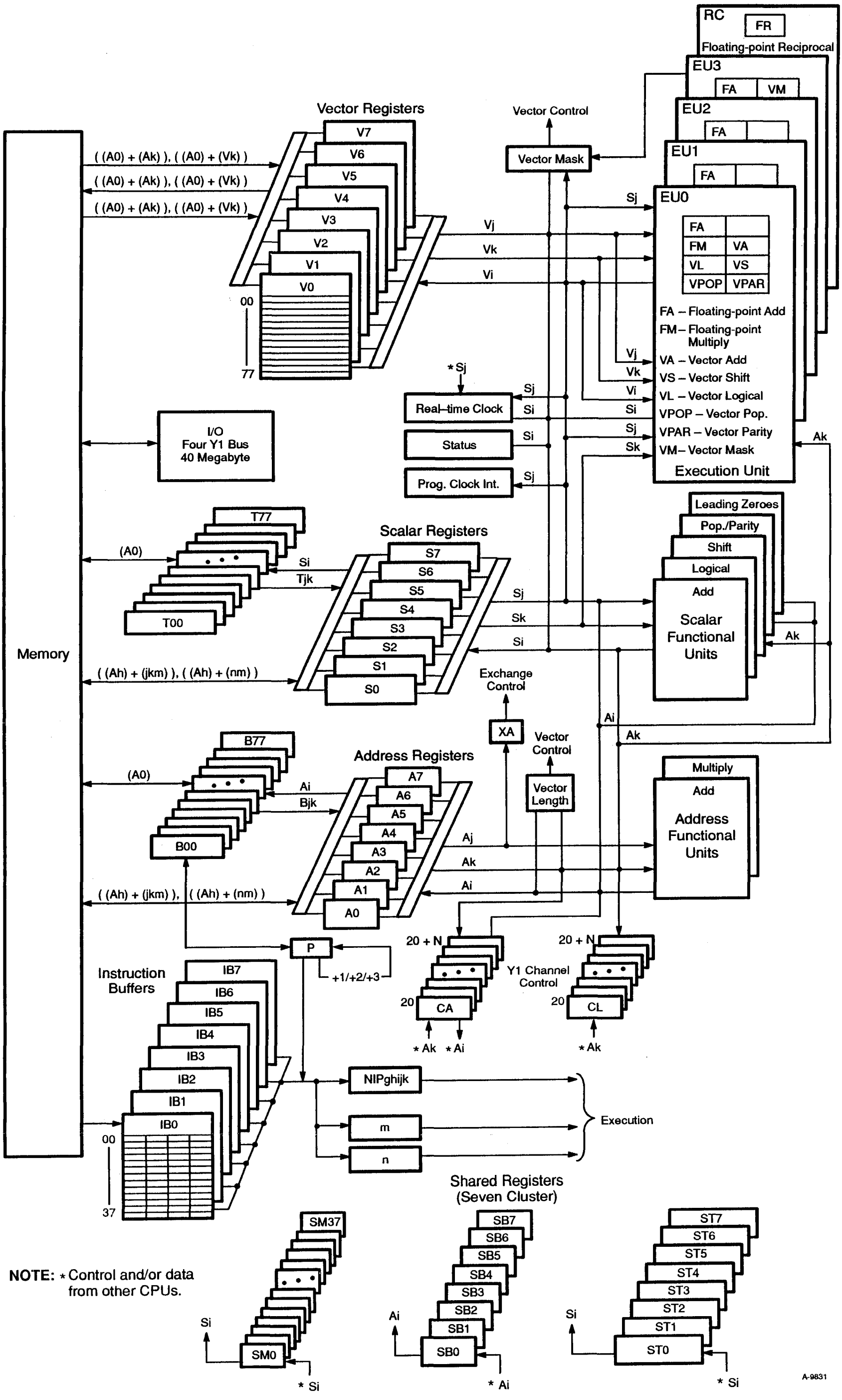


Figure 3-1. CRAY Y-MP EL Block Diagram

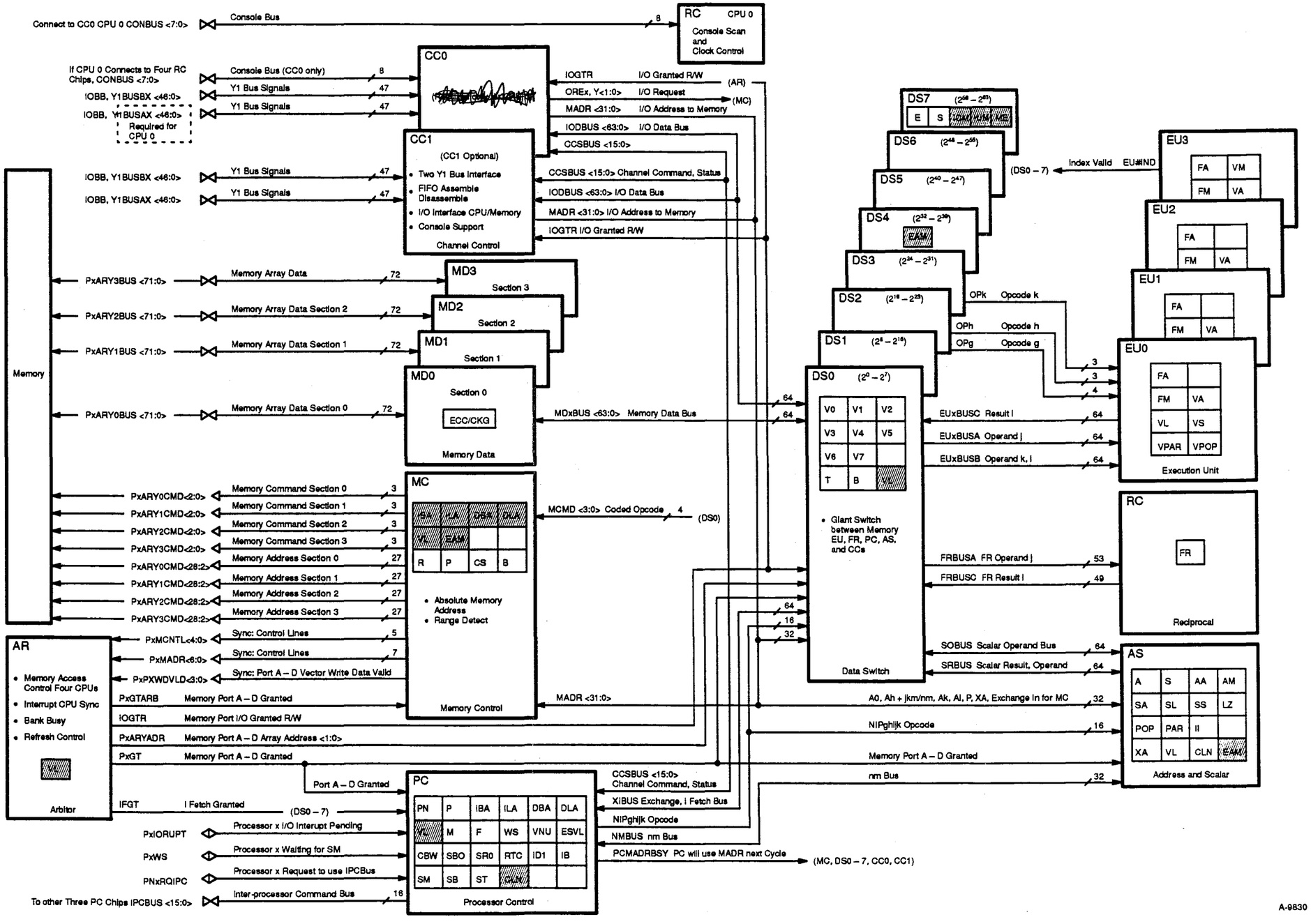


Figure 3-2. CPU Bus Block Diagram

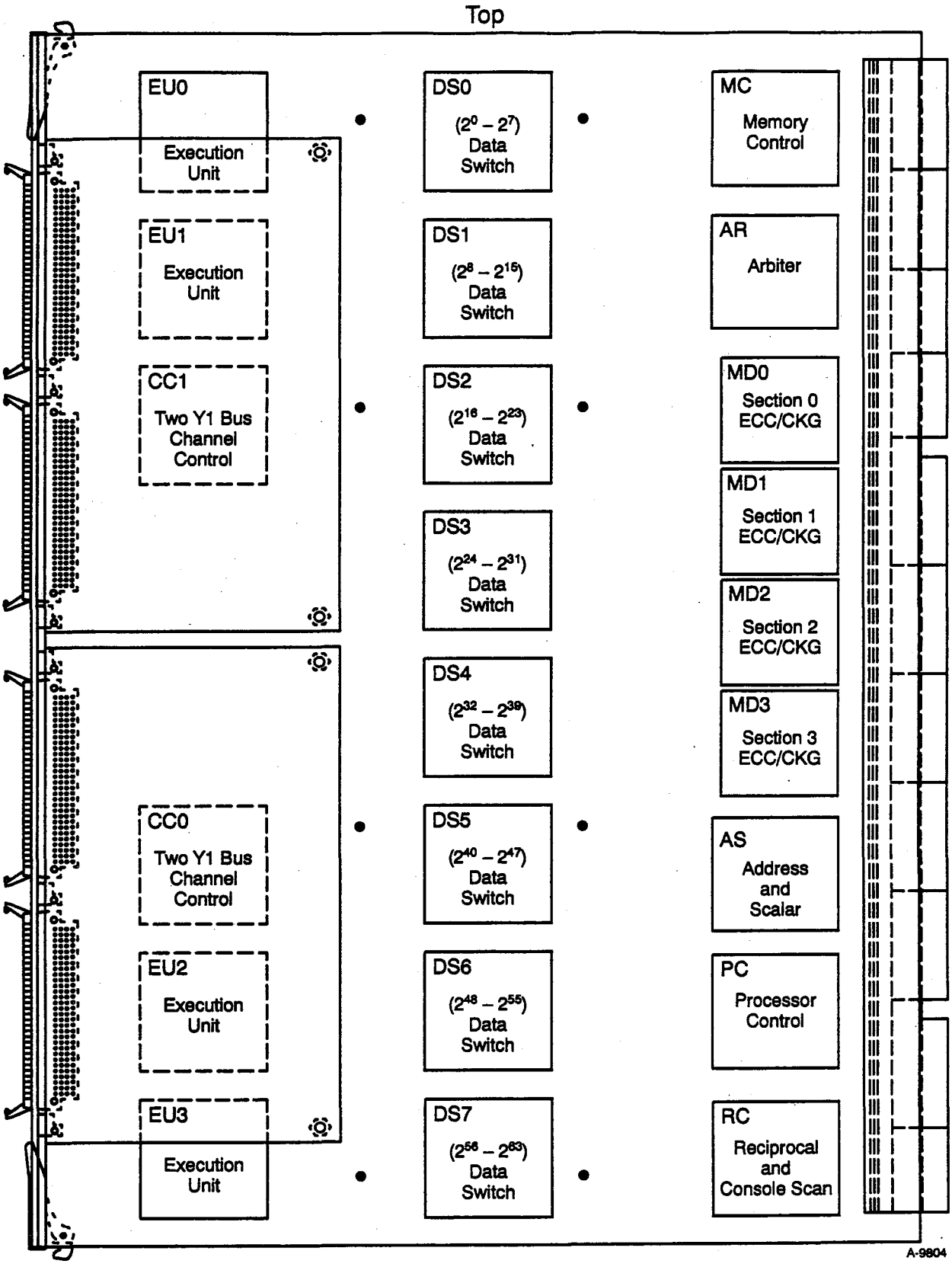


Figure 3-3. CPU/Channel Module

The representative diagram of the exchange package used in the CRAY Y-MP EL system, shown in Figure 3-4, is useful for troubleshooting. The exchange package may contain pertinent information about the state of the CPU at the point of failure. This information can be extracted by comparing the condition of the flag bits, mode bits, and the error word bits with the respective charts shown under the exchange package in Figure 3-4. In some cases, useful information can also be found in the A registers or the S registers, also shown in Figure 3-4. The usefulness of the A or S register information depends on the individual diagnostic used.

The CRAY Y-MP EL system supports one to four CPUs. Each of these CPUs can support up to four VME subsystems. The CPU module is completely self contained and plugs into the mainframe backplane using 11 connectors that provide 1230 signal pins.

When a CPU is indicated as the faulty unit in an incident, the only on-site repair performed is the replacement of the CPU module.

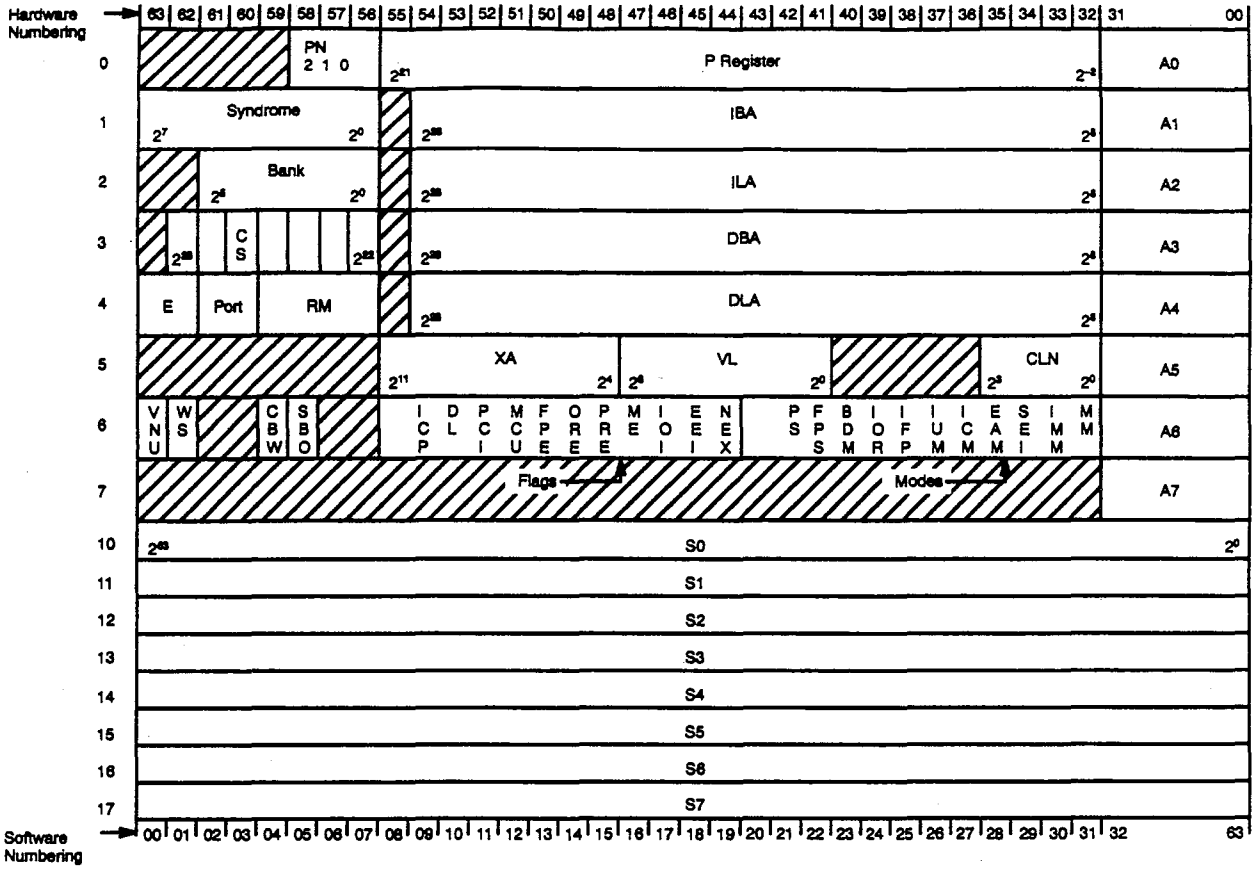
The CPU module connects to the mainframe memory via four 72-bit bidirectional ports. Each of these ports connects to a separate memory section. Each of the CPU modules in a CRAY Y-MP EL system contain a copy of all memory and shared register reservations, to reduce the possibility of conflicts. Each CPU has to check its local request registers, not the request registers of all of the CPUs.

Support for multiple CPUs in the mainframe includes such items as:

- Shared memory
- Shared registers
- Shared I/O channels
- Deadlock detection
- Shared deadstart paths

However, the CRAY Y-MP EL system does not currently support:

- Performance monitors
- High-speed (HISP) channels
- Very high-speed (VHISP) channels



Word 6		Flag Bits	Set Flag	Cause Exchange
55		Reserved		
54	ICP	Interrupt from Internal CPU	MM'	MM'
53	DL	Deadlock Interrupt	MM' and IMM	MM' and IMM
52	PCI	Programmable Clock Interrupt (staged)	MM'	MM'
51	MCU	MCU Interrupt	MM'	MM'
50	FPE	Floating-point Error Interrupt	MM and IMM	MM and IMM
49	ORE	Operand Range Error Interrupt	MM' and IMM	MM' and IMM
48	PRE	Program Range Error Interrupt	MM' and IMM	MM' and IMM
47	ME	Memory Error Interrupt	Always	Always
46	IOI	I/O Interrupt (staged)	MM'	MM'
45	EEI	Error Exit Interrupt	MM' and IMM	Always
44	NEX	Normal Exit Interrupt	MM'	Always

Word 6		Mode Bits
63	VNU	Vectors Not Used
62	WS	Waiting on Semaphores
59	CBW	Concurrent block Write (CRAY Y-MP EL only)
58	SBO	Scalar and block Overlap (CRAY Y-MP EL only)
43		Reserved
42	PS	Program State
41	FPS	Floating-point Status
40	BDM	Bidirectional Memory
39	IOR	Interrupt Operand Range Error
38	IFP	Interrupt Floating-point Error
37	IUM	Interrupt Uncorrectable Memory
36	ICM	Interrupt Correctable Memory
35	EAM	Extended Address Mode (32-bit)
34	SEI	Selected External Interrupt
33	IMM	Interrupt Monitor Mode
32	MM	Monitor Mode

E – Error Word 4		
63	U	Uncorrectable Memory Error
62	C	Correct Memory Error

P- Port				RM Read Mode	Port Usage
66 10	66 10	66 10	66 10	55 98	55 76	
A 00	B 01	C 10	D 11	00	01	Exchange
00	01	10	--	00	10	A or S
--	--	--	D xx	01	01	I/O Single
--	--	--	D xx	01	11	I/O Block
00	01	10	--	10	00	B or T
--	--	--	D xx	10	11	Fetch
00	01	10	--	11	00	Vector Stride
00	01	10	--	11	10	V Gather/Scatter

A-9829

Figure 3-4. Exchange Package

4 INPUT/OUTPUT SUBSYSTEM

The input/output subsection (IOS) of the CRAY Y-MP EL computer system is designed to act as a preprocessor and interface between the mainframe section [central processing unit (CPU) and memory] and the various customer-selected peripheral devices. The purpose of this section is to describe devices incorporated within the IOS as well as their functions.

Basic Architecture

The IOS used in the CRAY Y-MP EL system is a VMEbus-based device. This VME is a modular design, and thus is easily adapted to customer requirements. The IOS is available in three different backplane configurations:

- 10-slot + 10-slot
- 10-slot + 6-slot + 4-slot
- 6-slot + 4-slot + 6-slot + 4-slot

Cray Research, Inc. (CRI) uses a VME backplane that supports the double-height 233 mm (6U) x 160 mm printed circuit (PC) board, which fits into a standard 19-inch rack. The IOS is powered by a 1000-watt power supply and is air cooled.

The CRAY Y-MP EL system can support up to four independent IOSs for each installed CPU. Thus, a fully enhanced system containing four CPUs can support 16 IOSs. Each of the IOSs communicates with its associated CPU via a 40-Mbyte/s channel, designated the Y1 bus.

IOS 0 is required and must reside in the primary cabinet. This primary IOS, designated the multiplex input/output processor (MIOP), consists of:

- Type 68030-processor based processor board
- Local memory
- Control store

The primary IOS also includes the following devices that are connected to the small computer system interface (SCSI):

- Winchester disk drive
- Cartridge tape drive (.25-inch)
- Communications port for the operators console
- Remote diagnostic facility
- Optional helical-scan tape system

Many peripheral products can be connected to an IOS. Some of these are:

- Networks using TCP/IP
  - HYPERchannel
  - Fiber-distributed data interface (FDDI)
  - Ethernet
- Several varieties of disk drives
- Several varieties of tape drives

For a more detailed list of peripherals supported by the IOS, refer to Section 5 of this manual.

Each of these devices must be driven by a VMEbus-compatible device controller. Cray Research recommends and supports several of these controllers, but the customer may provide other controllers. The IOS backplane can contain up to 8 of these peripheral controllers (in the 10-slot configuration). However, each IOS must contain an I/O processor (IOP) board and a CPU channel communications interface board.

The IOP selected for the CRAY Y-MP EL system IOS is a type 68030-based board supplied by Heurikon Corporation. This IOP supports the SCSI, allows I/O computation, and controls IOS-to-CPU communications. Communication between the IOS and CPU takes place via a CRI board called the input/output buffer board (IOBB).

IOBB

The IOBB is used to provide buffer memory for the IOP and a communications interface between the IOS and the CPU. IOS-to-CPU communication takes place in the following manner: the IOP generates interrupts to initiate a CPU request, and the CPU generates interrupts to initiate a peripheral read or write operation or to terminate the CPU request. These interrupts are called I/O task control blocks (IOTCB), of which there are two types: I/O IOTCB and console IOTCB. Both of these types have the same format with minor variations (refer to Appendix B).

Once a channel interrupt has been received, the IOP initiates an IOTCB, sends an IOTCB pending interrupt to the CC application-specific integrated circuit (ASIC) on the CPU, and waits for the CPU to acknowledge the interrupt. When the interrupt is received by the CPU, it is handled by the CC ASIC, which acts as the IOTCB processor within the CC ASIC. Refer to Appendix B for illustrations and descriptions of the channel transfer sequences.

The IOBB also detects and reports errors. The Y1 bus enables parity transfers between the CPU and IOBB. The IOBB can thus detect and report parity errors, of which there are two types: errors during IOTCB fetch and errors during IOTCB execution. If a parity error occurs during the IOTCB fetch operation, the CC ASIC is not allowed to execute the IOTCB.

Errors that occur during IOTCB execution can also be of two types: command channel errors or data channel errors. In both cases, the execution of the IOTCB continues to completion, then the YC ASIC initiates a retry. If this retry is not successful, an error message (IOTCB execution error) is returned to the MIOP. At this point, the operating system determines the procedure to follow for further error resolution.

Figure 4-1 shows how the IOBB fits into the communication path employed by the CRAY Y-MP EL system. It must be remembered that the IOBB is a slave device to the IOP connected to it via the VMEbus. Refer to Figure 4-2 for a general block diagram of the IOBB.

Each of the Y1 busses has a channel pair number assigned to it. Because the Y1 bus is bidirectional, it must be considered a channel pair. These channel assignments are as follows:

- CPU 0
  - CC0 - channels 20/21
  - CC0 - channels 22/23
  - CC1 - channels 24/25
  - CC1 - channels 26/27

- CPU 1
  - CC0 - channels 30/31
  - CC0 - channels 32/33
  - CC1 - channels 34/35
  - CC1 - channels 36/37

- CPU 2
  - CC0 - channels 40/41
  - CC0 - channels 42/43
  - CC1 - channels 44/45
  - CC1 - channels 46/47

- CPU 3
  - CC0 - channels 50/51
  - CC0 - channels 52/53
  - CC1 - channels 54/55
  - CC1 - channels 56/57

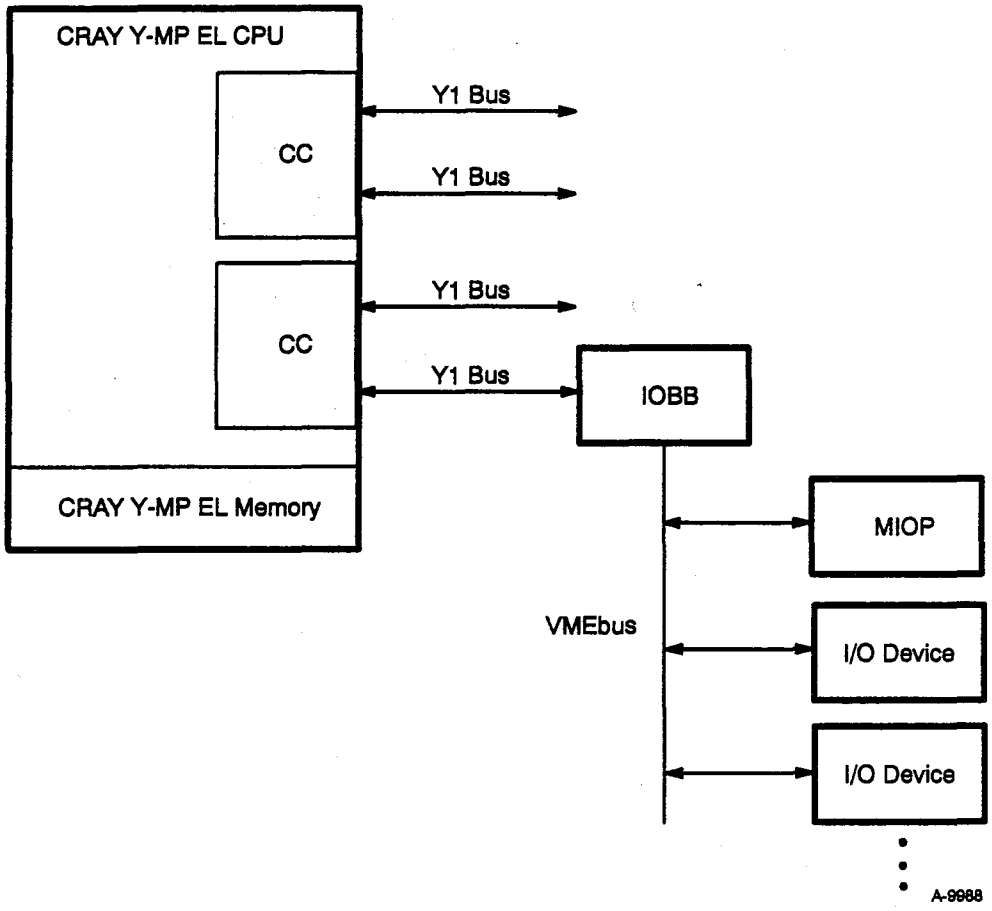


Figure 4-1. IOBB Communication

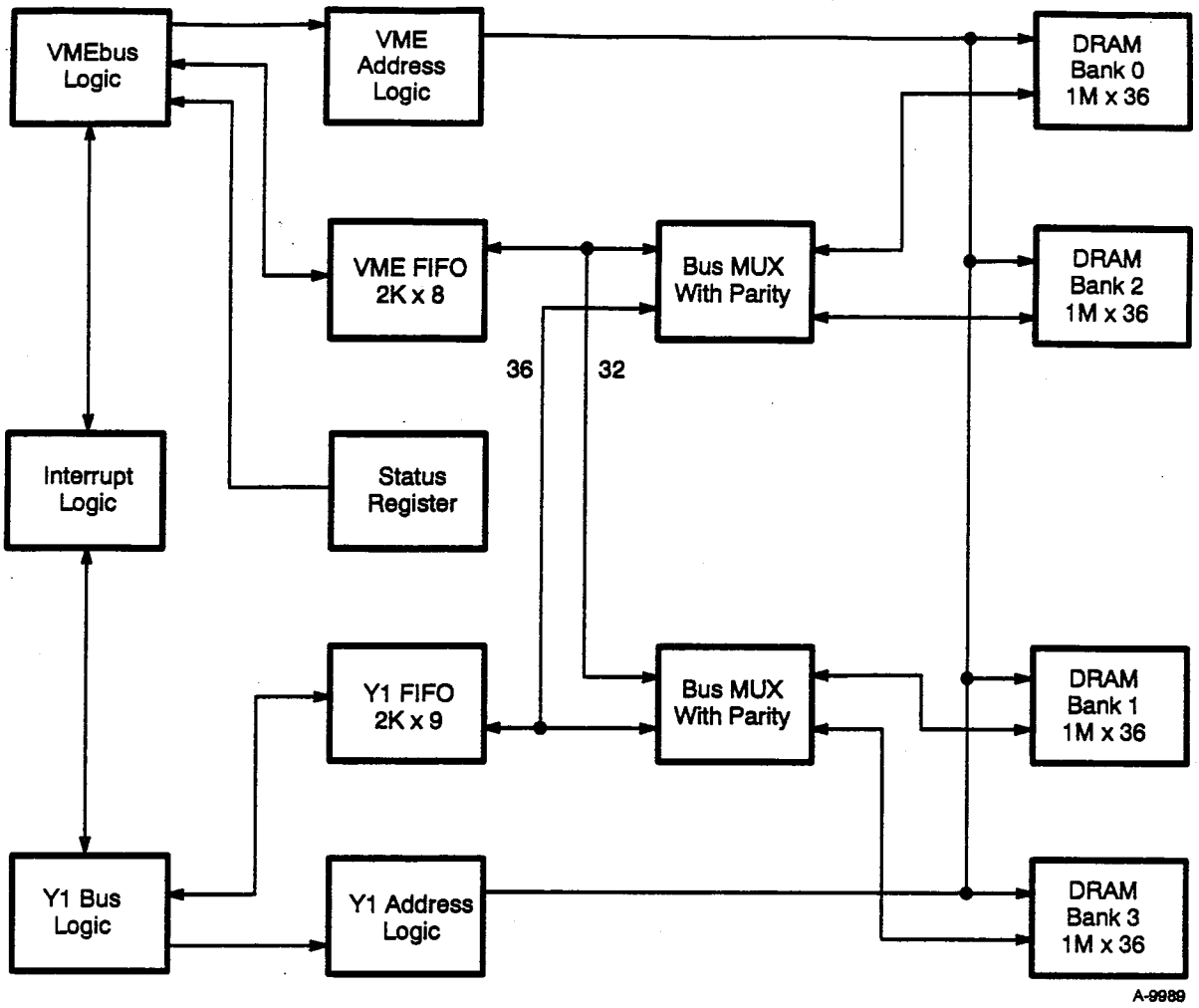


Figure 4-2. IOBB Block Diagram

Communications

No discussion of an IOS would be complete without an introduction to the communications channel. The communications channel in the CRAY Y-MP EL system is called the Y1 bus. The Y1 bus is capable of 40-Mbyte/s transfer rates; these data transfers exist as data bursts of 4, 32, 64, or 128 thirty-two-bit words. The actual data signal is a differentiated value that provides a high level of noise immunity. Refer to Appendix B for a general diagram of the Y1 bus, as well as a table that lists the exact pin assignments.

Communication between the MIOP, the other IOSs, and the maintenance workstation (MWS) takes place via an RS-485 serial interface that can sustain transfers of 1.2 Mbits/s. This is a serial interface; therefore, ~~any point that is defective eliminates the string~~. Essentially, if the MIOP is

if IOS x is defective - eliminates all IOS's, ANY other single IOS x failure only effects that IOS.

down, the entire system is down. Refer to Figure 4-3 for an illustration of this daisy chain. This figure also shows the communication path from the MIOP to the required system peripherals via the SCSI interface. These system peripherals are the .25-inch cartridge tape drive and the Winchester hard disk drive. The helical scan tape drive is optional, as is the system console. The system console used with the CRAY Y-MP EL system is a Wyse model 60 using an RS-232 interface to the MIOP.

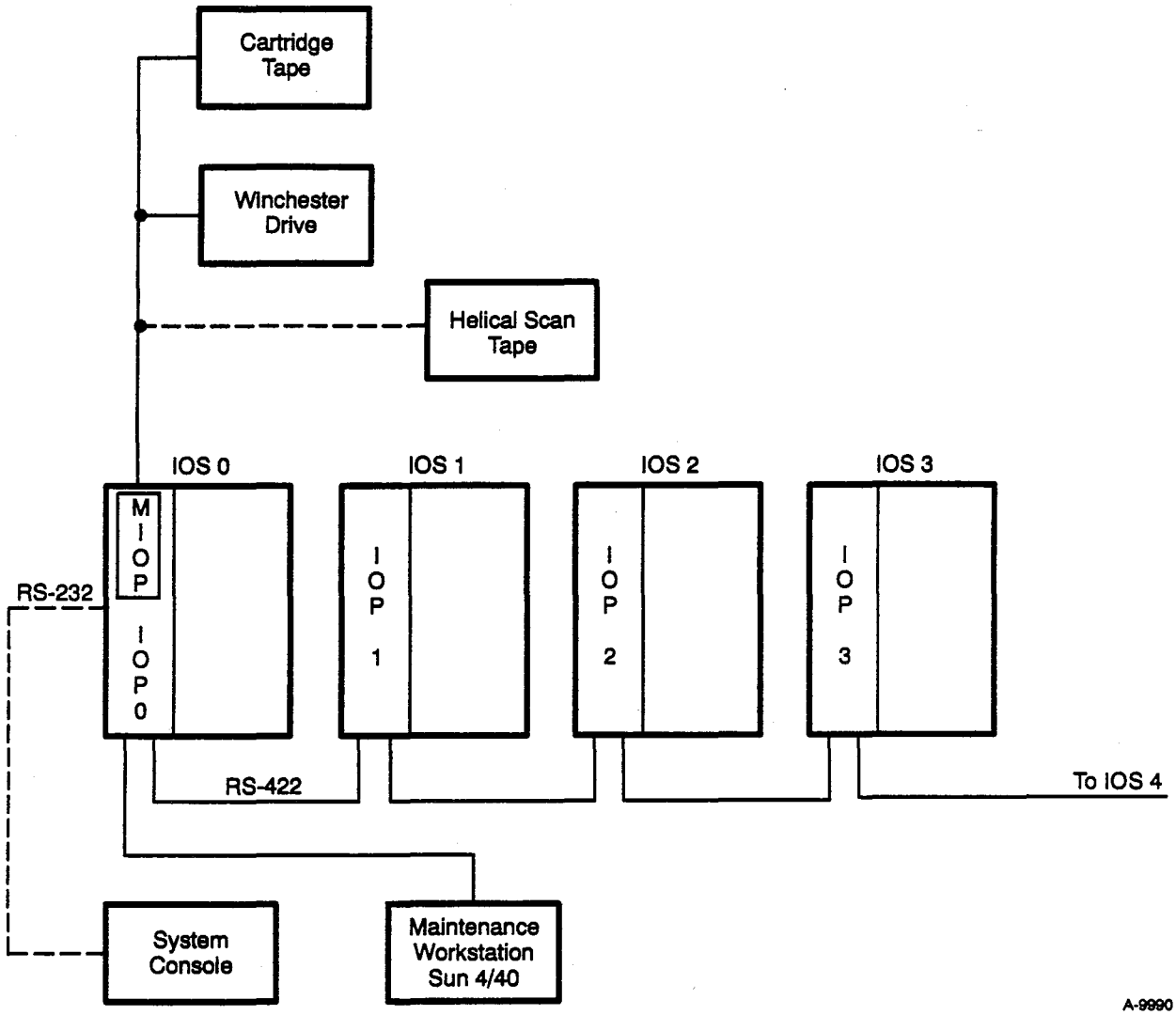


Figure 4-3. IOP Daisy Chain Configuration

IOS-supported Peripheral Controllers

The design of the IOS allows many different controllers to be installed. Consequently, many different peripheral devices can be connected to the CRAY Y-MP EL system. The types of controllers supported by Cray Research include:

- Enhanced serial drive interface (ESDI) disk controller with one to four 1.3-Gbyte drives
- IPI-2 disk controller with one or two 2.7-Gbyte drives
- Disk array subsystem (DAS) controller that can control 10 to 40 Gbytes of data
- Network controllers
  - Ethernet
  - FDDI
  - HYPERchannel
- Pertec controller with a 125 ips 9-track tape drive
- SCSI controller for square-cartridge tape drive (18-track)

Refer to Figure 4-4 for a configuration diagram of these devices. To gain a more complete understanding of the individual controllers, refer to the Original Equipment Manufacturer (OEM) manuals supplied with the system. The specific controllers are:

- DC-3 ESDI disk controller
- DC-4 IPI-2 disk controller
- DAS-2 disk array subsystem
  - 10 ESDI disk drives
- IFI1 FDDI
- HC1 HYPERchannel interface
- HI1 High performance parallel interface (HIPPI)
- SI1 VMEbus SCSI host bus
- TC-2 9-track tape drive interface (Pertec)

Refer to Appendix C for more specifications.

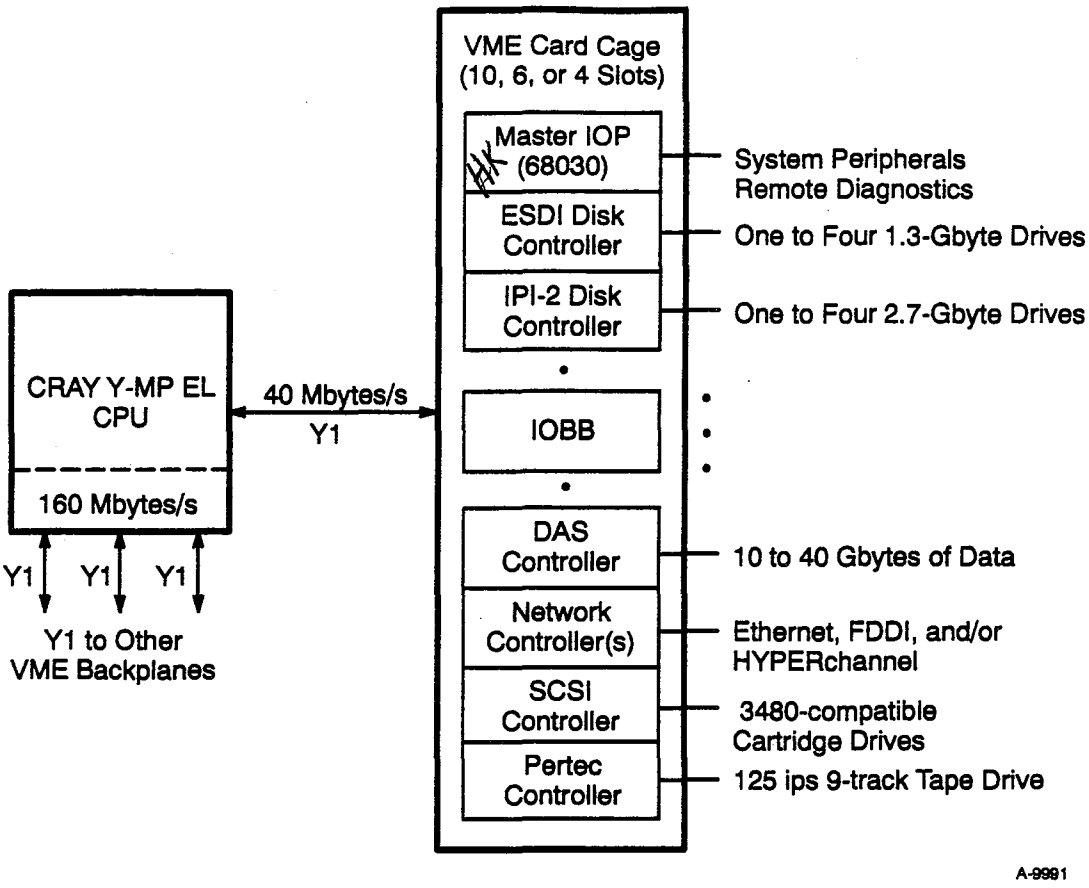


Figure 4-4. IOS Specifications

5 PERIPHERAL DEVICES

The CRAY Y-MP EL computer system is designed with customer peripheral requirements in mind. The CRAY Y-MP EL system can accommodate a wide range of peripheral devices with a diverse amount of storage and communication capabilities. Because of this wide range of capabilities, in most cases it is best to refer to the original equipment manufacturer (OEM) manual for specific information on the equipment. A list of available peripheral devices and their characteristics follows.

- DD-3 Winchester disk drive
  - High-speed access
  - High-speed data transfer rate (2.753 Mbytes/s)
  - Enhanced serial drive interface (ESDI) - industry standard
  - High mean time between failure (MTBF) (150,000 hours, MIL STD 2.17)
  - 1.321 Gbytes of formatted storage
  - No maintenance
- DD-4 IPI-2 (intelligent peripheral interface) disk drive
  - High-speed data transfer rate (9.34 Mbytes/s)
  - High MTBF (150,000 hours, MIL STD 2.17)
  - 2.7 Gbytes of formatted storage
- TD-2 9-track tape drive (covered in detail in this section)
- TD-3 18-track tape drive (covered in detail in this section)
- EX-2 8mm cartridge tape drive
  - High density (1638 tracks/in.; 74 Mbits/sq. in.)
  - Large capacity cartridge (5 Gbytes)
  - Peak transfer rate of 4 Mbytes/s
  - Sustained transfer rate of 500 Kbytes/s
  - MTBF is 40,000 hours
  - Intended as system backup device

- DAS-2 disk array sybsystem
  - 1 disk array controller (DAC)
  - 10 ESDI DD-3 drives forming one bank
  - 8 data, 1 parity, and 1 spare drive
  - 10.4 Gbytes of storage per bank
  - Sustained transfer rate of 15 Mbytes/s
  - Internal media defect management

- DAS-M disk array controller with multiplexer option installed

- DEB-2 disk array bank
  - 8 DD-3 data drives
  - 1 DD-3 parity drive
  - 1 DD-3 spare drive
  - 1 to 4 DEB-2s connect to 1 DAS-M

To obtain a more detailed description of these devices, refer to Appendix C for the design specifications.

All of the peripheral devices are mounted in the cabinets available. The input/output subsystem (IOS) that controls the peripheral is normally included in the same cabinet. Figure 5-1 shows a typical layout of the various components within the system. The exact placement of any component is determined by the system configuration.

The majority of the CRAY Y-MP EL system peripherals are considered field replaceable units (FRUs). This means that when one of the devices breaks down, it is completely replaced. There are no field repairable parts inside the peripherals, except in the 9-track tape drive (TD-2), the 18-track tape drive (TD-3), and the disk array subsystem (DAS-2) controller. These components are described in the following subsections.

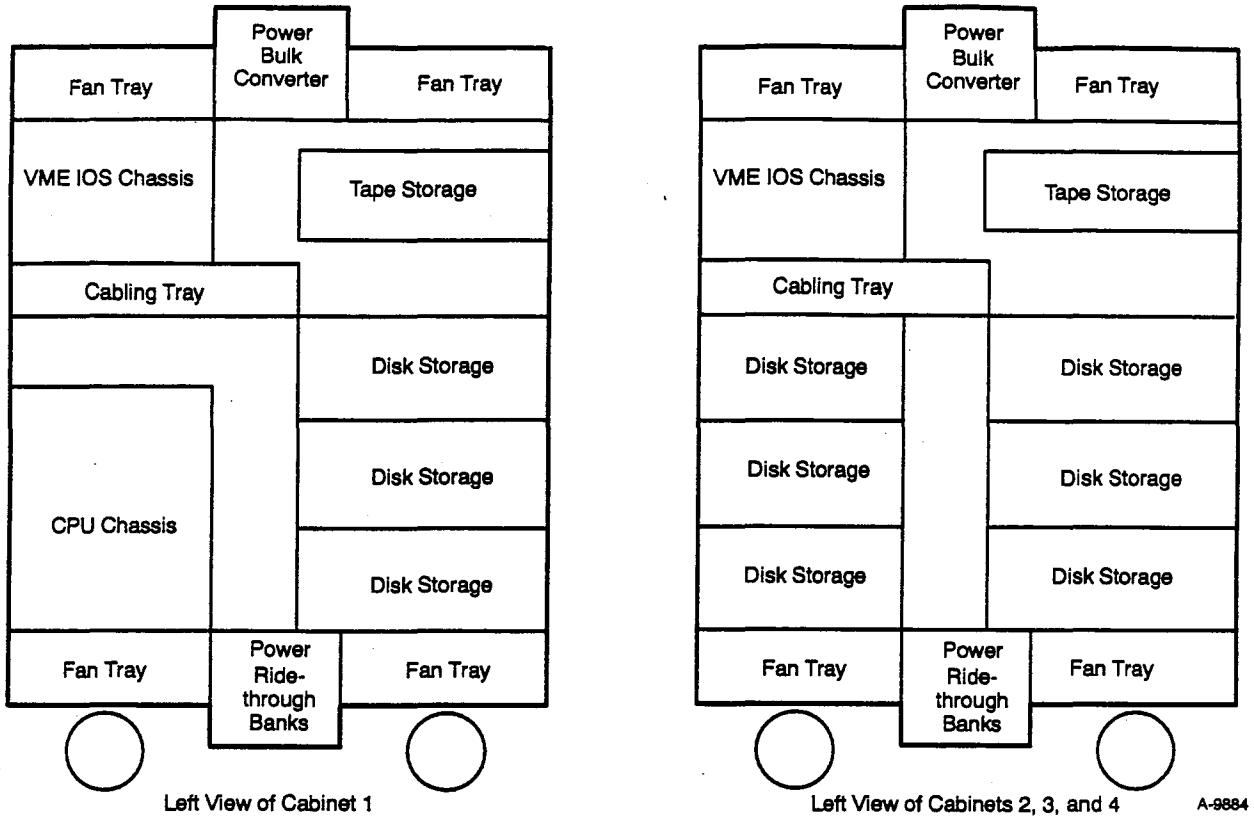


Figure 5-1. Example of Cabinet Layout for the CRAY Y-MP EL System

TD-2 Tape Drive

The TD-2 tape drive (hereafter referred to as the TD-2) is a 9-track tape drive that handles open reel 0.5-in. tape. Any reel up to 10.5 in. fits on the unit. The TD-2 is manufactured by Storage Tek Manufacturing, Ltd. of London as Model 9914. It is designed to handle four types of data encoding:

- NRZI - non-return to zero indicated (800 bpi)
- PE - phase encoded (1600 bpi)
- GCR - group coded recording (6250 bpi)
- DPE - double phase encoded (3200 bpi)

The TD-2 is controlled by the small computer system interface-1 (SI-1) controller card in the VMEbus that connects to a Pertec cache interface within the TD-2. The Pertec interface is one of the FRUs included in the TD-2. Other FRUs in the TD-2 are as follows:

- Data control board (DCB)
- Digital data processor board (DDP)

- Analog data processor board (ADP)
- Servo control board (SCB)
- Power supply board (PSB) (contains two fuses)
- Hub sensor board (HSB)
- In-chute sensor board

Failures on any of these FRUs can be located by using the onboard diagnostics. These diagnostics are run by using the front panel switches on the TD-2. Other than a tape device that indicates failure, there are no provisions for maintaining the TD-2 via remote diagnostics. Faults must be isolated on site.

For complete information on how to run and interpret these diagnostics, refer to the Storage Tek user/diagnostic manual (# 95121796) supplied with the system. Because several combinations of front panels, switches, and diagnostic programs are available, Storage Tek service and diagnostic manuals must be used as references.

When the failure is diagnosed to the FRU level, the FRU must be replaced using the procedures provided in the Storage Tek servicing manual (# 95121797) provided with the system. It should be noted that there are no individual tape-path FRUs. Instead, the entire tape path subassembly is removed in case of failure. When you remove or insert the tape path subassembly, ensure that the Tacho roller is not misaligned on its pivot shaft. The Tacho roller and the heads are the only components that can be damaged, and can cause the TD-2 to malfunction.

As mentioned, the other components that can be damaged during normal removal and replacement are the read/write heads. These heads are thin film heads and are useless if they are scratched. As a precaution when you remove or install the tape path subassembly, cover the heads with an adhesive bandage. Place the cloth pad over the face of the heads and press the adhesive to the sides. Ensure that the adhesive does not contact the face of the heads. After you install the tape path subassembly, clean the heads to ensure proper operation.

The TD-2 Model 9914 is very sensitive to power line voltages. When you install the TD-2, be sure to check the AC power source before inserting the power cord. If the power source measures less than 115 Vac, be sure to set the input power switch to 100 Vac. In all other instances, set the input power switch to match, as closely as possible, the actual supply voltage.

TD-3 Tape Drive

The TD-3 tape drive (TD-3) is also supplied by Storage Tek as the Model 4220 cartridge tape subsystem. The TD-3 is an 18-track tape drive that is IBM 3480 compatible.

The TD-3 comprises several subsystems. These subsystems include:

- Tape transport
- Servo electronics
- Disk drive electronics
- Read/write electronics
- Pneumatics
- Operator control panel
- DC power supply

The disk drive subsystem provides the TD-3 with both functional and diagnostic microcode. The floppy disk drive uses a 3.5-in., 720-Kbyte format, and is controlled by a single integrated circuit (IC) mounted on the system board (SB). Generated signals are sent to or from the drive through the bottom card (BT). The BT contains only foil runners (no active components); therefore, if there is a failure involving the floppy drive, the failing FRU is probably the drive itself or the SB.

As is true in any electro-mechanical device, three types of failure can occur in the TD-3: power-level electrical, mechanical, and signal-level electronic.

Power circuitry for the TD-3 is designed to accommodate either 100 to 120 Vac or 200 to 240 Vac, switch selectable from 47 to 63 Hz, single phase. From this input, the TD-3 supplies + 5 Vdc, +/- 12 Vdc, and + 24 Vdc to the various subassemblies. The only location in the TD-3 where AC power voltages exist is at the DC power supply board (DCPS). All voltages internal to the TD-3 are DC voltages. Refer to Figure 5-2 to locate the power supply.

The mechanical processes of the TD-3 are contained primarily on the tape deck. These mechanical processes deal with loading, unloading, and moving the tape after the cartridge is inserted into the deck. Figure 5-3 and Figure 5-4 show the location of the mechanical FRUs. When a mechanical problem occurs, the problem could be caused by another nonmechanical subassembly. For instance, the servo circuitry could be providing values to the mechanical assemblies that emulate a mechanical problem.

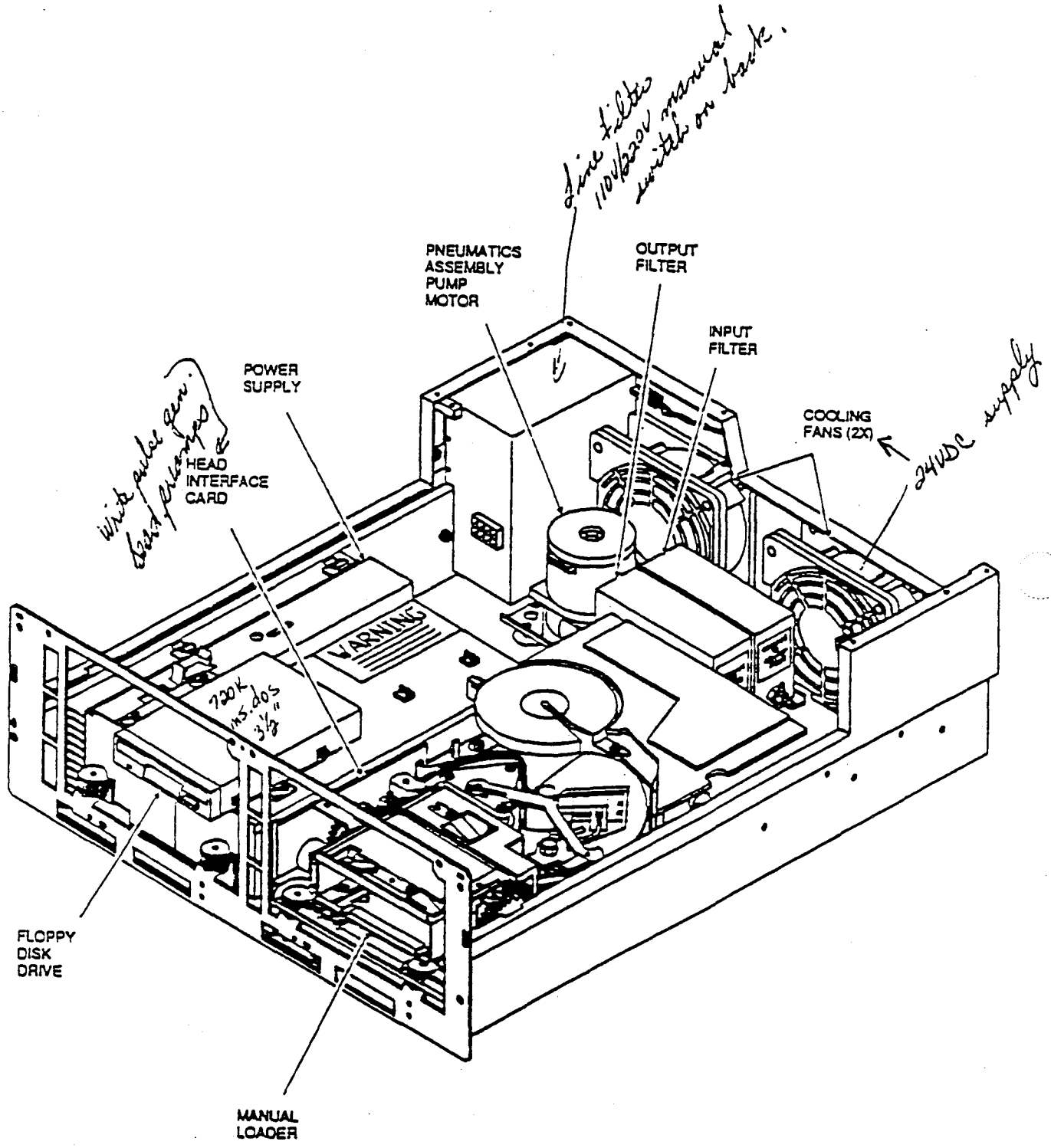


Figure 5-2. TD-3 Tape Drive (Power Supply)

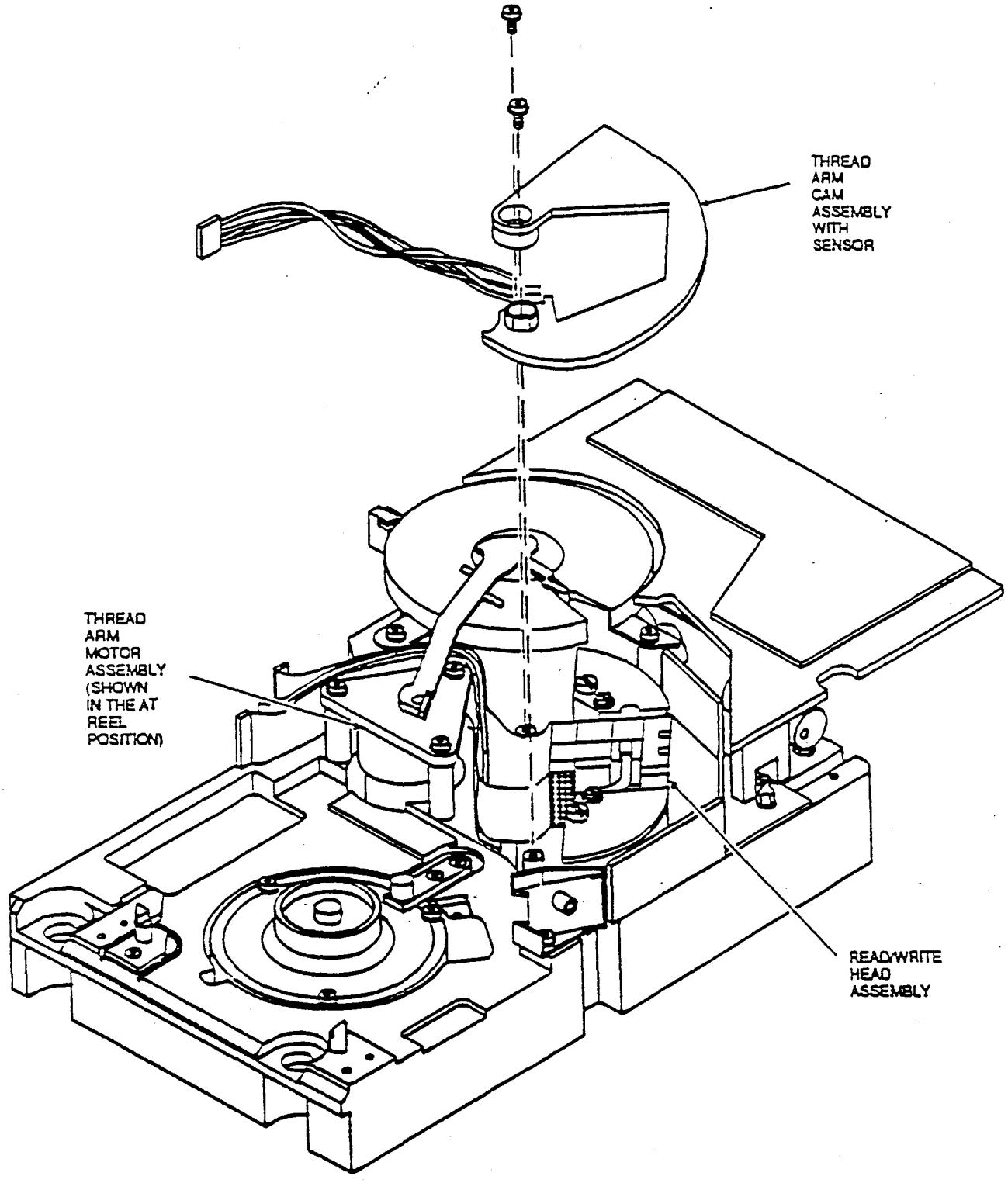


Figure 5-3. TD-3 Tape Drive (FRUs)

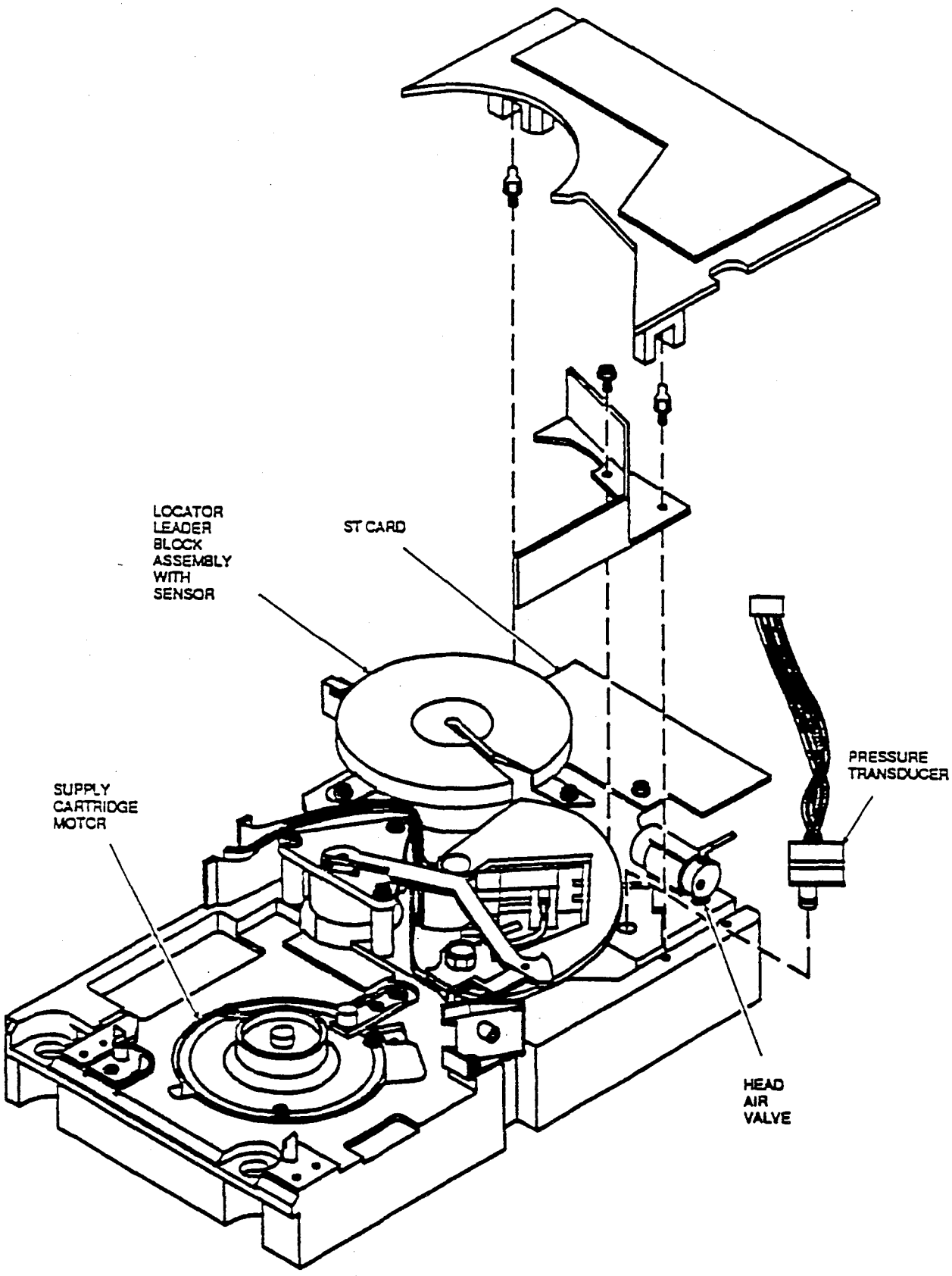


Figure 5-4. TD-3 Tape Drive (FRUs)

The TD-3 cannot be diagnosed from a remote location. A failing FRU within the TD-3 must be identified by using the front panel to load, run, and read the diagnostics and the error codes associated with them. Figure 5-5 shows the front panel of the TD-3. Note that there are four buttons on the panel, two of which are important to loading and running diagnostics: the scroll and the select buttons.

The scroll button advances the display through a menu, one step at a time. The menu is shown in Figure 5-6. When you reach the desired location in the menu, use the select button to select (lock in) the item. Then, push the select button a second time to run the selected item.

For a complete list and a more detailed explanation of the individual diagnostics available for the TD-3, refer to the Storage Tek manual for the Model 4220 that is supplied with the system. That manual contains an extensive explanation of the diagnostics, the error codes as returned to the operator display, and a complete FRU guide.

The following printed circuit (PC) boards comprise the signal-level electronics portion of the TD-3. Figure 5-7, Figure 5-8, and Figure 5-9 show the locations of these PC boards.

- Capacitor (CP) card
- Servo monitor (SM) card
- Servo power (SP) card
- Read interface(RI) card
- System (SB) card

Note that the PC boards reside on or under a tip-up lid on the top of the TD-3 (except the SCSI board) and cannot be accessed unless the TD-3 is extended from the rack. Follow the procedure provided in Section 10 of this manual to extend the TD-3.

The RI card controls generation of clock pulses for each track of data via three phase-locked loop (PLL) oscillators. The RI board also contains the write data encoders and peak detectors.

The SB card is the heart of the TD-3. It contains a 68010 microprocessor that processes host commands, provides I/O interface control, and controls the physical processes relating to tape operations. The SB card also includes a write formatter (WF) IC, a 2-Mbyte buffer, buffer FIFOs, an 8031 bus processor, deskew buffers, a floppy disk controller, and read data formatter devices. Be aware that all operations in the TD-3 are linked to the SB. When you troubleshoot the TD-3, remember that the SB may be faulty.

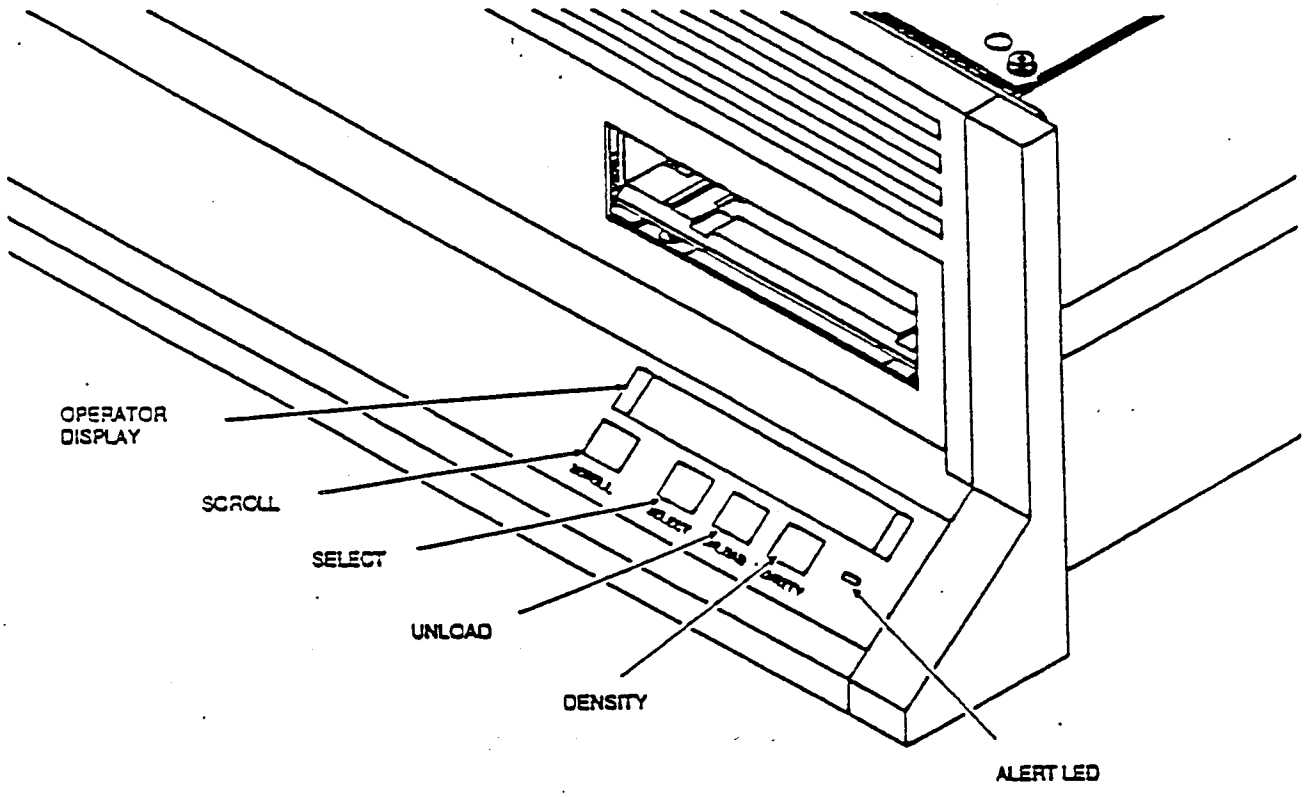


Figure 5-5. TD-3 Tape Drive Front Panel

Offline Menus

```
[OF:DIAG:      *]
[+SUBSYS STATUS]
      [*Online Request]
      [*Exit      ]
[+SET OR DISPLAY]
      [**CONFIGURATION]
            [> > Set Diags:None]
            [> > Diag EC LVL:0]
            [> > Set Host: SCSI]
            [> > Lang: English]
            [> > Set Part: Auto]
            [> > Set Sync Tm: 2]
            [> > Passkey: Enab]
            [> > Sync Nego:Enab]
            [> > Set BRN:   00]
            [> Exit      ]
      [*Retension Tape]
      [*Write Tape Mark]
      [**Set Scsi ID: 0]
      [**Set Lun:   0]
      [**Set Clean:  16K]
      [*Exit     ]
[+DIAGNOSTICS   ]
      [*Diag: Test 1   ]
      [*Diag: Test 2   ]
      [*Diag: Test 3   ]
      [*Diag: Test 4   ]
      [*Diag:Load/Unld]
      [**Diag: Loop 1]
      [Diag: Test Disp]
      [*Loader Sensors]
      [*Disply Pressure]
      [*Disply Tension]
      [*Exit      ]
[+SAVE TRACE   ]
      [*Save Trc: All]
      [*Exit     ]
```

Online Menus

```
[          *]
[ON:IDLE:     *]
[+SUBSYS STATUS]
      [*Offline Request]
      [*Exit     ]
```

Figure 5-6. Basic 4280 Menus with a SCSI Interface

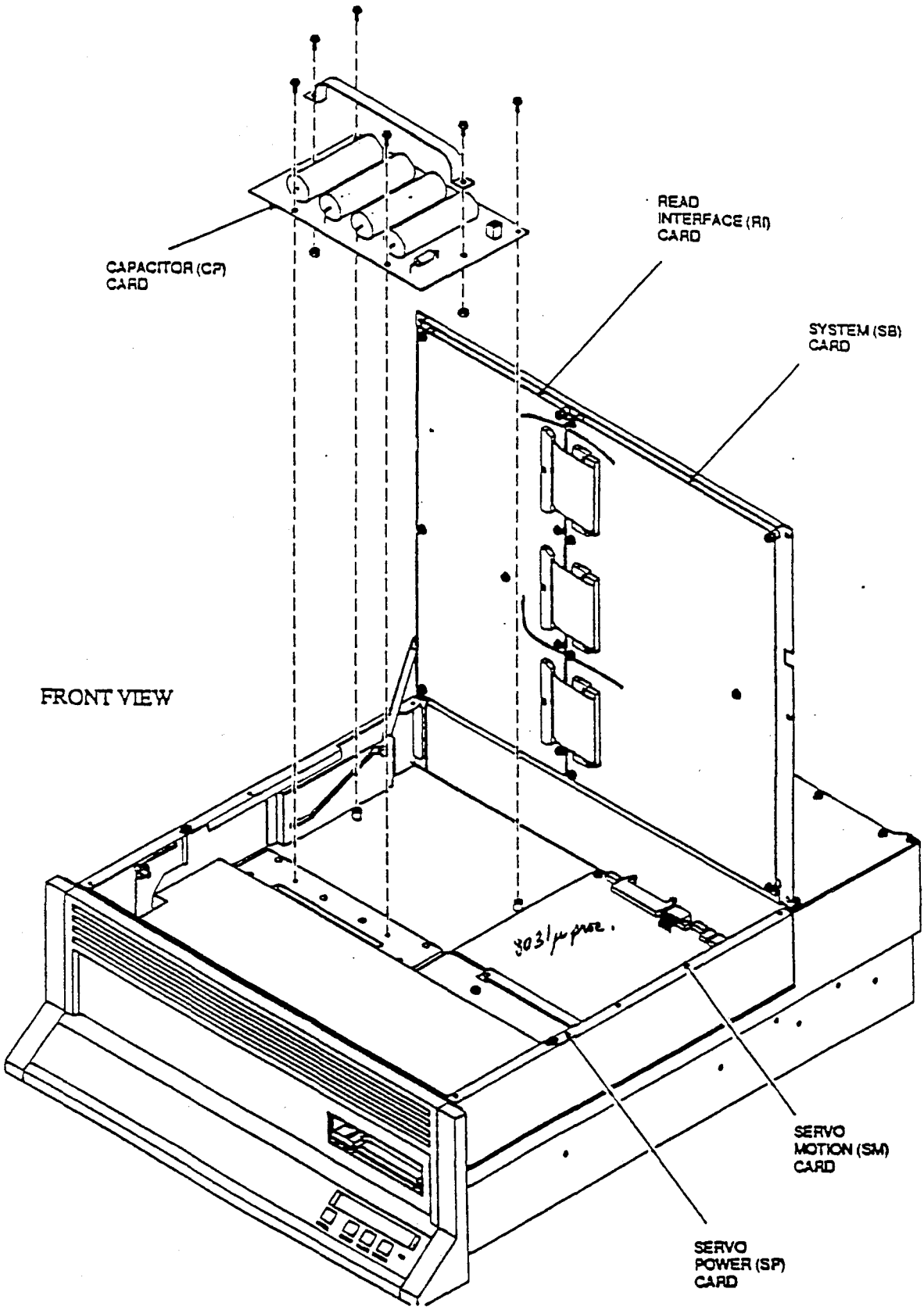


Figure 5-7. TD-3 Tape Drive Controller Module FRUs (Front View)

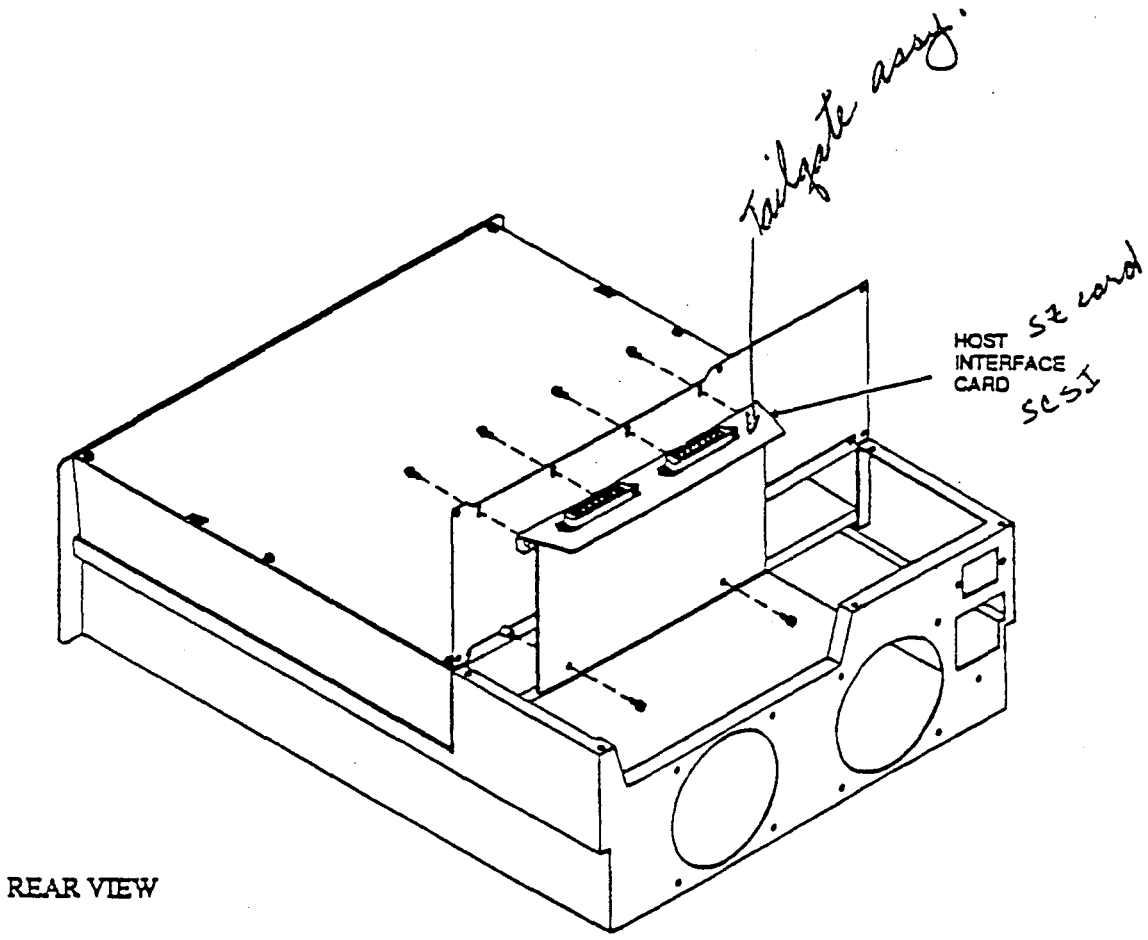


Figure 5-8. TD-3 Tape Drive Controller Module FRUs (Rear View)

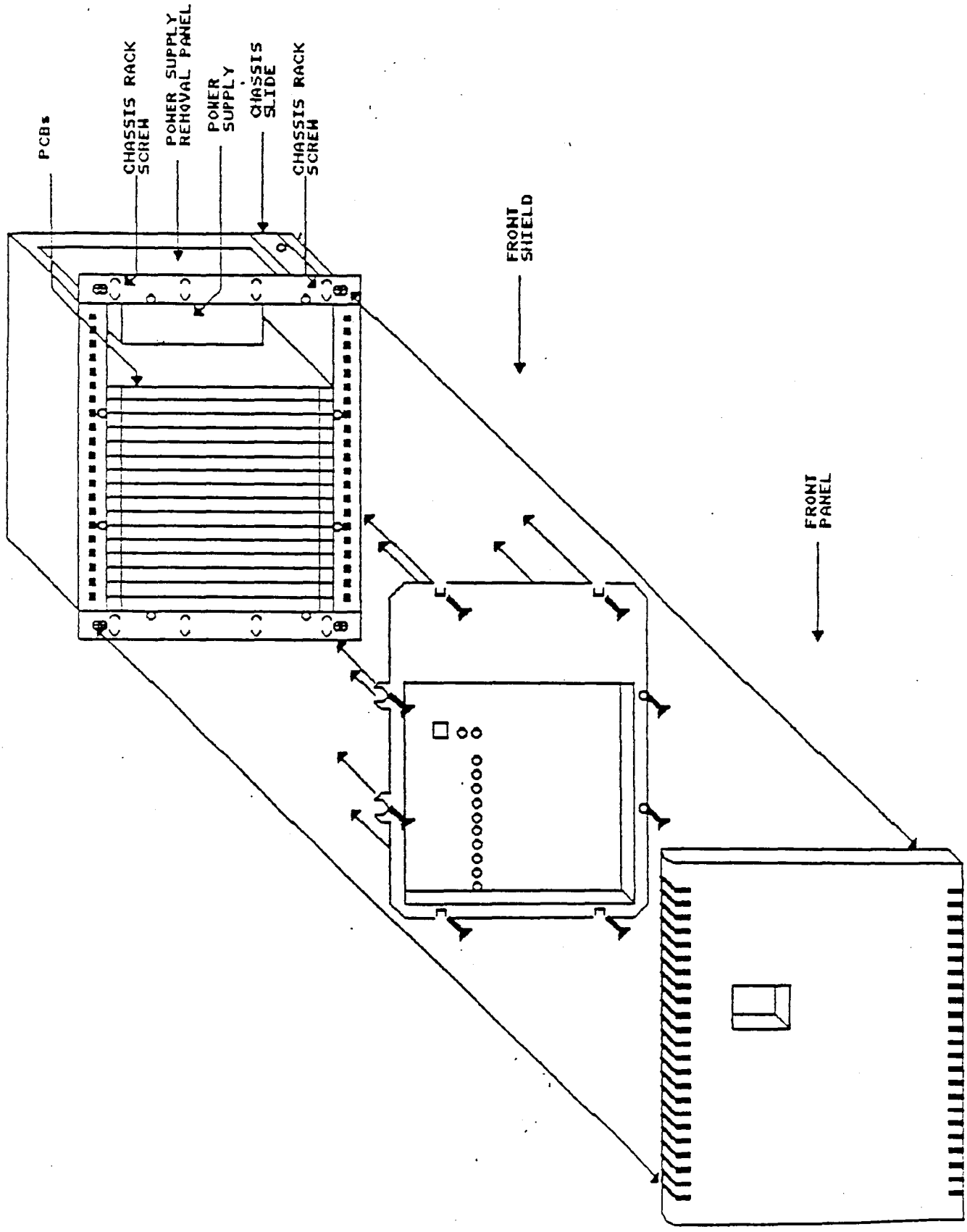


Figure 5-9. TD-3 Chassis

Disk Array Controller

The third non-FRU device in the CRAY Y-MP EL system is the disk array controller (DAC) unit supplied by Maximum Strategy, Inc. The DAC is an intelligent disk controller capable of storing and retrieving data from one to four banks of eight standard ESDI disk drives in parallel. The DAC also controls an additional drive for each bank of eight used to store a parity bit for fault protection as well as an operational standby (hot spare) drive used to replace a faulty drive from the bank.

The drives supported by the DAC are 5.25-in. ESDI serial data drives, capable of transferring data at a rate of 16 Mbytes/s.

Each of the ten disk drives in the bank are connected to a disk interface and data buffer PC board in the DAC. The DAC also contains a parity PC board, separate from the parity drive disk interface PC board, and a CPU PC board. The CPU contains a high-speed interface (HSI) unit. The DAC is designed to interface with up to four banks of ESDI drives. If more than one bank of drives is to be controlled, an additional HSI PC board must be installed for each bank. A multiplexer board must also be installed to link the four banks to the one controller.

Figure 5-9 indicates which components must be removed to access the PC boards, and Figure 5-10 shows the location of each of the PC boards within the DAC.

The DAC has a small cut-out on the front panel (refer to Figure 5-9) in which the READY LED, a RESET button, and RS-232 serial communication (COM) port are visible. The READY LED is located on the CPU card in slot 12, and is a visual indicator of the state of the DAC. When the READY LED is glowing solid red, it indicates that the DAC is offline. During a normal power-on sequence or a reset sequence, the LED glows red as the disk drives spin up. The normal time for this sequence should not exceed 120 seconds. If the LED has not turned green after 120 seconds, it indicates a problem with the DAC or with one of the disk drives. Note in Figure 5-9 that each of the disk interface PC boards has an LED visible through the front shield. As the disk drive associated with the interface board spins up, this LED is red. When the disk drive is up to speed and when the internal diagnostics for the disk interface PC board have run, the LED turns green.

If the CPU READY LED is red, no communication is possible with the DAC. If any one of the data buffer/disk interface LEDs is red, either the disk drive failed to reach speed or the internal diagnostics for that interface board failed. In either case, the next step is to initiate disk drive diagnostics.

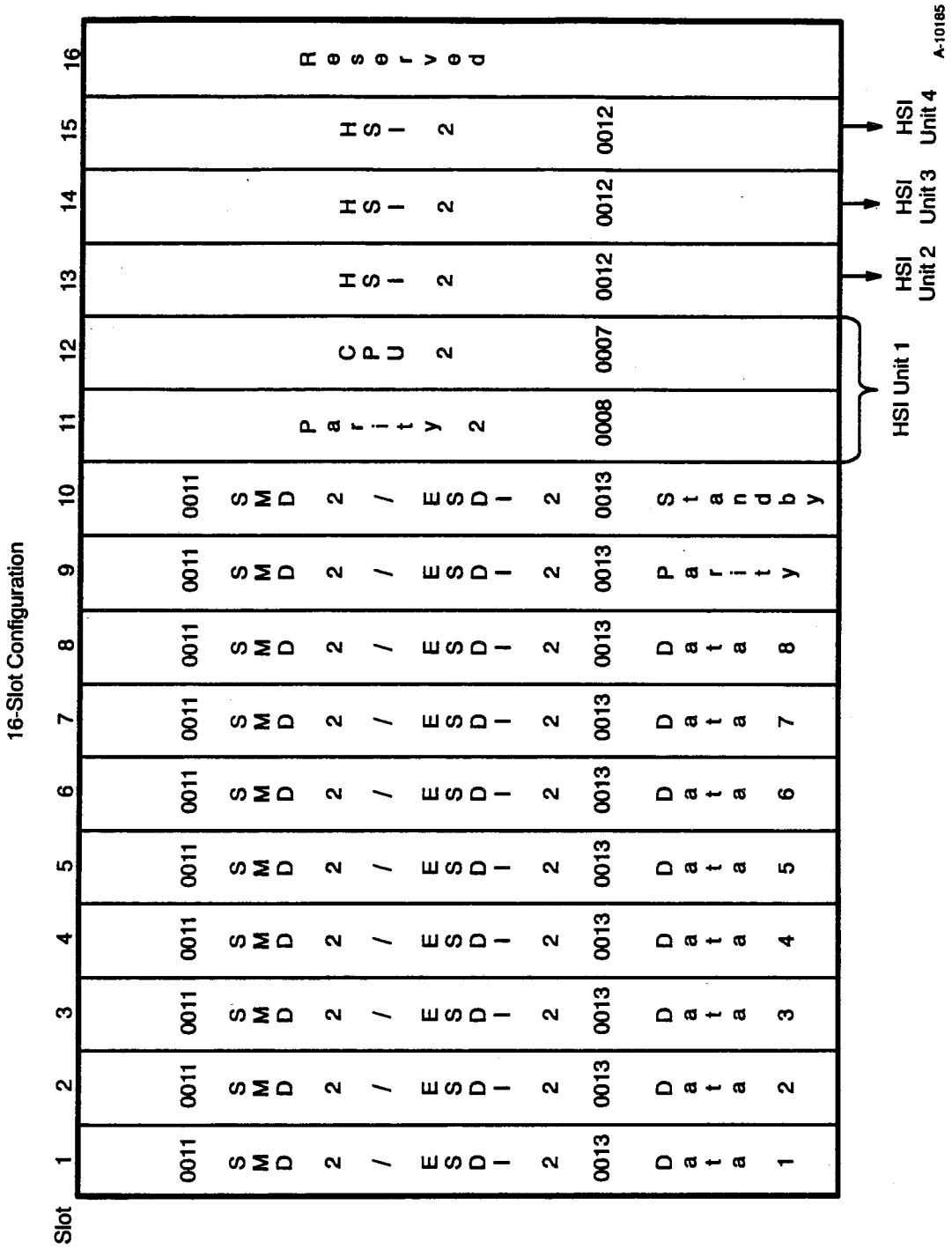


Figure 5-10. DAC Printed Circuit Board Locations

During normal operation, the RESET button should not be used. Instead, the reset function should be initiated by software through the IOS. However, during a power-up sequence you may use the RESET button once if the READY LED fails to turn green within 120 seconds.

The COM port located on the front of the DAC is a serial RS-232 connection that can be used for offline diagnostics or for online system configuration. These functions require test equipment not normally supplied, either on site or at the service center. If you need more information regarding the use of the COM port, refer to the Maximum Strategy documentation supplied with the system or contact Hardware Product Support.

Diagnostics

The peripheral devices associated with the CRAY Y-MP EL system are FRUs. There is only one online diagnostic test, named olcfdt, that checks the functionality of the peripherals. This test is explained in the *Cray Research Entry Level (EL) Computer System UNICOS Online Diagnostic Maintenance Manual*, publication number SPM-1025. The only response of the olcfdt diagnostic to UNICOS is pass or fail. Likewise, there are no offline diagnostics, in place or planned, to deal specifically with the CRAY Y-MP EL system peripherals.

Disk drives for the CRAY Y-MP EL system are driven by intelligent controllers that perform media defect (flaw) management without operator/technician intervention.

6 DIAGNOSTICS

If the CRAY Y-MP EL computer system does not operate properly, a customer employee is the first person notified. This notification usually occurs via a fault code provided by the UNICOS operating system. The customer employee then follows a procedure, defined by the maintenance contract, to gather error information and notify the Cray Research Service Center.

When the service center has been notified, the problem becomes the responsibility of the Cray Research field engineer, who troubleshoots the system using the tools that have been provided for that purpose. Among these tools is a complete set of Cray Research diagnostic tests, both online and offline, that are accessed by remote service when available or by on-site intervention. The purpose of this section is to provide a general description of these diagnostics.

Online Diagnostics

The online diagnostics available for the CRAY Y-MP EL system are listed in Table 6-1. Instructions for running these diagnostics as well as more detailed descriptions of these diagnostics are contained in the *Cray Research Entry Level (EL) Computer System UNICOS Online Diagnostic Maintenance Manual*, publication number SPM-1025. These diagnostic tests are designed to function as a submitted job under UNICOS, and can be used while user jobs are concurrently submitted into the queue.

Table 6-1. Online Diagnostics

Name	Test Description	Test Sections		Monitor	Notes
		Section Select	Function		
olcmon	Online confidence monitor			olcmon	Accepts and interprets commands
olcfpt	Online comprehensive floating-point test				
olcm	Online central memory test	1	Memory storage and scalar path test	olcmon	
		2	Memory storage and T register path test		
		3	Memory storage and B register path test		
		4	Memory storage and V register path test		Uses only the first vector logical unit
		5	Memory storage and V register path test		Uses both vector logical units
		6	Random data test		
		7	Memory conflict test		
olcrit	Online comprehensive random-instruction test			olcmon	Generates both random instructions and random data

Table 6-1. Online Diagnostics (continued)

Name	Test Description	Test Sections		Monitor	Notes
		Section Select	Function		
olcsvc	Online comprehensive scalar and vector comparison test			olcmon	Tests V registers, functional units (FUs) and paths; S registers, FUs, and paths; A registers, FUs, and paths must be functional
olibuf	Online instruction buffer test			olcmon	Tests data, in-stack, and out-of-stack jumps
olsbt	Online semaphore, shared B, and shared T test			olcmon	
olcfdt	Online confidence test for mass storage devices				

A group of diagnostic tests designed to be used in devices that have been removed from normal system operation is also available. These programs are still run as online programs, but are known as down device programs. They provide testing for individual central processing units (CPUs) and peripheral equipment. A list of the down device programs is provided in Table 6-2.

Two utility programs are also available as online maintenance devices. These utilities are:

- olhpa - A hardware performance analyzer that analyzes and reports the hardware errors and statuses reported in the system error log.
- runsequence - A utility used with the crontab command to perform automatic test sequencing.

More detailed information on both the down device tests and the utility programs is contained in the *Cray Research Entry Level (EL) Computer System UNICOS Online Diagnostic Maintenance Manual*, publication number SPM-1025.

Table 6-2. Down Device Programs

Name	Test Description	Monitor	Notes
oldmon	Down CPU monitor	self	
unitap	Online magnetic tape test		

Offline Diagnostics

In most cases, the online diagnostic tests should lead you to a logical swap and repair operation. However, for those instances when the online diagnostics do not identify the problem, there is a full suite of offline diagnostic tests available. The major disadvantage of using offline tests to diagnose a problem is that the system must be offline; that is, no user jobs can be running and the operating system must be turned off.

When the system has been taken offline, the product specialist can call up any of the offline diagnostics listed in Table 6-3, Table 6-4, and Table 6-5. There are two separate levels of diagnostics listed: level 0 and level 1. The level 0 tests are used as dead machine tests, while the level 1 tests are used as failure-specific tests.

All of the listed offline diagnostic tests are run under the mainframe maintenance environment (MME) on the maintenance workstation (MWS). The MME is a menu-driven program designed to work in all Cray Research computer systems. For detailed information on how to use MME and what it does, refer to the *CRAY Y-MP EL Offline Diagnostic User Guide*, publication number CDM-xxxx-PR1. This manual also contains a complete description of all the available offline diagnostic tests, including standard locations, restrictions, and the type of monitor used.

Table 6-3. Offline Diagnostics - Level 0 Tests

Name	Test Description	Notes
INTA	Checks integer instructions 030*ijk* through 033*ijk*	
YEXCH	Tests exchange package register	Tests exchange paths
YTD0	Tests instruction buffers, parcel 0	Tests ability to do fetch
YTD1	Tests instruction buffers, parcel 1	
YTD2	Tests instruction buffers, parcel 2	
YTD3	Tests instruction buffers, parcel 3	

Table 6-4. Offline Diagnostics - Monitors

Name	Description	Notes
YM8	Runs all processors with same diagnostic	
YMI	Interrupt-driven monitor	
YMM	Basic monitor	
YMS	Interrupt-driven, master/slave monitor	One diagnostic in all processors, reported by master
YSMI	Multi-function monitor	
YSMY	Multi-function monitor	Replaces all other monitors except M8

Table 6-5. Offline Diagnostics - Level 1 Tests

Name	Test Description	Test Sections		Monitor	Notes
		Section Select	Function		
BAAT	Basic address-adder test	One section only		OWN	Tests 030*ijk* and 031*ijk* instructions
CRIDY	Multiple-CPU random-instruction test	One section only		YSMI	
EEUTE	Execution unit (EU) test	One section only		YSMY	
YAAB	Address register basic test	Condition 1	022*ijk* instructions	MM or YSMY	
		Condition 2	020*ijk* instructions		
		Condition 3	021*ijk* instructions		
		Condition 4	030*ijk* instructions		Ai = Aj + Ak
		Condition 5	030*ijk* instructions		Path test
		Conditions 6 – 10	Special case instructions		030*i*0*k*, 030*ij*0, 031*i*00, 031*i*0*k*
		Condition 11	020 and 021 instructions		Walking a 1 through the unused *jk* fields
YAHT	Ah addressing test	0 – 9		MS or YSMY	
		7	Will not run unless CPU 0 enabled in location CPUS		
		8	Automatically disabled if MS not used		
YAMB	Address multiply basic test	0	K = 1; J = sliding ones	MM	
		1	j = 1; k = sliding ones		
		2	Predetermined operands for enables and satisfies		

Table 6-5. Offline Diagnostics - Level 1 Tests (continued)

Name	Test Description	Test Sections		Monitor	Notes
		Section Select	Function		
YAMB (cont.)		3	Predetermined operands for carries		
		4	Random increasing operands		
		5	Path test		
YARS	Address (A) and scalar (S) register add and multiply test	0	A register subtract	YSMY, MI, M8	All sections use toggle numbers of a 1, a 3, a 5, and a 4-bit random number in sequence
		1	A register add		
		2	A register multiply		
		3	S register subtract		
		4	S register add		
		5	S register multiply		
YAVE	Vector register test			MI, YSMY	
YBRT	Block transfer register test	0	B register basic and block transfer	MS, YSMY	Sections 0, 1, and 2 do not use B00 for return jumps; can detect erratic B00 operation
		1	T register basic and block transfer		
		2	V register basic and block transfer		
		3	B, T, and V registers comprehensive block transfer		

Table 6-5. Offline Diagnostics - Level 1 Tests (continued)

Name	Test Description	Test Sections		Monitor	Notes
		Section Select	Function		
YBTAS	B to A register transfer or T to S register transfer test	0	Tests 025*ijk*	MI, YSMY	
		1	Tests 025*ijk*		
		2	Tests 075*ijk*		
		3	Tests 024*ijk*		
		4	Tests random combinations of the four instructions		
YCMPY	Compatibility mode test			OWN	Determines CRAY Y-MP compatibility to CRAY Y-MP EL
YEJT	Exchange jump test	0	Tests A0 through S7 registers using scalar memory instructions	OWN	
		1	Tests (mn + Ah + DBA), (A0 + Vj + DBA), and (A0 + Ak + DBA) address adders		Uses sliding ones address pattern
		2	Tests DBA range error		
		3	Tests DLA range error		
		4	Tests instructions ability to set/clear mode bits		
		5	Tests 076*ijk*, 077*ijk*, and 0014*j*3 instructions		

Table 6-5. Offline Diagnostics - Level 1 Tests (continued)

Name	Test Description	Test Sections		Monitor	Notes
		Section Select	Function		
YEJT (cont.)		6	Tests for operand and program range errors		
		7	Tests address adders using random operands		
YFPT	Floating-point units test			Mi, M8, YSMY	Tests floating-point add, multiply, and reciprocal functional units
YJPT	Jump test	0	Tests 006*ijkm* instruction	OWN	Only runs in CPU selected as master
		1	Tests A0 conditional branch instructions		S4 = condition counter; A0 = failing data pattern
		2	Tests S0 conditional branch instructions		A1 = condition counter; S0 = failing data pattern
		3	Tests P to B00 path		A1 = condition counter; S0 = bits in error; S1 = actual data; S2 = expected data
		4	Tests B00 to P		A1 = condition counter; S0 = bits in error; S1 = actual data; S2 = expected data
		5	Bxx to P		A1 = Bxy; S0 = bits in error; S1 = actual data; S2 = expected data

Table 6-5. Offline Diagnostics - Level 1 Tests (continued)

Name	Test Description	Test Sections		Monitor	Notes
		Section Select	Function		
YJPT (cont.)		6	Various IBA jumps		
		7	Times in-buffer jumps; confirms that no fetch was done		A1 = condition counter; A7 = loop counter; B00 = address of failing code
		8	Parcel 1 of instruction in one instruction buffer; parcel 2 in different instruction buffer		A1 = condition counter (equals instruction buffer under test); A7 = loop counter
YPAVE	Memory addressing, conflicts, and port select tests	0	1 and 0 data; address limited to 11,000 words	MI, M8, or YSMY	
		1	Random data; address limited to 11,000 words		
		2	Random data; address unlimited		
		3	Random data; gather/scatter		
		4	Abort on operand range error		
YPRTC	Real-time/programmable clock test	0	RTC data integrity test	MI or MS	
		1	RTC propagate carry test		
		2	RTC path test		
		3	Basic PCI mechanism test		Forces time-out condition
		4	Basic CCI and DCI mechanism test		
		5	Basic ICD register test		

Table 6-5. Offline Diagnostics - Level 1 Tests (continued)

Name	Test Description	Test Sections		Monitor	Notes
		Section Select	Function		
YPRTC (cont.)		6	PCI II register timing test		
		7	RTC fanout test		
YSAB	Scalar register basic test	0	Checks zeroes, ones, and alternate patterns	MM	Tests S registers and S adders
		1	Checks compliment patterns mn to S		
		2	Tests 060 instructions		Predetermined operands
		3	Path test		
		4	Tests 023*ij*0 instruction		
		5	Tests 071*i*0*k* instruction		
		6	Tests 040 and 041 instructions		
YSAS	Scalar adder test	0	Address add	MI	
		1	Scalar add		
		2	Address multiply		
		3	Address subtract		
		4	Scalar subtract		
		5	Population count and leading zero		
		6	A to S floating-point		
		7	A to vector length (VL) register		

Table 6-5. Offline Diagnostics - Level 1 Tests (continued)

Name	Test Description	Test Sections		Monitor	Notes
		Section Select	Function		
YSCL	Scalar logical basic test	Condition 0	042 instruction	MM	
		Condition 1	043 instruction		
		Condition 2	044 instruction		Conditions 2 through 7 are tested with no S0 operands
		Condition 3	045 instruction		
		Condition 4	046 instruction		
		Condition 5	047 instruction		
		Condition 6	051 instruction		
		Condition 7	050 instruction		
		Condition 10	044 instruction		Conditions 10 through 15 are tested with S0 operands
		Condition 11	045 instruction		
		Condition 12	046 instruction		
		Condition 13	047 instruction		
		Condition 14	051 instruction		
		Condition 15	050 instruction		
YSCS	Scalar shift test	0	Shift all S registers left and right by a count of 1, 2, 4, 10, 20, and 40	MM or YSMY	
		1	Shifts an S register left and right by all bits of an A register 1, 2, and 4 until A is negative		
		2	Double shift left and right; random shift count and data		

Table 6-5. Offline Diagnostics - Level 1 Tests (continued)

Name	Test Description	Test Sections		Monitor	Notes
		Section Select	Function		
YSCS (cont.)		3	Selectable parcel; random shift instruction with random data and shift counts		
YSEM	Shared and semaphore register test	0	Shared B/T address and control tests	MS or YSMY	
		1	Shared B/T data test		
		2	Semaphore set/clear test		
		3	Semaphore master/slave or single CPU test		
		4	Multi-CPU deadlock timing test		
		5	Semaphore master/multiple slave CPUs		
YSMT	Check bit generation and memory error reporting test	0	Tests correct SECDED generation	YSMI	
		1	Tests exchange package fields associated with memory errors		
		2	Memory errors using A and S registers		
		3	Memory errors using B and T registers		
		4	Memory errors using V registers		
		5	Memory errors on exchange		

Table 6-5. Offline Diagnostics - Level 1 Tests (continued)

Name	Test Description	Test Sections		Monitor	Notes
		Section Select	Function		
YSMT (cont.)		6	Memory errors on fetch		
		7	Memory errors for I/O single and block references		
		8	Proper error reporting with back-to-back memory errors		
		9	Tests 001501 instruction		
		10	Tests error bits in status register		
YSR3	Register and scalar/vector instruction (3-parcel) conflicts test			YSMI	
YVBT	Vector register basic test	0	Scalar to vectors	MI or M8	Contains some special error locations:
		1	Vector logical		2001 - failing section
		2	Vector add		2002 - failing condition
		3	Vector shift		2003 - failing subcondition
		4	Vector mask/ compressed index		2004 - failing vector
		5	Vector population/ parity		2005 - failing element
		6	Second vector timing		2006 - vector length
YVPT	Vector path test	0	Vector register test	MI or M8	
		1	Vector path test		
		2	Different paths		

Table 6-5. Offline Diagnostics - Level 1 Tests (continued)

Name	Test Description	Test Sections		Monitor	Notes
		Section Select	Function		
YVPT (cont.)		3	Bit counter		
		4	140 - 177 instruction test		
YVSG	Gather/scatter test	0	Gather using port B	MI	
		1	Scatter using port C		
		2	Gather using port B		Port A conflicts
		3	Scatter using port C		Port A conflicts
		4	Gather using port B		Port C conflicts
		5	Scatter using port C		Port B conflicts
		6	Gather using port A		Port B conflicts
		7	Scatter using port C		Port A and port B conflicts
		10	Gather using port A		Port B and port C conflicts
		11	Scatter using port C		Port A and port B conflicts
		12	Gather using port A		Port B chaining and port C conflicts
		13	Scatter using port C and gather using port B		

7 POWER AND CONTROL SYSTEMS

To be provided.

8 UNICOS ADMINISTRATION

Because the CRAY Y-MP EL computer system has been designed to operate at unattended sites, it is possible that a hardware product specialist could be requested to perform some functions traditionally performed by a software product specialist. While this section can not convey the entire spectrum of software knowledge needed to administer a UNICOS system, it contains enough basic information to allow the hardware specialist to perform some of the basic functions of the system administrator. If you need more information than is provided here, Cray Research recommends that you attend the CRAY Y-MP EL system administrator course offered by Software Training. Another source of information that may be useful is the *UNICOS Installation Guide*, publication number SG-2112.

You need to refer to the latest System Installation Bulletin for the specific release of UNICOS you are working with. In order to run UNICOS 6.1 on the CRAY Y-MP EL system, the Heuricon HK68/V30 input/output processor (IOP) board must have a minimum hardware ECO level of 48. There is a Cray Research PROM chip supplied for installation on the IOP board. This PROM chip must be at revision (REV) level 5.3 to allow proper installation of UNICOS 6.1. You may also need the backup copy of the tape made by the system administrator when he/she installed the UNICOS version originally. If you are using a backup version of a tape, use caution so that no damage is done to the tape.

The release shipment for the current input/output subsystem (IOS) small computer system interface (SCSI) configuration consists of two tapes: an 0.25-in. cartridge tape and an 8-mm helical scan tape, along with pertinent release documents. At the site, there should also be a backup set of tapes. Use the procedure on page 3 of the *UNICOS 6.1 System Installation Bulletin for CRAY ELS Systems*, publication number EL-2.1-SIB, to install IOS software contained on the 0.25-in. cartridge tape. This procedure takes approximately ___ minutes.

The entire IOS and UNICOS installation will require approximately three hours to complete. During this time, the CRAY Y-MP EL system is without memory, so is removed from service. Reloading the UNICOS operating system should not be considered a valid troubleshooting process.

File manipulation, file recovery, dump recovery, and data recovery should not be attempted without proper training.

9 FIELD REPAIR PROCEDURES

To be provided.

Cray Research, Inc.
Hardware Publications and Training
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CRAY RESEARCH, INC.

ELS Division

CRAY Y-MP EL
HARDWARE REFERENCE CARD

INSTRUCTIONS

	Instruction	CAL		Unit	Description
	000000	ERR			Error Exit
††	0010jk	CA, Aj	Ak		Set the channel (Aj) CA register to (Ak) and begin I/O sequence
	001000	PASS			Pass
††	0011jk	CL, Aj	Ak		Set the channel (Aj) CL register to (Ak)
††	0012j0	CI, Aj			Clear channel (Aj) interrupt and error flags; clear device Master Clear (output channel)
††	0012j1	MC, Aj			Clear channel (Aj) interrupt and error flags; set device Master Clear (output channel); clear device ready-hold (input channel)
††	0013j0	XA	Aj		Transmit (Aj) to XA register
††	0014j0	RT	Sj		Transmit (Sj) to RTC register
††	0014j1	SIPI Aj			Set interprocessor interrupt request to CPU (Aj)
	001401	SIPI			Set interprocessor interrupt of CPU 0
††	001402	CIPI			Clear interprocessor interrupt
††	0014j3	CLN	Aj		Transmit (Aj) to CLN register

	Instruction	CAL		Unit	Description
††	0014j4	PCI	Sj		Enter interrupt interval (II) register with (Sj)
††	001405	CCI			Clear programmable clock interrupt (PCI) request
††	001406	ECI			Enable PCI request
††	001407	DCI			Disable PCI request
	00200k	VL	Ak		Transmit (Ak) to VL register
†	002000	VL	1		Transmit 1 to VL register
	002100	EFI			Enable interrupt on floating-point error
	002200	DFI			Disable interrupt on floating-point error
	002300	ERI			Enable operand range error interrupts
	002400	DRI			Disable operand range error interrupts
	002500	DBM			Disable bidirectional memory transfers
E	002504	DCBW			Disable concurrent block write
E	002506	DSBO			Disable scalar and block overlap
	002600	EBM			Enable bidirectional memory transfers
E	002604	ECBW			Enable concurrent block write
E	002606	ESBO			Enable scalar and block overlap
	002700	CMR			Complete memory reference
	0030j0	VM	Sj		Transmit (Sj) to VM register
	003000	VM	0		Clear VM register
	0034jk	SMjk	1, TS		Test and Set semaphore jk; $0 \le jk \le 37_8$
	0036jk	SMjk	0		Clear semaphore jk; $0 \le jk \le 37_8$
	0037jk	SMjk	1		Set semaphore jk; $0 \le jk \le 37_8$
	004000	EX			Normal exit
	0050jk	J	Bjk		Jump to (Bjk)
	006ijkm	j	exp		Jump to exp = ijkm
	007ijkm	R	exp		Return jump to exp = ijkm; set B00 to (P) + 2
	010ijkm	JAZ	exp		Jump to exp = ijkm if (A0) = 0 (2^2 of i = 0)

	Instruction	CAL		Unit	Description
	011ijkm	JAN	exp		Jump to exp = ijkm if (A0) ≠ 0 (2^2 of i = 0)
	012ijkm	JAP	exp		Jump to exp = ijkm if (A0) positive (2^2 of i = 0)
	013ijkm	JAM	exp		Jump to exp = ijkm if (A0) negative (2^2 of i = 0)
	014ijkm	JSZ	exp		Jump to exp = ijkm if (S0) = 0 (2^2 of i = 0)
	015ijkm	JSN	exp		Jump to exp = ijkm if (S0) ≠ 0 (2^2 of i = 0)
	016ijkm	JSP	exp		Jump to exp = ijkm if (S0) positive (2^2 of i = 0)
	017ijkm	JSM	exp		Jump to exp = ijkm if (S0) negative (2^2 of i = 0)
	01hijkm	Ah	exp		Transmit exp = ijkm to Ah (2^2 of i = 1)
†††, X	020ijkm	Ai	exp		Transmit exp = jkm to Ai
†††, Y	020i00mn	Ai	exp		Transmit exp = nm to Ai
†††	021ijkm	Ai	exp		Transmit one's complement of exp = jkm to Ai
†††, Y	021i00mn	Ai	exp		Transmit one's complement of exp = nm to Ai
†††	022ijk	Ai	exp		Transmit exp = jk to Ai
	023ij0	Ai	Sj		Transmit (Sj) to Ai
	023i01	Ai	VL		Transmit (VL) to Ai
	024ijk	Ai	Bjk		Transmit (Bjk) to Ai
	025ijk	Bjk	Ai		Transmit (Ai) to Bjk
	026ij0	Ai	PSj	S Pop	Transmit population count of (Sj) to Ai
	026ij1	Ai	QSj	S Pop	Transmit population count parity of (Sj) to Ai
	026ij7	Ai	SBj		Transmit (SBj) to Ai
	027ij0	Ai	ZSj	S/LZ	Transmit leading zero count of (Sj) to Ai
	027ij7	SBj	Ai		Transmit (Ai) to SBj
	030ijk	Ai	Aj + Ak	A Int Add	Integer sum of (Aj) and (Ak) to Ai
†	030i0k	Ai	Ak	A Int Add	Transmit (Ak) to Ai
†	030ij0	Ai	Aj + 1	A Int Add	Transmit integer sum of (Aj) plus 1 to Ai
	031ijk	Ai	Aj – Ak	A Int Add	Integer difference of (Aj) less (Ak) to Ai

	Instruction	CAL		Unit	Description
†	031i00	Ai	–1	A Int Add	Transmit –1 to Ai (Ai = 37777777777) in Y-mode
†	031i0k	Ai	–Ak	A Int Add	Transmit the negative of (Ak) to Ai
†	031ij0	Ai	Aj –1	A Int Add	Integer difference of (Aj) less 1 to Ai
	032ijk	Ai	Aj*Ak	A Int Mult	Integer product of (Aj) and (Ak) to Ai
	033i00	Ai	CI		Transmit lowest interrupting channel number to Ai (j = 0)
	033ij0	Ai	CA, Aj		Transmit address of channel (Aj) to Ai (j ≠ 0)
	033ij1	Ai	CE, Aj		Transmit error flag of channel (Aj) to Ai (j ≠ 0)
	034ijk	Bjk, Ai	,A0	Memory	Read (Ai) words to B registers starting at Bjk from memory address ((A0) + (DBA))
†	034ijk	Bjk, Ai,	0, A0	Memory	Read (Ai) words to B registers starting at Bjk from memory address ((A0) + (DBA))
	035ijk	,A0	Bjk, Ai	Memory	Write (Ai) words from B registers Bjk to memory address ((A0) + (DBA))
†	035ijk	0, A0	Bjk, Ai	Memory	Write (Ai) words from B registers Bjk to memory address ((A0) + (DBA))
	036ijk	Tjk, Ai	,A0	Memory	Read (Ai) words to T registers starting at Tjk from memory address ((A0) + (DBA))
†	036ijk	Tjk, Ai	0, A0	Memory	Read (Ai) words to T registers starting at Tjk from memory address ((A0) + (DBA))
	037ijk	,A0	Tjk, Ai	Memory	Write (Ai) words from T registers Tjk to memory address ((A0) + (DBA))
†	037ijk	0, A0	Tjk, A1	Memory	Write (Ai) words from T registers Tjk to memory address ((A0) + (DBA))
X	040ijkm	Si	exp		Transmit exp = jkm to Si
Y	040i00mn	Si	exp		Transmit exp = nm to Si
X	041ijkm	Si	exp		Transmit one's complement of exp = jkm to Si
Y	041i00mn	Si	exp		Transmit one's complement of exp = nm to Si
	042ijk	Si	<exp	S Logical	Form one's mask exp = 100_8 – jk bits in Si from the right
†	042ijk	Si	#>exp	S Logical	Form zeroes mask exp = jk bits in Si from the left
†	042i77	Si	1	S Logical	Enter 1 into Si
†	042i00	Si	–1	S Logical	Enter –1 into Si (Si = 177777 177777 177777 177777)
	043ijk	Si	>exp	S Logical	Form one's mask exp = jk bits in Si from the left
†	043ijk	Si	#<exp	S Logical	Form zeroes mask exp = 100_8 bits in Si from the right
†	043i00	Si	0	S Logical	Clear Si
	044ijk	Si	Sj&Sk	S Logical	Logical product of (Sj) and (Sk) to Si
†	044ij0	Si	Sj&SB	S Logical	Sign bit of (Sj) to Si
†	044ij0	Si	SB&Sj	S Logical	Sign bit of (Sj) to Si (j ≠ 0)
	045ijk	Si	#Sk&Sj	S Logical	Logical product of (Sj) and one's complement of (Sk) to Si
†	045ij0	Si	#SB&Sj	S Logical	Transmit (Sj) with sign bit cleared to Si
	046ijk	Si	Sj\Sk	S Logical	Logical difference of (Sj) and (Sk) to Si
†	046ij0	Si	Sj\SB	S Logical	Toggle sign bit of (Sj), enter into Si
†	046ij0	Si	SB\Sj	S Logical	Toggle sign bit of (Sj), enter into Si (j ≠ 0)
	047ijk	Si	#Sj\Sk	S Logical	Logical equivalence of (Sk) and (Sj) to Si
†	047i0k	Si	#Sk	S Logical	Transmit one's complement of (Sk) to Si
†	047ij0	Si	#Sj\SB	S Logical	Logical equivalence of (Sj) and sign bit to Si
†	047ij0	*Si*	*#SB\Sj*	S Logical	Logical equivalence of (Sj) and sign bit to Si (j ≠ 0)
†	047i00	Si	#SB	S Logical	Transmit one's complement of sign bit into Si
	050ijk	Si	Sj|Si&Sk	S Logical	Logical product of ((Si) and (Sk) complement) ORed with logical product of ((Sj) and (Sk)) to Si *scalar merge
†	050ij0	Si	Sj|Si&SB	S Logical	Scalar merge of (Si) and sign bit of (Sj) to Si

	Instruction	CAL		Unit	Description
	051ijk	SI	Sj|Sk	S Logical	Logical sum of (Sj) and (Sk) to SI
†	051i0k	SI	Sk	S Logical	Transmit (Sk) to SI
†	051ij0	SI	Sj|SB	S Logical	Logical sum of (Sj) and sign bit to Si
†	051ij0	SI	SB|Sj	S Logical	Logical sum of (Sj) and sign bit to SI (j ≠ 0)
†	051i00	SI	SB	S Logical	Transmit sign bit into SI
	052ijk	S0	SI < exp	S Shift	Shift (SI) left exp = jk places to S0
	053ijk	S0	SI > exp	S Shift	Shift (SI) right exp = 100_8 – jk places to S0
	054ijk	SI	SI < exp	S Shift	Shift (Si) left exp = jk places to SI
	055ijk	SI	SI > exp	S Shift	Shift (SI) right exp = 100_8 – jk places to SI
	056ijk	SI	SI, Sj < Ak	S Shift	Shift (SI and Sj) left (Ak) places to SI
†	056ij0	SI	SI, Sj < 1	S Shift	Shift (SI and Sj) left one place to Si
†	056i0k	SI	SI < Ak	S Shift	Shift (SI) left (Ak) places to SI
	057ijk	SI	Sj, SI > Ak	S Shift	Shift (Sj and SI) right (Ak) places to SI
†	057ij0	SI	Sj, SI > 1	S Shift	Shift (Sj and SI) right one place to SI
†	057i0k	SI	SI > Ak	S Shift	Shift (SI) right (Ak) places to SI
	060ijk	SI	Sj + Sk	S Int Add	Integer sum of (Sj) and (Sk) to SI
†	060i0k	SI	Sk	S Int Add	Transmit (Sk) to SI
†	060ij0	SI	Sj + S0	S Int Add	Integer sum 2^{63} and (Sj) to SI
	061ijk	SI	Sj – Sk	S Int Add	Integer difference of (Sj) less (Sk) to SI
†	061i0k	SI	–Sk	S Int Add	Transmit negative of (Sk) to SI
†	061ij0	SI	Sj – S0	S Int Add	Integer difference of (Sj) less 2^{63} to SI
	062ijk	SI	Sj – FSk	Fp Add	Floating-point sum of (Sj) and (Sk) to SI
†	062i0k	SI	+FSk	Fp Add	Normalize (Sk) to SI
	063ijk	SI	Sj – FSk	Fp Add	Floating-point difference of (Sj) and (Sk) to SI
†	063i0k	SI	–FSk	Fp Add	Transmit normalized negative of (Sk) to Si
	064ijk	SI	Sj * FSk	Fp Mult	Floating-point product of (Sj) and (Sk) to SI
	065ijk	SI	Sj * HSk	Fp Mult	Half-precision rounded floating-point product of (Sj) and (Sk) to Si
	066ijk	SI	Sj * RSk	Fp Mult	Full-precision rounded floating-point product of (Sj) and (Sk) to SI
	067ijk	SI	Sj * ISk	Fp Mult	Two minus the floating-point product of (Sj) and (Sk) to SI
	070ij0	SI	/HSj	Fp Recp	Floating-point reciprocal approximation of (Sj) to SI
	071i0k	SI	Ak		Transmit (Ak) to SI with no sign extension
	071i1k	SI	+Ak		Transmit (Ak) to SI with sign extension
	071i2k	SI	+Fak		Transmit (Ak) to SI as unnormalized floating-point number (exponent = 40060)
	071i30	SI	0.6		Transmit constant 0.75 x 2^{48} to SI (SI = 040060 140000 000000 000000)
	071i40	SI	0.4		Transmit constant 0.5 to SI (SI = 040000 100000 000000 000000)
	071i50	SI	1.0		Transmit constant 1.0 to SI (SI = 040001 100000 000000 000000)
	071i60	SI	2.0		Transmit constant 2.0 to SI (SI = 040002 100000 000000 000000)
	071i70	SI	4.0		Transmit constant 4.0 to SI (SI = 040003 100000 000000 000000)
	072i00	SI	RT		Transmit (RTC) to SI
	072i02	SI	SM		Transmit (SM) to SI
	072ij3	SI	STj		Transmit (STj) to SI
	073i00	SI	VM		Transmit (VM) to SI
	073i01	SI	SRj		Transmit status register (SRj) bits to SI
	073i11	¶¶			Read performance counter to SI
	073i31	¶¶			Clear memory maintenance modes and read status register into SI
	073i02	SM	SI		Transmit (SI) to SM
	0731j3	STj	SI		Transmit (SI) to STj
	074ijk	SI	Tjk		Transmit (Tjk) to SI
	075ijk	Tjk	SI		Transmit (SI) to Tjk
	076ijk	SI	Vj,Ak		Transmit (Vj, element (Ak)) to SI

	Instruction	CAL		Unit	Description
	077ijk	Vi,Ak	Sj		Transmit (Sj) to Vi element (Ak)
†	077i0k	Vi,Ak	0		Clear Vi element (Ak)
	10hijkm	Ai	exp,Ah	Memory	Read from memory address ((Ah) + jkm + (DBA)) to Ai (h ≠ 0)
Y	10hi00mn	Ai	exp,Ah	Memory	Read from memory address ((Ah) + nm + (DBA)) to Ai (h ≠ 0)
†, X	100ijkm	Ai	exp,0	Memory	Read from memory address (jkm + (DBA)) to Ai
Y	100i00mn	Ai	exp,0	Memory	Read from memory address (nm + (DBA)) to Ai
†, X	100ijkm	Ai	exp,	Memory	Read from memory address (jkm + (DBA)) to Ai
Y	100i00mn	Ai	exp,	Memory	Read from memory address (nm + (DBA)) to Ai
†, X	10hi000	Ai	,Ah	Memory	Read from memory address ((Ah) + (DBA)) to Ai (h ≠ 0)
Y	10hi0000	Ai	,Ah	Memory	Read from memory address ((Ah + (DBA)) to Ai (h ≠ 0)
X	11hijkm	exp,Ah	Ai	Memory	Write (Ai) to memory address ((Ah) + jkm + (DBA)) (h ≠ 0)
Y	11hi00mn	exp,Ah	Ai	Memory	Write (Ai) to memory address ((Ah) + nm + (DBA)) (Ah ≠ 0)
†, X	110ijkm	exp,0	Ai	Memory	Write (Ai) to memory address (jkm + (DBA))
Y	110i00mn	exp,0	Ai	Memory	Write (Ai) to memory address (nm + (DBA))
†, X	110ijkm	exp,	Ai	Memory	Write (Ai) to memory address (jkm + (DBA))
Y	110i00mn	exp,	Ai	Memory	Write (Ai) to memory address (nm + (DBA))
†, X	11hi000	,Ah	Ai	Memory	Write (Ai) to memory address ((Ah) + (DBA)) (h ≠ 0)
Y	11hi0000	,Ah	Ai	Memory	Write (Ai) to memory address ((Ah + (DBA)) (h ≠ 0)
X	12hijkm	Si	exp,Ah	Memory	Read from memory address ((Ah) + jkm + (DBA)) to Si (h ≠ 0)
Y	12hi00mn	Si	exp,Ah	Memory	Read from memory address ((Ah) + nm + (DBA)) to Si (h ≠ 0)
X	120ijkm	Si	exp,0	Memory	Read from memory address (jkm + (DBA)) to Si
Y	120i00mn	Si	exp,0	Memory	Read from memory address (nm + (DBA)) to Si
†, X	120ijkm	Si	exp,	Memory	Read from memory address (jkm + (DBA)) to Si
Y	120i00mn	Si	exp,	Memory	Read from memory address (nm + (DBA)) to Si
†, X	12hi000	Si	,Ah	Memory	Read from memory address ((Ah) + (DBA)) to Si (h ≠ 0)
Y	12hi0000	Si	,Ah	Memory	Read from memory address ((Ah) + (DBA)) to Si (h ≠ 0)
X	13hijkm	exp,Ah	Si	Memory	Write (Si) to memory address ((Ah) + jkm + (DBA)) (h ≠ 0)
Y	13hi00mn	exp,Ah	Si	Memory	Write (Si) to memory address ((Ah) + nm + (DBA)) (h ≠ 0)
†, X	130ijkm	exp,0	Si	Memory	Write (Si) to memory address (jkm + (DBA))
Y	130i00mn	exp,0	Si	Memory	Write (Si) to memory address (nm + (DBA))
X	130ijkm	exp,	Si	Memory	Write (Si) to memory address (jkm + (DBA))
Y	130i00mn	exp,	Si	Memory	Write (Si) to memory address (nm + (DBA))
X	13hi000	,Ah	Si	Memory	Write (Si) to memory address ((Ah) + (DBA)) (h ≠ 0)
Y	13hi0000	,Ah	Si	Memory	Write (Si) to memory address ((Ah) + (DBA)) (h ≠ 0)
	140ijk	Vi	Sj&Vk	V logical	Logical products of (Sj) and (Vk) to Vi
	141ijk	Vi	Vj&Vk	V logical	Logical products of (Vj) and (Vk) to Vi
	142ijk	Vi	Sj|Vk	V logical	Logical sums of (Sj) and (Vk) to Vi
†	142i0k	Vi	Vk	V logical	Transmit (Vk) to Vi
	143ijk	Vi	Vj|Vk	V logical	Logical sums of (Vj) and (Vk) to Vi
	144ijk	Vi	Sj\Vk	V logical	Logical differences of (Sj) and (Vk) to Vi

	Instruction	CAL		Unit	Description
	145ijk	Vi	Vj\Vk	V logical	Logical differences of (Vj) and (Vk) to Vi
†	145iil	Vi	0	V logical	Clear Vi
	146ijk	Vi	Sj| Vk&VM	V logical	Transmit (Sj) if VM bit = 1; (Vk) if VM bit = 0 to Vi *scalar *vector merge
†	146i0k	Vi	#VM&Vk	V logical	Vector merge of (Vk) and 0 to Vi
	147ijk	Vi	Vj| Vk&VM	V logical	Transmit (Vj) if VM bit = 1; (Vk) if VM bit = 0 to Vi *vector *vector merge
	150ijk	Vi	Vj < Ak	V Shift	Shift (Vj) left (Ak) places to Vi
	150ij0	Vi	Vj < 1	V Shift	Shift (Vj) left one place to Vi
	151ijk	Vi	Vj > Ak	V Shift	Shift (Vj) right (Ak) places to Vi
	151ij0	Vi	Vj > 1	V Shift	Shift (Vj) right one place to Vi
	152ijk	Vi	Vj,Vj < Ak	V Shift	Double shift (Vj) left (Ak) places to Vi
†	152ij0	Vi	Vj,Vj < 1	V Shift	Double shift (Vj) left one place to Vi
	153ijk	Vi	Vj,Vj > Ak	V Shift	Double shift (Vj) right (Ak) places to Vi
	153ij0	Vi	Vj,Vj > 1	V Shift	Double shift (Vj) right one place to Vi
	154ijk	Vi	Sj + Vk	V Int Add	Integer sums of (Sj) and (Vk) to Vi
	155ijk	Vi	Vj + Vk	V Int Add	Integer sums of (Vj) and (Vk) to Vi
	156ijk	Vi	Sj – Vk	V Int Add	Integer differences of (Sj) and (Vk) to Vi
	156i0k	Vi	–Vk	V Int Add	Transmit negative of (Vk) to Vi
	157ijk	Vi	Vj – Vk	V Int Add	Integer differences of (Vj) and (Vk) to Vi
	160ijk	Vi	Sj * FVk	Fp Mult	Floating-point products of (Sj) and (Vk) to Vi
	161ijk	Vi	Vj * FVk	Fp Mult	Floating-point products of (Vj) and (Vk) to Vi
	162ijk	Vi	Sj * HVk	Fp Mult	Half-precision rounded floating-point products of (Sj) and (Vk) to Vi
	163ijk	Vi	VJ * HVk	Fp Mult	Half-precision rounded floating-point products of (Vj) and (Vk) to Vi
	164ijk	Vi	Sj * RVk	Fp Mult	Rounded floating-point products of (Sj) and (Vk) to Vi
	165ijk	Vi	Vj * RVk	Fp Mult	Rounded floating-point products of (Vj) and (Vk) to Vi
X	166ijk	Vi	Sj * IVk	Fp Mult	Two minus the floating-point products of (Sj) and (Vk) to Vi
Y	166ijk	Vi	Sj * Vk	Fp Mult	32-bit integer products of (Sj) and (Vk) to Vi
	167ijk	Vi	Vj * IVk	Fp Mult	Two minus the floating-point products of (Vj) and (Vk) to Vi
	170ijk	Vi	Sj + FVk	Fp Add	Floating-point sums of (Sj) and (Vk) to Vi
†	170i0k	Vi	+FVk	Fp Add	Normalize (Vk) to Vi
	171ijk	Vi	Vj + FVk	Fp Add	Floating-point sums of (Vj) and (Vk) to Vi
	172ijk	Vi	Sj – FVk	Fp Add	Floating-point differences of (Sj) and (Vk) to Vi
†	172i0k	Vi	–FVk	Fp Add	Transmit normalized negatives of (Vk) to Vi
	173ijk	Vi	Vj – FVk	Fp Add	Floating-point differences of (Vj) and (Vk) to Vi
	174ij0	Vi	/HVj	Fp Recp	Floating-point reciprocal approximations of (Vj) to Vi
	174ij1	Vi	PVj	V pop	Population counts of (Vj) to Vi
	174ij2	Vi	QVj	V pop	Population count parities of (Vj) to Vi
	1750j0	VM	Vj,Z	V logical	VM = 1 if (Vj) = 0
	1750j1	VM	Vj,N	V logical	VM = 1 if (Vj) ≠ 0
	1750j2	VM	Vj,P	V logical	VM = 1 if (Vj) positive; 0 is positive
	1750j3	VM	Vj,M	V logical	VM = 1 if (Vj) negative; 1 is negative
	175ij4	Vi,VM	Vj,Z	V logical	VM bit = 1 if (Vj) element) = 0 and element index is loaded into (compressed Vi)
	175ij5	Vi,VM	Vj,N	V logical	VM bit = 1 if (Vj) element) ≠ 0 and element index is loaded into (compressed Vi)
	175ij6	Vi,VM	Vj,P	V logical	VM bit = 1 if (Vj) element) ≥ 0 and element index is loaded into (compressed Vi)

Instruction	CAL		Unit	Description
175ij7	Vi,VM	Vj,M	V logical	VM bit = 1 if (Vj element) < 0 and element index is loaded into (compressed Vi)
176i0k	Vi	A0,Ak	Memory	Read (VL) words to Vi from memory address ((A0) + (DBA)) incremented by (Ak)
176i00	Vi	A0,1	Memory	Read (VL) words to Vi from memory address ((A0 + (DBA)) incremented by 1
176i1k	Vi	A0,Vk	Memory	Read (VL) words to Vi from memory address ((A0 + (Vk) + (DBA)) *gather
1770jk	,A0,Ak	Vj	Memory	Write (VL) words from Vj to memory address ((A0) + (DBA)) incremented by (Ak)
1770j0	,A0, 1	Vj	Memory	Write (VL) words from Vj to memory address ((A0) + (DBA)) incremented by 1
1771jk	,A0,Vk	Vj	Memory	Write (VL) words from Vj to memory address ((A0) + (Vk) + (DBA)) *scatter

† – Special syntax mode
†† – Priviledged to monitor mode
††† – Generated depending on exp.
¶¶ – Not supported by CAL version 2
X – X-mode instruction
Y – Y-mode instruction
( ) – Read as *the contents of ...*

Register	Value
Ah, h = 0	0
Ai, i = 0	(A0)
Aj, j = 0	0
Ak, k = 0	1
Si, i = 0	(S0)
Sj, j = 0	0
Sk, k = 0	2^{63}

Revision	Date	Changes made
A	6/28/91	Added Console Interrupt Vector. Added jumper selectable addressing range map. Changed UNUSED to GND on Y1BUS except P1-31,32. Added VME read parity error and console interrupt to status register. Removed Y1 Clock. Modified block diagrams

Table of Contents

2.0 Definition of Terms

IOBB :
Input/Output Buffer Board, a board in the IOS which serves as a buffer and communication path between devices on the VMEbus and the CC.

CC :
Channel Controller, an ASIC in the Y-MP EL CPU which has the intelligence to carry out actual data transfers between IOBB and Y-MP EL memory. There are up to two Y1BUS interfaces on each CC ASIC.

IOS :
IO Subsystem, refers to the contents of a single VME rack and any related peripherals. Each IOS contains a minimum of an MIOP and an IOBB. There can be up to 16 IOSs in a Y-MP EL. An IOS can be configured as a 4, 6, or 10 slot VME rack.

IOTCB :
IO Task Control Block, used by the MIOP to request a data transfer between Y-MP EL memory and IOBB (to be interpreted by CC).

MIOP - Master IO Processor, refers to the CPU card in an IOS.

Y1BUS - A Cray Research proprietary bus which connects the IOBB and CC(YC) together.

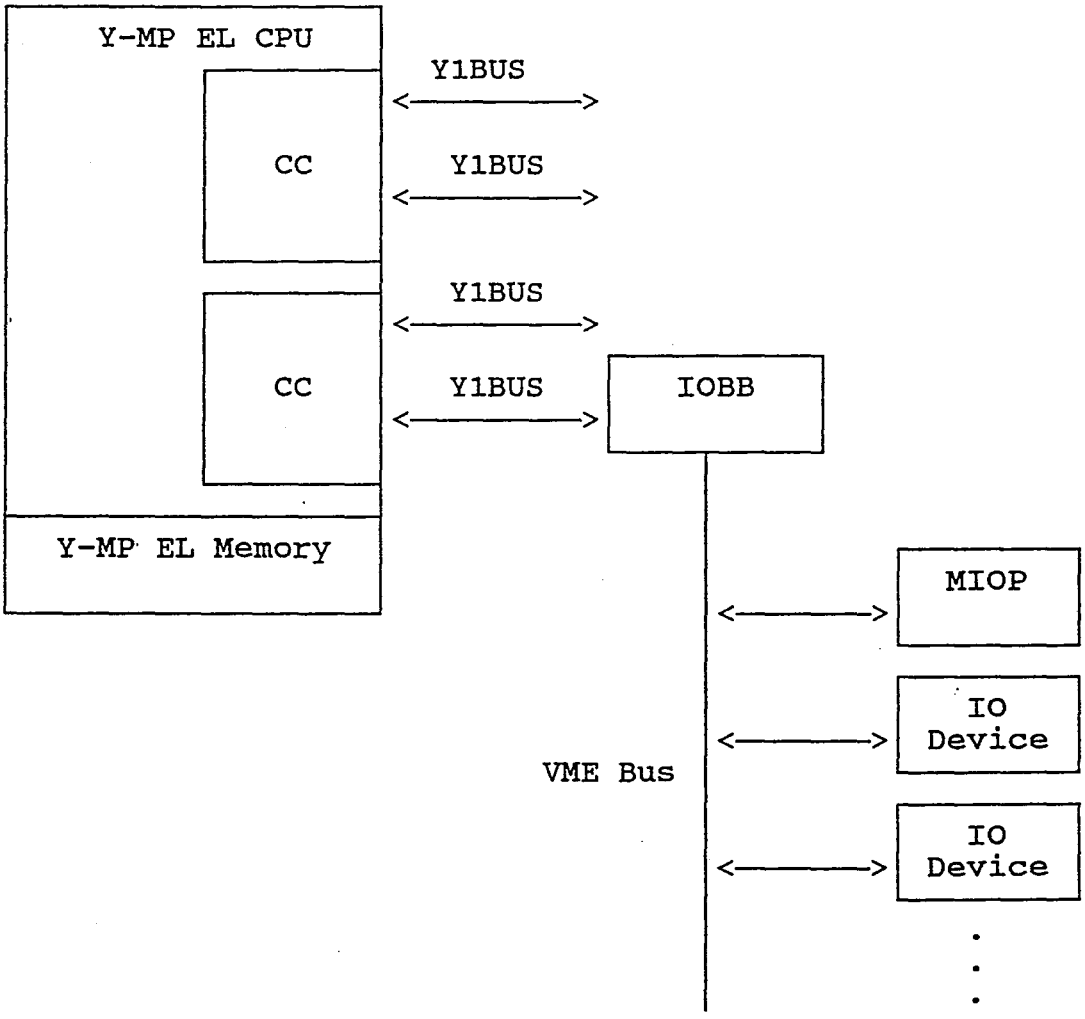
YC :
Y-MP EL Channel, the circuitry within the CC which connects a Y1BUS to Y-MP EL memory, there are two YCs in a CC.

CB :
Control Block, a general term, refers to control information sent by the Y-MP EL CPU to the IOS.

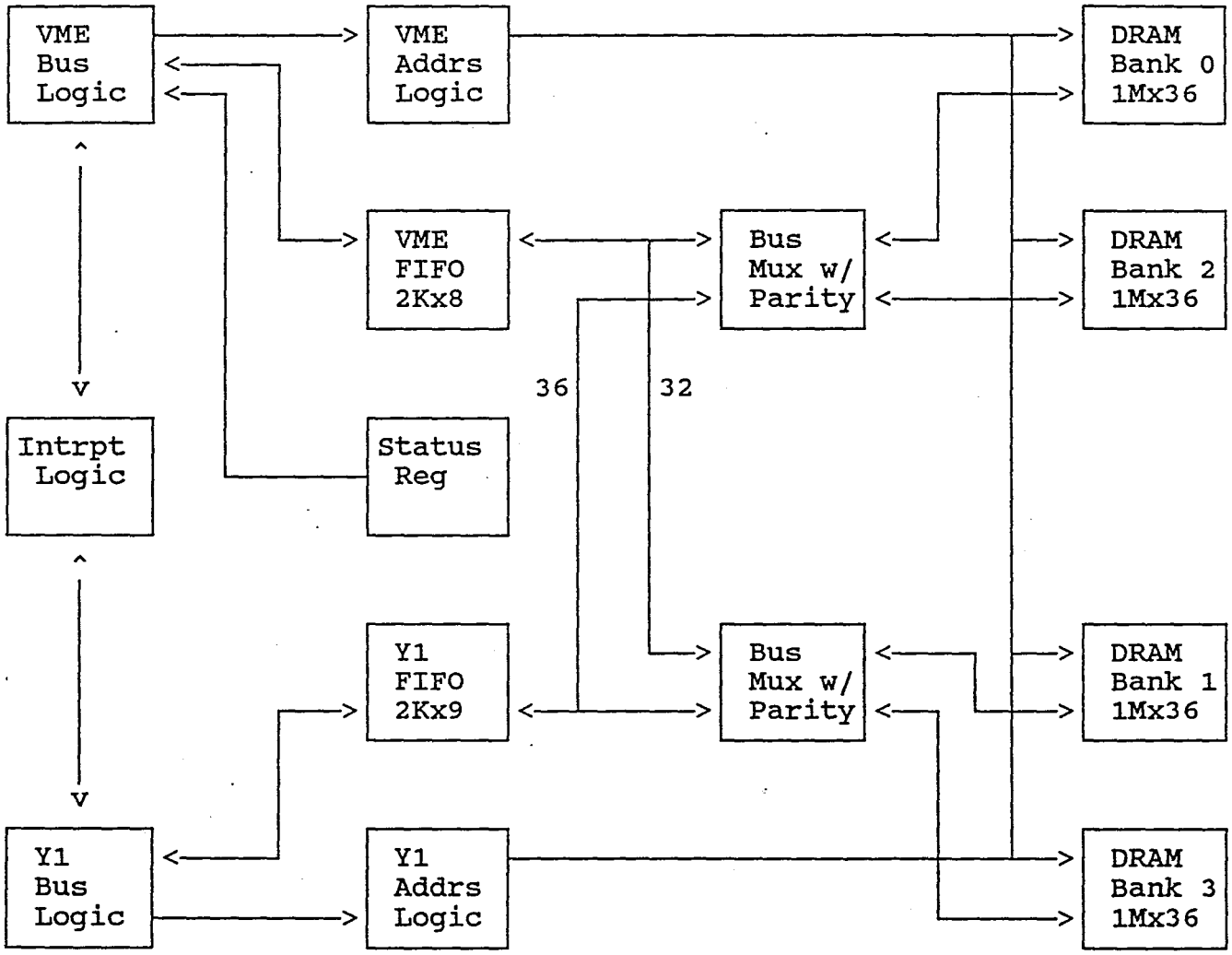
RSB :
Return Status Block, a general term, refers to status information sent back from IOS to Y-MP EL CPU in response to a CB.

2.0 Input Output Buffer Board (IOBB) Overview

The IOBB is a VME 6U x 160mm board that provides a buffer memory and a communication path between a Y-MP EL CPU and a Y-MP EL IOS. Each Y-MP EL CPU contains two Channel Controller (CC) ASICs. Each CC contains two Y1BUS interfaces. Therefore each Y-MP EL CPU contains four Y1BUS interfaces. A Y-MP EL IO Subsystem (IOS) is VME based and contains the IO device controllers for disk drives, tape drives, network interfaces etc. The IOBB provides an interface between the Y1BUS and the VME bus. For data transfers between the VME Bus and Y1BUS, data only travels across the VME Bus once. Data travels from an IO device across the VME Bus to IOBB memory, and then directly from IOBB memory to Y-MP EL memory via Y1BUS, and vice versa. The communication path is implemented using interrupts in both directions. Following is a general block diagram that shows how the IOBB fits into the Y-MP EL System.



A general block diagram of the IOBB follows.

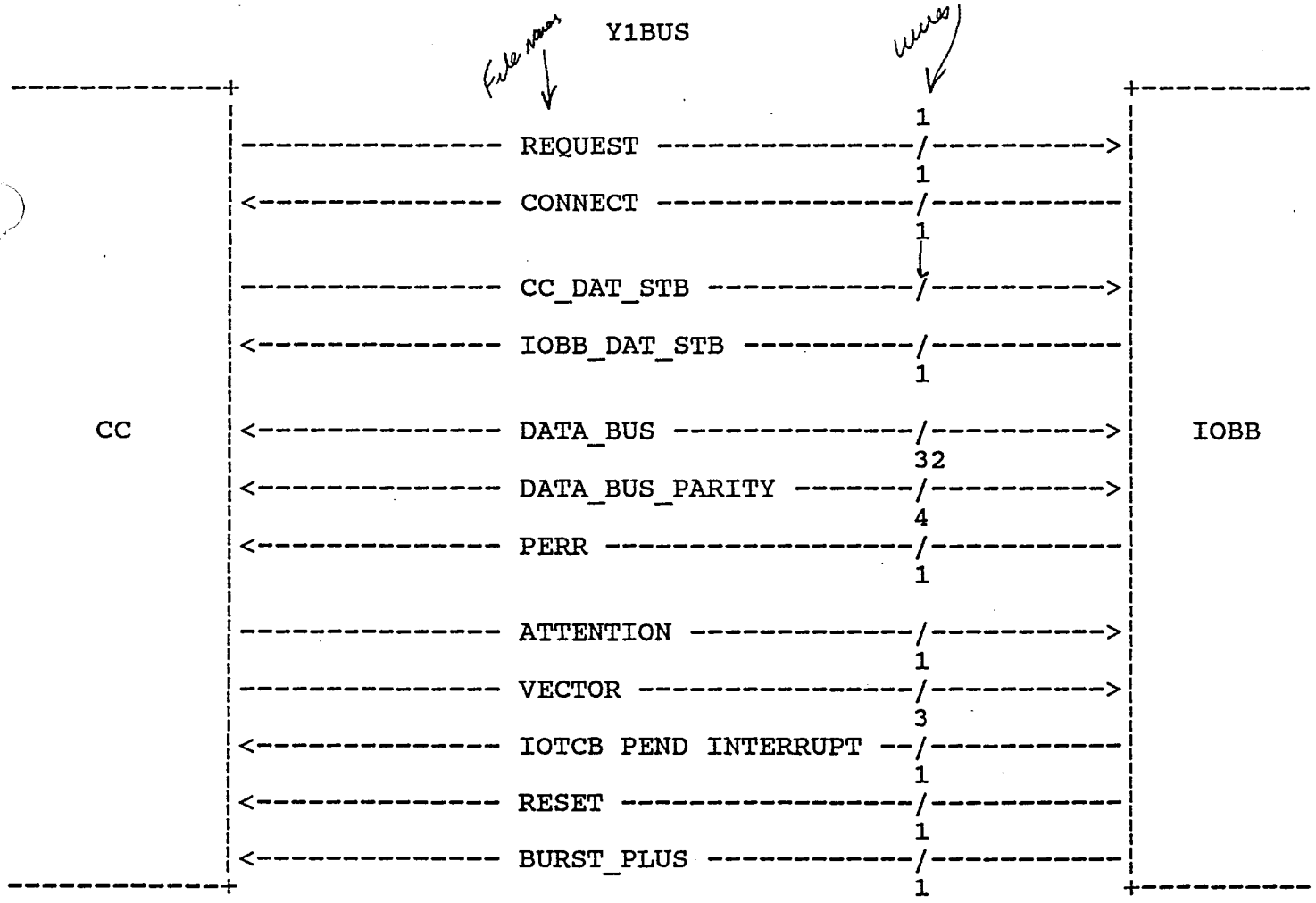


3.0 Y1BUS Interface

The Y1BUS is used to transfer data at high speed over long distance between IOBB and CC. Characteristics of the Y1BUS include :

1) Point-to-point connection with the IOBB side being a slave memory.
2) Data bus is bidirectional, 32-bits wide and has byte parity.
3) Address, control and data are time multiplexed using the single 32-bit data bus.
4) Data bursts can be 4, 32, 64, or 128 32-bit words long.
5) Maximum burst rate is 80 MB/sec.
6) Maximum cable length is 50 ft.
7) Capable of passing interrupts in both directions at any time (independent of data transfers).
8) All signals are differential for high noise immunity.

3.1 Signal Descriptions



REQUEST (active high) :
When the CC wants to communicate to the IOBB, it places the following information on the DATA_BUS :

Bits	Definition
21:0	IOBB memory address (addresses 4M 32 bit words)
28:22	Reserved (driven low).
30:29	00 = 32 word data burst. 01 = 64 word data burst. 10 = 128 word data burst. 11 = 4 word burst.
31	1 = Data transfer from CC to IOBB (write). 0 = Data transfer from IOBB to CC (read).

The CC then asserts REQUEST after this information has been valid on the DATA_BUS for 50ns minimum. This information should remain valid on the DATA_BUS until the IOBB asserts CONNECT. The IOBB can therefore use the rising edge of REQUEST to latch the information. REQUEST can be re-asserted only when CONNECT has been negated. Each REQUEST and CONNECT sequence can transfer a burst of 4, 32, 64, or 128 32-bit words of data.

CONNECT (active high) :
IOBB responds to a REQUEST by asserting CONNECT to indicate that the address, direction and burst size are latched. CC should keep the address and direction on the bus until CONNECT is asserted by the IOBB. REQUEST and CONNECT should remain asserted for the duration of the transfer except on reads where the CC may drop the REQUEST after receiveing a CONNECT from the IOBB. At the end of a write the CC should negate the REQUEST signal. IOBB will respond by negating the CONNECT signal when it also detects the end of transfer.

CC_DAT_STB (active high) :
CC_DAT_STB is used to send data from the CC to the IOBB. After connection is established by REQUEST and CONNECT and the transfer is from CC to IOBB, 4, 32, 64, or 128 CC_DAT_STB pulses (a burst of data) should be sent to the IOBB. The maximum frequency of the CC_DAT_STB is one pulse every 50ns making the maximum burst transfer rate 80 Mbytes/sec. If the data transfer ends at a non-burst boundary, the last burst will be less than 4, 32, 64, or 128 words.

BURST_PLUS (active high) :
When BURST_PLUS is asserted, it informs the CC that the new IOBB is present so that faster burst transfer rates are possible and that burst lengths of 4, 32, 64, and 128 words are supported.

IOBB_DAT_STB (active high):
IOBB_DAT_STB is used to send data from the IOBB to the CC. After connection is established by REQUEST and CONNECT and the transfer is from IOBB to CC, 4, 32, 64, or 128 IOBB_DAT_STB pulses should be sent to the CC. The maximum frequency of the IOBB_DAT_STB is one pulse every 50ns making the maximum burst transfer rate 80 Mbytes/sec.

DATA_BUS and DATA_BUS_PARITY (active high):
The DATA_BUS is a 32 bit bidirectional data bus with odd byte parity. P3 is for bits 31:24, P2 is for bits 23:16, P1 is for bits 15:8, and P0 is for bits 7:0. Data, address, direction and burst lentgh information is transfered via the DATA_BUS. IOBB should always be in the receiving mode unless it is ready to transfer data to CC.

PERR (active high):
IOBB uses this signal to report a parity error of address or data to the CC. IOBB sends the PERR pulse whenever it detects a parity error during the data or address transfer sequence. CC will not terminate the transfer when a parity error is detected. When address parity error is detected in the IOBB, CC will continue with the sequence of data transfers, but IOBB must not write the data into its memory.

ATTENTION and VECTOR (active high):
ATTENTION is the interrupt signal from CC to IOBB. The three VECTOR bits indicate the reason for the interrupt. They are defined as follows:

VECTOR <2>	VECTOR <1>	VECTOR <0>	Cause for the interrupt
1	1	1	Console interrupt.
1	1	0	CA is loaded to the input channel (ready to receive RSB).
1	0	1	CA is loaded to the output channel (CB pending).
1	0	0	Reset opcode is received in the output channel.
0	1	1	IOTCB done.
0	1	0	IOTCB fetch error.
0	0	1	IOTCB execution error.
0	0	0	Not used.

CC may send consecutive interrupts to the IOBB at a rate of one pulse (50ns) every 330ns. IOBB should save the interrupts and vectors in the status register for the MIOP to look at.

IOTCB PEND INTERRUPT (active high):
When an IOTCB is ready in the IOBB memory, IOBB will interrupt the CC. The interrupt is a pulse 50ns(min) wide. CC can queue up to 7 IOTCB PEND interrupt pulses without responding to them.

RESET (active high):
RESET will reset the Y-MP EL channel which the MIOP is connected to. This can be used to force CC to look for the next IOTCB at location zero of the IOBB memory.

3.2 Y1BUS pin assignments

The IOBB interfaces to the Y1BUS thru two 60 pin connectors on the front panel of the board, P1 and P2. The pin assignments are as follows :

P1 Pin	Signal Name	P1 Pin	Signal Name
1	BURSTPLUS	31	UNUSED
2	GND	32	UNUSED
3	GND	33	DB12P
4	GND	34	DB12N
5	DB00P	35	DB13P
6	DB00N	36	DB13N
7	DB01P	37	DB14P
8	DB01N	38	DB14N
9	DB02P	39	GND
10	DB02N	40	GND
11	DB03P	41	DB15P
12	DB03N	42	DB15N
13	DB04P	43	DB16P
14	DB04N	44	DB16N
15	DB05P	45	DB17P
16	DB05N	46	DB17N
17	DB06P	47	DB18P
18	DB06N	48	DB18N
19	DB07P	49	DB19P
20	DB07N	50	DB19N
21	GND	51	DB20P
22	GND	52	DB20N
23	DB08P	53	DB21P
24	DB08N	54	DB21N
25	DB09P	55	DB22P
26	DB09N	56	DB22N
27	DB10P	57	GND
28	DB10N	58	GND
29	DB11P	59	GND
30	DB11N	60	GND

P2 Pin	Signal Name	P2 Pin	Signal Name
1	GND	31	RESET
2	GND	32	GND
3	GND	33	DBP3P
4	GND	34	DBP3N
5	DB23P	35	IOCCDRDYP
6	DB23N	36	IOCCDRDYN
7	DB24P	37	IOBBDRDYP
8	DB24N	38	IOBBDRDYN
9	DB25P	39	GND
10	DB25N	40	GND
11	DB26P	41	REQP
12	DB26N	42	REQN
13	DB27P	43	CONNP
14	DB27N	44	CONNN
15	DB28P	45	TCBPENDP
16	DB28N	46	TCBPENDN
17	DB29P	47	PERRP
18	DB29N	48	PERRN
19	DB30P	49	VECT2P
20	DB30N	50	VECT2N
21	GND	51	VECT1P
22	GND	52	VECT1N
23	DB31P	53	VECT0P
24	DB31N	54	VECT0N
25	DBP0P	55	ATTNP
26	DBP0N	56	ATTNN
27	DBP1P	57	GND
28	DBP1N	58	GND
29	DBP2P	59	GND
30	DBP2N	60	GND

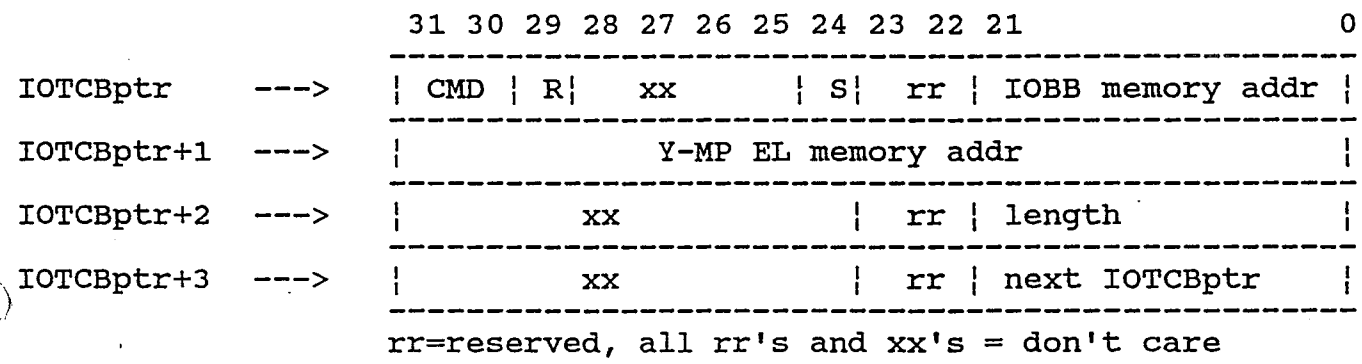
3.3 Timing Diagrams

4.0 Y1BUS Channel Operations

The Y-MP EL system has two types of logical channels, command and data. Y-MP EL CPU instructions control Command Input and Command Output channels. The Y-MP EL CPU uses Output Channels to send commands to the IOS and Input Channels to receive status from the IOS. Data Channels are controlled by the IOS. The IOS uses Data Channels to transfer data between Y-MP EL memory and IOBB memory.

All of the actual channel operations are initiated by the MIOP in the form of IOTCBs. The MIOP has to set up an IOTCB in IOBB memory for every transfer between Y-MP EL memory and IOBB (maximum of 7 outstanding IOTCBs allowed). There are two types of IOTCB's. There is an IO IOTCB (S=0) and a console IOTCB (S=1). The format of the two IOTCBs follows :

Format of an IO IOTCB (S=0) :



CMD = 00 : Input Command Channel
      01 : Output Command Channel
      10 : Data Channel Input (from IOS to Y-MP EL CPU)
      11 : Data Channel Output (from Y-MP EL CPU to IOS)
  R = 0 : no retry
       1 : automatic hardware retry, 1 time

IOBB memory addr :
This is the starting address in IOBB memory where data should be read from or written to. 22 bits can address up to 4M 32-bit words (16 Mbytes) of IOBB memory. Note that the "IOBB memory addr" is a 32-bit word address, and must be divisable by 32 (i.e.<4:0> = 00000) for a 32, 64, and 128 word burst.

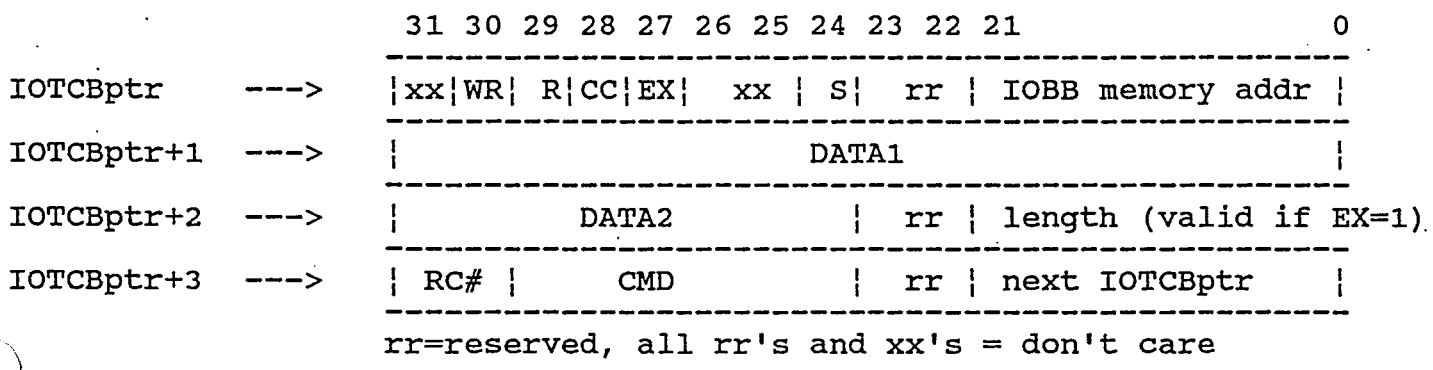
Y-MP EL memory addr :
Starting address in Y-MP EL memory where data should be read from or written to. This field is ignored by the CC if CMD=0x.

length :
The number of 32-bit words to be transfered, limited by the total amount of memory on IOBB. The length must be even (i.e. CC ignores bit<0>). This field is ignored by the CC if CMD = 0X.

next IOTCBptr :
An IOBB memory address where the next IOTCB resides. Note that the "next IOTCBptr" is a 32-bit word address, and must be divisible by 4 (i.e. <1:0> = 00).

Note: length=0 means noop (data channel only), however, IOTCBptr will get loaded and completion interrupt will be generated normally.

Format of a console IOTCB (S=1) :



RC# = 00 : Command is for RC chip of processor number 0.
= 01 : Command is for RC chip of processor number 1.
= 10 : Command is for RC chip of processor number 2.
= 11 : Command is for RC chip of processor number 3.
CC = 1 : Local operation (local to CC), no need to initiate any CONBUS cycles.
EX = 1 : Extra data, the following fields are valid :
IOBB memory addr - starting address.
length - number of 32 bit words transferred.
WR=0 - read from IOBB.
WR=1 - write to IOBB.
R = 0 : no retry (same as IO IOTCB).
= 1 : automatic hardware retry, one time.

All memory operations still use normal IO IOTCBs.

4.1 Command Input Channel

There are 5 registers in the CC associated with each Input Channel :
CA - Channel address, starting memory address in Y-MP EL memory.
CL - Channel limit, ending memory address in Y-MP EL memory.
CE - Channel error flag.
CI - Channel interrupt flag.
C# - Channel number.

Following is the operating sequence of an Input Channel :
1) Y-MP EL CPU loads CL.
2) Y-MP EL CPU loads CA, the corresponding Input Channel (C#) is opened.
3) CC sends a "ready to receive RSB" interrupt to MIOP via IOBB.
4) MIOP sets up a Return Status Block (RSB) in IOBB memory.
5) MIOP sets up an IOTCB (CMD=00, IOBB memory address=starting address of RSB to be read).
6) MIOP sends an "IOTCB pending" interrupt to CC via IOBB.
7) CC fetches IOTCB (pointed to by IOTCBptr), picks up IOBB memory address, uses CA and CL instead of Y-MP EL memory address from IOTCB, and completes the transfer.
8) CC interrupts Y-MP EL CPU when CA=CL.
9) CC sends a "IOTCB done" interrupt to MIOP via IOBB.

4.2 Command Output Channel

There are 5 registers in CC associated with each Output Channel :
CA - Channel address, starting memory address in Y-MP EL memory.
CL - Channel limit, ending memory address in Y-MP EL memory.
CE - Channel error flag.
CI - Channel interrupt flag.
C# - Channel number.

Following is the operating sequence of an Output Channel :
1) Y-MP EL CPU sets up a Control Block (CB) in Y-MP EL memory.
2) Y-MP EL CPU loads CL.
3) Y-MP EL CPU loads CA, the corresponding Output Channel (C#) is opened.
4) CC sends a "CB pending" interrupt to MIOP via IOBB.
5) MIOP sets up an IOTCB (CMD=01, IOBB memory address=starting address for loading CB).
6) MIOP sends an "IOTCB pending" interrupt to CC via IOBB.
7) CC fetches IOTCB (pointed to by IOTCBptr), picks up IOBB memory address, uses CA and CL instead of Y-MP EL memory address from IOTCB, and completes the transfer.
8) CC interrupts Y-MP EL CPU when CA=CL.
9) CC sends an "IOTCB done" interrupt to MIOP via IOBB.

4.3 Data Channel (Input and Output)

Following is the operating sequence of a Data Channel :
1) MIOP sets up an IOTCB (CMD=10 or 11, ...).
2) MIOP sends an "IOTCB pending" interrupt to CC via IOBB.
3) CC fetches IOTCB (pointed to by IOTCBptr), picks up all parameters from IOTCB, and completes the transfer.
4) CC sends an "IOTCB done" interrupt to MIOP via IOBB.

4.4 YC Control

Each YC is bascially an "IOTCB processor". It accesses IOBB memory twice for every IOTCB. First it fetchs the IOTCB itself, then it executes the request contained in the IOTCB. The YC is the master on the Y1BUS. It handles interrupts to and from the Y1BUS, and accesses Y-MP EL memory.

Following is a summary of the different types of interrupts on the Y1BUS.

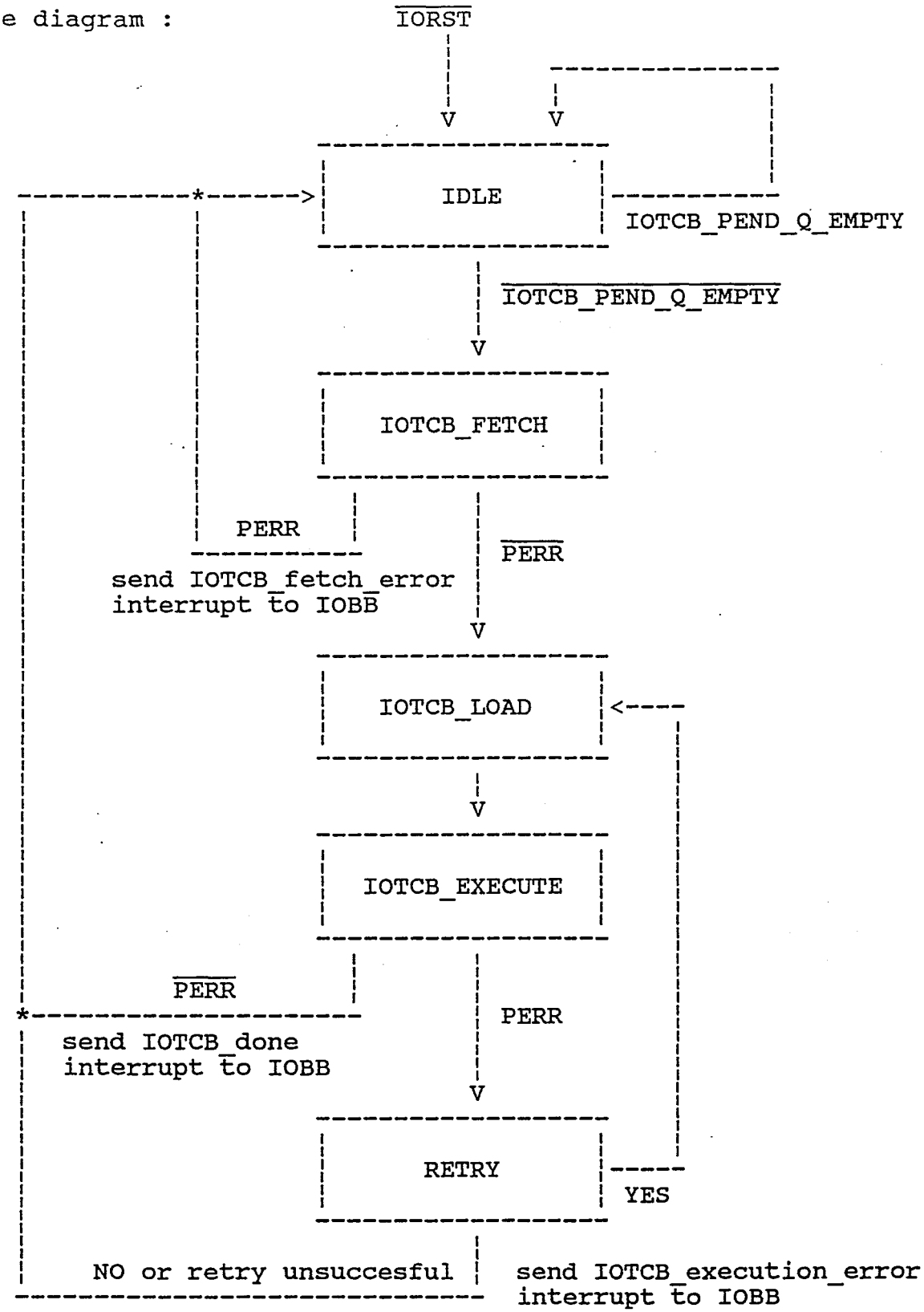
Interrupts from IOBB to YC :
1) IOTCB pending - an IOTCB is ready in IOBB memory. (IOTCBptr always points to the next pending IOTCB).

Interrupts from YC to IOBB :
1) Ready to receive RSB - An Input Command Channel has been opened.
2) CB pending - An Output Command Channel has been opened.
3) Reset - Resets channel.
4) IOTCB done - The task specified by the IOTCB has been completed successfully.
5) IOTCB fetch error - Parity error detected when fetching IOTCB.
6) IOTCB execution error - Parity error detected during IOTCB execution.

The YC Control has 4 basic states, IDLE, IOTCB_FETCH, IOTCB_LOAD, and IOTCB_EXECUTE (refer to state diagram on next page). After IO Reset, YC is in IDLE state, and IOTCBptr is forced to zero, which is the beginning of the IOTCB chain. The "IOTCB pending queue" is empty and YC is waiting for the first "IOTCB pending interrupt" from IOBB. When the "IOTCB pending queue" is not empty, YC goes into IOTCB_FETCH state. An IOTCB pointed to by IOTCBptr register is fetched from IOBB memory. YC then goes into IOTCB_LOAD state, which sets up the control registers in the YC according to the newly fetched IOTCB. Finally, YC goes into IOTCB_EXECUTE state. Y-MP EL memory and IOBB memory accesses are generated accordingly. When the transfer is done, an "IOTCB done" interrupt will be sent to IOBB.

To correctly use the hardware, the MIOP must place the first IOTCB at location zero of IOBB memory. Each subsequent IOTCB must have IOTCBptr pointing to the next IOTCB. It is OK for the MIOP to send "IOTCB pending" interrupts any time as long as there are less then 7 IOTCBs outstanding. For best performance, it is recommended that IOTCBs be stacked up so that YC can start fetching the next IOTCB immediately after the current one is finished.

A YC state diagram :



7.5 Error Handling

Error detection is only applicable to parity across the data bus portion of the Y1BUS (data, as well as address & control, are multiplexed onto the 32-bit data bus, see section 3.0). Therefore, all errors are parity errors occuring on different instances across the Y1BUS. Parity errors can be divided into two catagories, errors associated with IOTCB fetching, and errors associated with IOTCB execution. If a parity error occurs when YC is fetching an IOTCB, YC will not execute the IOTCB. YC will clear its "IOTCB pending queue", reset IOTCBptr to zero, and send an "IOTCB fetch error" interrupt to MIOP via IOBB. To restart, MIOP must load the next IOTCB to memory location zero on IOBB, which is the default beginning of the IOTCB chain. A parity error occuring during IOTCB execution can be divided into two catagories, Command Channel(CMD=0x) errors and Data Channel(CMD=1x) errors. In both cases, when a parity error is detected, IOTCB execution will continue. When the entire transfer is finished, if the Retry bit in the IOTCB is set, hardware will automatically retry once. If successful, IOBB will get a normal "IOTCB done" interrupt and a scan only flip-flop will indicate a successful retry has occured. If the retry is not successful, an "IOTCB execution error" interrupt is sent to MIOP via IOBB. It is then up to the MIOP to take appropriate actions. YC then goes on to fetch the next IOTCB if any are pending. In addition, if the IOTCB in error is Command Channel related, the corresponding CE register will be set.

In summary, MIOP gets one of the following interrupts back for every IOTCB processed by YC :

1) IOTCB done - Current IOTCB completed successfully, YC will process the next IOTCB.
2) IOTCB execution error - Current IOTCB completed with data parity error, YC will process the next IOTCB.
3) IOTCB fetch error - Current IOTCB execution is aborted, all outstanding IOTCBs are disgarded, IOTCBptr reset to zero.

To ensure that IOTCBptr stays at zero after an IOTCB fetch error, the MIOP should, after the initial IOTCBs are processed, place an IOTCB with length=0 (noop) and "next IOTCBptr"=0 (IOTCBptr points to itself) at location zero of IOBB memory (do not send any "IOTCB pending" interrupts though !!).

5.0 VME Bus Interface

The IOBB is a slave and an interrupter on the VME Bus. All physical and electrical requirements conform to The VME Bus Specification Rev D.

5.1 VME Slave Characteristics

a. 16 Mbytes of DRAM memory with parity.
b. 80 Mbytes/sec max block transfer rate (64 bit mode).
c. Short (A16), Standard (A24), extended (A32), and long (A64) addressing capabilities (for A64 only 32 address bits are used).
d. Address modifiers for data access only (no program access).
f. Word (D16) or longword (D32) data transfers.
g. Byte (D08(O),D08(E)) transfer in single cycle only.
h. No unaligned transfer capability.
i. No read-modify-write capability.
j. Supports block transfers (D16, D32, and D64).

5.2 VME Interrupter characteristics

a. D08(O).
b. Interrupt level = 4.
c. RORA (release on register access).
d. The Status/ID is programmable from a master on the VME Bus.

Interrupts from the Y1BUS set appropriate bits of the status register. Any of the bits of the status register, when set, will cause an interrupt request of level 4 to the MIOP. An 8-bit vector, taken from the int_vector register (programmable from the MIOP) will be placed on the VMEbus when the interrupt request is acknowledged, D08(O). The MIOP should read the status register to find out the cause of the interrupt. IOBB, upon detecting a read of the status register, will reset the status register and release the interrupt request (RORA).

5.3 Control, Status, and Interrupt Vector Registers

There are two control registers, one status register, and one interrupt vector register on the IOBB.

a. Short addressing (A16) from 1000 to 1003 with Jumper J1 absent.
b Short addressing (A16) from 1040 to 1043 with Jumper J1 present.
c. Address modifier 29,2D.
d. D16 transfers only.

Register	Address (A16)	R/W	Action
Status	1000 (1040)	R	Read IOBB status, release interrupt request.
		W	Send "IOTCB pending" interrupt to CC. (no actual writing to status register)
Int_vector	1002 (1042)	W	Write 8-bit interrupt vector and send a Y1BUS IO reset.
		R	Read int_vector register.

The status register contains 10 bits of information :
<9> : "1" = Parity error detected on VME read from IOBB.
<8> : "1" = Received one (or more) "console interrupts" from CC.
<7> : "1" = Received one (or more) "ready to receive RSB" interrupt from CC.
<6> : "1" = Received one (or more) "CB pending" interrupt from CC.
<5> : "1" = Received one (or more) "reset" interrupt from CC.
<4> : "1" = Received one (or more) "IOTCB fetch error" interrupt from CC.
<3> : "1" = Received one (or more) "IOTCB execution error" interrupt from CC.
<2:0> : The total number of "IOTCB done" and "IOTCB execution error" interrupts received from CC, example, "000" = none, "100" = 4.

The int_vector register contains the following information :
<15> : "1" = Reset the IO channel.
<7:0> : The VME interrupt vector.

All control information from CC passes through the Y1BUS to the status register on IOBB. However, there is no hardware interlock to ensure that the MIOP will receive all the interrupts. For bits<7:5> of the status register, it is assumed that CC would not send more than one interrupt of each type before MIOP has a chance to read the status register and respond.

If bit<4> of the status register is set, MIOP should ignore bits<3:0>, and restart by placing an IOTCB at IOBB memory location zero.

When bit<3>=0, bits<2:0> indicate the number of IOTCBs completed sucessfully since the last time the status register was read. Since the maximum number of outstanding IOTCBs is 7, MIOP must not start any more IOTCBs until completion interrupts are received by reading the status register. If bit<3> is set, one (or more) of the IOTCBs completed was not successful. The status register does not provide enough information to indicate which IOTCB was bad, therefore MIOP must retry the total number of IOTCBs indicated by bits<2:0>.

5.4 VME MEMORY MAP JUMPER ASSIGNMENTS FOR NEW IOBB

J3	J2	J1	Addr Modifier	VME Address Range	AM	Size
0	0	0	29, 2D	1000 - 1003	A16	4B
			3F, 3D, 3B, 39	40 0000 - 7F FFFF	A24	4MB
			0F, 0D, 0B, 09	0040 0000 - 007F FFFF	A32	4MB
0	0	1	29, 2D	1040 - 1043	A16	4B
			3F, 3D, 3B, 39	80 0000 - BF FFFF	A24	4MB
			0F, 0D, 0B, 09	0080 0000 - 00BF FFFF	A32	4MB
0	1	0	29, 2D	1000 - 1003	A16	4B
			0F, 0D, 0B, 09	0400 0000 - 04FF FFFF	A32	16MB
			0C, 08 00, 01		A64	16MB
			03, 04, 05, 07			
0	1	1	29, 2D	1040 - 1043	A16	4B
			0F, 0D, 0B, 09	0800 0000 - 08FF FFFF	A32	16MB
			0C, 08, 00, 01		A64	16MB
			03, 04, 05, 07			
1	0	0	29, 2D	2000 - 2003	A16	4B
			0F, 0D, 0B, 09	0C00 0000 - 0CFF FFFF	A32	16MB
			0C, 08, 00, 01		A64	16MB
			03, 04, 05, 07			
1	0	1	29, 2D	2040 - 2043	A16	4B
			0F, 0D, 0B, 09	1000 0000 - 10FF FFFF	A32	16MB
			0C, 08, 00, 01		A64	16MB
			03, 04, 05, 07			
1	1	0	29, 2D	5000 - 5003	A16	4B
			0F, 0D, 0B, 09	1400 0000 - 14FF FFFF	A32	16MB
			0C, 08, 00, 01		A64	16MB
			03, 04, 05, 07			
1	1	1	29, 2D	5040 - 5043	A16	4B
			0F, 0D, 0B, 09	1800 0000 - 18FF FFFF	A32	16MB
			0C, 08, 00, 01		A64	16MB
			03, 04, 05, 07			

Notes:

1. Jumper present = 1, Jumper absent = 0.
2. To emulate an old IOBB jumpers J2 and J3 must be installed. J1 becomes the same as the jumper as on the old IOBB.
3. When emulating an old IOBB, only 4MB of DRAM can be accessed. We may only populate the board with 4MB DRAM.
4. The address ranges shown above can be changed within limits by reprogramming a PAL device.
5. In A64 mode only address bits A01 thru A31 are used.

CRAY Y-MP EL

DD-3 WINCHESTER DISK DRIVE

ESDI

FEATURES

- High-speed Access (14 msec. in average)
- High-Speed Data Transfer Rate
- Superior Reliability
- ESDI Industry Standard Interface
- Synchronized spindle
- Proven sputtered media and thin film head
- High Mean Time Between Failures

The DD-3 disk drive is a compact 5 1/4-inch format high-performance WINCHESTER disk drive with a capacity of 1.3 Gbytes formatted. The disk drive operates at sustained data transfer rates of approximately 2 Mbytes/sec. with a peak of 2.753 Mbytes/sec.

The reliability of the DD-3 disk drive is exceptionally high with a Mean Time Between Failures (MTBF) in excess of 150,000 hours of power-on operation (as determined by MIL STD 2.17). No preventive maintenance is required.

The DD-3 disk drive connects to the DC-3 disk controller. The DC-3 is an intelligent controller that supports from one to four disk drives. Intelligent disk management techniques include overlapping seeks on multiple drives connected to the disk controller. The controller transfers data from one drive at a time.

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SPECIFICATIONS

PERFORMANCE SPECIFICATIONS

Total Storage Capacity:	Unformatted:	1.538 Mbytes
	Formatted:	1.321 Mbytes
Capacity per Track:	45.88 Bytes	
Number of Cylinders:	2,235	
Number of Disks:	8	
Number of Heads:	15/1 15data/1servo	
Access Time:	Average:	14 msec.
	Maximum:	30 msec.
	Minimum:	3 msec.
Average Latency:	8.3 msec.	
Disk Rotational Speed:	~~3600 (rpm)~~ 3600 RPM	
Data Transfer Rate:	2.753 Mbytes/sec.	
Recording Density:	44.06 (bpi)	
Track Density:	2 (tpi)	
Recording Method:	1-7 (RLL)	

PHYSICAL SPECIFICATIONS

Dimensions:	Height:	3.25 in. (82.5mm)
	Width:	5.75 in. (146mm)
	Depth:	8 in. (203mm)
Weight:	7.7 lbs approx.	
Power Requirements:	VDC +5, +12	
Power Dissipation:	35 W	
Temperature:	Operating:	41 to 113 F
	Storage:	- 40 to 140 F
Humidity:	Operating:	8 to 80 %
	Non-oper.:	8 to 90 %
Vibration:	Operating:	0.25 g or less
	Non-oper:	0.5 G or less
Alt. above Sea Level:	Operating:	10,000 feet
	Non-oper.:	40,000 feet

CRAY Y-MP EL

DD-4 Disk Drive

IPI

FEATURES

- High-Speed Data Transfer Rate
- IPI-2 Interface Industry Standard
- Synchronized spindle
- Thin film media/heads
- Proven Reliability
- Fast Seek Time
- No preventive Maintenance

The DD-4 disk drive is a high-performance, two-head parallel IPI-2 drive with a capacity of 2.7 Gbytes/sec. (formatted) and a peak transfer rate of 9.34 Mbytes/sec. The disk drive operates at a sustained data transfer rate of 7 Mbytes/sec.

The DC-4 disk controller is an intelligent controller that can transfer data from two drives simultaneously. Up to four DD-4 drives may be attached to a DC-4 disk controller.

The reliability of the DD-4 disk drive is exceptionally high with a Mean Time Between Failures (MTBF) in excess of 150,000 hours of power-on operation (as determined by MIL STD 2.17). No preventive maintenance is required.

SPECIFICATIONS

PERFORMANCE SPECIFICATIONS

Total Storage Capacity:	Unformatted: 3.05 Mbytes
Interface:	IPI-2
External Transfer Rate:	9.34 Mbytes/sec.
Track-to-Track Seek:	2 msec.
Average Seek:	12 msec.
Spindle Speed:	4,365 (rpm)
Average Latency:	6.87 msec.
Number of Disks:	11
Data Surfaces:	18
Read/Write Heads:	1
Capacity per Track:	127,680 Bytes
Capacity per Cylinder:	1,149,120 Bytes
Number of Cylinders:	2,655
Recording Method:	1.7 (RLL)

18 data/4 servo ?
1/data surface ?
> 9 tracks/cyl.

PHYSICAL SPECIFICATIONS

Dimensions:	Height:	4.75 in. (120.6mm)
	Width:	8.5 in. (216mm)
	Depth:	14.7 in. (373.3mm)
Weight:	26 lbs approx. (13 kg)	
Power Requirements:	VDC +5, +12, +24	
Power Dissipation:	110/375 W	
Temperature:	Operating:	10 to 45 C
Humidity:	Operating:	20 to 80 %

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CRAY Y-MP EL

DC-3 ESDI Disk Controller

FEATURES

Cache Memory of 512 Kbytes
High Performance Microprocessor
Sustained Cache Throughput of 6 Mbytes/sec.
Multiple Circular Command Queues
Lookahead Caching to increase the Throughput
Transfer Rate Capability of 30 Mbytes/sec.
Disk Drive Serial Data Rates of up to 20 Mhz
Command Optimization
ESDI Interface (supports up to four DD-3 drives)
ESDI Transfer Rate
VMEbus Interface Compatible
UNIX Drivers, Extensive Software Support available
Scatter/Gather Data Transfer
Reduced Latency Operations
Operating Logging
48-bit ECC Error Correction
Defective Media Management
Diagnostic Capabilities
Programmable Disk Formats

Large Cache Memory and High Performance Microprocessor, coupled with High Speed disk and bus interfaces, are the building blocks for improving disk throughput. A large cache allows multiple tracks of disk data to reside in controller resident memory, where access time is measured in milliseconds.

The Multiple Circular Command Queues (each supporting greater than 2000 commands), link the operating system to the DC-3. With the access to all pending disk requests, it reduces Physical Latency Times, optimizes Disk Head Motion and minimizes Disk Accesses.

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The High Transfer Rate Capability is allowed by moving Data across the bus at a rate limited by the capability of most memory boards, and the DC-3 uses only a small fraction of the available bus bandwidth for Data Transfers.

Disk Drive Serial Data Rates on all Drives, provide VMEbus System architects with the tools to build a system that has ample Storage Capacity at the Highest Possible Data Rates. Regardless of the drives selected, intelligent Management Techniques, such as automatic overlapped seeks on multiple drives, insure Maximum Performance.

The VMEbus Interface: Da
are supported with Addressi
bits. Hardware support for b
VMEbus is provided.

which of these values do we use?

Procedure?

re maintained enabling
ised as defective sector

nostic
ilable

through software c

others?

SPECIFI

Single slot
Double Height Eurocard Form Factor Board
Board Size: 233 x 160mm
Power Requirements: 5 V at 6 amps typical
Ambient Temperature: 0-55 C degrees
Air Flow: 200 linear feet/min.

CRAY Y-MP EL

DC-4 Disk Controller (IPI-2 VME)

FEATURES

Up to 24 MB/sec. Dual-Channel IPI Throughput
High-Speed DMA oveer 35 MB/sec.
Supports Parallel-Head Drives
6U Form Factor Single-Slot Solution
1 MB Multi-Threaded Cache Buffer
Sophisticated Dynamic Caching Algorithms
Intelligent Read-Ahead Algorithms
Zero-Latency Reads/Minimum-Latency Writes
Advanced Reed Solomon ECC
12.0 MB/sec. Disk Support
Supports up to four DD-4 Drives
Multi-tasking Firmware
Full 32-Bit VMEbus Support
Asynchronous Command Queuing
Exclusive DYNAThrottle
Programmable Bus Control
Voltage Mode Differential Drivers/Receivers
Comprehensive Fault-Isolating Self-Diagnostic Tests
Extensive Use of VLSI
UNIX Software Support

Scalable Disk Channel Architecture

The DC-4 controller architecture can support multiple independent disk channels. Designed to handle transfers up to 12.0 Mbytes/sec., more than the maximum rate in the IPI-2 specification.

It has 2 disk channels each, and this allows the controller to have an effective IPI throughput of 24 Mbytes/sec., when performing Reads and Writes simultaneously on both channels.

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Multi-tasking Firmware

The Firmware on the IPI-2 disk controller has a multi-tasking executive that can process more than 15 commands concurrently. Multi-tasking 'hides" the overhead time of one command by processing another command during latency periods.

Optimal Command Execution

The DC-4 Controller reorders commands targeted for the same drive unit according to the physical location to be accessed, minimizing seeks. Also, the controller can use a single disk write operation to satisfy multiple write commands when the target disk locations are sequential, even iF the write operation is already in process.

Read-Ahead

The DC-4 controller reads data blocks past those requested in a given read command, until it reaches a cylinder boundary or fills the allocated cache. Since most file systems request a number of sequential sectors, the "hit" rate will be high, even for multiple block reads. The controller intelligently tracks the "hits" and "misses" of its read-ahead operations to determine their performance value. It will turn read-ahead on or off based on performance thresholds set by the driver software.

SPECIFICATIONS

Board Size: 233 x 160mm
Shielded Connectors: A front panel with 2 shielded connectors is includedConformance to FCC specifications is expected but must be confirmed in the user system
Power Requirements: Not to exceed 6 amps @+5V
Ambient Temperature: 0-55 C degrees
Relative Humidity: 90 % maximum (non-condens.)

CRAY Y-MP EL

TD-2 Tape Drive Subsystem

9 track

FEATURES

- Four Speeds
- Automatic Loading
- Data Transfer Rate of 2 MB/sec.
- Fully Modular Design and Construction
- Desktop or Rack-mount Unit
- Extensive Built-in Diagnostics
- PE Upgrade to Quad Density
- Low Component Count
- Up to four TD-2s per CRAY Y-MP EL cabinet

The CRAY Y-MP EL TD-2 9-track drive is a high-performance digital vacuum-buffered drive for 1/2-inch open reel tape. Read/write tape speed is 125 ips for 800 bpi, 1600 bpi, or 6250 bpi tape densities.

The vacuum column tape path reduces tape stresses for consistent read/write performance. A microprocessor-controlled closed-loop servo system ensures gentle and precise handling of tape during read/write and high-speed rewind.

A permanent active, intelligent eight-digit alpha numeric display provides continuous status information. Any size reel of tape is automatically loaded. If a reel is placed in an inverted position or if a power failure occurs, it automatically stops. Multiple load retries are initiated automatically if the tape leader is imperfect, minimizing the need for operator intervention. All card slots at the rear of the drive are easily accessible. When a new board is inserted, calibration and is automatic and the parameters are stored in the battery backed-up RAM.

Upgrading to ~~SCSI~~ Interface requires a ~~SI-1~~ Interface Card ~~that~~ supports up to ~~?~~ ~~SCSI~~ devices in a daisy-chained arrangement.

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It also provides connectivity to outboard STK (or compatible) SCSI tape units such as the STK 4780 which provides connectivity to the STK 4400.

The use of gate arrays has cut the component count to one quarter of that for equivalent circuitry with ICs, thus substantially enhancing reliability.

Absolutely no field adjustments are required because of its adaptive design. Multiple microprocessors monitor and automatically make any corrective adjustments to keep the drive functioning well within specification.

SPECIFICATIONS

PERFORMANCE SPECIFICATIONS

Tape Format:	6250 bpi (GCR), 3200 bpi (PE), 1600 bpi (PE), 800 bpi (NRZ)
Tape Threading:	Fully Automatic
Auto Loading:	6 in to 10.5 in (IBM Hub)
Tape Speeds:	Standard 42 ips(low), 125 (high) Option 50 ips(low), 100 (high)
Reposition Time:	912 ms (maximum)
Rewind Speed:	320 ips, 150 ips archive
MTBF:	20,000 hours
MTTR:	30 min.

PHYSICAL SPECIFICATIONS

Dim. Rack-Mounted:	Height:	8.7 in.(220 mm)
	Width:	17.45 in. (444 mm)
	Depth:	22.83 in. (580 mm)
Dim. Desktop:	Height:	9.65 in. (245 mm)
	Width:	18.97 in. (482 mm)
	Depth:	25.59 in. (650 mm)
Weight:	77 lbs. (35 kg)	
Temperature:	Operating: 50 to 104 F (10 to 40 C)	
Power Requirements:	100, 120, 220, 240 V, +15 %, 150 VA Standby, 350 VA max	

CRAY Y-MP EL

TD-3 Tape Drive Subsystem

3480 Cart

FEATURES

- Transfer Rate of 3 MB/sec.
- Compact 18-track Dri ve
- Time proven Design
- Long-Life Tape transport
- Ultra Long-Life Pneumatics
- 22,000 Hours MTBF
- Designed for ICRC (Compression/Compaction)
- Field Maintainable
- UL, CSA, FCC, VDE-B approved
- Up to four TD-3s per CRAY Y-MP EL cabinet

The CRAY Y-MP EL TD-3 18-track drive consists of a Controller and Tape Transport with universal power and heavy-duty pneumatics supplies.

With a 2-megabyte buffer, a 2-m/sec. read/write velocity and a 4-m/sec. rewind, search and locate speed, the TD-3 provides optimum throughput at all times.

The TD-3 Drive understands Field Support, and is comprised of field replaceable units (FRUs). A 720 Mbyte MS-DOS-Compatible flexible disk is included for storage of diagnostic, configuration, logging, and trace firmware.

The TD-3 3480-compatible cartridge drive subsystem provides high speed access to 3480-compatible cartridges. Each TD-3 requires an SI-1 Interface Card.

Power systems are amply derated for reliability and stability. Fans are oversize to reduce thermal gradients.

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SPECIFICATIONS

PERFORMANCE SPECIFICATIONS

Media:	1/2 in. Cartridge, ANSI specified
Capacity:	200-800 MB (with ICRC)
Read/Write Velocity:	79 in./sec. (2m/sec.)
Rew./Search Velocity:	159 in./sec. (4m/sec.)
Rewind Time:	55 sec. (165 meter standard Cart.)
Data Transfer Rate:	2.982 MB/sec. (to tape)
Connectivity:	SCSI
Error Management:	Parity, CRC, DRC, VRC
Flux Density:	9,720 FRPCM (24,689 FRPI)
Data Density:	40-160 KB/in. with ICRC

PHYSICAL SPECIFICATIONS

Dimensions:	Height:	6.91 in. (170.66 mm)
	Width:	17.6 in. (440.7 mm)
	Depth:	22 in. (550.9 mm)
Weight:	61 lbs. (28 kg)	
Temperature:	Operating: 50 to 104 F (10 to 40 C)	
Relative Humidity:	20-90 %	
Voltage:	90-132, 180-264 VAC, 50-60 Hz	
Power Consumption:	0.3 kVA	

C

CRAY Y-MP EL
DAS-2 Disk Array Subsystem

Features

- Intelligent Disk Array Controller
- Parity and Standby Drives
- Rapid Drive Reconstruction
- Transparent Recovery
- Overlapped Seeks
- Command Re-ordering
- Data Caching
- Multi-port Configuration
- Internal Diagnostics

The CRAY Y-MP EL DAS-2 disk array storage subsystem consists of an intelligent disk array controller supporting eight drives for data storage. The disk drive used is the DD-3 high-reliability, 5 1/4-inch drive.
The DAS-2 open architectureprovides substancial improvements in mass storageperformance, reliability and scalability though greatly increased storage capacity, and a sustained data transfer rate in excess of 15 Mbytes/sec. on large blocks, with a peak transfer rate of 18 Mbytes/sec.

The Disk Array Concept

The disk array subsystem consists of one to four banks of eight drives for data storage (10.4 Gbytes formatted per bank), plus one drive for parity and error recovery and one spare drive serving as a h[illegible]standby should one of the data storage d[illegible] ray ves A d to the nion.

Which hardware striping technique?

Data Reliability

Complete media defect management built into the array controller automatically handles bad sector and track replacement for both initial and subsequently developed flaws.

Data integrity is further enhanced using a 48-bit ECC polynomial stored with every 1024 bytes written to disk.

Fault Tolerance

If a disk becomes inoperable, the parity drive allows the array controller to dynamically regenerate the data on that disk onto the hot standby drive.

The standby drive is automatically switched in to take the place of the failed drive, and operation of the array subsystem continues uninterrupted.

Subsystem Configuration

The DAS-2 consists of a disk array controller with 10 drives: eight 1.3 MB disk drives for data storage, one parity drive, one hot spare drive and a VME controller.

What happens when Bad Spindle replaced

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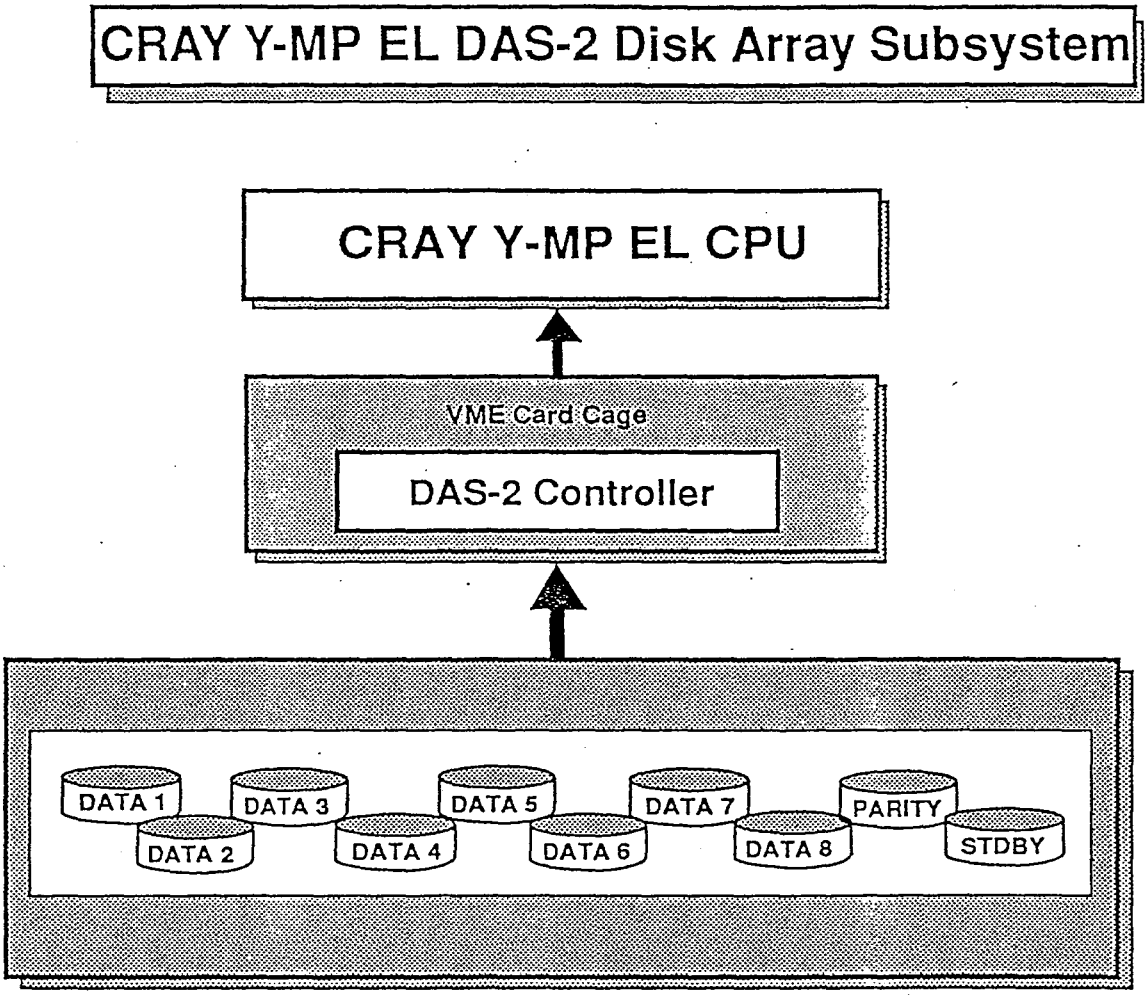

DAS-2 SPECIFICATIONS

PERFORMANCE SPECIFICATIONS

Sustained Data Transfer Rates: 15 Mbytes/sec.

Burst Data Transfer Rate: 40 Mbytes/sec.

Data Capacity per Controller: 10 to 40 Gbytes

Error Detection/Correction:
48 Bit Polynomial for every 1024 Bytes

Parity Drives/Standby Drives:
Data reconstruction and redundancy

PHYSICAL SPECIFICATIONS

Dimensions:	Height: 14 inches (355.6 mm)
	Width: 19 inches (482.6 mm)
	Depth: 10 inches (254 mm)
Weight:	50 pounds (23 kg)
Power Requirements:	AC Voltage:
	90-132 VAC Single Phase
	180-264 VAC Single Phase
AC Frequency:	47-63 hz
Power Consumption:	575 watts maximum
Heat Dissipation:	2185 BTU per hour maximum
Temperature:	Operating: 10-40 degrees C
	Storage: 0-50 degrees C
Relative Humidity:	Operating: 10-90 %
	Storage: 10-95 %

CRAY Y-MP EL

SI-1 VMEbus SCSI Host Bus

FEATURES

Control over SCSI bus Operations
Large Circular command Queue
Transfer Rate Capability of 30 MB/sec.
Support for up to 4 floppy drives
5.0 MB/sec. synchronous SCSI bus Transfer Rate
Single-ended or Differential SCSI bus Interface
Seven level dynamic Interrupter Support
Drivers for the System V version of Unix available
Command Optimization
Scatter/Gather Transfer Technique
Automatic Diagnostic

Complete Control over SCSI bus Operation

A software Interface using pass-through commands allows the system to select which commands are sent to the peripheral controllers. The SI-1 parameter blocks have a SCSI command descriptor block embedded in them.

The board will issue the command descriptor block directly to the SCSI bus upon reading it from system memory. This allows the use of any mandatory, optional, and vendor-unique SCSI commands as well as commands defined in the Common Command Set (CCS) specification.

Large Circular Command Queue

Designed for System Software, links the Operating System to the SI-1 adapter. The queue, with a command capacity exceeding practical limits, receives requests from the Operating System Driver as soon as they are ready, with no timing restrictions.

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With access to all pending SCSI requests, it can take advantage of the disconnect/reconnect capability of the SCSI bus and issue overlapped commands for different devices.

Transfer Rate Capability of 30 MB/sec.

The SI-1 System Interface gate arrays increase the bus efficiency by moving data across it at a rate limited by the capability of system memory boards, and using only a small fraction of the available bus bandwidth for data transfers.

Support for up to four single, dual, or quad density floppy Drives

Provides users with an economical method of floppy capability in their system. By buffering all floppy data in on-board local memory, SCSI performance is not degraded during floppy transfers. Supporting IBM PC XT/AT compatible drives, floppies continue to prove valuable as a method of loading software patches and updates, running diagnostics, transporting files, and even as a modest backup alternative.

The VMEbus Interface

Data Transfers of 8, 16 and 32 bits are supported with Addressing Capability of 16, 24 and 32 bits. Hardware support of byte and word order swapping of VMEbus is provided.

SPECIFICATIONS

Single slot
Double Height Eurocard Form Factor Board

Board Size:	233 x 160mm
Power Requirements:	5 V at 4 amps typical
Ambient Temperature:	0-55 C degrees
Air Flow:	200 linear feet/min.

CRAY Y-MP EL

/EX-2 8 mm Cartridge Tape Subsytem

FEATURES

5 1/4-inch Form Factor
High Density
High Speed of 150 ips
Large Capacity Cartridge of 5 GB
High Reliability of 40,000 hours MTBF
Low Power Requirements
Integrated SCSI Controller

The CRAY Y-MP EL EX-2 consists of an helical scan Cartridge Tape Drive recording technology and employing read and write head pairs, coupled with an integrated one MB speed machine buffer.

It now achieves a Data Transfer Rate of 500 KB/sec. with Peak Transfers up to 4 MB/sec. High speed search up to 37.5 MB/sec. allows rapid file retrieval. The EX-2 also provides up to 5 GB of Data Storage on a single, standard 8 mm Data Cartridge and is intended primarily as a backup device.

Packaged in the industry standard 5 1/4-inch form factor, the EX-2 performs onboard Error Correction Code and Error Recovery Procedures, along with full Read-after-Write verification to ensure data integrity.

The EX-2 is controlled directly from the MIOP and does not use a VME slot.

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SPECIFICATIONS

PERFORMANCE SPECIFICATIONS

Tape Motion

Tape Speed:	0.429 ips
Head-to-Head Speed:	150 ips
Max. Rewind Speed:	75 times nominal
Max. Search Speed:	37.5 MB/sec.

Format

Recording Format:	8 mm Helican-Scan Digital Computer Tape
Head Configuration:	Read-after-write Head pairs (seperate full-width erase head)
Track Density:	1638 tracks per in.
Areal Density:	74 million bits/sq. in.

Performance

Peak Transfer Rate:	4.0 MB/sec. synchronous 1.5 MB/sec. asynchronous
Sustained Transfer Rate:	500 KB/sec.
Buffer Size:	1 MB
Power on diagnostics:	<10 seconds.

Reliability

MTBF:	40,000 hours
MTTR:	<30 min.

PHYSICAL SPECIFICATIONS

Dimensions:	Height:	3.25 in.
	Width:	5.75 in.
	Depth:	8.00 in.
Weight:	4.5 lbs.	
Power Requirements:	VDC +5, +12 (~5%)	
Power Dissipation:	15 W	
Temperature:	Operating:	41 to 104 F
	Storage:	- 40 to +140 F
Relative Humidity:	20 to 80 % (non-condensing)	

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CRAY Y-MP EL

/HI-1 High-Performance Parallel Interface

FEATURES

Functionally compliant with the HIPPI ANSI standard
32 bit Data Channel
Equivalent Single Channel Rate of 800 Mbits/sec.
Host-side Interface Single-ended TTL
(designed for use with external FIFO)
Channel-side Interface Differential
Four Rank Data and Control Signal Synchronization
Byte Parity Checking
Lenght/Longitudinal Redundancy Checkword
(LLRC) Generation and Checking
Automatic Division of Data into HIPPI bursts
16-bit READY counter forFlow Control
Max. Latency through both Interface Circuits
(Connection: 600 ns; Data: 400 ns)
Diagnostic nodes for self test

GENERAL DESCRIPTION

The HI-1 consists of Source and Destination Interface circuits for the High-Performance Parallel Interface (HIPPI) Standard. These circuits are designed to completely meet the signalling protocol of the HIPPI ANSI specification.

They include both LLRC generation and checking as well as byte parity checking, and also a sophisticated four rank synchronization scheme to insure that the incoming Data and Control signals are coupled to the local clock. Data Flow Control is provided by q 16-bit ready counter in both the Source and the Destination Circuits. HIPPI Data BURST Partitioning is provided in the Source Circuit.

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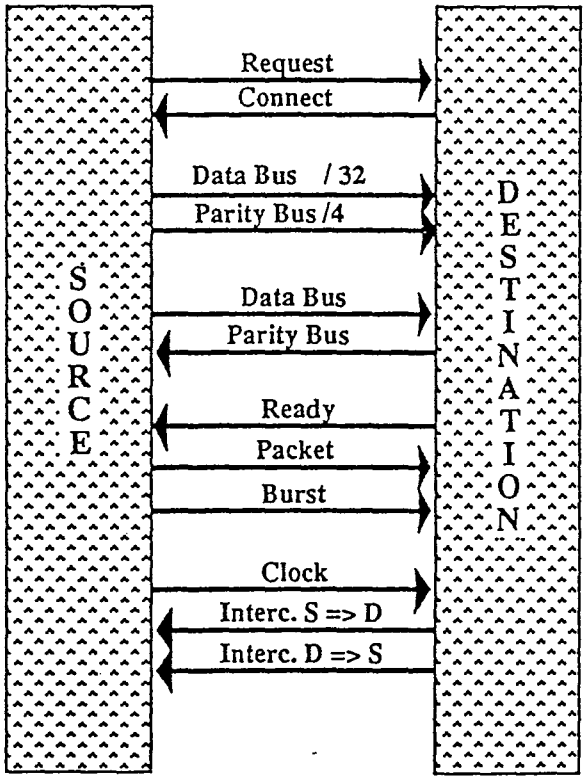
SPECIFICATIONS

Power Requirements:	Standard +5V, 0V (gnd), -5.2V
Package:	225 pin ceramic PGA

Interface Signal Summary



CRAY Y-MP EL

FI-1 Fiber Distributed Data Interface

FEATURES

FXP Full-Throughput Architecture
Local Microprocessor Unit (MPU)
512 Group Address Matching capability
High Performance 32-bit VMEbus Master Mode
Hardware Byte Alignement for Fragment Assembly
Link-level Driver (LLD) and Onboard Processing
Firmwares optimized for Interfacing Host-based TCP/IP protocols

FXP Architecture

The CRAY Y-MP EL FI-1 employs FXP Full-Throughput Architecture which offers an intelligent distributed Interface between the VMEbus host system and the FDDI, providing the speed, reliability, Sequencing, Protocol Processing and Data Flow Control.

Data Storage uses Multiport Dynamic Video Memory (VDRAM), normally used in video displays and having the fastest Data Access Time available. Not having to Factor Memory Contention into performance calculations allows full performance at Peak Host Transfer and Network Data Rates.

Local Microprocessor Unit

The processor used as the MPU in the FI-1 executes at a Clock Rate of 25 MHz. The MPU controls DMA access to the VMEbus and to the Network Module, executes Kernel functions, Link-Level, and Network Communications Protocol Processing, and runs Diagnostics Tests on start-up. One MByte VDRAM is used for the local instruction and Stack Memory. Instruction Access is at 25 MHz with no wait states.

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Packet Memory Module

The Multiport VDRAM is the Central Memory for all Network/Host/MPU Data and Protocol Processing. The VDRAM has two actual 32-bit ports: one for regular DRAM Access and the Serial Access Memory (SAM) used for High Speed Sequential Access. Normal VDRAM reads and writes to and from the DRAM port are done by the Processing Module and for DMA burst from the FDDI Network Module. SAM reads and writes are performed by the VMEbus High Speed DMA Channel.

Control Firmware

The FI-1 executes the physical, link, Network and Transport Layer Protocols onboard, removing this processing burden from the Host. The FDDI Link-layer Control (LLC) handles Network Access, while the MPU controls higher Layer Protocols.

SPECIFICATIONS

PERFORMANCE SPECIFICATIONS

Microprocessor Unit:	25 MHz clock frequency
Program PROM:	512 KBytes EPROM
Program VDRAM:	1 MBbyte zero-wait-state 40 ns instruction access
Download/Mo. Port:	Serial I/O port (SCC Interface)
Memory type:	1 Mbyte multiport Video RAM
Memory Cycle Time:	80 ns DMA cycle time 80 ns SAM cycle time
Buffer Memory:	256Kbytes. 45ns Static RAM
Asynchr. on VMEbus:	277Mbps transfer rate

PHYSICAL SPECIFICATIONS

Dimensions:	6U x 160 mm
Power Requirements:	+5,+12 V
Temperature:	Operating: 5 to 50 C degrees Storage: - 40 to 85 C degrees
Humidity:	Operating: 5 to 95 %

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CRAY Y-MP EL

HC-1 Processor Interface

FEATURES

The CRAY Y-MP EL HC-1 consists of a series of Processor Interface Boards. It provides transparent Interface from a VMEbus-based computer to the Network Systems HYPERchannel.

The HC-1 is equiped with Network Systems NETwork EXecutive (NETEX) software. This allows the user to make use of the HYPERchannel Network in the most efficient manner. An expanded buffer size increases the transmission rate of NETEX, thereby decreasing the time to send data.

More than one Processor Interface can connect to the same adapter, and all will have equal status on the HYPERchannel Network. Features of NETEX and the HYPERchannel Adapters allow hosts of different manufacturers to communicate freely.

Working together, NETEX and its utilities, the HC-1 and HYPERchannel provide all but the Application Layer of the ISO Open Systems Interconnection model.ISO Open Systems Interconnection model.

SPECIFICATIONS

PHYSICAL SPECIFICATIONS

Board Dimensions:	Height:	6.3 in. (160 mm)
	Width:	9.2 in. (233 mm)
Temperature:		
Storage:		- 67 to 257 F degrees (- 55 to 125 C)
Operating:		32 to 158 F degrees (0 to 70 C)
Relative Humidity:		0 to 95 % (non-condensing)
Altitude:		Storage: 50.000 feet max
		Operating: 20.000 max

POWER REQUIREMENTS

Voltage:	5 +/- 5 %(VDC)
Operating Current:	6.7 amps maximum at + 5 VDC
	3.2 amps typical at + 5 VDC
Heat Dissipation:	22 Btu/hr

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