CRAY X-MP EA/464 CHASSIS MAP (S/N 1103 AND UP)

SECTION 2 / CPU 2 / CPU Ø / SECTION Ø (top row)

A (SECTION 2)
- 3YS BANK 73
- 3YS BANK 72
- 3YS BANK 71
- 3YS BANK 70
- 3YS BANK 53
- 3YS BANK 52
- 3YS BANK 51
- 3YS BANK 50
- 3YL SECTION 2 WRITE DATA/ ADDRESS 3YL
- NOT USED

B
- NOT USED
- 3YJ SECTION 2 READ DATA 3YJ
- 3YG SECTION 2 ADDRESS
- NOT USED
- BANK 33
- 3YS BANK 32
- 3YS BANK 31
- 3YS BANK 30
- 3YS BANK 13
- 3YS BANK 12
- 3YS BANK 11
- 3YS BANK 10

C
- NOT USED
- 3MU 1ST AND 2ND LEVEL MULT.
- 3MV 1ST AND 2ND LEVEL MULT.
- 3MW 1ST AND 2ND LEVEL MULT.
- 3MZ MULTIPLY EXPONENT AND CONTROL
- 3MX FINAL LEVEL MULTIPLY
- 3MY FINAL LEVEL MULTIPLY
- 3AY MEMORY DATA DELAY CPU 2 SEC 2
- 3AY MEMORY DATA DELAY CPU 3 SEC 2
- 3ZI MEMORY SECTION CONTROL
- 3VF / 3VF VECTOR LOGICAL
- 3RY A2 FINAL RESULT
- 3RX A2 FORMATION
- 3RW A1² POP. COUNT FINAL
- 3RV A1 FORMATION
- 3HM PERFORMANCE LOG
- 3HL EXCHANGE PARAMETER
- 3AY MEMORY DATA DELAY CPU Ø SEC 2
- 3AY MEMORY DATA DELAY CPU Ø SEC 3
- 3HQ ERROR LOG
- 3DE I/O INPUT DATA ERROR CORRECTION
- 3DJ / 3DJ INPUT DATA BUFFER HISP, CHAN. 6
- 3DD / 3DD OUTPUT DATA BUFFER HISP, CHAN. 6
- 3DW HISP CHANNEL CONTROL
- 3TC CLOCK FANOUT
- 3DS UPPER MEMORY ADDRESS
- 3DL ADDR. LOWER AND REF. CONTROL

D (CPU 2)
- 3FE FINAL LEVEL, NORMALIZE
- 3FD J,K ADD
- 3FC FL. ADD K COEFF. ALIGN
- 3FB FL. ADD J COEFF. ALIGN
- 3FA FL. ADD EXP. AND CONTROL
- 3GS SCALAR REGISTERS 3GS
- 3GB SCALAR SHIFT
- 3GA / 3GA SCALAR ADD
- 3GB SCALAR SHIFT
- 3GS SCALAR REGISTERS 3GS
- 3AK MEMORY DATA SELECTION BITS 48-63
- 3AK MEMORY DATA SELECTION BITS 32-47
- 3AK MEMORY DATA SELECTION BITS 16-31
- 3AK MEMORY DATA SELECTION BITS 0-15
- 3BW ADDRESS DELAY SEC. 2 CPU 0,2
- 3BW ADDRESS DELAY SEC. 2 CPU 1,3
- 3ZE ERROR CORRECTION SEC. 2 BITS 0-31 CPU 2
- 3ZE ERROR CORRECTION SEC. 2 BITS 32-63 CPU 2
- 3ZE ERROR CORRECTION SEC. 2 BITS 0-31 CPU 3
- 3ZE ERROR CORRECTION SEC. BITS 32-63 CPU 3
- 3DT I/O MULTIPLEX

E
- 3VE / 3VE VECTOR SHIFT
- 3VB VECTOR OPERAND DATA 3VB
- 3VC VECTOR OPERAND DATA VECTOR LENGTH
- 3VA VECTOR RESULT DATA 3VA
- 3BT LOWER ADDRESS MULT. BITS 0-15
- 3BU MIDDLE ADDRESS MULT. BITS 16-23
- 3BV UPPER ADDRESS MULT. BITS 24-31
- 3JC SCALAR ISSUE
- 3JJ ADDRESS ISSUE
- 3JK VECTOR ISSUE
- 3JR CIP FANOUT J,H
- 3JR CIP FANOUT K,I,H
- 3JR CIP FANOUT K,I
- 3HO LOWER NIP
- 3HN UPPER NIP
- 3HH PROGRAM COUNTER
- 3JL SHARED REGISTER LOCAL CONTROL
- 3HS INSTRUCTION BUFFER PARCEL Ø
- 3HS INSTRUCTION BUFFER PARCEL 1

F
- 3VG / 3VG VECTOR ADD
- 3VR VECTOR REGISTERS 3VR
- 3VD / 3VD VECTOR REGISTER CONTROL
- 3ZE ERROR CORRECTION SEC. Ø BITS 0-31 CPU 2
- 3ZE ERROR CORRECTION SEC. Ø BITS 32-63 CPU 2
- 3ZE ERROR CORRECTION SEC. Ø BITS 0-31 CPU 3
- 3ZE ERROR CORRECTION SEC. Ø BITS 32-63 CPU 3
- 3BS ADDRESS ADDER
- 3BR ADDRESS REGISTERS 3BR
- 3BJ MEMORY ADDRESS SELECTION 5-14
- 3BJ MEMORY ADDRESS SELECTION BITS 15-25
- 3BM SCALAR REFERENCE
- 3BB I/O CONTROL
- 3BL FETCH AND EXCHANGE REFERENCE
- 3AH LOWER BLOCK ADDER CPU Ø
- 3AH LOWER BLOCK ADDER CPU 2
- 3BI UPPER BLOCK ADDER CPU Ø
- 3BI UPPER BLOCK ADDER CPU 2
- 3AN FOUR PORT CONFLICT SECTION Ø
- 3AN FOUR PORT CONFLICT SECTION 1

G
- 3VG / 3VG VECTOR ADD
- 3VR VECTOR REGISTERS 3VR
- 3VD / 3VD VECTOR REGISTER CONTROL
- 3ZE ERROR CORRECTION SEC.2 BITS 0-31 CPU Ø
- 3ZE ERROR CORRECTION SEC.2 BITS 32-63 CPU Ø
- 3ZE ERROR CORRECTION SEC. 2 BITS 0-31 CPU 1
- 3ZE ERROR CORRECTION SEC. 2 BITS 32-63 CPU 1
- 3BS ADDRESS ADDER
- 3BR ADDRESS REGISTERS 3BR
- 3BJ MEMORY ADDR. SEL. BITS 5-14
- 3BJ MEMORY ADDR. SEL. BITS 15-25
- 3BM SCALAR REFERENCE
- 3BB I/O CONTROL
- 3BL FETCH AND EXCHANGE REFERENCE
- 3TO MASTER CLOCK
- 3DN I/O CONTROL
- 3JM SEM. COMMON CONTROL CPU Ø
- 3JM SEM. COMMON CONTROL CPU 2
- 3JM SEM. COMMON CONTROL CPU 2
- 3JM SEM. COMMON CONTROL CPU 3

H
- 3VE / 3VE VECTOR SHIFT
- 3VB VECTOR OPERAND DATA 3VB
- 3VC VECTOR OPERAND DATA VECTOR LENGTH
- 3VA VECTOR RESULT DATA 3VA
- 3BT LOWER ADDR. MULT. BITS 0-15
- 3BU MIDDLE ADDR. MULT. BITS 16-23
- 3BV UPPER ADDR. MULT. BITS 24-31
- 3JC SCALAR ISSUE
- 3JJ ADDRESS ISSUE
- 3JK VECTOR ISSUE
- 3JR CIP FANOUT J,H
- 3JR CIP FANOUT K,I,H
- 3JR CIP FANOUT K, I
- 3HO LOWER NIP
- 3HN UPPER NIP
- 3HH PROGRAM COUNTER
- 3JL SHARED REGISTER LOCAL CONTROL
- 3HS INSTRUCTION BUFFER PARCEL Ø
- 3HS INSTRUCTION BUFFER PARCEL 1

I (CPU Ø)
- 3FE FINAL LEVEL, NORMALIZE
- 3FD J,K ADD
- 3FC FL. ADD K COEFF. ALIGN
- 3FB FL. ADD J COEFF. ALIGN
- 3FA FL. ADD EXP. AND CONTROL
- 3GS SCALAR REGISTERS 3GS
- 3GB SCALAR SHIFT
- 3GA / 3GA SCALAR ADD
- 3GB SCALAR SHIFT
- 3GS SCALAR REGISTERS 3GS
- 3AK MEMORY DATA SEL. BITS 48-63
- 3AK MEMORY DATA SEL. BITS 32-47
- 3AK MEMORY DATA SEL. BITS 16-31
- 3AK MEMORY DATA SEL. BITS 0-15
- 3BW ADDRESS DELAY SEC. 0 CPU 0,2
- 3BW ADDRESS DELAY SEC. Ø CPU 1-3
- 3ZE ERROR CORRECTION SEC.Ø BITS 0-31 CPU Ø
- 3ZE ERROR CORRECTION SEC. Ø BITS 32-63 CPU Ø
- 3ZE ERROR CORRECTION SEC.Ø BITS 0-31 CPU 1
- 3ZE ERROR CORRECTION SEC. Ø BITS 32-63 CPU 1
- 3DT I/O MULTIPLEX

J
- NOT USED
- 3MU 1ST AND 2ND LEVEL MULT.
- 3MV 1ST AND 2ND LEVEL MULT.
- 3MW 1ST AND 2ND LEVEL MULT.
- 3MZ MULT. EXPONENT AND CONTROL
- 3MX FINAL LEVEL MULT.
- 3MY FINAL LEVEL MULT.
- 3AY MEMORY DATA DELAY CPU Ø SEC. Ø
- 3AY MEMORY DATA DELAY CPU 1 SEC. Ø
- 3ZI MEMORY SECTION CNTL.
- 3VF VECTOR LOGICAL
- 3VF VECTOR LOGICAL
- 3RY A2 FINAL RESULT
- 3RX A2 FORMATION
- 3RW A1² AND POP. COUNT FINAL
- 3RV A1 FORMATION
- 3HM PERFORMANCE LOG
- 3HL EXCHANGE PARAMETER
- 3AY MEMORY DATA DELAY CPU 2 SEC. Ø
- 3AY MEMORY DATA DELAY CPU 2 SEC 1
- 3HQ ERROR LOG
- 3DE I/O INPUT DATA ERROR CORR.
- 3DJ / 3DJ INPUT DATA BUFFER HISP, CHANNEL 10,12,7
- 3DD / 3DD OUTPUT DATA BUFFER CHAN 11,13,7
- 3DW HISP CHANNEL AND CONTROL
- 3TC CLOCK FANOUT
- 3DS UPPER I/O MEMORY ADDRESS
- 3DL ADDR. LOWER AND REF. CONTROL

K (SECTION Ø)
- NOT USED
- 3YJ SECTION Ø READ DATA 3YJ
- 3YG SECTION Ø ADDRESS
- NOT USED
- 3YS BANK 23
- 3YS BANK 22
- 3YS BANK 21
- 3YS BANK 20
- 3YS BANK 3
- 3YS BANK 2
- 3YS BANK 1
- 3YS BANK 0

L
- 3YS BANK 63
- 3YS BANK 62
- 3YS BANK 61
- 3YS BANK 60
- 3YS BANK 43
- 3YS BANK 42
- 3YS BANK 41
- 3YS BANK 40
- 3YL SECTION Ø WRITE DATA/ ADDRESS 3YL
- NOT USED

SECTION 3 / CPU 3 / CPU 1 / SECTION 1 (bottom row)

M (SECTION 3)
- NOT USED
- 3YL SECTION 3 WRITE DATA/ ADDRESS 3YL
- 3YS BANK 54
- 3YS BANK 55
- 3YS BANK 56
- 3YS BANK 57
- 3YS BANK 74
- 3YS BANK 75
- 3YS BANK 76
- 3YS BANK 77

N
- 3YS BANK 14
- 3YS BANK 15
- 3YS BANK 16
- 3YS BANK 17
- 3YS BANK 34
- 3YS BANK 35
- 3YS BANK 36
- 3YS BANK 37
- NOT USED
- 3YG SECTION 3 ADDRESS
- 3YJ SECTION 3 READ DATA 3YJ
- NOT USED

O
- 3DL ADDR. LOWER AND REF. CONTROL
- 3DS UPPER I/O MEM. ADDRESS
- 3DI SSD CHANNEL CONTROL CHANNEL 6
- 3DW HISP CHANNEL CONTROL
- 3DD / 3DD OUTPUT DATA BUFFER HISP, CHAN. 6
- 3DJ / 3DJ INPUT DATA BUFFER HISP, CHAN. 6
- 3DE I/O INPUT DATA ERROR CORR.
- 3HQ ERROR LOG
- 3AY MEM. DATA DELAY CPU 1 SEC.2
- 3AY MEM. DATA DELAY CPU 1 SEC. 3
- 3HL EXCHANGE PARAMETER
- 3HM PERFORMANCE LOG
- 3RV A1 FORMATION
- 3RW A1² AND POP COUNT FINAL
- 3RX A2 FORMATION
- 3RY A2 FINAL RESULT
- 3VF / 3VF VECTOR LOGICAL
- 3ZI MEM. SECTION CONTROL
- 3AY MEM. DATA DELAY CPU 2 SEC. 3
- 3AY MEM. DATA DELAY CPU 3 SEC. 3
- 3MY FINAL LEVEL MULT.
- 3MX FINAL LEVEL MULT.
- 3MZ MULT. EXPONENT AND CONTROL
- 3MW 1ST AND 2ND LEVEL MULTIPLY
- 3MV 1ST AND 2ND LEVEL MULTIPLY
- 3MU 1ST AND 2ND LEVEL MULTIPLY
- NOT USED

P (CPU 3)
- 3TC CLOCK FANOUT
- 3ZE ERROR CORRECTION SEC. 3 BITS 0-31 CPU 2
- 3ZE ERROR CORRECTION SEC. 3 BITS 32-63 CPU 2
- 3ZE ERROR CORRECTION SEC. 3 BITS 0-31 CPU 3
- 3ZE ERROR CORRECTION SEC. 3 BITS 32-63 CPU 3
- 3BW ADDRESS DELAY SEC. 3 CPU 1,3
- 3BW ADDRESS DELAY SEC.3 CPU 0,2
- 3AK MEM. DATA SELECTION BITS 0-15
- 3AK MEM. DATA SELECTION BITS 16-31
- 3AK MEM. DATA SELECTION BITS 32-47
- 3AK MEM. DATA SELECTION BITS 48-63
- 3GS SCALAR REGISTERS 3GS
- 3GB SCALAR SHIFT
- 3GA / 3GA SCALAR ADD
- 3GB SCALAR SHIFT
- 3GS SCALAR REGISTERS 3GS
- 3FA FL. ADD EXP. AND CONTROL
- 3FB FL. ADD J COEFF. ALIGN
- 3FC FL. ADD K COEFF. ALIGN
- 3FD J AND K ADD
- 3FE FINAL LEVEL, NORMALIZE

Q
- 3HS INSTRUCTION BUFFER PARCEL 2
- 3HS INSTRUCTION BUFFER PARCEL 3
- 3JL SHARED REGISTER LOCAL CONTROL
- 3HH PROGRAM COUNTER
- 3HN UPPER NIP
- 3HO LOWER NIP
- 3JR CIP FANOUT K,I
- 3JR CIP FANOUT K,I,H
- 3JR CIP FANOUT J,H
- 3JK VECTOR ISSUE
- 3JJ ADDRESS ISSUE
- 3JC SCALAR ISSUE
- 3BV UPPER ADDR. MULT.
- 3BU MIDDLE ADDR. MULT.
- 3BT LOWER ADDR. MULT.
- 3VA VECTOR RESULT DATA 3VA
- 3VC VECTOR OPERAND DATA VECTOR LENGTH
- 3VB VECTOR OPERAND DATA 3VB
- 3VE / 3VE VECTOR SHIFT

R
- 3AN FOUR PORT CONFLICT SECTION 2
- 3AN FOUR PORT CONFLICT SECTION 3
- 3BI UPPER BLOCK ADDR. CPU 3
- 3BI UPPER BLOCK ADDR. CPU 1
- 3AH LOWER BLOCK ADDER CPU 3
- 3AH LOWER BLOCK ADDER CPU 1
- 3BL FETCH AND EXCHANGE REFERENCE
- 3BB I/O CONTROL
- 3BM SCALAR REFERENCE
- 3BJ MEMORY ADDRESS SEL. BITS 15-25
- 3BJ MEMORY ADDRESS SEL. BITS 5-14
- 3BR ADDRESS REGISTERS 3BR
- 3BS ADDRESS ADDER
- 3ZE ERROR CORRECTION SEC 1 BITS 0-31 CPU 2
- 3ZE ERROR CORRECTION SEC. 1 BITS 32-63 CPU 2
- 3ZE ERROR CORRECTION SEC 1 BITS 0-31 CPU 3
- 3ZE ERROR CORRECTION SEC. 1 BITS 32-63 CPU 3
- 3VD / 3VD VECTOR REGISTER CONTROL
- 3VR VECTOR REGISTERS 3VR
- 3VG / 3VG VECTOR ADD

S
- 3JO SHARED REGS. LOWER BITS
- 3JO SHARED REGS. LOWER BITS
- 3JO SHARED REGS. LOWER BITS
- 3JO SHARED REGS. LOWER BITS
- 3GH REAL TIME CLOCK
- 3GH REAL TIME CLOCK
- 3BL FETCH AND EXCHANGE REFERENCE
- 3BB I/O CONTROL
- 3BM SCALAR REFERENCE
- 3BJ MEMORY ADDR. SEL. BITS 15-25
- 3BJ MEMORY ADDR. SEL. BITS 5-14
- 3BR ADDRESS REGISTERS 3BR
- 3BS ADDRESS ADDER
- 3ZE ERROR CORRECTION SEC. 3 BITS 0-31 CPU Ø
- 3ZE ERROR CORRECTION SEC. 3 BITS 32-63 CPU Ø
- 3ZE ERROR CORRECTION SEC. 3 BITS 0-31 CPU 1
- 3ZE ERROR CORRECTION SEC. 3 BITS 32-63 CPU 1
- 3VD / 3VD VECTOR REGISTER CONTROL
- 3VR VECTOR REGISTERS 3VR
- 3VG / 3VG VECTOR ADD

T
- 3HS INSTRUCTION BUFFER PARCEL 2
- 3HS INSTRUCTION BUFFER PARCEL 3
- 3JL SHARED REGISTERS LOCAL CONTROL
- 3HH PROGRAM COUNTER
- 3HN UPPER NIP
- 3HO LOWER NIP
- 3JR CIP FANOUT K,I
- 3JR CIP FANOUT K,I,H
- 3JR CIP FANOUT J,H
- 3JK VECTOR ISSUE
- 3JJ ADDRESS ISSUE
- 3JC SCALAR ISSUE
- 3BV UPPER ADDR. MULT.
- 3BU MIDDLE ADDR. MULT.
- 3BT LOWER ADDR. MULT.
- 3VA VECTOR RESULT DATA 3VA
- 3VC VECTOR OPERAND DATA VECTOR LENGTH
- 3VB VECTOR OPERAND DATA 3VB
- 3VE / 3VE VECTOR SHIFT

U (CPU 1)
- 3TC CLOCK FANOUT
- 3ZE ERROR CORRECTION SEC. 1 BITS 0-31 CPU Ø
- 3ZE ERROR CORRECTION SEC. 1 BITS 32-63 CPU Ø
- 3ZE ERROR CORRECTION SEC. 1 BITS 0-31 CPU 1
- 3ZE ERROR CORRECTION SEC. 1 BITS 32-63 CPU 1
- 3BW ADDRESS DELAY SEC. 1 CPU 1,3
- 3BW ADDRESS DELAY SEC. 1 CPU 0,2
- 3AK MEMOR DATA SEL. BITS 0-15
- 3AK MEMORY DATA SEL. BITS 16-31
- 3AK MEMORY DATA SEL. BITS 32-47
- 3AK MEMORY DATA SEL. BITS 48-63
- 3GS SCALAR REGISTERS 3GS
- 3GB SCALAR SHIFT
- 3GA / 3GA SCALAR ADDER
- 3GB SCALAR SHIFT
- 3GS SCALAR REGISTERS 3GS
- 3FA FL. ADD EXP.
- 3FB FL. ADD J COEFF. ALIGN
- 3FC FL. ADD K COEFF. ALIGN
- 3FD J AND K ADD
- 3FE FINAL LEVEL, NORMALIZE

V
- 3DL ADDR. LOWER AND REF. CONTROL
- 3DS UPPER I/O MEM. ADDR.
- 3DI SSD CHANNEL CNTL.
- 3DW HISP. CHANNEL CNTL.
- 3DD / 3DD OUTPUT DATA BUFFER CHAN 15,17,7
- 3DJ / 3DJ INPUT DATA BUFFER HISP, CHAN 14,16,7
- 3DE I/O INPUT DATA ERROR CORR.
- 3HQ ERROR LOG
- 3AY MEMORY DATA DELAY CPU 3 SEC. Ø
- 3AY MEMORY DATA DELAY CPU 3 SEC. 1
- 3HL EXCHANGE PARAMETER
- 3HM PERFORMANCE LOG
- 3RV A1 FORMATION
- 3RW A1² AND POP. COUNT FINAL
- 3RX A2 FORMATION
- 3RY A2 FINAL RESULT
- 3VF / 3VF VECTOR LOGICAL
- 3ZI MEMORY SECTION CNTL.
- 3AY MEMORY DATA DELAY CPU Ø SEC. 1
- 3AY MEMORY DATA DELAY CPU 1 SEC. 1
- 3MY FINAL LEVEL MULT.
- 3MX FINAL LEVEL MULT.
- 3MZ MULT. EXPONENT AND CONTROL
- 3MW 1ST AND 2ND LEVEL MULT.
- 3MV 1ST AND 2ND LEVEL MULT.
- 3MV 1ST AND 2ND LEVEL MULT.
- NOT USED

W (SECTION 1)
- 3YS BANK 4
- 3YS BANK 5
- 3YS BANK 6
- 3YS BANK 7
- 3YS BANK 24
- 3YS BANK 25
- 3YS BANK 26
- 3YS BANK 27
- NOT USED
- 3YG SECTION 1 ADDRESS
- 3YJ SECTION 1 READ DATA 3YJ
- NOT USED

X
- NOT USED
- 3YL SECTION 1 WRITE DATA/ ADDRESS 3YL
- 3YS BANK 44
- 3YS BANK 45
- 3YS BANK 46
- 3YS BANK 47
- 3YS BANK 64
- 3YS BANK 65
- 3YS BANK 66
- 3YS BANK 67

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