Troubleshooting Double-bit Memory Errors

HMM-433-0
CRAY T916 and CRAY T932 Systems
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Figures

Tables

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Introduction

This document provides information that you can use to troubleshoot CRAY T916 and CRAY T932 double-bit memory failures.

It includes procedures for the following situations:

- What to do when double-bit memory errors occur
- What to do when SCE cannot assert a configuration because of a DMA problem
- How to use `cmt11` to force memory miscompares

It also includes the following reference information to aid you while you troubleshoot memory failures:

- Guidelines for using spare chips and replacing memory module stacks
- Flawable syndromes
- CRAY T916 memory module stack isolation (for CM02, CM03, and CM04 modules)
- Information about determining the physical memory section from the global address in 4-section lower mode or 4-section upper mode

What to Do When Double-bit Memory Errors Occur

Perform the following procedure when double-bit errors occur:

1. Gather as much information about the failure as possible.
2. Correlate that information to possible hardware failures.
3. Remove components from the system until you have a working system.
4. Add components to the configuration until you detect the failing hardware.

Gather Information about the Failure

When double-bit memory errors occur, gather as much information about the errors as you can. Gather information from the following sources:

- The `olhpa` report from the operating system
- The error logger report
- The `cmt11` offline diagnostic test output

Compare the information from the `olhpa` and error logger reports because each report is likely to be missing information as a result of the timing of the failure. By comparing the two reports, you will develop a better understanding of the “complete picture” of exactly which failures occurred and when.

Note: It may be difficult to interpret this information because a bad CP can write bad data to all of the other CPs in the system. The other CPs will correctly read the bad data, but the error logger will report problems for all CPs that received the bad data.

Correlate the Information to Possible Hardware Failures

After you have gathered all the information that you can, answer the following questions:

- Are all CPs involved, are all CPs in a single stack involved, or is only a single CP involved?
- Are all memory sections involved or only a single section?
- Are all memory subsections involved or only a single subsection?
- Are all banks in a subsection involved or only a single bank?

Use this information and Figure 1 and Figure 2 to get a better understanding of what hardware is being used and what hardware might be failing.

Be aware of the following concepts as you correlate the information to possible hardware failures:

- If a single subsection (all banks) fails, the failing hardware is either a memory module or network port.
- If only a single section, single subsection, and one or two banks fail, the failing hardware is a memory module.
- The following conditions indicate network failures:
    - Only all odd or only all even subsections in a memory module stack fail.
    - Only four CPUs in one stack fail.
    - Only one memory module stack fails.
- For intermittent failures, the failing hardware may appear to be simply one CPU when it is actually more hardware. This occurs because only one CPU was referencing memory at the time the failure occurred.
- Do not remove a module from the system until the symptoms are clear (for example, wait until you can isolate to one subsection, etc.).

Figure 1. CRAY T916 Memory Chassis Map

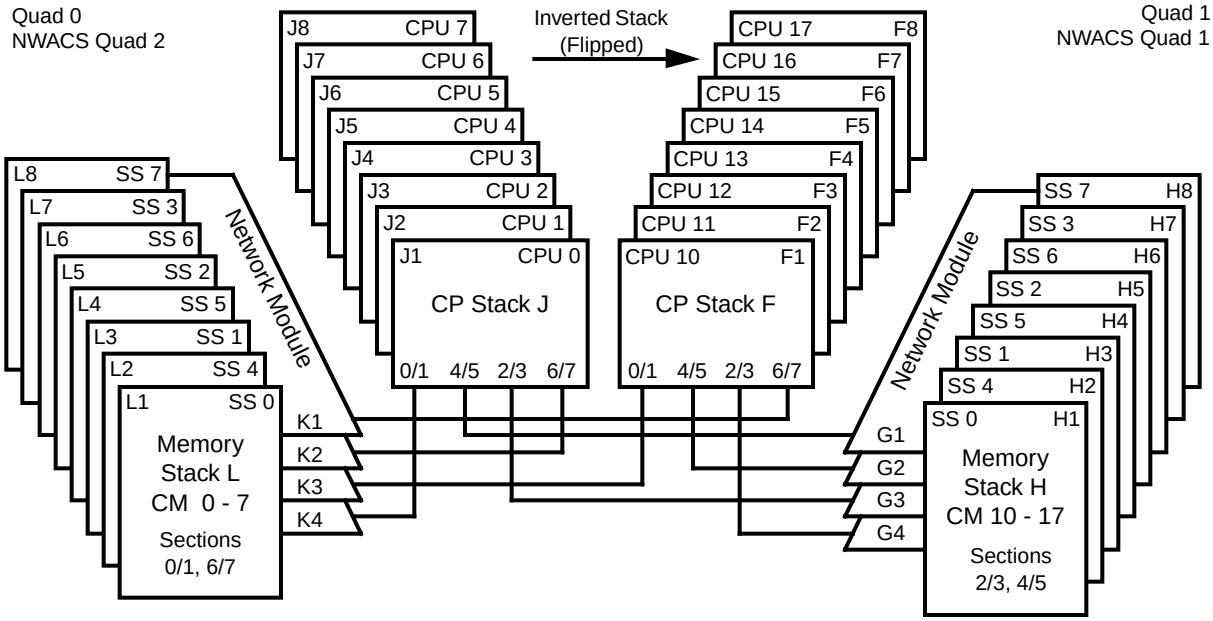
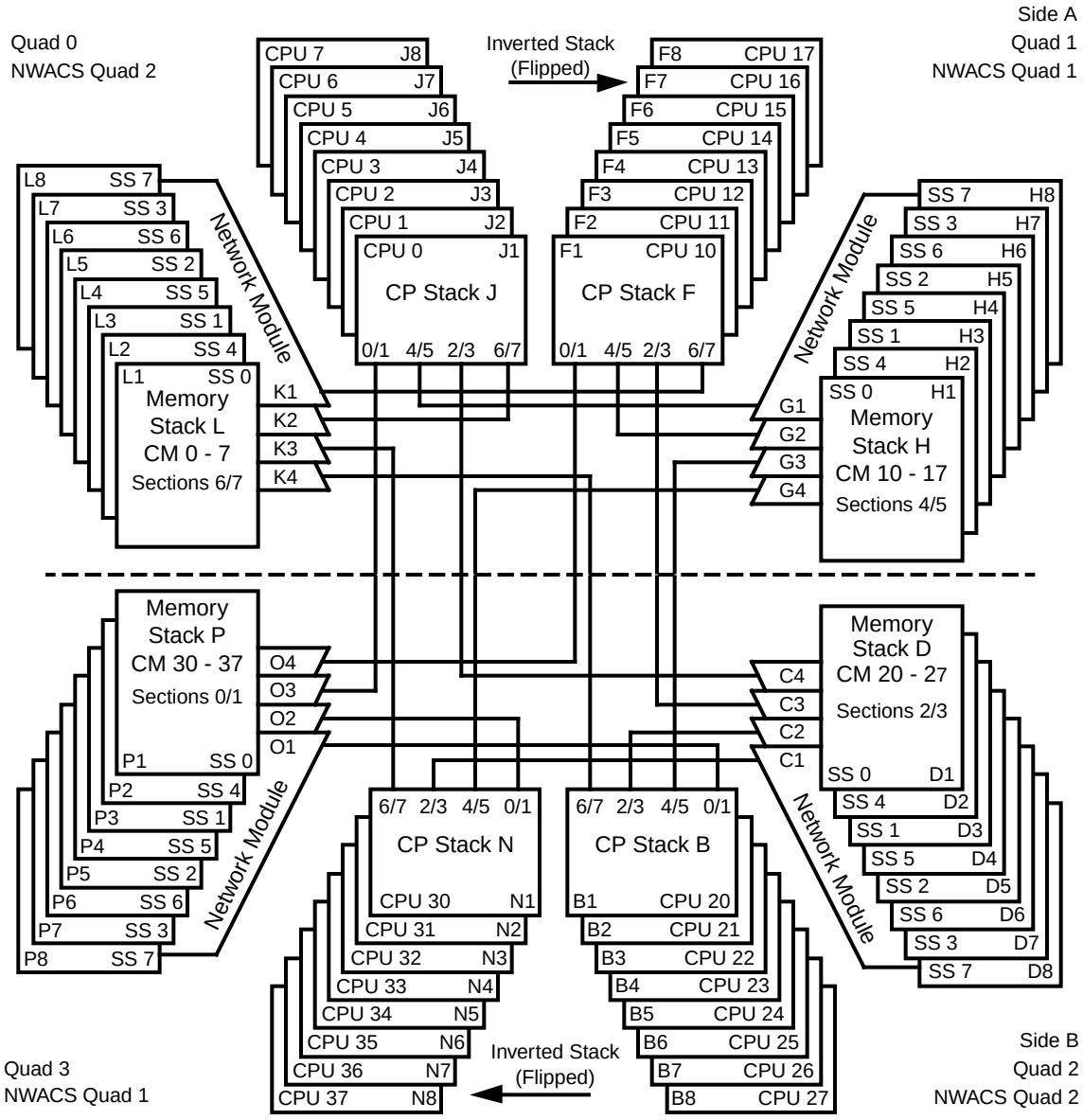


Figure 2. CRAY T932 Memory Chassis Map



Remove Components from the System Configuration

If you cannot locate the failing hardware by using the information that you have collected along with Figure 1 and Figure 2, you should systematically remove components from the configuration and test the system. Continue to remove hardware from the configuration and test the system until you get a configuration that operates without failure.

Remember the following concepts as you remove components from the configuration:

- On a CRAY T916 system, you can reduce the configuration to two memory modules by varying the selected sections and subsections.
- On a CRAY T916 system, if you have no idea where the failure is, reduce the configuration to one stack of CPUs and one-half of memory. Use `cmt11` to test this configuration. If you do not detect an error, reduce the configuration to the other stack of CPUs and the other half of memory. Test the system again with `cmt11`.
  - If you reduce memory by half in a CRAY T916 system and a failure for all subsections disappears, a network module caused the failure.
  - If you reduce memory by half in a CRAY T916 system and a problem with only one failing subsection disappears, the failing hardware could still be either a memory module or a network module.
- On a CRAY T932 system, you can reduce the configuration to two memory modules by varying the selected sections and subsections.

Note: If you remove as many components from the system as possible and still receive SCE DMA failures when you assert the configuration, refer to "What to Do When SCE Cannot Assert a Configuration" on page 11 for more information.

Add Components to the System Configuration

Once you have a working configuration, start adding hardware to the configuration and test it with `cmt11` until an error occurs. Then, determine the hardware that caused the failure and replace the hardware.

Quick-reference Flowchart

Figure 3 and Figure 4 provide a quick-reference overview of this troubleshooting process.

Figure 3. Troubleshooting Flowchart (Part 1 of 2)

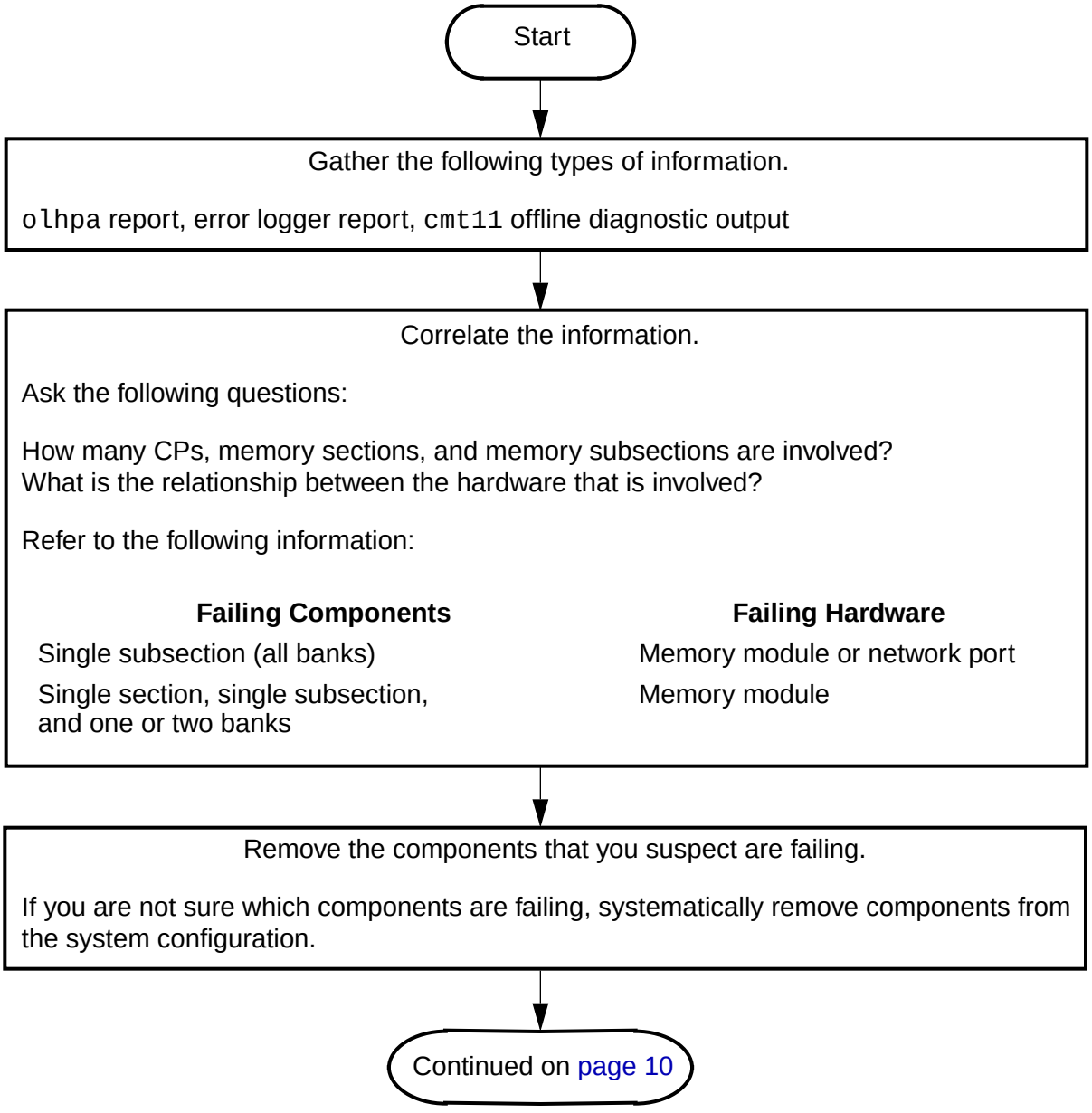
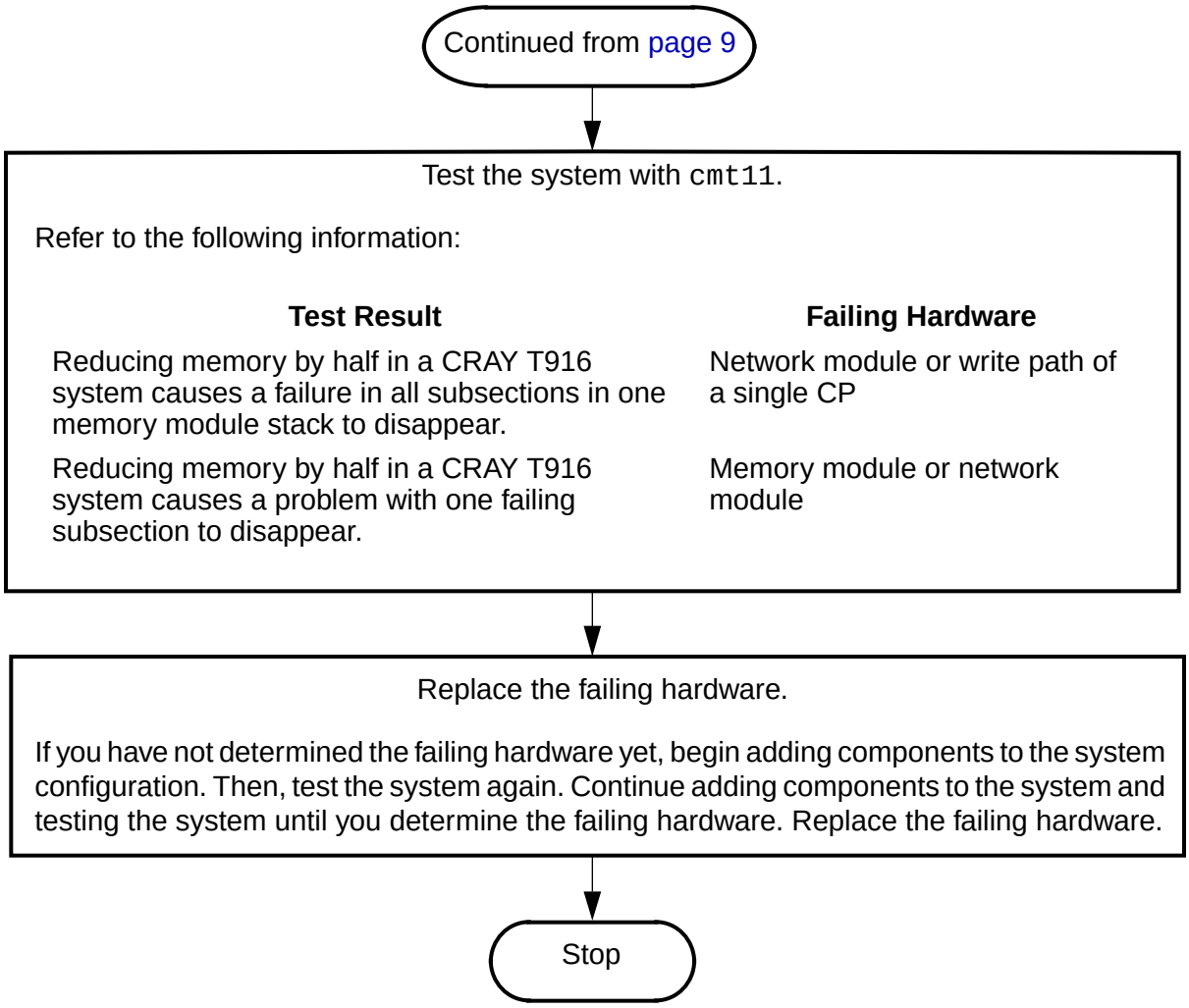


Figure 4. Troubleshooting Flowchart (Part 2 of 2)

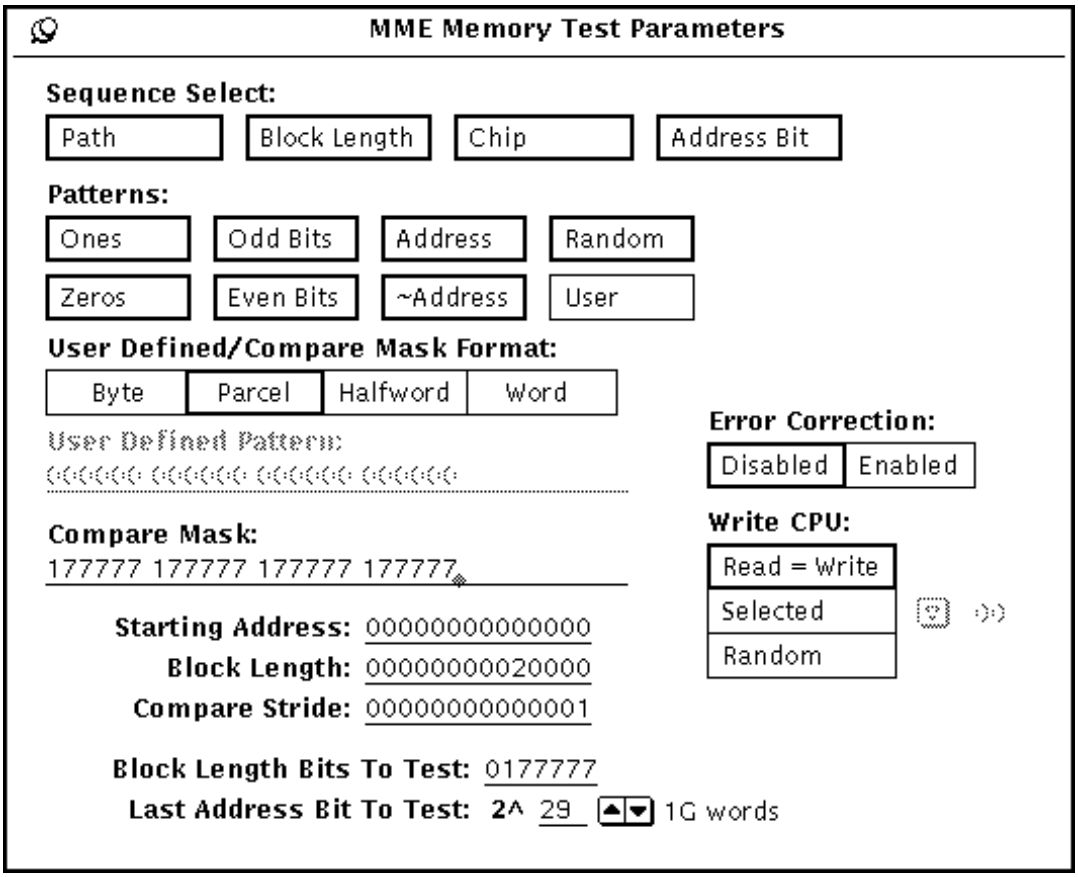


What to Do When SCE Cannot Assert a Configuration

Perform the following procedure when you have reduced the memory configuration as much as possible and you still receive a DMA failure when you apply the configuration with SCE:

1. Disable chip flawing. (Chip flawing is the only SCE operation that uses DMA operations.)
2. Apply the configuration.
3. Start MME in environment 0. (Be sure it is in Manual mode.)
4. Select the Memory Test. (Figure 5 shows the MME environment 0 memory test parameters.)

Figure 5. MME Environment 0 Memory Test Parameters



5. Set the Starting Address to the suspected failing section/subsection address.

   If you do not have a suspected failing section/subsection, start writing a few words of data to the beginning of a section and see if the test detects an error. If the test does not detect an error, try writing a few words of data to the beginning of another section. Continue this process until the test detects an error.

6. Set the Block Length to 1.

7. Click on the Go button to start the test.

Note: After you have detected the failing section, the maintenance channel will be hung. You must re-assert SCE to clear the maintenance channel.

Using cmt11 to Force Memory Miscompares

Use the `cmt11` diagnostic test to force memory miscompares in the offline diagnostic environment. `cmt11` uses CPU exclusive writes, so a multiple-CPU and multiple-subsection error indicates a failing network board or system interconnect board (SIB).

Note: Because of the network module's design, `cmt11` may report multiple failing subsections when only one subsection is failing. In this situation, your first assumption will be that the network module is failing, but the actual failing hardware is a memory module. To check for this, test the system in half-subsection mode before you replace any hardware to ensure that the failure occurs in both upper-only and lower-only modes. If only one of these modes fails, the failing hardware is actually a memory module. (This note applies only to data miscompares that `cmt11` reports; it does not apply to any SBEs or MBEs that the error logger reports.)

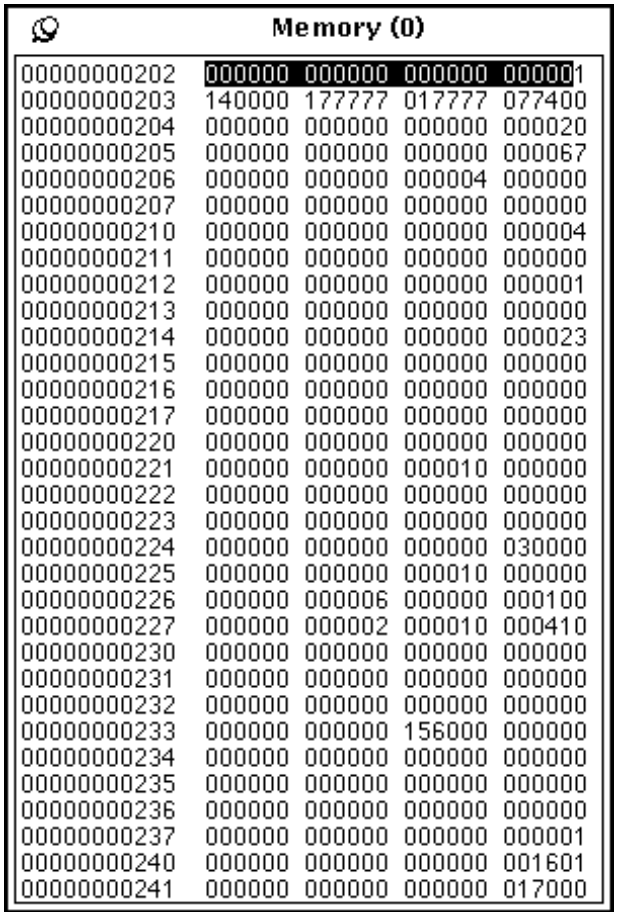
The following procedure describes how to configure and use `cmt11` to provide the most stress on the memory-to-CP path. (Use Fast clock to check for multiple-bit errors and miscompares.)

1. Load the appropriate version of `cmt` (`cmt.t` or `cmt.e`) into MME environment 1.

2. Deselect all sections except section 11 (`cmt11.t` or `cmt11.e`).

3. Use the View -> Memory command to change memory location 202 from 77 to 1. (Refer to Figure 6.)

Figure 6. Setting Memory Location 202 to 1



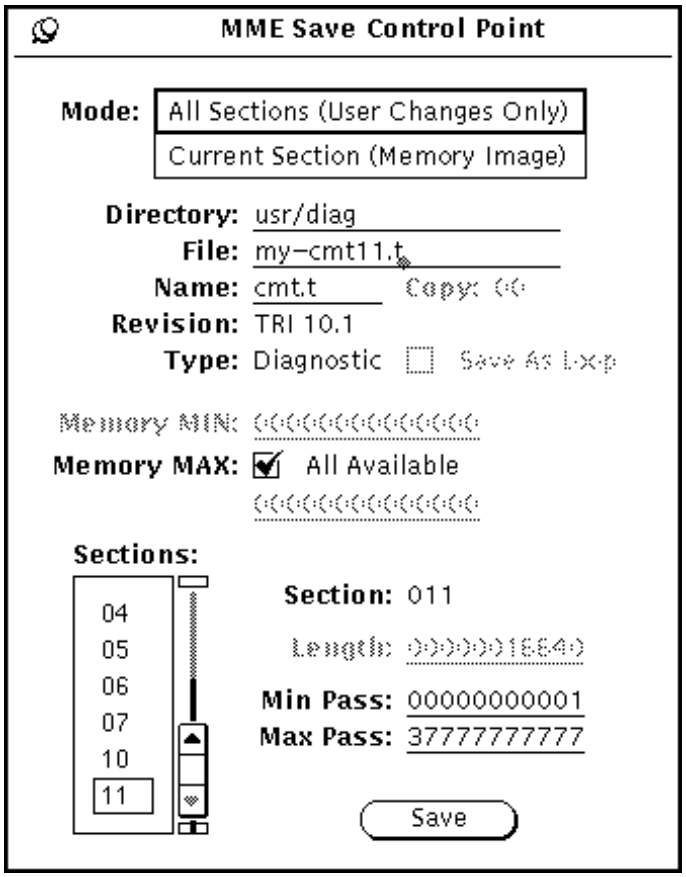
This process selects only condition 0. (Condition 0 writes an alternating pattern of all 0's and all 1's. This data pattern draws the most current and causes all transistors to turn on at the same level at the same time, which stresses crosstalk issues.)

4. Change memory location 204 from 20 to 0. (This specifies that the test should continue when it encounters an error.)

5. Use the File -> Save -> Control Point command to save the control point so you can load multiple copies in environment 2. (Refer to Figure 7.)

   - Use the All Sections (User Changes Only) mode.
   - Enter the filename in the File field.

Figure 7. Saving the Modified Control Point



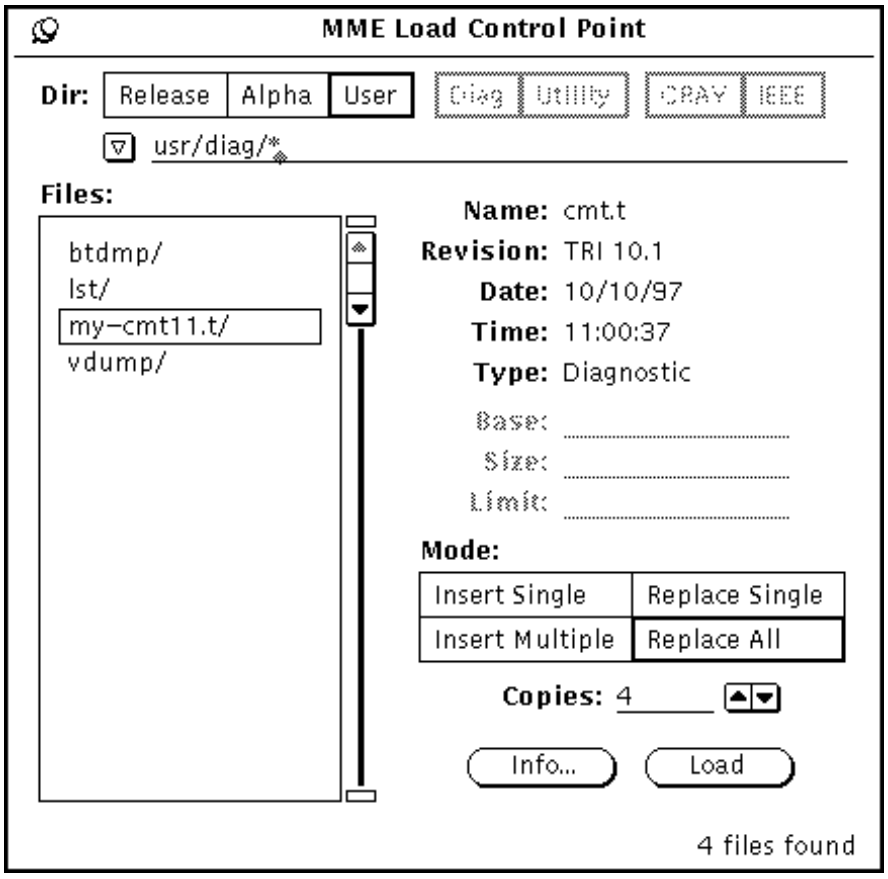
6. Use the Properties -> Environment -> ENV2 command to switch to environment 2. (In environment 2, you can load multiple copies of the control point, so each CPU can run a copy of the control point.)

7. Use the File -> Load -> Control Point command to load your modified version of the control point. (Refer to Figure 8.)

    - Click on the Dir: User setting to access your modified control point.

    - Click on the Load button to load the control point (or double click on the filename in the Files box).

Figure 8. Loading Your Modified Control Point



8. Click on the Go button in the Mainframe Maintenance Environment window to start the test.

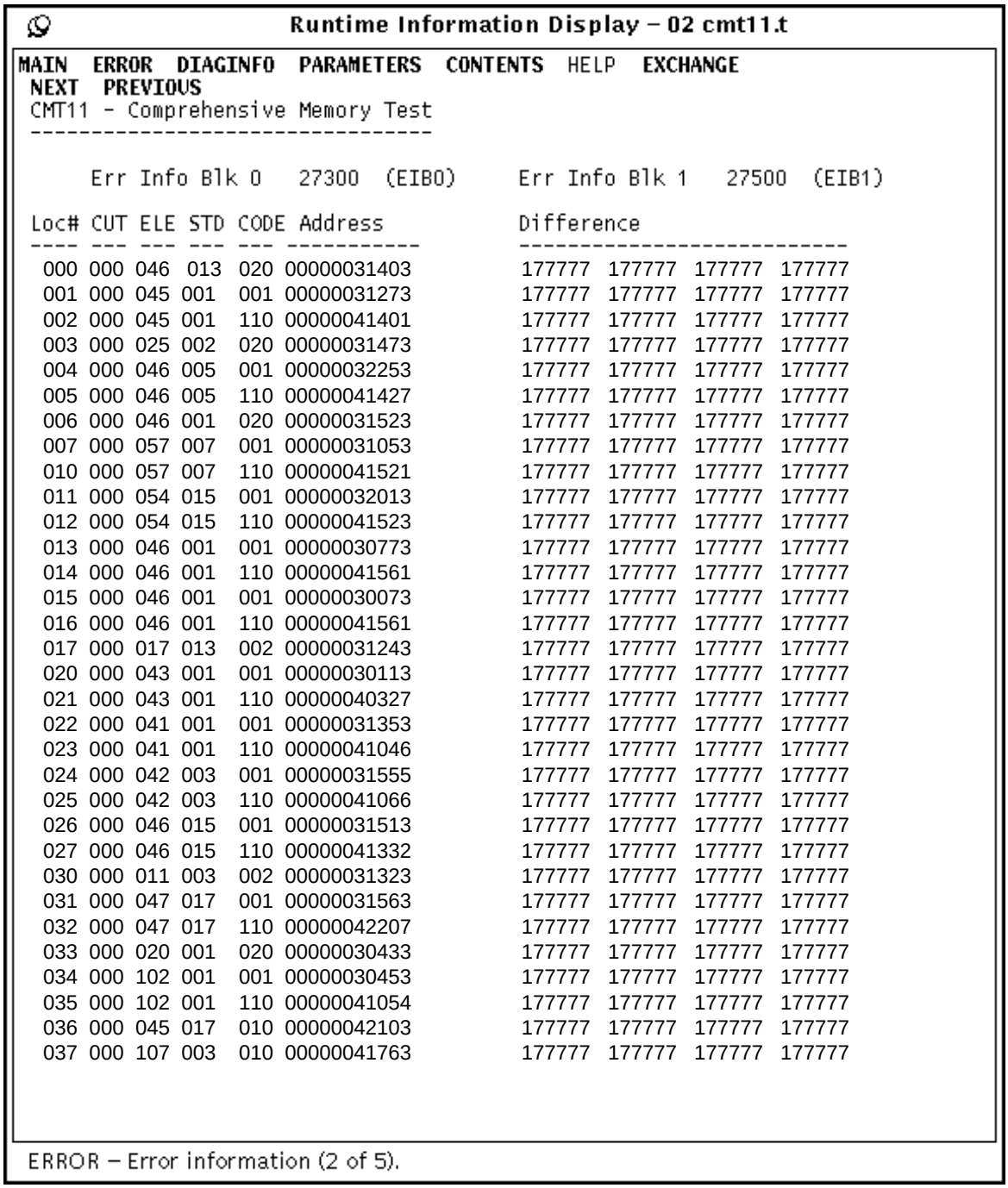
9. When a failure occurs, click on the failing CPU in the Control Points scroll box.

10. Use the View -> Runtime Information -> Current command to display the runtime information for the control point.

11. Click on ERROR to view the error information displays.

12. Click on NEXT to view the error information blocks. (Refer to Figure 9.)

Figure 9. Viewing the Error Information Blocks for the Failing CPU



Runtime Information Display – 02 cmt11.t

MAIN ERROR DIAGINFO PARAMETERS CONTENTS HELP EXCHANGE
NEXT PREVIOUS

CMT11 - Comprehensive Memory Test

Err Info Blk 0 27300 (EIB0) Err Info Blk 1 27500 (EIB1)

Loc#	CUT	ELE	STD	CODE	Address	Difference
000	000	046	013	020	00000031403	177777 177777 177777 177777
001	000	045	001	001	00000031273	177777 177777 177777 177777
002	000	045	001	110	00000041401	177777 177777 177777 177777
003	000	025	002	020	00000031473	177777 177777 177777 177777
004	000	046	005	001	00000032253	177777 177777 177777 177777
005	000	046	005	110	00000041427	177777 177777 177777 177777
006	000	046	001	020	00000031523	177777 177777 177777 177777
007	000	057	007	001	00000031053	177777 177777 177777 177777
010	000	057	007	110	00000041521	177777 177777 177777 177777
011	000	054	015	001	00000032013	177777 177777 177777 177777
012	000	054	015	110	00000041523	177777 177777 177777 177777
013	000	046	001	001	00000030773	177777 177777 177777 177777
014	000	046	001	110	00000041561	177777 177777 177777 177777
015	000	046	001	001	00000030073	177777 177777 177777 177777
016	000	046	001	110	00000041561	177777 177777 177777 177777
017	000	017	013	002	00000031243	177777 177777 177777 177777
020	000	043	001	001	00000030113	177777 177777 177777 177777
021	000	043	001	110	00000040327	177777 177777 177777 177777
022	000	041	001	001	00000031353	177777 177777 177777 177777
023	000	041	001	110	00000041046	177777 177777 177777 177777
024	000	042	003	001	00000031555	177777 177777 177777 177777
025	000	042	003	110	00000041066	177777 177777 177777 177777
026	000	046	015	001	00000031513	177777 177777 177777 177777
027	000	046	015	110	00000041332	177777 177777 177777 177777
030	000	011	003	002	00000031323	177777 177777 177777 177777
031	000	047	017	001	00000031563	177777 177777 177777 177777
032	000	047	017	110	00000042207	177777 177777 177777 177777
033	000	020	001	020	00000030433	177777 177777 177777 177777
034	000	102	001	001	00000030453	177777 177777 177777 177777
035	000	102	001	110	00000041054	177777 177777 177777 177777
036	000	045	017	010	00000042103	177777 177777 177777 177777
037	000	107	003	010	00000041763	177777 177777 177777 177777

ERROR – Error information (2 of 5).

13. Look at the CODE column in Figure 9. Look for values that have only one bit set (for example, 1, 10, 20, etc.) These are reads. (Ignore values that are in the 100 range [100, 110, 120, etc.] because these values are writes.)

    For example, in Figure 9, location number 0 contains the following information:

    ```
    000  000  046   013   020  00000031403
    ```

    The CODE column contains 020, which indicates that the failure occurred during a read.

14. Look at the address to determine the section. (Use the last digit of the address and Table 1 to determine the section.)

    Table 1. Section Indicated by the Last Digit of an Address

Global Address Last Digit	Physical Memory Section [a]		
	8-section Mode	4-section Lower Mode	4-section Upper Mode
0	0	0	7
1	1	1	6
2	2	2	5
3	3	3	4
4	4	3	4
5	5	2	5
6	6	1	6
7	7	0	7

[a] Refer to "Determining the Physical Memory Section from the Global Address in 4-section Mode" on page 26 for more information about how to determine the physical memory section from the last digit of the global address.

    In the example in Figure 9, the address is 00000031403, so the last digit is 3. The failing section is either section 3 (if the system is configured in 8-section mode or 4-section [lower] mode) or section 4 (if the system is configured in 4-section [upper] mode).

15. Enable only the processors on the same SIB level as the failing processor.

    Table 2 lists the CP modules that are connected to the same SIB layers in CRAY T916 mainframes.

    Table 2. CP Modules Connected to SIB Layers (CRAY T916 Mainframes)

SIB Layer	CP Modules
1	0, 10
2	1, 11
3	2, 12
4	3, 13
5	4, 14
6	5, 15
7	6,16
8	7, 17

    Table 3 lists the CP modules that are connected to the same SIB layers in CRAY T932 mainframes.

    Table 3. CP Modules Connected to SIB Layers (CRAY T932 Mainframes)

SIB Layer	CP Modules
1	0, 10, 20, 30
2	1, 11, 21, 31
3	2, 12, 22, 32
4	3, 13, 23, 33
5	4, 14, 24, 34
6	5, 15, 25, 35
7	6, 16, 26, 36
8	7, 17, 27, 37

16. Remove one of the failing CP modules from the configuration and run the test again. If the other CP modules do not have errors, there is crosstalk on the SIB.

Network Module Failures

Network module failures can cause double-bit memory errors, single-bit memory errors, and CPU hangs.

If both sides of a network module are bad (both odd and even subsections), take the clock fibre off and reconnect it. (If necessary, clean it and measure it.) If it still fails, swap the fibres to another board and see if the failure moves to the new board. If the failure stays with the module, it is a network module failure. If the problem moves to the new location, it is a clock problem.

Note: Do not perform these operations on network modules that have cut fibres. Refer to the installation report for information about any network module fibres in the system that have been cut. If you cannot determine whether the system includes network modules with cut fibres, contact Hardware Product Support (HPS) for more information.

Reference Information

This section provides the following reference information:

- Guidelines for using spare chips
- Guideline for replacing memory module stacks
- Tables of flawable syndrome values
- Information about CRAY T916 memory module stack isolation
- Information about determining the physical memory section from the global address in 4-section lower mode or 4-section upper mode

Guidelines for Using Spare Chips

Use the following guidelines to determine whether you should use the SCE spare-chip management function to flaw a chip so that a spare chip replaces the flawed chip.

Single-byte Errors

A single-byte error (SBE) means that 1 to 2 bits are failing on the same memory chip.

During a 24-hour period, a memory chip that exhibits a consistent or increasing SBE failure rate is a possible candidate for flawing. Monitor the frequency of failures over a 7-day period; at least 250 hits per day over a 7-day period should occur before you consider flawing the chip. However, use the spare chip feature before system performance is compromised.

Bursting Memory Chips

A burst is defined as multiple SBEs that are logged rapidly in a short time. Bursts are not counted in specific numbers; for example, more than 500 hits in 1 second would be considered a burst.

During a 24-hour period, a memory chip that experiences one burst is not a candidate for flawing. If the chip experiences more than three bursts during a 24-hour period, consider flawing the chip.

During a 7-day period, a memory chip that experiences one burst is not a candidate for flawing. If the burst repeats on more than 3 days during a 7-day period, consider flawing the chip.

Note: You should log all SBEs as they occur for individual modules. If a module is returned to Central Repair for a double-bit error or meets the criteria to be returned for flaws, this log and the flaw map should accompany the module. The log enables Central Repair to change chips that do not currently meet the criteria for flawing but that may fail more seriously in the future.

Guideline for Replacing Memory Module Stacks

Cray Research recommends that you replace a memory module stack when a second SBE in one bank occurs (in the same half of the word). Replace the memory module stack at the next convenient time for the customer.

Flawable Syndromes

Table 4 lists the flawable syndromes for CM03 module correctable errors.

Table 4. Flawable Syndromes for CM03 Modules (Correctable Errors)

Bits (A, B, C, D [a])	Syndrome					
	A	B	C	D	AB	CD
0, 16, 1, 17	0105	0212	0405	1012	0317	1417
2, 18, 3, 19	2005	4012	2505	5212	6017	7717
4, 20, 5, 21	7105	3612	5505	6612	4717	3317
6, 22, 7, 23	2024	4050	0025	0052	6074	0077
8, 24, 9, 25	2425	5052	4427	7051	7477	3476
10, 26, 11, 27	6426	3053	2120	4240	5475	6360
12, 28, 13, 29	0124	0250	2125	4252	0374	6377
14, 30, 15, 31	2136	4247	2133	4255	6371	6366
32, 48, 33, 49	0501	1202	0504	1210	1703	1714
34, 50, 35, 51	0520	1240	0525	1252	1760	1777
36, 52, 37, 53	0571	1236	0555	1266	1747	1733
38, 54, 39, 55	2420	5040	2500	5200	7460	7700
40, 56, 41, 57	2424	5250	2744	5170	7774	7634
42, 58, 43, 59	2664	5330	2021	4042	7554	6063
44, 60, 45, 61	2401	5002	2521	5242	7403	7763
46, 62, 47, 63	3621	4742	3321	5542	7163	6663
64, 67, 65, 68	0001	0002	0004	0010	0003	0014
66, 69, 72, 75	0020	0040	2000	4000	0060	6000
70, 73, 71, 74	0100	0200	0400	1000	0300	1400

[a] If you flaw one pair of bits (A, B or C, D), the other pair is also flawed.

Table 5 lists the flawable syndromes for CM03 module uncorrectable errors.

Table 5. Flawable Syndromes for CM03 Modules (Uncorrectable Errors)

Bits (A, B, C, D[a])	Syndrome								
	AC	AD	BC	BD	ABC	ABD	ACD	BCD	ABCD
0, 16, 1, 17	0500	1117	0617	1200	0712	1305	1512	1605	1700
2, 18, 3, 19	0500	7217	6517	1200	4512	3205	5712	3705	1700
4, 20, 5, 21	2400	1717	6317	5000	1212	2105	4212	0505	7400
6, 22, 7, 23	2001	2076	4075	4002	6051	6026	2053	4027	6003
8, 24, 9, 25	6002	5474	1475	2003	3050	0426	1053	6424	4001
10, 26, 11, 27	4506	2666	1173	7213	7555	1635	0746	5333	3715
12, 28, 13, 29	2001	4376	2375	4002	2251	4126	6253	6127	6003
14, 30, 15, 31	0005	6363	6374	0012	4242	2124	4250	2121	0017
32, 48, 33, 49	0005	1711	1706	0012	1207	0513	1215	0516	0017
34, 50, 35, 51	0005	1772	1765	0012	1245	0532	1257	0537	0017
36, 52, 37, 53	0024	1717	1763	0050	1212	0521	1242	0505	0074
38, 54, 39, 55	0120	7620	7540	0240	5160	2660	5320	2740	0360
40, 56, 41, 57	0260	7454	7514	0320	5030	2604	5310	2464	0140
42, 58, 43, 59	0645	6626	7311	1372	5575	3516	4607	3353	1537
44, 60, 45, 61	0120	7643	7523	0240	5122	2641	5362	2761	0360
46, 62, 47, 63	0500	6363	7463	1200	4242	2421	5042	2121	1700
64, 67, 65, 68	0005	0011	0006	0012	0007	0013	0015	0016	0017
66, 69, 72, 75	2020	4020	2040	4040	2060	4060	6020	6040	6060
70, 73, 71, 74	0500	1100	0600	1200	0700	1300	1500	1600	1700

[a] If you flaw one pair of bits (A, B or C, D), the other pair is also flawed.

Table 6 lists the flawable syndromes for CM02 and CM04 module correctable errors.

Table 6. Flawable Syndromes for CM02 and CM04 Modules (Correctable Errors)

Bits (A, B[a])	Syndrome		
	A	B	AB
0, 16	0105	0212	0317
1, 17	0405	1012	1417
2, 18	2005	4012	6017
3, 19	2505	5212	7717
4, 20	7105	3612	4717
5, 21	5505	6612	3317
6, 22	2024	4050	6074
7, 23	0025	0052	0077
8, 24	2425	5052	7477
9, 25	4427	7051	3476
10, 26	6426	3053	5475
11, 27	2120	4240	6360
12, 28	0124	0250	0374
13, 29	2125	4252	6377
14, 30	2136	4247	6371
15, 31	2133	4255	6366
32, 48	0501	1202	1703
33, 49	0504	1210	1714
34, 50	0520	1240	1760
35, 51	0525	1252	1777
36, 52	0571	1236	1747
37, 53	0555	1266	1733
38, 54	2420	5040	7460
39, 55	2500	5200	7700
40, 56	2424	5250	7774
41, 57	2744	5170	7634
42, 58	2664	5330	7554
43, 59	2021	4042	6063
44, 60	2401	5002	7403
45, 61	2521	5242	7763
46, 62	3621	4742	7163
47, 63	3321	5542	6663

Table 6. Flawable Syndromes for CM02 and CM04 Modules (Correctable Errors) (continued)

Bits (A, B[a])	Syndrome		
	A	B	AB
64, 67	0001	0002	0003
65, 68	0004	0010	0014
66, 69	0020	0040	0060
70, 73	0100	0200	0300
72, 75	2000	4000	6000
71, 74	0400	1000	1400

[a] If you flaw one bit (A or B), the other bit is also flawed.

CRAY T916 Memory Module Stack Isolation for CM02 Modules

Table 7 shows the correlation between chip locations, banks, and sections on CM02 modules for CRAY T916 mainframes.

Table 7. Correlation of Chip Locations, Banks, and Sections for CM02 Modules in CRAY T916 Mainframes

Bits	Mode	Chip Location	Banks	Sections
Lower Bits	Bank Bit 2^1 Forced to 0	AB	0, 4	0, 2
		AC	1, 5	
		BB	0, 4	1, 3
		BC	1, 5	
	Bank Bit 2^1 Forced to 1	AD	2, 6	4, 6
		AE	3, 7	
		BD	2, 6	5, 7
		BE	3, 7	
Upper Bits	Bank Bit 2^1 Forced to 0	AF	0, 4	0, 2
		AG	1, 5	
		BF	0, 4	1, 3
		BG	1, 5	
	Bank Bit 2^1 Forced to 1	AH	2, 6	4, 6
		AI	3, 7	
		BH	2, 6	5, 7
		BI	3, 7	

CRAY T916 Memory Module Stack Isolation for CM03 Modules

Table 8 shows the correlation between chip locations, banks, and sections on CM03 modules for CRAY T916 mainframes.

Table 8. Correlation of Chip Locations, Banks, and Sections for CM03 Modules in CRAY T916 Mainframes

Bits	Mode	Chip Location	Banks	Sections
Lower Bits	Bank Bit 2^1 Forced to 0	AB	0, 4,10,14	0, 2
		AD	1,5,11,15	
		BB	0, 4,10,14	1, 3
		BD	1,5,11,15	
	Bank Bit 2^1 Forced to 1	AF	2, 6,12,16	4, 6
		AH	3, 7,13,17	
		BF	2, 6,12,16	5, 7
		BH	3, 7,13,17	
Upper Bits	Bank Bit 2^1 Forced to 0	AC	0, 4,10,14	0, 2
		AE	1,5,11,15	
		BC	0, 4,10,14	1, 3
		BE	1,5,11,15	
	Bank Bit 2^1 Forced to 1	AG	2, 6,12,16	4, 6
		AI	3, 7,13,17	
		BG	2, 6,12,16	5, 7
		BI	3, 7,13,17	

CRAY T916 Memory Module Stack Isolation for CM04 Modules

Table 9 shows the correlation between chip locations, banks, and sections on CM04 modules for CRAY T916 mainframes.

Table 9. Correlation of Chip Locations, Banks, and Sections for CM04 Modules in CRAY T916 Mainframes

Bits	Mode	Chip Location	Banks	Sections
Lower Bits	Bank Bit 2^1 Forced to 0	AB	0, 4,10,14	0, 2
		AC	1,5,11,15	
		BB	0, 4,10,14	1, 3
		BC	1,5,11,15	
	Bank Bit 2^1 Forced to 1	AD	2, 6,12,16	4, 6
		AE	3, 7,13,17	
		BD	2, 6,12,16	5, 7
		BE	3, 7,13,17	
Upper Bits	Bank Bit 2^1 Forced to 0	AF	0, 4,10,14	0, 2
		AG	1,5,11,15	
		BF	0, 4,10,14	1, 3
		BG	1,5,11,15	
	Bank Bit 2^1 Forced to 1	AH	2, 6,12,16	4, 6
		AI	3, 7,13,17	
		BH	2, 6,12,16	5, 7
		BI	3, 7,13,17	

Determining the Physical Memory Section from the Global Address in 4-section Mode

The lower 3 bits in the global address are the section bits. Normally, these bits directly correspond to the physical memory section (for example, a 1 indicates section 1, a 3 indicates section 3, and a 7 indicates section 7.)

When you configure a system in 4-section mode, the bits for the sections that are mapped out (sections 4, 5, 6, an 7 in 4-section lower mode and sections 0, 1, 2, and 3 in 4-section upper mode) are inverted to maintain cache coherency.

Refer to Table 10 and Table 11. These tables show how the last digit of the global address relates to physical memory sections in 4-section mode.

Table 10. Relation of Global Address to Physical Memory Section (4-section Lower Mode)

Global Address Digit	Original Value			Inverted Value			Physical Memory Section
	Bit 2	Bit 1	Bit 0	Bit 2	Bit 1	Bit 0	
0	0	0	0	--	--	--	0
1	0	0	1	--	--	--	1
2	0	1	0	--	--	--	2
3	0	1	1	--	--	--	3
4	1	0	0	0	1	1	3
5	0	0	1	0	1	0	2
6	1	1	0	0	0	1	1
7	1	1	1	0	0	0	0

Table 11. Relation of Global Address to Physical Memory Section (4-section Upper Mode)

Global Address Digit	Original Value			Inverted Value			Physical Memory Section
	Bit 2	Bit 1	Bit 0	Bit 2	Bit 1	Bit 0	
0	0	0	0	1	1	1	7
1	0	0	1	1	1	0	6
2	0	1	0	1	0	1	5
3	0	1	1	1	0	0	4
4	1	0	0	--	--	--	4
5	0	0	1	--	--	--	5
6	1	1	0	--	--	--	6
7	1	1	1	--	--	--	7

You should be aware of these changes when you work with any software that reports a global address (for example, the `cmt11` diagnostic test.)

Note: The error logger reports the actual physical memory section of a failure.

Troubleshooting Hints

Be aware of the following hints when you troubleshoot double-bit memory errors:

- If there are simultaneous errors from two memory sections that are in the same CM stack (especially if there are multiple subsections), check `nwacs` for a power supply failure. (Power supplies can fail without issuing a warning.)

  This condition rarely occurs, but it has occurred on two systems. Usually, after the failure, everything appears to run correctly because the power supply affects only the bus as the power supply fails. Identifying the failure can be confusing if you do not remember to check `nwacs`.

- You can use the MME environment 0 memory test to verify a failing path. To do this, select the write CPU and/or disable other CPUs. Testing with this configuration indicates whether an error is on the read path or the write path from a CPU to memory. It works only for fairly solid errors and mainly provides more detailed information that you can use to repair the failure. You will usually already know that this a problem, such as a solid SBE; however, this process isolates it to either the read or write path.