IOS MODEL C CHASSIS MAP

	A	B	C	D	
72	2YH ERROR LOG	2YI MAINTENANCE DATA	2YB-5 00-03	2YB-5 00-03	49
71					
70	2YJ MAINTENANCE CONTROL	3TO-1 1ST CLOCK	2YB-5 04-07	2YB-5 04-07	48
69					
68	2YP 00-07	3TC-1 2ND CLOCK	2YB-5 08-11	2YB-5 08-11	47
67			2YB-5 12-15	2YB-5 12-15	46
66	08-15	2YF GROUP 0 WRITE	2YB-5 16-19	2YB-5 16-19	45
65	HISP BUFFER				
64	16-23	2YF GROUP 0 READ	2YB-5 20-23	2YB-5 20-23	44
63		SECDED			
62	24-31	2YF GROUP 1 WRITE	2YB-5 24-27	2YB-5 24-27	43
61			2YB-5 28-31	2YB-5 28-31	42
60	2YP 32-39	2YF GROUP 1 READ	2YB-5 32-35	2YB-5 32-35	41
59					
58	2YO HISP ADDRESS/BL	2YG GROUP CONTROL	2YB-5 36-39	2YB-5 36-39	40
57			2YB-5 40-43	2YB-5 40-43	39
56	2YP 40-47	2YM ADDRESS	2YB-5 44-47	2YB-5 44-47	38
55					
54	48-55	2YK MAIN CONTROL	2YB-5 48-51	2YB-5 48-51	37
53	HISP BUFFER				
52	56-63	2YL 00-11	2YB-5 52-55	2YB-5 52-55	36
51			2YB-5 56-59	2YB-5 56-59	35
50	2YP S0-S7	12-23	2YB-5 60-63	2YB-5 60-63	34
49					
48	2YR HISP CONTROL	DATA 24-35	2YB-5 S0-S3	2YB-5 S0-S3	33
47		FANIN			
46	2YZ 00-23	FANOUT 36-47	2YB-5 S4-S7	2YB-5 S4-S7	32
45			2YB-5 00-03	2YB-5 32-35	31
44	24-47	48-59	2YB-5 04-07	2YB-5 36-39	30
43	VHISP DATA		2YB-5 08-11	2YB-5 40-43	29
42	48-71	2YL 60-63 S0-S7	2YB-5 12-15	2YB-5 44-47	28
41					
40	00-23		2YB-5 16-19	2YB-5 48-51	27
39		2NR BUFFER MEMORY PRO 0,1 SEC 0,2	2YB-5 20-23	2YB-5 52-55	26
38	24-47				
37		2NR READ DATA PRO 2,3 SEC 1,3	2YB-5 24-27	2YB-5 56-59	25
36	2YZ 48-71				
35		2NW WRITE DATA	2YB-5 28-31	2YB-5 60-63	24
34	2YY VHISP CONTROL		2YB-1 00-03	2YB-5 S0-S3	23
33		2NA ADDRESS	2YB-1 04-07	2YB-5 S4-S7	22
32					
31	2IK LOSP4 OUTPUT	2NC CONTROL	2YB-1 08-11	2YB-5 00-03	21
30					
29	2IL LOSP4 ACCUMULATOR	2NX XOVER 0,1	2YB-1 12-15	2YB-5 04-07	20
28		2NX XOVER 2,3			
27	2II LOSP4 CONTROL	2BZ0 SEC 0 0-7	2YB-1 CB's	2YB-5 08-11	19
26		LOCAL			
25	2IJ LOSP4 INPUT	2BZ1 SEC 1 0-7	2YB-1 00-03	2YB-5 12-15	18
24					
23	2IV HSX INPUT	2BZ2 SEC 2 0-7	2YB-1 04-07	2YB-5 16-19	17
22		MEMORY			
21	2IU HSX OUTPUT	2BZ3 SEC 3 0-7	2YB-1 08-11	2YB-5 20-23	16
20					
19	2BZ0 SEC 0 0-7	2BR EVEN BITS	2YB-1 12-15	2YB-5 24-27	15
18	LOCAL	ACCUMULATOR			
17	2BZ1 SEC 1 0-7	2BR REGISTERS ODD BITS	2YB-1 CB's	2YB-5 28-31	14
16					
15	2BZ2 SEC 2 0-7	2BA ADDER	2YB-1 00-03	2YB-5 32-35	13
14	MEMORY				
13	2BZ3 SEC 3 0-7	2BI INSTRUCTION STACK	2YB-1 04-07	2YB-5 36-39	12
12					
11	2BR EVEN BITS	2BT ISSUE CONTROL	2YB-1 08-11	2YB-5 40-43	11
10	ACCUMULATOR				
9	2BR REGISTERS ODD BITS	2BO LOCAL MEMORY CONTROL	2YB-1 12-15	2YB-5 44-47	10
8					
7	2BA ADDER	2BZ4 SEC 0 8-15	2YB-1 CB's	2YB-5 48-51	9
6		LOCAL			
5	2BI INSTRUCTION STACK	2BZ5 SEC 1 8-15	2YB-1 00-03	2YB-5 52-55	8
4					
3	2BT ISSUE CONTROL	2BZ6 SEC 2 8-15	2YB-1 04-07	2YB-5 56-59	7
2		MEMORY			
1	2BO LOCAL MEMORY CONTROL	2BZ7 SEC 3 8-15	2YB-1 08-11	2YB-5 60-63	6
0					
0	2BZ4 SEC 0	2BC I/O ADDRESS	2YB-1 12-15	2YB-5 S0-S3	5
1	LOCAL				
2	2BZ5 SEC 1 8-15	2BH EXIT STACK	2YB-1 CB's	2YB-5 S4-S7	4
3					
4	2BZ6 SEC 2 8-15	2BK HSP LOSP MOS CONTROL	2IS HISP INPUT	2IS HISP INPUT	3
5	MEMORY				
6	2BZ7 SEC 3 8-15	2BL ADDRESS, BL REGISTERS			2
7					
8	2BC I/O ADDRESS	2BM CONSOLE I/O INTERRUPTS	2IR HISP OUTPUT	2IR HISP OUTPUT	1
9					
10	2BH EXIT STACK	2BP HISP OUTPUT LOSP MOS INP			0
11					
12	2BK HSP LOS MOS CONTROL	2BQ HISP INPUT SECDED	2BZ0 SEC 0 0-7	2BZ0 SEC 0 0-7	0
13			LOCAL	LOCAL	
14	2BL ADDRESS, BL REGISTERS	2BU HISP BYPASS LSP MOS OUT	2BZ1 SEC 1 0-7	2BZ1 SEC 1 0-7	1
15					
16	2BM CONSOLE I/O, INTERRUPTS	2IH DMAO EXPANDER INTR.	2BZ2 SEC 2 0-7	2BZ2 SEC 2 0-7	2
17			MEMORY	MEMORY	
18	2BP HISP OUTPUT LSP MOS INP	2IJ DMAI 20-27	2BZ3 SEC 3 0-7	2BZ3 SEC 3 0-7	3
19		LSP4			
20	2BQ HISP INPUT SECDED	2IJ DMA2 30-37	2BR EVEN BITS	2BR EVEN BITS	4
21		INPUT	ACCUMULATOR	ACCUMULATOR	
22	2BU HISP BYPASS LOSP MOS OUT	2II DMAI 20-27	2BR REGISTERS ODD BITS	2BR REGISTERS ODD BITS	5
23		LSP4			
24	2IY DMAO 20-23	2II DMA2 30-37	2BA ADDER	2BA ADDER	6
25	BMC5	CONTROL			
26	2IY DMAI 24-27	2IL DMAI 20-27	2BI INSTRUCTION STACK	2BI INSTRUCTION STACK	7
27	DATA	LSP4			
28	2IY DMA2 30-33	2IL DMA2 30-37	2BT ISSUE CONTROL	2BT ISSUE CONTROL	8
29		ACCUMULATOR			
30	2IX DMAO 20-23	2IK DMAI 20-27	2BO LOCAL MEMORY CONTROL	2BO LOCAL MEMORY CONTROL	9
31	BMC5	LSP4			
32	2IX DMAI 24-27	2IK DMA2 30-37	2BZ4 SEC 0 8-15	2BZ4 SEC 0 8-15	10
33	CONTROL	OUTPUT	LOCAL	LOCAL	
34	2IX DMA2 30-33	2BX ERROR MULTIPLEX	2BZ5 SEC 1 8-15	2BZ5 SEC 1 8-15	11
35					
36	2IW DMAO CH 20	3TC-1 2ND CLOCK	2BZ6 SEC 2 8-15	2BZ6 SEC 2 8-15	12
37	BMC5		MEMORY	MEMORY	
38	2IW DMAO CH 21	3TO-2 1ST CLOCK	2BZ7 SEC 3 8-15	2BZ7 SEC 3 8-15	13
39					
40	2IW DMAO CH 22	2BV DEADSTART / MASTER CLR	2BC I/O ADDRESS	2BC I/O ADDRESS	14
41	CHANNEL				
42	2IW DMAO CH 23		2BH EXIT STACK	2BH EXIT STACK	15
43		2IG CONSOL INTR			
44	2IW DMAI CH 24	2IE DMAO CH 20	2BK HSP LOS MOS CONTROL	2BK HSP LOS MOS CONTROL	16
45	BMC5	DCU5			
46	2IW DMAI CH 25	2IE DMAO CH 21	2BL ADDRESS, BL REGISTERS	2BL ADDRESS, BL REGISTERS	17
47					
48	2IW DMAI CH 26	2IE DMAO CH 22	2BM CONSOLE I/O, INTERRUPTS	2BM CONSOLE I/O, INTERRUPTS	18
49	CHANNEL	INTERFACE			
50	2IW DMAI CH 27	2IE DMAO CH 23	2BP HISP OUTPUT LOSP MOS INP	2BP HISP OUTPUT LOSP MOS INP	19
51					
52	2IW DMA2 CH 30	2IE DMAI CH 24	2BQ HISP INPUT SECDED	2BQ HISP INPUT SECDED	20
53	BMC5	DCU5			
54	2IW DMA2 CH 31	2IE DMAI CH 25	2BU HISP BYPASS LOSP MOS OUT	2BU HISP BYPASS LOSP MOS OUT	21
55					
56	2IW DMA2 CH 32	2IE DMAI CH 26	2ID DMAO 20-23	2ID DMAO 20-23	22
57	CHANNEL	INTERFACE	DCU5	DCU5	
58	2IW DMA2 CH 33	2IE DMAI CH 27	2ID DMAI 24-27	2ID DMAI 24-27	23
59					
60	2IZ DMAO 20-21	2IE DMA2 CH 30	2ID DMA2 30-33	2ID DMA2 30-33	24
61	BMC5	DCU5	CONTROL	CONTROL	
62	2IZ DMAO 22-23	2IE DMA2 CH 31	2ID DMA5 34-37	2ID DMA5 34-37	25
63					
64	2IZ DMAI 24-25	2IE DMA2 CH 32	2IE DMAI CH 24	2IE DMAO CH 20	26
65	LEVEL	INTERFACE	DCU5	DCU5	
66	2IZ DMAI 26-27	2IE DMA2 CH 33	2IE DMAI CH 25	2IE DMAO CH 21	27
67		DCU5 INTERFACE			
68	2IZ DMA2 30-31	2IE DMA5 CH 37	2IE DMAI CH 26	2IE DMAO CH 22	28
69	TRANS		INTERFACE	INTERFACE	
70	2IZ DMA2 32-33		2IE DMAI CH 27	2IE DMAO CH 23	29
71					
72	2AZ HSP 6-9 ERR		2AZ HSP 2-5 ERR		30
			2IE DMA2 CH 32	2IE DMA2 CH 30	31
			DCU5 INTERFACE		
			2IE DMA2 CH 33	2IE DMA2 CH 31	32
			2IE DMA5 CH 34	2IE DMA5 CH 34	33
				DCU5	
			2IE DMA5 CH 35	2IE DMA5 CH 35	34
			2IE DMA5 CH 36	2IE DMA5 CH 36	35
				INTERFACE	
				2IE DMA5 CH 37	36
	M	N	O	P	
	IOP3	IOP0	IOP1	IOP2	

NOTE: DMA3 PROC LOSP/MOS
DMA4 PROC HISP