300 Series Disk Systems Guide

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Each time this manual is fully revised and reprinted, all change packets to the previous version are incorporated into the new version, and the new version is assigned an alphabetical revision level, which is indicated in the publication number on each page of the manual. A revised manual does not usually contain change bars.

REVISION	DESCRIPTION
1/28/94	Internal Review

PREFACE

The *300 Series Disk Systems Guide* is designed as a reference manual for Cray Research, Inc. (CRI) field engineers who have had I/O subsystem model E (IOS-E) and 300 series disk systems training. This manual incorporates diagnostic and hardware information relative to disk drive operations.

The following conventions are used throughout this manual:

- `Courier` font indicates directory pathnames, filenames, commands, utilities, and screen output.
- **`Courier bold`** font indicates commands and options that the user should enter.
- *Italic* font indicates a variable or user-supplied entry.
- Commands must be entered as shown in the command syntax. Spaces must be included or left out as shown; do not use tabs.
- The ↵ symbol indicates pressing the return key.
- Control signals for the IPI-2 interface are in capital letters. For example, BUS CONTROL.

If you have any criticisms, comments, or suggestions related to this manual, please fill out a reader comment form and send it back to Hardware Publications and Training. Reader comment forms are located in the front and back of this manual.

INSTALLING NEW DISK ARRAYS
(DCA-3)

1) install hardware + cabling
2) run offline diagnostics (Dms2)
3) Boot Unicos (probably single user mode)
4) execute "mkspice -t da301 -i [1/0 PATH(S)]
   or da60
   or da62
5) use ddms to initialize (label) the arrays "ddms -a scrub [-i Path]
6) use ddms to surf the arrays (optional)
7) give back to customer

DMENU

on techops
/usr/oldiag/toolbox/ddms/7c/dmenu
/array (for Disk arrays)

Put them both in cl/bin

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1 300 SERIES DISK SYSTEM OVERVIEW

A 300 series disk system consists of DD-301 spindles, DW-300 drawers, a DE-100 disk enclosure, and spare spindle(s). The DE-100 contains up to four DW-300 drawers of up to 20 disk drives each, for a total of up to 80 drives per DE-100 Figure 1-1 is a block diagram example of a 300 series disk system.

The system connects to an I/O subsystem model E (IOS-E) through a disk channel adapter, either a DCA-2 or a DCA-3. Disk devices connected to a DCA-2 are referred to as DD-301 disk drives. Five DD-301s connected to a DCA-3 are referred to as a DA-301 disk array.

PRELIMINARY INFORMATION
DO NOT DISSEMINATE

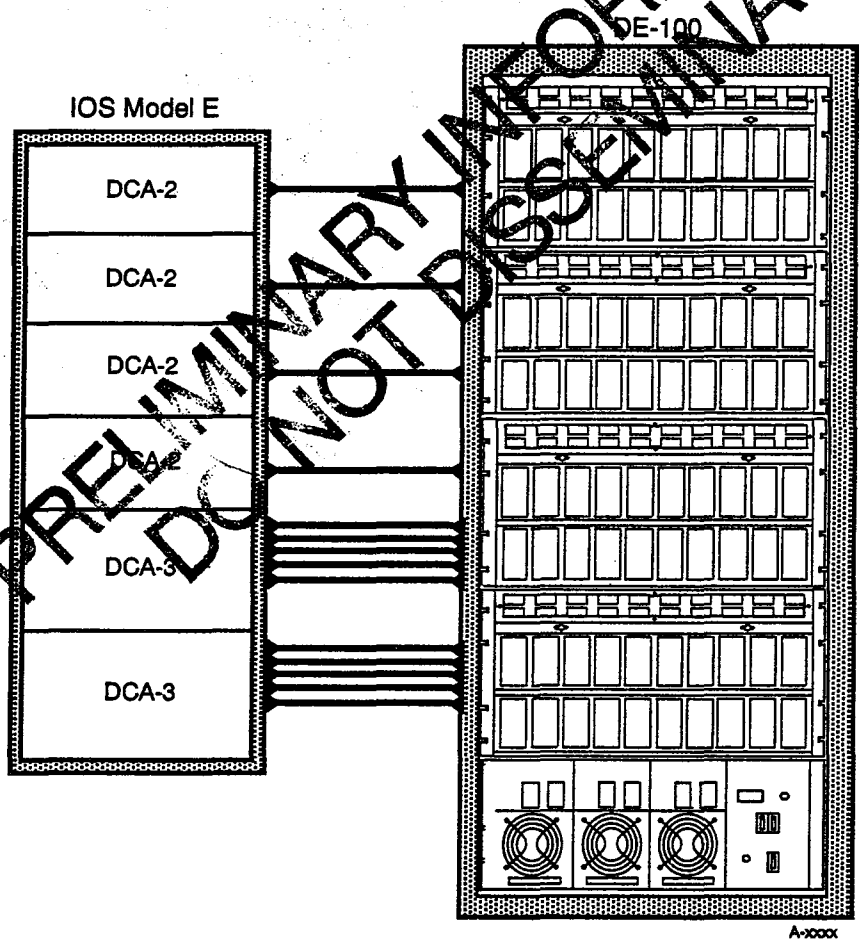


Figure 1-1. 300 Series Disk System Connected to an IOS-E

Disk Devices

The 300 series disk devices provide long-term data storage for a Cray Research, Inc. (CRI) computer system.

DD-301 Disk Drive

The DD-301 is a two-head parallel disk storage unit which connects to a DCA-2 disk channel adaptor. It has a sustained transfer rate of 8.2 Mbytes/sec and a usable storage capacity of ≈1.38 Gbytes. Figure 1-2 shows the DD-301 in a carrier assembly.

One DD-301 contains seven selectable read/write head groups and one servo head. During data transfers, two heads are used simultaneously to read or write data. The servo head transfers head position information to the servo control circuitry in the DD-301.

A sector of data from a DD-301 contains 512 64-bit words of IOP data. Data is transferred between the DD-301 and DCA-2 in blocks of this fixed size. Each track contains 25 sectors where data can be stored and retrieved by the IOS-E.

The DCA-2 creates a sector from two physical sectors in the DD-301 (one from each head in the head group). Each physical sector contains one half of an IOP data sector.

Seven logical tracks make up one cylinder in the DD-301. DD-301s contain 1927 (3607_8) data cylinders, 1 maintenance cylinder, and 2 flaw table cylinders.

DA-301 Disk Array

The DA-301 is a disk array composed of five DD-301 spindles connected to a DCA-3 disk channel adaptor. Four of the spindles store data while the fifth spindle holds parity information. A DA-301 has a sustained transfer rate of 32.8 Mbytes/sec and a storage capacity of 5.51 Gbytes.

A sector of data from a DA-301 contains 2048 64-bit words of IOP data. Data is transferred between the DA-301 and DCA-3 in blocks of this fixed size. Each track contains 25 sectors where data can be stored and retrieved by the IOS-E.

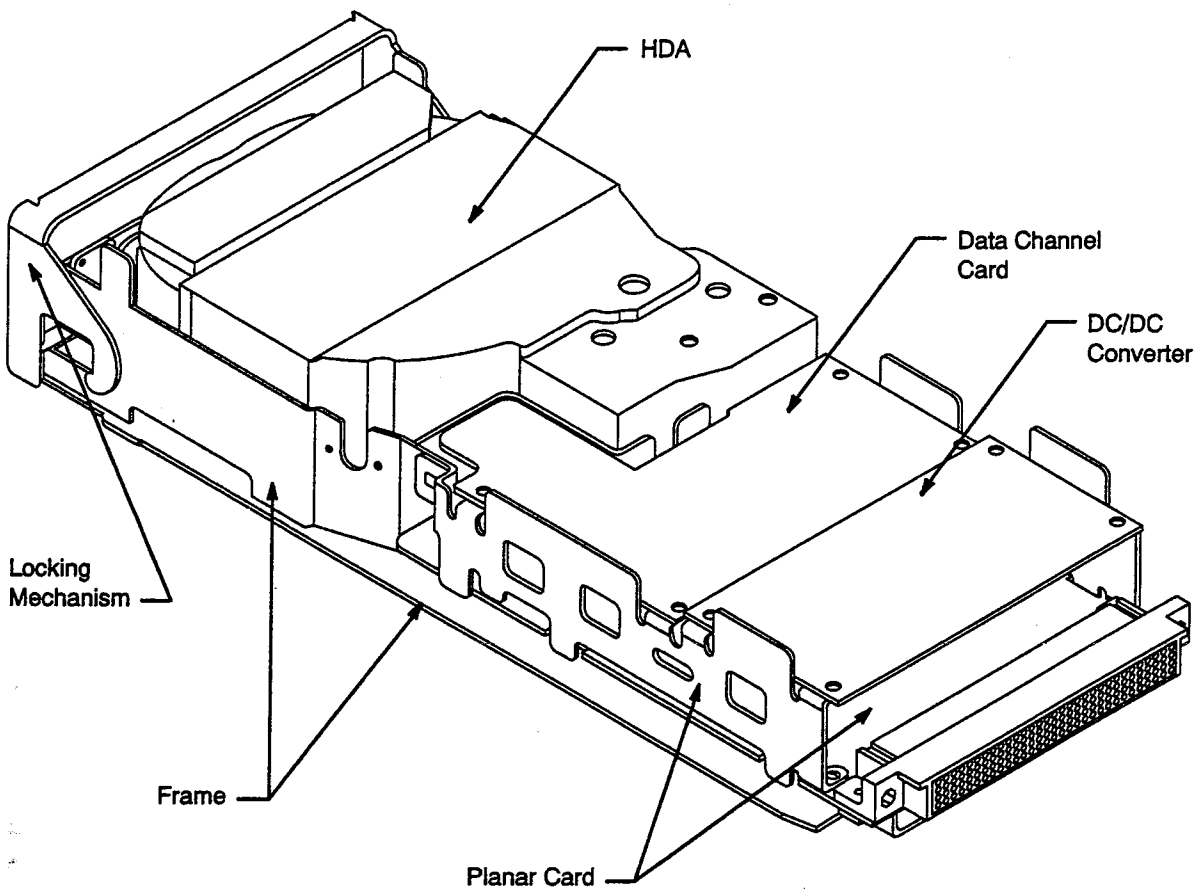


Figure 1-2. DD-301 Assembly

DW-300 Disk Drive Drawer

A disk drive drawer assembly consists of the drawer housing, back plane, cooling fans, ON/OFF breakers and the wiring to distribute power to the back plane power connector. Each DW-300 accommodates up to 20 DD-301s, or 4 DA-301s. Refer to Figure 1-3 for an illustration of the DW-300 front panel. Figure 1-4 shows the rear view of the DW-300.

The drawer may contain from one to 20 spindles depending on the configuration required. Since each slot has an ON/OFF breaker, drives may be replaced without interrupting the operation of other drives.

A resilient fan assembly consisting of three fan units cools a DW-300. If one fan fails, the remaining two fans provide ample cooling. Upon failure the fan will send a signal to the environmental monitoring system to indicate a fan failure has occurred.

The back plane distributes 36 V power and the data signals. Features of the back plane include data and synchronization cable connections, and individual drive address assignment.

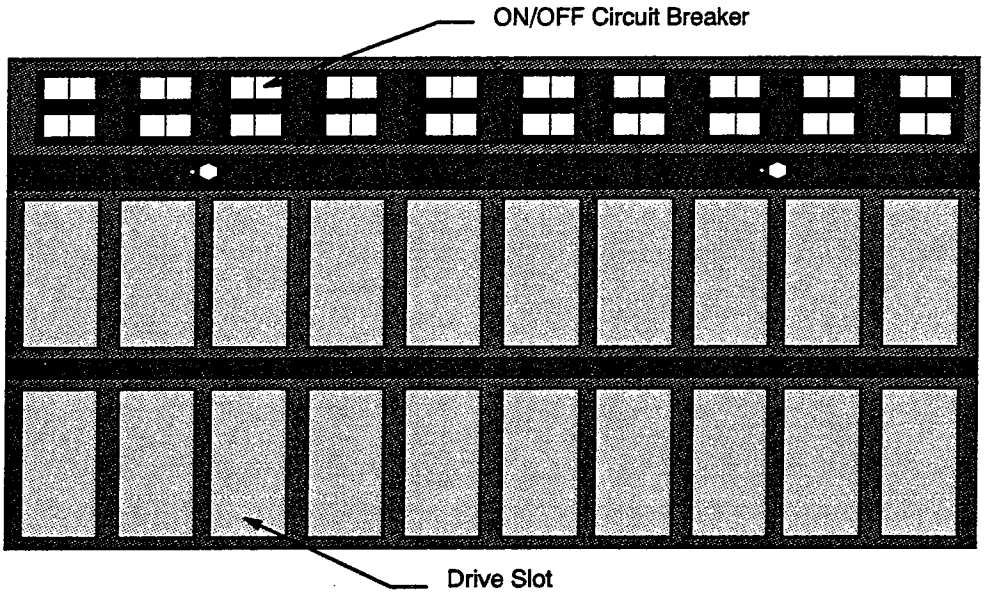


Figure 1-3. DW-300 Front Panel (cover removed)

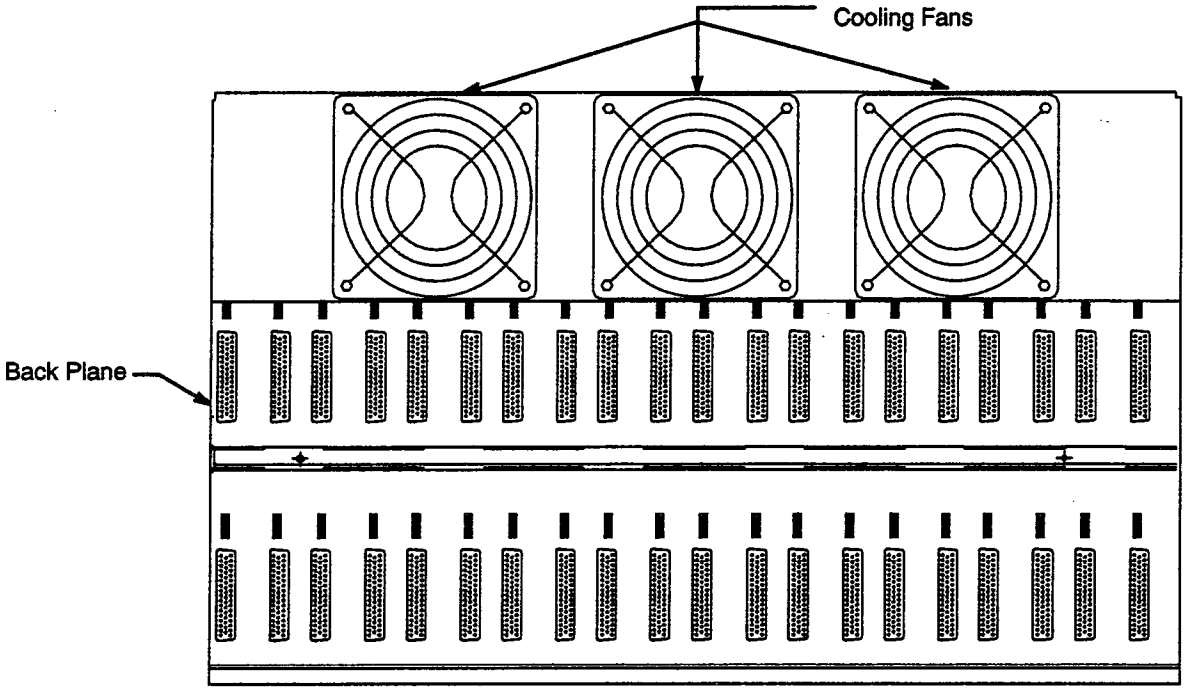


Figure 1-4. DW-300 Rear View

DD-301 Characteristics

DD-301s are 2-head parallel disk drives formatted to Cray Research specifications. Table 1-1 lists the characteristics of the DD-301.

Table 1-1. 300 Series Disk Drive Characteristics

Parameter	DD-301	DA-301
Spindle type	2-head parallel	(5) 2-head parallel
Channel adaptor type	DCA-2	DCA-3
Sustained transfer rate	8.2 Mbytes/s	32.8 Mbytes/s
Burst transfer rate	9.2 Mbytes/s	36.8 Mbytes/s
Storage capacity (customer)	1.3777 Gbytes	5.51 Gbytes
Heads per drive	14 data, 1 servo	14 data, 1 servo X 5
Heads active at one time	2	10
Cylinders per drive	0-1935 (0-3617_8)	0-1935 (0-3617_8)
Head groups	0-6 (0-6_8)	0-6 (0-6_8)
Sectors per logical track	0-24 (0-30_8)	0-24 (0-30_8)
Logical sector size in 64-bit words	512 CRI words	2048 CRI words
User / Factory flaw table cylinder	1928 (3610_8)	1928 (3610_8)
Vendor defect list cylinder	1929 (3611_8)	1929 (3611_8)
Maintenance (CE) cylinder	1927 (3607_8)	1927 (3607_8)
Average single track seek time	Read 1.5 ms Write 2.5 ms	Read 1.5 ms Write 2.5 ms
Average seek time	Read 9.4 ms Write 11.4 ms	Read 9.4 ms Write 11.4 ms
Full track seek time	Read 18.0 ms Write 20.0 ms	Read 18.0 ms Write 20.0 ms
Average latency	5.56 ms	5.56 ms
Rotational speed (nominal)	5400 rpm	5400 rpm
Start time (without sequence delay)	<15 s	<15 s
Stop time (maximum)	<13 s	<13 s
Single disk drive weight (including power supply)	1.8 lbs (0.8 kg)	1.8 lbs (0.8 kg) X 5
Actuator type	Balanced rotary	Balanced rotary
Data coding to/from media	Run Length Limited RLL 0,4/4	Run Length Limited RLL 0,4/4
Type of interface	Intelligent peripheral interface-2 (IPI-2) (ENHANCED)	Intelligent peripheral interface-2 (IPI-2) (ENHANCED)

IBM P17

DE-100 Disk Enclosure

The DE-100 disk enclosure houses combinations of one to four DW-300 disk drive drawers, or up to 80 disk drives. Figure 1-5 shows a fully loaded DE-100. In addition to the disk drives, the DE-100 contains a power distribution unit (PDU), cooling fans, and a warning and control system (WACS).

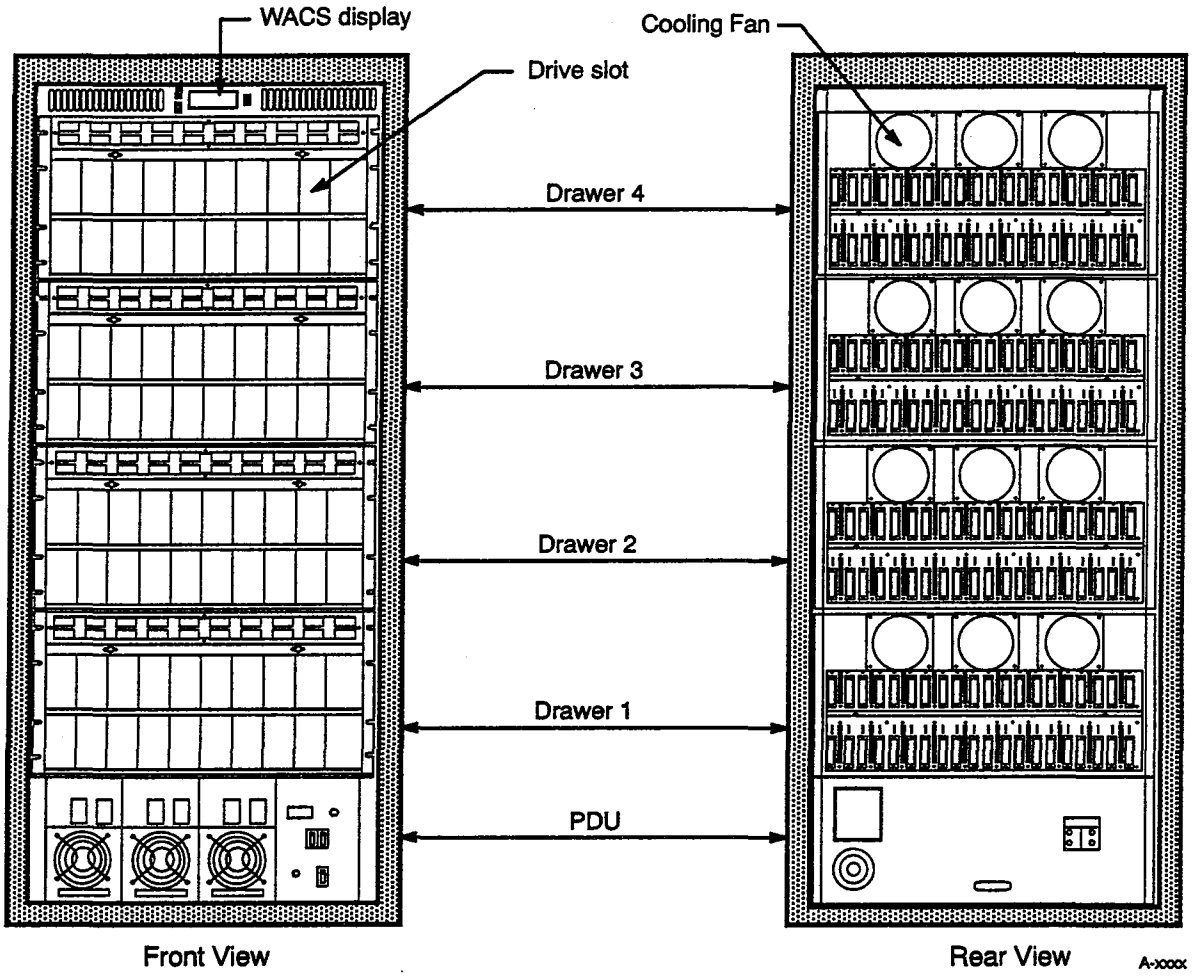


Figure 1-5. Front and Rear Views of the DE-100

The PDU converts incoming power to 36 Vdc via power supply modules. The power supplies distribute the power to ON/OFF breakers for each drive. Individual drives can be power cycled without interfering with the operation of the other devices.

The power supply modules are installed in an n+1 configuration, which provides resiliency. If a power supply module fails, the remaining module(s) will provide sufficient power to allow uninterrupted operation. Each power supply module can supply adequate power for 2 DW-300 drawers. A partially loaded DE-100 cabinet is equipped with 2 power supply modules, while a fully loaded DE-100 is equipped with 3 power supply modules.

The cooling fans draw air through louvers on the front of the cabinet and across the spindles. The air is directed to the rear of the cabinet and exhausted through vents in the top and rear of the DE-100.

The characteristics of a DE-100 vary depending on the number of DD-300 series disk drives it contains. Table 1-2 lists the physical characteristics of a fully loaded DE-100 with 80 DD-301 disk drives installed.

Table 1-2. Characteristics of a Fully Loaded DE-100

Characteristic	80 DD-301s
Height	74.75 in (190 cm)
Width	27.50 in (70 cm)
Depth	31.50 in (80 cm)
Floor space	6 ft.^{2} (.56 m^2)
Weight (maximum)	940 lbs (426 kg) (1000 lbs)
Cooling requirement	Ambient air
Heat dissipation to air (80 disk drives)	13.31 kBtu/hr (3.9 kW) maximum
Access requirements: Side Front Back	 2.00 in (5 cm) 36.00 in. (91 cm) 30.00 in. (76 cm)
Maximum data cable length (standard) (optional)	 20 meters (66 feet) 30 meters (99 feet)
Power requirement	4.00 kVA (3.9 kW) maximum
Input Power (selectable)	200-208 Vac, 50/60 Hz, 3 phase, 4-wire, delta, 20 A or 380-416 Vac, 50/60 Hz, 3 phase, 5-wire, wye, ~~16 A~~ 17 A
Power receptacle: North America and Japan International	 IEC 309, 3-phase, 208 Vac, 30-amp, Hubbell #430C9W or equivalent IEC 309, 3-phase, 400 Vac, 32-amp, Hubbell #532C6W or equivalent

DCA-2 Disk Channel Adapter

The DCA-2 provides a communication link between the auxiliary input/output processor (EIOP) in the IOS-E and the disk drives (refer to Figure 1-6). The DCA-2 transfers system data from the EIOP buffer board to the disk drive. The DCA-2 also converts control functions from the EIOP into IPI-2 protocol for the disk drives.

The primary functions of the DCA-2 include:

- Communicating with up to eight disk drives
- Passing control functions from the EIOP to the disk drives
- Receiving status from the disk drives
- Generating error-correction codes for write data
- Checking read data error-correction codes and parity

There are several restrictions to the configuration options that are possible with the DCA-2 and the disk drives. These configuration options include the following restrictions:

- Even though the DCA-2 channel adapter supports 60 series drives, all drives connected to a single DCA-2 should be of the same type. 300 series and 60 series drives should not be connected to the same channel adapter. (it will work, but not recommended)

- Even though each EIOP supports up to four channel adapters, all channel adapters connected to a single EIOP must share a common IOS kernel driver. DCA-2 and DCA-3 channel adaptors are supported by a common IOS kernel driver.

Software drivers { eiop.dca2 – works for DCA-2's (will support 32 devices)
eiop.dca3 – works for Both DCA-2's and DCA-3's (will support 24 devices)

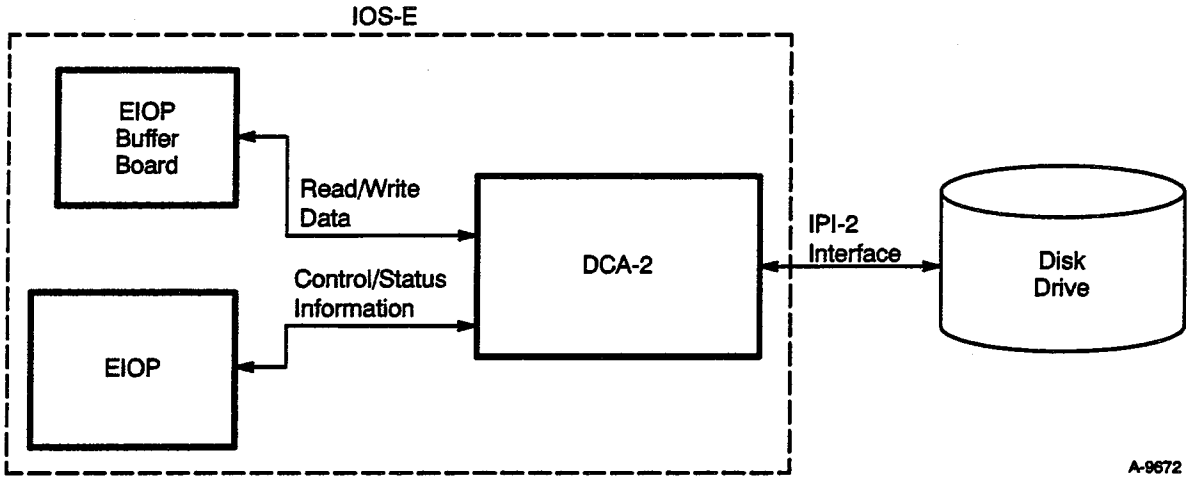


Figure 1-6. Block Diagram of DCA-2 Operations

DCA-3 Disk Channel Adapter

The DCA-3 provides a communication link between the auxiliary input/output processor (EIOP) in the IOS-E and the DA-300 disk arrays (refer to Figure 1-7). The DCA-3 transfers data between the EIOP buffer board and the disk array.

The primary functions of the DCA-3 include:

- Communicating with up to eight disk arrays
- Communicating to each array in 1-, 4-, or 5-spindle mode
- Passing control functions from the EIOP to the disk arrays
- Receiving status from the disk arrays
- Generating error-correction codes for write data
- Checking read data error-correction codes and parity
- Striping write data and parity across the 5-spindle array
- Performing parity reconstruction on read data

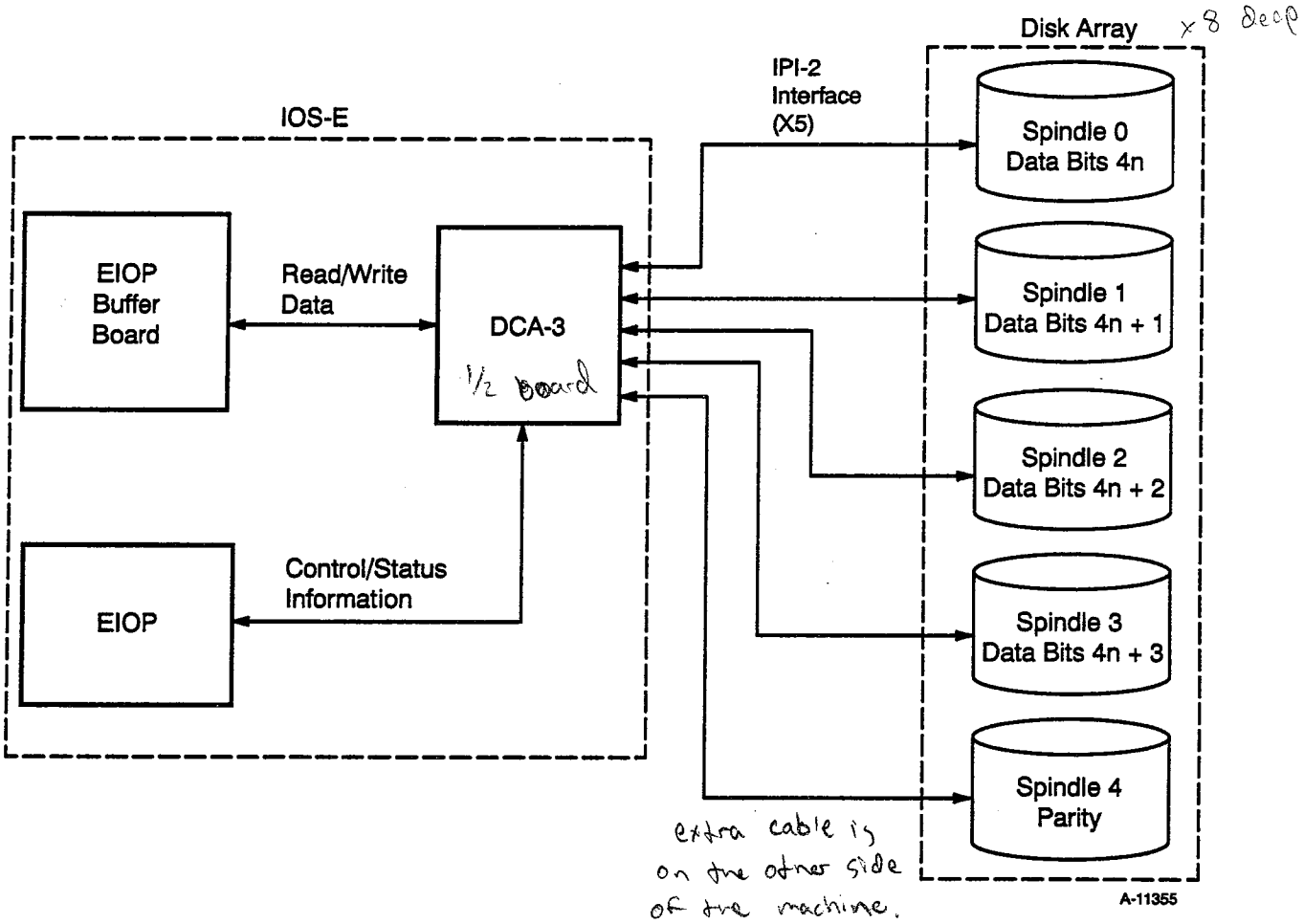


Figure 1-7. Block Diagram of DCA-3 Operations

DCA-2 and DCA-3 Comparison

A DCA-3 can connect to a DA-301 disk array. The DA-301 comprises five DD-301 spindles. In each array type, data is striped across four of the spindles while the fifth spindle is used for odd parity.

Use of the terms drive and spindle can be confusing. The type of channel adapter a device is connected to determines whether it is referred to as a drive or spindle. If a DD-301 is connected to a DCA-2 channel adapter, it is an individually accessible I/O device and is referred to as a drive. However, a DD-301 connected to a DCA-3 represents one-fifth of an array and is referred to as a spindle.

The hardware design and software support of the DCA-3 enable a disk array to sustain full performance and data integrity through a wide variety of problems, up to and including the complete failure of a spindle. Alternate path configurations can provide additional resiliency against the failure of a DCA-3. Refer to the "DCA-3 to Disk Array Cabling" section later in this manual.

The spindles used for the disk array are housed in a DE-100 cabinet. Because each cabinet can house up to 80 spindles, a single DE-100 can accommodate up to 16 complete arrays. The number of spindles per cabinet can vary depending on the number and configuration of arrays involved. Cabling configuration details for the disk array are located in the "300 Series Disk Drive Cabling" section later in this manual.

The format specification for an individual DD-301 spindle does not change if the spindle is connected to the DCA-3. However, when connected to the DCA-3, each spindle is regarded as one-fifth of the logical device. Data buffering on the DCA-3 allows hideable flaws to be handled on a per-spindle basis. Specific format information is in the "DD-301 Format and Flaw Management" sections later in this manual.

Status definitions also differ between the DCA-2 and DCA-3 channel adapters. Refer to the "300 Series Disk Systems Status" section in this manual for information specific to the DCA-3.

Disk array performance is basically four times that of the same spindle type connected to a DCA-2. Refer again to Table 1-1 for characteristics of the DD-301 drives and the DA-301 disk arrays.

Spare Disk Drives

One or more DD-301 disk drives may be cabled into a disk system and configured as a spare device on an existing DCA-2 channel. If a customer disk drive starts to fail, the data from the failing drive can be moved to a spare device using UNICOS utilities. The spare disk drive can store the data until the failing drive is repaired or replaced.

Only one spare disk drive is needed per device type, rather than per DE-100. For each IOS-E, at least one available position on a DCA-2 disk channel should be reserved to accommodate connection to a spare device.

For DA-301 disk array applications, the spare DD-301 need not be connected to the array until failure of an existing spindle warrants replacement. If DCA-2 channel adapters exist on the site, the spare drive should be maintained as a DD-301 up until the time it may be needed to replace a failing spindle in a DA-301 disk array.

2 DE-100 DISK ENCLOSURE

The DE-100 disk enclosure accommodates up to four DW-300 drawer assemblies (1-4). Drawer locations are numbered from the bottom up as shown in Figure 2–1. Each drawer can hold up to 20 drives each for a combined total of 80 drives per cabinet. Refer to the DW-300 section of this manual for detailed information on the DW-300 drawer assemblies.

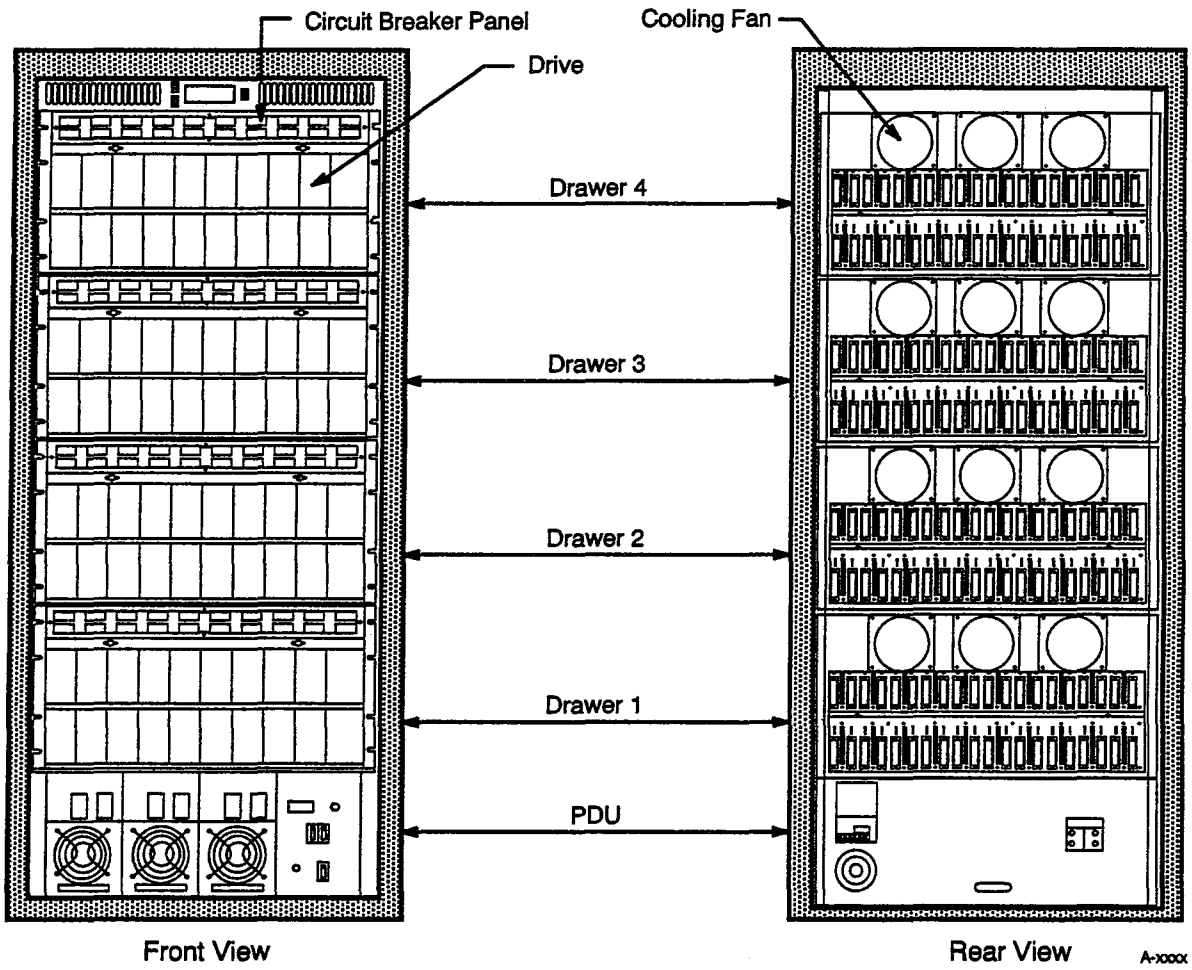


Figure 2–1. Front and Rear Views of the DE-100

DE-100 Power Distribution

Power Distribution Overview

The DE-100 cabinet is designed to operate from a customer supplied power source. The DE-100 power input box delivers power to switching-mode power supply modules which supply DC power to the drives in the DW-300 drawer assemblies. In addition, the power input box supplies AC power to the WACS assembly and the cooling fans within each DW-300 drawer as shown in Figure 2–2.

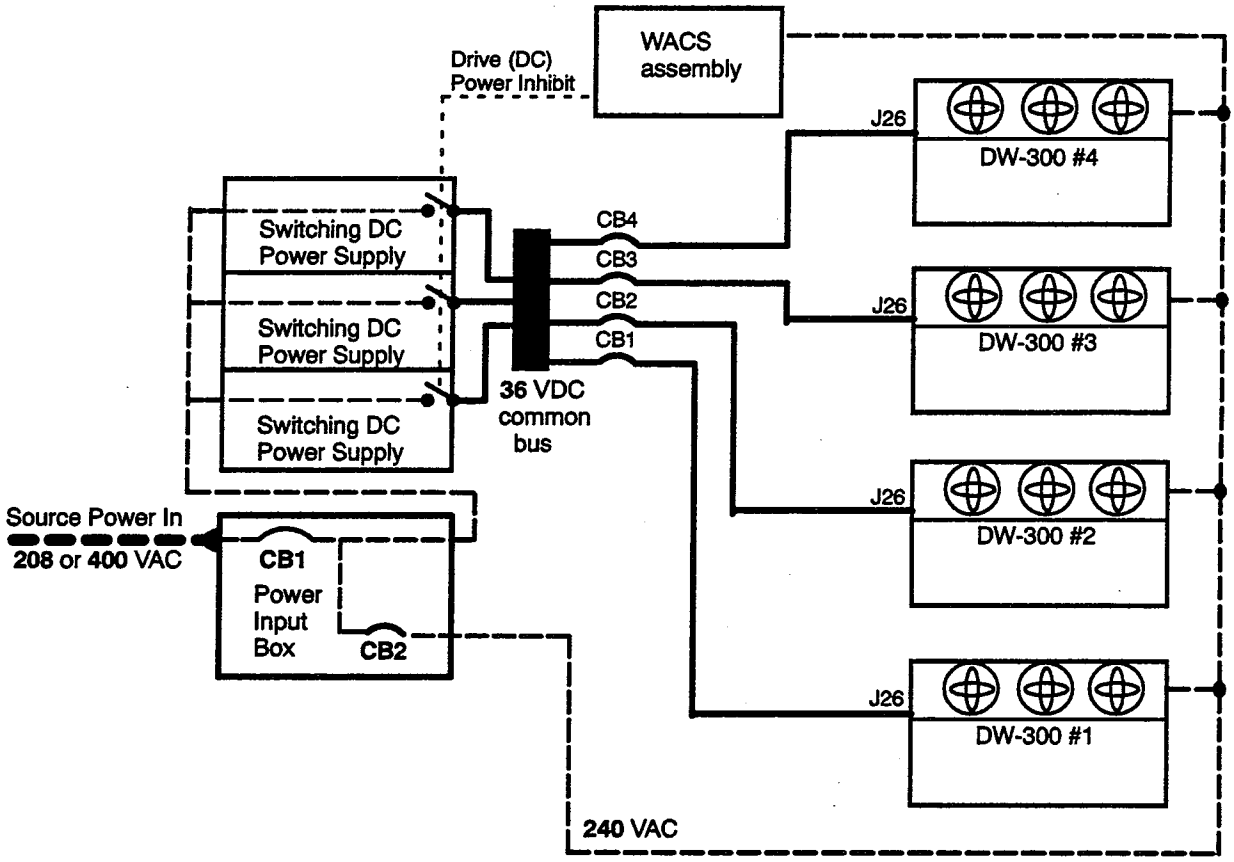


Figure 2–2. DE-100 Power Distribution Block Diagram

The acceptable source power parameters include the following:

- 200-208 Vac, 3-phase, 4-wire, delta
- 380-416 Vac, 3-phase, 5-wire, wye

Power Supply Assembly

The power supply assembly contains the power input box and up to 3 switching power supply modules. Source power enters through one of two possible connections at the rear of the power supply assembly. Source power of 400 Vac enters the power input box through the upper socket while 208 Vac source power uses the lower socket. In either case, a protective panel is positioned to cover the unused socket (refer to Figure 2–3).

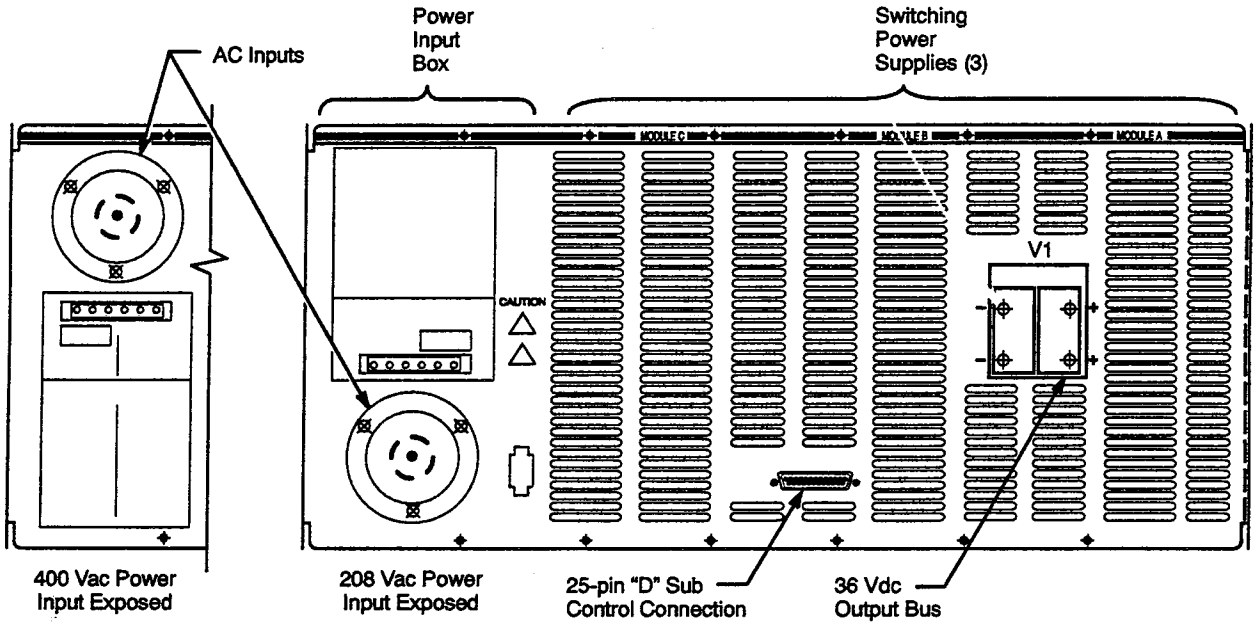


Figure 2–3. Rear View of DE-100 Power Supply Assembly

In addition to housing the major power components, the power supply assembly provides the following interconnects:

- AC power to the switching power supply modules
- Voltage control to the switching power supply modules
- AC power to the cooling fans and WACS circuitry
- Communication with the WACS circuitry
- DC power to each DW-300 drawer assembly

Power Input Box

Input power is controlled by the main circuit breaker CB1 located on the front of the power input box (refer to Figure 2–4). AC power is then delivered to a secondary circuit breaker CB2 which controls distribution to the cooling fans and WACS circuitry in the DE-100 cabinet.

A master voltage adjustment control is also located on the front of the power input box (refer again to Figure 2–4). It is necessary to center the master voltage control before making any voltage adjustments on the switching power supply modules. Refer to the :Maintenance Procedures" section of this manual for more information on maintaining the power components of the DE-100.

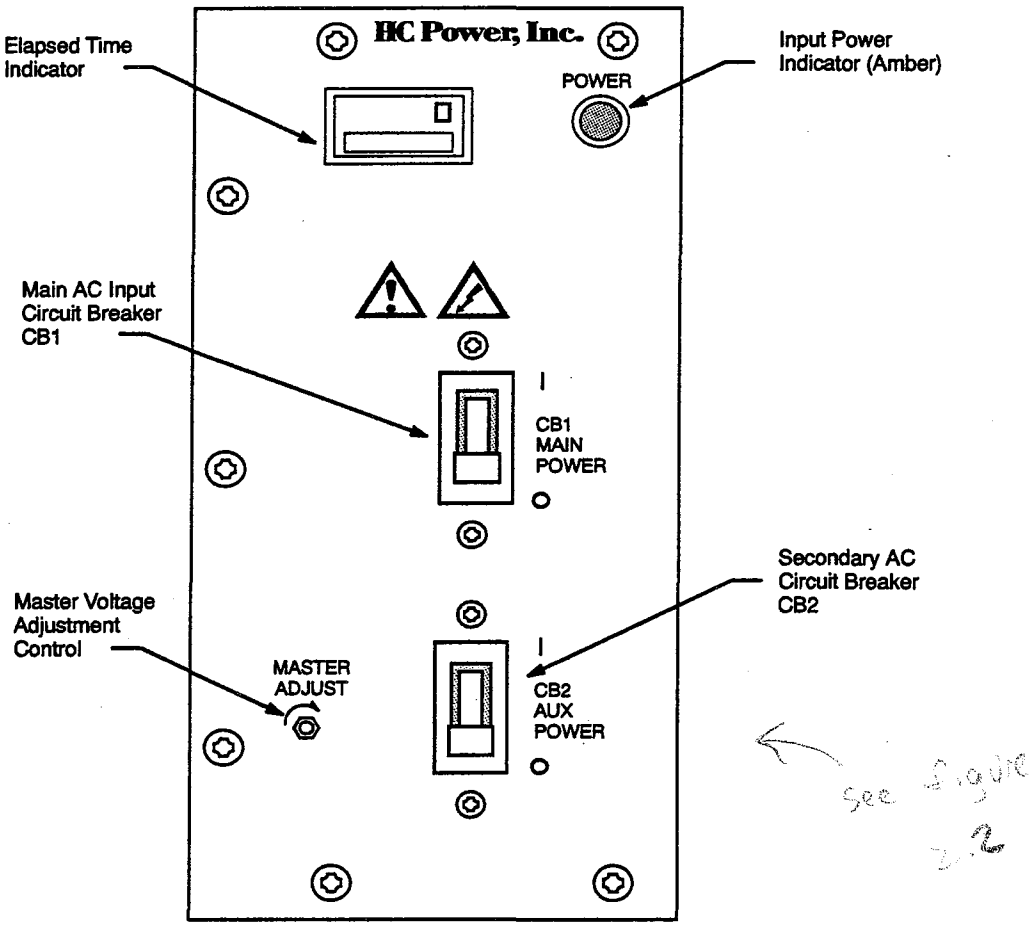


Figure 2–4. Front View of DE-100 Power Input Box

Switching Power Supplies

The DE-100 uses 2 or 3 switching-mode power supplies, which provide 36 volts DC to the disk drives within the DW-300 drawers.

The input AC power is rectified to a high voltage DC. The DC is pulsed or "switched" into a step-down transformer. The output of the transformer is rectified through diodes and filtered to produce the 36 volt DC output. Additional features include control and monitoring, soft start, and power factor correction. Refer to Figure 2–5.

The voltage adjustment located on each power supply module is used for balancing the module set for equal load distribution. The "Maintenance Procedures" section of this manual provides detailed information on maintaining the power components of the DE-100.

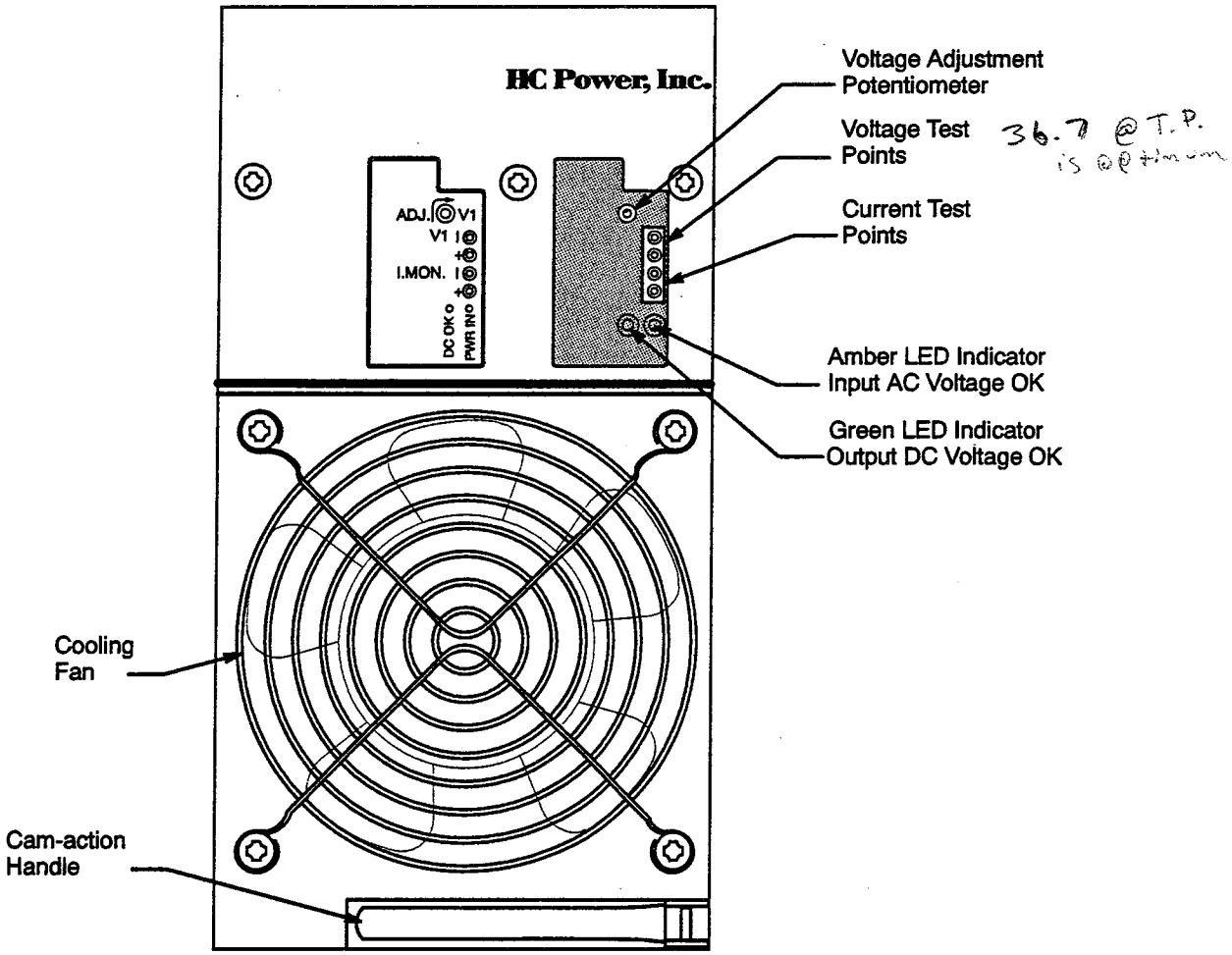


Figure 2–5. Front View of DE-100 Switching Power Supply Module

DW-300 DC Power Distribution

The following subsection provides details of the DC power distribution within a DW-300 drawer.

The 36 Vdc power required by the disk drives enters the DW-300 drawer, and is distributed, through a power distribution board. This board is located behind the drawer's circuit breaker panel (refer to Figure 2–6).

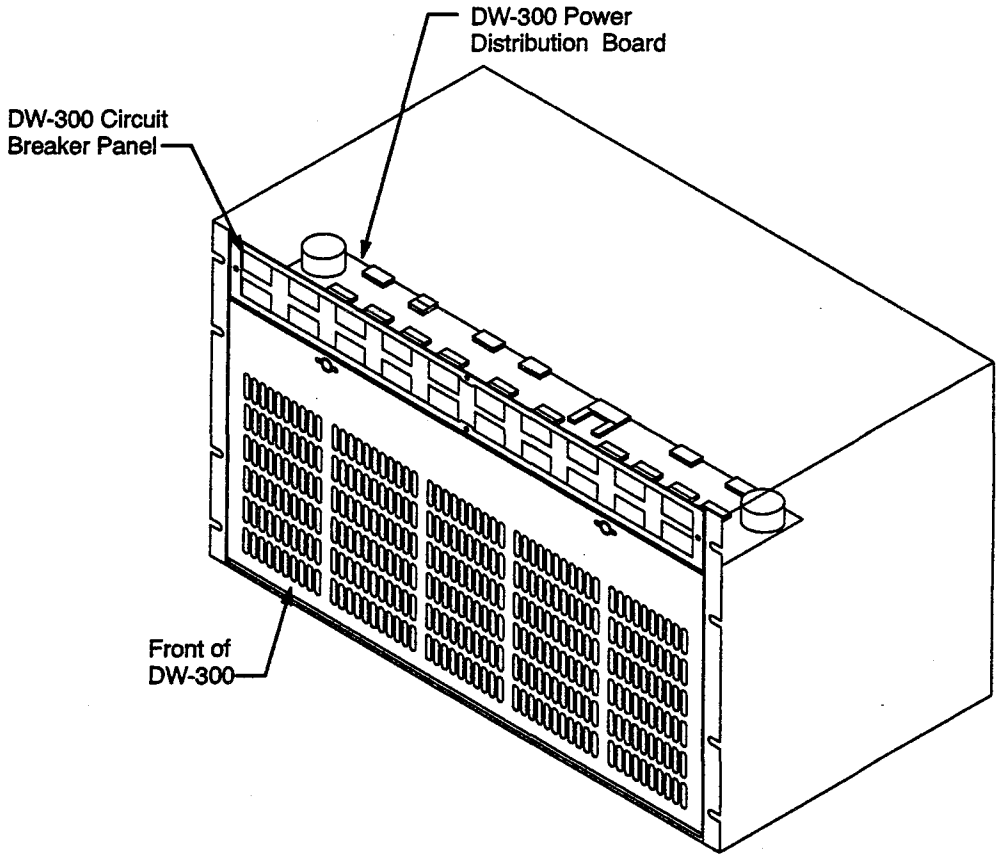


Figure 2–6. DW-300 Power Distribution Board Location

The 36 Vdc output from the power supply assembly enters the power distribution board through connector J26. The power is fanned out to each of the circuit breakers via 20 on-board connectors. After passing through the circuit breakers, the power flows from 5 output connectors (J21 to J25) on the power distribution board to the DW-300 backplane. Figure 2–8 shows the location of these connectors on the power distribution board.

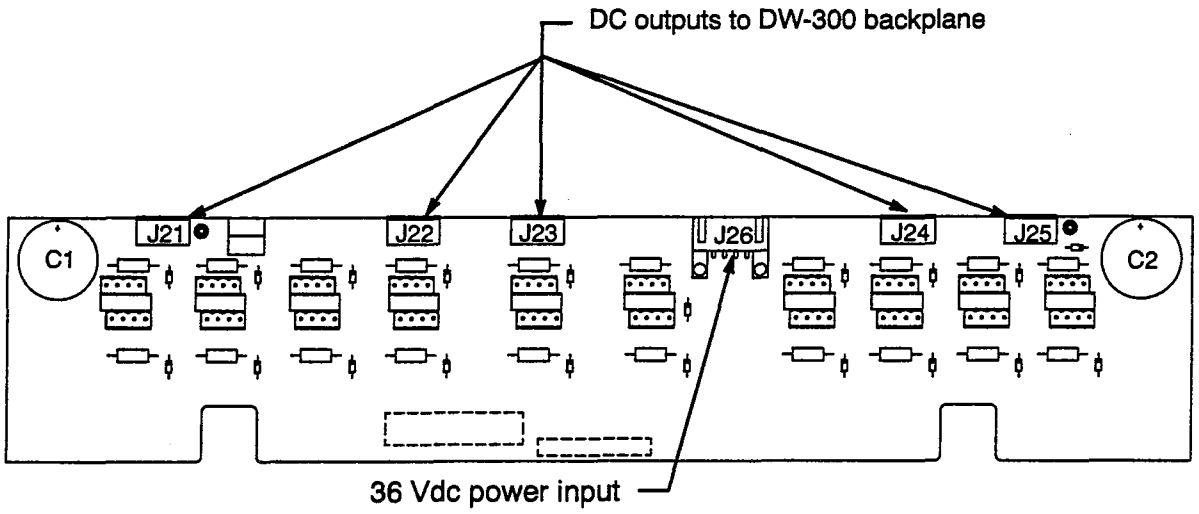


Figure 2–7. DW-300 Power Distribution Board (top view)

Each of the five cables used to deliver DC power to the backplane services a block of four circuit breakers and drive slots as shown in Figure 2–8.

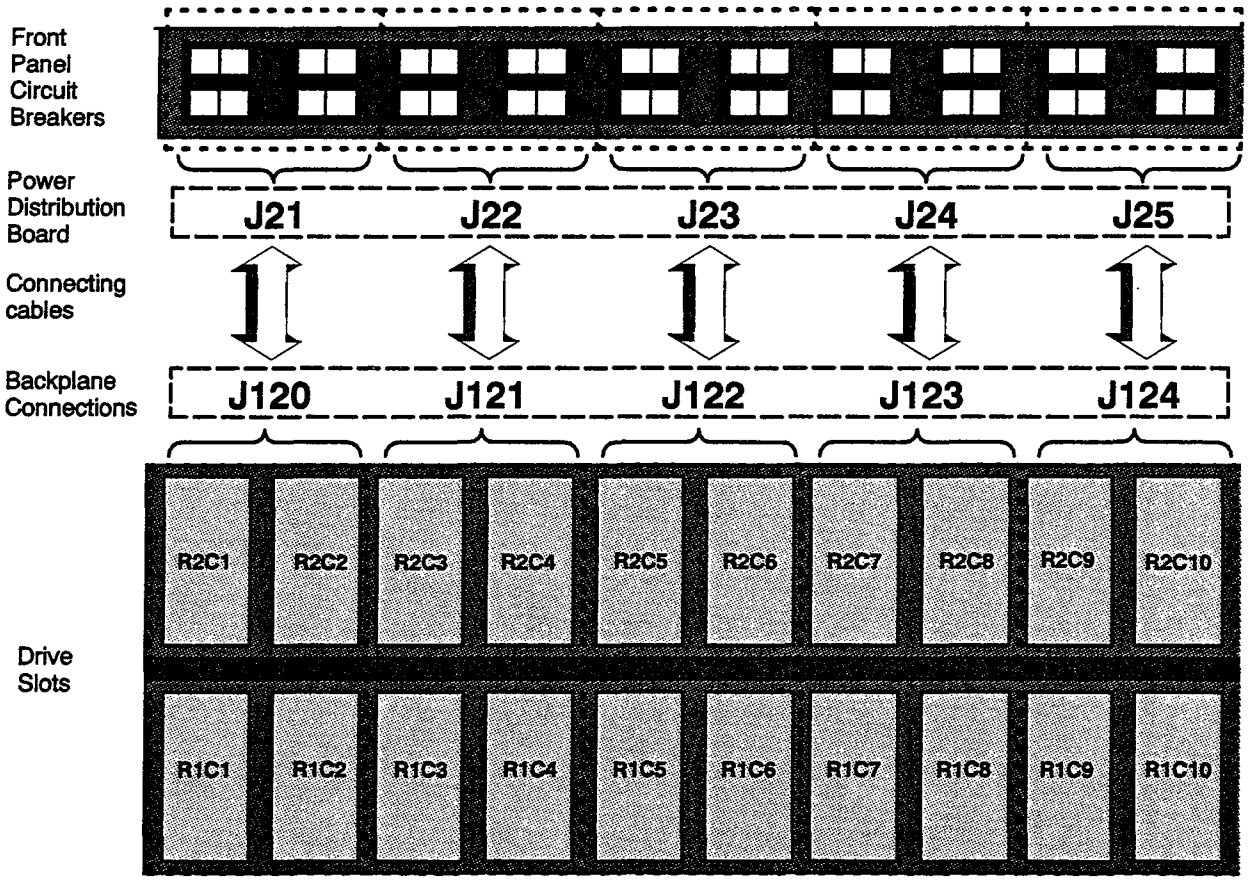


Figure 2–8. DW-300 Drive (DC) Power Distribution

DE-100 Warning and Control System (WACS)

The DE-100 warning and control system (WACS) monitors the air-discharge temperature and fan operation for each DW-300 drawer within the cabinet. The WACS also monitors the 36 Vdc common bus which supplies power to the disk drives.

Fan operation and DC bus voltage are monitored for display purposes. Only temperature faults will result in loss of power to the disk drives.The WACS assembly is housed in a tray at the top of the DE-100 cabinet (refer to Figure 2–9).

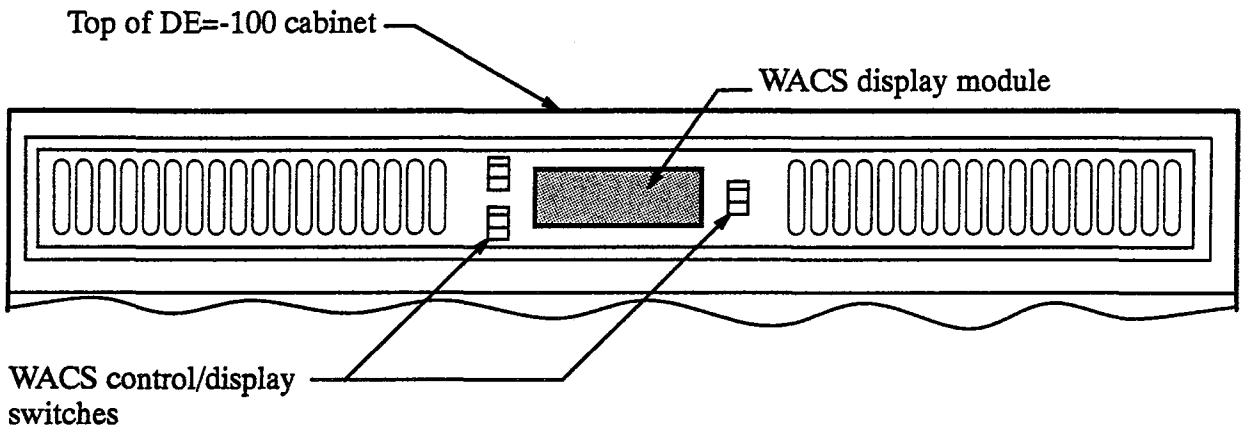


Figure 2–9. WACS assembly (front view)

WACS Theory of Operation

The WACS hardware incorporates a redundant design in all of its major components. A pair of independent microprocessors (Scanner A and B) are incorporated to allow continued operation of the WACS should either one fail. Each chip contains the following:

- A microprocessing unit (MPU)
- Integrated firmware
- Scanner logic for multiplexing sensor inputs
- A-D converters

The independent operation of these microprocessor/scanners permits either one to powerdown the disk drives if safety limits are exceeded.

Critical temperature parameters within the cabinet are monitored through a redundant pair of thermistors (primary and backup) to guard against the failure of a single thermistor. Both the primary and backup thermistor

must indicate an unsafe condition before either scanner will powerdown the disk drives. A logical overview of the WACS operation is shown in Figure 2–10.

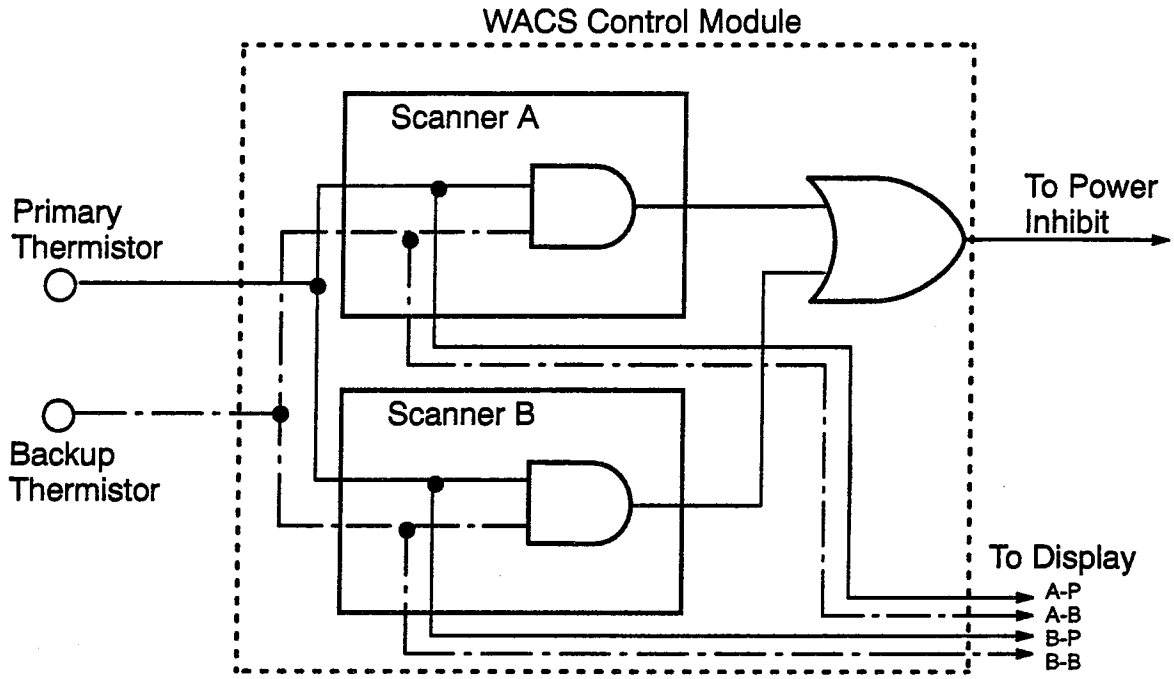


Figure 2–10. WACS Operational Overview

WACS Component Descriptions

The following subsection describes the physical and functional characteristics of the following WACS components:

- The WACS Display Module
- The WACS Control Module
- The WACS Warning Module
- Thermistors
- Cooling Fans

All three WACS modules are mounted inside a removable tray which can be accessed through the top of the DE-100 cabinet. Figure 2–11 shows the location of the three WACS modules within the tray.

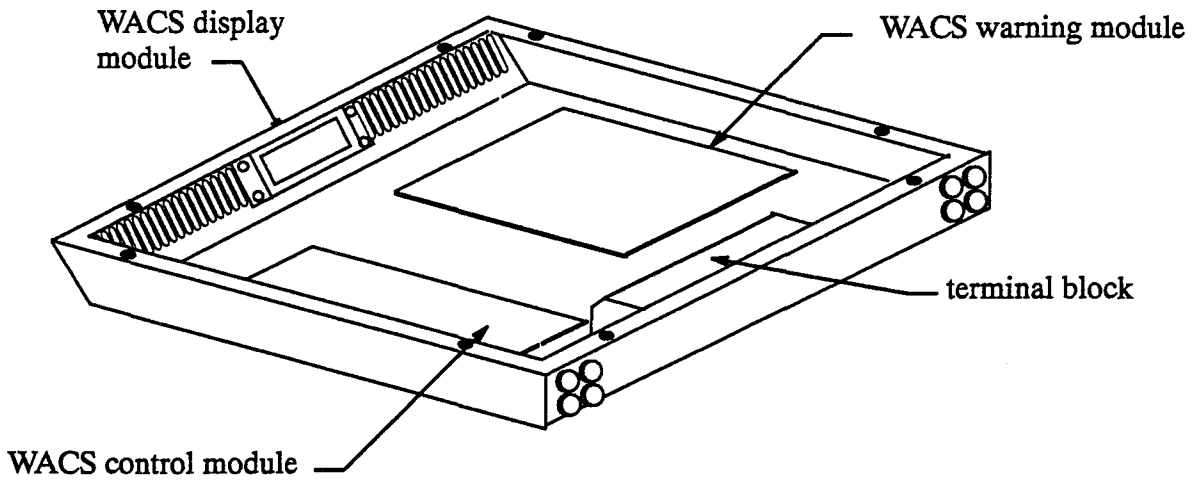


Figure 2–11. WACS module locations (top view)

WACS Display Module

The WACS display module is located at the top-front of the DE-100, and provides a local readout of monitored parameters. Figure 2–12 shows a WACS display module which is removed from it's mounting.

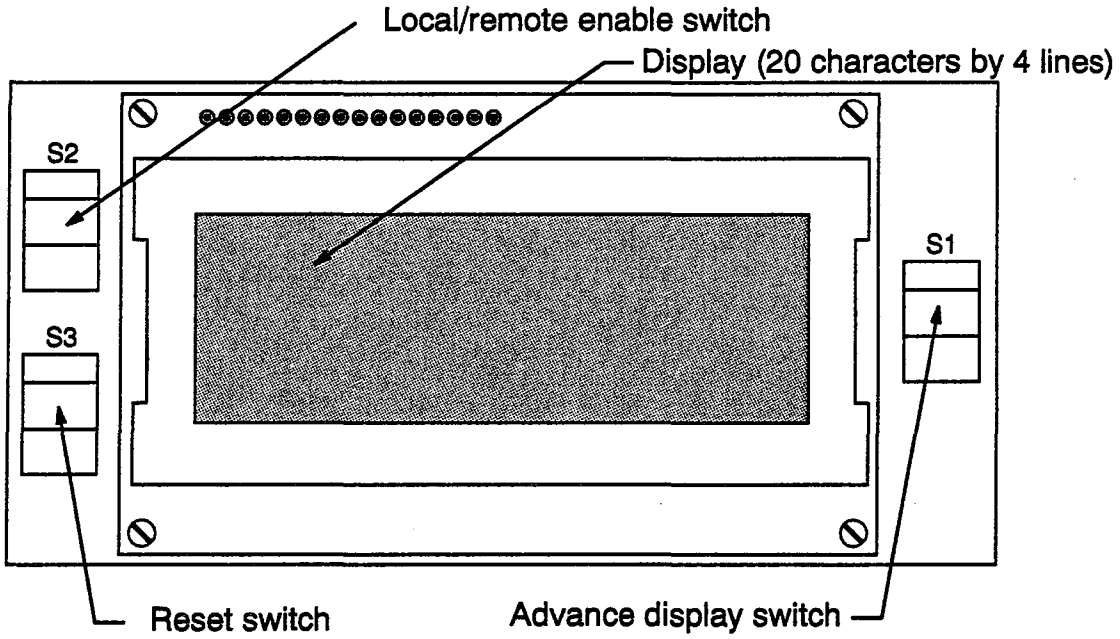


Figure 2–12. WACS Display Module

WACS Control Module

The WACS Control module is located inside the WACS tray and performs the following functions (refer to Figure 2–13 for component locations).

- Monitors and analyzes all sensor readings through a pair of redundant microprocessor/scanners (scanner A and B).
- Disables the DC output of the switching power supplies when unsafe temperature conditions are detected.
- Rectifies the 240 Vac input at TB1 to produce the DC voltages required to operate all 3 WACS modules.
- Communicates with the Warning module to acquire sensor readings and relay display information (J4)

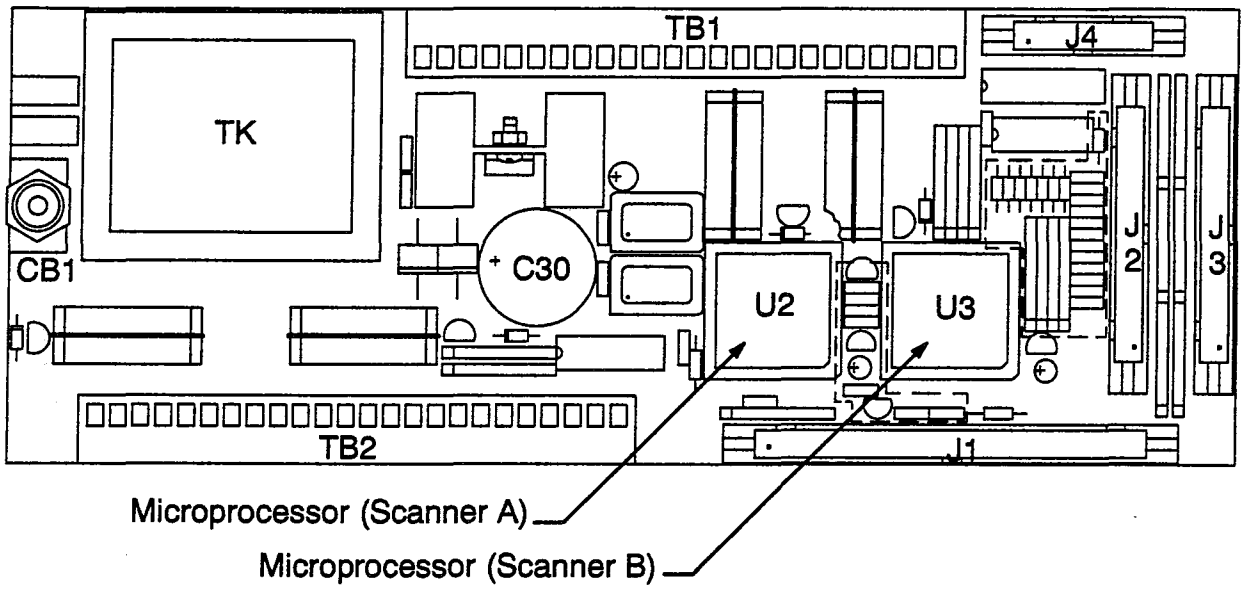


Figure 2–13. WACS Control Module

Fan operation and DC voltage information is relayed to the Control module via the Warning module, however temperature information from each drawer is fed directly into the Control module. If an unsafe temperature is detected by both thermistors (primary and backup) in a drawer, the control module will disable the DC power to all disk drives in the cabinet.

WACS Warning Module

The WACS Control module is located inside the WACS tray and performs the following functions (refer to Figure 2–14 for component locations).

- Provides an interface between the WACS control module at J6 and the local display module at J5.
- Provides an RS-232 interface, at J7 or J8, for connection to a Maintenance Work Station (MWS).
- Monitors sensor inputs for local or remote display at J1 – J4.
- Supports temperature displays in Celsius and Fahrenheit (S1-1).

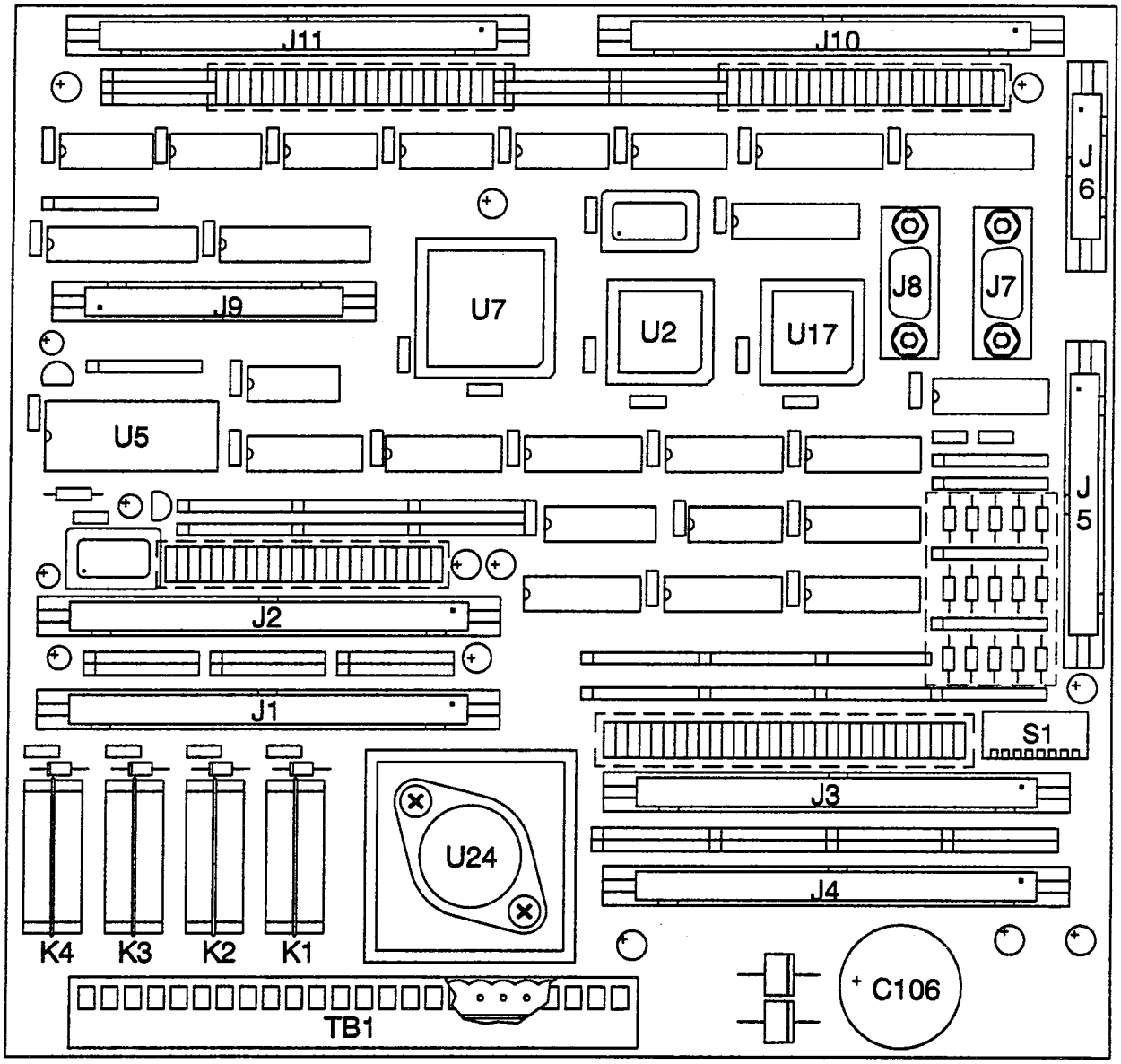


Figure 2–14. WACS Warning Module

Thermistors

Primary and backup thermistors are attached to a power distribution board inside each of the 4 possible DW-300 drawers in a DE-100 cabinet. The primary thermistor is located in the upper-left corner of the drawer, while the backup thermistor is in the upper-right corner (refer to Figure 2–15)

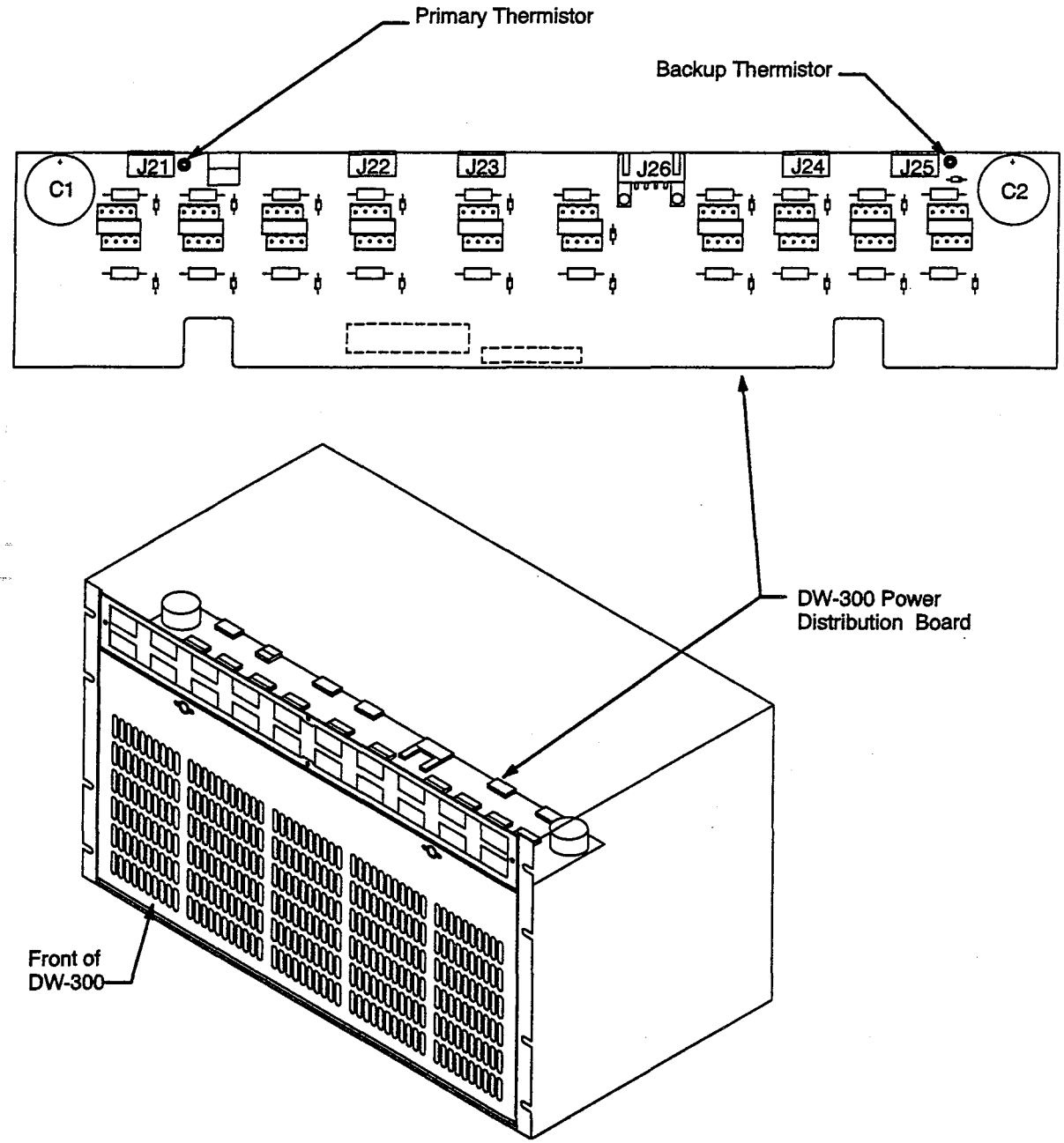


Figure 2–15. DW-300 Thermistor Locations

Cooling Fans

Three cooling fans are located at the rear of each DW-300 drawer. These "smart" fans monitor and compensate each other for failures. If one fan fails, the remaining fans will increase the air flow to provide the necessary cooling for the affected drawer. Sense wires for each fan are connected to the WACS to provide an operational status readout.

Monitored Conditions and Displays

The DE-100 WACS assembly monitors conditions in three major areas:

- DC voltage on the common output bus
- DC voltage internal to the WACS
- Air Temperature within each DW-300 drawer
- Operation of 3 cooling fans within each DW-300 drawer

DC Voltage Monitoring

Sensing wires attached to the 36 VDC common output bus allow the WACS to monitor the actual voltage present on the bus. This voltage reading can be displayed on the local display panel (refer to Figure 2–16), or on the MWS console through a remote connection.

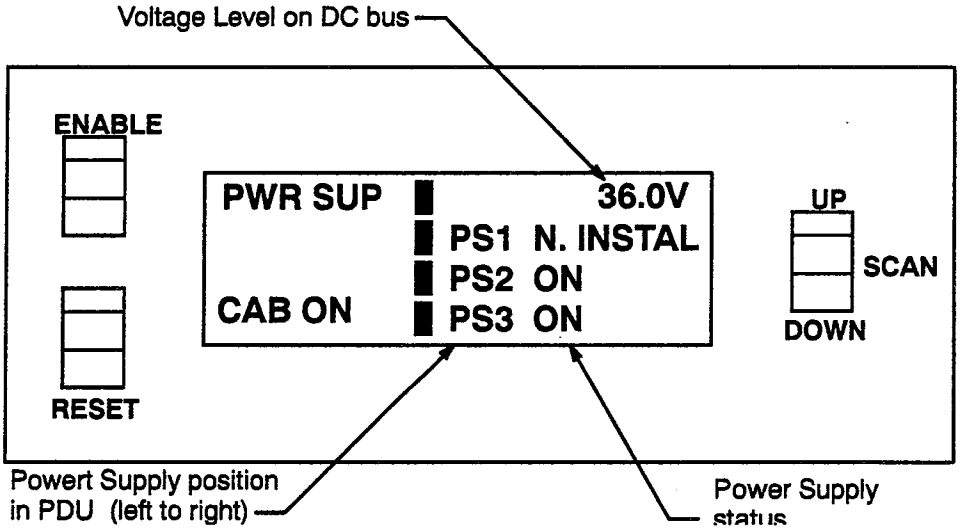


Figure 2–16. WACS Drive Voltage Display

An empty power supply slot in the PDU is indicated by a **N. INSTAL** status. A failed power supply is indicated by an **OFF** status.

The WACS also monitors its internally regulated DC power and reference voltages. Figure 2–17 shows the Scanner A display for these internal DC voltages. A similar display is available for Scanner B.

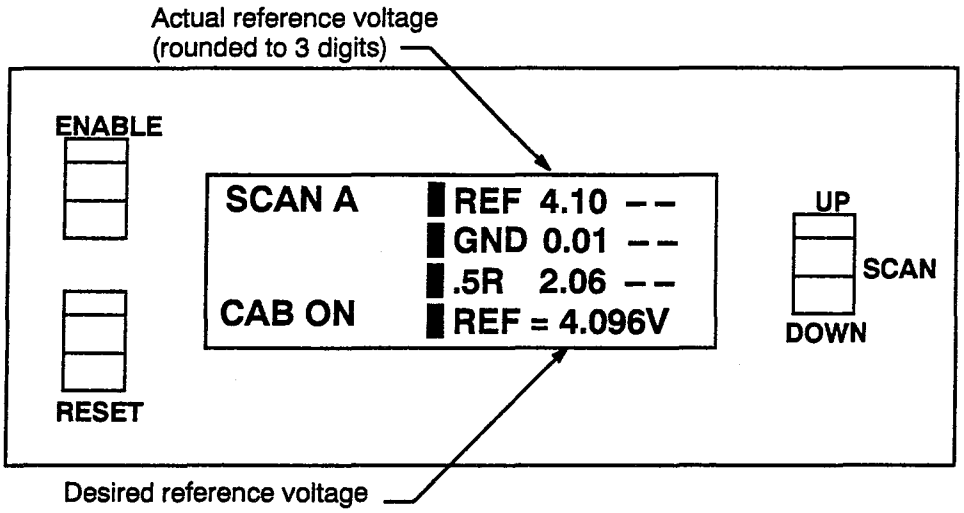


Figure 2–17. WACS Internal Voltage Display (Scanner A)

Drawer Temperature Monitoring

A pair of thermistors (primary and backup) are located in each DW-300 drawer assembly. These temperature readings can be displayed as a summary of the entire cabinet (up to 4 drawers) as shown in Figure 2–18. The summary temperatures shown are an averaged value based on the primary and backup sensor readings from both scanner A and B. Warning or Fault conditions display in the right-most column with the following:

- LW (Low Temp Warning)
- LF (Low Temp Fault)
- HW (High Temp Warning)
- HF (High Temp Fault)

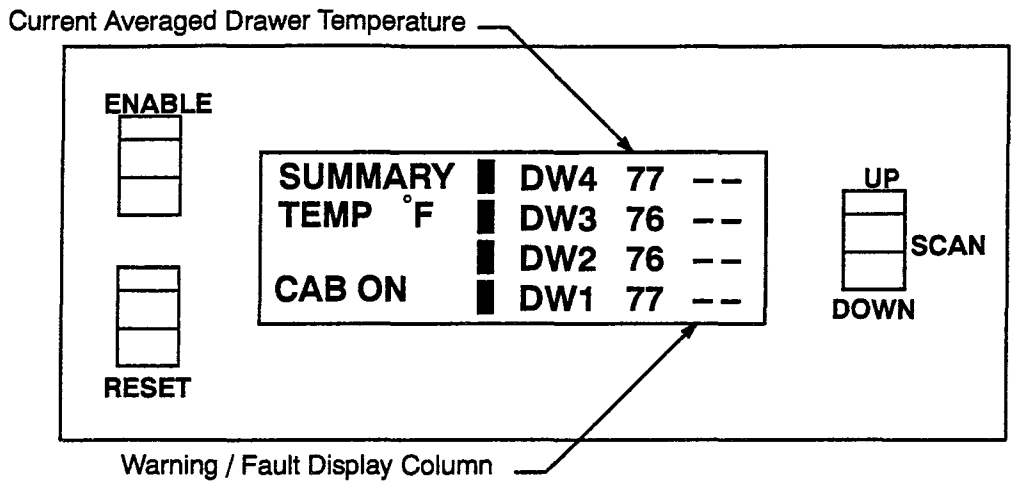


Figure 2–18. WACS Temperature Summary Display

The WACS also displays a separate temperature readout for each of the 4 possible DW-300 drawers. The temperature display for each drawer shows the primary and backup thermistor readings from both scanner A and B. Figure 2–19 shows a temperature display for drawer #1 (drawer #1 is located nearest the bottom in the DE-100 cabinet).

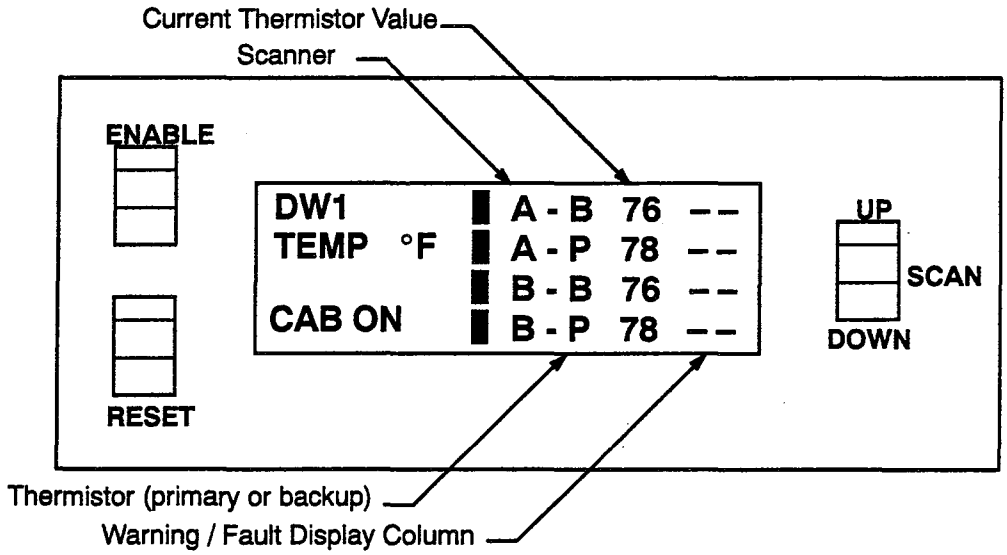


Figure 2–19. WACS DW-300 Temperature Display (1 of 4)

Cooling Fan Monitoring

Performance of the 3 cooling fans within each DW-300 are monitored by the WACS circuitry for local or remote (MWS) display. Figure 2–20 shows the WACS Fan Summary display. The "**OK**" displayed corresponds to each fans position as viewed from the front of the cabinet. The "**OK**" changes to "**BD**" to indicate the failure of a cooling fan.

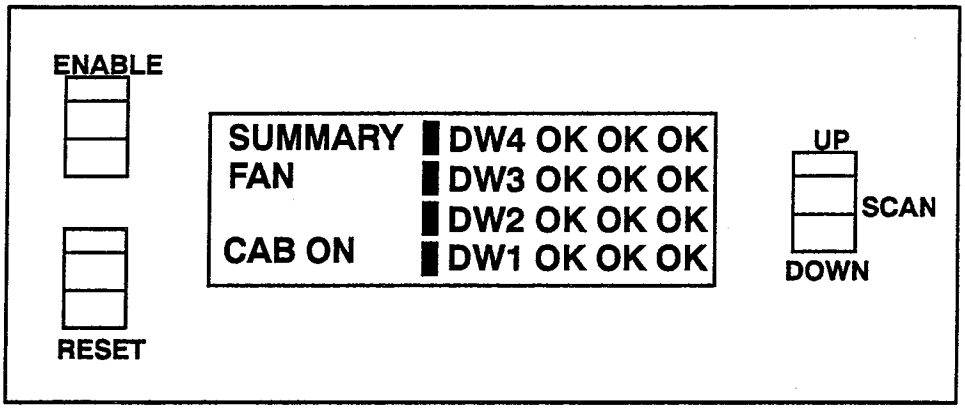


Figure 2–20. WACS Fan Summary Display

WACS Troubleshooting

A warning or fault condition can occur for one of several reasons. Any of the following can cause a warning or fault indication on the WACS display:

- An over-temperature condition within one or more DW-300 drawers
- The failure of one or more cooling fans in the DW-300 drawers
- A defective WACS Control module
- A defective WACS Warning module
- A defective sensor or sense wire path

The flowcharts shown in Figure 2–21 and Figure 2–22 can be used to determine the actual cause of a fault or warning condition.

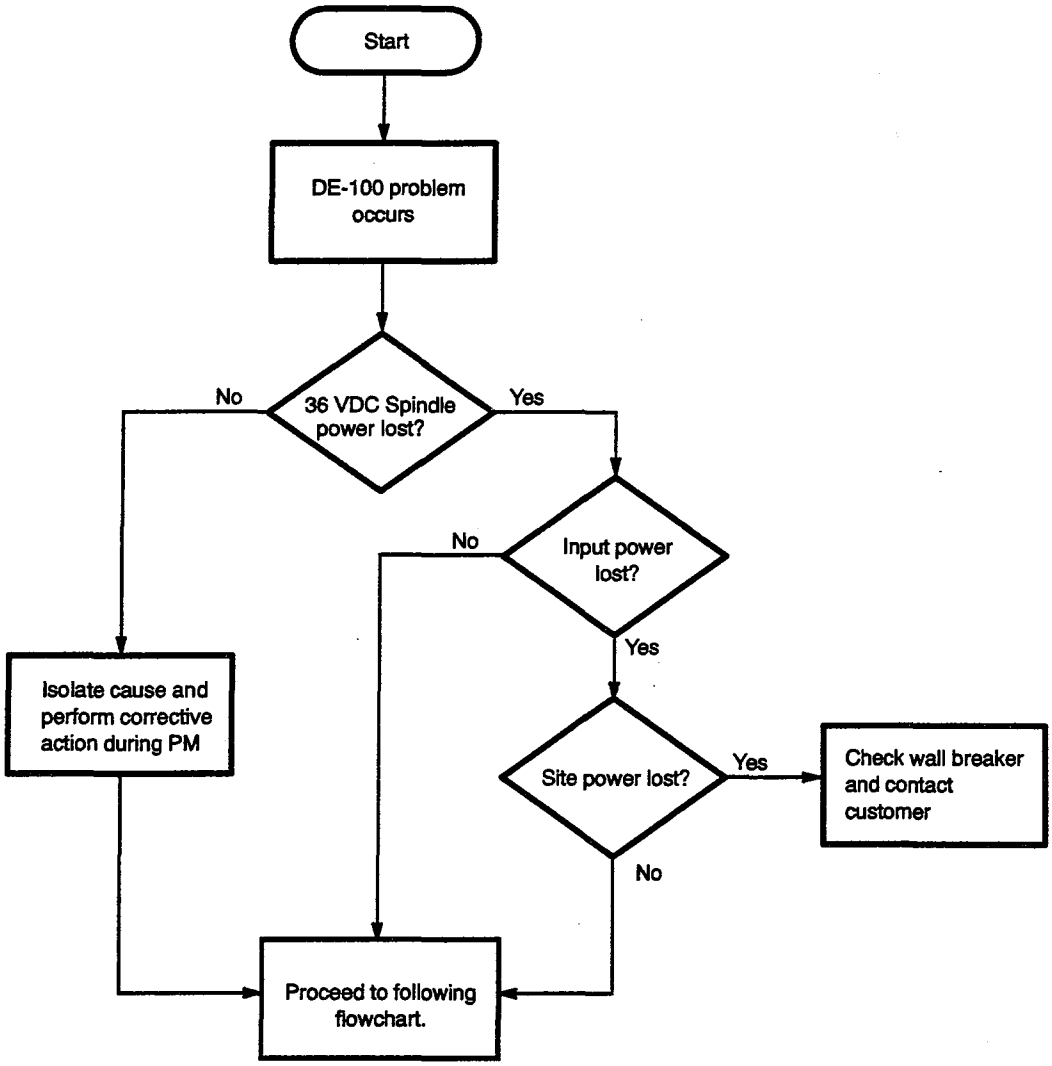


Figure 2–21. Primary Troubleshooting Flowchart

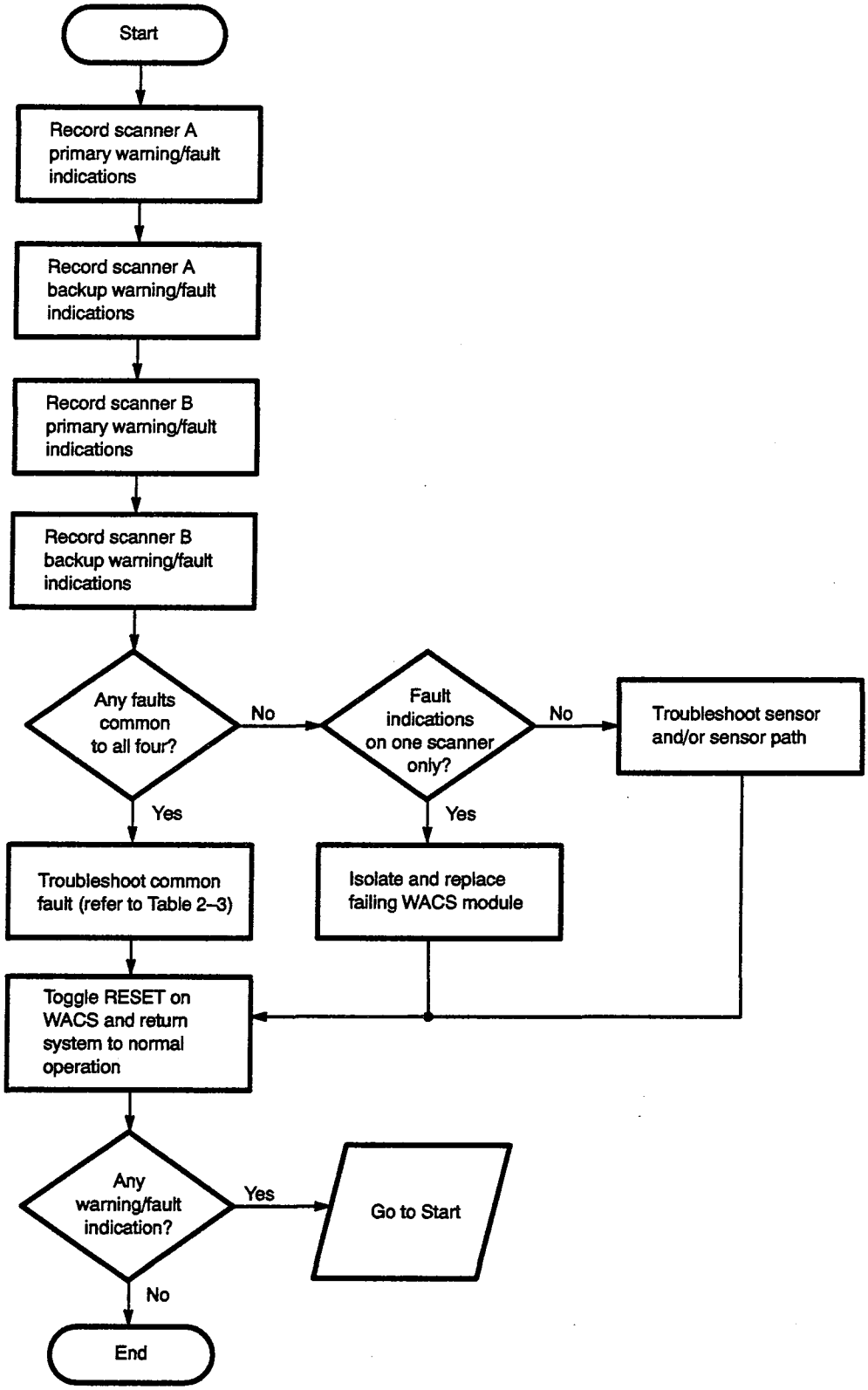


Figure 2–22. WACS Fault Isolation Flowchart

WACS Firmware and Sensor Limits

The WACS display indicates warning and fault conditions for most of the parameters being monitored. A warning usually indicates a pending failure or cause for concern, while a fault indicates an actual failure of a component or dangerous condition. Table 2–3 lists the conditions being monitored, threshold values, display indication, and probable cause for each failure type..

Table 2–3. DE-100 Troubleshooting Chart

Condition	Display Indicator	WACS Threshold	WACS action	Probable cause
High temperature Warning	**HW**	120° F (49° C)	Display only	Failure of 2 or more cooling fans in the drawer. Rise in ambient air temperature (room temp).
High temperature Fault	**HF**	130° F (54° C)	Powerdown of drives	Failure of 2 or more cooling fans in the drawer. Rise in ambient air temperature (room temp).
Low temperature Warning	**LW**	40° F (5.5° C)	Display only	Drop in ambient air temperature (room temp).
Low temperature Fault	**LF**	30° F (–1° C)	Powerdown of drives	Drop in ambient air temperature (room temp).
Loss of Cooling Fan †	**BD**	Short on sense wire	Display only	Defective fan. Loose power connection on fan.
Loss of Switching Power Supply ‡	**OFF**	Loss of "good" signal from Power Supply	Display only	Failure of a Switching Power Supply. Power Suuply failures can result from thermal shutdown, overcurrent, overvoltage, etc.

† Loss of a cooling fan results in an automatic compensation by the remaining 2 fans.
‡ Loss of a Switching Power Supply results in an automatic compensation by the remaining unit(s).

3 DW-300 DRAWER

A DW-300 drawer consists of a drawer housing, back plane, cooling fans, ON/OFF breakers and drive slot power distribution wiring. The drawer may contain up to 20 drives.

DW-300 Drawer Components

Front Panel Drive Slots and Switches

A DW-300 drawer assembly contains 20 drive slot positions for placement of disk drives. The drive slots are identified by row (R) and column (C). The lower row is referred to as row 1, while the upper row is referred to as row 2. When viewed from the front of the drawer, the lower left-hand slot is referred to as row 1, column 1 (R1,C1). The upper right-hand slot is referred to as row 2, column 10 (R2, C10). In addition, a circuit breaker is provided for each slot. Refer to Figure 3–1.

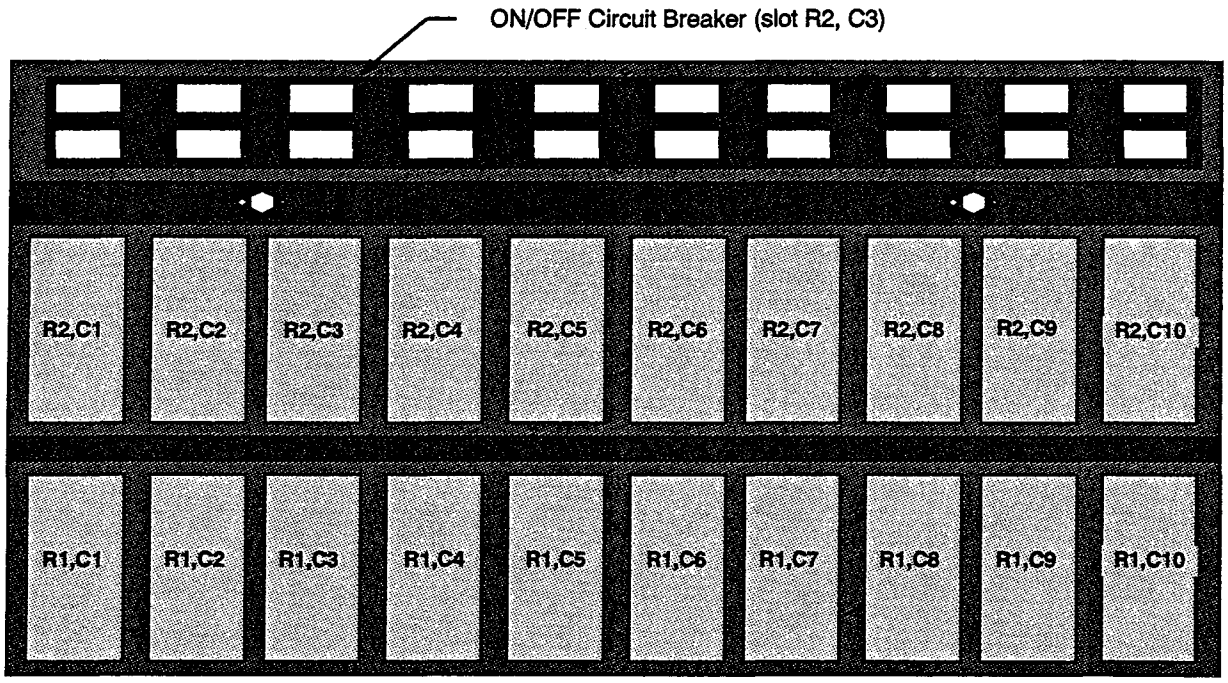


Figure 3–1. Drive Slot Column and Row Identification (front view)

When viewed from the rear of the DW-300, the column position numbers are reversed as shown in Figure 3–2.

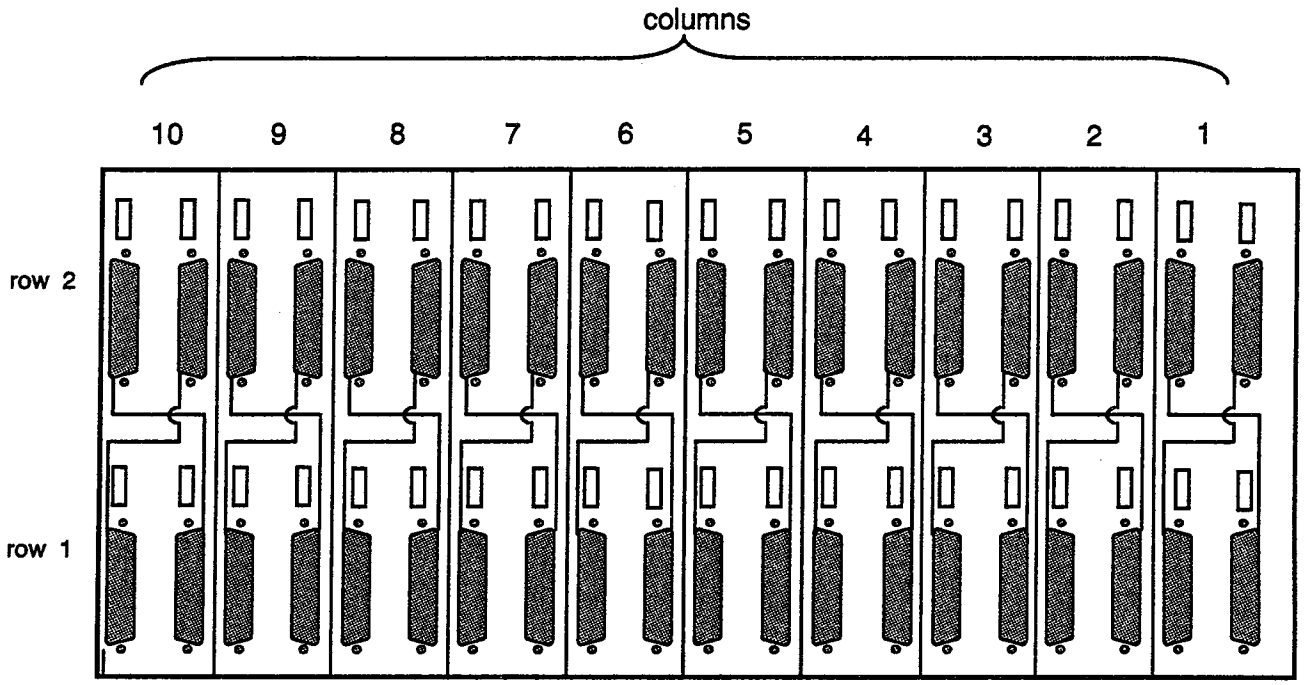


Figure 3–2. Drive Slot Column and Row Identification (rear view)

Each of the 20 drive slots within a DW-300 has the following features:

- 8 unit address selection (0-7) with parity protection
- alternate path capability for data signals
- alternate path capability for synchronization signals (for disk array applications)
- independent power connection with illuminated switch
- mechanical locking mechanism (holds the drive in position)

Details on implementation of these features are described in the following subsections.

Backplane Connections and Jumpers

The DW-300 backplane includes jumpers, synchronization cable connections, data cable connections, and a jumper which disables idle functions in the drive. Refer to Figure 3–3 for the location of these features.

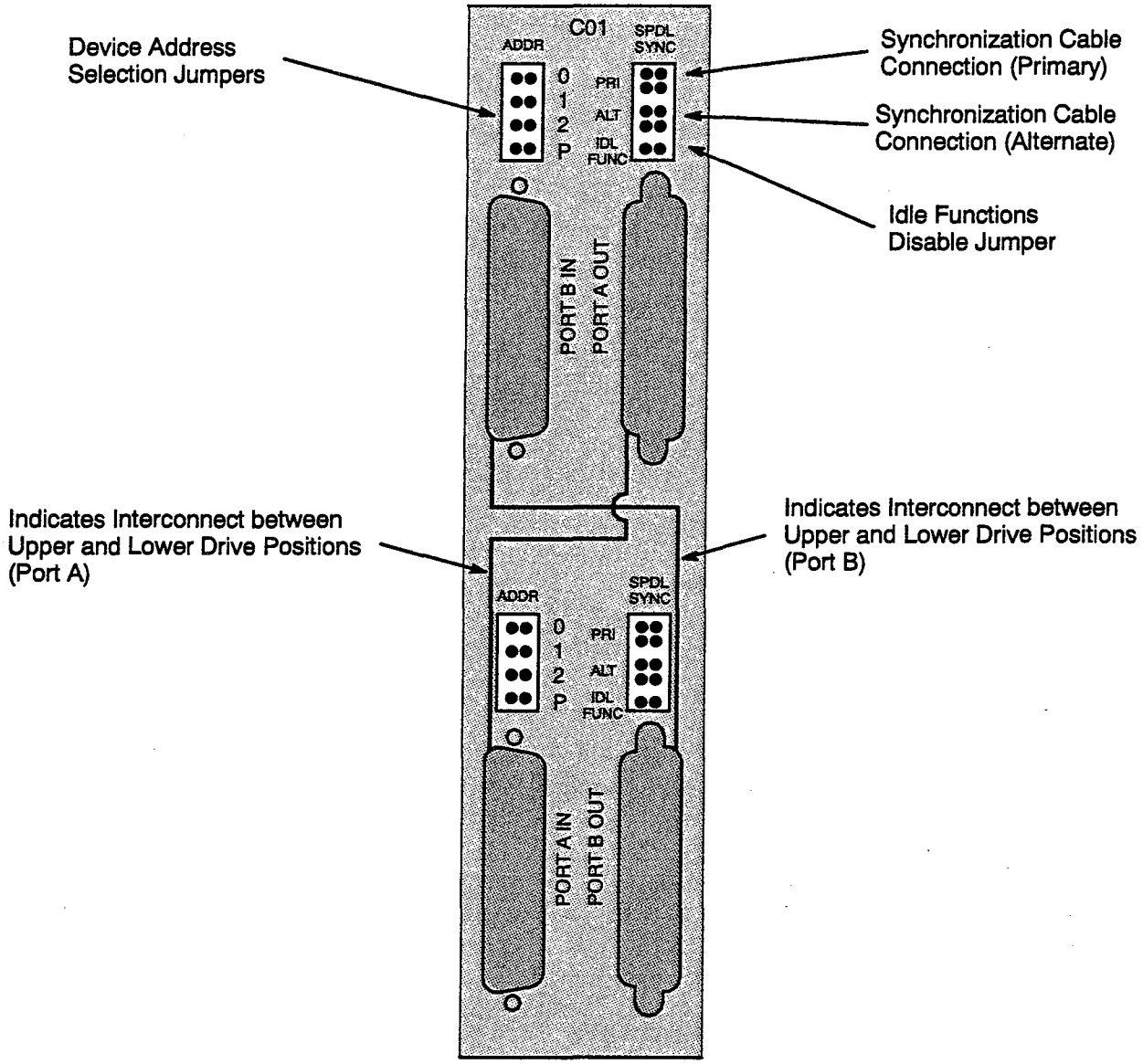


Figure 3–3. DW-300 Backplane - Column 1 Detail

NOTE: Locations of the Port A and Port B connections are reversed on all even numbered columns.

Device Address Selection

Four jumper pairs located above each drive slot determine the device address. A three-bit address select supports a valid address range of 0 through 7. An additional jumper is used to provide odd parity on the selected address. Figure 3–3 shows the position of the address selection jumpers while Table 3–1 shows the jumper placement for each possible address setting.

Table 3–1. DW-300 Jumper Settings for Device Address Selection

Device Address	Bit 0 Jumper	Bit 1 Jumper	Bit 2 Jumper	Parity (P) Jumper
0	open	open	open	jumpered
1	jumpered	open	open	open
2	open	jumpered	open	open
3	jumpered	jumpered	open	jumpered
4	open	open	jumpered	open
5	jumpered	open	jumpered	jumpered
6	open	jumpered	jumpered	jumpered
7	jumpered	jumpered	jumpered	open

CAUTION

Ensure that device address jumper placement reflects proper parity. Improper parity setting will result in a power up failure of the affected device.

Data Path Interconnects

Cable connections from the IOS-E are made using D-sub connectors located on the rear of the DW-300 drawer. These D-sub connectors are electrically connected through the DW-300 backplane to the drive carrier connectors within each slot. Connection to a drive is made when the drive is inserted and locked into position.

Within each column, the upper and lower drive data paths are physically interconnected via foils in the back plane. These interconnects provide a dual-port daisy chain connection between the upper and lower drive slots without the need for additional cables. Refer again to Figure 3–3.

The Port A connection for the lower drive in each column is daisy chained to Port A of the upper drive. The Port A output connection provides for daisy chaining to another column, or the installation of a terminator. The Port B connections are daisy chained between upper and lower drive positions in the same manner, with additional daisy chaining or termination provided at the Port B output connection. The location of the Port A and B connections are reversed between adjacent columns to, again, ease in cabling daisy chain configurations of 3 or more devices.

Synchronization (Sync) Cable Connections

When drives are configured as a DA-301 disk array, it is necessary to interconnect the five spindles within an array with synchronization cables. Each drive slot within the DW-300 provides a primary and alternate connection for the attachment of these synchronization cables.

An array spindle designated as the sync master transmits pulses on the sync connection, while a spindle designated as a slave receives pulses on this connection. Use of an alternate sync connection contributes to the overall resiliency of the disk array subsystem. Recovery software will automatically activate the alternate sync connections on an array if the primary connections are broken.

The DW-300 backplane provides 4 pins each for both the primary and alternate sync connections. Typical use of these connections is shown in Figure 3–4. For more information on cabling DA-301 disk arrays, refer to the "Cabling and Configuration" section in this manual.

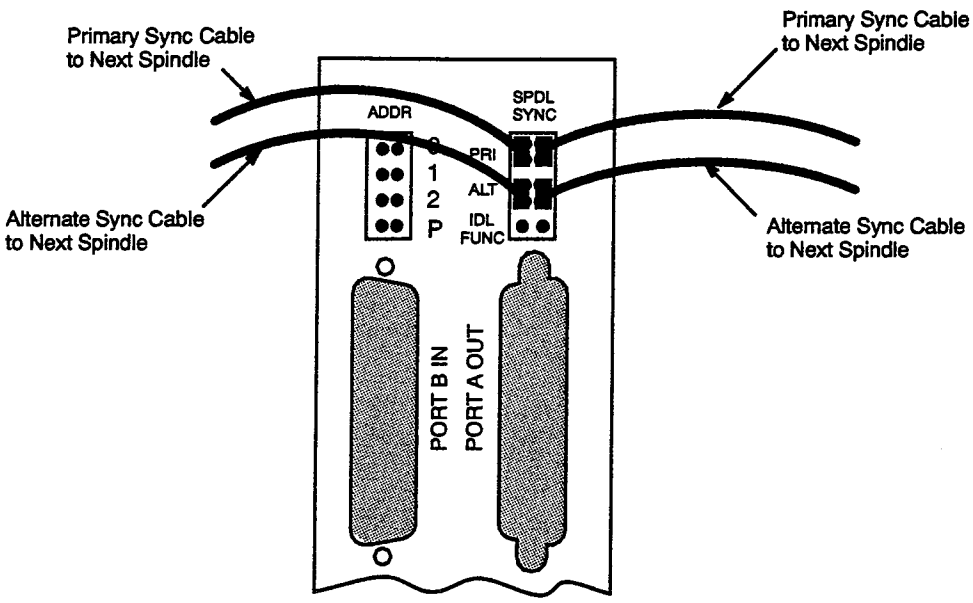


Figure 3–4. Synchronization (Sync) Cable connections for Disk Array Applications

CAUTION

Use of both Primary and Alternate Sync cable connections is mandatory in DA-301 Disk Array applications. Failure to do so can result in unnecessary system errors and/or interrupts.

Disable Idle Functions

The DD-301 disks incorporate several idle time functions which can enhance reliability. These functions include:

- Thermal Offset Compensation
- Disk Sweep
- Bias Current Shutoff

Although a jumper connection (which disables these functions) is provided for each drive slot, this connection must be left open (enabled). Refer to Figure 3–3 for the location of this jumper connection.

CAUTION

Ensure the IDL FUNC jumper connection is in an open (enabled) condition. Failure to do so results in loss of reliability and warranty violation.

Cooling Fans

Each DW-300 is cooled by three fans located at the rear of the drawer assembly (refer to Figure 3–5). These fans pull room air in through the front of the DW-300 and exhaust the heated air out the rear of the drawer. The fans have failure detection capability which signals the WACS subsystem. For more information on the WACS subsystem, refer to the previous section of the manual.

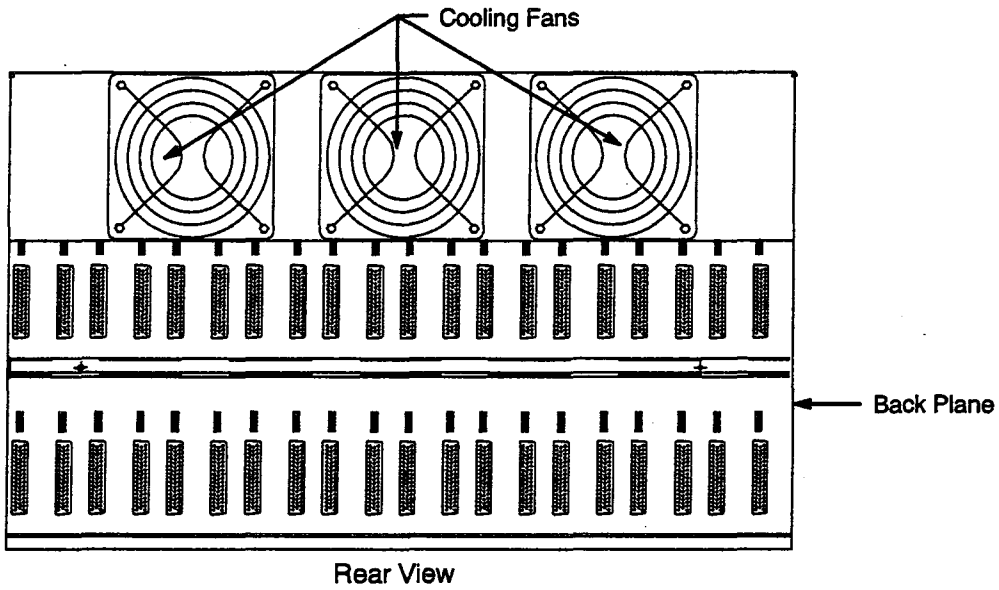


Figure 3–5. Rear View of DW-300

Because a DW-300 can be cooled effectively by two fans, the design incorporates a n+1 configuration. If a fan fails in the DW-300, the remaining two fans will increase in speed to compensate, thus providing the required cooling for the drawer. The drawer will operate normally until the failing fan can be removed and replaced. The n+1 configuration increases system resiliency and reliability.

4 300 SERIES DISK DRIVE CABLING

This section describes the cabling between the DCA-2 and DCA-3 channel adapters in an I/O subsystem model E (IOS-E), and 300 series disk drives. A description of the hardware used to connect the components, and examples of several cabling configurations are included.

General information

The following subsection contains general information concerning the configuring and cabling of 300 series disk devices. Specific information about cabling DD-301 and DA-301 devices is covered in subsequent subsections.

Terminology

Because configuration options are numerous and complex, the terminology used to define the components must be accurate and consistent. The following list provides preferred terms and their definitions.

Channel Number

Channel number refers to the logical address assigned to an I/O channel as determined by the channel adapter's location in the mainframe chassis. The possible channel pairs for a DCA-2 quarter board include 30/31, 32/33, 34/35 and 36/37(octal). The possible channel pairs for a DCA-3 half board are 34/35 and 36/37(octal).

Device Type

Device type refers to the type of peripheral device. A DCA-2 device is referred to as a DD-301. A DCA-3 device is referred to as a DA-301 disk array.

Unit Number

Unit number refers to the logical address setting of a peripheral device. Unit numbers are set using jumpers located on the back of the DW-300 drawer assembly. Unit numbers range from 0 to 7, and represent the maximum number of devices that can be daisy chained on a single channel. If the device type is a disk array, each spindle within the array is set to the same unit number.

Daisy Chain vs. Alternate Path

Daisy Chain refers to 2 or more devices connected to a single channel. In simple daisy chaining, only one port (Port A or B) on the device is used. All devices on a daisy chain share a common channel and must be set to unique unit numbers.

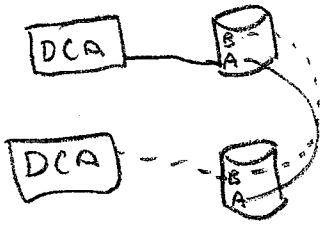
Alternate Path refers to a dual-ported daisy chain where 2 or more devices are connected to 2 separate channels. One channel connects to Port A while the second channel connects to Port B. Each of the 2 channels is configured as either the primary or the alternate path to the device(s).

When 2 daisy chains are interconnected in an alternate path configuration, the result is a single, dual-ported daisy chain. For example, if a daisy chain of 2 devices is configured as an alternate path to another daisy chain of 2 devices, the result is a single, dual-ported daisy chain of 4 devices. In this case, all 4 devices must have unique unit numbers.

Drive vs. Spindle

Drive refers to a logical peripheral device. A drive for a DCA-2 is defined as a single spindle. A drive for a DCA-3 is defined as an array of 5 spindles that share a common unit address and are accessed as a single I/O device.

Spindle refers to a single disk component within an array or drive. A spindle usually consists of a head disk assembly (HDA), logic circuit boards, and the necessary containment hardware.



Use of the terms drive and spindle can be confusing. Whether a device is referred to as a drive or a spindle is largely determined by the type of channel adapter to which the device is connected. If a DD-301 is connected to a DCA-2 channel adapter, it is an individually accessible I/O device and should be referred to as a drive. However, a DD-301 connected to a DCA-3 represents one-fifth of an array and should be referred to as a spindle.

Alternate Path = Dual-Ported daisy chain

Key Considerations

The following information addresses several key points which must be considered when configuring and cabling 300 series disk systems:

CAUTION

Configuration and cabling options for the 300 series disk drives are numerous and complicated. This manual attempts to describe all of the principles and guidelines which determine these options. Thorough understanding of these principles is essential for determining the best options, and maintaining these devices. To document examples of all possible options is beyond the scope of this or any other manual.

- Mixing DCA-2 and DCA-3 Channel Adapters – DCA-2 and DCA-3 channel adapters may be installed within a single EIOP. Each EIOP accommodates up to 4, quarter-board channel adapters. Since the DCA-3 is a half-board adapter, a single EIOP can accommodate 4 DCA-2s, 2 DCA-3s, or 2 DCA-2s and 1 DCA-3.

- Mixing 60 Series and 300 Series Device Types – Due to cable length restrictions, 60 series and 300 series disk devices **cannot** be mixed on a daisy chain. Both device types can exist on an I/O subsystem provided they are assigned to separate channel adapters.

- Cabling Between DE-100 Cabinets – Cables **cannot** be run between DE-100 cabinets. Due to cable length restrictions, all cabling of 300 series devices must be confined to within a DE-100 cabinet. Cables can be run between DW-300 drawers if necessary.

- Use of Alternate Path Configurations – Alternate path cabling must be used whenever possible to increase the overall resiliency of the I/O subsystem. The design of the DW-300 drawer allows for easy implementation of alternate path connections.

- Setting Device Addresses – Device addresses are set using jumpers on the rear of the DW-300 drawer. Odd parity protects the integrity of the address setting through the use of a parity jumper. A device will fail spinup if incorrect parity is detected on the address.

Upper (row 2) and lower (row 1) devices within a column constitute an implied daisy chain due to the design of the DW-300 drawer. Devices within the same column must have unique address settings to avoid address duplication on a daisy chain.

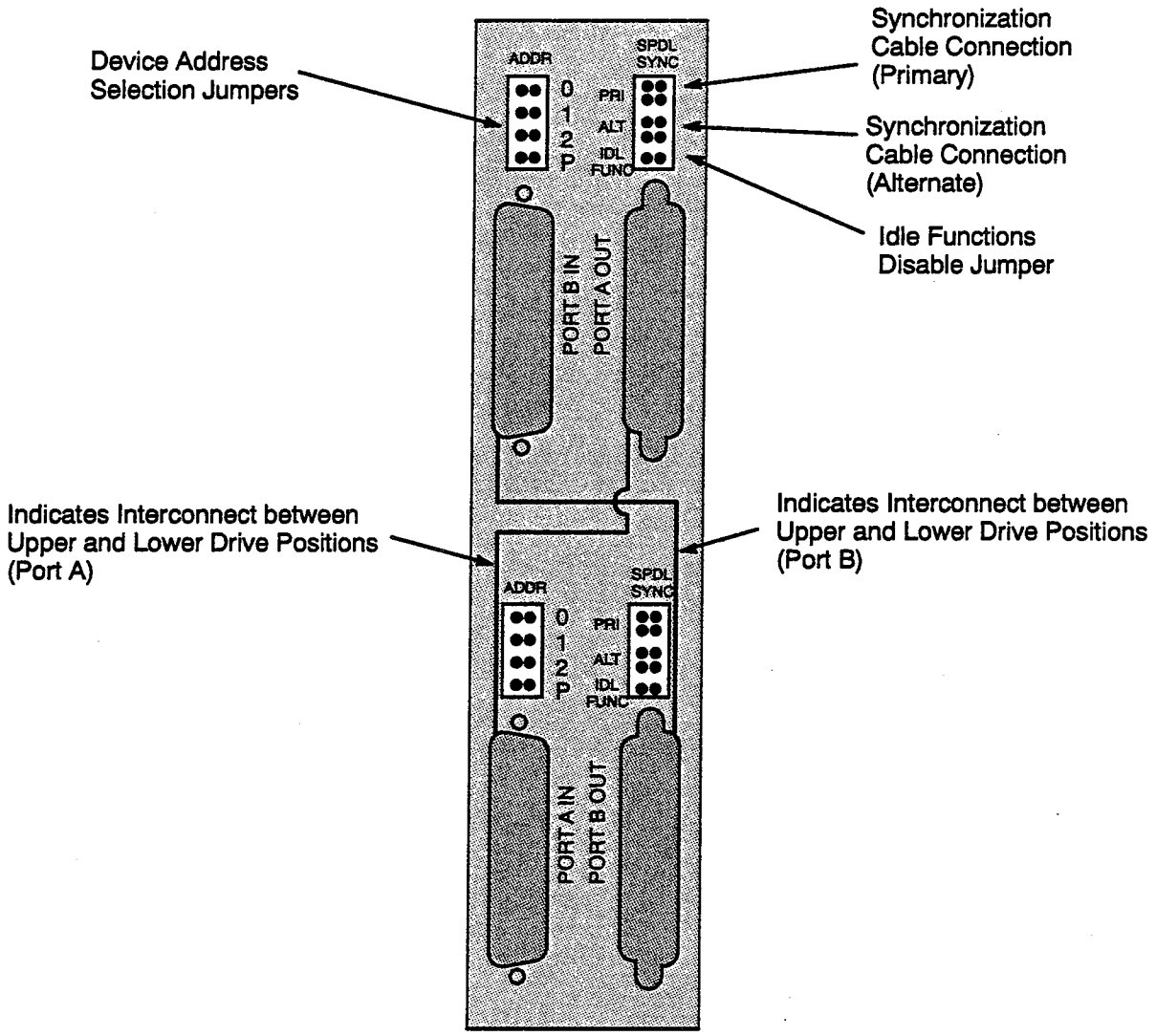
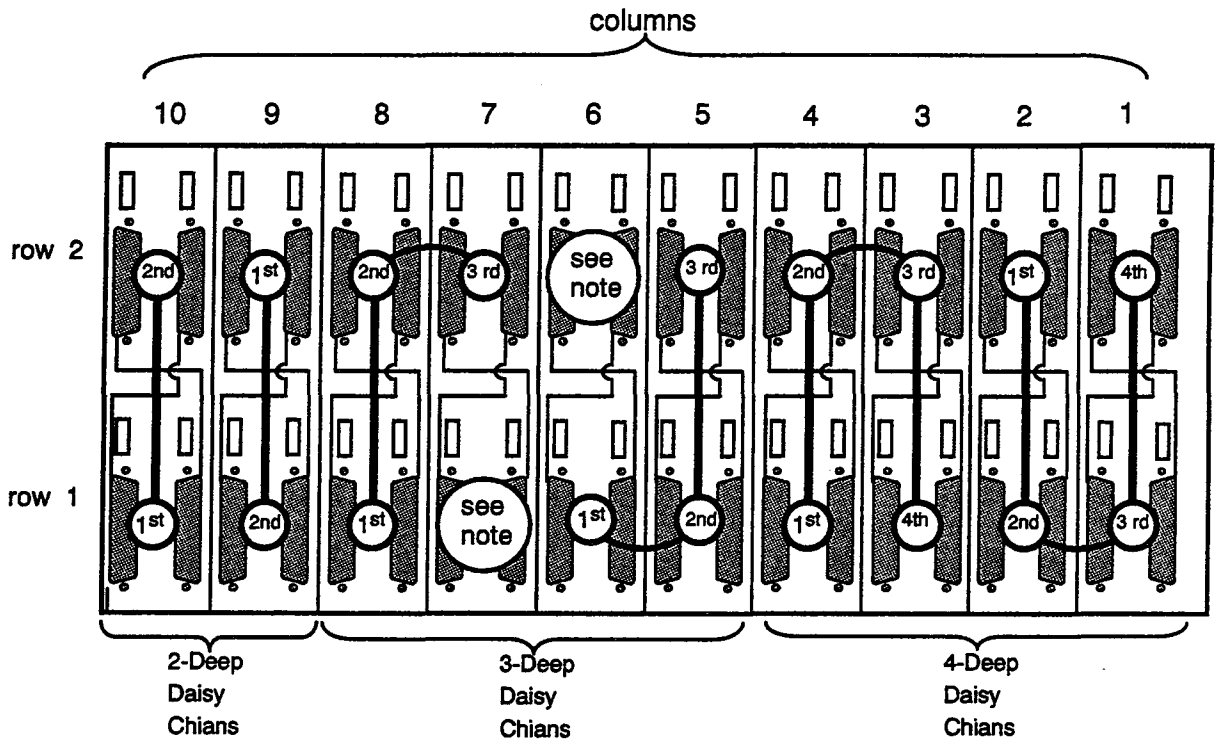


Figure 4-6 DW-300 Single Column Detail

- Implied Dual-Port Interconnects within a DW-300 Drawer Column – The Port A and Port B cable connections between upper and lower drive slots within a column are interconnected via the DW-300 backplane design. Only position drives above/below each other within a column when daisy chain or alternate path configurations are desired. Figure 4-6 illustrates the details of a single column within a DW-300 drawer.

- Drive Positioning in the DW-300 Drawer – The DW-300 drawer can easily accommodate daisy chain and alternate path configurations if the drives are properly positioned within the drawer. When 2 devices are to be connected in a daisy chain or alternate path, they should be positioned above or below each other. When 3 or more devices are to be configured in a daisy chain or alternate path, the IOS-E cable must connect to one of the devices on the left side of the chain (as viewed from the rear of the DW-300). Figure 4-7 shows positioning examples for 2, 3, and 4 deep daisy chain configurations.



Note: These positions may be left vacant to avoid the implicit connections between the upper and lower slots.

Figure 4-7. Drive Positioning for Daisy Chain or Alternate Path (DW-300 rear view)

- DA-301 Disk Array (DCA-3) Cabling Considerations – Cabling of DA-301 disk arrays will require additional cables to provide for the synchronization of the 5 spindles which make up an array. These synchronization (sync) cables are available in various lengths to accommodate numerous drive placement options. Examples of disk array cabling appear at the end of this section.

Cabling Hardware

Cabling hardware for the 300 Series disk drives includes the following:

- IOS-E to Disk Drive Cables (2 lengths)
- Slot-to-Slot Daisy Chain Cable
- Variable Length Daisy Chain Cables (3 lengths)
- Data Cable Terminator
- Synchronization Cables for DA-301 applications (7 lengths)

Table 4-1 lists the cabling hardware components for the 300 series disk drives along with CRI part numbers for each.

CAUTION

These part numbers are subject to change. The part numbers listed below were current at the time this manual was published. Confirm descriptions and part numbers whenever placing orders.

Table 4-1. 300 Series Disk Systems Cable Descriptions

Cable Description	Cable Length	CRI Part Number
IOS-E to Disk Drive Cable (standard)	20 m (66 ft.)	12127800
IOS-E to Disk Drive Cable (optional)	30 m (99 ft.)	12127801
Daisy Chain Cable (slot-to-slot)	10 cm (4 in.)	12299400
Daisy Chain Cable	61 cm (2 ft.)	12300800
Daisy Chain Cable	1.22 m (4 ft.)	12300801
Daisy Chain Cable	2.44 m (8 ft.)	12300802
Synchronization Cable (DCA-3 applications)	10 cm (4 in.)	12301800
Synchronization Cable (DCA-3 applications)	20 cm (8 in.)	12301801
Synchronization Cable (DCA-3 applications)	30.5 cm (1 ft.)	12301802
Synchronization Cable (DCA-3 applications)	61 cm (2 ft.)	12301803
Synchronization Cable (DCA-3 applications)	1.22 m (4 ft.)	12301804
Synchronization Cable (DCA-3 applications)	2.44 m (8 ft.)	12301805
Synchronization Cable (DCA-3 applications)	6.1 m (20 ft.)	12301806
Data Cable Terminator	N/A	01686600

IOS-E to 300 Series Disk Drive Cables

The cables that connect the DCA-2 to a disk drive come in two lengths: 20 m (66 ft) and 30 meters (99 ft). The 20-m cable is standard, and the 30-m cable is optional. Table 4-2 lists the signal assignments for each wire pair in a IOS-E to disk drive cable. Figure 4-1 shows the pin and socket locations on both ends of the cable.

Table 4-2. IOS-E to Disk Drive Cable Signal Definitions

Pair No.	Signal Name	CINCH Connector Socket Number (+)	CINCH Connector Socket Number (–)	Disk Drive Connector Socket Number (+)	Disk Drive Connector Socket Number (–)
1	DC Ground	2	1	1	34
2	Select Out	14	13	43	27
3	Master Out	12	11	45	29
4	Sync Out	6	5	41	25
5	Sync In	10	9	15	48
6	Slave In	8	7	39	23
7	Attention In	4	3	20	4
8	Bus A – Bit 0	34	33	13	46
9	Bus A – Bit 1	37	36	30	14
10	Bus A – Bit 2	39	38	22	6
11	Bus A – Bit 3	41	40	26	10
12	Bus A – Bit 4	43	42	11	44
13	Bus A – Bit 5	45	44	28	12
14	Bus A – Bit 6	47	46	37	21
15	Bus A – Bit 7	49	48	5	38
16	Bus A – Parity Bit	51	50	47	31
17	Bus B – Bit 0	16	15	32	16
18	Bus B – Bit 1	18	17	49	33
19	Bus B – Bit 2	20	19	3	36
20	Bus B – Bit 3	22	21	7	40
21	Bus B – Bit 4	24	23	24	8
22	Bus B – Bit 5	26	25	9	42
23	Bus B – Bit 6	28	27	18	2
24	Bus B – Bit 7	30	29	35	19
25	Bus B – Parity Bit	32	31	17	50

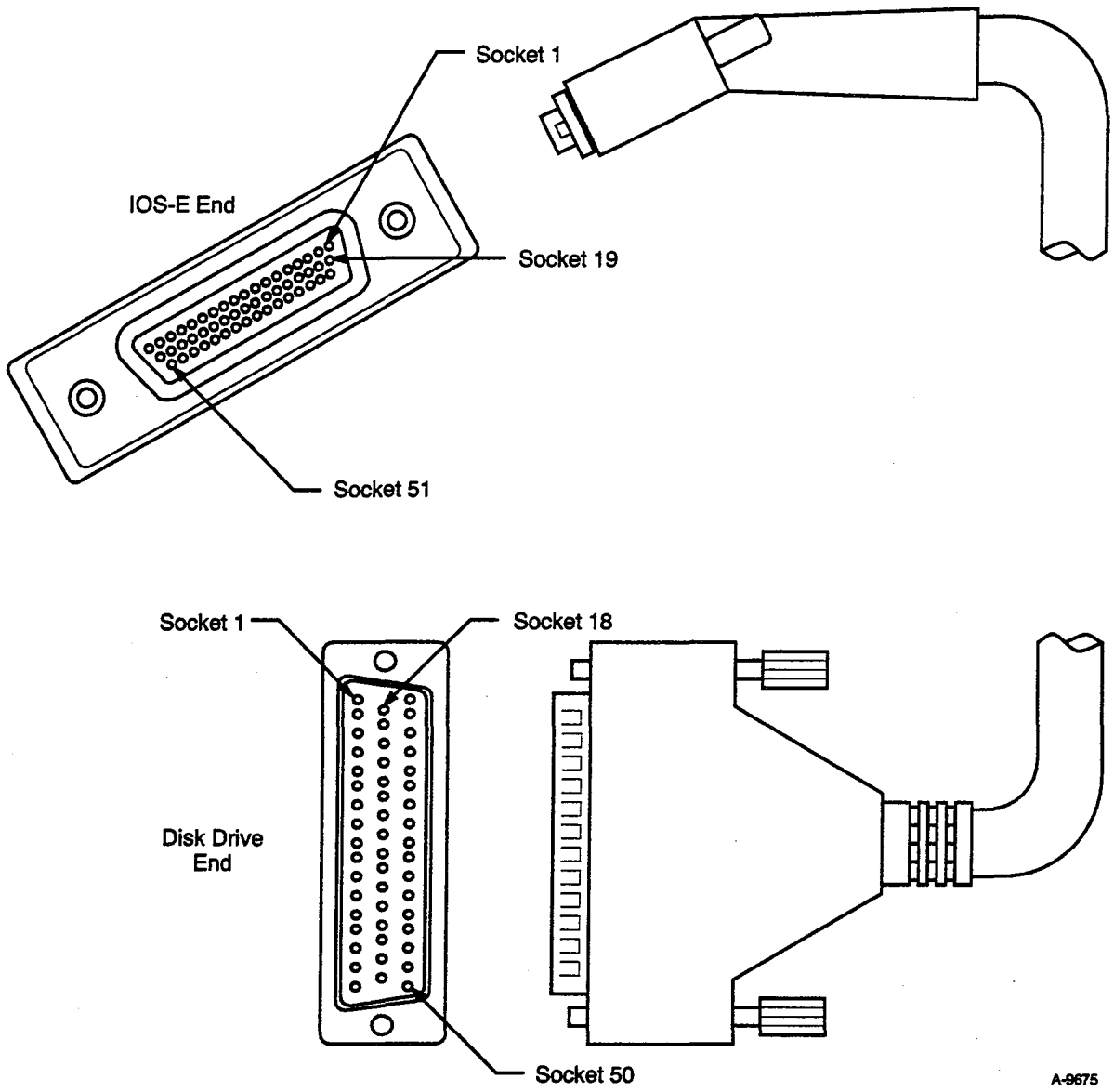


Figure 4-1. IOS-E to Disk Drive Cable Pin and Socket Locations

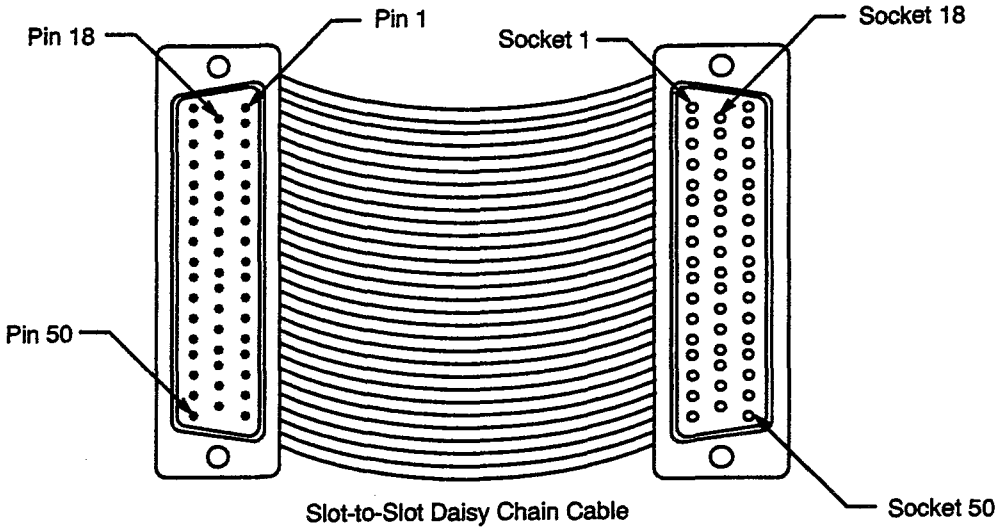
Daisy Chain Cables

Two different daisy chain cables are available for the 300 series disk drives. The daisy chain cable (slot-to-slot) used for connecting between adjacent slots within a single drawer are 4 in long. The daisy chain cables (drawer-to-drawer) used for connecting across greater distances are 2, 4,

and 8 feet in length. Table 4-3 lists the signal assignments for each wire in the daisy chain cables. Figure 4-2 shows the pin and socket locations on both ends of these cables.

Table 4-3. Daisy Chain Cable Signal Definitions

Pair No.	Signal Name	Disk Drive Connector Pin Number (+)	Disk Drive Connector Pin Number (–)	Disk Drive Connector Socket Number (+)	Disk Drive Connector Socket Number (–)
1	DC Ground	1	34	1	34
2	Select Out	43	27	43	27
3	Master Out	45	29	45	29
4	Sync Out	41	25	41	25
5	Sync In	15	48	15	48
6	Slave In	39	23	39	23
7	Attention In	20	4	20	4
8	Bus A – Bit 0	13	46	13	46
9	Bus A – Bit 1	30	14	30	14
10	Bus A – Bit 2	22	6	22	6
11	Bus A – Bit 3	26	10	26	10
12	Bus A – Bit 4	11	44	11	44
13	Bus A – Bit 5	28	12	28	12
14	Bus A – Bit 6	37	21	37	21
15	Bus A – Bit 7	5	38	5	38
16	Bus A – Parity Bit	47	31	47	31
17	Bus B – Bit 0	32	16	32	16
18	Bus B – Bit 1	49	33	49	33
19	Bus B – Bit 2	3	36	3	36
20	Bus B – Bit 3	7	40	7	40
21	Bus B – Bit 4	24	8	24	8
22	Bus B – Bit 5	9	42	9	42
23	Bus B – Bit 6	18	2	18	2
24	Bus B – Bit 7	35	19	35	19
25	Bus B – Parity Bit	17	50	17	50



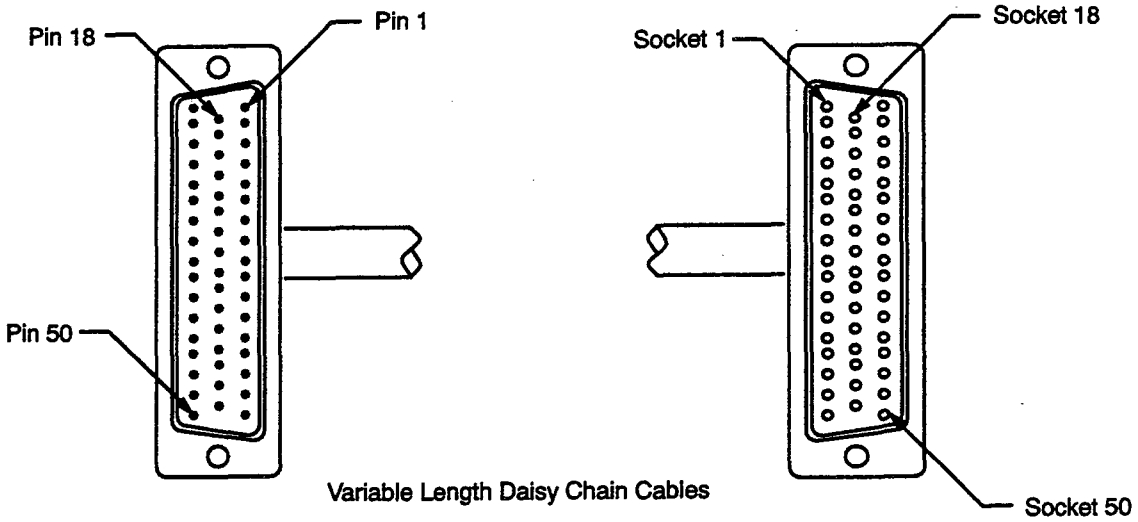


Figure 4-2. Daisy Chain Cable Pin and Socket Locations

Terminator

The terminator for the 300 series disk drives must be used to terminate signals on the last, or only, device connected to a channel. The CRI part number for the terminator is 01686600. Figure 4-3 shows the terminator.

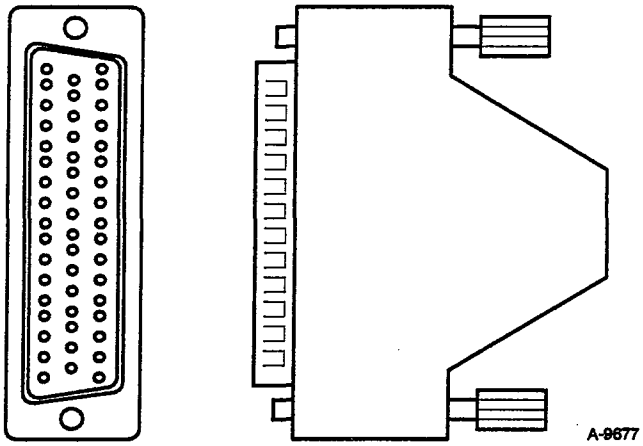


Figure 4-3. Terminator for 300 Series Disk Systems

Synchronization Cables (DCA-3 applications only)

The spindle-to-spindle sync cables are connected between the five spindles within an array to accommodate rotational synchronization. The sync cables are available in 7 different lengths to accommodate the various distances separating spindles within a disk array. The sync cable connectors attach to the primary and alternate sync connections at the rear of each spindle slot in the DW-300 drawer. Termination for the sync signal is unnecessary due to the design of the DW-300 drawer. Refer to Figure 4-4 for an illustration of the sync cable.

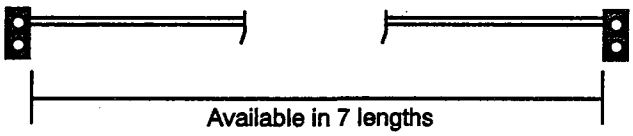


Figure 4-4. Synchronization (Sync) Cables

Two separate sync cables are required for each spindle within a disk array to provide for primary and alternate synchronization connections. Refer to Figure 4–14 and Figure 4-16 for examples of sync cable connections.

Cable Labels

Label all drive cables at both ends to avoid connecting 300 series disk drives to the wrong type of channel adapter. Each label should contain the EIOP identification, channel number, device type, drive unit number(s), and physical location of the device(s) to which the cable connects. A range of unit numbers can be specified for daisy chained channels. Figure 4-5 shows an example of a sample cable label.

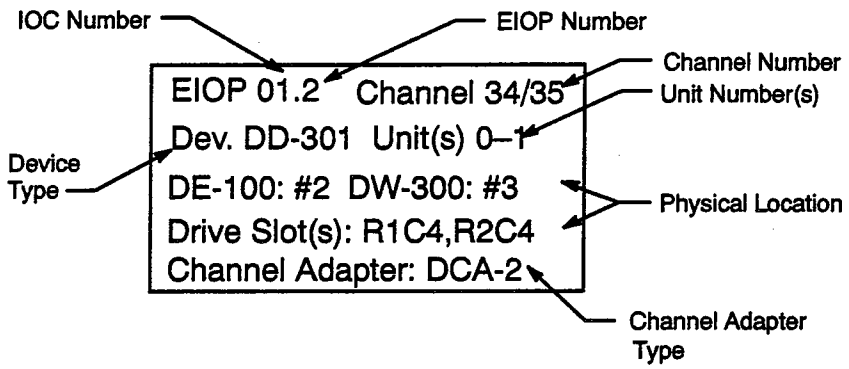


Figure 4-5. 300 Series Disk Drive Cable Label

Configurations

300 series disk drives can be cabled in the following configurations:

- Single device
- Daisy Chain (Single-port)
- Alternate Path (Dual-port daisy chain)

Table 4-4. Comparison of 300 Series Disk Drive Configurations

Configuration	# of Channel Adapters	Disk Devices	Advantages
Single device	1	1	Fast data-transfer rate
Daisy chain	1	2 to 8	Large storage capacity per channel
Alternate path	2	2 to 8	Dual-channel access to devices for resiliency to channel failures

Single Device Configuration

A single device configuration connects one channel adapter to one disk device. In this configuration, the channel accesses information at the maximum data-transfer rate of the disk device. Because only one device connects to the channel, the storage capacity of the channel is the storage capacity of the disk device.

Daisy Chain Configuration

A daisy chain configuration connects one channel adapter to a maximum of eight devices. The data-storage capacity of the channel is the total storage capacity of all the devices in the daisy chain. Because only one device can transfer data at a time, the data-transfer rate of the channel is the maximum transfer rate of one device.

Alternate-Path Configuration

In an alternate path configuration, devices are accessible from either of two channel adapters. In application, alternate-path configurations can be described as a dual-ported connection to a daisy chain. For example, two disk drives are each connected to separate channel adapters in a single device configuration. If the two drives are interconnected using a second port on each drive, an alternate-path connection results. Under normal operation, each channel provides access to one of the disk drives, but if either channel becomes inaccessible both drives can be accessed from the remaining channel as a daisy chain.

The design of the 300 series disk systems includes hardware connections which support alternate-path configurations. Refer to the "DW-300 " section in this manual for more information on these connections.

Recent software releases provide support for the resiliency advantages of alternate-path configurations. When the primary path to a device becomes inaccessible, software commands can be used to enable the alternate path.

Three possibilities exist for the location of the two channel adapters used in an alternate path configuration: within an EIOP, between two EIOPs, or between two input/output clusters (IOCs).

- Alternate-path within an EIOP

  When the two channel adapters used in an alternate path configuration exist within the same EIOP, the device(s) are only resilient to the failure of a channel adapter. A failure of the respective EIOP results in all devices attached to the EIOP being inaccessible.

- Alternate-path between two EIOPs

  When the two channel adapters used in an alternate path configuration exist within the same cluster (IOC) but separate EIOPs, the device(s) are resilient to the failure of a channel adapter and an EIOP. However, a failure of the respective IOC results in all devices attached to the IOC being inaccessible.

- Alternate-path between two IOCs

  When the two channel adapters used in an alternate path configuration exist within separate clusters (IOCs), maximum resiliency is realized. This, however, requires the I/O subsystem to include a minimum of two clusters.

DD-301 Cabling Configurations

The following subsection describes several configuration options which are possible for the DD-301 disk drives. IOS-E bulkhead connections, block diagrams, and DW-300 connections are shown for each example.

The examples in this subsection demonstrate the basic principles surrounding the configuration options of the DD-301 disk drives. Actual applications may involve combinations of these basic options. Once you understand all the functional implications of each option, you can apply these principles to your site.

DCA-2 Bulkhead Connectors

Disk drives are connected to DCA-2 channel adapters through the IOS-E bulkhead. Figure 4-6 shows possible input/output cluster (IOC) 0 connector locations on the Z side of a CRAY Y-MP8I computer system.

Each EIOP has up to four channel adapters. Two channel adapter connectors are located on each side of the chassis. For example, the connectors for channel adapters 0 and 2, which are connected to EIOP 0, are on the Z side of the chassis (refer to Figure 4-6). The connectors for channel adapters 1 and 3, which are also connected to EIOP 0, are on the Y side of the chassis (not shown in Figure 4-6).

300 series disk drive cables attach to the even-numbered connector (In) of the connector pair for each DCA-2. For example, the cable for a DD-301 connected to the DCA-2 in the number 5 channel adapter position would attach to connector 04 (refer again to Figure 4-6).

The exact layout of an IOS-E bulkhead depends on the chassis type and serial number of a particular machine. The 700, 1600, 1700, 1900, and 2600 series products all represent slight differences in bulkhead design. In addition, differences can exist between machines of different serial numbers within a product group. Not all possible bulkhead layouts are represented in this manual.

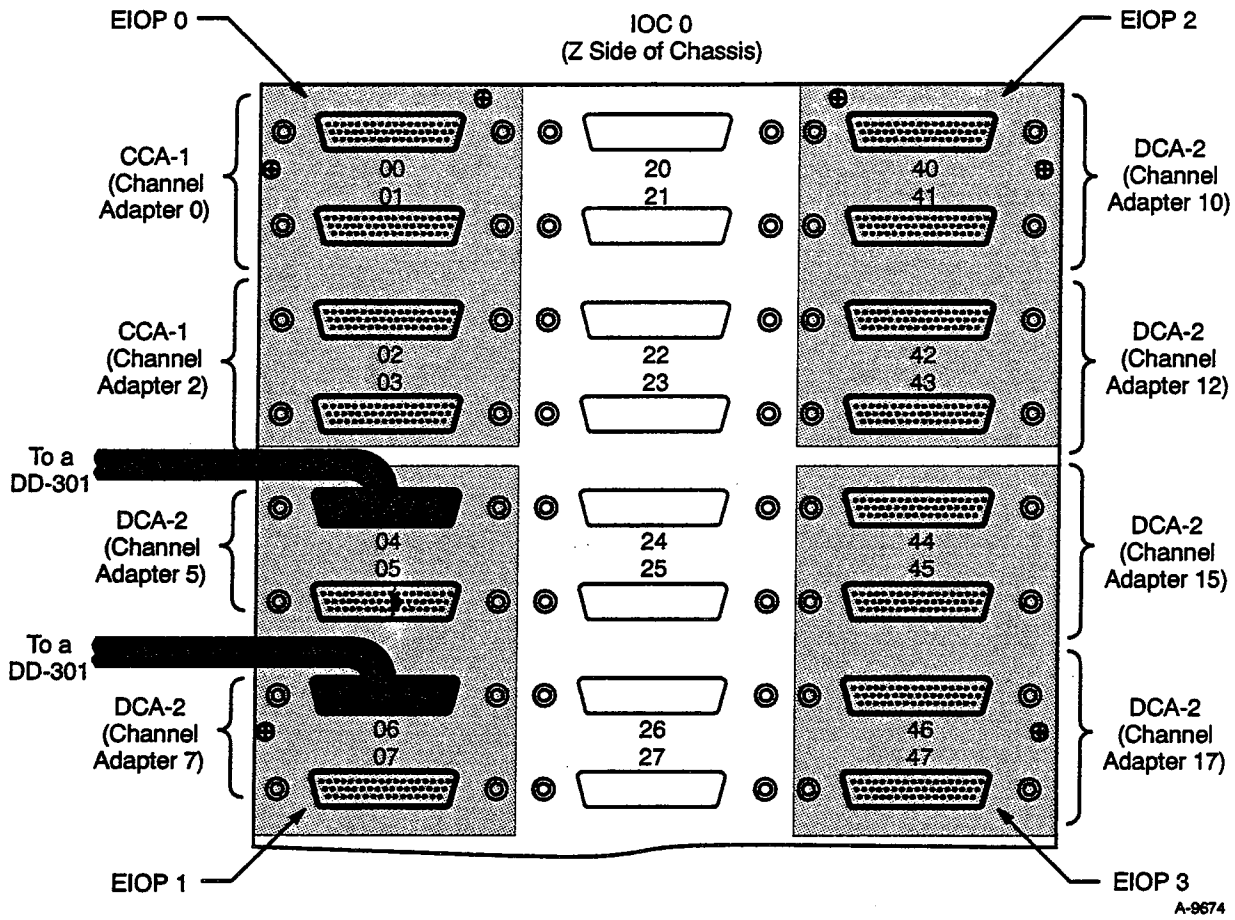


Figure 4-6. Possible IOC 0 Configuration on a CRAY Y-MP8I Computer System

Ensure that all cables and bulkhead connections are clearly labeled to avoid incorrect connections. Channel adapters must only be connected to devices for which they are designed.

CAUTION

Always ensure DCA-2 channel adapters connect to IPI-2 type disk drives only. Connecting channel adapters to the wrong type of device results in damage to the device(s) and/or channel adapters.

Single Primary Devices with Alternate-Path

In the following example, 20 DD-301 disk devices within a DW-300 drawer are connected in a single device configuration with alternate-path capabilities. It is important to note that the alternate path interconnects are provided in the design of the DW-300 by default. Refer to the "DW-300 Drawer" section in this manual for more information on these interconnects.

Figure 4-7 shows a block diagram of this example. Figure 4-8 shows the DW-300 drawer connections for this example.

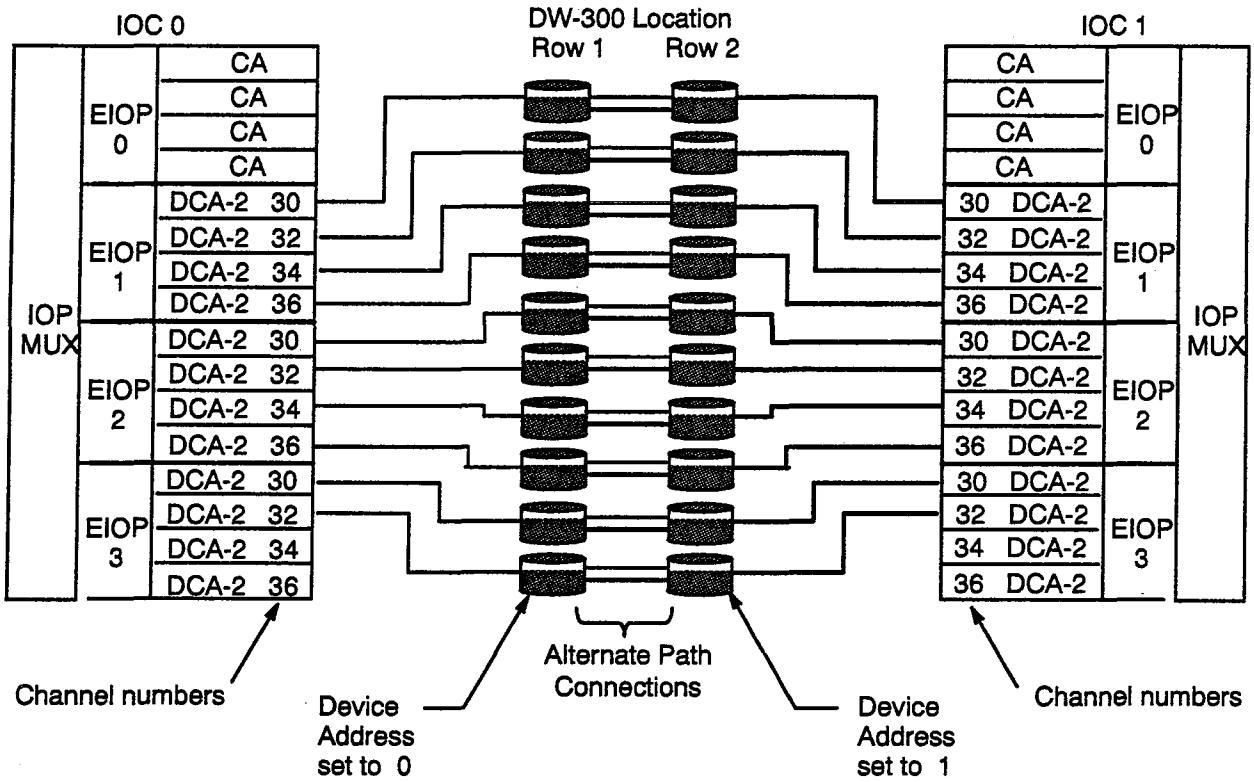


Figure 4-7. Single Device Configuration with Alternate Path

CAUTION

Ensure DD-301 disk drives which occupy the same column in a DW-300 drawer are set to unique device addresses. Failure to do so results in address duplication on a daisy chain and channel errors.

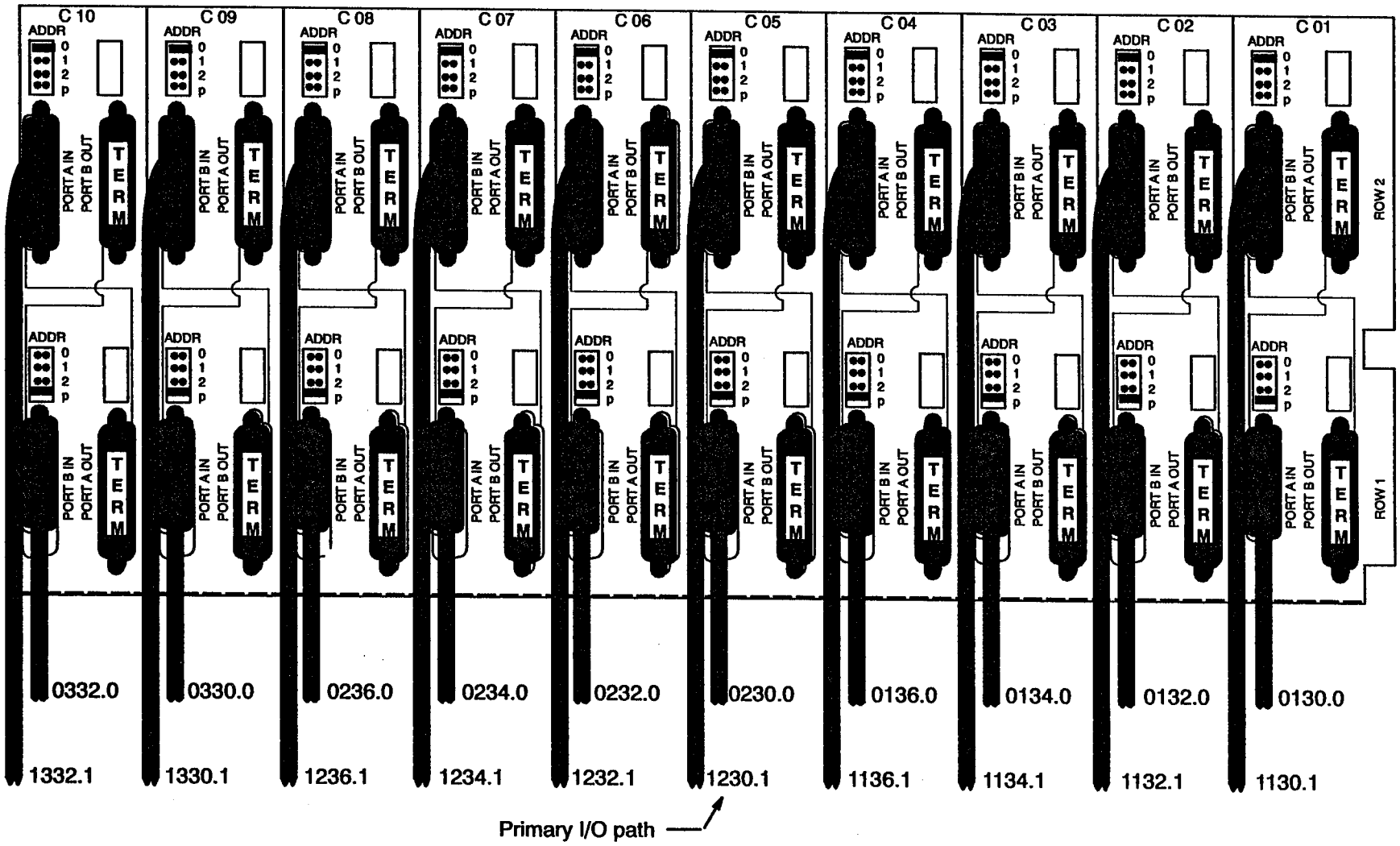


Figure 4-8. DW-300 Connections for Single Device Cabling with Alternate Path

Daisy Chain Cabling with Alternate-Path

In the following example, 20 DD-301 disk devices within a DW-300 drawer are connected in daisy chain configurations with alternate-path capabilities.

Figure 4-9 shows a block diagram of this example. Figure 4-10 shows the DW-300 drawer connections for this example.

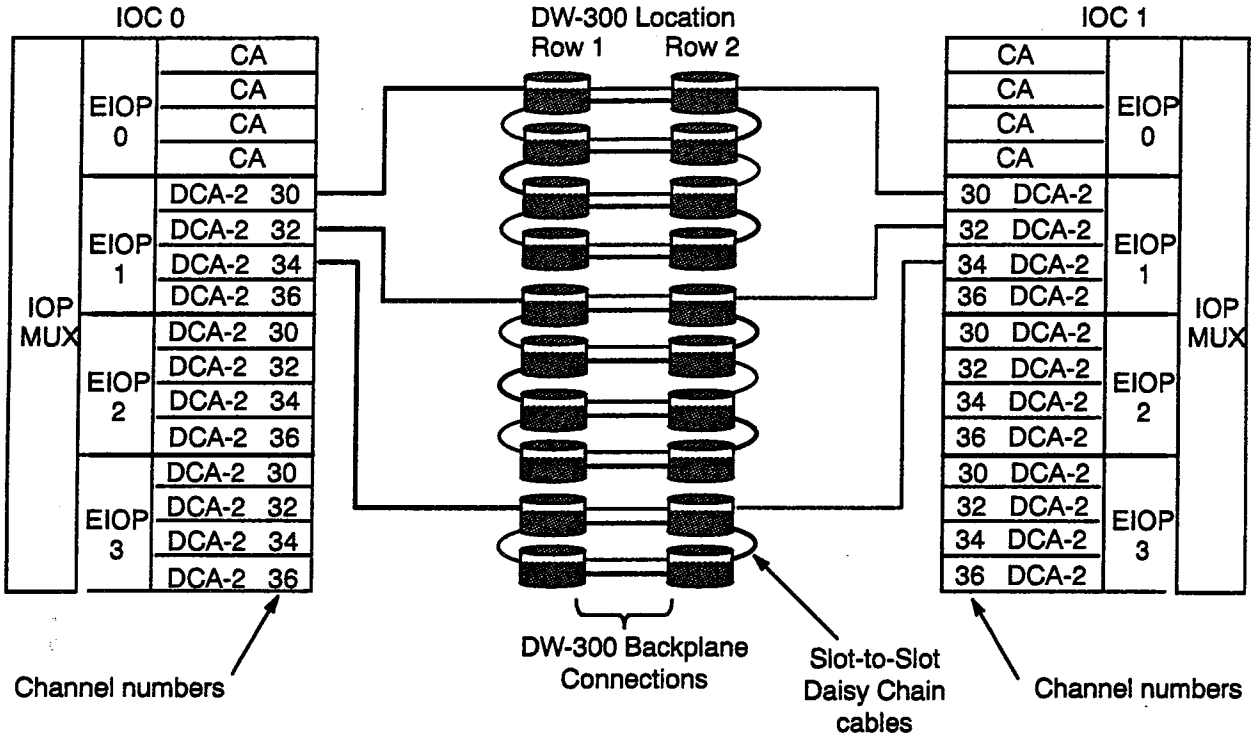


Figure 4-9. DD-301 Daisy Chain Configurations with Alternate Path

NOTE: The drive slots within a DW-300 drawer should be filled from column 10 to column 1 whenever slot-to-slot daisy chain cables are used. Refer again to Figure 4-10.

CAUTION

Ensure DD-301 disk drives which occupy the same column in a DW-300 drawer are set to unique device addresses. Failure to do so results in address duplication on a daisy chain and channel errors.

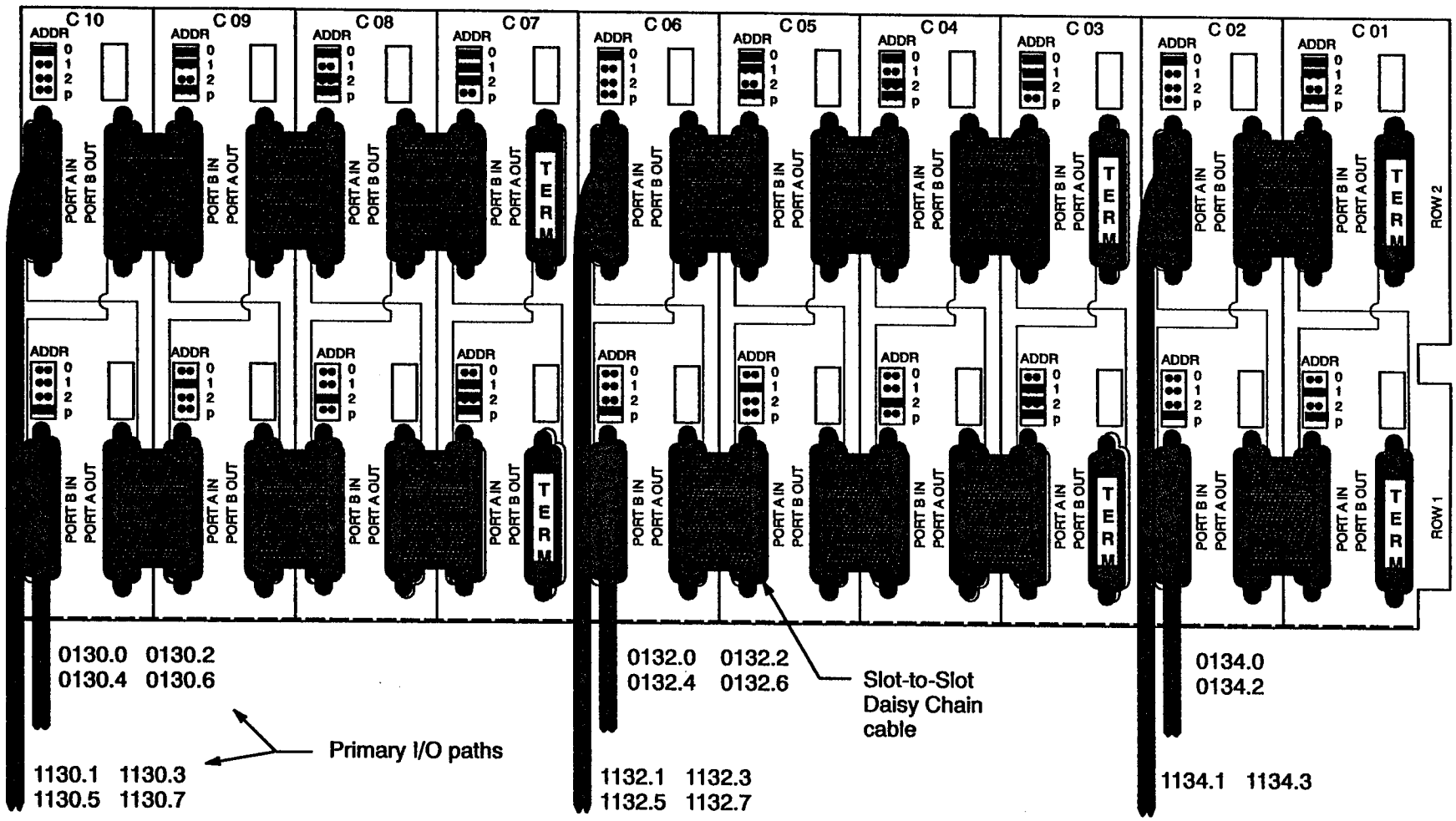


Figure 4-10. DW-300 Connections for Daisy Chain Configurations with Alternate Path

DA-301 Disk Array Cabling Configurations

The DCA-3 channel adapter supports a five-spindle disk array referred to as a DA-301. Four of the spindles hold data while the fifth spindle contains parity information on the data. As many as eight disk arrays can be daisy chained on a single DCA-3. Figure 4-11 is an overview of a two-array daisy chain.

The spindles are housed in DW-300 drawers within DE-100 disk enclosures. Each cabinet contains up to four drawers while each drawer contains up to twenty spindles. As many as four disk arrays can be housed within a single DW-300 drawer, with up to sixteen arrays in a single DE-100 cabinet.

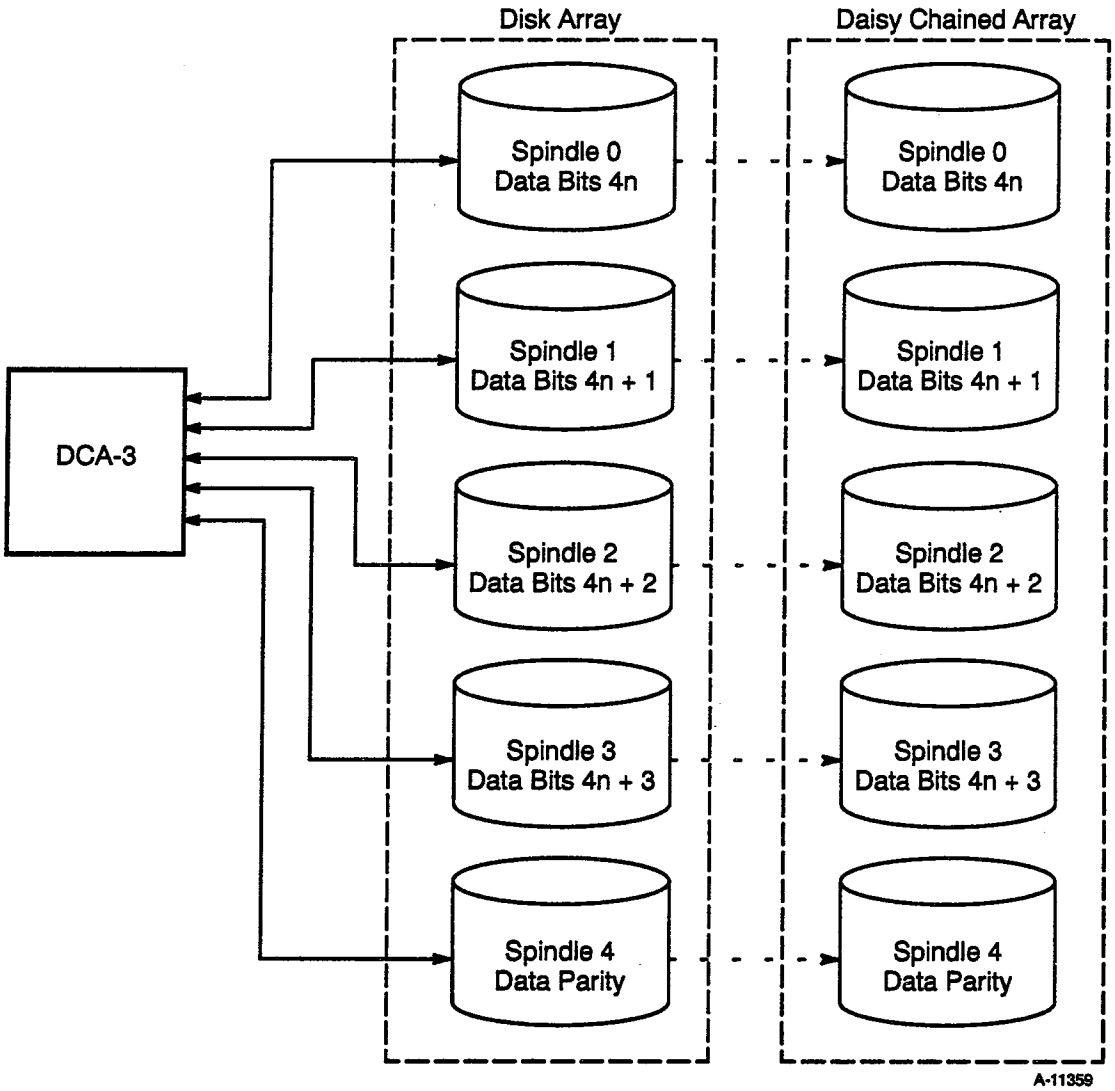


Figure 4-11. Disk Array Overview Block Diagram

IOS-E Bulkhead Connections

Standard bulkhead arrangements on an IOS-E allow for two connections per quarter board position. Because the DCA-3 is a half board channel adapter, it uses each pair of connections normally assigned to the two quarter board positions it occupies. For example, a DCA-3 installed as logical channel pair 34/35 uses the two bulkhead connections for those channels as well as the two connections for channel pair 30/31. A DCA-3 installed as logical channel pair 36/37 also uses the bulkhead connections for channel pair 32/33.

The half board design of the DCA-3 provides four bulkhead connections (one for each of the data spindles), but a fifth connection is needed for the parity spindle. Special wiring in the backplane of the IOS-E accommodates this fifth connection. Field change orders (FCOs) and Engineering change orders (ECOs) exist to provide this special wiring. This manual assumes the necessary wiring has been installed in the IOS-E.

In all DCA-3 applications, the four data spindle cables are connected to one side of the IOS-E/mainframe chassis; the parity spindle cable is connected to the opposite side. Bundling the cables should enable the parity spindle cable to reach the opposite side of the chassis.

The exact layout of an IOS-E bulkhead depends on the chassis type and serial number of a machine. The 700, 1600, 1700, 1900, and 2600 series products all represent slight differences in bulkhead design. In addition, differences can exist between different serial numbers within a product group. Not all possible bulkhead layouts are represented in this manual. Table 4-5 lists the DCA-3 bulkhead assignments for cluster 0 of a 700 series IOS-E. Figure 4-12 shows the position of these connections on the bulkhead.

Table 4-5. DCA-3 Bulkhead Connections for 700 Series (Cluster 0)

Physical Position	Logical I/O Path	Data Spindle (0,1,2,3) Connections	Parity Spindle Connection
CA0 / CA2	00034	ZB 00, 01, 02, 03 (A)†	YB 20 (A)†
CA1 / CA3	00036	YB 00, 01, 02, 03 (B)†	ZB 20 (B)†
CA4 / CA6	00134	YB 04, 05, 06, 07 (C)†	ZB 22 (C)†
CA5 / CA7	00136	ZB 04, 05, 06, 07 (D)†	YB 22 (D)†
CA10 / CA12	00234	ZB 40, 41, 42, 43 (E)†	YB 24 (E)†
CA11 / CA13	00236	YB 40, 41, 42, 43 (F)†	ZB 24 (F)†
CA14 / CA16	00334	YB 44, 45, 46, 47 (G)†	ZB 26 (G)†
CA15 / CA17	00336	ZB 44, 45, 46, 47 (H)†	YB 26 (H)†

† Denotes position indicator used in Figure 4-12

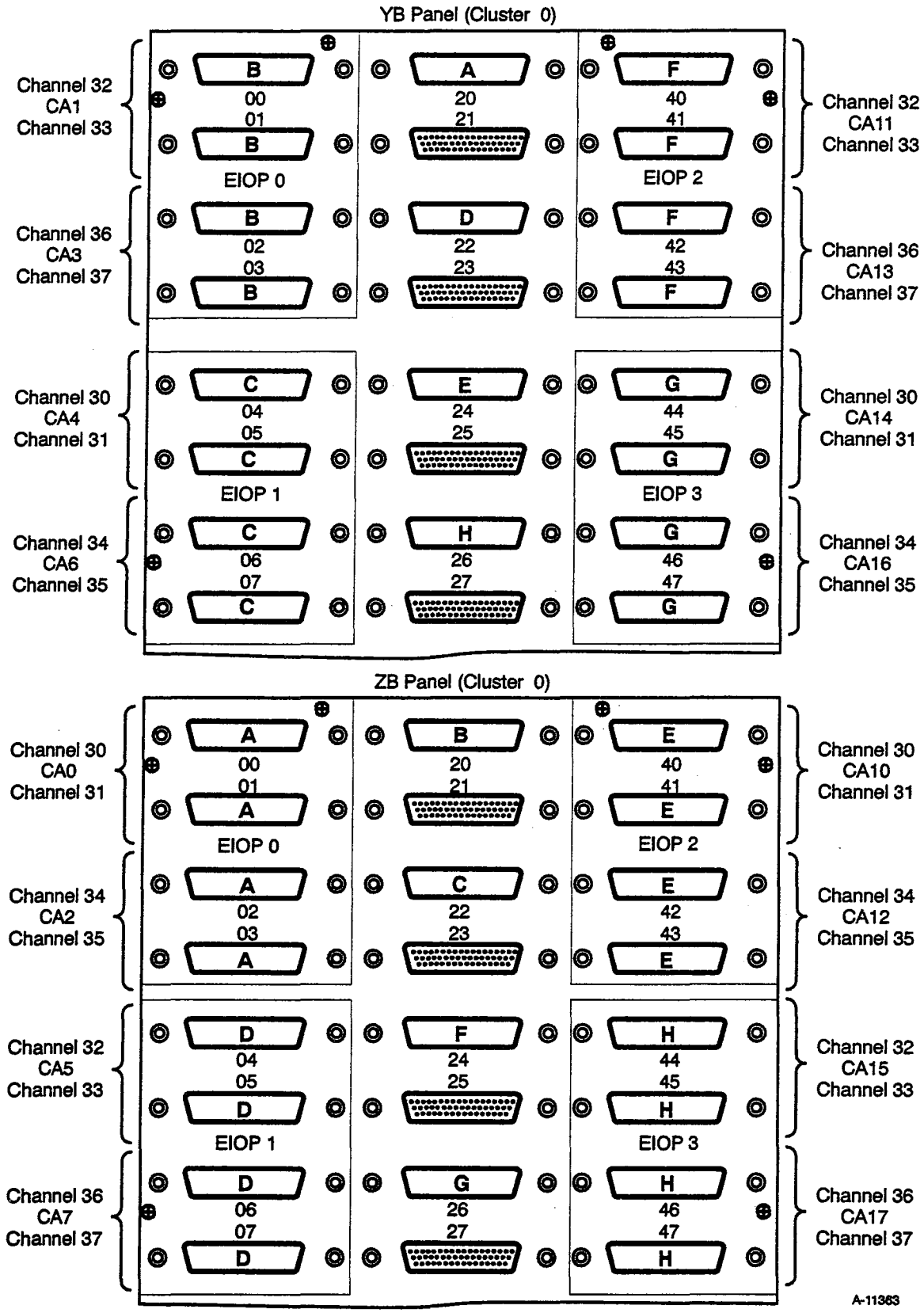


Figure 4-12. DCA-3 Bulkhead Connections for 700 Series IOS-E

Single Array Configurations with Alternate Path

In the following example, the 20 spindles within a DW-300 drawer are grouped into 4 DA-301 disk arrays. Each array is accessible through a separate primary channel, with the DW-300 backplane design providing alternate path access between array pairs (row 1 and row 2).

The same device address setting is used for all 5 spindles within a disk array, however disk arrays which are connected in an alternate path configuration must have unique address settings. Figure 4-13 shows a block diagram of this example. Figure 4–14 shows the DW-300 drawer connections for this example.

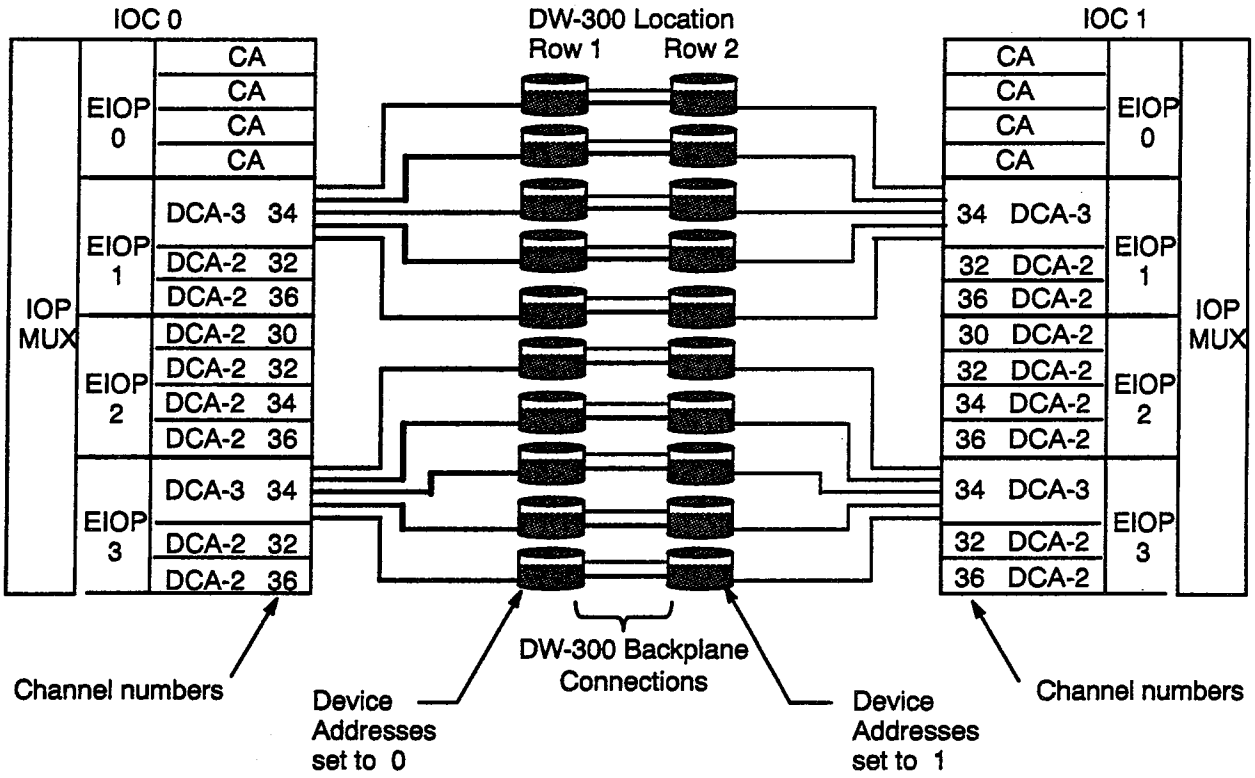


Figure 4-13. Single Array Configuration with Alternate Path

CAUTION

Ensure DD-301 spindles which occupy the same column in a DW-300 drawer are set to unique device addresses. Failure to do so results in address duplication on a daisy chain and channel errors.

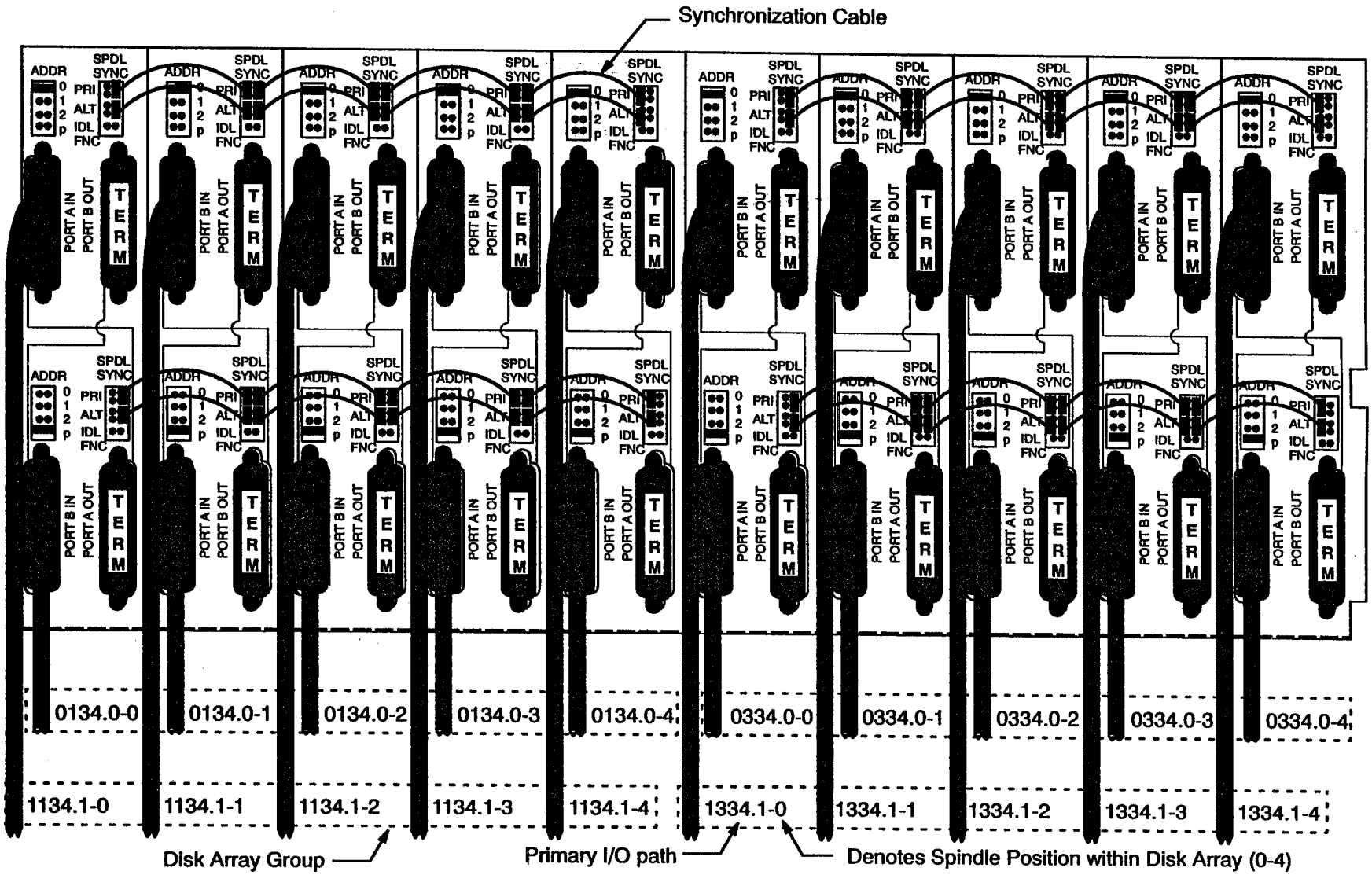


Figure 4–14. DW-300 Connections for Single Array Configurations with Alternate Path

Daisy Chain Array Configurations with Alternate Path

In the following example, the 20 spindles within a DW-300 drawer are grouped into 4 DA-301 disk arrays. Two daisy chain arrays are assigned as primary devices on each of the DCA-3 channel adapters, with the DW-300 backplane design providing alternate path access between array pairs.

The same device address setting is used for all 5 spindles within a disk array, however disk arrays which are connected in an alternate path configuration must have unique address settings. Figure 4-15 shows a block diagram of this example. Figure 4-16 shows the DW-300 drawer connections for this example.

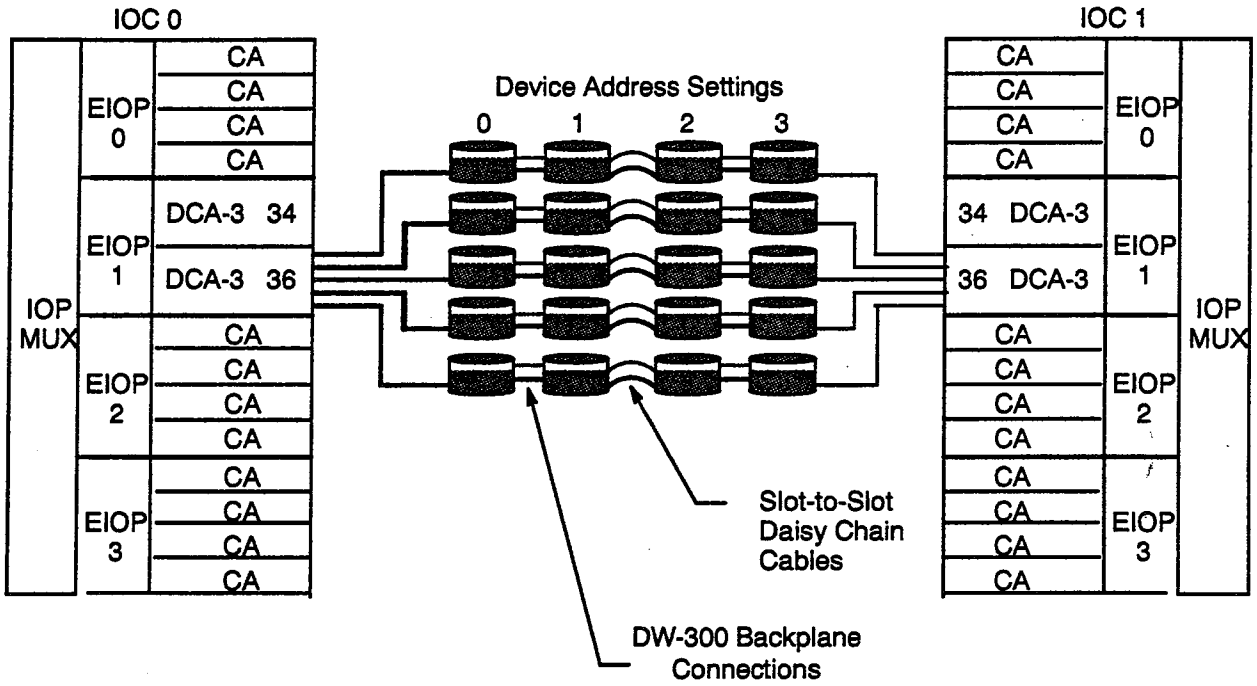


Figure 4-15. Daisy Chain Array Configuration with Alternate Path

CAUTION

Ensure DD-301 spindles which occupy the same column in a DW-300 drawer are set to unique device addresses. Failure to do so results in address duplication on a daisy chain and channel errors.

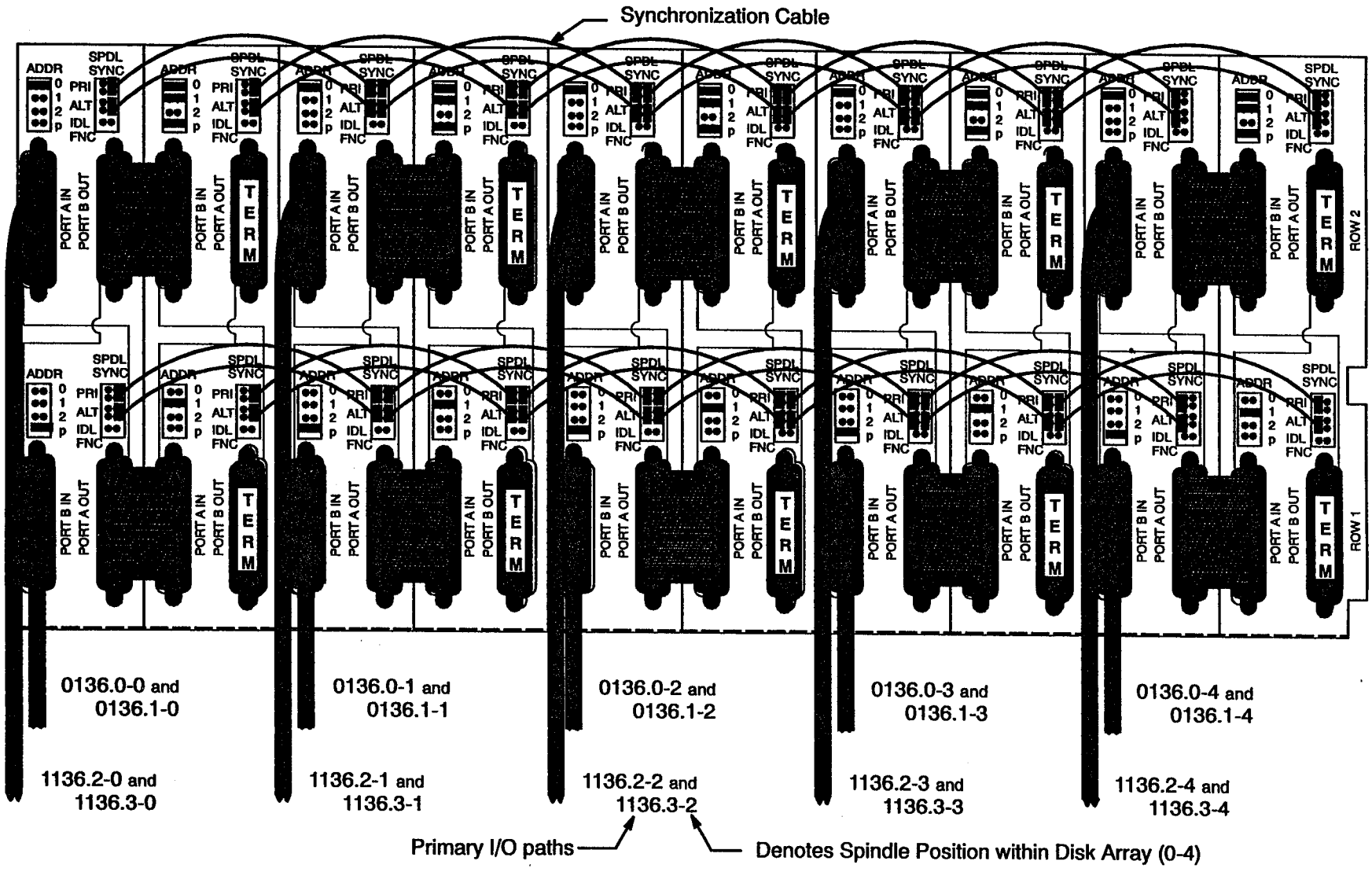


Figure 4-16. DW-300 Connections for an Array Daisy Chain Configuration with Alternate Path

DE-100 cabinet #____ DW-300 Drawer #____ **FRONT VIEW**

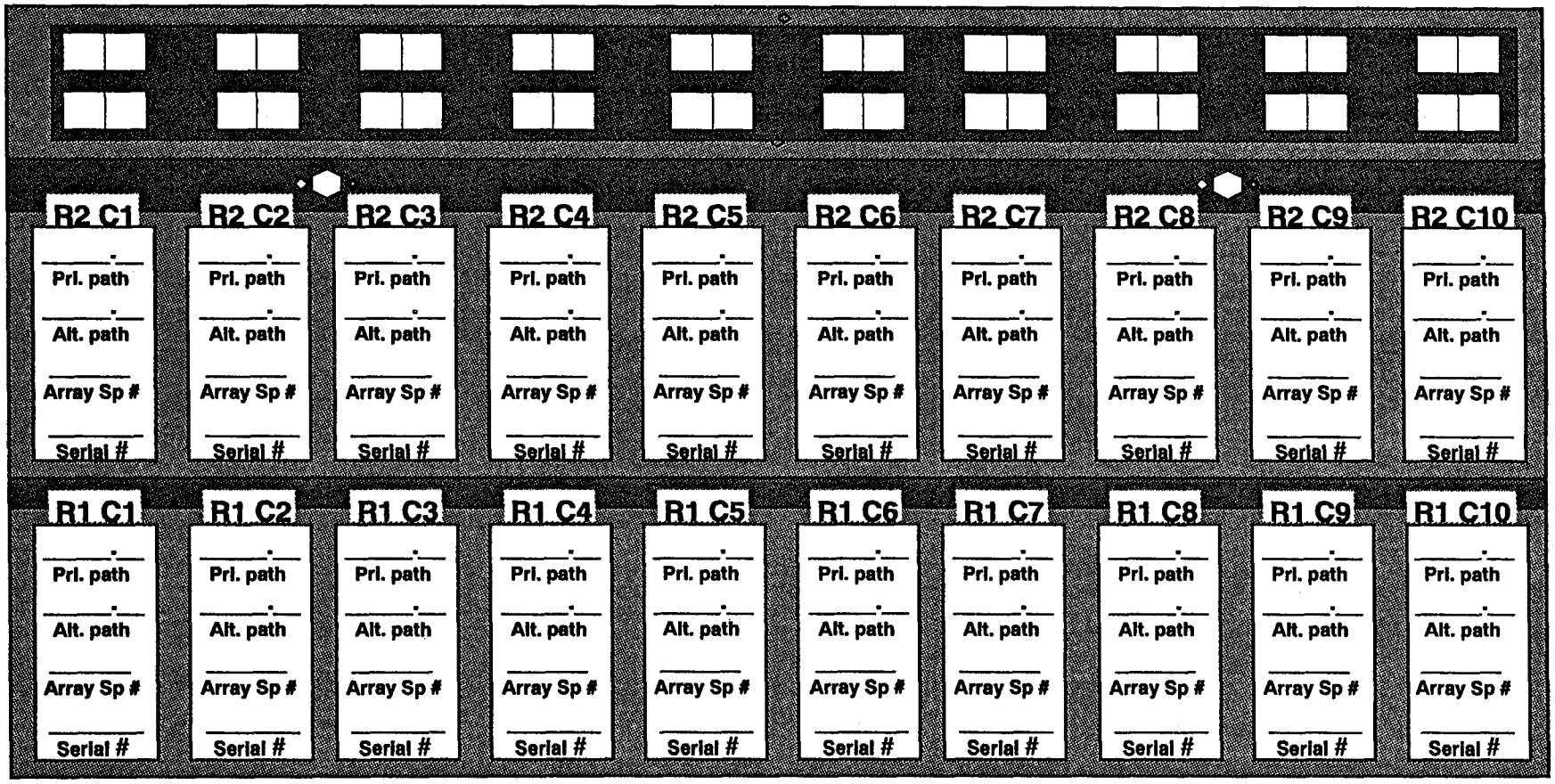


Figure 4–17. DW-300 Device Labeling Chart (front)

DE-100 cabinet #____ DW-300 Drawer #____ **REAR VIEW**

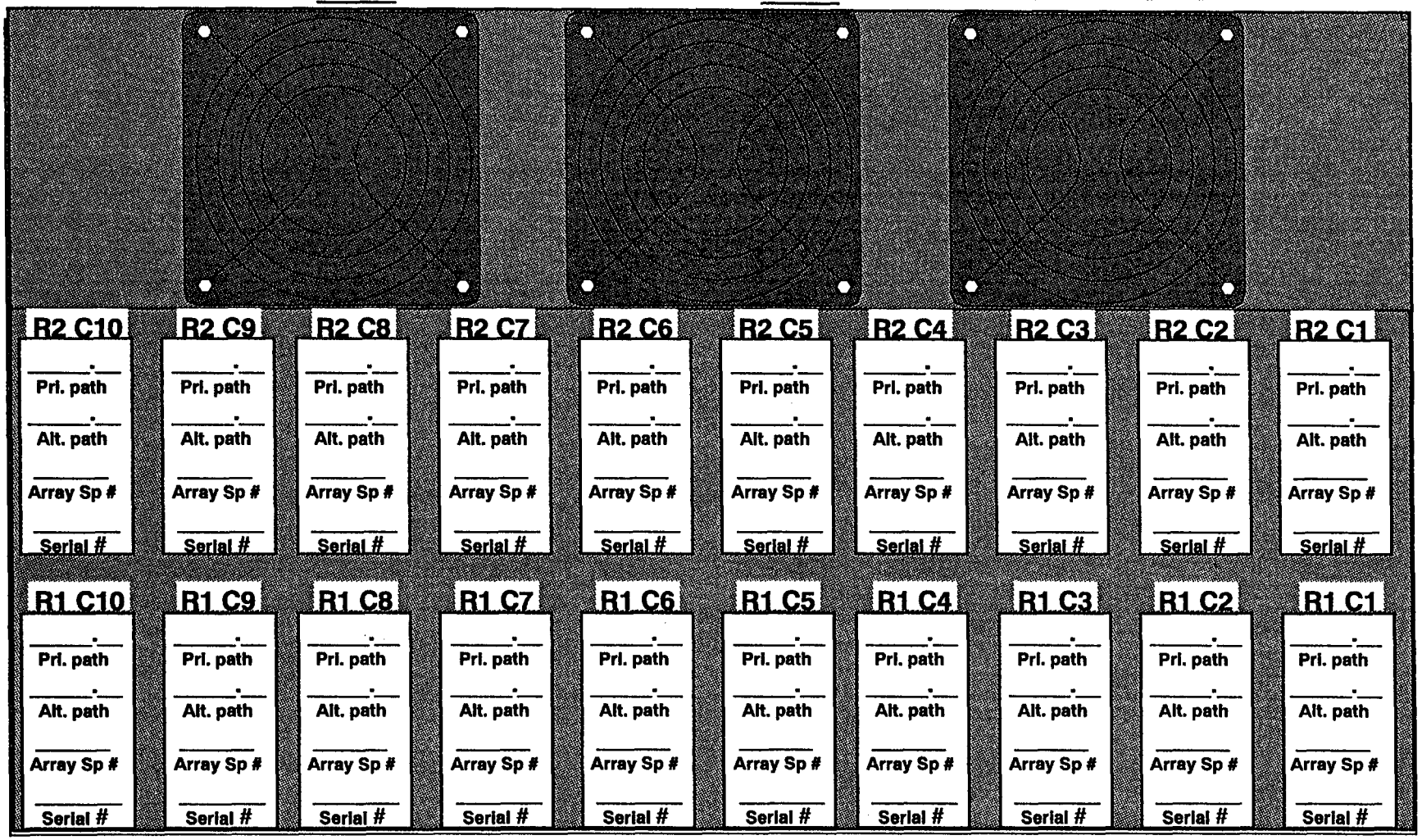


Figure 4–18. DW-300 Device Labeling Chart (rear)

5 DD-301 HARDWARE DESCRIPTION

The DD-301 is a 3.5 inch Winchester type device packaged in a carrier assembly which enables it to plug into a DW-300 drawer. Pin pairs in the rear connector supply +36 Vdc to the drive.

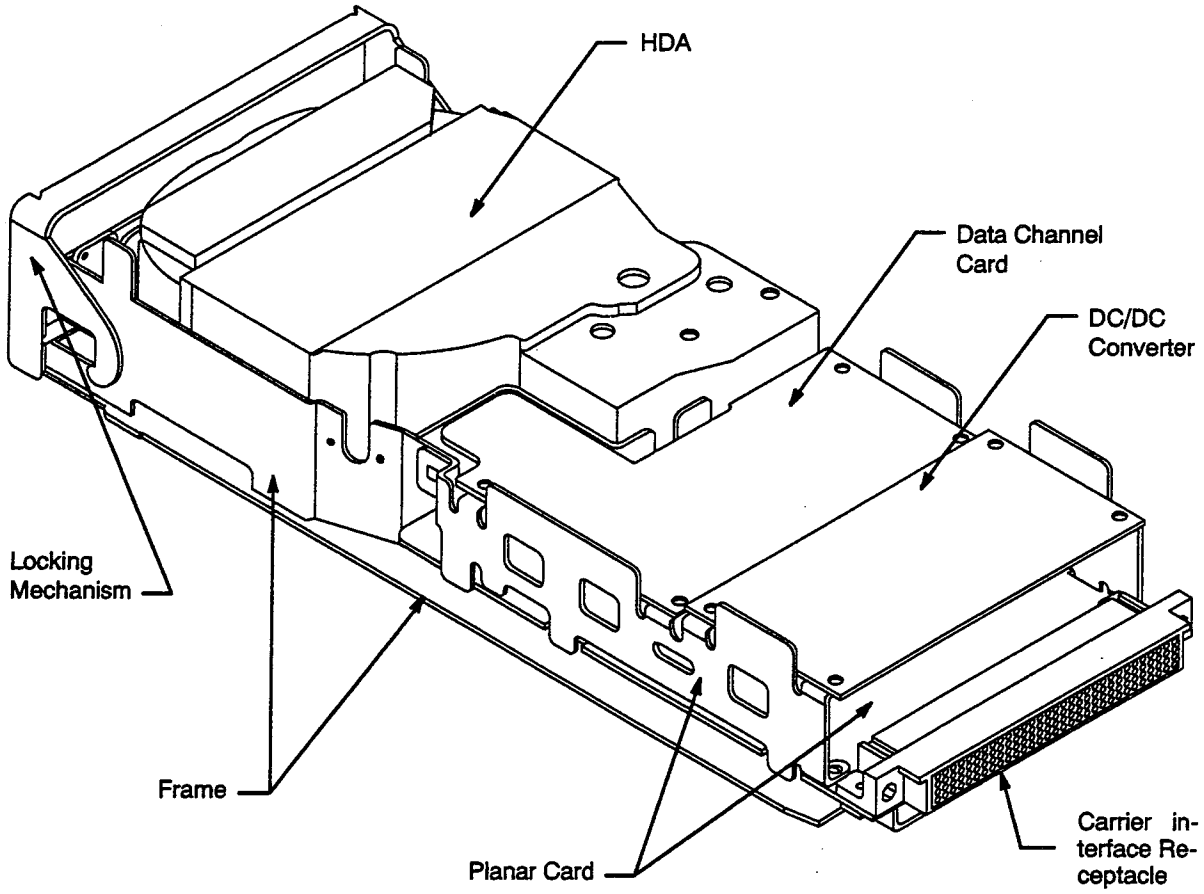


Figure 5-1. RDS Carrier Assembly

Front Panel

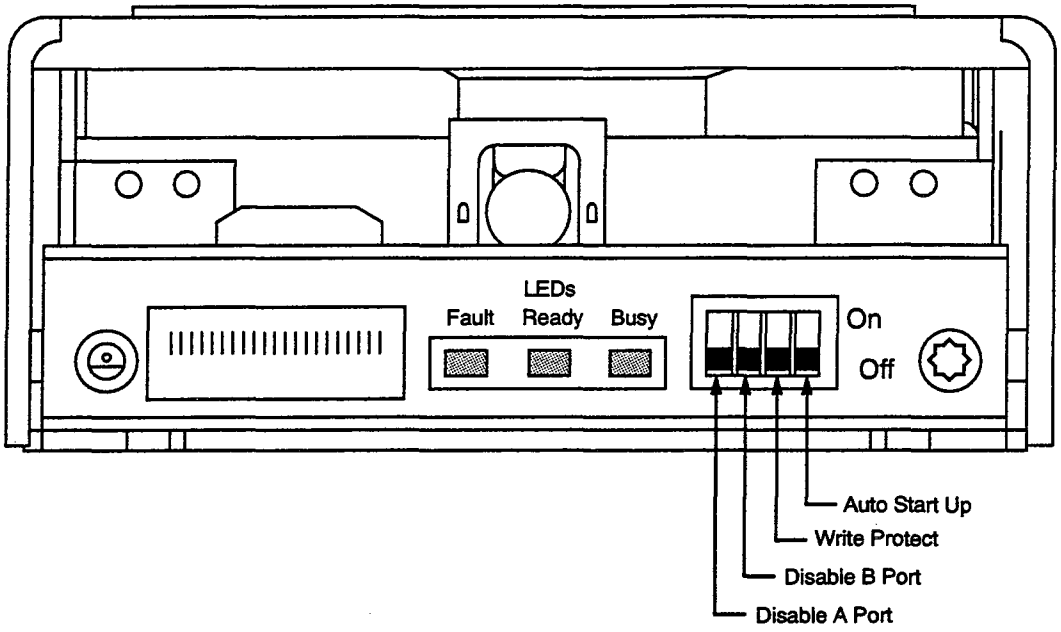


Figure 5-2. DD-301 Front Panel

Front Panel Switch Settings

The front panel of the DD-301 includes a four position switch block that allows selection of automatic motor startup, write protection, and port enable/disable (refer to Figure 5-3).

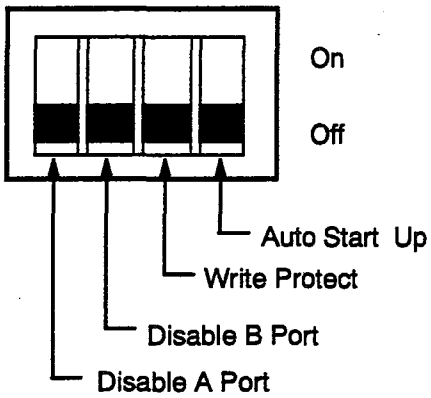


Figure 5-3. DD-301 Front Panel Switches

The recommended switch settings for the front panel switch block are described below in Table 5-6.

Table 5-6. Front Panel Switch Descriptions

Switch Label	Switch Setting	Description
Disable A Port	OFF	When set to the OFF position, this switch enables Port A for communication with a host.
Disable B Port	OFF	When set to the OFF position, this switch enables Port B for communication with a host.
Write Protect	OFF	When set to the OFF position, the drive is enabled to perform writes.
Auto Spin Up	OFF	When set to the OFF position, the drive will spinup when the IPI-2 Spin Up function code is transferred from the host controller. When set to the ON position, the drive will start the drive motor when power is applied.

Front Panel LED Display

Three drive condition indicators, Busy, Ready, and Fault, are provided on the DD-301 front panel (refer to Figure 5-4).

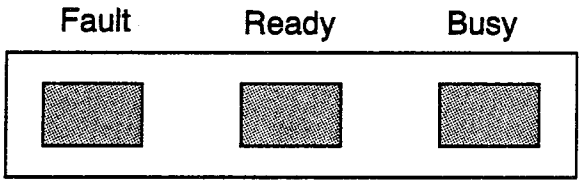


Figure 5-4. Front Panel LED Indicators

A brief description of the front panel LED indicators is shown in Table 5-7.

Table 5-7. Indicator LED Descriptions

LED label	Description
Fault	This indicator is activated asynchronously by the drive whenever an error is detected which causes a transition to a Not Ready condition.
Ready	This indicator is active whenever the drive is in a Ready condition.
Busy	This indicator is active when the drive is selected through either port or the drive has reserved the interface to perform an idle time function.

LED Sequencing During Power-up

During a power-up sequence, the drive proceeds through the following steps and LED indications:

1. All three LED indicators will light while the drive microprocessor executes a basic test sequence. If the basic test sequence fails, the drive hangs and all three indicators remain lit. The basic test sequence runs in less than 1 second.

2. When the basic test sequence completes, the Fault and Ready indicators are deactivated, the Busy indicator remains active until initialization is completed. If the Auto Start switch is ON, the drive will initiate a motor start and begin a spin-up sequence.

3. After the spindle reaches operating speed (either through an Auto Start or reception of a Spin-up command), a second test sequence is executed. The Busy LED remains active during this sequence. If the second test sequence fails, the Fault LED is activated while the Busy LED is deactivated. The drive will be spun up but Not Ready. If the second test sequence completes successfully, The Busy LED is deactivated while the Ready LED is activated. The Ready LED remains active whenever the drive is in a Ready condition.

Rear Panel

The rear of the DD-301 is comprised of a carrier interface receptacle. This receptacle provides all of the electrical connections to the drive when inserted into the DW-300 drawer. Refer to Figure 5-5 for a diagram of this receptacle. Table 5-8 describes the pin-out assignments of this receptacle.

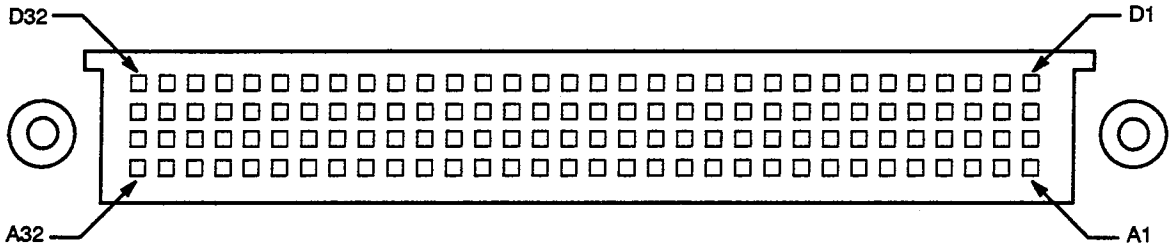


Figure 5-5. DD-301 Carrier Interface Receptacle

Table 5-8. Interface Connector Pin Assignments

Pin (+)	Pin (-)	Signal Name	Signal Source
D20	C20	Bus A Bit 0 (Port A)	Master(Slave)
D19	C19	Bus A Bit 1 (Port A)	Master(Slave)
A20	B20	Bus A Bit 2 (Port A)	Master(Slave)
D25	C25	Bus A Bit 3 (Port A)	Master(Slave)
D23	C23	Bus A Bit 4 (Port A)	Master(Slave)
D22	C22	Bus A Bit 5 (Port A)	Master(Slave)
A18	B18	Bus A Bit 6 (Port A)	Master(Slave)
A19	B19	Bus A Bit 7 (Port A)	Master(Slave)
D18	C18	Bus A Parity (Port A)	Master(Slave)
D16	C16	Bus B Bit 0 (Port A)	Slave(Master)
D15	C15	Bus B Bit 1 (Port A)	Slave(Master)
A16	B16	Bus B Bit 2 (Port A)	Slave(Master)
A22	B22	Bus B Bit 3 (Port A)	Slave(Master)
A23	B23	Bus B Bit 4 (Port A)	Slave(Master)
A25	B25	Bus B Bit 5 (Port A)	Slave(Master)
A14	B14	Bus B Bit 6 (Port A)	Slave(Master)
A15	B15	Bus B Bit 7 (Port A)	Slave(Master)

Table 5-8. Interface Connector Pin Assignments (continued)

Pin (+)	Pin (-)	Signal Name	Signal Source
D14	C14	Bus B Parity (Port A)	Slave(Master)
A17	B17	Attention In(Port A)	Slave
A24	B24	Sync Out (Port A)	Master
A21	B21	Slave In (Port A)	Slave
D17	C17	Sync In (Port A)	Slave
D21	C21	Master Out (Port A)	Master
D24	C24	Select Out (Port A)	Master
B07	A07	Bus A Bit 0 (Port B)	Master (Slave)
B06	A06	Bus A Bit 1 (Port B)	Master (Slave)
C08	D08	Bus A Bit 2 (Port B)	Master (Slave)
B12	A12	Bus A Bit 3 (Port B)	Master (Slave)
B10	A10	Bus A Bit 4 (Port B)	Master (Slave)
B09	A09	Bus A Bit 5 (Port B)	Master (Slave)
C06	D06	Bus A Bit 6 (Port B)	Master (Slave)
C07	D07	Bus A Bit 7 (Port B)	Master (Slave)
B05	A05	Bus A Parity (Port B)	Master (Slave)
B03	A03	Bus B Bit 0 (Port B)	Slave (Master)
B02	A02	Bus B Bit 1 (Port B)	Slave (Master)
C04	D04	Bus B Bit 2 (Port B)	Slave (Master)
C10	D10	Bus B Bit 3 (Port B)	Slave (Master)
C11	D11	Bus B Bit 4 (Port B)	Slave (Master)
C13	D13	Bus B Bit 5 (Port B)	Slave (Master)
C02	D02	Bus B Bit 6 (Port B)	Slave (Master)
C03	D03	Bus B Bit 7 (Port B)	Slave (Master)
B01	A01	Bus B Parity (Port B)	Slave (Master)
C05	D05	Attention In (Port B)	Slave
C12	D12	Sync Out (Port B)	Master
C09	D09	Slave In (Port B)	Slave
B04	A04	Sync In (Port B)	Slave
B08	A08	Master Out (Port B)	Master
B11	A11	Select Out (Port B)	Master
C01	D01	Group Select (Port B)	Master
A13	B13	Group Select (Port A)	Master

Table 5-8. Interface Connector Pin Assignments (continued)

Pin (+)	Pin (-)	Signal Name	Signal Source
D26	C26	Spindle Sync A	Bi-directional (enables via DW-300 backplane)
A26	B26	Spindle Sync B	Bi-directional (enables via DW-300 backplane)
D27		-Drive Address Bit 0	DW-300 Back Plane Jumper
C27		-Drive Address Bit 1	DW-300 Back Plane Jumper
B27		-Drive Address Bit 2	DW-300 Back Plane Jumper
A27		-Drive Address Parity	DW-300 Back Plane Jumper
B29		-Write Protect	Remote Switch (optional)
B28		Manufacturing Test Point	MFG Testers
A28		-Fault	IDM
C28		-Ready	IDM
D29		-Busy	IDM
D30		Disable Idle Functions	DW-300 Back Plane Jumper
A29		+12 V N/U	Drive Internal DC/DC Converter
A30		+12 V N/U	Drive Internal DC/DC Converter
A31		+36 V Source A	Power Supply Modules in DE-100 cabinet
A32		+36 V Source A	Power Supply Modules in DE-100 cabinet
C29		+5 V N/U	Drive Internal DC/DC Converter
C30		+5 V N/U	Drive Internal DC/DC Converter
C31		+36 V Source B	Power Supply Modules in DE-100 cabinet
C32		+36 V Source B	Power Supply Modules in DE-100 cabinet
B30		+DC/DC Enable	Power Supply Modules in DE-100 cabinet
D28		Ground	Power Supply Modules in DE-100 cabinet
D31		Ground	Power Supply Modules in DE-100 cabinet
D32		Ground	Power Supply Modules in DE-100 cabinet
B31		Ground	Power Supply Modules in DE-100 cabinet
B32		Ground	Power Supply Modules in DE-100 cabinet

Internal Components

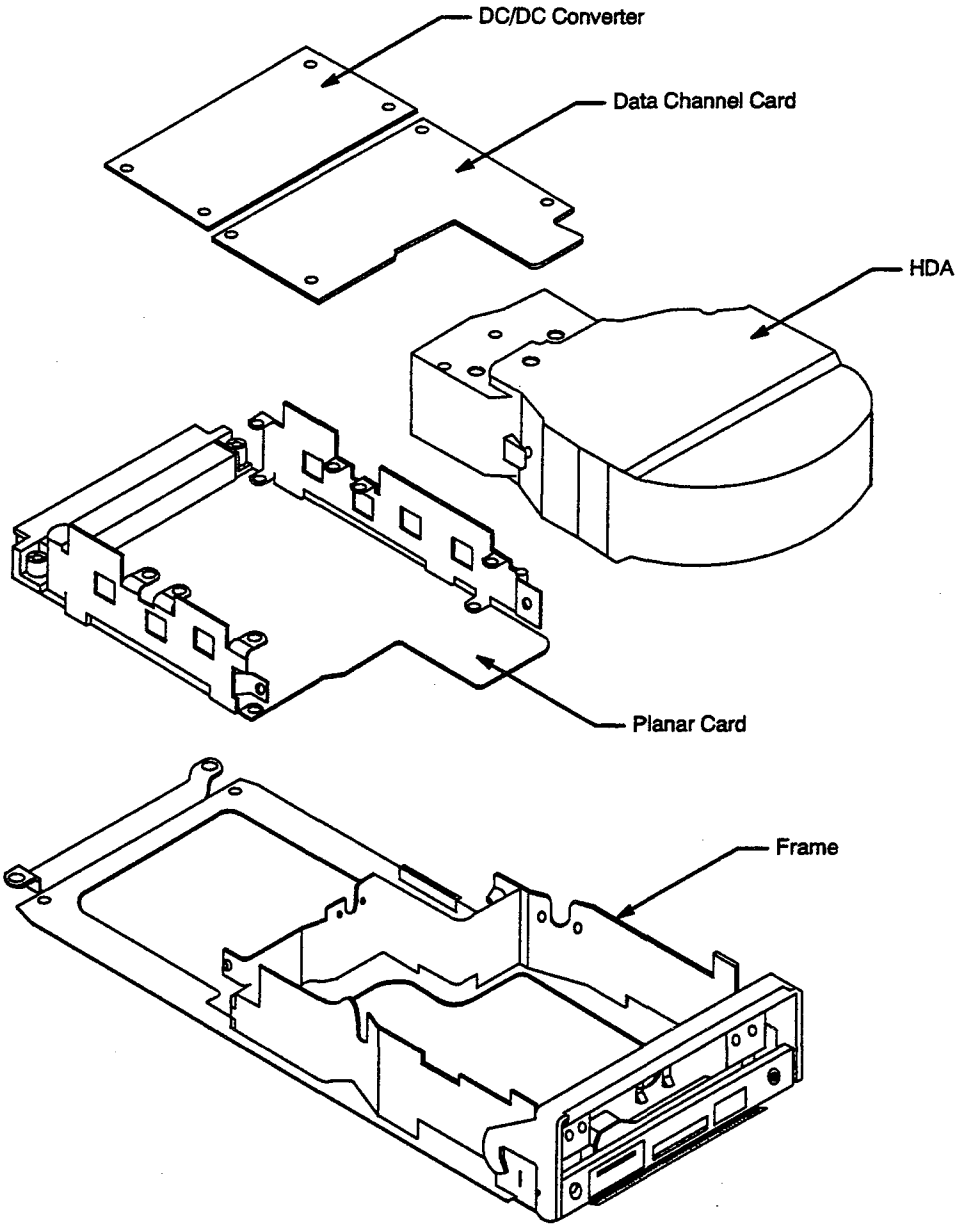


Figure 5-6. DD-301 Internal Component Locations

Circuit Boards

HDA Module

The DD-301 Head-Disk assembly (HDA) consists of platters, heads, actuator, and spindle motor (refer to Figure 5-7). The following subsection describes these components in more detail.

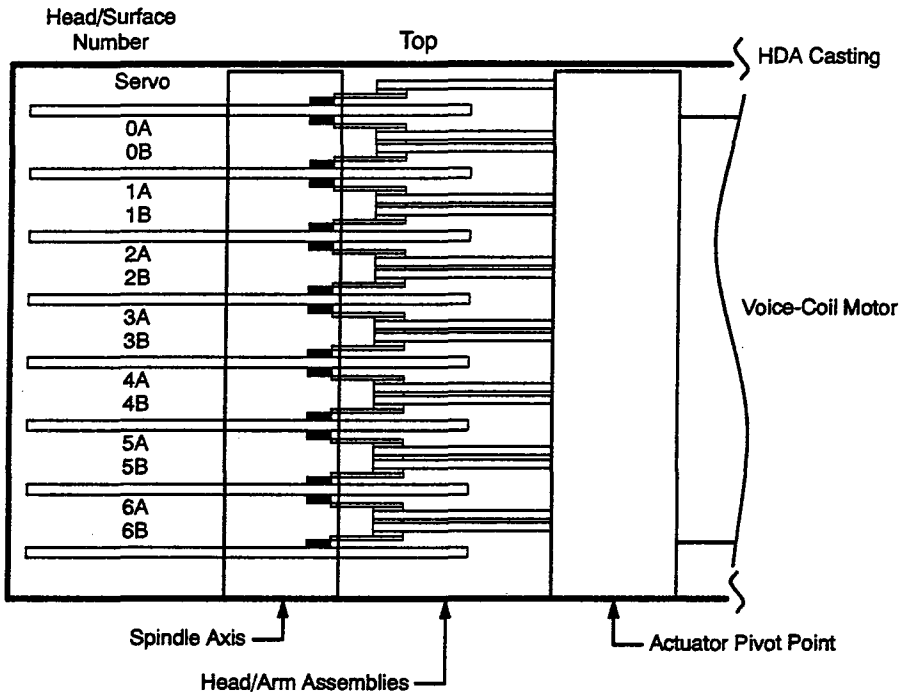


Figure 5-7. Cutaway of the DD-301 Head-Disk Assembly (HDA)

Platters

The DD-301 contains 8 physical disk platters used for storing information. These platters represent 14 recording surfaces for storing customer data, and a read-only surface containing servo information recorded at the factory.

Heads

There are 15 physical heads within the DD-301 HDA. One of these heads is used for reading servo information while the remaining 14 heads are accessed in A/B pairs (i.e. head groups) for writing and reading data. Refer again to Figure 5-7.

Actuator

The DD-301 HDA incorporates a rotary balanced actuator assembly with a monolithic comb to which the 14 data heads and 1 servo head are mounted.

Spindle and Motor

The DD-301 HDA incorporates an in-hub brushless DC spindle motor which is monitored and controlled by dedicated servo microprocessor unit (MPU) within the drive.

6 DD-301 FORMAT AND FLAW MANAGEMENT

This section covers the format specifications and flaw management properties of the DD-301, including flaw maps and tables.

Cylinder Mapping

The DD-301 has 1,930 cylinders, including data cylinders, diagnostic cylinders, and a flaw table cylinder. Table 6-1 shows the addresses of these cylinders in decimal and octal.

Table 6-1. DD-301 Cylinder Map

Description	Cylinder Addresses
Customer Data cylinders	0 - 1,921 (0 - 3601_8)
UNICOS spares area	1,922 - 1,924 (3602 - 3604_8)
Online CE (scratch) cylinders	1,925 - 1,926 (3605 - 3606_8)
Offline CE (scratch) cylinder	1,927 (3607_8)
Factory flaw table cylinder User flaw table cylinder	1,928 (3610_8) Even sectors 1,928 (3610_8) Odd sectors
Vendor defect list	1,929 (3611_8)
IPI diagnostic cylinder	1,930 (3612_8)
Thermal compensation reserve tracks	3613 - 3617

Data cylinders store system data. Do not write data patterns to these cylinders unless the customer data is offloaded to an alternate location.

The UNICOS spares area contains sectors assigned as alternates for unusable sectors in the customer data area.

The online CE area does not contain customer data and is the default testing area used by the online disk utility DDMS.

The offline CE cylinder does not contain customer data and is reserved for offline diagnostics.

The flaw table cylinder holds both factory and user flaw table data.

The IPI diagnostic cylinder is reserved for use by disk drive firmware. The DD-301 performs a write/read test on this cylinder during spin-up.

Sector Format

After receiving write data from a DCA-2 or DCA-3, each DD-301 stores the data in two physical sectors (one under each head in a 2-head group). Hardware striping of the data is done on byte boundaries, such that all even numbered bytes are stored under head 0 of a head group while the odd numbered bytes are stored under head 1 of a head group. Figure 6-1 shows the format of a physical sector under one head of a head group.

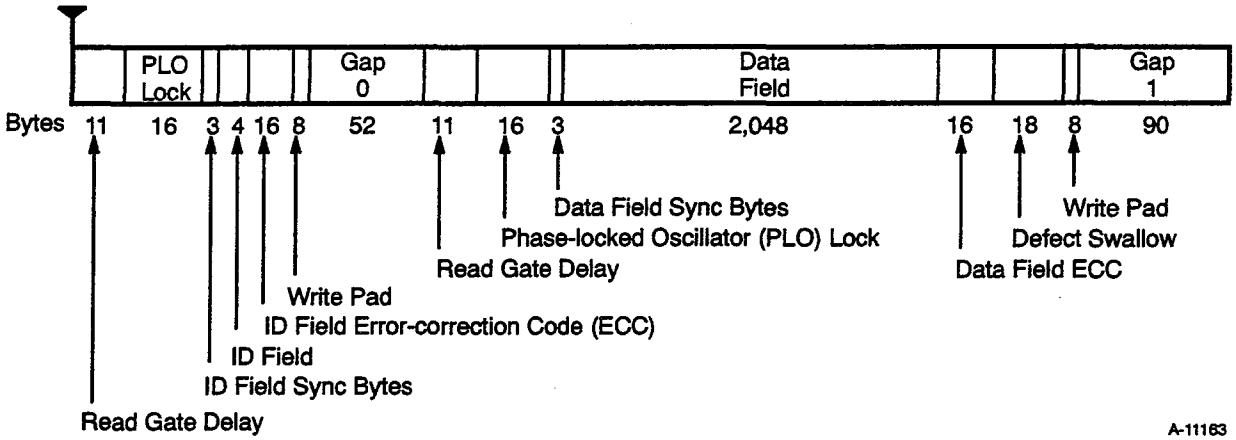


Figure 6-1. DD-301 Physical Sector Format (1/2 logical sector because logical sector contains both heads)

Each sector contains five field types: timing, ID, data, ECC, and defect swallow. Timing field sizes are identical under each physical head while the remaining fields are logically distributed between both heads of the head group. Table 6-2 shows the relation between the size of a physical field and the logical size of the combined information from both heads.

Table 6-2. DD-301 Sector Field Sizes

Sector Field	Physical Size in Bytes	Logical Size in Bytes
ID	4.0	8.0
ID field ECC	16.0	32.0
Data	2,048	4,096
Data field ECC	16.0	32.0
Defect swallow	18.0	36.0

Timing Fields

Timing fields within a sector include read gate delay, phase-locked oscillator (PLO) lock, sync bytes, write pad, gap 0, and gap 1. These fields allow time delays for synchronization of the timing circuits during read or write operations. For example, gap 0 provides a time delay for issuance, acceptance, and execution of the next command (a read or write data field).

Data Field

A physical data field contains 2,048 bytes of system data. The DD-301 divides the 4,096 bytes of write data received from the channel adapter between the 2 physical data fields.

ECC Fields

The ECC fields contain ECC generated by the channel adapter during a write data operation. Each physical sector contains 16 bytes of ECC for the ID field in that sector and 16 bytes of ECC for the data field in that sector. The channel adapter uses this information during read operations to detect data corruption, and calculate correction vectors for use by the host.

During a read data operation, the channel adapter reads the data or ID field and generates a new ECC for that field from each sector. The channel adapter then compares the new ECCs to the information read from the sector ECC fields. If the ID or data field ECCs do not match the generated ECCs, the channel adapter signals the EIOP that an ECC error occurred. If the error occurred in the data field, the channel adapter attempts to calculate vectors to be used for correction by the host.

Defect Swallow

The defect swallow (sometimes called a defect pad) allows small media defects to be hidden within a sector. Placement and detection of this defect swallow is controlled by the channel adapter by means of a defect address contained in the ID information. For more information on defect swallow and hideable flaws, refer to the "Media Flaws" subsection in this section.

ID Field

A DD-301 splits the 8 bytes of logical ID information between the 2 physical heads of a head group. The ID information contains the logical sector address and flaw information (refer to Figure 6-2). Table 6-3 describes each bit of the ID information.

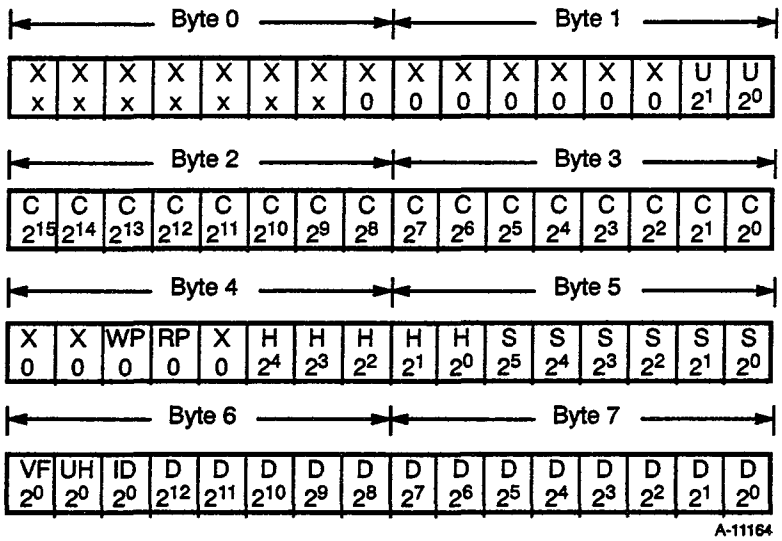


Figure 6-2. DD-301 Logical ID Information

Table 6-3. DD-301 ID Information Descriptions

Bit Symbol	Name	Description
X	Not used	This bit is not used.
U	Defective head	When set to 1, these bits indicate the physical head (head in head group) under which a known media flaw exists.
C	Cylinder address	These bits contain the cylinder address of the sector ($0 - 3610_8$).
H	Head address	These bits contain the logical head address (head group) of the sector ($0 - 6_8$).
S	Sector address	These bits contain the sector address of the data ($0 - 30_8$).
WP	Write protect (must be set to 0)	When set to 1, this bit indicates that data cannot be written to the sector unless this bit is also set in parameter register 1 (currently unsupported).
RP	Read protect (must be set to 0)	When set to 1, this bit indicates that data cannot be read from the sector unless this bit is also set in parameter register 1 (currently unsupported).
VF	Valid flaw	When set to 1, this bit indicates that the sector contains a known hideable flaw. The position of the defect pad used to hide the flaw is indicated by the defect parameter.
UH	Unhideable flaw	When set to 1, this bit indicates that the flaw in the sector is unhideable.
ID	ID field flaw	When set to 1, this bit indicates that the ID field contains an unhideable flaw.
D	Defect parameter	These bits contain the defect parameter. If the sector does not have a media flaw in the data field, the defect parameter is 1004_8.

The ID information is transferred between each disk drive and channel adapter in four 16-bit parcels using both bus A and bus B. For example, the first parcel transferred contains byte 0 and byte 1 of the logical ID information.

The entire logical ID information does not reside under an individual head in the head group. Each physical ID field contains 4 bytes of the information. Each even-numbered byte transferred is stored under head 0 of the head group. The odd-numbered bytes transferred are stored under head 1 of the head group.

During a write ID field operation, the DD-301 disk drives distribute the logical ID information to the 2 physical ID fields. After the 8 bytes of information are written to the disk drive, each physical ID field contains 4 bytes of the information. Bytes 0, 2, 4, and 6 are written under head 0 of the head group, and bytes 1, 3, 5, and 7 are written under head 1 of the head group. Figure 6-3 shows the ID fields for the 2 heads in a head group.

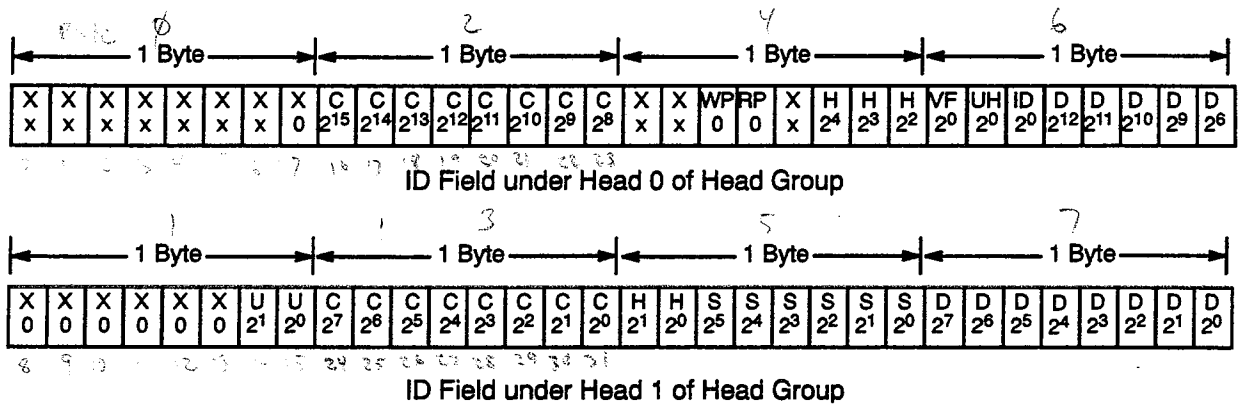


Figure 6-3. DD-301 Physical ID Fields

if flaw is longer than or equal to 32 bits, then it is unhidable

also, if 2 flaws are farther than 18 bytes apart, it is unhidable

D.P	VF	UH (EP)	ID	
623	1	0	0	= valid flaw
427	0	1	0	= unhidable flaw
735	0	1	1	= flaw in ID AND data field
1004	1	0	0	= flaw in defect param.
1004	0	0	0	= No flaw

Media Flaws

A media flaw is a defect on the surface of a platter that does not allow the disk drive to read or write information correctly. Flaws are grouped into two categories: hideable flaws and unhideable flaws.

Hideable Flaws

A hideable flaw is a media defect in the data field that can be effectively covered by a defect pad. The channel adapter creates this defect pad when it writes data to the disk drive, and effectively skips the defect pad when the data is read..

Hiding a Media Flaw

When a media defect is found during surface analysis or from an error report, the cylinder, head, and sector address of the flaw is identified along with a defect parameter. The defect parameter for a DD-301 represents the halfword (4-byte) boundary in the physical data field where the channel adapter starts to create an 18-byte defect pad.

Values for the defect parameter range from 0_8 to 1004_8 (0 to 516). The defect parameter, or location of the start of the defect pad, is calculated so that the 18-byte pad most effectively covers the media flaw. For example, if a media flaw is located at byte 50_8, the defect parameter for this flaw is 10_8 (refer to Figure 6-4).

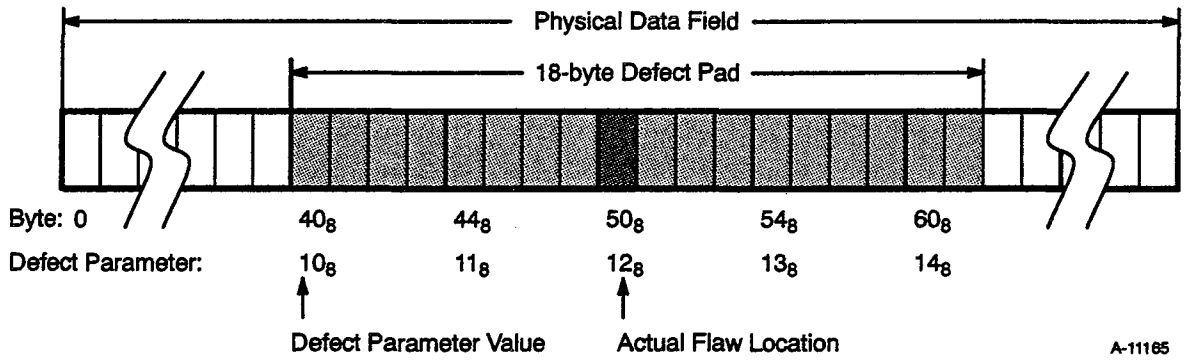


Figure 6-4. Defect Parameter and Actual Flaw Locations in a DD-301 Data Field

Before a write data field operation begins, the defect parameter is read from the sector ID field and transferred to a register in the channel adapter (refer again to Figure 3-1). The data parcel counter in the channel adapter is reset to 0.

The channel adapter uses a parcel counter to count each parcel of data as it is transferred to the disk drive. To count each 64-bit word (or 4 parcels) of data sent to the disk, the channel adapter disregards bits 2^0 and 2^1 of the parcel counter. Because the DD-301 uses 2 parallel heads to write data, one 64-bit word of data sent to the disk drive is equivalent to 32 bits (4 bytes) of data under each head of the head group.

When the value of the word count (from the parcel counter) is equivalent to the defect parameter, the channel adapter halts the parcel counter and starts decrementing a defect counter.

While the defect counter is decrementing, the channel adapter halts the transfer of customer data. Because the channel adapter halts the transfer of new data, it repeatedly transfers the previous parcel (for DCA-2) or next parcel (for DCA-3) of data to the disk drive. This continues until 18 repeated parcels of data have been transferred to the disk drive, resulting a an 18-byte defect pad under each of the 2 physical heads

By sending repeated parcels of data to each disk drive, the channel adapter creates a defect pad in the same location under each of the 2 parallel heads (refer to Figure 6-5).

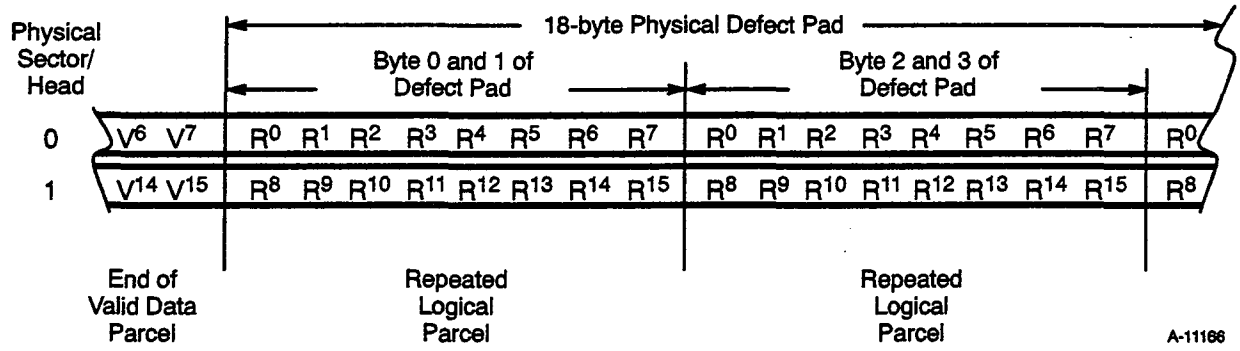


Figure 6-5. DD-301 Defect Pad Placement

After creating the defect pads, the channel adapter restarts the parcel counter and resumes the transfer of customer write data. This continues until all of the data and ECC for the logical sector is sent to the disk drive.

Sector Format with a Hideable Flaw

When a defect pad is inserted into a physical sector, the valid data following the defect pad is shifted by 18-bytes toward the end of the sector. Figure 6-6 shows the format of a physical sector (under one of the two parallel heads) with a hideable flaw.

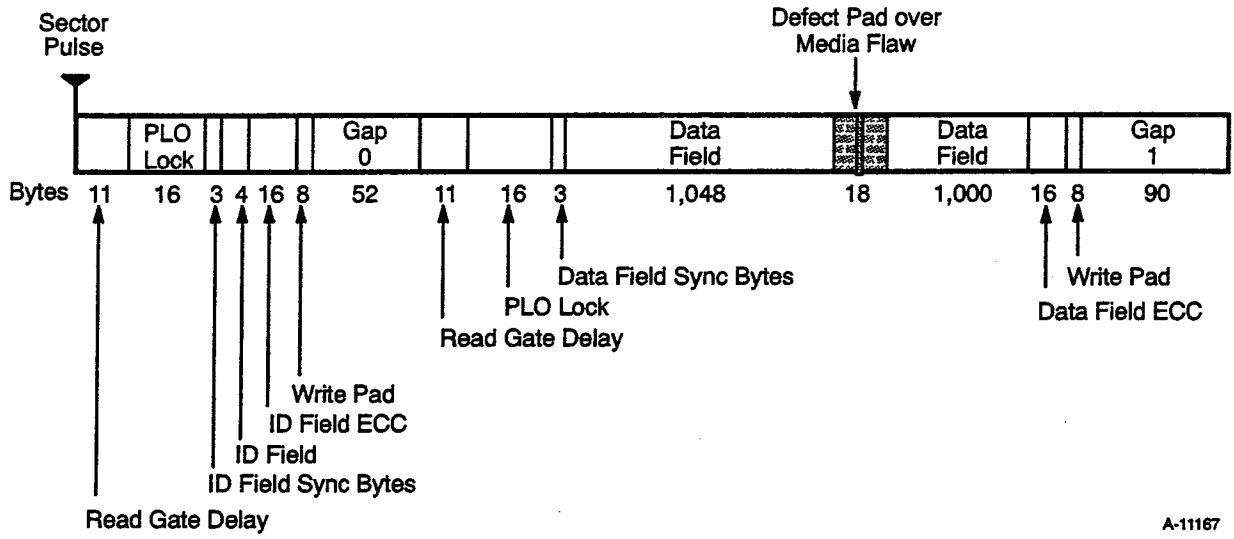


Figure 6-6. DD-301 Physical Sector with a Hideable Flaw

Hiding Multiple Media Flaws in One Logical Sector

Two flaws in the same sector under separate physical heads may still be hideable if the combined flaws can be effectively covered by a single defect pad. Figure 6-7 shows one defect pad covering two separate flaws.

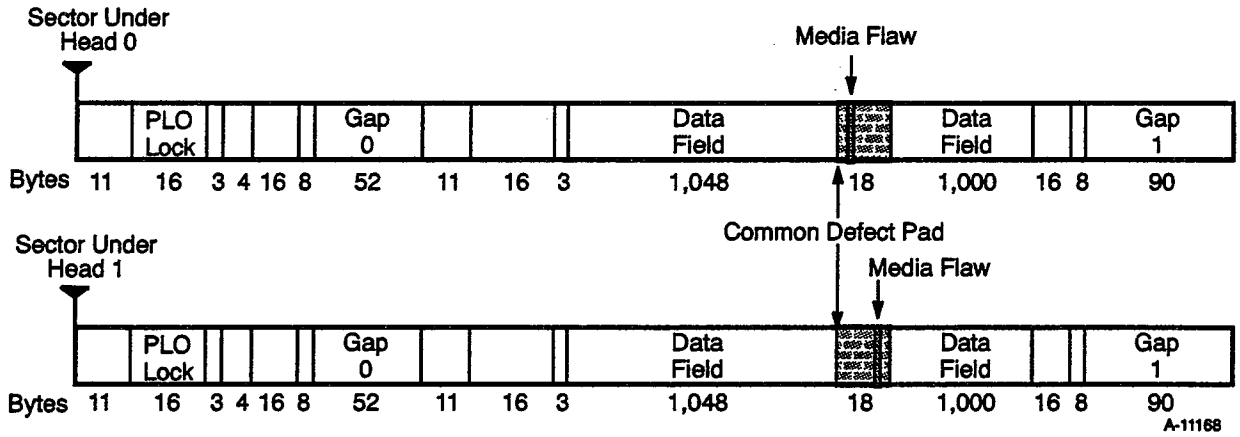


Figure 6-7. Two Physical Sectors with Hideable Flaws Covered by One Defect Pad

Reading a Sector with a Hideable Flaw

Before performing a read data field operation, the channel adapter reads the sector ID field and stores the defect parameter in a register. The channel adapter then resets the parcel counter (refer again to Figure 3-1).

The channel adapter uses the parcel counter to count each parcel of data as it is transferred from the disk drive. To count each 64-bit word (or 4 parcels) of data read from the disk drive, the channel adapter disregards bits 2^0 and 2^1 of the parcel counter. Because the DD-301 use 2 parallel heads to read data, one 64-bit word of data from the disk drive is equivalent to 32 bits of data from each physical data field.

When the value of the word count (from the parcel counter) is equivalent to the defect parameter, the channel adapter halts the parcel counter and starts decrementing a defect counter.

While the defect counter is decrementing, the channel adapter rejects the data parcels read from the defect pad area. This process continues until the defect pad data has transferred from the disk drive to the channel adapter.

After all of the repeated data is transferred, the channel adapter restarts the parcel counter and resumes the acceptance of data parcels from the disk drive. This process continues until the rest of the data field and ECC is transferred to the channel adapter.

Unhideable Flaws

An unhideable flaw is a media flaw that cannot be hidden by a defect pad. If an unhideable flaw occurs, the entire sector is unable to store data. Any sectors that contain an unhideable flaw are marked by the operating system as unusable sectors. The following list describes some of the conditions that create an unhideable flaw.

- A flaw exists in the first 8 bytes of the data field.
- A flaw exists outside of the data field of a sector (such as ID or sync byte fields).
- A flaw is longer than 32 bits.
- Two or more flaws exist under each head of the head group and the combined flaw cannot be covered by one defect pad.

Flaw Maps and Tables

Flaw maps and tables store the locations of media flaws in the DD-301. The maps and tables include a factory flaw map, a user flaw table, and a UNICOS flaw map.

Factory Flaw Table

The DD-301 drives contain a factory flaw table on the even-numbered sectors of cylinder ~~2,654~~ 1,928 (~~5136~~ 3610$_8$), under all heads. The factory flaw table lists the physical locations of all the flaws found during manufacturing checkout. This information is used when the DD-301 are initially formatted.

User Flaw Table

The user flaw table contains a list of all the flaws, hideable and unhideable, including those added since the disk drive was initially formatted. It is located on the odd-numbered sectors of cylinder ~~2,654~~ 1928 3610$_8$ (~~5136~~$_8$), under all heads. The user flaw table is updated whenever new flaws are added to the DD-301. Table 6-4 shows the format of the user flaw table.

Table 6-4. User Flaw Table Format

Word	Parcel	Description
0	0	Cray Research, Inc. serial number in ASCII (bits 2^{63} through 2^{48})
	1	Cray Research, Inc. serial number in ASCII (bits 2^{47} through 2^{32})
	2	Cray Research, Inc. serial number in ASCII (bits 2^{31} through 2^{16})
	3	Cray Research, Inc. serial number in ASCII (bits 2^{15} through 2^{0})
1	0	Not used
	1	Not used
	2	Not used
	3	Date of recording in hexadecimal (mm/yy) (latest time)
2 through last entry	0	Flaw ID field parcel 0 (refer to Figure 6-2)
	1	Flaw ID field parcel 1 (refer to Figure 6-2)
	2	Flaw ID field parcel 2 (refer to Figure 6-2)
	3	Flaw ID field parcel 3 (refer to Figure 6-2)
Terminator	0	All 1's
	1	All 1's
	2	All 1's
	3	All 1's

UNICOS Spares Map

The UNICOS flaw map is used by the operating system to locate sectors that contain unhideable flaws. If a sector is unusable, the operating system can remap the logical sector to another location in the DD-301. For DCA-3 applications, a sector which is unusable on one spindle will be marked by the operating system as unusable on all 5 array spindles and remapped to an alternate sector in the spares area of the drive.

NOTE: System flaw tables (sometimes referred as OS flaw tables or $EFTs) do not apply to the 300 series disk drives. Cylinder 0, which was previously used to store the system flaw table on IOS Model D drives, is a customer data cylinder on IOS Model E drives.

134158-1

7 IPI-2 Interface Signals

IPI-2 interface signals transfer information between the channel adapter and the 300 series disk drives. The 24 signals consist of control, attention in, and data signals. Figure 7-1 shows the signals in an IPI-2 interface.

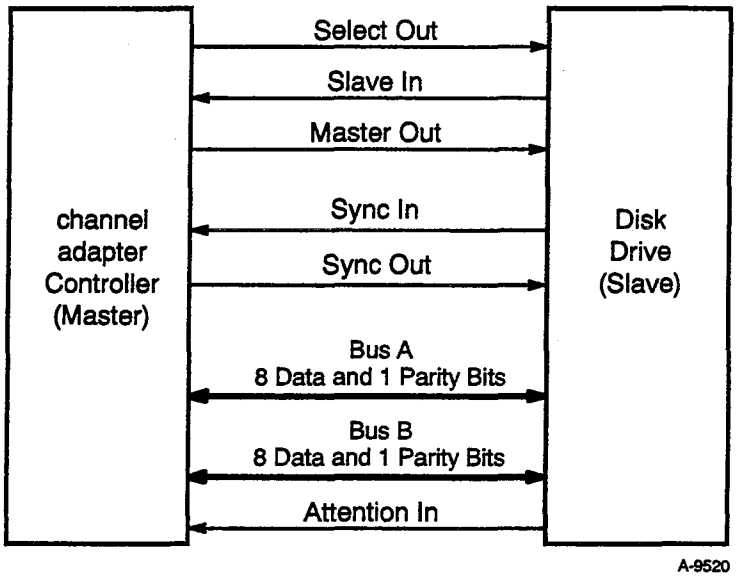


Figure 7-1. IPI-2 Interface Signals

Control Signals

Five signals control disk drive operations. These signals are Select Out, Slave in, Master Out, Sync In, and Sync Out.

Select Out

The channel adapter sends the Select Out signal to select a disk drive for use by the channel. Initially, when the Select Out signal is set, the requested disk drive address is transferred on bus A. The Select Out signal remains set until the controller releases the disk drive from the channel.

Slave In

The disk drive sends the Slave In signal in response to a Select Out signal or a Master Out signal from the channel adapter. During a select operation, the disk drive responds to the Select Out signal with the Slave In signal in order to acknowledge channel reservation. During a reset operation, the disk drive responds to the Master Out signal with the Slave In signal in order to acknowledge the reset operation.

Master Out

The channel adapter sends the Master Out signal during a data transfer or disk drive reset. To initiate a data transfer, the channel adapter sets the Master Out signal after loading bus A and bus B with data. To initiate a disk drive reset, the channel adapter sets the Master Out signal after loading bus A with a reset parameter.

Sync In

The disk drive sends the Sync In signal during a data transfer or bus control operation. During read or write operations, the disk drive sets the Sync In signal to acknowledge the data transfer. For a read operation, the Sync In signal indicates valid data on the bus lines. For a write operation, the Sync In signal indicates that the disk drive is ready to accept data over the bus lines. During a bus control operation, the disk drive sets the Sync In signal to indicate acceptance of the bus control parameter.

Sync Out

The channel adapter sends the Sync Out signal during a data transfer or bus control operation. During a read or write operation, the channel adapter sets the Sync Out signal to acknowledge the data transfer. For a read operation, the Sync Out signal indicates the data on the bus lines was received. For a write operation, the Sync Out signal indicates valid data on the bus lines. During a bus control operation, the channel adapter sets the Sync Out signal after loading bus A with the bus control parameter.

Attention In Signal

The disk drive uses the Attention In signal to inform the channel adapter that service is required. The disk drive sets the Attention In signal if any of the following interrupts occur:

- Rotational position sensing (RPS) interrupt

- Command completion interrupt
- Status pending interrupt
- No longer busy interrupt

Data Signals

All information transfers between the channel adapter and disk drive occur over bus A and bus B. Each bus carries nine signals. Eight of the signals are data bits and one signal is an odd parity bit.

Bus A

The channel adapter uses bus A to transfer command parameters to the disk drive. Refer to the "IPI-2 Interface States" subsection in this section for more information on disk drive operations.

Bus B

The disk drive uses bus B to transfer command responses to the channel adapter. Refer to the "IPI-2 Interface States" subsection in this section for more information on disk drive operations.

Bus A and Bus B

During write operations, the channel adapter uses bus A and bus B to transfer 18 bits of information to the disk drive. During read operations, the disk drive uses bus A and bus B to transfer 18 bits of information to the channel adapter. Refer to the "IPI-2 Interface States" subsection in this section for more information on disk drive operations.

IPI-2 Interface States

An IPI-2 interface state occurs when all control signals on the IPI-2 interface have a stable logical value. For example, the BUS CONTROL state has the Select Out signal set to 1, the Slave In signal set to 1, the Master Out signal set to 0, the Sync In signal set to 0, and the Sync Out signal set to 1 (refer to Figure 7-2).

Figure 7-2 shows all IPI-2 states. The arrows indicate which states are accessible from the other states. For example, the SLAVE ACKNOWLEDGE state can change into the DESELECT, BUS CONTROL, or TRANSFER READY state.

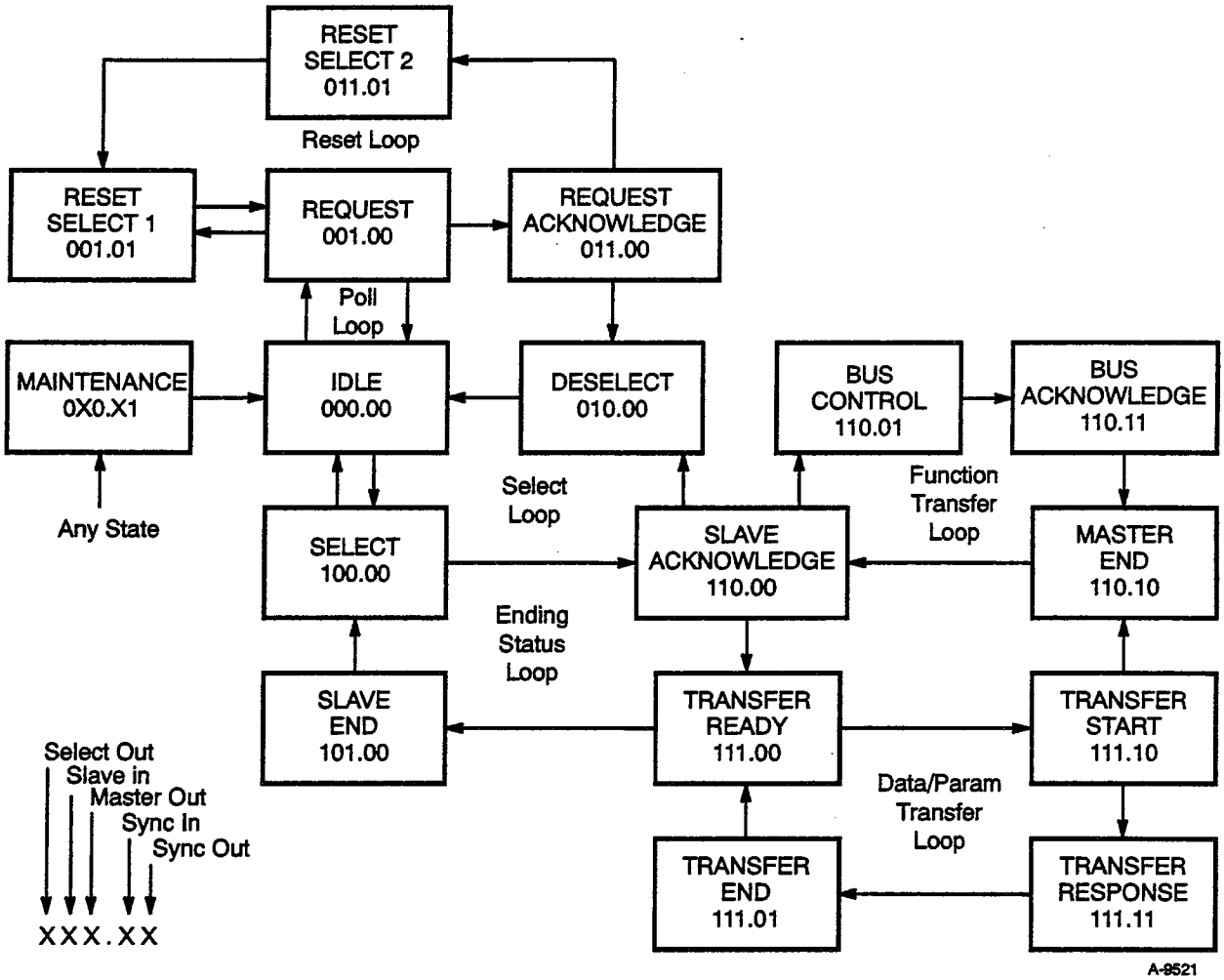


Figure 7-2. IPI-2 Interface States

During normal operation, the IPI-2 interface changes state when one signal changes logical value. For example, to change from the BUS CONTROL state to the BUS ACKNOWLEDGE state, only the Sync In signal changes from 0 to 1 (refer again to Figure 7-2).

All communication between the channel adapter and disk drive follows a call-and-response sequence through the IPI-2 states. For example, when the interface is in the IDLE state, the channel adapter sets the Select Out signal to 1, which puts the interface in the SELECT state. In response, the disk drive sets the Slave In signal to 1, which puts the interface into the SLAVE ACKNOWLEDGE state.

Each disk drive operation follows a sequence through the IPI-2 states. The sequencer on the channel adapter controls the IPI-2 signals, which determine the order of the sequence. At the appropriate time in a sequence, the sequencer loads bus A and bus B with information and transfers it to the disk drive.

IPI-2 Interface State Sequences

An IPI-2 interface state sequence is a set path through the IPI-2 interface states that the sequencer controls. During the sequence, the channel adapter and disk drive exchange information needed for disk drive operations. The sequences for disk drive operations are:

- Select disk drive
- Bus control
- Interlocked transfer to disk
- Interlocked transfer from disk
- Noninterlocked transfer to disk
- Noninterlocked transfer from disk
- Ending status
- Deselect
- Interrupt request (poll)
- Reset disk drive
- Master reset
- Transfer settings request
- Drive interrupt request

Each sequence determines what information the sequencer or disk drive must place on bus A or bus B. Table 7-1 lists the contents of bus A and bus B for all of the IPI-2 interface state sequences.

The following subsections describe each of the disk drive operation sequences in detail.

Table 7-1. Bus A and Bus B Contents for Each IPI Bus State Sequence

Sequence	Bus A								Bus B							
	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Select disk drive	0	Disk drive address Bit 2^4 is the least significant bit			0	0	0	Priority select	Disk drive 7	Disk drive 6	Disk drive 5	Disk drive 4	Disk drive 3	Disk drive 2	Disk drive 1	Disk drive 0
Bus control	Transfer control or data	Transfer out or in	0	Advance head	Bus control parameter				Bus B is not defined so each bit is set to 0							
Interlocked transfer-to-disk	IPI command parameters from the EIOP local memory to the disk drive								IPI command parameters from the EIOP local memory to the disk drive							
Interlocked transfer-from-disk	IPI status from the disk drive to the DCA2								IPI status from the disk drive to the DCA2							
Noninterlocked transfer-to-disk	Write data from the EIOP buffer board to the disk drive								Write data from the EIOP buffer board to the disk drive							
Noninterlocked transfer-from-disk	Read data from the disk drive to the EIOP buffer board								Read data from the disk drive to the EIOP buffer board							
Ending status	Good transfer	Bus parity error	0	0	0	0	0	0	Good transfer	Bus parity error	Odd byte transfer	Time dependent operation	Final status after operation			
Deselect	Bus A is not defined during a deselect sequence								Bus B is not defined during a deselect sequence							
Interrupt request (Poll)	0	Report busy status	Report ready status	Slave power failure alert	Power on status request	Report status pending interrupt	Report RPS interrupt	Report command complete interrupt	Disk drive 7	Disk drive 6	Disk drive 5	Disk drive 4	Disk drive 3	Disk drive 2	Disk drive 1	Disk drive 0
Reset disk drive	1	Disk drive address Bit 2^4 is the least significant bit			Disable interface drivers	Reset disk drive	Reset logical interface	Reset physical interface	Bus B is not defined during a reset disk drive sequence							
Master reset	Data out 2	Not used	Not used	Data out 1	Not used	Not used	Data out 0	Not used	Bus B is not defined during a master reset sequence							
Transfer settings request	1	Disk drive address Bit 2^4 is the least significant bit			0	0	0	0	0	0	1	0	0	1	1	0
Drive interrupts request	1	Disk drive address Bit 2^4 is the least significant bit			1	0	0	0	0	Busy status	Ready status	0	Priority select status	Status pending interrupt active	RPS interrupt active	Command complete interrupt

Select Disk Drive Sequence

The select disk drive sequence logically connects the channel adapter to a disk drive. Figure 7-3 shows a select disk drive sequence.

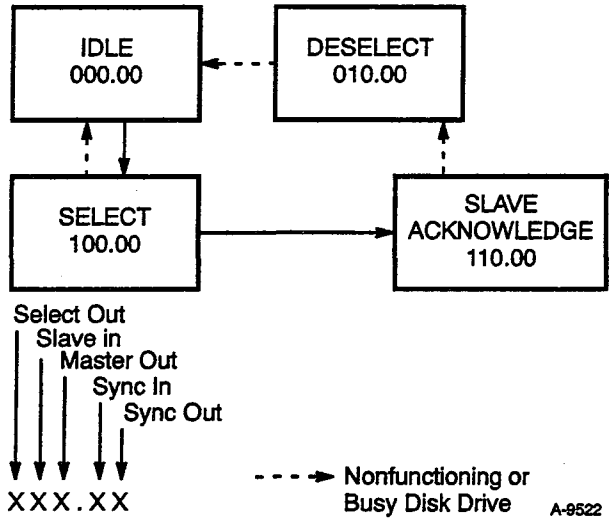


Figure 7-3. Select Disk Drive Sequence

Before a select disk drive sequence begins, a register in the channel adapter must be loaded with the disk drive address (refer to Table 7-2).

Normal Selection

If no errors occur during the select disk drive sequence, a normal selection sequence occurs. The following sequence describes a normal selection sequence.

1.. While the IPI-2 interface is in the IDLE state, the sequencer transfers the disk drive address from the *j* register in the channel adapter to bus A (refer to Table 7-2).

Table 7-2. Disk Drive Address on Bus A

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
0	Disk drive address Bit 2^4 is the least significant bit			0	0	0	Priority select

2.. The sequencer sets the Select Out signal to 1, which puts the IPI-2 interface in the SELECT state.

3.. The disk drive loads bus B with the drive select response and sets the Slave In signal equal to 1 (refer to Table 7-3), which puts the interface in the SLAVE ACKNOWLEDGE state and completes the select disk drive sequence.

Table 7-3. Drive Select Response on Bus B

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Disk drive 7	Disk drive 6	Disk drive 5	Disk drive 4	Disk drive 3	Disk drive 2	Disk drive 1	Disk drive 0

Busy Drive Selection

The following sequence describes a busy disk drive selection sequence.

1.. While the IPI-2 interface is in the IDLE state, the sequencer transfers the disk drive address (refer to Table 7-2) from the *j* register in the channel adapter to bus A.

2.. The sequencer sets the Select Out signal to 1, which puts the IPI-2 interface in the SELECT state.

3.. If the requested disk drive is functioning normally, but cannot perform bus exchanges or information transfers, the disk drive sets the Slave In signal equal to 1 but does not load bus B with the select response. As a result, the interface is put in the SLAVE ACKNOWLEDGE state.

4.. The sequencer resets the Select Out signal to 0 to enter the DESELECT state. The disk drive resets the Slave In signal to 0 to return the interface to the IDLE state.

Nonfunctioning Drive Selection

The following sequence describes a nonfunctioning disk drive selection sequence.

1.. While the IPI-2 interface is in the IDLE state, the sequencer transfers the disk drive address from the *j* register in the channel adapter to bus A (refer to Table 7-2).

2.. The sequencer sets the Select Out signal to 1, which puts the IPI-2 interface in the SELECT state.

3.. If the requested disk drive does not set the Slave In signal within a given time limit, the sequencer resets the Select Out signal to 0 and returns the interface to the IDLE state.

Bus Control Sequence

The bus control sequence transfers IPI-2 commands from the channel adapter to the disk drive. Figure 7-4 shows a bus control sequence.

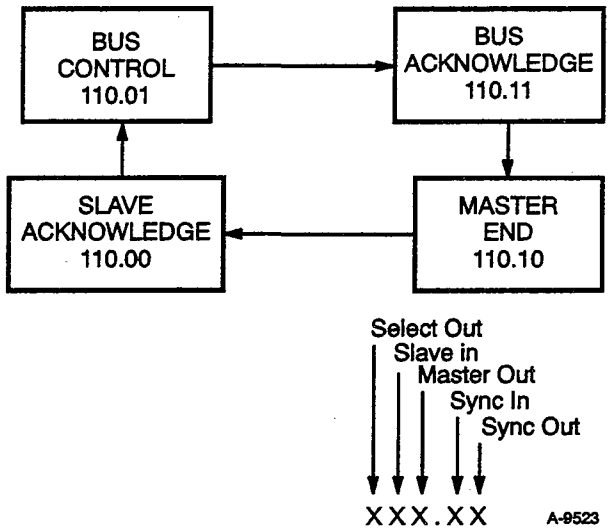


Figure 7-4. Bus Control Sequence

Before a bus control sequence begins, the *j* and *k* registers in the channel adapter must be loaded with bus control commands (refer to Table 7-4).

1.. While the IPI-2 interface is in the SLAVE ACKNOWLEDGE state, the sequencer transfers a bus control command from the *j* or *k* register in the channel adapter to bus A (refer to Table 7-4).

Table 7-4. Bus Control Command on Bus A

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Transfer control or data	Transfer out or in	0	Advance head	Bus control parameter			

Table 7-5 shows some examples of bus control commands used by Cray Research, Inc. (CRI).

Table 7-5. Sample Bus Control Commands Used by CRI

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Description
0	0	0	0	0	1	0	0	Load cylinder address
0	0	0	0	0	1	0	1	Load head address
0	0	0	0	0	1	1	0	Load rotational positional sensing (RPS) target sector
0	0	0	0	0	1	1	1	Load position
1	1	0	0	1	0	0	0	Read header
1	1	0	0	1	1	0	0	Read header at target
1	1	0	0	0	0	0	1	Read field
1	0	0	0	0	0	0	1	Write field
1	0	0	0	1	1	0	0	Write header at target

2.. The sequencer sets the Sync Out signal to 1, which puts the interface into the BUS CONTROL state.

3.. The disk drive loads bus B with the bus control response (refer to Table 7-6) and sets the Sync In signal to 1, which puts the interface into the BUS ACKNOWLEDGE state.

Table 7-6. Bus Control Response on Bus B

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Bus B is not defined, so each bit is set to 0							

4.. The sequencer resets the Sync Out signal to 0, which puts the interface in the MASTER END state. Bus A is not loaded with any information.

5.. The disk drive resets the Sync In signal to 0. This puts the interface in the SLAVE ACKNOWLEDGE state and completes a bus control sequence. Bus B is not loaded with any information.

Interlocked Transfer-to-disk Sequence

The interlocked transfer-to-disk sequence is used to transfer IPI command parameters from the EIOP local memory to the disk drive. Figure 7-5 shows an interlocked transfer-to-disk sequence.

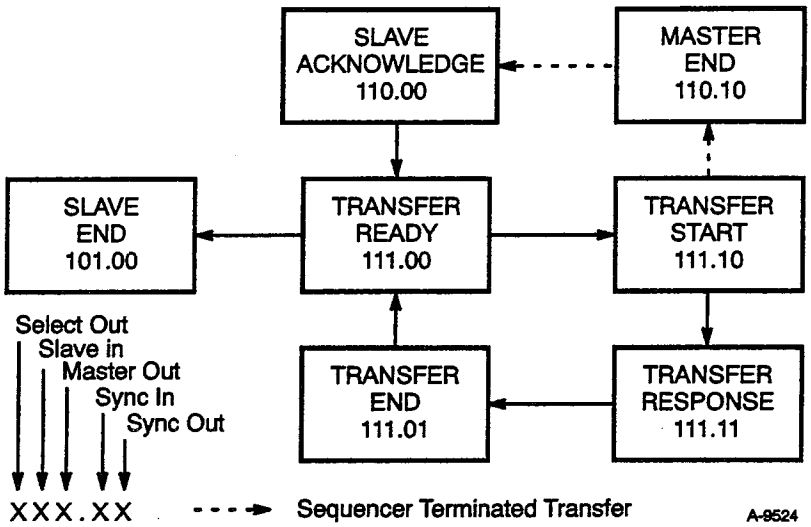


Figure 7-5. Interlocked Transfer-to-disk Sequence

Before starting an interlocked transfer-to-disk sequence, the sequencer must have successfully completed a bus control sequence.

Drive-terminated Transfer

If an interlocked transfer-to-disk sequence completes successfully, the disk drive terminates the transfer as shown in the following sequence.

1.. While the IPI-2 interface is in the SLAVE ACKNOWLEDGE state, the sequencer sets the Master Out signal to 1. Doing so puts the interface in the TRANSFER READY state and signals the disk drive that an information transfer is about to begin.

2.. The disk drive sets the Sync In signal to 1, which puts the interface in the TRANSFER START state and signals the controller that the disk drive is ready to receive information.

3.. The sequencer transfers one parcel of the command parameter from EIOP local memory to bus A and bus B and sets the Sync Out signal to 1, which puts the interface in the TRANSFER RESPONSE state.

4.. The disk drive resets the Sync In signal to 0 to acknowledge that it received the parcel of information, which puts the interface in the TRANSFER END state.

5.. The sequencer resets the Sync Out signal to 0 to acknowledge the transfer of 1 parcel of information to the disk drive. This puts the interface in the TRANSFER READY state.

If there is more than 1 parcel of information to be transferred to the disk drive, the sequencer repeats Steps 2 through 5 until all of the parcels are transferred from local memory to the disk drive.

6.. The disk drive resets the Slave In signal to 0 to end the interlocked transfer, which puts the interface in the SLAVE END state.

Sequencer-terminated Transfer

If an error occurs during an interlocked transfer to disk sequence, the sequencer terminates the transfer as shown in the following sequence.

1.. At some point in the transfer, the disk drive sets the Sync In signal to 1, which puts the interface into the TRANSFER START state and signals the controller that the disk drive is ready to receive information.

2.. While the IPI-2 interface is in the TRANSFER START state, the sequencer resets the Master Out signal to 0 to terminate the interlocked transfer, which puts the interface in the MASTER END state.

3.. The disk drive resets the Sync In signal to 0 to acknowledge the termination, which puts the interface in the SLAVE ACKNOWLEDGE state.

4.. The sequencer sets the Master Out signal to 1 to put the interface in the TRANSFER READY state.

5.. The disk drive resets the Slave In signal to 0 to exit the transfer loop, which puts the interface in the SLAVE END state.

Interlocked Transfer-from-disk Sequence

The interlocked transfer-from-disk sequence is used to transfer IPI-2 status information from the disk drive to the EIOP local memory. Figure 7-6 shows an interlocked transfer-from-disk sequence.

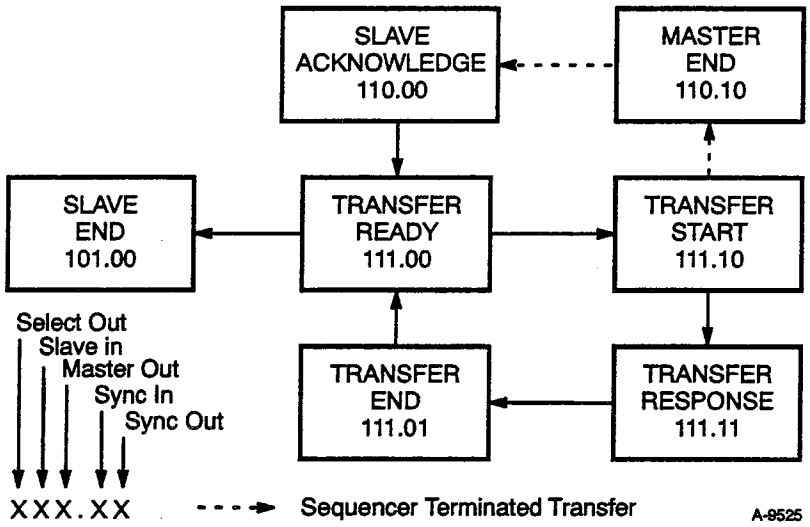


Figure 7-6. Interlocked Transfer-from-disk Sequence

Before starting an interlocked transfer-from-disk sequence, the sequencer must have successfully completed a bus control sequence.

Drive-terminated Transfer

If an interlocked transfer-from-disk sequence completes successfully, the disk drive terminates the transfer as shown in the following sequence.

1.. While the IPI-2 interface is in the SLAVE ACKNOWLEDGE state, the sequencer sets the Master Out signal to 1. Doing so puts the interface in the TRANSFER READY state and signals the disk drive that an information transfer is about to begin.

2.. The disk drive loads bus A and bus B with information and sets the Sync In signal to 1. Doing so puts the interface in the TRANSFER START state.

3.. The sequencer receives the data and sets the Sync Out signal to 1. Doing so puts the interface in the TRANSFER RESPONSE state.

4.. The disk drive resets the Sync In signal to 0 to acknowledge that the channel adapter received a parcel of data. Doing so puts the interface in the TRANSFER END state.

5.. The sequencer resets the Sync Out signal to 0 to acknowledge that the transfer of 1 parcel of information from the disk drive. Doing so puts the interface in the TRANSFER READY state.

If there is more than 1 parcel of information to be transferred from the disk drive, the sequencer repeats Steps 2 through 5 until all of the parcels are transferred from the disk drive.

6.. The disk drive resets the Slave In signal to 0 to terminate the interlocked transfer, which puts the interface in the SLAVE END state.

Sequencer-terminated Transfer

If an error occurs during an interlocked transfer from disk sequence, the sequencer terminates the transfer as shown in the following sequence.

1.. At some point in the transfer, the disk drive sets the Sync In signal to 1, which puts the interface in the TRANSFER START state and signals the controller that the disk drive is ready to receive information.

2.. While in the TRANSFER START state, the sequencer resets the Master Out signal to 0 to terminate the interlocked transfer. Doing so puts the interface in the MASTER END state.

3.. The disk drive resets the Sync In signal to 0 to acknowledge the termination. Doing so puts the interface in the SLAVE ACKNOWLEDGE state.

4.. The sequencer sets the Master Out signal to 1 to put the interface in the TRANSFER READY state.

5.. The disk drive resets the Slave In signal to 0 to exit the transfer loop. Doing so puts the interface in the SLAVE END state.

Noninterlocked Transfer-to-disk Sequence

The noninterlocked transfer-to-disk sequence is used to transfer data from the EIOP buffer board to the disk drive media. Figure 7-7 shows a noninterlocked transfer-to-disk sequence.

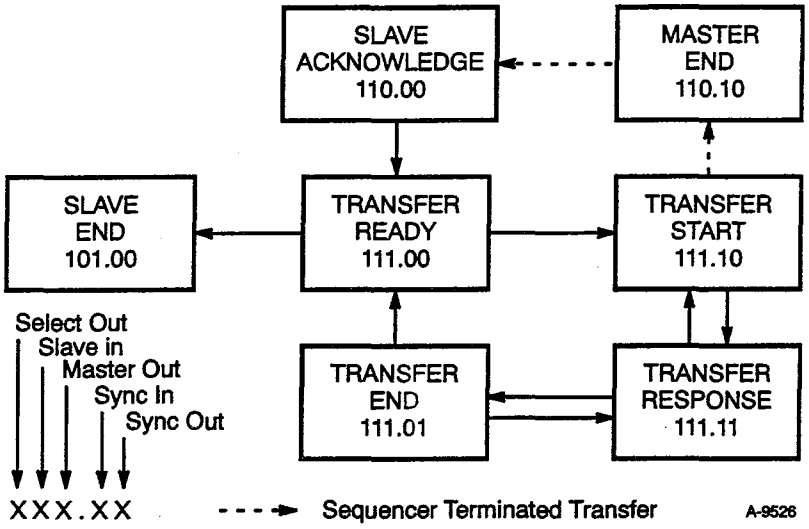


Figure 7-7. Noninterlocked Transfer-to-disk Sequence

Before starting a noninterlocked transfer-to-disk sequence, the sequencer must have successfully completed a bus control sequence.

Drive-terminated Transfer

If a noninterlocked data transfer-to-disk sequence completes successfully, the disk drive terminates the transfer as shown in the following sequence.

1.. While the IPI-2 interface is in the SLAVE ACKNOWLEDGE state, the sequencer sets the Master Out signal to 1. Doing so puts the interface in the TRANSFER READY state and signals the disk drive that an information transfer is about to begin.

2.. The disk drive and sequencer enter the noninterlocked transfer mode. In the noninterlocked mode, the interface does not follow a set sequence through the IPI bus states. All information transfers between the channel adapter and disk drive media occur in noninterlocked mode.

The disk drive sets and resets the Sync In signal to create a pulse. After acknowledging the pulse, the sequencer transfers a parcel from the EIOP buffer board to bus A and bus B and sets the Sync Out signal to 1.

Every pulse of the Sync In signal created by the disk drive must be answered with a pulse of the Sync Out signal from the sequencer. Each Sync Out signal pulse sends a parcel of information over bus A and bus B. The pulses continue until all of the information has been transferred to the disk drive.

3.. After the disk drive sends a number of Sync In signal pulses to the sequencer, the disk drive must receive an equal number of Sync Out signals from the sequencer. When this occurs, the disk drive resets the Slave In signal to 0 and terminates the information transfer. Doing so puts the interface in the SLAVE END state.

Sequencer-terminated Transfer

If an error occurs during a noninterlocked data transfer to disk sequence, the sequencer terminates the transfer as shown in the following sequence.

1.. While the IPI-2 interface is in the SLAVE ACKNOWLEDGE state, the sequencer sets the Master Out signal to 1. Doing so puts the interface in the TRANSFER READY state and signals the disk drive that an information transfer is about to begin.

2.. The disk drive and sequencer enter the noninterlocked transfer mode. The disk drive sets and resets the Sync In signal to create a pulse. After acknowledging the pulse, the sequencer transfers a parcel of information from the EIOP buffer board to bus A and bus B and sets the Sync Out signal to 1.

Every Sync In signal pulse created by the disk drive must be answered with a Sync Out signal pulse by the sequencer. Each Sync Out signal pulse sends a parcel of information out on bus A and bus B.

3.. To terminate the data transfer, the sequencer replaces one of the Sync Out signal pulses with a Master Out signal pulse. After sending the Master Out signal pulse, the sequencer stops transferring information to bus A and bus B.

4.. Again, the disk drive must receive the same number of Sync Out signal pulses (including the one Master Out signal pulse) as Sync In signal pulses it sent to the sequencer. When this occurs, the disk drive resets the Slave In signal to 0 and terminates the information transfer. Doing so puts the interface in the SLAVE END state.

Noninterlocked Transfer-from-disk Sequence

The noninterlocked transfer-from-disk sequence is used to transfer data from the disk drive to the EIOP buffer board. Figure 7-8 shows a noninterlocked transfer-from-disk sequence.

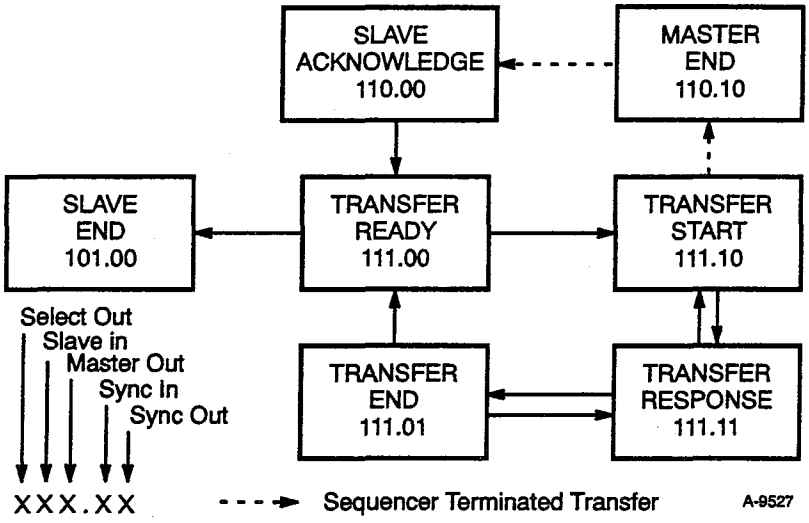


Figure 7-8. Noninterlocked Transfer-from-disk Sequence

Before starting a noninterlocked transfer-from-disk sequence, the sequencer must have successfully completed a bus control sequence.

Drive-terminated Transfer

If an information transfer from disk completes successfully, the disk drive terminates the transfer as shown in the following sequence.

1.. While the IPI-2 interface is in the SLAVE ACKNOWLEDGE state, the sequencer sets the Master Out signal to 1. Doing so puts the interface in the TRANSFER READY state and signals the disk drive that an information transfer is about to begin.

2.. The disk drive and sequencer enter the noninterlocked transfer mode. The noninterlocked mode is a condition where the interface does not follow a set sequence through the IPI-2 bus states. All information transfers between the channel adapter and disk drive media occur in noninterlocked mode.

The disk drive loads a parcel of information on bus A and bus B and sets the Sync In signal to 1. The disk drive then resets the Sync In signal to 0 to create a pulse. Each pulse sends a parcel of information on bus A and bus B.

3.. After receiving the first parcel of information, the sequencer transfers the parcel to the EIOP buffer board and generates a Sync Out signal pulse. Every Sync In signal pulse created by the disk drive must be answered by a Sync Out signal pulse from the sequencer; however, the disk drive does not have to wait for a Sync Out signal pulse before sending another parcel of information.

4.. After sending all parcels of information, the disk drive must receive the same number of Sync Out signal pulses from the sequencer as Sync In signal pulses it sent to the sequencer. When this occurs, the disk drive resets the Slave In signal to 0 and terminates the information transfer. Doing so puts the interface into the SLAVE END state.

Sequencer-terminated Transfer

If an error occurs during an information transfer-from-disk sequence, the sequencer terminates the transfer as shown in the following sequence.

1.. While the IPI-2 interface is in the SLAVE ACKNOWLEDGE state, the sequencer sets the Master Out signal to 1. Doing so puts the interface into the TRANSFER READY state and signals the disk drive that an information transfer is about to begin.

2.. The disk drive and sequencer enter the noninterlocked transfer mode. The disk drive loads a parcel of information on bus A and bus B and sets the Sync In signal to 1. The disk drive then resets the Sync In signal to 0 to create a pulse. Each pulse sends a parcel of information on bus A and bus B. Every Sync In signal pulse must be answered by a Sync Out signal pulse from the sequencer.

3.. To terminate the data transfer, the sequencer replaces one of the Sync Out signal pulses with a Master Out signal. After sending the Master Out signal pulse, the sequencer accepts up to eight Sync In signal pulses while it waits for the disk drive response.

4.. Again, the disk drive must receive the same number of Sync Out signal pulses (including the one Master Out signal pulse) as Sync In signal pulses it sent to the sequencer. After receiving the pulses, the disk drive resets the Slave In signal to 0 and terminates the information transfer. Doing so puts the interface in the SLAVE END state.

Ending Status Sequence

The ending status sequence generates controller and disk drive status after an information transfer. Figure 7-9 shows a block diagram of an ending status sequence.

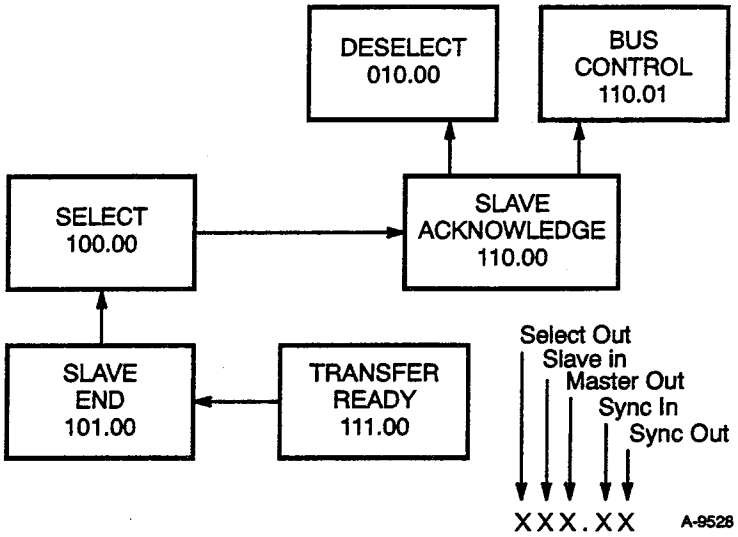


Figure 7-9. Ending Status Sequence

After every information transfer between the channel adapter and disk drive, the sequencer must perform an ending status sequence.

1.. After an information transfer, the disk drive resets the Slave In signal to 0. Doing so puts the interface into the SLAVE END state.

2.. The sequencer places the controller status on bus A and resets the Master Out signal to 0 (refer to Table 7-7). Doing so puts the interface into the SELECT state.

Table 7-7. Controller Status on Bus A

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Good transfer	Bus parity error	0	0	0	0	0	0

Table 7-8 shows examples of a successful and an unsuccessful information transfer.

Table 7-8. Sample Controller Statuses

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Description
1	0	0	0	0	0	0	0	The channel adapter indicates the information transfer was successful.
0	0	0	0	0	0	0	0	The channel adapter indicates the information transfer was not successful.

3.. The disk drive places the drive ending status on bus B and sets the Slave In signal to 1 (refer to Table 7-9). Doing so puts the interface in the SLAVE ACKNOWLEDGE state.

Table 7-9. Drive Ending Status on Bus B

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Good transfer	Bus parity error	Odd byte transfer	Timed operation	Final status after operation			

Table 7-10 shows examples of drive ending status. For more information on the drive ending statuses on bus B, refer to the "channel adapter Systems Status" section.

Table 7-10. Sample Drive Ending Statuses

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Description
1	0	0	0	0	0	0	0	The disk drive indicates a successful information transfer.
0	1	0	0	0	0	0	0	The disk drive detected a parity error on a bus control command, information transfer, or controller status.
0	0	0	1	0	0	0	0	The disk drive has not completed the last command.
0	0	0	0	0	0	0	1	The disk drive is busy and did not accept the last bus control command.

If the sequencer is starting another disk drive operation, it loads bus A with a bus control command and starts a bus control sequence.

If the sequencer is deselecting the disk drive, it starts a deselect sequence.

Deselect Sequence

The deselect sequence logically disconnects a disk drive from the channel adapter. Figure 7-10 shows a deselect sequence.

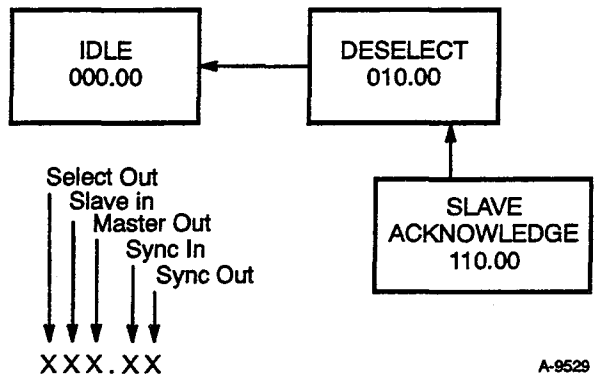


Figure 7-10. Deselect Sequence

The deselect sequence starts from the SLAVE ACKNOWLEDGE state. The sequencer performs a deselect sequence after an ending status or select sequence.

1.. While the IPI-2 interface is in the SLAVE ACKNOWLEDGE state, the sequencer resets the Select Out signal to 0. Doing so puts the interface in the DESELECT state. Bus A and bus B do not contain any information.

2.. The disk drive resets the Slave In signal to 0. Doing so puts the interface in the IDLE state. Bus A and bus B do not contain any information.

During disk drive operations, the sequencer must perform a deselect sequence before performing an interrupt request (poll), disk drive reset, master reset, transfer settings request, or drive interrupt request sequence.

Interrupt Request (Poll) Sequence

The interrupt request (poll) sequence requests all disk drives connected to the channel that have specific interrupts pending to respond on bus B. Figure 7-11 shows an interrupt request sequence.

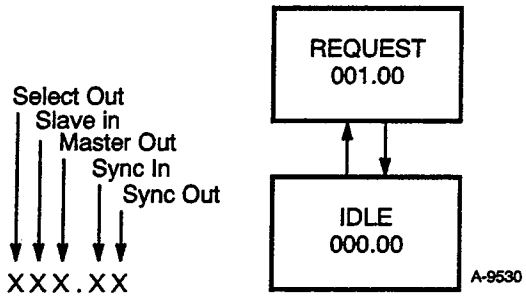


Figure 7-11. Interrupt Request (Poll) Sequence

Before an interrupt request sequence begins, the *j* and *k* registers in the channel adapter must be loaded with the interrupt request (refer to Table 7-11). The *i* register in the channel adapter must also be loaded with a bit mask set for the requested disk drive.

1.. The sequencer transfers the interrupt request from the *j* register to bus A and sets the Master Out signal to 1 (refer to Table 7-11). Doing so puts the interface in the REQUEST state.

Table 7-11. Interrupt Request on Bus A

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
0	Report busy status	Report ready status	Slave power failure alert	Power on status request	Report status pending interrupt	Report RPS interrupt	Report command complete interrupt

2.. Each disk drive that matches the interrupt request loads bus B with the drive select response (refer to Table 7-12) and sets the Attention In signal. As soon as the disk drive that matches the bit mask in the *i* register responds, the sequencer resets the Master Out signal to 0 to complete the interrupt request sequence.

Table 7-12. Drive Select Response on Bus B

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Disk drive 7	Disk drive 6	Disk drive 5	Disk drive 4	Disk drive 3	Disk drive 2	Disk drive 1	Disk drive 0

Reset Disk Drive Sequence

The reset disk drive sequence resets a selected disk drive. Figure 7-12 shows a reset disk drive sequence.

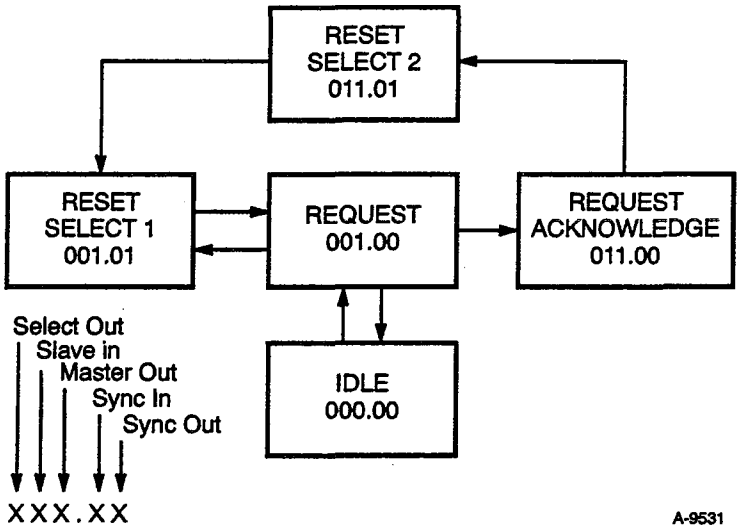


Figure 7-12. Reset Disk Drive Sequence

Before a reset disk drive sequence begins, the *j* register in the channel adapter must be loaded with the selective reset (refer to Table 7-13).

1.. The sequencer transfers the selective reset (refer to Table 7-13) from the *j* register in the channel adapter to bus A and sets the Master Out signal to 1. Doing so puts the interface in the REQUEST state.

Table 7-13. Selective Reset on Bus A

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	Disk drive address Bit 2^4 is the least significant bit			Disable interface drivers	Reset disk drive	Reset logical interface	Reset physical interface

2.. The disk drive sets the Slave In signal to 1, which puts the interface in the REQUEST ACKNOWLEDGE state. Bus B is not defined during a reset disk drive sequence.

3.. The sequencer sets the Sync Out signal to 1 to put the interface in the RESET SELECT 2 state.

4.. The disk drive resets the Slave In signal to 0 to enter the RESET SELECT 1 state.

5.. The disk drive starts the reset action after the Sync Out signal is set to 1 for at least 2 microseconds.

6.. After a set amount of time, the sequencer resets the Sync Out signal to 0 to reenter the REQUEST state.

7.. The sequencer terminates the reset disk drive sequence by resetting the Master Out signal to 0.

Master Reset Sequence

The sequencer performs a master reset sequence to enter the MAINTENANCE state. Figure 7-13 shows a master reset sequence.

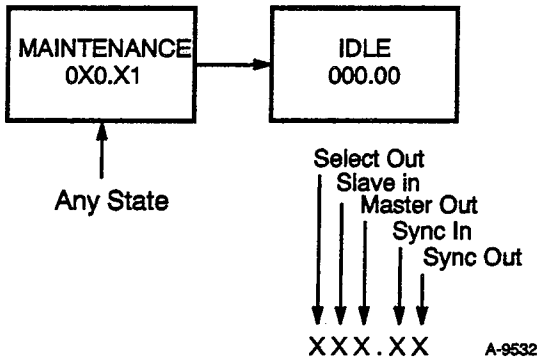


Figure 7-13. Master Reset Sequence

The master reset sequence starts from any state on the IPI-2 interface.

1.. The sequencer resets the Select Out and Master Out signals to 0 and sets the Sync Out signal to 1 for at least 10 microseconds. Doing so puts the interface into the MAINTENANCE state.

2.. The sequencer loads bus A with a master reset parameter (refer to Table 7-14) and resets the Sync Out signal to 0 to enter the IDLE state. (Only two of the three data out bits, 2^1, 2^4, or 2^7 are set.)

Table 7-14. Master Reset on Bus A

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Data out 2	Not used	Not used	Data out 1	Not used	Not used	Data out 0	Not used

Transfer Settings Request Sequence

The transfer settings request sequence sends the transfer settings for a specific disk drive to the channel adapter. Figure 7-14 shows a transfer settings request sequence.

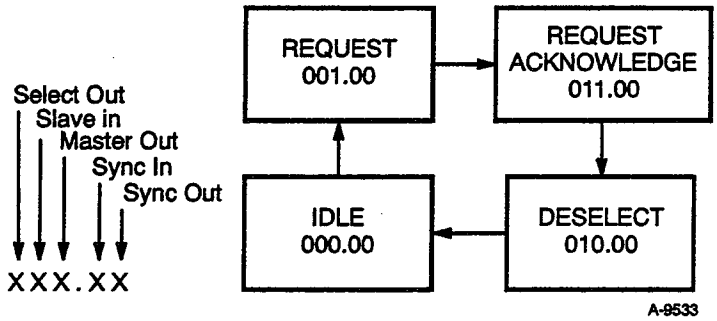


Figure 7-14. Transfer Settings Request and Interrupt Request Sequence

Before a transfer settings request sequence begins, the *j* and *k* registers in the channel adapter must be loaded with the transfer settings request (refer to Table 7-15).

1.. The sequencer transfers the transfer settings request (refer to Table 7-15) from the *j* register in the channel adapter to bus A and sets the Master Out signal to 1. Doing so puts the interface in the REQUEST state.

Table 7-15. Transfer Settings Request on Bus A

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	Disk drive address Bit 2^4 is the least significant bit			0	0	0	0

2.. The disk drive loads bus B with the transfer settings (refer to Table 7-16) and sets the Slave In signal to 1. Doing so puts the interface in the REQUEST ACKNOWLEDGE state.

Table 7-16. Transfer Settings on Bus B

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
0	0	1	0	0	1	1	0

3.. The sequencer resets the Master Out signal to 0 to terminate the transfer settings request. Doing so puts the interface into the DESELECT state.

4.. The disk drive acknowledges the termination and resets the Slave In signal to 0 to put the interface into the IDLE state.

Drive Interrupt Request Sequence

The drive interrupt request sequence transfers the interrupts for a specific disk drive to the channel adapter. Figure 7-14 shows a drive interrupt request sequence. Before a drive interrupt request sequence begins, the *j* and *k* registers in the channel adapter must be loaded with the drive interrupt request (refer to Table 7-17).

1.. The sequencer transfers the drive interrupt request (refer to Table 7-17) from the *j* register in the channel adapter to bus A and sets the Master Out signal to 1. Doing so puts the interface in the REQUEST state.

Table 7-17. Drive Interrupt Request on Bus A

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	Disk drive address Bit 2^4 is the least significant bit			1	0	0	0

2.. The disk drive loads bus B with the drive interrupts (refer to Table 7-18) and sets the Slave In signal to 1. Doing so puts the interface into the REQUEST ACKNOWLEDGE state.

Table 7-18. Drive Interrupts on Bus B

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
0	Busy status	Ready status	0	Priority select status	Status pending interrupt active	RPS interrupt active	Command complete interrupt

3.. The sequencer resets the Master Out signal to 0 to terminate the drive interrupt request. Doing so puts the interface in the DESELECT state.

4.. The disk drive acknowledges the termination and resets the Slave In signal to 0 to enter the IDLE state.

8 DCA-2 BASIC THEORY OF OPERATIONS

This section covers the basic theory of the DCA-2 disk channel adapter, including a description of the options on the DCA-2 and a description of the intelligent peripheral interface-2 (IPI-2) protocol.

DCA-2 Options

The DCA-2 contains 12 options that translate EIOP commands into IPI-2 protocol and transfer data between the EIOP and the disk drives. These options are described below. Figure 8-1 is a block diagram of the options on the DCA-2.

3YA Option

The 3YA option is an interface between the DCA-2 and the EIOP buffer board. It transfers data during write data and read data operations.

During write operations, the EIOP transfers a 72-bit word from the EIOP buffer board to the 3YA option in six 12-bit transfers. A word contains 64 bits of data and 8 single-error correction/double-error detection (SECDED) check bits. For each data word, a check byte (an 8-bit Hamming Code †) is generated. The 3YA option sends the 72-bit word to the 3YC option in five 16-bit transfers.

During read operations, the 3YA option receives each word from the 3YB option in four 16-bit transfers. During the last two transfers, the 3YA also receives check bits from the 3YB in 4-bit transfers. After receiving the data and check bits, the 3YA option sends the 72-bit word to the EIOP buffer board in six 12-bit transfers.

† † Hamming, R. W. "Error Detection and Correcting Codes." *Bell System Technical Journal.* 29.2 (1950): 147-160.

3YC Option

The 3YC option stores data and checks for errors during write data operations. After receiving the data and check bits from the 3YA option, the 3YC generates a new set of check bits for the data. If the new check bits do not match the previous set of check bits, the 3YC checks for a single-bit or double-bit SECDED error.

If a single-bit error has occurred, the 3YC option changes the value of the incorrect bit and sends a signal to the 3DD option that a single-bit error occurred. If a double-bit error occurred, the 3YC is incapable of determining the incorrect bits and sends a signal to the 3DD option that a double-bit error occurred.

After performing SECDED, the 3YC generates 2 parity bits for each parcel of data. One parity bit is for bits 2^0 through 2^7 (bus B information) and the other parity bit is for bits 2^8 through 2^{15} (bus A information). The 3YC sends the parcel and parity bits to the 3DH options.

3DH0 Option

The 3DH0 option contains four separate circuits that generate error correction code (ECC) for half of a sector in a DD-301. For example, one circuit generates ECC for bits 2^0 and 2^8. These bits correspond to the data read from or written to channel 0 of a head group in a DD-301 (refer to the "Read/Write Boards" subsection in Section 5 of this manual.)

During write data operations, the 3DH0 receives 8 bits of data (bits 2^0 through 2^3 and bits 2^8 through 2^{11} of a parcel) from the 3YC option. The 3DH0 calculates a partial ECC for each byte of data and sends the byte of data to the 3DF option. After a sector of data passes through the 3DH0, the 3DH0 sends the complete ECC for four of the channels in a head group to the 3DF option in 8-bit transfers. The 3DH0 option also generates parity bits on the ECC data. The 3DH0 also receives a parity bit for bits 2^0 through 2^7 of a parcel (bus B information) from the 3YC option. The 3DH0 sends this parity bit with each byte of data it transfers to the 3DF option.

During read data operations, the 3DH0 receives 8 bits of data from the 3DE option (bits 2^0 through 2^3 and bits 2^8 through 2^{11} of a parcel). The 3DH0 calculates a partial ECC for each byte of data and stores the information. Immediately after receiving a sector of data, the 3DH0 receives ECC channels 0 through 3 in a head group from the 3DE option. The 3DH0 compares this ECC with the ECC it generated. If the codes do not match, the 3DH0 sends an ECC error to the 3DG option.

3DH1 Option

The 3DH1 option performs the same operations as the 3DH0 option; however, it receives bits 2^4 through 2^7 and 2^{12} through 2^{15} of a parcel. These bits correspond to channels 4 through 7 of a head group in a DD-301. The 3DH1 also transfers the parity bit for bits 2^8 through 2^{15} of a parcel (bus A information) from the 3YC option to the 3DF option.

3DF Option

The 3DF option contains signal lines and registers used for IPI-2 information transfers to the disk drive. It also transfers write data from the DCA-2 to the disk drive.

The 3DF option is the IPI-2 communication link for transfers from the DCA-2 to the disk drive. It contains the Select Out, Master Out, Sync Out, Bus A, and Bus B signals used for IPI-2 protocol.

The 3DF option also contains *i*, *j*, and *k* registers, which store IPI commands. Before an information transfer occurs, the *i*, *j*, or *k* registers of the 3DF option are loaded with IPI commands. After receiving a signal from the sequencer (RAM), the 3DF transfers the information stored in the registers to the disk drive over bus A.

During a write data operation, the 3DF receives a parcel of information from the 3DH options. The 3DF option receives bits 2^0 through 2^3 and 2^8 through 2^{11} from 3DH0 and bits 2^4 through 2^7 and 2^{12} through 2^{15} from 3DH1. After receiving the parcel of data, 3DF loads bus B with bits 2^0 through 2^7 and bus A with bits 2^8 through 2^{15}.

The 3DF option also receives two parity bits from the 3DH options. Write data on bus B is protected with the parity bit from 3DH0, and write data on bus A is protected with the parity bit from 3DH1. The 3DF option sends the data and parity bits to the disk drive after it receives them from the 3DH options.

3DE Option

The 3DE option receives IPI-2 control and information transfers from the disk drive. It also receives read data from the disk drive and transfers it to the other options on the DCA-2.

The 3DE option is the IPI-2 communication link for transfers from the disk drive to the DCA-2. It receives the Slave In, Sync In, Bus A, and Bus B signals used for IPI-2 protocol.

During a read data operation, the 3DE receives a byte of data plus a parity bit from both bus A and bus B. After receiving the data and parity bits, the 3DE transfers the information to the 3YB, 3DG, 3DH0, and 3DH1 options. If the read data is ending status or status response information, the 3DE transfers the information from bus B to the 3DJ and 3DI options.

The 3DE option can also perform bit stream replacement, which corrects misread data from a failing head. The 3DE option replaces the data from the failing head with the sum of the data from the other heads and the parity head. The DCA-2:17 channel function transfers the information needed for bit stream replacement to the 3DE. For more information on channel functions, refer to the "DCA-2 Channel Functions" section of this manual.

3YB Option

The 3YB option stores data and generates SECDED check bits during read data operations. It also checks the parity information.

During read data operations, the 3YB receives a word of data from the 3DE option in four 16-bit transfers. While receiving the word of data, the 3YB generates eight SECDED check bits for the word. It sends the word of data to the 3YA option in four 16-bit transfers. During the last two transfers of data, the 3YB sends the check bits in 4-bit transfers.

The 3YB option also generates a new parity bit for each byte of data it receives from the 3DE. If the new parity bit does not match the previous parity bit, the 3YB signals the 3DD that a byte 0 (bus B) or byte 1 (bus A) parity error occurred.

3DG Option

The 3DG option contains registers for comparing the sector ID field to the expected ID field. It also contains counters for counting parcels of information transferred between the DCA-2 and the disk drive.

The parameter register and cylinder register in the 3DG option store sector ID field parameters. The parameter register stores the head, sector, and option bits (ID parameter 1) of the ID field. The cylinder register stores the cylinder address (ID parameter 0) of the ID field. For more information on the sector ID field, refer to the "Format and Flaw Management" disk drive sections of this manual.

The 3DG option also contains a parcel counter and a defect counter. The parcel counter counts each parcel as it is transferred between the DCA-2 and the disk drive. The defect counter is used to create a defect pad that hides media flaws. For more information on media flaws and the defect pad, refer to the "Format and Flaw Management" disk drive sections of this manual.

3DD Option

The 3DD option receives DCA-2 channel functions and transfers control signals between the EIOP and DCA-2. After receiving a DCA-2 channel function from the EIOP, the 3DD transfers the function information to the appropriate options on the DCA-2. The 3DD option also contains registers that store errors and internal status generated by the DCA-2. When requested, the 3DD transfers this status information to the EIOP.

3DI Option

The 3DI option counts the number of information transfers between the EIOP and the DCA-2. It also controls the sequencer address (3DJ option) and sends data to the RAM, hereafter referred to as the sequencer.

The transfer counter in the 3DI option counts the transfers between the EIOP local memory or EIOP buffer board and the DCA-2. Before an information transfer occurs, the transfer counter is loaded with the number of parcels to be transferred. The transfer counter decrements once for each parcel transferred.

The 3DI option also controls the sequencer address. The 3DI option signals the 3DJ option when to reset the sequencer address, when to advance the sequencer address, and when the transfer counter reaches zero.

3DJ Option

The 3DJ option transfers the sequencer address to the sequencer. After receiving the signals from the 3DI option, the 3DJ increments the sequencer address or resets the sequencer address to zero. The 3DJ option also monitors conditions of the other options on the DCA-2 that are used for branch control of the sequencer address.

RAM

The RAM is a sequencer that controls the operation of the DCA-2 registers and IPI-2 signal lines. It contains 1,024 addresses that each hold 32 bits of sequencer data.

After receiving the sequencer address from the 3DJ option, the sequencer transfers the sequencer data to the 3DI and the 3DJ options. As the 3DJ option increments through the addresses of the sequencer, the sequencer data controls when the registers on each option are transferred to signal lines and when the IPI-2 signal lines are set or reset.

The information stored in the RAM may be transferred to the EIOP local memory or written over by information from the EIOP local memory. For more information on loading or reading the sequencer data, refer to the "DCA-2 Channel Functions" section of this manual.

9 DCA-2 CHANNEL FUNCTIONS

Channel functions for the DCA-2 channel adapter load registers in the DCA-2 and auxiliary input/output processor (EIOP) with information for disk drive operations. The channel functions also transfer a sequencer starting address to initiate an IPI-2 bus state sequence. This section describes each channel function and sample disk drive routines.

Channel Function Descriptions

Table 9-1 briefly describes each DCA-2 channel function; the following subsections describe each function in more detail.

Table 9-1. Channel Functions

Function	EIOP Channel	Description
DCA2:0	Even or odd	Clears the channel busy and channel done flags
DCA2:1	Even	Transfers information from the DCA-2 to local memory
DCA2:1	Odd	Transfers information from local memory to the DCA-2
DCA2:2	Even or odd	Loads the cylinder register with ID parameter 0
DCA2:3	Even or odd	Loads the parameter register with ID parameter 1
DCA2:4	Even or odd	Loads the DCA-2 transfer counter with the transfer count
DCA2:5	Even or odd	Transfers information between the DCA-2 and buffer board
DCA2:6	Even or odd	Disables channel interrupts
DCA2:7	Even or odd	Enables channel interrupts
DCA2:10	Even or odd	Reads the channel local memory address register
DCA2:11	Even or odd	Reads the channel parcel counter
DCA2:12	Even or odd	Reads one of four status parcels
DCA2:13	Even or odd	Reads one of three status parcels
DCA2:14	Even or odd	Loads the channel local memory address register
DCA2:15	Even or odd	Loads the channel local memory parcel counter
DCA2:16	Even or odd	Loads the DCA-2 *j* and *k* registers with IPI-2 commands
DCA2:17	Even	Loads the sequencer mode select register
DCA2:17	Odd	Loads the bit stream head select register

DCA2:0 – Clear Channel Busy and Channel Done Flags

The DCA2:0 function resets the EIOP channel busy and channel done flags to 0 or performs a master clear of the channel. The value of the function modifier bits in the *d* field of the EIOP instruction or in the B register on the EIOP selects the operation to be performed (refer to Figure 9-1).

d Field or B Register								
2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
M 2^3	M 2^2	M 2^1	M 2^0	C 2^4	C 2^3	C 2^2	C 2^1	C 2^0

M = Function Modifier Bits
C = Channel Number

Figure 9-1. EIOP Instruction *d* Field or EIOP B Register

If the function modifier bits are set to 0, the function clears the channel busy and channel done flags. The flags cannot be sampled until 8 clock pulses have passed since the function was issued.

If function modifier bits 1, 2, and 3 are set to 1, this function performs a master clear of the DCA-2.

DCA2:1 – Local Memory Input and Output Transfer

The DCA2:1 function transfers the starting address for the sequencer and a value for the *i* register from the accumulator to the DCA-2. This function is used for information transfers between the DCA-2 and EIOP local memory.

Figure 9-2 shows the format of the sequencer starting address and *i* register value in the accumulator. When this function is executed, the DCA-2 loads the *i* register in the 3DF option with the *i* register value and loads the sequencer with the sequencer starting address.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
i 2^7	i 2^6	i 2^5	i 2^4	i 2^3	i 2^2	i 2^1	i 2^0	X x	SQ 2^6	SQ 2^5	SQ 2^4	SQ 2^3	SQ 2^2	SQ 2^1	SQ 2^0

i = *i* Register Value
X = Not Used
SQ = Sequencer Starting Address

Figure 9-2. DCA2:1 Sequencer Starting Address

After receiving the starting address, the sequencer starts an interlocked information transfer. If the DCA2:1 function is executed on the even EIOP channel, the sequencer transfers information from the DCA-2 to local memory. If the function is executed on the odd EIOP channel, the sequencer transfers information from local memory to the DCA-2. The value of the function modifier bits selects the type of information transferred: IPI-2 protocol, sequencer microcode, or the error-correction code (ECC) register contents (refer to Table 9-2).

Table 9-2. Function Modifier Bits

Modifier Bits 2^3	2^2	2^1	2^0	Description
0	0	0	0	IPI-2 protocol transfer from local memory to the disk drive
0	0	0	1	IPI-2 status transfer from the disk drive to local memory
0	0	1	0	Sequencer microcode transfer from local memory to the DCA-2
0	0	1	1	Sequencer microcode transfer from the DCA-2 to local memory
0	1	0	1	ECC register transfer from the DCA-2 to local memory

IPI-2 Protocol Transfers

IPI-2 information is transferred from local memory to the disk drive in an interlocked transfer-to-disk sequence. For an example of this operation, refer to the "Seek Routine" subsection in this section.

IPI-2 status information is transferred from the drive to local memory in an interlocked transfer-from-disk sequence (refer to Figure 7-6). The *i* register value determines what type of status is transferred.

Sequencer Microcode Transfers

All transfers start at the first address of the sequencer and exchange 1,024 32-bit data words. After executing a transfer of sequencer microcode, the DCA2:0 function is executed. This function clears the DCA-2 control logic and direct memory access (DMA) references. The same channel numbering convention is used for the DCA2:0 function as for the DCA2:1 function.

Error-correction Code Register Transfer

During an ECC register transfer, the contents of all eight 4-byte ECC registers are transferred from the 3DH options to local memory.

DCA2:2 – Set ID Parameter 0

The DCA2:2 function transfers the cylinder address (ID parameter 0) from the accumulator to the cylinder register in the 3DG option of the DCA-2. Figure 9-3 shows the format of ID parameter 0 in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
C 2^{15}	C 2^{14}	C 2^{13}	C 2^{12}	C 2^{11}	C 2^{10}	C 2^{9}	C 2^{8}	C 2^{7}	C 2^{6}	C 2^{5}	C 2^{4}	C 2^{3}	C 2^{2}	C 2^{1}	C 2^{0}

C = Cylinder Address (0 - 5062_8)

Figure 9-3. ID Parameter 0 Format

DCA2:3 – Set ID Parameter 1

The DCA2:3 function transfers the sector address, head address, and option bits (ID parameter 1) from the accumulator to the parameter register in the 3DG option of the DCA-2. Figure 9-4 shows the format of ID parameter 1 in the accumulator. Refer to the "Format and Flaw Management" disk drive sections of this manual for more information on the ID information bit descriptions (which include ID parameter 1).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
X	X	WP	RP	X	H	H	H	H	H	S	S	S	S	S	S
x	x	2^{0}	2^{0}	x	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

X = Not Used
WP = Write Protected
RP = Read Protected
H = Head Group Address
S = Sector Address

Figure 9-4. ID Parameter 1 Format

DCA2:4 – Set Transfer Count

The DCA2:4 function transfers the transfer count from the accumulator to the 3DI option in the DCA-2. The transfer count is the total number of parcels to be transferred between the DCA-2 and the disk drive (in octal). Figure 9-5 shows the format of the transfer count in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

T = Transfer Count

Figure 9-5. Transfer Count Format

DCA2:5 – Starting Sequencer Address and *i* Register Value

The DCA2:5 function transfers the starting address for the sequencer and a value for the *i* register from the accumulator to the DCA-2. This function is used for information transfers between the DCA-2 and the EIOP buffer board.

Figure 9-6 shows the format of the sequencer starting address and *i* register value in the accumulator. When this function is executed, the DCA-2 loads the *i* register in the 3DF option with the *i* register value and loads the sequencer with the sequencer starting address.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
i 2^{7}	i 2^{6}	i 2^{5}	i 2^{4}	i 2^{3}	i 2^{2}	i 2^{1}	i 2^{0}	X x	SQ 2^{6}	SQ 2^{5}	SQ 2^{4}	SQ 2^{3}	SQ 2^{2}	SQ 2^{1}	SQ 2^{0}

i = *i* Register Value
X = Not Used
SQ = Sequencer Starting Address

Figure 9-6. DCA2:5 Sequencer Starting Address Format

After receiving the starting address, the sequencer starts an IPI-2 bus state sequence. For an example, refer to the "Write Sector Data Routine" subsection later in this section.

DCA2:6 – Disable Interrupt Enable

The DCA2:6 function sets the EIOP channel enable interrupts flag to 0. When the enable interrupts flag is 0, the channel does not acknowledge any interrupts it receives. This function does not change the states of the channel busy or channel done flags.

DCA2:7 – Enable Interrupt Enable

The DCA2:7 function sets the EIOP channel enable interrupts flag to 1. When the enable interrupts flag is 1, the channel acknowledges any interrupts it receives. This function does not change the states of the channel busy or channel done flags.

DCA2:10 – Read Local Memory Address

The DCA2:10 function transfers the current local memory address from the EIOP channel local memory address register to the accumulator. Figure 9-7 shows the format of the local memory address in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
LM 2^{15}	LM 2^{14}	LM 2^{13}	LM 2^{12}	LM 2^{11}	LM 2^{10}	LM 2^{9}	LM 2^{8}	LM 2^{7}	LM 2^{6}	LM 2^{5}	LM 2^{4}	LM 2^{3}	LM 2^{2}	LM 2^{1}	LM 2^{0}

LM = Current Local Memory Address

Figure 9-7. Current Local Memory Address Format

DCA2:11 – Read Local Memory Parcel Count

The DCA2:11 function transfers the inverse of the EIOP channel parcel counter to the accumulator. To obtain the correct parcel count, the accumulator contents must be inverted. Figure 9-8 shows the format of the inverted parcel count in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
IP 2^{15}	IP 2^{14}	IP 2^{13}	IP 2^{12}	IP 2^{11}	IP 2^{10}	IP 2^{9}	IP 2^{8}	IP 2^{7}	IP 2^{6}	IP 2^{5}	IP 2^{4}	IP 2^{3}	IP 2^{2}	IP 2^{1}	IP 2^{0}

IP = Inverted Parcel Count from the 3DG Option

Figure 9-8. Inverted Parcel Count Format

DCA2:12 – Status Function 0

The DCA2:12 function transfers 1 of 5 status parcels from the DCA-2 to the accumulator. The initial value of the accumulator determines which status parcel is transferred. Figure 9-9 shows the format of the initial accumulator value.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
X	X	X	X	X	X	X	X	X	X	X	X	X	X	ST	ST
x	x	x	x	x	x	x	x	x	x	x	x	x	x	2^{1}	2^{0}

X = Not Used ST = Status Select Bits

Figure 9-9. Status Select Format

Adapter Status

If the status select bits are both 0, the DCA-2 transfers the adapter status to the accumulator. Figure 9-10 shows the format of the adapter status in the accumulator. For more information on status, refer to the "DCA-2 Systems Status" section of this manual.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
SP	SP	SP	SP	V5	V4	DS	SS	CS	CS	CS	CS	CS	CS	CS	CS
2^{3}	2^{2}	2^{1}	2^{0}	2^{0}	2^{0}	2^{0}	2^{0}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

SP = Sequencer Parity Error
V5 = Voltage Fault +5 V
V4 = Voltage Fault –4.5 V
DS = Double-bit Error
SS = Single-bit Error
CS = Channel Adapter Status

Figure 9-10. Adapter Status Format

6X Condition Bits

If the status select bits are both 0 and the sequencer is first given a starting address of 36_8 (using the DCA2:5 function), the DCA-2 transfers the 6X condition bits to the accumulator. Figure 9-11 shows the format of the 6X condition bits in the accumulator. For more information on status, refer to the "DCA-2 Systems Status" section of this manual.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
X x	X x	X x	X x	X x	X x	X x	X x	6X 2^{7}	6X 2^{6}	6X 2^{5}	6X 2^{4}	6X 2^{3}	6X 2^{2}	6X 2^{1}	6X 2^{0}

6X = 6X Condition Bits

Figure 9-11. 6X Condition Bits Format

7X Condition Bits

If the status select bits are both 0 and the sequencer is first given a starting address of 37_8 (using the DCA2:5 function), the DCA-2 transfers the 7X condition bits to the accumulator. Figure 9-12 shows the format of the 7X condition bits in the accumulator. For more information on status, refer to the "DCA-2 Systems Status" section of this manual.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
X x	X x	X x	X x	X x	X x	X x	X x	7X 2^{7}	7X 2^{6}	7X 2^{5}	7X 2^{4}	7X 2^{3}	7X 2^{2}	7X 2^{1}	7X 2^{0}

7X = 7X Condition Bits

Figure 9-12. 7X Condition Bits Format

Syndrome Status

If status select bit 2^1 is 0 and bit 2^0 is 1, the DCA-2 transfers the syndrome status to the accumulator. Figure 9-13 shows the format of the syndrome status in the accumulator. For more information on status, refer to the "DCA-2 Systems Status" section of this manual.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
DC 2^{3}	DC 2^{2}	DC 2^{1}	DC 2^{0}	SC 2^{3}	SC 2^{2}	SC 2^{1}	SC 2^{0}	SY 2^{7}	SY 2^{6}	SY 2^{5}	SY 2^{4}	SY 2^{3}	SY 2^{2}	SY 2^{1}	SY 2^{0}

DC = Double-bit Error Count
SC = Single-bit Error Count
SY = Syndrome Bits

Figure 9-13. Syndrome Status Format

Transfer Count Status

If status select bit 2^1 is 1 and bit 2^0 is 0, the DCA-2 sends the transfer count status to the accumulator. The transfer count is the current value of the transfer counter in the 3DI option of the DCA-2. Figure 9-14 shows the format of the byte count status in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
T 2^{15}	T 2^{14}	T 2^{13}	T 2^{12}	T 2^{11}	T 2^{10}	T 2^9	T 2^8	T 2^7	T 2^6	T 2^5	T 2^4	T 2^3	T 2^2	T 2^1	T 2^0

T = Transfer Count

Figure 9-14. Byte Count Status Format

Tag Status

If both status select bits are 1, the DCA-2 transfers the tag status to the accumulator. Figure 9-15 shows the format of the tag status in the accumulator. For more information on status, refer to the "DCA-2 Systems Status" section of this manual.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{11}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^1
X x	X x	X x	X x	X x	X x	X x	X x	X x	SO 2^0	MO 2^0	SL 2^0	X x	SI 2^0	SV 2^0	AI 2^0

X = Not Used
SO = Sync Out Signal
MO = Master Out Signal
SL = Select Out Signal
SI = Sync In Signal
SV = Slave In Signal
AI = Attention In Signal

Figure 9-15. Tag Status Format

DCA2:13 – Status Function 1

The DCA2:13 function transfers 1 of 3 status parcels to the accumulator. The initial value of the accumulator determines which status parcel is transferred. Figure 9-9 shows the format of the initial accumulator value.

Drive Ending Status

If the status select bits are both 0, the DCA-2 transfers the drive ending status to the accumulator. Figure 9-16 shows the format of the drive ending status in the accumulator. For more information on status, refer to the "DCA-2 Systems Status" section of this manual.

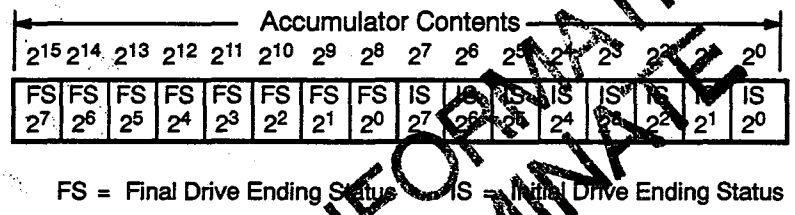


Figure 9-16. Drive Ending Status Format

ID Parameter 0 Status

If status select bit 2^1 is 0 and bit 2^0 is 1, the DCA-2 transfers ID parameter 0 status to the accumulator. ID parameter 0 status is the current value stored in the cylinder register (ID parameter 0) of the 3DG option on the DCA-2. Refer again to Figure 9-3 for the format of ID parameter 0 in the accumulator.

ID Parameter 1 Status

If status select bit 2^1 is 1 and bit 2^0 is 0, the DCA-2 transfers ID parameter 1 status to the accumulator. ID parameter 1 status is the current value stored in the parameter register (ID parameter 1) of the 3DG option on the DCA-2. Refer again to Figure 9-4 for the format of ID parameter 1 in the accumulator.

PRELIMINARY INFORMATION
DO NOT DISSEMINATE

DCA2:14 – Enter Local Memory Starting Address

The DCA2:14 function transfers the local memory starting address from the accumulator to the EIOP channel local memory address register. The local memory starting address is the EIOP local memory address that contains the first parcel of data to be transferred to the DCA-2, or the EIOP local memory address to which the DCA-2 transfers the first parcel of data. Figure 9-17 shows the format of local memory starting address in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
LS 2^{15}	LS 2^{14}	LS 2^{13}	LS 2^{12}	LS 2^{11}	LS 2^{10}	LS 2^{9}	LS 2^{8}	LS 2^{7}	LS 2^{6}	LS 2^{5}	LS 2^{4}	LS 2^{3}	LS 2^{2}	LS 2^{1}	LS 2^{0}

LS = Local Memory Starting Address

Figure 9-17. Local Memory Starting Address Format

During a data transfer, the local memory address register of the channel automatically increments once with each parcel transferred. Execute the DCA2:10 function to transfer the current value of the local memory address register of the channel to the accumulator.

DCA2:15 – Enter Local Memory Parcel Count

The DCA2:15 function transfers the local memory parcel count from the accumulator to the EIOP channel parcel counter. The parcel count is the number of parcels to be transferred between the EIOP local memory and the DCA-2. Figure 9-18 shows the format of the parcel count in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
PC 2^{15}	PC 2^{14}	PC 2^{13}	PC 2^{12}	PC 2^{11}	PC 2^{10}	PC 2^{9}	PC 2^{8}	PC 2^{7}	PC 2^{6}	PC 2^{5}	PC 2^{4}	PC 2^{3}	PC 2^{2}	PC 2^{1}	PC 2^{0}

PC = Parcel Count

Figure 9-18. Parcel Count Format

During a data transfer, the channel parcel counter automatically decrements once for each parcel transferred. Execute the DCA2:11 function to transfer the inverted current value of the channel parcel counter to the accumulator.

DCA2:16 – Enter *j* and *k* Control Register Contents

The DCA2:16 function transfers values for the *j* and *k* registers from the accumulator to the 3DF option in the DCA-2. The *j* and *k* registers store bus control codes or IPI-2 command information bytes. Figure 9-19 shows the format of the *j* and *k* register values in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
k 2^7	k 2^6	k 2^5	k 2^4	k 2^3	k 2^2	k 2^1	k 2^0	j 2^7	j 2^6	j 2^5	j 2^4	j 2^3	j 2^2	j 2^1	j 2^0

k = *k* Register Value j = *j* Register Value

Figure 9-19. *j* and *k* Register Values

The sequencer on the DCA-2 controls when the *j* and *k* register contents are sent to the disk drive over bus A or over both bus A and bus B. For an example of this, refer to the "Write Sector Data Routine" subsection later in this section.

DCA2:17 – Enter Mode Select

The DCA2:17 function performs different operations when it is executed on the even channel than when it is executed on the odd channel. The differences are described below.

Even Channel

When executed on the even channel, the DCA2:17 function transfers sequencer mode bits from the accumulator to the sequencer on the DCA-2. The mode bits can be altered for any function sequence. Figure 9-20 shows the format of the sequencer mode bits in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
X	X	X	X	X	X	X	X	M	M	M	M	M	M	M	M
x	x	x	x	x	x	x	x	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

X = Not Used M = Mode Bits for Sequencer

Figure 9-20. Mode Bits for the Sequencer

The sequencer mode bits abort an executing DCA-2 function, disable ECC circuitry, disable ID compare circuitry, enable bit stream mode, toggle the parity bit, or identify the specific disk drive type. Table 9-3 describes each sequencer mode bit.

Table 9-3. Sequencer Mode Bits

Bit	Name	Description
2^0	Abort	When set to 1, this bit signals the sequencer to terminate its operation. The channel Busy, Done, and Active signals are set to 0. (This bit is used only during an interrupt request (poll) sequence.
2^1	No ECC	When set to 1, this bit signals the sequencer to disable the ECC circuits.
2^2	Read ID	When set to 1, this bit signals the sequencer to transfer the first 4 parcels of ID information to the I/O buffer. This mode bit is used by ID verification utilities.
2^3	Read absolute	When set to 1, this bit signals the sequencer to read the data field without comparing the read ID field to the stored ID parameters.
2^4	Bit stream replacement	When set to 1, this bit signals the sequencer to enter the bit stream replacement mode. This mode is used with the DCA2:17 channel function on the odd channel.
2^5	Toggle parity	When set to 1, this bit signals the sequencer to toggle the parity bit on both buses for read or write operations.
2^6	2-head-parallel disk drive mode	When set to 1, this bit signals the sequencer that it is connected to a 2-head-parallel drive.
2^7	Serial disk drive mode	When set to 1, this bit signals the sequencer that it is connected to a serial disk drive.

Odd Channel

When executed on the odd channel, the DCA2:17 function transfers the lower byte of the accumulator to the bit stream mask register in the sequencer. Figure 9-21 shows the format of the bit stream select bits in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
X x	X x	X x	X x	X x	X x	X x	X x	B 2^{7}	B 2^{6}	B 2^{5}	B 2^{4}	B 2^{3}	B 2^{2}	B 2^{1}	B 2^{0}

X = Not Used B = Bit Stream Select Bits

Figure 9-21. Bit Stream Select Bits

NOTE: When not performing bit stream replacement, the bit stream number register contents must be set to 0's or data will be read incorrectly.

When a bit stream select bit is set to 1, the corresponding bits of bus A and bus B are replaced with a bit stream. The bit stream is calculated by summing the parity stream data with the other seven data streams. This enables data recovery to occur whenever a problem exists under a single head of the disk drive.

Sample Disk Drive Function Routines

Unlike previous Cray Research, Inc. channel adapter functions, DCA-2 channel functions do not correspond one-to-one with disk drive functions. For example, executing the DCA2:2 function (Set ID Parameter 0) does not cause the disk drive to seek to the cylinder address loaded in the accumulator.

Disk drive functions such as select, seek, or read operations are done with a function routine that may contain several channel functions. Generally, function routines consist of the following procedures:

1.. Clearing the channel busy and channel done flags for both EIOP channels.

2.. Loading the EIOP local memory or EIOP buffer board with information for the disk drive operation.

3.. Loading the registers in the DCA-2 with the values needed for the disk drive operation.

4.. Loading the counter registers in the DCA-2 and EIOP channel with the number of parcels to be transferred.

5.. Loading the sequencer with the starting address of the IPI-2 sequence for the disk drive operation.

The following subsections describe sample disk drive function routines. The actual routines and control codes used by the drivers, recovery routines, diagnostics, and utilities may not be the same as the following routines.

Select Unit Routine

The select unit routine logically connects the IOS to a disk drive. The routine consists of the following steps:

1.. The DCA2:0 function is executed on both channels to clear the EIOP channel busy and channel done flags.

2.. The accumulator is loaded with the disk drive address (refer to Table 7-2). Figure 9-22 shows an example of a disk drive address in the accumulator. This example selects the disk drive with the logical address 5. Refer to the "DD-301 Hardware Description" section of this manual for more information on the logical address.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
k	k	k	k	k	k	k	k	j	j	j	j	j	j	j	j
0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0

k = *k* Register Value j = *j* Register Value

Figure 9-22. Disk Drive Address for Logical Address 5

3.. The DCA2:16 function is executed. This function transfers the disk drive address to the *j* register in the 3DF option on the DCA-2.

4.. The accumulator is loaded with 13_8, the starting address of the select disk drive sequence (refer to Figure 9-23).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
i	i	i	i	i	i	i	i	X	SQ	SQ	SQ	SQ	SQ	SQ	SQ
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

i = *i* Register Value
X = Not Used
SQ = Sequencer Starting Address

Figure 9-23. Sequencer Starting Address for Select Disk Drive Sequence

5.. The DCA2:5 function is executed. This function transfers the starting address to the sequencer. After receiving the address, the sequencer performs a select disk drive sequence (refer to Figure 7-3). When the sequence is finished, the IPI-2 interface is in the SLAVE ACKNOWLEDGE state.

The following optional steps verify that the disk drive was successfully selected.

6.. The accumulator is loaded with 00_8, the status select bits for status 01 (refer to Figure 9-24).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
X	X	X	X	X	X	X	X	X	X	X	X	X	X	ST	ST
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

X = Not Used
ST = Status Select Bits

Figure 9-24. Status Select for Status 01

7.. The DCA2:13 function is executed. This function transfers the drive ending status to the accumulator. The ending status for a select disk drive sequence is the drive select response (refer to Table 7-3). Figure 9-25 shows the drive select response for logical address 5 in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
ES	ES	ES	ES	ES	ES	ES	ES	X	X	X	X	X	X	X	X
0	0	1	0	0	0	0	0	x	x	x	x	x	x	x	x

X = Not Used
ES = Ending Status

Figure 9-25. Drive Select Response in the Accumulator

Seek Routine

The seek routine moves the heads to a desired location over the platters. The seek routine consists of the following steps:

1.. A select unit routine is performed.

2.. Two sequential local memory addresses are loaded with data: the first with 0's and the second with the cylinder address (ID parameter 0). Refer to Figure 9-3 for the format of the cylinder address.

3.. The DCA2:0 function is executed on both EIOP channels to clear the channel busy and channel done flags.

4.. The accumulator is loaded with 02_8, the transfer count for a seek routine (refer to Figure 9-26).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

T= Transfer Count

Figure 9-26. Transfer Count for a Seek Routine

5.. The DCA2:4 function is executed. This function transfers the transfer count from the accumulator to the transfer counter in the 3DI option.

6.. The accumulator is loaded with the local memory starting address. The local memory starting address is the address that contains the cylinder address you entered in Step 2.

7.. The DCA2:14 function is executed. This function transfers the local memory starting address to the EIOP channel local memory address register.

8.. The accumulator is loaded with 02_8, the local memory parcel count for a seek routine (refer to Figure 9-27).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 1	PC 0

PC = Parcel Count

Figure 9-27. Parcel Count for a Seek Routine

9.. The DCA2:15 function is executed. This function transfers the parcel count to the EIOP channel's parcel count register.

10.. Bits 2^0 through 2^8 of the accumulator are loaded with the load cylinder bus control code (refer to Figure 9-28).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
k 0	k 0	k 0	k 0	k 0	k 0	k 0	k 0	j 0	j 0	j 0	j 0	j 0	j 1	j 0	j 0

k = *k* Register Value j = *j* Register Value

Figure 9-28. Load Cylinder Bus Control Code

11.. The DCA2:16 function is executed. This function transfers the bus control codes to the *j* and *k* registers in the 3DF option on the DCA-2.

12.. The accumulator is loaded with 04_8, the sequencer starting address for a command load (refer to Figure 9-29).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
i 0	i 0	i 0	i 0	i 0	i 0	i 0	i 0	X 0	SQ 0	SQ 0	SQ 0	SQ 0	SQ 1	SQ 0	SQ 0

i = *i* Register Value
X = Not Used
SQ = Sequencer Starting Address

Figure 9-29. Sequencer Starting Address for Command Load

13.. The DCA2:1 function is executed on the odd channel. This signals the sequencer to perform a bus control sequence (refer to Figure 7-4), an interlocked transfer-to-disk sequence (refer to Figure 7-5), and an ending status sequence (refer to Figure 7-9). When the sequences are finished, the IPI-2 interface is in the SLAVE ACKNOWLEDGE state.

Load Position Routine

The load position routine moves the heads to a desired location over the platters and selects the desired head. The load position routine consists of the following steps:

1.. A select unit routine is performed.

2.. Nine (11_8) sequential local memory addresses are loaded with the rotational position sensing (RPS) parameter. Refer to Table 9-4 for the format of the RPS parameter.

Table 9-4. RPS Parameter Parcel Descriptions

Parcels	Description
0 through 1_8	Cylinder address (ID parameter 0)
2	Head address
3	RPS target sector address
4	RPS pulse width extension
5 through 6_8	RPS pulse width
7 through 10_8	RPS pulse width skew

3.. The DCA2:0 function is executed on both channels to clear the channel's busy and done flags.

4.. The accumulator is loaded with 11_8, the transfer count for a load position routine (refer to Figure 9-30).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

T= Transfer Count

Figure 9-30. Transfer Count for a Load Position Routine

5.. The DCA2:4 function is executed. This function transfers the transfer count from the accumulator to the transfer counter in the 3DI option.

6.. The accumulator is loaded with the local memory starting address. The local memory starting address is the address that contains the parameters entered in Step 2.

7.. The DCA2:14 function is executed. This function transfers the local memory starting address to the EIOP channel local memory address register.

8.. The accumulator is loaded with 11_8, the local memory parcel count for a load position routine (refer to Figure 9-31).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 1	PC 0	PC 0	PC 1

PC = Parcel Count

Figure 9-31. Parcel Count for a Load Position Routine

9.. The DCA2:15 function is executed. This function transfers the parcel count to the EIOP channel's parcel count register.

10.. Bits 2^0 through 2^8 of the accumulator are loaded with the load position bus control code (refer to Figure 9-32).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
k 0	k 0	k 0	k 0	k 0	k 0	k 0	k 0	j 0	j 0	j 0	j 0	j 0	j 1	j 1	j 1

k = *k* Register Value j = *j* Register Value

Figure 9-32. Load Position Bus Control Code

11.. The DCA2:16 function is executed. This function transfers the bus control codes to the *j* and *k* registers in the 3DF option on the DCA-2.

12.. The accumulator is loaded with 04_8, the sequencer starting address for a command load (refer again to Figure 9-29).

13.. The DCA2:1 function is executed on the odd channel. This signals the sequencer to perform a bus control sequence (refer to Figure 7-4), an interlocked transfer-to-disk sequence (refer to Figure 7-5), and an ending status sequence (refer to Figure 7-9). When the sequences are finished, the IPI-2 interface is in the SLAVE ACKNOWLEDGE state.

Poll Routine

The poll routine requests all disk drives connected to the channel that have certain interrupts pending to report back to the DCA-2. Before the interrupt request (poll) sequence begins, the IPI-2 interface must be in the IDLE state. The following example is written assuming that the interface is in the SLAVE ACKNOWLEDGE state. The poll routine consists of the following steps:

1.. The DCA2:0 function is executed on both channels to clear the channel busy and channel done flags.

2.. The accumulator is loaded with 0's.

3.. The DCA2:16 function is executed. This function transmits the 0's to the *j* and *k* registers of the 3DF option in the DCA-2.

4.. The accumulator is loaded with 14_8, the sequencer starting address for a deselect sequence (refer to Figure 9-33).

Accumulator Contents

2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
i	i	i	i	i	i	i	i	X	SQ	SQ	SQ	SQ	SQ	SQ	SQ
0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

i = *i* Register Value
X = Not Used
SQ = Sequencer Starting Address

Figure 9-33. Sequencer Starting Address for a Deselect Sequence

5.. The DCA2:5 function is executed. This function signals the sequencer to perform a deselect sequence (refer to Figure 7-10). When the sequence is finished, the IPI-2 interface is in the IDLE state.

6.. The accumulator is loaded with the interrupt request (refer to Table 7-11). Figure 9-34 shows the interrupt request for an RPS interrupt. This request checks whether a disk drive has completed a load position routine.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
k	k	k	k	k	k	k	k	j	j	j	j	j	j	j	j
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

k = *k* Register Value j = *j* Register Value

Figure 9-34. Interrupt Request in the Accumulator

7.. The DCA2:16 function is executed. This function transfers the interrupt request to the *j* register in the 3DF option of the DCA-2.

8.. The accumulator is loaded with a bit-mapped drive address and the sequencer starting address (10_8) of an interrupt request (poll) sequence. Figure 9-35 shows the bit-mapped drive address for logical address 5 and the starting sequencer address for a poll sequence.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
i	i	i	i	i	i	i	i	X	SQ	SQ	SQ	SQ	SQ	SQ	SQ
0	0	1	0	0	0	0	0	x	0	0	0	1	0	0	0

i = *i* Register Value
X = Not Used
SQ = Sequencer Starting Address

Figure 9-35. Sequencer Starting Address for a Poll Sequence

9.. The DCA2:5 function is executed. This function signals the sequencer to perform an interrupt request (poll) sequence (refer to Figure 7-11). When the disk drive with the logical address selected in the *i* register responds, the sequencer returns the IPI-2 interface to the IDLE state.

Write Sector Data Routine

The write sector data routine writes a sector of data to the disk drive and consists of the following steps:

1.. A select unit routine is performed.

2.. A load position routine is performed.

3.. The accumulator is loaded with the cylinder address, ID parameter 0 (refer again to Figure 9-3).

4.. The DCA2:2 function is executed. This function transfers the cylinder address to the cylinder register in the 3DG option of the DCA-2.

5.. The accumulator is loaded with the head and sector address, ID parameter 1 (refer to Figure 9-4).

6.. The DCA2:3 function is executed. This function transfers the head and sector address to the parameter register in the 3DG option of the DCA-2.

7.. The accumulator is loaded with the transfer count. The transfer count for a write sector data routine is the total number of parcels in the ID field, ID error-correction code (ECC) field, data field, defect swallow field, and data ECC field. Figure 9-36 shows the transfer count (20154_8) for a DD-301 disk drive.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T
0	0	1	0	0	0	0	0	0	1	1	0	1	1	0	0

T = Transfer Count in Octal

Figure 9-36. Transfer Count for a DD-301 Disk Drive

8.. The DCA2:4 function is executed. This function transfers the transfer count from the accumulator to the transfer counter in the 3DI option.

9.. The accumulator is loaded with the read header at target and write field bus control commands. The read header at target bus control command is loaded into the *j* register and the write field bus control command into the *k* register (refer to Figure 9-37).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
k	k	k	k	k	k	k	k	j	j	j	j	j	j	j	j
1	0	0	0	0	0	0	1	1	1	0	0	1	1	0	0

k = *k* Register Value j = *j* Register Value

Figure 9-37. Read Header at Target and Write Field Bus Control Codes

10.. The DCA2:16 function is executed. This function transfers the bus control codes to the *j* and *k* registers in the 3DF option of the DCA-2.

11.. The accumulator is loaded with 24_8, the sequencer starting address for a write data sequence (refer to Figure 9-38).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
i	i	i	i	i	i	i	i	X	SQ	SQ	SQ	SQ	SQ	SQ	SQ
0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0

i = *i* Register Value
X = Not Used
SQ = Sequencer Starting Address

Figure 9-38. Sequencer Starting Address for a Write Data Sequence

12.. The DCA2:5 function is executed. This function signals the sequencer to perform a write data sequence, which contains several IPI-2 sequences:

a. The sequencer performs a bus control sequence (refer again to Figure 7-4). During this sequence, the sequencer transfers the contents of the *j* register (read header at target bus control code) to the disk drive.

b. The sequencer performs a noninterlocked transfer-from-disk sequence (refer again to Figure 7-8). During this sequence, the DCA-2 compares the ID field read from the disk drive to the ID parameters stored in the 3DG option.

c. The sequencer performs an ending status sequence (refer to Figure 7-9). During this sequence the DCA-2 and disk drive exchange statuses.

d. The sequencer performs another bus control sequence (refer to Figure 7-4). During this sequence, the sequencer transfers the contents of the *k* register (write data field bus control code) to the disk drive.

e. The sequencer performs a noninterlocked transfer-to-disk sequence (refer to Figure 7-7). During this sequence, the DCA-2 receives a sector of data from the EIOP buffer board and transfers it to the disk drive.

f. The sequencer performs another ending status sequence (refer to Figure 7-9). When finished, the IPI-2 interface is in the SLAVE ACKNOWLEDGE state.

Read Sector Data Routine

The read sector data routine reads a sector of data from the disk drive and consists of the following steps:

1.. A select unit routine is performed.

2.. A load position routine is performed.

3.. The accumulator is loaded with the cylinder address, ID parameter 0. Refer to Figure 9-3.

4.. The DCA2:2 function is executed. This function transfers the cylinder address to the cylinder register in the 3DG option of the DCA-2.

5.. The accumulator is loaded with the head and sector address, ID parameter 1. Refer to Figure 9-4.

6.. The DCA2:3 function is executed. This function transfers the head and sector address to the parameter register in the 3DG option of the DCA-2.

7.. The accumulator is loaded with the transfer count. The transfer count for a read sector data routine is the total number of parcels in the ID field, ID ECC field, data field, defect swallow field, and data ECC field. Figure 9-36 shows the transfer count (20154_8) for a DD-301 disk drive.

8.. The DCA2:4 function is executed. This function transfers the transfer count from the accumulator to the transfer counter in the 3DI option.

9.. The accumulator is loaded with the read header at target (*j* register contents) and read field (*k* register contents) bus control commands. Refer to Figure 9-39.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
k 1	k 1	k 0	k 0	k 0	k 0	k 0	k 1	j 1	j 1	j 0	j 0	j 1	j 1	j 0	j 0

k = *k* Register Value j = *j* Register Value

Figure 9-39. Read Header at Target and Read Field Bus Control Codes

10.. The DCA2:16 function is executed. This function transfers the bus control codes to the *j* and *k* registers in the 3DF option of the DCA-2.

11.. The accumulator is loaded with the sequencer starting address (20_8) for a read data sequence (refer to Figure 9-40).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
i 0	i 0	i 0	i 0	i 0	i 0	i 0	i 0	X 0	SQ 0	SQ 0	SQ 1	SQ 0	SQ 0	SQ 0	SQ 0

i = i Register Value
X = Not Used
SQ = Sequencer Starting Address

Figure 9-40. Sequencer Starting Address for a Read Data Sequence

12.. The DCA2:5 function is executed. This function signals the sequencer to perform a read data sequence, which contains several IPI-2 sequences.

a. The sequencer performs a bus control sequence (refer to Figure 7-4). During this sequence, the sequencer transfers the contents of the *j* register (read header at target bus control code) to the disk drive.

b. The sequencer performs a noninterlocked transfer-from-disk sequence (refer to Figure 7-8). During this sequence, the DCA-2 compares the ID field read from the disk drive to the ID parameters stored in the 3DG option.

c. The sequencer performs an ending status sequence (refer to Figure 7-9). During this sequence, the DCA-2 and disk drive exchange statuses.

d. The sequencer performs another bus control sequence (refer to Figure 7-4). During this sequence, the sequencer transfers the contents of the *k* register (read data field bus control code) to the disk drive.

e. The sequencer performs another noninterlocked transfer-from-disk sequence (refer to Figure 7-8). During this sequence, the DCA-2 receives a sector of data from the disk drive and transfers it to the EIOP buffer board.

f. The sequencer performs another ending status sequence (refer to Figure 7-9). When finished, the IPI-2 interface is in the SLAVE ACKNOWLEDGE state.

10 DCA-3 BASIC THEORY OF OPERATION

The DCA-3 channel adapter is a half-board controller for an array of five IPI-2 disk storage units. Four spindles (spindles 0 through 3) store data and a fifth spindle (spindle 4) stores parity (refer to Figure 10-1).

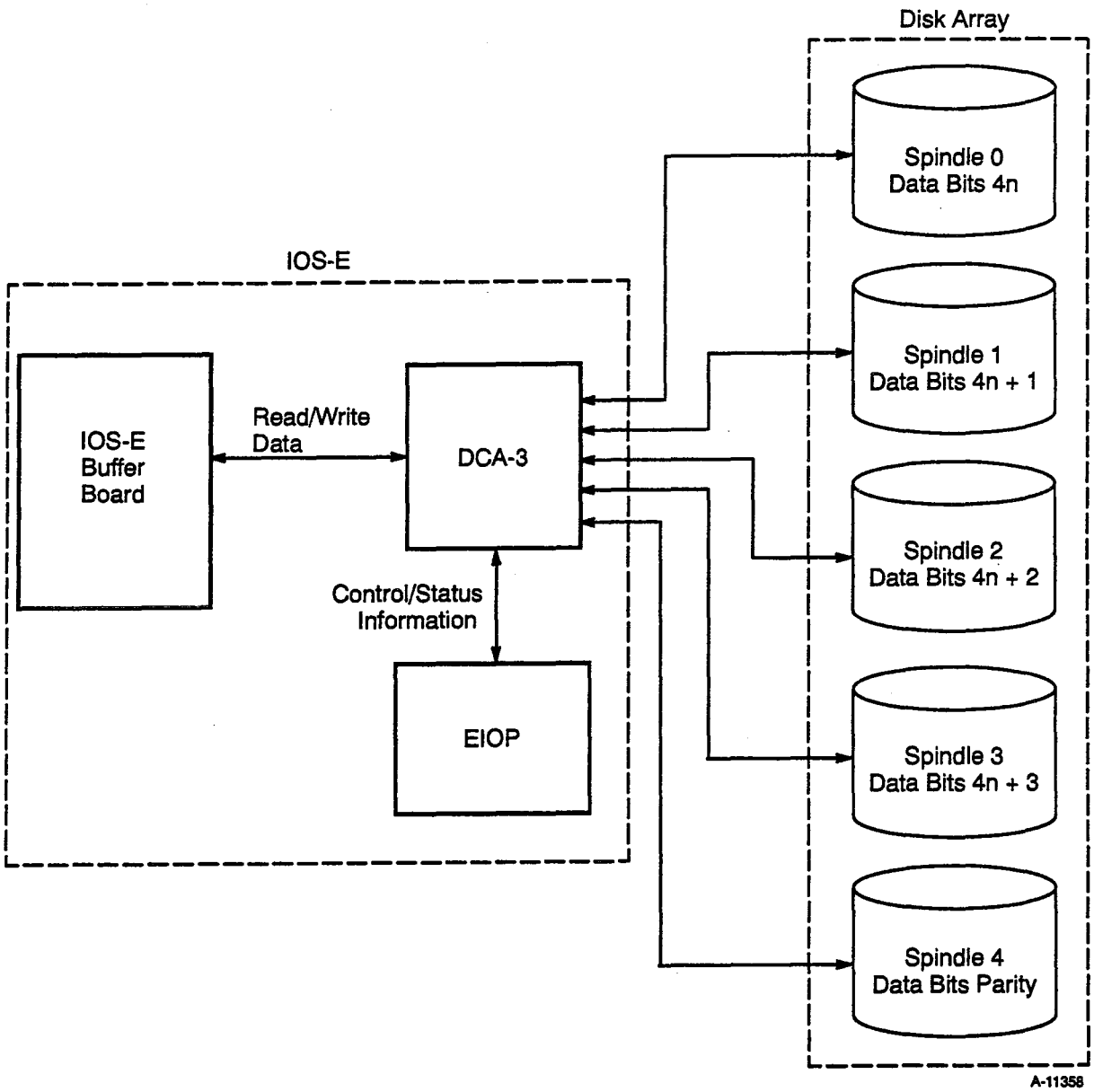


Figure 10-1. Block Diagram of DCA-3 to Disk Array Interface

NOTE: The DCA-3 channel adapter uses data striping as a means of transferring data to the disk array. Data striping is a method by which a Cray word is split into four sections; each section is then sent to a corresponding spindle to be transferred in parallel with the other three sections. This means one striped-data transfer using four spindles completes four times faster than a data transfer using one spindle.

The DCA-3 hardware stripes data from a single I/O buffer path onto the disk array. Spindle 0 stores every fourth bit starting with bit 0, spindle 1 stores every fourth bit starting with bit 1, and so on, for spindles 2 and 3. The parity spindle stores odd parity calculated on each nibble written to the four data spindles. The spindles are synchronized to allow parallel data transfers.

Data buffers on the DCA-3 store 2 Kbytes of data for each spindle of the disk array. The data buffers store at least 75 μsec of data for each spindle, creating a synchronization tolerance of ± 37.5 μsec.

Programming the DCA-3 disk array is similar to programming the DCA-2 single-drive controller. When the DCA-3 issues drive commands such as cylinder seek commands, the disk array operates as a single logical drive. The disk array also operates as a single unit during normal read and write operations. Drive status functions are more complex than those of the DCA-2 because the status from each individual spindle can be unique.

Under normal operation, functions are fanned out to all spindles in the disk array. However, a spindle mask function (DCA3:17, M0 = 1) can be used to select an individual spindle within the array or to deselect an individual spindle within the array.

A single spindle is most often used by diagnostics and utilities for flaw maintenance and troubleshooting. Deselection of a single spindle (i.e., four-spindle mode) is used to recover from single-spindle failures. Data is read from the four active spindles and parity can be used to reconstruct the data from a failed spindle. Data writes can also be done in four-spindle mode. After a failed spindle is replaced, four-spindle mode is used for parity reconstruction of the data to the replacement spindle.

Data Format

The data format of each individual spindle is identical to the format specification of the drives used with the DCA-2. The same ID field, including a defect parameter, is contained in each sector, including 32 bytes of error-correction code (ECC) that protect the data. The parity data on spindle four is also protected by ECC.

The DCA-3 contains 40 ECC generators, eight for each spindle. This provides one generator for each bit within the read and write data bytes. Each ECC generator creates 32 bits of ECC per sector of data. This 32-bit ECC can detect any data bit(s) in error for its read and write path.

A 32-bit ECC provides a 21-bit correction vector and an 11-bit data correction mask field. The 21-bit correction vector field specifies the starting address of the defect. The 11-bit correction mask indicates which bits are in error.

For a write ECC function, the parity spindle stores parity from the ECC data sent to the data spindles in place of a generated ECC. When data is read from four spindles with data reconstruction enabled, the reconstructed data from the parity spindle and the three good data spindles is substituted for the data on the disabled spindle.

DCA-3 Options

The DCA-3 contains 12 options (four option types) that translate EIOP commands into IPI-2 protocol and transfer data between the EIOP and the disk array. These options are described below. Figure 10-2 is a block diagram of the options on the DCA-3.

7DK Option

The 7DK option provides the communication interface to the EIOP. Channel commands are transmitted from the EIOP to the DCA-3 on a 4-bit path. This path is also used by the DCA-3 to transmit status and response data back to the EIOP.

The 7DK option contains a spindle mask register that allows the DCA-3 to determine which spindles in the array are currently active. This mask is set using the DCA3:17 function. Drive commands issued to the DCA-3 are fanned out to all selected spindles. The DCA-3 monitors the done response for selected spindle(s) only. The DCA-3 supports selection of one, four, or five spindles at a time. Any attempt to select two or three spindles constitutes a command error.

SECDED and voltage statuses are monitored within the 7DK option. If a buffer data error occurs during a write to the array, a syndrome value and error count are sent to the 7DK from the 7DL option. Most other DCA-3 status information is delivered to the 7DK via the 6DM options. The DCA-3 statuses are requested via the DCA3:12 and DCA3:13 functions.

The 7DK option contains a transfer length register to set the number of data transfers between the drive and the EIOP buffer board. EIOP buffer board data transfers are controlled by the 7DK via the 7DL option. Transfer counts vary depending on the specific drive function issued. The transfer count values are set using the DCA3:4 function.

7DL Option

The 7DL option provides a hardware interface to the EIOP buffer board. Single-error correction/double-error detection (SECDED) functions are performed by the 7DL option. Data striping, parity generation, parity checking, and data reconstruction are also performed on the 7DL.

During write operations, the 7DL option receives each 72-bit data word from the EIOP buffer board in six 12-bit transfers. Each word contains 64 data bits and 8 check bits. The 7DL generates new check bits for each data word received from the EIOP buffer board. These check bits are compared to the 8 check bits, which arrived with each word. If the bits do not compare, the 7DL signals the 7DK option that a SECDED error has occurred and transfers the error count and syndrome values. If a single bit is corrupted, the 7DL corrects the data by toggling the bit in error.

After SECDED checking occurs on the write data, the 7DL option stripes the data across four paths; each path is assigned to one of the data spindles. Every fourth bit of data, starting with bit 0, is sent to spindle 0 (4n data). Spindle 1 receives every fourth bit starting with bit 1 (4n+1 data), etc. While striping the data, the 7DL generates an odd parity bit for each nibble sent to the data spindles. This nibble parity bit becomes the write data stream for path 4 (parity spindle).

In addition to generating nibble parity, the 7DL option also generates an odd parity bit for each byte of data transferred to the spindles on bus A and bus B. Table 10-1 shows the bit striping and distribution on the DCA-3.

Table 10-1. DCA-3 Disk Array Data Striping

Spindle	Cray Data Word																	
0	P	60	52	44	36	56	48	40	32	P	28	20	12	4	24	16	8	0
1	P	61	53	45	37	57	49	41	33	P	29	21	13	5	25	17	9	1
2	P	62	54	46	38	58	50	42	34	P	30	22	14	6	26	18	10	2
3	P	63	55	47	39	59	51	43	35	P	31	23	15	7	27	19	11	3
4	P	Nibble Parity (ODD)								P	Nibble Parity (ODD)							

Table 10-1. DCA-3 Disk Array Data Striping

Spindle	Cray Data Word			
IPI Bus	P	Bus A (byte 1)	P	Bus B (byte 0)

P = Byte Parity protection for transfer on the IPI Bus

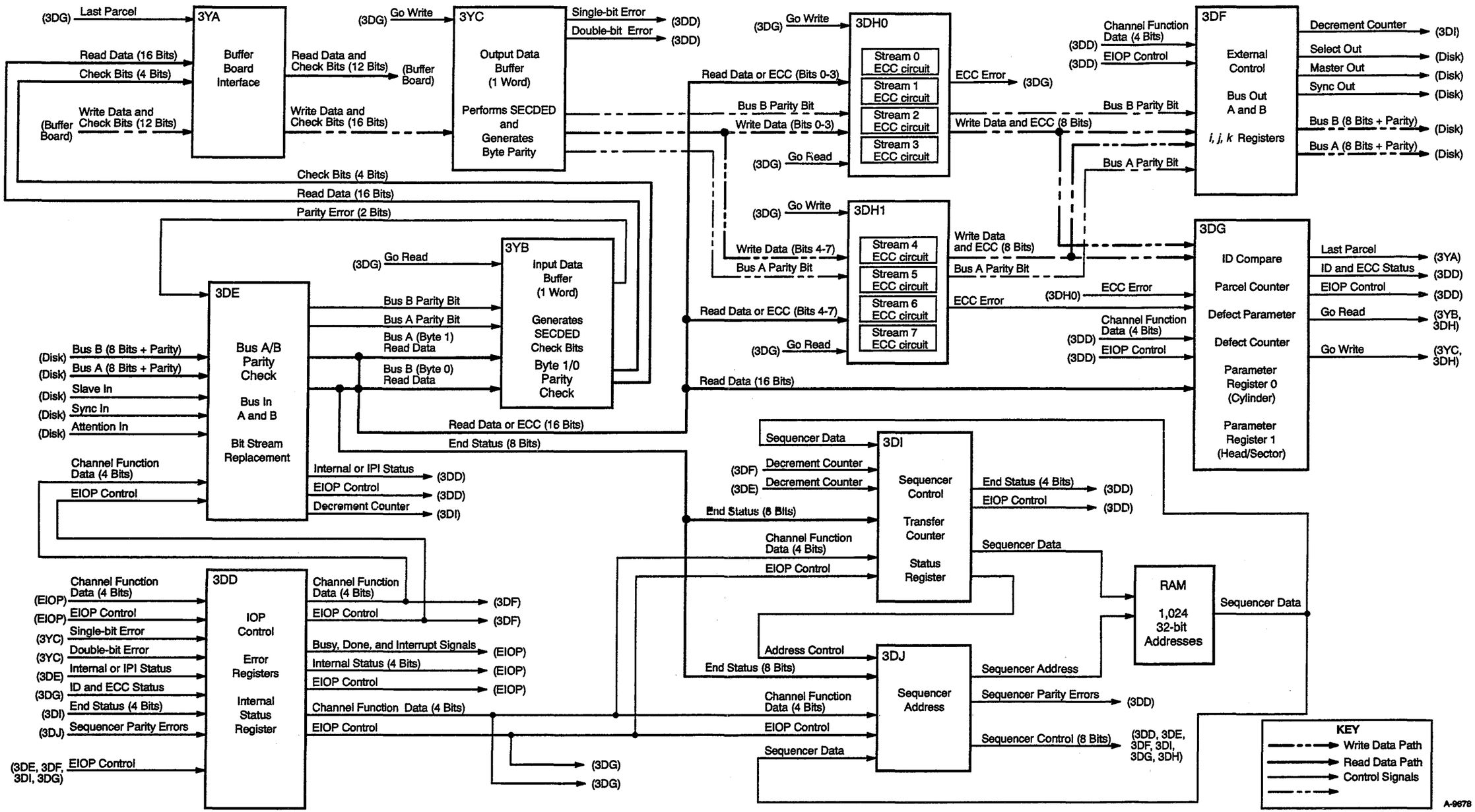


Figure 8-1. DCA-2 Options, Data Paths, and Control Signals

3DF Option

The 3DF option contains signal lines and registers used for IPI-2 information transfers to the disk drive. It also transfers write data from the DCA-2 to the disk drive.

The 3DF option is the IPI-2 communication link for transfers from the DCA-2 to the disk drive. It contains the Select Out, Master Out, Sync Out, Bus A, and Bus B signals used for IPI-2 protocol.

The 3DF option also contains *i*, *j*, and *k* registers, which store IPI commands. Before an information transfer occurs, the *i*, *j*, or *k* registers of the 3DF option are loaded with IPI commands. After receiving a signal from the sequencer (RAM), the 3DF transfers the information stored in the registers to the disk drive over bus A.

During a write data operation, the 3DF receives a parcel of information from the 3DH options. The 3DF option receives bits 2^0 through 2^3 and 2^8 through 2^{11} from 3DH0 and bits 2^4 through 2^7 and 2^{12} through 2^{15} from 3DH1. After receiving the parcel of data, 3DF loads bus B with bits 2^0 through 2^7 and bus A with bits 2^8 through 2^{15}.

The 3DF option also receives two parity bits from the 3DH options. Write data on bus B is protected with the parity bit from 3DH0, and write data on bus A is protected with the parity bit from 3DH1. The 3DF option sends the data and parity bits to the disk drive after it receives them from the 3DH options.

3DE Option

The 3DE option receives IPI-2 control and information transfers from the disk drive. It also receives read data from the disk drive and transfers it to the other options on the DCA-2.

The 3DE option is the IPI-2 communication link for transfers from the disk drive to the DCA-2. It receives the Slave In, Sync In, Bus A, and Bus B signals used for IPI-2 protocol.

During a read data operation, the 3DE receives a byte of data plus a parity bit from both bus A and bus B. After receiving the data and parity bits, the 3DE transfers the information to the 3YB, 3DG, 3DH0, and 3DH1 options. If the read data is ending status or status response information, the 3DE transfers the information from bus B to the 3DJ and 3DI options.

The 3DE option can also perform bit stream replacement, which corrects misread data from a failing head. The 3DE option replaces the data from the failing head with the sum of the data from the other heads and the parity head. The DCA-2:17 channel function transfers the information needed for bit stream replacement to the 3DE. For more information on channel functions, refer to the "DCA-2 Channel Functions" section of this manual.

3YB Option

The 3YB option stores data and generates SECDED check bits during read data operations. It also checks the parity information.

During read data operations, the 3YB receives a word of data from the 3DE option in four 16-bit transfers. While receiving the word of data, the 3YB generates eight SECDED check bits for the word. It sends the word of data to the 3YA option in four 16-bit transfers. During the last two transfers of data, the 3YB sends the check bits in 4-bit transfers.

The 3YB option also generates a new parity bit for each byte of data it receives from the 3DE. If the new parity bit does not match the previous parity bit, the 3YB signals the 3DD that a byte 0 (bus B) or byte 1 (bus A) parity error occurred.

3DG Option

The 3DG option contains registers for comparing the sector ID field to the expected ID field. It also contains counters for counting parcels of information transferred between the DCA-2 and the disk drive.

The parameter register and cylinder register in the 3DG option store sector ID field parameters. The parameter register stores the head, sector, and option bits (ID parameter 1) of the ID field. The cylinder register stores the cylinder address (ID parameter 0) of the ID field. For more information on the sector ID field, refer to the "Format and Flaw Management" disk drive sections of this manual.

The 3DG option also contains a parcel counter and a defect counter. The parcel counter counts each parcel as it is transferred between the DCA-2 and the disk drive. The defect counter is used to create a defect pad that hides media flaws. For more information on media flaws and the defect pad, refer to the "Format and Flaw Management" disk drive sections of this manual.

3DD Option

The 3DD option receives DCA-2 channel functions and transfers control signals between the EIOP and DCA-2. After receiving a DCA-2 channel function from the EIOP, the 3DD transfers the function information to the appropriate options on the DCA-2. The 3DD option also contains registers that store errors and internal status generated by the DCA-2. When requested, the 3DD transfers this status information to the EIOP.

3DI Option

The 3DI option counts the number of information transfers between the EIOP and the DCA-2. It also controls the sequencer address (3DJ option) and sends data to the RAM, hereafter referred to as the sequencer.

The transfer counter in the 3DI option counts the transfers between the EIOP local memory or EIOP buffer board and the DCA-2. Before an information transfer occurs, the transfer counter is loaded with the number of parcels to be transferred. The transfer counter decrements once for each parcel transferred.

The 3DI option also controls the sequencer address. The 3DI option signals the 3DJ option when to reset the sequencer address, when to advance the sequencer address, and when the transfer counter reaches zero.

3DJ Option

The 3DJ option transfers the sequencer address to the sequencer. After receiving the signals from the 3DI option, the 3DJ increments the sequencer address or resets the sequencer address to zero. The 3DJ option also monitors conditions of the other options on the DCA-2 that are used for branch control of the sequencer address.

RAM

The RAM is a sequencer that controls the operation of the DCA-2 registers and IPI-2 signal lines. It contains 1,024 addresses that each hold 32 bits of sequencer data.

After receiving the sequencer address from the 3DJ option, the sequencer transfers the sequencer data to the 3DI and the 3DJ options. As the 3DJ option increments through the addresses of the sequencer, the sequencer data controls when the registers on each option are transferred to signal lines and when the IPI-2 signal lines are set or reset.

The information stored in the RAM may be transferred to the EIOP local memory or written over by information from the EIOP local memory. For more information on loading or reading the sequencer data, refer to the "DCA-2 Channel Functions" section of this manual.

9 DCA-2 CHANNEL FUNCTIONS

Channel functions for the DCA-2 channel adapter load registers in the DCA-2 and auxiliary input/output processor (EIOP) with information for disk drive operations. The channel functions also transfer a sequencer starting address to initiate an IPI-2 bus state sequence. This section describes each channel function and sample disk drive routines.

Channel Function Descriptions

Table 9-1 briefly describes each DCA-2 channel function; the following subsections describe each function in more detail.

Table 9-1. Channel Functions

Function	EIOP Channel	Description
DCA2:0	Even or odd	Clears the channel busy and channel done flags
DCA2:1	Even	Transfers information from the DCA-2 to local memory
DCA2:1	Odd	Transfers information from local memory to the DCA-2
DCA2:2	Even or odd	Loads the cylinder register with ID parameter 0
DCA2:3	Even or odd	Loads the parameter register with ID parameter 1
DCA2:4	Even or odd	Loads the DCA-2 transfer counter with the transfer count
DCA2:5	Even or odd	Transfers information between the DCA-2 and buffer board
DCA2:6	Even or odd	Disables channel interrupts
DCA2:7	Even or odd	Enables channel interrupts
DCA2:10	Even or odd	Reads the channel local memory address register
DCA2:11	Even or odd	Reads the channel parcel counter
DCA2:12	Even or odd	Reads one of four status parcels
DCA2:13	Even or odd	Reads one of three status parcels
DCA2:14	Even or odd	Loads the channel local memory address register
DCA2:15	Even or odd	Loads the channel local memory parcel counter
DCA2:16	Even or odd	Loads the DCA-2 *j* and *k* registers with IPI-2 commands
DCA2:17	Even	Loads the sequencer mode select register
DCA2:17	Odd	Loads the bit stream head select register

DCA2:0 – Clear Channel Busy and Channel Done Flags

The DCA2:0 function resets the EIOP channel busy and channel done flags to 0 or performs a master clear of the channel. The value of the function modifier bits in the *d* field of the EIOP instruction or in the B register on the EIOP selects the operation to be performed (refer to Figure 9-1).

d Field or B Register								
2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
M 2^3	M 2^2	M 2^1	M 2^0	C 2^4	C 2^3	C 2^2	C 2^1	C 2^0

M = Function Modifier Bits
C = Channel Number

Figure 9-1. EIOP Instruction *d* Field or EIOP B Register

If the function modifier bits are set to 0, the function clears the channel busy and channel done flags. The flags cannot be sampled until 8 clock pulses have passed since the function was issued.

If function modifier bits 1, 2, and 3 are set to 1, this function performs a master clear of the DCA-2.

DCA2:1 – Local Memory Input and Output Transfer

The DCA2:1 function transfers the starting address for the sequencer and a value for the *i* register from the accumulator to the DCA-2. This function is used for information transfers between the DCA-2 and EIOP local memory.

Figure 9-2 shows the format of the sequencer starting address and *i* register value in the accumulator. When this function is executed, the DCA-2 loads the *i* register in the 3DF option with the *i* register value and loads the sequencer with the sequencer starting address.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
i 2^7	i 2^6	i 2^5	i 2^4	i 2^3	i 2^2	i 2^1	i 2^0	X x	SQ 2^6	SQ 2^5	SQ 2^4	SQ 2^3	SQ 2^2	SQ 2^1	SQ 2^0

i = *i* Register Value
X = Not Used
SQ = Sequencer Starting Address

Figure 9-2. DCA2:1 Sequencer Starting Address

After receiving the starting address, the sequencer starts an interlocked information transfer. If the DCA2:1 function is executed on the even EIOP channel, the sequencer transfers information from the DCA-2 to local memory. If the function is executed on the odd EIOP channel, the sequencer transfers information from local memory to the DCA-2. The value of the function modifier bits selects the type of information transferred: IPI-2 protocol, sequencer microcode, or the error-correction code (ECC) register contents (refer to Table 9-2).

Table 9-2. Function Modifier Bits

Modifier Bits 2^3	2^2	2^1	2^0	Description
0	0	0	0	IPI-2 protocol transfer from local memory to the disk drive
0	0	0	1	IPI-2 status transfer from the disk drive to local memory
0	0	1	0	Sequencer microcode transfer from local memory to the DCA-2
0	0	1	1	Sequencer microcode transfer from the DCA-2 to local memory
0	1	0	1	ECC register transfer from the DCA-2 to local memory

IPI-2 Protocol Transfers

IPI-2 information is transferred from local memory to the disk drive in an interlocked transfer-to-disk sequence. For an example of this operation, refer to the "Seek Routine" subsection in this section.

IPI-2 status information is transferred from the drive to local memory in an interlocked transfer-from-disk sequence (refer to Figure 7-6). The *i* register value determines what type of status is transferred.

Sequencer Microcode Transfers

All transfers start at the first address of the sequencer and exchange 1,024 32-bit data words. After executing a transfer of sequencer microcode, the DCA2:0 function is executed. This function clears the DCA-2 control logic and direct memory access (DMA) references. The same channel numbering convention is used for the DCA2:0 function as for the DCA2:1 function.

Error-correction Code Register Transfer

During an ECC register transfer, the contents of all eight 4-byte ECC registers are transferred from the 3DH options to local memory.

DCA2:2 – Set ID Parameter 0

The DCA2:2 function transfers the cylinder address (ID parameter 0) from the accumulator to the cylinder register in the 3DG option of the DCA-2. Figure 9-3 shows the format of ID parameter 0 in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
C 2^{15}	C 2^{14}	C 2^{13}	C 2^{12}	C 2^{11}	C 2^{10}	C 2^{9}	C 2^{8}	C 2^{7}	C 2^{6}	C 2^{5}	C 2^{4}	C 2^{3}	C 2^{2}	C 2^{1}	C 2^{0}

C = Cylinder Address (0 - 5062_8)

Figure 9-3. ID Parameter 0 Format

DCA2:3 – Set ID Parameter 1

The DCA2:3 function transfers the sector address, head address, and option bits (ID parameter 1) from the accumulator to the parameter register in the 3DG option of the DCA-2. Figure 9-4 shows the format of ID parameter 1 in the accumulator. Refer to the "Format and Flaw Management" disk drive sections of this manual for more information on the ID information bit descriptions (which include ID parameter 1).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
X	X	WP	RP	X	H	H	H	H	H	S	S	S	S	S	S
x	x	2^{0}	2^{0}	x	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

X = Not Used
WP = Write Protected
RP = Read Protected
H = Head Group Address
S = Sector Address

Figure 9-4. ID Parameter 1 Format

DCA2:4 – Set Transfer Count

The DCA2:4 function transfers the transfer count from the accumulator to the 3DI option in the DCA-2. The transfer count is the total number of parcels to be transferred between the DCA-2 and the disk drive (in octal). Figure 9-5 shows the format of the transfer count in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

T = Transfer Count

Figure 9-5. Transfer Count Format

DCA2:5 – Starting Sequencer Address and *i* Register Value

The DCA2:5 function transfers the starting address for the sequencer and a value for the *i* register from the accumulator to the DCA-2. This function is used for information transfers between the DCA-2 and the EIOP buffer board.

Figure 9-6 shows the format of the sequencer starting address and *i* register value in the accumulator. When this function is executed, the DCA-2 loads the *i* register in the 3DF option with the *i* register value and loads the sequencer with the sequencer starting address.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
i 2^{7}	i 2^{6}	i 2^{5}	i 2^{4}	i 2^{3}	i 2^{2}	i 2^{1}	i 2^{0}	X x	SQ 2^{6}	SQ 2^{5}	SQ 2^{4}	SQ 2^{3}	SQ 2^{2}	SQ 2^{1}	SQ 2^{0}

i = *i* Register Value
X = Not Used
SQ = Sequencer Starting Address

Figure 9-6. DCA2:5 Sequencer Starting Address Format

After receiving the starting address, the sequencer starts an IPI-2 bus state sequence. For an example, refer to the "Write Sector Data Routine" subsection later in this section.

DCA2:6 – Disable Interrupt Enable

The DCA2:6 function sets the EIOP channel enable interrupts flag to 0. When the enable interrupts flag is 0, the channel does not acknowledge any interrupts it receives. This function does not change the states of the channel busy or channel done flags.

DCA2:7 – Enable Interrupt Enable

The DCA2:7 function sets the EIOP channel enable interrupts flag to 1. When the enable interrupts flag is 1, the channel acknowledges any interrupts it receives. This function does not change the states of the channel busy or channel done flags.

DCA2:10 – Read Local Memory Address

The DCA2:10 function transfers the current local memory address from the EIOP channel local memory address register to the accumulator. Figure 9-7 shows the format of the local memory address in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
LM 2^{15}	LM 2^{14}	LM 2^{13}	LM 2^{12}	LM 2^{11}	LM 2^{10}	LM 2^{9}	LM 2^{8}	LM 2^{7}	LM 2^{6}	LM 2^{5}	LM 2^{4}	LM 2^{3}	LM 2^{2}	LM 2^{1}	LM 2^{0}

LM = Current Local Memory Address

Figure 9-7. Current Local Memory Address Format

DCA2:11 – Read Local Memory Parcel Count

The DCA2:11 function transfers the inverse of the EIOP channel parcel counter to the accumulator. To obtain the correct parcel count, the accumulator contents must be inverted. Figure 9-8 shows the format of the inverted parcel count in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
IP 2^{15}	IP 2^{14}	IP 2^{13}	IP 2^{12}	IP 2^{11}	IP 2^{10}	IP 2^{9}	IP 2^{8}	IP 2^{7}	IP 2^{6}	IP 2^{5}	IP 2^{4}	IP 2^{3}	IP 2^{2}	IP 2^{1}	IP 2^{0}

IP = Inverted Parcel Count from the 3DG Option

Figure 9-8. Inverted Parcel Count Format

DCA2:12 – Status Function 0

The DCA2:12 function transfers 1 of 5 status parcels from the DCA-2 to the accumulator. The initial value of the accumulator determines which status parcel is transferred. Figure 9-9 shows the format of the initial accumulator value.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
X	X	X	X	X	X	X	X	X	X	X	X	X	X	ST	ST
x	x	x	x	x	x	x	x	x	x	x	x	x	x	2^{1}	2^{0}

X = Not Used ST = Status Select Bits

Figure 9-9. Status Select Format

Adapter Status

If the status select bits are both 0, the DCA-2 transfers the adapter status to the accumulator. Figure 9-10 shows the format of the adapter status in the accumulator. For more information on status, refer to the "DCA-2 Systems Status" section of this manual.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
SP	SP	SP	SP	V5	V4	DS	SS	CS	CS	CS	CS	CS	CS	CS	CS
2^{3}	2^{2}	2^{1}	2^{0}	2^{0}	2^{0}	2^{0}	2^{0}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

SP = Sequencer Parity Error
V5 = Voltage Fault +5 V
V4 = Voltage Fault –4.5 V
DS = Double-bit Error
SS = Single-bit Error
CS = Channel Adapter Status

Figure 9-10. Adapter Status Format

6X Condition Bits

If the status select bits are both 0 and the sequencer is first given a starting address of 36_8 (using the DCA2:5 function), the DCA-2 transfers the 6X condition bits to the accumulator. Figure 9-11 shows the format of the 6X condition bits in the accumulator. For more information on status, refer to the "DCA-2 Systems Status" section of this manual.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
X x	X x	X x	X x	X x	X x	X x	X x	6X 2^{7}	6X 2^{6}	6X 2^{5}	6X 2^{4}	6X 2^{3}	6X 2^{2}	6X 2^{1}	6X 2^{0}

6X = 6X Condition Bits

Figure 9-11. 6X Condition Bits Format

7X Condition Bits

If the status select bits are both 0 and the sequencer is first given a starting address of 37_8 (using the DCA2:5 function), the DCA-2 transfers the 7X condition bits to the accumulator. Figure 9-12 shows the format of the 7X condition bits in the accumulator. For more information on status, refer to the "DCA-2 Systems Status" section of this manual.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
X x	X x	X x	X x	X x	X x	X x	X x	7X 2^{7}	7X 2^{6}	7X 2^{5}	7X 2^{4}	7X 2^{3}	7X 2^{2}	7X 2^{1}	7X 2^{0}

7X = 7X Condition Bits

Figure 9-12. 7X Condition Bits Format

Syndrome Status

If status select bit 2^1 is 0 and bit 2^0 is 1, the DCA-2 transfers the syndrome status to the accumulator. Figure 9-13 shows the format of the syndrome status in the accumulator. For more information on status, refer to the "DCA-2 Systems Status" section of this manual.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
DC 2^{3}	DC 2^{2}	DC 2^{1}	DC 2^{0}	SC 2^{3}	SC 2^{2}	SC 2^{1}	SC 2^{0}	SY 2^{7}	SY 2^{6}	SY 2^{5}	SY 2^{4}	SY 2^{3}	SY 2^{2}	SY 2^{1}	SY 2^{0}

DC = Double-bit Error Count
SC = Single-bit Error Count
SY = Syndrome Bits

Figure 9-13. Syndrome Status Format

Transfer Count Status

If status select bit 2^1 is 1 and bit 2^0 is 0, the DCA-2 sends the transfer count status to the accumulator. The transfer count is the current value of the transfer counter in the 3DI option of the DCA-2. Figure 9-14 shows the format of the byte count status in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
T 2^{15}	T 2^{14}	T 2^{13}	T 2^{12}	T 2^{11}	T 2^{10}	T 2^9	T 2^8	T 2^7	T 2^6	T 2^5	T 2^4	T 2^3	T 2^2	T 2^1	T 2^0

T = Transfer Count

Figure 9-14. Byte Count Status Format

Tag Status

If both status select bits are 1, the DCA-2 transfers the tag status to the accumulator. Figure 9-15 shows the format of the tag status in the accumulator. For more information on status, refer to the "DCA-2 Systems Status" section of this manual.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{11}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^1
X x	X x	X x	X x	X x	X x	X x	X x	X x	SO 2^0	MO 2^0	SL 2^0	X x	SI 2^0	SV 2^0	AI 2^0

X = Not Used
SO = Sync Out Signal
MO = Master Out Signal
SL = Select Out Signal
SI = Sync In Signal
SV = Slave In Signal
AI = Attention In Signal

Figure 9-15. Tag Status Format

DCA2:13 – Status Function 1

The DCA2:13 function transfers 1 of 3 status parcels to the accumulator. The initial value of the accumulator determines which status parcel is transferred. Figure 9-9 shows the format of the initial accumulator value.

Drive Ending Status

If the status select bits are both 0, the DCA-2 transfers the drive ending status to the accumulator. Figure 9-16 shows the format of the drive ending status in the accumulator. For more information on status, refer to the "DCA-2 Systems Status" section of this manual.

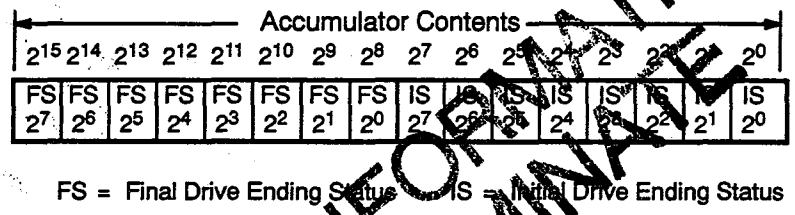


Figure 9-16. Drive Ending Status Format

ID Parameter 0 Status

If status select bit 2^1 is 0 and bit 2^0 is 1, the DCA-2 transfers ID parameter 0 status to the accumulator. ID parameter 0 status is the current value stored in the cylinder register (ID parameter 0) of the 3DG option on the DCA-2. Refer again to Figure 9-3 for the format of ID parameter 0 in the accumulator.

ID Parameter 1 Status

If status select bit 2^1 is 1 and bit 2^0 is 0, the DCA-2 transfers ID parameter 1 status to the accumulator. ID parameter 1 status is the current value stored in the parameter register (ID parameter 1) of the 3DG option on the DCA-2. Refer again to Figure 9-4 for the format of ID parameter 1 in the accumulator.

PRELIMINARY INFORMATION
DO NOT DISSEMINATE

DCA2:14 – Enter Local Memory Starting Address

The DCA2:14 function transfers the local memory starting address from the accumulator to the EIOP channel local memory address register. The local memory starting address is the EIOP local memory address that contains the first parcel of data to be transferred to the DCA-2, or the EIOP local memory address to which the DCA-2 transfers the first parcel of data. Figure 9-17 shows the format of local memory starting address in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
LS 2^{15}	LS 2^{14}	LS 2^{13}	LS 2^{12}	LS 2^{11}	LS 2^{10}	LS 2^{9}	LS 2^{8}	LS 2^{7}	LS 2^{6}	LS 2^{5}	LS 2^{4}	LS 2^{3}	LS 2^{2}	LS 2^{1}	LS 2^{0}

LS = Local Memory Starting Address

Figure 9-17. Local Memory Starting Address Format

During a data transfer, the local memory address register of the channel automatically increments once with each parcel transferred. Execute the DCA2:10 function to transfer the current value of the local memory address register of the channel to the accumulator.

DCA2:15 – Enter Local Memory Parcel Count

The DCA2:15 function transfers the local memory parcel count from the accumulator to the EIOP channel parcel counter. The parcel count is the number of parcels to be transferred between the EIOP local memory and the DCA-2. Figure 9-18 shows the format of the parcel count in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
PC 2^{15}	PC 2^{14}	PC 2^{13}	PC 2^{12}	PC 2^{11}	PC 2^{10}	PC 2^{9}	PC 2^{8}	PC 2^{7}	PC 2^{6}	PC 2^{5}	PC 2^{4}	PC 2^{3}	PC 2^{2}	PC 2^{1}	PC 2^{0}

PC = Parcel Count

Figure 9-18. Parcel Count Format

During a data transfer, the channel parcel counter automatically decrements once for each parcel transferred. Execute the DCA2:11 function to transfer the inverted current value of the channel parcel counter to the accumulator.

DCA2:16 – Enter *j* and *k* Control Register Contents

The DCA2:16 function transfers values for the *j* and *k* registers from the accumulator to the 3DF option in the DCA-2. The *j* and *k* registers store bus control codes or IPI-2 command information bytes. Figure 9-19 shows the format of the *j* and *k* register values in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
k 2^7	k 2^6	k 2^5	k 2^4	k 2^3	k 2^2	k 2^1	k 2^0	j 2^7	j 2^6	j 2^5	j 2^4	j 2^3	j 2^2	j 2^1	j 2^0

k = *k* Register Value j = *j* Register Value

Figure 9-19. *j* and *k* Register Values

The sequencer on the DCA-2 controls when the *j* and *k* register contents are sent to the disk drive over bus A or over both bus A and bus B. For an example of this, refer to the "Write Sector Data Routine" subsection later in this section.

DCA2:17 – Enter Mode Select

The DCA2:17 function performs different operations when it is executed on the even channel than when it is executed on the odd channel. The differences are described below.

Even Channel

When executed on the even channel, the DCA2:17 function transfers sequencer mode bits from the accumulator to the sequencer on the DCA-2. The mode bits can be altered for any function sequence. Figure 9-20 shows the format of the sequencer mode bits in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
X	X	X	X	X	X	X	X	M	M	M	M	M	M	M	M
x	x	x	x	x	x	x	x	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

X = Not Used M = Mode Bits for Sequencer

Figure 9-20. Mode Bits for the Sequencer

The sequencer mode bits abort an executing DCA-2 function, disable ECC circuitry, disable ID compare circuitry, enable bit stream mode, toggle the parity bit, or identify the specific disk drive type. Table 9-3 describes each sequencer mode bit.

Table 9-3. Sequencer Mode Bits

Bit	Name	Description
2^0	Abort	When set to 1, this bit signals the sequencer to terminate its operation. The channel Busy, Done, and Active signals are set to 0. (This bit is used only during an interrupt request (poll) sequence.
2^1	No ECC	When set to 1, this bit signals the sequencer to disable the ECC circuits.
2^2	Read ID	When set to 1, this bit signals the sequencer to transfer the first 4 parcels of ID information to the I/O buffer. This mode bit is used by ID verification utilities.
2^3	Read absolute	When set to 1, this bit signals the sequencer to read the data field without comparing the read ID field to the stored ID parameters.
2^4	Bit stream replacement	When set to 1, this bit signals the sequencer to enter the bit stream replacement mode. This mode is used with the DCA2:17 channel function on the odd channel.
2^5	Toggle parity	When set to 1, this bit signals the sequencer to toggle the parity bit on both buses for read or write operations.
2^6	2-head-parallel disk drive mode	When set to 1, this bit signals the sequencer that it is connected to a 2-head-parallel drive.
2^7	Serial disk drive mode	When set to 1, this bit signals the sequencer that it is connected to a serial disk drive.

Odd Channel

When executed on the odd channel, the DCA2:17 function transfers the lower byte of the accumulator to the bit stream mask register in the sequencer. Figure 9-21 shows the format of the bit stream select bits in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
X x	X x	X x	X x	X x	X x	X x	X x	B 2^{7}	B 2^{6}	B 2^{5}	B 2^{4}	B 2^{3}	B 2^{2}	B 2^{1}	B 2^{0}

X = Not Used B = Bit Stream Select Bits

Figure 9-21. Bit Stream Select Bits

NOTE: When not performing bit stream replacement, the bit stream number register contents must be set to 0's or data will be read incorrectly.

When a bit stream select bit is set to 1, the corresponding bits of bus A and bus B are replaced with a bit stream. The bit stream is calculated by summing the parity stream data with the other seven data streams. This enables data recovery to occur whenever a problem exists under a single head of the disk drive.

Sample Disk Drive Function Routines

Unlike previous Cray Research, Inc. channel adapter functions, DCA-2 channel functions do not correspond one-to-one with disk drive functions. For example, executing the DCA2:2 function (Set ID Parameter 0) does not cause the disk drive to seek to the cylinder address loaded in the accumulator.

Disk drive functions such as select, seek, or read operations are done with a function routine that may contain several channel functions. Generally, function routines consist of the following procedures:

1.. Clearing the channel busy and channel done flags for both EIOP channels.

2.. Loading the EIOP local memory or EIOP buffer board with information for the disk drive operation.

3.. Loading the registers in the DCA-2 with the values needed for the disk drive operation.

4.. Loading the counter registers in the DCA-2 and EIOP channel with the number of parcels to be transferred.

5.. Loading the sequencer with the starting address of the IPI-2 sequence for the disk drive operation.

The following subsections describe sample disk drive function routines. The actual routines and control codes used by the drivers, recovery routines, diagnostics, and utilities may not be the same as the following routines.

Select Unit Routine

The select unit routine logically connects the IOS to a disk drive. The routine consists of the following steps:

1.. The DCA2:0 function is executed on both channels to clear the EIOP channel busy and channel done flags.

2.. The accumulator is loaded with the disk drive address (refer to Table 7-2). Figure 9-22 shows an example of a disk drive address in the accumulator. This example selects the disk drive with the logical address 5. Refer to the "DD-301 Hardware Description" section of this manual for more information on the logical address.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
k	k	k	k	k	k	k	k	j	j	j	j	j	j	j	j
0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0

k = *k* Register Value j = *j* Register Value

Figure 9-22. Disk Drive Address for Logical Address 5

3.. The DCA2:16 function is executed. This function transfers the disk drive address to the *j* register in the 3DF option on the DCA-2.

4.. The accumulator is loaded with 13_8, the starting address of the select disk drive sequence (refer to Figure 9-23).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
i	i	i	i	i	i	i	i	X	SQ	SQ	SQ	SQ	SQ	SQ	SQ
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

i = *i* Register Value
X = Not Used
SQ = Sequencer Starting Address

Figure 9-23. Sequencer Starting Address for Select Disk Drive Sequence

5.. The DCA2:5 function is executed. This function transfers the starting address to the sequencer. After receiving the address, the sequencer performs a select disk drive sequence (refer to Figure 7-3). When the sequence is finished, the IPI-2 interface is in the SLAVE ACKNOWLEDGE state.

The following optional steps verify that the disk drive was successfully selected.

6.. The accumulator is loaded with 00_8, the status select bits for status 01 (refer to Figure 9-24).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
X	X	X	X	X	X	X	X	X	X	X	X	X	X	ST	ST
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

X = Not Used
ST = Status Select Bits

Figure 9-24. Status Select for Status 01

7.. The DCA2:13 function is executed. This function transfers the drive ending status to the accumulator. The ending status for a select disk drive sequence is the drive select response (refer to Table 7-3). Figure 9-25 shows the drive select response for logical address 5 in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
ES	ES	ES	ES	ES	ES	ES	ES	X	X	X	X	X	X	X	X
0	0	1	0	0	0	0	0	x	x	x	x	x	x	x	x

X = Not Used
ES = Ending Status

Figure 9-25. Drive Select Response in the Accumulator

Seek Routine

The seek routine moves the heads to a desired location over the platters. The seek routine consists of the following steps:

1.. A select unit routine is performed.

2.. Two sequential local memory addresses are loaded with data: the first with 0's and the second with the cylinder address (ID parameter 0). Refer to Figure 9-3 for the format of the cylinder address.

3.. The DCA2:0 function is executed on both EIOP channels to clear the channel busy and channel done flags.

4.. The accumulator is loaded with 02_8, the transfer count for a seek routine (refer to Figure 9-26).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

T= Transfer Count

Figure 9-26. Transfer Count for a Seek Routine

5.. The DCA2:4 function is executed. This function transfers the transfer count from the accumulator to the transfer counter in the 3DI option.

6.. The accumulator is loaded with the local memory starting address. The local memory starting address is the address that contains the cylinder address you entered in Step 2.

7.. The DCA2:14 function is executed. This function transfers the local memory starting address to the EIOP channel local memory address register.

8.. The accumulator is loaded with 02_8, the local memory parcel count for a seek routine (refer to Figure 9-27).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 1	PC 0

PC = Parcel Count

Figure 9-27. Parcel Count for a Seek Routine

9.. The DCA2:15 function is executed. This function transfers the parcel count to the EIOP channel's parcel count register.

10.. Bits 2^0 through 2^8 of the accumulator are loaded with the load cylinder bus control code (refer to Figure 9-28).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
k 0	k 0	k 0	k 0	k 0	k 0	k 0	k 0	j 0	j 0	j 0	j 0	j 0	j 1	j 0	j 0

k = *k* Register Value j = *j* Register Value

Figure 9-28. Load Cylinder Bus Control Code

11.. The DCA2:16 function is executed. This function transfers the bus control codes to the *j* and *k* registers in the 3DF option on the DCA-2.

12.. The accumulator is loaded with 04_8, the sequencer starting address for a command load (refer to Figure 9-29).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
i 0	i 0	i 0	i 0	i 0	i 0	i 0	i 0	X 0	SQ 0	SQ 0	SQ 0	SQ 0	SQ 1	SQ 0	SQ 0

i = *i* Register Value
X = Not Used
SQ = Sequencer Starting Address

Figure 9-29. Sequencer Starting Address for Command Load

13.. The DCA2:1 function is executed on the odd channel. This signals the sequencer to perform a bus control sequence (refer to Figure 7-4), an interlocked transfer-to-disk sequence (refer to Figure 7-5), and an ending status sequence (refer to Figure 7-9). When the sequences are finished, the IPI-2 interface is in the SLAVE ACKNOWLEDGE state.

Load Position Routine

The load position routine moves the heads to a desired location over the platters and selects the desired head. The load position routine consists of the following steps:

1.. A select unit routine is performed.

2.. Nine (11_8) sequential local memory addresses are loaded with the rotational position sensing (RPS) parameter. Refer to Table 9-4 for the format of the RPS parameter.

Table 9-4. RPS Parameter Parcel Descriptions

Parcels	Description
0 through 1_8	Cylinder address (ID parameter 0)
2	Head address
3	RPS target sector address
4	RPS pulse width extension
5 through 6_8	RPS pulse width
7 through 10_8	RPS pulse width skew

3.. The DCA2:0 function is executed on both channels to clear the channel's busy and done flags.

4.. The accumulator is loaded with 11_8, the transfer count for a load position routine (refer to Figure 9-30).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

T= Transfer Count

Figure 9-30. Transfer Count for a Load Position Routine

5.. The DCA2:4 function is executed. This function transfers the transfer count from the accumulator to the transfer counter in the 3DI option.

6.. The accumulator is loaded with the local memory starting address. The local memory starting address is the address that contains the parameters entered in Step 2.

7.. The DCA2:14 function is executed. This function transfers the local memory starting address to the EIOP channel local memory address register.

8.. The accumulator is loaded with 11_8, the local memory parcel count for a load position routine (refer to Figure 9-31).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 1	PC 0	PC 0	PC 1

PC = Parcel Count

Figure 9-31. Parcel Count for a Load Position Routine

9.. The DCA2:15 function is executed. This function transfers the parcel count to the EIOP channel's parcel count register.

10.. Bits 2^0 through 2^8 of the accumulator are loaded with the load position bus control code (refer to Figure 9-32).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
k 0	k 0	k 0	k 0	k 0	k 0	k 0	k 0	j 0	j 0	j 0	j 0	j 0	j 1	j 1	j 1

k = *k* Register Value j = *j* Register Value

Figure 9-32. Load Position Bus Control Code

11.. The DCA2:16 function is executed. This function transfers the bus control codes to the *j* and *k* registers in the 3DF option on the DCA-2.

12.. The accumulator is loaded with 04_8, the sequencer starting address for a command load (refer again to Figure 9-29).

13.. The DCA2:1 function is executed on the odd channel. This signals the sequencer to perform a bus control sequence (refer to Figure 7-4), an interlocked transfer-to-disk sequence (refer to Figure 7-5), and an ending status sequence (refer to Figure 7-9). When the sequences are finished, the IPI-2 interface is in the SLAVE ACKNOWLEDGE state.

Poll Routine

The poll routine requests all disk drives connected to the channel that have certain interrupts pending to report back to the DCA-2. Before the interrupt request (poll) sequence begins, the IPI-2 interface must be in the IDLE state. The following example is written assuming that the interface is in the SLAVE ACKNOWLEDGE state. The poll routine consists of the following steps:

1.. The DCA2:0 function is executed on both channels to clear the channel busy and channel done flags.

2.. The accumulator is loaded with 0's.

3.. The DCA2:16 function is executed. This function transmits the 0's to the *j* and *k* registers of the 3DF option in the DCA-2.

4.. The accumulator is loaded with 14_8, the sequencer starting address for a deselect sequence (refer to Figure 9-33).

Accumulator Contents

2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
i	i	i	i	i	i	i	i	X	SQ	SQ	SQ	SQ	SQ	SQ	SQ
0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

i = *i* Register Value
X = Not Used
SQ = Sequencer Starting Address

Figure 9-33. Sequencer Starting Address for a Deselect Sequence

5.. The DCA2:5 function is executed. This function signals the sequencer to perform a deselect sequence (refer to Figure 7-10). When the sequence is finished, the IPI-2 interface is in the IDLE state.

6.. The accumulator is loaded with the interrupt request (refer to Table 7-11). Figure 9-34 shows the interrupt request for an RPS interrupt. This request checks whether a disk drive has completed a load position routine.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
k	k	k	k	k	k	k	k	j	j	j	j	j	j	j	j
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

k = *k* Register Value j = *j* Register Value

Figure 9-34. Interrupt Request in the Accumulator

7.. The DCA2:16 function is executed. This function transfers the interrupt request to the *j* register in the 3DF option of the DCA-2.

8.. The accumulator is loaded with a bit-mapped drive address and the sequencer starting address (10_8) of an interrupt request (poll) sequence. Figure 9-35 shows the bit-mapped drive address for logical address 5 and the starting sequencer address for a poll sequence.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
i	i	i	i	i	i	i	i	X	SQ	SQ	SQ	SQ	SQ	SQ	SQ
0	0	1	0	0	0	0	0	x	0	0	0	1	0	0	0

i = *i* Register Value
X = Not Used
SQ = Sequencer Starting Address

Figure 9-35. Sequencer Starting Address for a Poll Sequence

9.. The DCA2:5 function is executed. This function signals the sequencer to perform an interrupt request (poll) sequence (refer to Figure 7-11). When the disk drive with the logical address selected in the *i* register responds, the sequencer returns the IPI-2 interface to the IDLE state.

Write Sector Data Routine

The write sector data routine writes a sector of data to the disk drive and consists of the following steps:

1.. A select unit routine is performed.

2.. A load position routine is performed.

3.. The accumulator is loaded with the cylinder address, ID parameter 0 (refer again to Figure 9-3).

4.. The DCA2:2 function is executed. This function transfers the cylinder address to the cylinder register in the 3DG option of the DCA-2.

5.. The accumulator is loaded with the head and sector address, ID parameter 1 (refer to Figure 9-4).

6.. The DCA2:3 function is executed. This function transfers the head and sector address to the parameter register in the 3DG option of the DCA-2.

7.. The accumulator is loaded with the transfer count. The transfer count for a write sector data routine is the total number of parcels in the ID field, ID error-correction code (ECC) field, data field, defect swallow field, and data ECC field. Figure 9-36 shows the transfer count (20154_8) for a DD-301 disk drive.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T
0	0	1	0	0	0	0	0	0	1	1	0	1	1	0	0

T = Transfer Count in Octal

Figure 9-36. Transfer Count for a DD-301 Disk Drive

8.. The DCA2:4 function is executed. This function transfers the transfer count from the accumulator to the transfer counter in the 3DI option.

9.. The accumulator is loaded with the read header at target and write field bus control commands. The read header at target bus control command is loaded into the *j* register and the write field bus control command into the *k* register (refer to Figure 9-37).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
k	k	k	k	k	k	k	k	j	j	j	j	j	j	j	j
1	0	0	0	0	0	0	1	1	1	0	0	1	1	0	0

k = *k* Register Value j = *j* Register Value

Figure 9-37. Read Header at Target and Write Field Bus Control Codes

10.. The DCA2:16 function is executed. This function transfers the bus control codes to the *j* and *k* registers in the 3DF option of the DCA-2.

11.. The accumulator is loaded with 24_8, the sequencer starting address for a write data sequence (refer to Figure 9-38).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
i	i	i	i	i	i	i	i	X	SQ	SQ	SQ	SQ	SQ	SQ	SQ
0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0

i = *i* Register Value
X = Not Used
SQ = Sequencer Starting Address

Figure 9-38. Sequencer Starting Address for a Write Data Sequence

12.. The DCA2:5 function is executed. This function signals the sequencer to perform a write data sequence, which contains several IPI-2 sequences:

a. The sequencer performs a bus control sequence (refer again to Figure 7-4). During this sequence, the sequencer transfers the contents of the *j* register (read header at target bus control code) to the disk drive.

b. The sequencer performs a noninterlocked transfer-from-disk sequence (refer again to Figure 7-8). During this sequence, the DCA-2 compares the ID field read from the disk drive to the ID parameters stored in the 3DG option.

c. The sequencer performs an ending status sequence (refer to Figure 7-9). During this sequence the DCA-2 and disk drive exchange statuses.

d. The sequencer performs another bus control sequence (refer to Figure 7-4). During this sequence, the sequencer transfers the contents of the *k* register (write data field bus control code) to the disk drive.

e. The sequencer performs a noninterlocked transfer-to-disk sequence (refer to Figure 7-7). During this sequence, the DCA-2 receives a sector of data from the EIOP buffer board and transfers it to the disk drive.

f. The sequencer performs another ending status sequence (refer to Figure 7-9). When finished, the IPI-2 interface is in the SLAVE ACKNOWLEDGE state.

Read Sector Data Routine

The read sector data routine reads a sector of data from the disk drive and consists of the following steps:

1.. A select unit routine is performed.

2.. A load position routine is performed.

3.. The accumulator is loaded with the cylinder address, ID parameter 0. Refer to Figure 9-3.

4.. The DCA2:2 function is executed. This function transfers the cylinder address to the cylinder register in the 3DG option of the DCA-2.

5.. The accumulator is loaded with the head and sector address, ID parameter 1. Refer to Figure 9-4.

6.. The DCA2:3 function is executed. This function transfers the head and sector address to the parameter register in the 3DG option of the DCA-2.

7.. The accumulator is loaded with the transfer count. The transfer count for a read sector data routine is the total number of parcels in the ID field, ID ECC field, data field, defect swallow field, and data ECC field. Figure 9-36 shows the transfer count (20154_8) for a DD-301 disk drive.

8.. The DCA2:4 function is executed. This function transfers the transfer count from the accumulator to the transfer counter in the 3DI option.

9.. The accumulator is loaded with the read header at target (*j* register contents) and read field (*k* register contents) bus control commands. Refer to Figure 9-39.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
k 1	k 1	k 0	k 0	k 0	k 0	k 0	k 1	j 1	j 1	j 0	j 0	j 1	j 1	j 0	j 0

k = *k* Register Value j = *j* Register Value

Figure 9-39. Read Header at Target and Read Field Bus Control Codes

10.. The DCA2:16 function is executed. This function transfers the bus control codes to the *j* and *k* registers in the 3DF option of the DCA-2.

11.. The accumulator is loaded with the sequencer starting address (20_8) for a read data sequence (refer to Figure 9-40).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
i 0	i 0	i 0	i 0	i 0	i 0	i 0	i 0	X 0	SQ 0	SQ 0	SQ 1	SQ 0	SQ 0	SQ 0	SQ 0

i = i Register Value
X = Not Used
SQ = Sequencer Starting Address

Figure 9-40. Sequencer Starting Address for a Read Data Sequence

12.. The DCA2:5 function is executed. This function signals the sequencer to perform a read data sequence, which contains several IPI-2 sequences.

a. The sequencer performs a bus control sequence (refer to Figure 7-4). During this sequence, the sequencer transfers the contents of the *j* register (read header at target bus control code) to the disk drive.

b. The sequencer performs a noninterlocked transfer-from-disk sequence (refer to Figure 7-8). During this sequence, the DCA-2 compares the ID field read from the disk drive to the ID parameters stored in the 3DG option.

c. The sequencer performs an ending status sequence (refer to Figure 7-9). During this sequence, the DCA-2 and disk drive exchange statuses.

d. The sequencer performs another bus control sequence (refer to Figure 7-4). During this sequence, the sequencer transfers the contents of the *k* register (read data field bus control code) to the disk drive.

e. The sequencer performs another noninterlocked transfer-from-disk sequence (refer to Figure 7-8). During this sequence, the DCA-2 receives a sector of data from the disk drive and transfers it to the EIOP buffer board.

f. The sequencer performs another ending status sequence (refer to Figure 7-9). When finished, the IPI-2 interface is in the SLAVE ACKNOWLEDGE state.

10 DCA-3 BASIC THEORY OF OPERATION

The DCA-3 channel adapter is a half-board controller for an array of five IPI-2 disk storage units. Four spindles (spindles 0 through 3) store data and a fifth spindle (spindle 4) stores parity (refer to Figure 10-1).

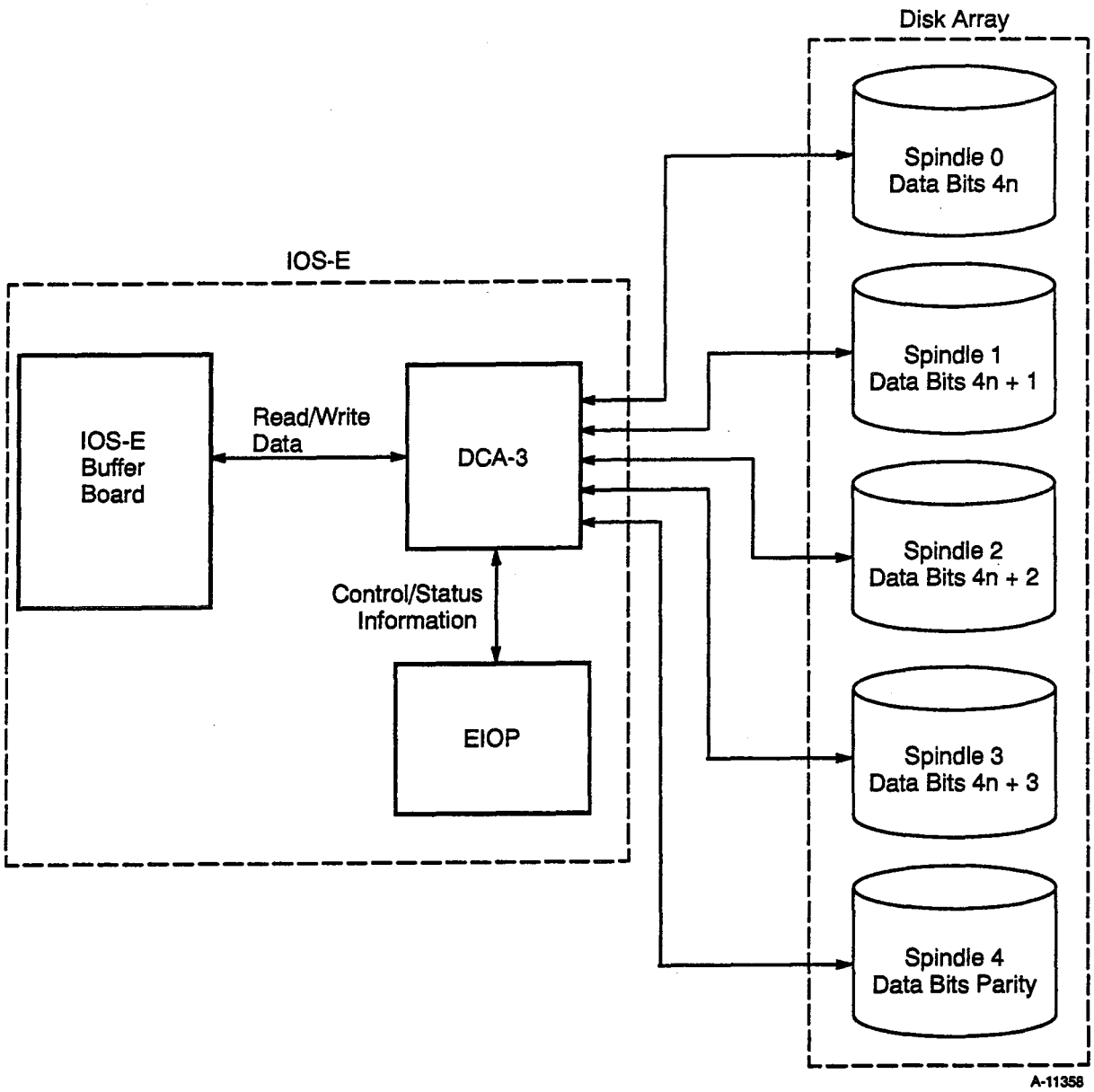


Figure 10-1. Block Diagram of DCA-3 to Disk Array Interface

NOTE: The DCA-3 channel adapter uses data striping as a means of transferring data to the disk array. Data striping is a method by which a Cray word is split into four sections; each section is then sent to a corresponding spindle to be transferred in parallel with the other three sections. This means one striped-data transfer using four spindles completes four times faster than a data transfer using one spindle.

The DCA-3 hardware stripes data from a single I/O buffer path onto the disk array. Spindle 0 stores every fourth bit starting with bit 0, spindle 1 stores every fourth bit starting with bit 1, and so on, for spindles 2 and 3. The parity spindle stores odd parity calculated on each nibble written to the four data spindles. The spindles are synchronized to allow parallel data transfers.

Data buffers on the DCA-3 store 2 Kbytes of data for each spindle of the disk array. The data buffers store at least 75 μsec of data for each spindle, creating a synchronization tolerance of ± 37.5 μsec.

Programming the DCA-3 disk array is similar to programming the DCA-2 single-drive controller. When the DCA-3 issues drive commands such as cylinder seek commands, the disk array operates as a single logical drive. The disk array also operates as a single unit during normal read and write operations. Drive status functions are more complex than those of the DCA-2 because the status from each individual spindle can be unique.

Under normal operation, functions are fanned out to all spindles in the disk array. However, a spindle mask function (DCA3:17, M0 = 1) can be used to select an individual spindle within the array or to deselect an individual spindle within the array.

A single spindle is most often used by diagnostics and utilities for flaw maintenance and troubleshooting. Deselection of a single spindle (i.e., four-spindle mode) is used to recover from single-spindle failures. Data is read from the four active spindles and parity can be used to reconstruct the data from a failed spindle. Data writes can also be done in four-spindle mode. After a failed spindle is replaced, four-spindle mode is used for parity reconstruction of the data to the replacement spindle.

Data Format

The data format of each individual spindle is identical to the format specification of the drives used with the DCA-2. The same ID field, including a defect parameter, is contained in each sector, including 32 bytes of error-correction code (ECC) that protect the data. The parity data on spindle four is also protected by ECC.

The DCA-3 contains 40 ECC generators, eight for each spindle. This provides one generator for each bit within the read and write data bytes. Each ECC generator creates 32 bits of ECC per sector of data. This 32-bit ECC can detect any data bit(s) in error for its read and write path.

A 32-bit ECC provides a 21-bit correction vector and an 11-bit data correction mask field. The 21-bit correction vector field specifies the starting address of the defect. The 11-bit correction mask indicates which bits are in error.

For a write ECC function, the parity spindle stores parity from the ECC data sent to the data spindles in place of a generated ECC. When data is read from four spindles with data reconstruction enabled, the reconstructed data from the parity spindle and the three good data spindles is substituted for the data on the disabled spindle.

DCA-3 Options

The DCA-3 contains 12 options (four option types) that translate EIOP commands into IPI-2 protocol and transfer data between the EIOP and the disk array. These options are described below. Figure 10-2 is a block diagram of the options on the DCA-3.

7DK Option

The 7DK option provides the communication interface to the EIOP. Channel commands are transmitted from the EIOP to the DCA-3 on a 4-bit path. This path is also used by the DCA-3 to transmit status and response data back to the EIOP.

The 7DK option contains a spindle mask register that allows the DCA-3 to determine which spindles in the array are currently active. This mask is set using the DCA3:17 function. Drive commands issued to the DCA-3 are fanned out to all selected spindles. The DCA-3 monitors the done response for selected spindle(s) only. The DCA-3 supports selection of one, four, or five spindles at a time. Any attempt to select two or three spindles constitutes a command error.

SECDED and voltage statuses are monitored within the 7DK option. If a buffer data error occurs during a write to the array, a syndrome value and error count are sent to the 7DK from the 7DL option. Most other DCA-3 status information is delivered to the 7DK via the 6DM options. The DCA-3 statuses are requested via the DCA3:12 and DCA3:13 functions.

The 7DK option contains a transfer length register to set the number of data transfers between the drive and the EIOP buffer board. EIOP buffer board data transfers are controlled by the 7DK via the 7DL option. Transfer counts vary depending on the specific drive function issued. The transfer count values are set using the DCA3:4 function.

7DL Option

The 7DL option provides a hardware interface to the EIOP buffer board. Single-error correction/double-error detection (SECDED) functions are performed by the 7DL option. Data striping, parity generation, parity checking, and data reconstruction are also performed on the 7DL.

During write operations, the 7DL option receives each 72-bit data word from the EIOP buffer board in six 12-bit transfers. Each word contains 64 data bits and 8 check bits. The 7DL generates new check bits for each data word received from the EIOP buffer board. These check bits are compared to the 8 check bits, which arrived with each word. If the bits do not compare, the 7DL signals the 7DK option that a SECDED error has occurred and transfers the error count and syndrome values. If a single bit is corrupted, the 7DL corrects the data by toggling the bit in error.

After SECDED checking occurs on the write data, the 7DL option stripes the data across four paths; each path is assigned to one of the data spindles. Every fourth bit of data, starting with bit 0, is sent to spindle 0 (4n data). Spindle 1 receives every fourth bit starting with bit 1 (4n+1 data), etc. While striping the data, the 7DL generates an odd parity bit for each nibble sent to the data spindles. This nibble parity bit becomes the write data stream for path 4 (parity spindle).

In addition to generating nibble parity, the 7DL option also generates an odd parity bit for each byte of data transferred to the spindles on bus A and bus B. Table 10-1 shows the bit striping and distribution on the DCA-3.

Table 10-1. DCA-3 Disk Array Data Striping

Spindle	Cray Data Word																	
0	P	60	52	44	36	56	48	40	32	P	28	20	12	4	24	16	8	0
1	P	61	53	45	37	57	49	41	33	P	29	21	13	5	25	17	9	1
2	P	62	54	46	38	58	50	42	34	P	30	22	14	6	26	18	10	2
3	P	63	55	47	39	59	51	43	35	P	31	23	15	7	27	19	11	3
4	P	Nibble Parity (ODD)								P	Nibble Parity (ODD)							

Table 10-1. DCA-3 Disk Array Data Striping

Spindle	Cray Data Word			
IPI Bus	P	Bus A (byte 1)	P	Bus B (byte 0)

P = Byte Parity protection for transfer on the IPI Bus

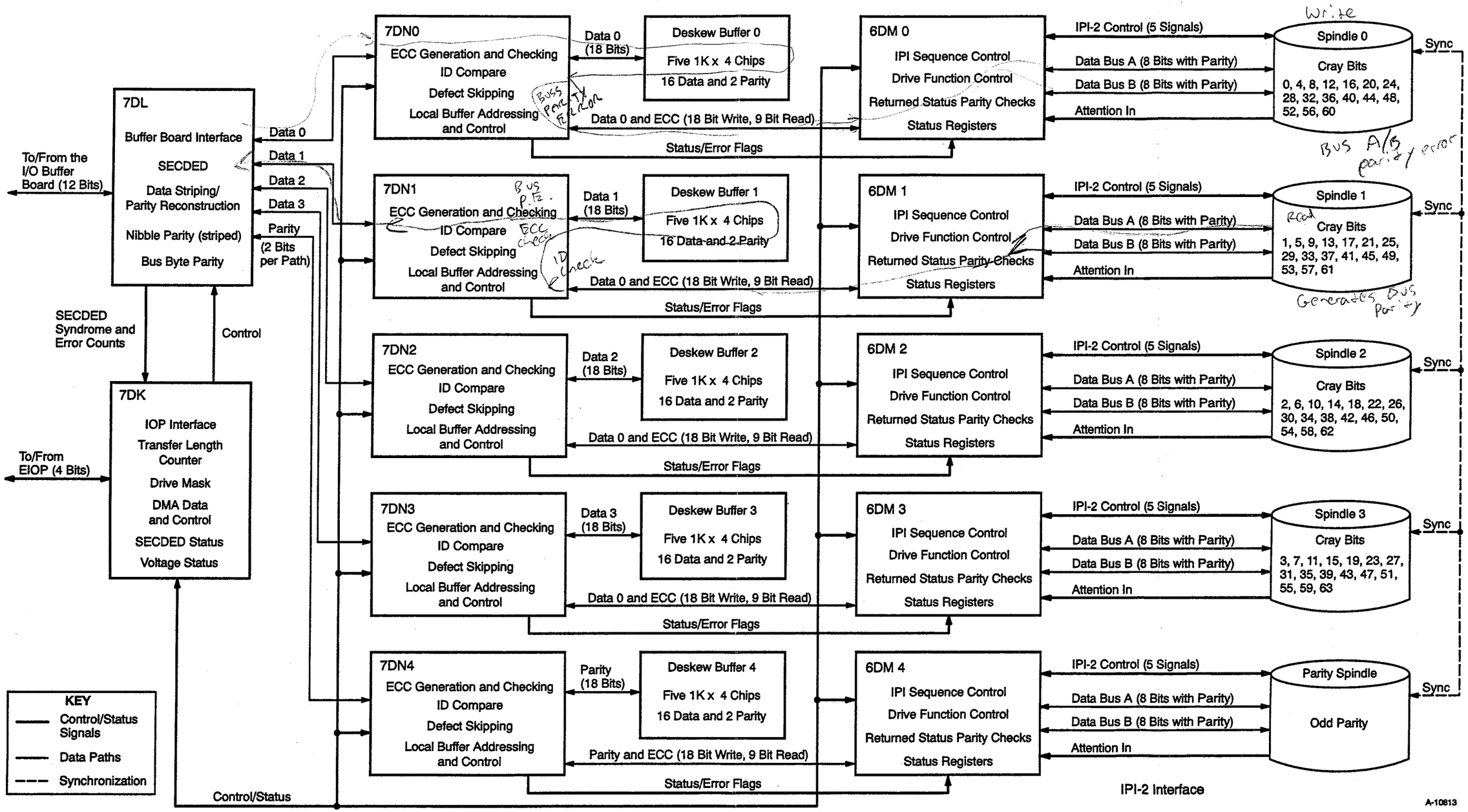


Figure 10-2. DCA-3 Block Diagram

During read operations, the 7DL option receives data from each selected spindle through the appropriate 7DN options. Parity checking is performed on each nibble of striped data using the information read from the parity spindle. Nibble parity errors are flagged by setting bit 7 of the interrupt status parcel (data parity error).

If a nibble parity error occurs, ECC and status information can be examined to determine which spindle within the array returned the corrupted data. Once the spindle (data stream) is identified, information read from the parity spindle can be used to reconstruct the corrupted data stream. If a spindle within the array is disabled, the 7DL option automatically uses the information from the parity spindle to reconstruct data from the disabled spindle until it is enabled again.

Once parity checking and/or data reconstruction is complete, the 7DL option generates 8 check bits for each 64-bit word to be transmitted to the EIOP buffer board. Each 72-bit word is then sent to the buffer board in six 12-bit transfers.

7DN Options

Five 7DN options reside on the DCA-3, each assigned to handle data for one of the five spindles. Each 7DN option receives write/read data and caches the data in a dedicated deskew buffer. At the appropriate time, the 7DN reads the data from the deskew buffer for transfer to the next option.

Each 7DN option performs most of the functions of an entire DCA-2 channel adapter. The 7DN options handle control of the deskew buffers, ID compare, ECC generation and checking, and defect skipping.

Under normal operations, the read and compare of sector ID field information must precede the transfer of customer data. The ID field data is received by the 7DN options and compared to expected values held in parameter registers 0 and 1. If the actual ID data does not match the expected values, an ID compare error is flagged by setting bit 8 of the interrupt status. In addition, ECC checking is also performed on the ID field data. All ECC errors are flagged by setting bit 9 of the interrupt status. Refer to the "DCA-3 Systems Status" section of this manual for additional status information.

During write operations, each 7DN option receives write data from the 7DL option in 2-bit transfers. The 7DN assembles the data into 2-byte parcels including the parity bit on each byte. The 7DN stores each parcel (16 data bits and 2 parity bits) to a unique location in its associated deskew buffer starting at address location 0. When the spindle is ready to

receive write data, the 7DN reads the data from the deskew buffer for transfer to the disk via the respective 6DM option. As the data is read out of the deskew buffer, each byte is striped across eight ECC circuits in the 7DN option; ECC0 receives bit 0 of each byte, EEC1 receives bit 1 of each byte, and so on. ECC generation is not performed on the byte parity bits read from the deskew buffer; however, the 7DN4 option can generate ECC protection on the nibble parity data for transfer to the parity spindle. Each of the eight ECC circuits generates a 32-bit ECC code.

Defect pad detection and skipping is also performed by the 7DN options. The defect address from a spindle sector is read into the respective 7DN as part of the ID field. When the spindle head is at the beginning of the defect pad, the 7DN stops incrementing the deskew buffer addressing and starts decrementing a defect counter to count the length of the defect pad. While the head crosses over the defect pad, the 7DN repeats (stutters) the next valid parcel of data to create the defect pad. When the defect counter has decremented to 0, indicating the end of the defect area, the 7DN resumes reading valid write data from the deskew buffer for transfer to the spindle.

During read operations, each 7DN option receives read data parcels from its associated 6DM option in two 9-bit transfers (8 data bits plus parity). Each data parcel is written to the deskew buffer along with two parity bits. At the proper time, the data parcels are read out of the buffer and parity checking is performed on each byte of data. Byte parity errors are flagged by setting bit 0 of the interrupt status parcel (drive parity error).

Following the parity check, each byte is striped across the eight ECC circuits for regeneration of the 32-bit protection code. At the completion of the data transfer, the regenerated ECC is compared to the ECC information read from the spindle. If the ECC information does not compare, the error is flagged by bit 9 of the interrupt status (ECC error). After the data ECC is checked, the read data from each of the 7DN options is sent to the 7DL option in 2-bit transfers. The DCA3:1 channel function is used to examine all ECC registers to determine which data stream is in error.

Deskew Buffers

The DCA-3 includes five deskew buffers that provide data buffering for each of the spindle data paths. All control and addressing of the deskew buffers is performed by the respective 7DN options. Each buffer comprises five memory chips. Each chip contains 1024 addresses; each address holds four bits of data. Four of these chips hold read/write data, and the fifth chip stores the two parity bits. Each deskew buffer stores up

to 75 μs of data, allowing a total synchronization tolerance of ± 37.5 μs between spindles. This tolerance also allows the DCA-3 to handle defect skipping individually for each spindle. For example, data transfers can occur on four of the spindles while a defect pad is being skipped on the fifth.

6DM options

The DCA-3 contains five 6DM options, one for each of the spindles of the array. The 6DM options maintain the IPI protocol and sequencing between the DCA-3 and the spindles. Unlike the DCA-2, there is no microcode firmware on the DCA-3; sequencing is performed by the design logic. Most error conditions detected by the 7DN options are reported to status registers in the 6DM options. These statuses are subsequently transferred to the channel via the 7DK option. The 6DM options also perform parity checking on the IPI buses during ending status sequences and other non-data transfers. All read data destined for the EIOP buffer board is passed through the 6DM options without a parity check. Parity checking for read data is performed by the 7DL option.

During write operations, each 6DM option receives write data parcels in two 9-bit transfers (8 data bits plus parity) from the associated 7DN option. The 6DM transfers each parcel of data to the spindle by placing the even byte (0) on bus B and the odd byte (1) on bus A. Each transfer on the buses is accompanied by a Sync Out pulse.

During read operations, each 6DM option receives a parcel of data on each transfer from the spindle; an even byte arrives on bus B while the odd byte arrives on bus A. Each byte transferred on the A and B buses is accompanied by a parity bit. The 6DM transfers the read data parcels to the respective 7DN option in two 9-bit transfers (8 data bits plus parity).

DCA-3 Handling Precautions

The DCA-3 channel adapter is fragile and must be handled with extreme care. Observe all precautions to ensure that nothing comes in contact with the surface of this half-board. Handle the DCA-3 by the edge connectors only and observe all electrostatic discharge (ESD) precautions. Refer to Figure 11–3 for information on the physical layout of the DCA-3 channel adapter.

Table 10-2. DCA-3 to DA-60 Data Bit Distribution

Spindle	Cray Data Word																
0	60	52	44	36	56	48	40	32	28	20	12	4	24	16	8	0	
1	61	53	45	37	57	49	41	33	29	21	13	5	25	17	9	1	
2	62	54	46	38	58	50	42	34	30	22	14	6	26	18	10	2	
3	63	55	47	39	59	51	43	35	31	23	15	7	27	19	11	3	
4	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	
Head in 8-head group	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
IPI bus	BUS A (byte 1)								BUS B (byte 0)								Byte Parity
Memory chip location for spindle 0 data	AAE3				AAE2				AAE1				AAE0				AAE4
Memory chip location for spindle 1 data	ACB3				ACB2				ACB1				ACB0				ACB4
Memory chip location for spindle 2 data	AEB3				AEB2				AEB1				AEB0				AEB4
Memory chip location for spindle 3 data	AFB3				AFB2				AFB1				AFB0				AFB4
Memory chip location for spindle 4 data	AAB3				AAB2				AAB1				AAB0				AAB4

Table 10-3. DCA-3 to DA-62 Data Bit Distribution

Spindle	Cray Data Word																
0	60	52	44	36	56	48	40	32	28	20	12	4	24	16	8	0	
1	61	53	45	37	57	49	41	33	29	21	13	5	25	17	9	1	
2	62	54	46	38	58	50	42	34	30	22	14	6	26	18	10	2	
3	63	55	47	39	59	51	43	35	31	23	15	7	27	19	11	3	
4	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	
Head in 2-head group	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	
IPI bus	BUS A (byte 1)								BUS B (byte 0)								Buffer Parity
Memory chip location for spindle 0 data	AAE3				AAE2				AAE1				AAE0				AAE4
Memory chip location for spindle 1 data	ACB3				ACB2				ACB1				ACB0				ACB4
Memory chip location for spindle 2 data	AEB3				AEB2				AEB1				AEB0				AEB4
Memory chip location for spindle 3 data	AFB3				AFB2				AFB1				AFB0				AFB4
Memory chip location for spindle 4 data	AAB3				AAB2				AAB1				AAB0				AAB4

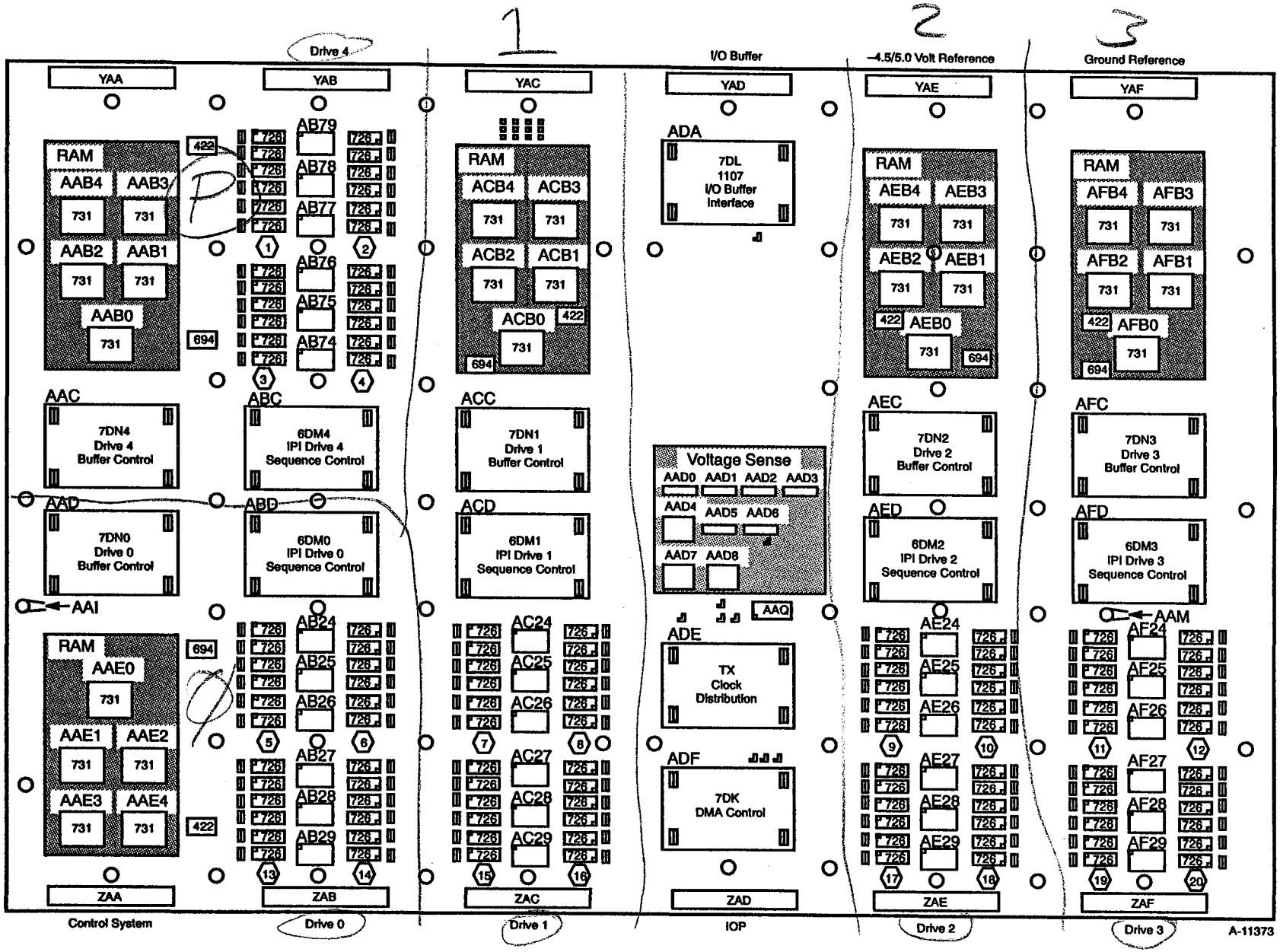


Figure 11–3. DCA-3 Board Assembly

11 DCA-3 CHANNEL FUNCTIONS

Channel functions for the DCA-3 channel adapter transfer information for disk array operations to registers in the DCA-3 and input/output processor (EIOP). This section describes each channel function.

Channel Function Descriptions

Table 11-1 lists the DCA-3 channel functions and describes them briefly.

Table 11-1. DCA-3 Channel Functions

Function	Description
DCA3:0	Clear channel flags
DCA3:1	Start Transfer Start input transfer (even channel) M3, M2, M1, M0 = 0001: Read drive response M3, M2, M1, M0 = 0101: Read ECC registers Start output transfer (odd channel) M3, M2, M1, M0 = 0000: Write drive command
DCA3:2	Set ID parameter 0 (cylinder address)
DCA3:3	Set ID parameter 1 (head and sector address)
DCA3:4	Set transfer count
DCA3:5	Start device function
DCA3:6	Clear interrupt enable flag
DCA3:7	Set interrupt enable flag
DCA3:10	Read local memory address
DCA3:11	Read inverted local memory parcel count
DCA3:12	Read status 0
DCA3:13	Read status 1
DCA3:14	Set local memory starting address
DCA3:15	Set local memory parcel count
DCA3:16	Write control bus data
DCA3:17	M0 = 0: Set Array Type M0 = 1: Set Array Mode

Except for DCA3:1, functions of an even channel with M0=0 are functions to the a-pointer and functions to an odd channel with M0=1 are functions to the b-pointer. Figure 11-1 shows the bit assignments for the modifier (M) bits and channel number in the *d* field or B Register.

d Field or B Register								
2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
M 2^3	M 2^2	M 2^1	M 2^0	C 2^4	C 2^3	C 2^2	C 2^1	C 2^0

M = Function Modifier Bits
C = Channel Number

Figure 11-1. EIOP Instruction *d* Field or EIOP B Register

DCA3:0 – Clear Channel Flags

The DCA3:0 function resets the EIOP channel busy and channel done flags to 0 or performs a master clear of the channel.

Channel function DCA3:0 also clears the following status bits:

- Interrupt status bits 2^0 through 2^3 and bits 2^6 through 2^{10}
- SECDED status bits 2^8 through 2^{15}
- All drive busy, drive done, and DMA acknowledge pending bits

DCA3:1 - Start Transfer

The DCA3:1 function starts data transfers between the EIOP local memory and the DCA-3 channel adapter. The condition of function modifier bit 0 determines the direction of the transfer; bits 1 through 3 determine the type of transfer. Refer to Table 11-2 for a list of the modifier bit values used with the DCA3:1 function.

DCA3:1 - Start Input Transfer (even channel)

This function initiates a data transfer from the channel adapter to EIOP local memory. Modifier bit M0 must be set to 1. Bit M2 determines what data is transferred (refer again to Table 11-2).

Table 11-2. DCA3:1 Function Modifier Bits

Modifier Bits 2^3	2^2	2^1	2^0	Description
0	0	0	0	Drive command control function (odd channel)
0	0	0	1	Drive response function (even channel)
0	1	0	1	Read ECC register (even channel)

The even channel operation of this function (for both defined combinations) is as follows:

M3	M2	M1	M0	Operation
0	0	0	1	Drive response function. This function is an interlocked transfer and provides command status information. The lower four bits of the accumulator must be 6_8 (refer to Figure 11-2). The lower byte of the previous DCA3:16 function sent to the odd channel is a response control byte sent to all spindles, which causes them to return information. Parcel 0 from spindles 0 through 4 is stored as parcels 0 through 4 in local memory; parcel 1 is stored as parcels 5 through 9; and so forth. A done flag for the odd-numbered channel indicates that all spindles have completed their responses. A done flag for the even-numbered channel indicates that the response data has been stored in local memory. The transfer length should be set to the number of parcels expected from one spindle. The local memory parcel count should be set to five times the transfer length. If a spindle is not selected, its locations in local memory are filled with indeterminate data.

Accumulator Contents

2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Figure 11-2. DCA3:1 Accumulator Contents for Drive Response

M3	M2	M1	M0	Operation
0	1	0	1	Read ECC register. This function transfers the contents of the ECC registers to local memory. Parcel 0 of the ECC from spindle 0 is transferred first, followed by parcel 0 of the ECC from spindle 1. Parcel 15 of the ECC from spindle 4 is transferred last. The transfer length should be set to 16_{10} (20_8). The local-memory parcel count should be set to 80_{10} (120_8) to receive five 16-parcel ECCs.

DCA3:1 - Start Output Transfer (odd channel)

This function initiates a data transfer from EIOP local memory to the channel adapter. Modifier bit M0 must be cleared to 0. Bits M1 and M3 determine what data is transferred.

The operation of this function for the only defined combination of M0 through M3 is described in the following paragraphs.

M3	M2	M1	M0	Operation
0	0	0	0	Drive command control function. This function transfers information from IOP local memory to all selected spindles. The lower four bits of the accumulator must be set to 04_8 (refer to Figure 11-3). This information transfer follows, and supports, a drive command control byte previously transferred on the even channel with a DCA3:16 function. A done flag for the odd channel indicates that all data has been sent from local memory. A done flag for the even channel indicates that the drive function has been completed. The transfer length count is not used.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Figure 11-3. DCA3:1 Accumulator Contents for Drive Command

DCA3:2 – Set ID Parameter 0

The DCA3:2 function transfers the requested cylinder address (ID parameter 0) from the accumulator to the cylinder register in the 7DN options of the DCA-3. Figure 11-4 shows the format of ID parameter 0 in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
C 2^{15}	C 2^{14}	C 2^{13}	C 2^{12}	C 2^{11}	C 2^{10}	C 2^9	C 2^8	C 2^7	C 2^6	C 2^5	C 2^4	C 2^3	C 2^2	C 2^1	C 2^0

C = Cylinder Address

Figure 11-4. ID Parameter 0 Format

NOTE: Sector ID fields are formatted using the DCA3:5 function with a device function code of 25_8.

DCA3:3 – Set ID Parameter 1

The DCA3:3 function transfers the requested sector address, head address, and option bits (ID parameter 1) from the accumulator to the parameter register in the 7DN options of the DCA-3. Figure 11-5 shows the format of ID parameter 1 in the accumulator. Refer to the "Format and Flaw Management" disk drive sections of this manual for more information on the ID bit descriptions (which include ID parameter 1).

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
X	X	WP	RP	X	H	H	H	H	H	S	S	S	S	S	S
x	x	2^0	2^0	x	2^4	2^3	2^2	2^1	2^0	2^5	2^4	2^3	2^2	2^1	2^0

X = Not Used
WP = Write Protected
RP = Read Protected
H = Head Group Address
S = Sector Address

Figure 11-5. ID Parameter 1 Format

NOTE: Sector ID fields are formatted using the DCA3:5 function with a device function code of 25_8.

DCA3:4 – Set Transfer Count

The DCA3:4 function transfers the transfer count from the accumulator to the DCA-3. Figure 11-6 shows the format of the transfer count in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

T = Transfer Count

Figure 11-6. Transfer Count Format

Transfer count values can be decoded by the DCA-3 as bytes, parcels, or halfwords depending on the type of transfer initiated. Transfer types are determined by the number of spindles being referenced and the device function issued. Table 11-3 defines the transfer count settings.

Table 11-3. DCA-3 Transfer Counts

Transfer Type	Transfer Count Setting
Data transfer (array mode)	Sector size (halfwords): 010000_8 ($4{,}096_{10}$)
Data transfer (single spindle mode)	Sector size (bytes): 010000_8 ($4{,}096_{10}$)
Read or write data to/from buffer board with ECC	Sector size (halfwords) + 32_{10}: 010040_8 ($4{,}128_{10}$)
Read (verify) sector ID or Write (format) sector ID	Sector ID size (parcels): 000004 a (does not include ID ECC data)

DCA3:5 - Start Device Function

Bits 2^0 through 2^4 of the accumulator contain the device function interpreted by the DCA-3 controller. Figure 11-7 shows the accumulator format. Device functions 5, 7, and 17 through 27 use the lower byte of the DCA3:16 function data as a command control code. The sequence error flag is set if the drive interface is not initially in the SLAVE ACKNOWLEDGE (slaveack) state for all bus control functions. Table 11-4 provides detailed descriptions of the device functions supported by the DCA-3.

Accumulator Contents	
2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^9 2^8 2^7 2^6 2^5	2^4 2^3 2^2 2^1 2^0
Not Used	Device Function Code

Figure 11-7. DCA3:3 Parameter 1 Control Parcel

Table 11-4. DCA3:5 Device Function Descriptions

Function (Octal)	Device Function Type	Description
00	Write data buffer	Data from the I/O buffer is written into the drive data buffers of the DCA-3 controller. Each word of data is sent to every drive data buffer. The maximum transfer length is 1 Kparcel.
01	Write data buffer striped	This function stores the data from the I/O buffer in the drive data buffers. The transfer length count should be set to 2000 halfwords ($4{,}096_{10}$ parcels).
02	Read data buffer	Data is transferred from the drive data buffers to the I/O buffer. Word 0 of I/O buffer data is the first word from the drive 0 buffer, word 1 of I/O buffer data is the first word from the drive 1 buffer, and so on. The maximum transfer length is 374_8 parcels.
03	Read data buffer striped	The current contents of the drive data buffers are transferred to the I/O buffer. A parity check from the parity drive buffer is performed if all spindles are selected. Data reconstruction can also be enabled for this reason. This function can be used as part of a diagnostic test of the drive data buffers.
05	Drive command control function	The lower byte of the previous DCA3:16 function is a command control byte. Data from the I/O buffer is sent to all spindles. The transfer length count should be the number of parcels to be sent to the spindles.
07	Drive response control function	The lower byte of the previous DCA3:16 function is a response control byte. Response data from the drives is sent to the I/O buffer. After the transfer completes, word 0 of the I/O buffer contains the first 4 parcels of data received from drive 0. Word 1 contains the first 4 parcels of drive 1. The transfer length count should be set to the number of parcels expected from each spindle.
10	Request interrupts poll	The response from a request interrupt sequence is ANDed with the upper bits of the accumulator. The channel status signals done when the results of the AND functions are nonzero for all selected spindles. A DCA3:0 function terminates this function.
11	Request slave interrupts or transfer settings	This function reports data as defined on the A bus. The drives with the status pending respond by putting the radial address on the B bus.
12	Request interrupt	This function reports interrupt status on the B bus from the spindle designated by the A bus.
13	Select	The ending status error flag sets if the drive response is zero. A sequence error flag sets if the interface is not initially in the idle state or if the drive does not respond in 100μs.
14	Deselect	The sequence error flag sets if the drive interface is not initially in the slave acknowledge (slavack) state.
15	Master reset	This function turns off the drive interface.
16	Selective reset	The sequence error flag sets if the drive is not initially in the idle state. This function then performs a reset function as defined by bits 0–2 on the A bus.

Table 11-4. DCA3:5 Device Function Descriptions (continued)

Function (Octal)	Device Function Type	Description
17	Command with no information transfer	The lower byte of the previous DCA3:16 function is used as a command control in a bus exchange sequence. The bus control sequence is terminated before any information is transferred.
20	Read sector data	This function reads the header data-in bus exchange sequence using bus control in the lower byte of DCA3:16 until ID compare and ECC checking is complete. The field data-in bus exchange sequence uses bus control in the upper byte of DCA3:16 and checks ECC.
21	Read sector ID	This function reads the header using bus control in the lower byte of DCA3:16 and checks ECC. Parcels 0 through 3 of the ID are transferred to the I/O buffer.
22	Read sector absolute	This function reads the header at the target data-in bus exchange sequence using bus control in the lower byte of DCA3:16, without ID compare and without checking ECC. The field data-in exchange sequence uses bus control in the upper byte of DCA3:16 and checks ECC.
23	Read sector data and ECC to the I/O buffer	This function reads the header data-in bus exchange sequence using bus control in the lower byte of DCA3:16 until ID compare and ECC checking is complete. The field data-in bus exchange sequence uses bus control in the upper byte of DCA3:16 without checking ECC. ECC is included in the data passed to the I/O buffer.
24	Write sector data	This function reads the header data-in bus exchange sequence using bus control in the lower byte of DCA3:16 until ID compare and ECC checking is complete. The write field data-out bus exchange sequence uses bus control in the upper byte of DCA3:16 and generates ECC.
25	Write sector ID (format)	This function writes the header at the target data-out bus exchange sequence using bus control in the lower byte of DCA3:16 and generates ECC.
27	Write sector data and ECC from the I/O buffer	This function reads the header data-in bus exchange sequence using bus control in the lower byte of DCA3:16 until ID compare and ECC checking is complete. A write field data-out bus exchange sequence uses bus control in the upper byte of DCA3:16 without generating ECC. (ECC is part of the data from the I/O buffer.)

DCA3:6 – Disable Interrupt Enable Flag

The DCA3:6 function sets the EIOP channel enable interrupt flag to 0. When the enable interrupt flag is 0, the channel does not acknowledge any interrupts it receives. This function does not change the states of the channel busy or channel done flags.

DCA3:7 – Enable Interrupt Enable

The DCA3:7 function sets the EIOP channel enable interrupts flag to 1. When the enable interrupt flag is 1, the channel acknowledges any interrupts it receives. This function does not change the states of the busy and done flags.

DCA3:10 – Read Local Memory Address

The DCA3:10 function transfers the current local memory address from the EIOP channel local-memory address register to the accumulator. Figure 11-8 shows the format of the local memory address in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
LM 2^{15}	LM 2^{14}	LM 2^{13}	LM 2^{12}	LM 2^{11}	LM 2^{10}	LM 2^{9}	LM 2^{8}	LM 2^{7}	LM 2^{6}	LM 2^{5}	LM 2^{4}	LM 2^{3}	LM 2^{2}	LM 2^{1}	LM 2^{0}

LM = Current Local Memory Address

Figure 11-8. Current Local Memory Address Format

DCA3:11 – Read Inverted Local Memory Parcel Count

The DCA3:11 function transfers the inverse of the EIOP channel parcel counter to the accumulator. To obtain the correct parcel count, the accumulator contents must be subtracted from 177777_8. Figure 11-9 shows the format of the inverted parcel count in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
IP 2^{15}	IP 2^{14}	IP 2^{13}	IP 2^{12}	IP 2^{11}	IP 2^{10}	IP 2^{9}	IP 2^{8}	IP 2^{7}	IP 2^{6}	IP 2^{5}	IP 2^{4}	IP 2^{3}	IP 2^{2}	IP 2^{1}	IP 2^{0}

Figure 11-9. Inverted Parcel Count Format

DCA3:12 - Read Status 0

This function transmits one of seven status parcels to the accumulator. The contents of accumulator bits 2^0, 2^1, and 2^2 when the function is issued, determine which status parcel is returned. Table 11-5 shows the seven available status parcels.

Table 11-5. DCA3:12 Status Parcels

Bit	000 Interrupt Status	001 SECDED Status	010 Transfer Count	011 Control Bus Status	100 Busy Status	101 Done Status	110 DMA Ack. Pending Status	111
2^0	Spindle parity error	Syndrome bit 0	Transfer count 2^0	Select out	Spindle 0 busy	Spindle 0 done	Spindle 0 pending	Not Used
2^1	Sequence error	Syndrome bit 1	Transfer count 2^1	Slave-in	Spindle 1 busy	Spindle 1 done	Spindle 1 pending	Not Used
2^2	Lost data error	Syndrome bit 2	Transfer count 2^2	Master-out	Spindle 2 busy	Spindle 2 done	Spindle 2 pending	Not Used
2^3	Ending status error	Syndrome bit 3	Transfer count 2^3	Sync-in	Spindle 3 busy	Spindle 3 done	Spindle 3 pending	Not Used
2^4	–4.5 V voltage fault	Syndrome bit 4	Transfer count 2^4	Sync-out	Spindle 4 busy	Spindle 4 done	Spindle 4 pending	Not Used
2^5	+5.0 V voltage good	Syndrome bit 5	Transfer count 2^5	Attention-in	Not Used	Not Used	Not Used	Not Used
2^6	SECDED error	Syndrome bit 6	Transfer count 2^6	Gate bus A out	Not Used	Not Used	Not Used	Not Used
2^7	Data parity error	Syndrome bit 7	Transfer count 2^7	Gate bus B out	Not Used	Not Used	Not Used	Not Used
2^8	ID compare error	Single-bit error count 2^0	Transfer count 2^8	Not Used	Not Used	Not Used	Not Used	Not Used
2^9	ECC error	Single-bit error count 2^1	Transfer count 2^9	Not Used	Not Used	Not Used	Not Used	Not Used
2^{10}	ID error	Single-bit error count 2^2	Transfer count 2^{10}	Not Used	Not Used	Not Used	Not Used	Not Used
2^{11}	Hideable flaw	Single-bit error count 2^3	Transfer count 2^{11}	Not Used	Not Used	Not Used	Not Used	Not Used
2^{12}	Unhidable flaw	Double-bit error count 2^0	Transfer count 2^{12}	Not Used	Not Used	Not Used	Not Used	Not Used
2^{13}	ID field flaw	Double-bit error count 2^1	Transfer count 2^{13}	Not Used	Not Used	Not Used	Not Used	Not Used
2^{14}	Write protect	Double-bit error count 2^2	Transfer count 2^{14}	Not Used	Not Used	Not Used	Not Used	Not Used
2^{15}	Read protect	Double-bit error count 2^3	Transfer count 2^{15}	Not Used	Not Used	Not Used	Not Used	Not Used

The following information applies to the seven status parcels shown in Table 11-5:

- Issuing a DCA3:0 function clears the following status bits:
  - Interrupt status bits 2^0 through 2^3 and bits 2^6 through 2^{10}
  - SECDED status bits 2^8 through 2^{15}
  - All spindle busy, spindle done, and DMA acknowledge pending status bits.
- The spindle busy and spindle done status parcels are intended to simplify the process of isolating a failure to an individual spindle. When a function is completed with an error, the busy and done flags set. If a failure, such as a spindle parity error, can be attributed to an individual spindle, the busy and done flags for each spindle can be read to determine which spindle had the error. The DMA acknowledge pending status can be used to isolate a hung local memory command or response control to a particular spindle.
- Unlike the DCA-2, stacked functions proceed on the DCA-3 even if the previous function ended in error.

The following information applies to the interrupt status (DCA3:12 accumulator = 0) parcel:

- Bits 2^0 through 2^3 and bits 2^8 through 2^{15} of the interrupt status and all bits of the control bus status are logical ORs of the information from each selected spindle.
- Bits 2^{11} through 2^{15} of the interrupt status are copies from the ID field during the last ID compare operation. If bits 2^{12}, 2^{13} or 2^{14} are set, they will result in a busy/done condition. Bits 2^{11} and 2^{15} are informational only.
- Single-bit SECDED errors do not cause the busy flag to remain set after a function has completed.
- If bits 2^0 through 2^3, 2^8, 2^9, and 2^{10} of the interrupt status parcel are set, the individual spindle controller that had the error remains busy after a function has completed.
- Bit 2^0 (spindle parity error) indicates that the spindle response data or that the spindle read data had a parity error.

- Bit 2^1 (sequence error) indicates that a spindle function was attempted from an invalid initial IPI state or that a Select signal timed out.

- Bit 2^2 (a lost data error) is set if the I/O buffer data is not supplied to the spindle data buffer early enough during a write, or if the spindle data buffer is not sent to the I/O buffer quickly enough during a read. Loss of spindle synchronization is one cause of a lost data error. If one spindle has a lost data error, that spindle may be out of sync. If all spindles but one have lost data errors, the one spindle without a lost data error may be out of sync.

- Bit 2^3 (an ending status error) is set after a bus control sequence completes if the spindle ending status bits 2^0 through 2^3 are nonzero, if bit 6 has a parity error, or if bit 2^7 is zero.

- Bits 2^4 and 2^5 (voltage faults) are informational only and do not result in any hardware-initiated action.

- Bit 2^6 indicates a SECDED error. This bit is set if either the single-bit error count or the double-bit error count is not zero.

- Bit 2^7 (data parity error) is set when any nibble parity errors are detected and can occur only during striped reads with all spindles enabled.

- Bit 2^{10} (ID error) is set if a write or a read is stopped by an ID error. Bits 2^8, 2^9, 2^{12}, and 2^{13} provide further information if there is an ID error. If an ID error is detected, a parity error may occur because the data read did not occur. If only bit 2^9 (ECC error) is set, the ECC error occurred after the data field read. Bit 2^9 can be the only bit set if there is an ECC error on a read ID function.

DCA3:13 - Read Status 1

This function transmits one of four status parcels to the accumulator. When the function issues, the contents of accumulator bits 2^0 and 2^1 determine which status parcel is returned. Table 11-6 shows the four status parcels.

Each of the status parcels is a logical OR of the information from each selected spindle. Function DCA3:17 (M0 = 1) determines which spindles are selected.

Table 11-6. DCA3:13 Status Parcels

Bit	Accumulator Bits 2^1 and 2^0			
	00 Ending Status	01 ID Parameter 0	10 ID Parameter 1	11 Bus A and Bus B Data
2^0	Ending status 0 bit 0	Cylinder bit 0	Sector bit 0	Bus B data bit 0
2^1	Ending status 0 bit 1	Cylinder bit 1	Sector bit 1	Bus B data bit1
2^2	Ending status 0 bit 2	Cylinder bit 2	Sector bit 2	Bus B data bit 2
2^3	Ending status 0 bit 3	Cylinder bit 3	Sector bit 3	Bus B data bit 3
2^4	Ending status 0 bit 4	Cylinder bit 4	Sector bit 4	Bus B data bit 4
2^5	Ending status 0 bit 5	Cylinder bit 5	Sector bit 5	Bus B data bit 5
2^6	Ending status 0 bit 6	Cylinder bit 6	Head group 0	Bus B data bit 6
2^7	Ending status 0 bit 7	Cylinder bit 7	Head group 1	Bus B data bit 7
2^8	Ending status 1 bit 0	Cylinder bit 8	Head group 2	Bus A data bit 0
2^9	Ending status 1 bit 1	Cylinder bit 9	Head group 3	Bus A data bit 1
2^{10}	Ending status 1 bit 2	Cylinder bit 10	Head group 4	Bus A data bit 2
2^{11}	Ending status 1 bit 3	Cylinder bit 11	Not used	Bus A data bit 3
2^{12}	Ending status 1 bit 4	Cylinder bit 12	Not used	Bus A data bit 4
2^{13}	Ending status 1 bit 5	Cylinder bit 13	Not used	Bus A data bit 5
2^{14}	Ending status 1 bit 6	Cylinder bit 14	Not used	Bus A data bit 6
2^{15}	Ending status 1 bit 7	Cylinder bit 15	Not used	Bus A data bit 7

DCA3:14 – Set Local Memory Starting Address

The DCA3:14 function transfers the local memory starting address from the accumulator to the EIOP channel local-memory address register. The local memory starting address is the EIOP local memory address that contains the first parcel of data to be transferred to the DCA-3, or the

EIOP local memory address to which the DCA-3 transfers the first parcel of data. Figure 11-10 shows the format of the local memory starting address in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
LS 2^{15}	LS 2^{14}	LS 2^{13}	LS 2^{12}	LS 2^{11}	LS 2^{10}	LS 2^{9}	LS 2^{8}	LS 2^{7}	LS 2^{6}	LS 2^{5}	LS 2^{4}	LS 2^{3}	LS 2^{2}	LS 2^{1}	LS 2^{0}

LS = Local Memory Starting Address

Figure 11-10. Local Memory Starting Address Format

During a data transfer, the local memory address register of the channel automatically increments once with each parcel transferred. Execute the DCA3:10 function to transfer the current value of the local memory address register of the channel to the accumulator.

DCA3:15 – Set Local Memory Parcel Count

The DCA3:15 function transfers the local memory parcel count from the accumulator to the EIOP channel parcel counter. The parcel count is the number of parcels to be transferred between the EIOP local memory and the DCA-3. Figure 11-11 shows the format of the parcel count in the accumulator.

Accumulator Contents															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
PC 2^{15}	PC 2^{14}	PC 2^{13}	PC 2^{12}	PC 2^{11}	PC 2^{10}	PC 2^{9}	PC 2^{8}	PC 2^{7}	PC 2^{6}	PC 2^{5}	PC 2^{4}	PC 2^{3}	PC 2^{2}	PC 2^{1}	PC 2^{0}

PC = Parcel Count

Figure 11-11. Parcel Count Format

During a data transfer, the channel parcel counter automatically decrements once for each parcel transferred. Execute the DCA3:11 function to transfer the inverted current value of the channel parcel counter to the accumulator.

DCA3:16 – Write Control Bus Data

The DCA3:16 function transfers drive control commands from the accumulator to a register in the DCA-3. This register stores bus control codes or IPI-2 command information bytes. The DCA-3 controls the transfer of the register contents to the selected spindle(s) over bus A or over both bus A and bus B. Figure 11-12 shows the format of the command register values in the accumulator.

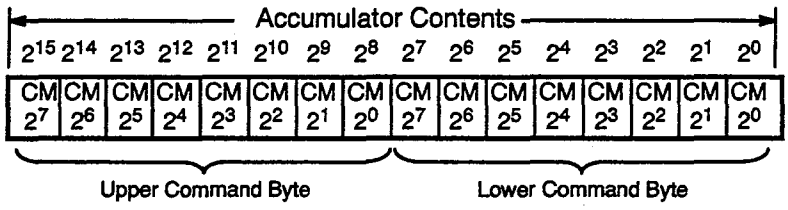


Figure 11-12. Control Register Values

Table 11-7 contains some of the IPI-2 control commands used by CRI.

Table 11-7. Sample Bus Control Commands Used by CRI

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Description
0	0	0	0	0	0	1	0	Load format specification
0	1	0	0	0	0	1	0	Read format specification
0	0	1	0	0	0	1	0	Spin up
0	0	1	0	0	0	0	1	Spin down
0	0	1	0	1	1	1	0	Disable master sync device
0	0	1	0	1	1	1	1	Enable master sync device
0	0	0	0	0	1	0	0	Load cylinder address (seek)
0	0	0	0	0	1	0	1	Load head address (head select)
0	0	0	0	0	1	1	0	Load rotational position sensing (RPS) target sector
0	0	0	0	0	1	1	1	Load position (cylinder, head, sector)
1	1	0	0	1	0	0	0	Read header
1	1	0	0	1	1	0	0	Read header at target
1	1	0	0	0	0	0	1	Read data field
1	0	0	0	0	0	0	1	Write data field
1	0	0	0	1	1	0	0	Write header at target (format)

0	1	0	0	0	1	0	0	Read status
0	1	0	0	1	0	0	0	Read extended status

DCA3:17 - Set Operating Mode

Modifier bit M0 determines which operation is performed by the DCA3:17 function. The following paragraphs explain the different operations.

Set Array Type with M0 = 0

This function uses the accumulator contents to provide the DCA-3 with the number of heads and logical sector size of the disk array type connected. This function should be executed immediately following a DCA3:17 set array mode (M0=1) function to properly initialize the array. Figure 11-13 shows the accumulator format.

2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^{9}	2^{8} 2^{7} 2^{6} 2^{5} 2^{4}	2^{3} 2^{2} 2^{1} 2^{0}
32K 16K 8K 4K 2K 1K 512 Sector Size (32 bit halfwords)	Not Used	8 4 2 1 Number of Heads (per spindle head group)
010002_8		

Figure 11-13. DCA3:17 Control Parcel (Even Channel)

Set Array Mode with M0 = 1

This function uses the accumulator contents to enable or disable individual spindles, enable or disable single-spindle mode, and enable or disable data reconstruction during reads. This command must precede all others to ensure proper initialization of the array. Valid spindle enables include selection of 1, 4, or 5 spindles. Two- or three-spindle modes are not supported. Figure 11-14 shows the accumulator format.

2^{15}	2^{14}	2^{13} 2^{12} 2^{11} 2^{10} 2^{9} 2^{8} 2^{7} 2^{6} 2^{5}	2^{4} 2^{3} 2^{2} 2^{1} 2^{0}
		Not Used (Clear to 0)	Spindle 4 Spindle 3 Spindle 2 Spindle 1 Spindle 0
	Set Single-spindle Mode		Spindle Enables
Enable data reconstruction during reads (Can Be Set at All Times)			

Figure 11-14. DCA3:17 Control Parcel (Odd Channel)

12 300 SERIES DISK SYSTEMS STATUS

This section provides status information for the 300 series disk systems, including error report examples, channel adapter statuses for the DCA-2 and DCA-3, and disk drive status information for the DD-301 spindles.

Error Reports

System errors for 300 series disk systems can be displayed through the OLHPA and ERRPT report generators. The following subsection includes example error report examples for DCA-2 and DCA-3 channel adapters using both report generators.

DD-301 (DCA-2) Error Reports

The following subsection provides examples of DD-301 error reports using the OLHPA and ERRPT report generators.

OLHPA Report for DD-301 / DCA-2 Errors

Figure 12-1 shows an OLHPA error report for a DD-301 disk drive. Refer to Table 12-1 for a cross-reference to the tables that describe each status.

```
HOST ERROR PACKET
Device: 301-00-3-36.3   Major: 000      Minor: 210
          Primary       Alternate      Active
I/O Path: 0336.3        0000.0         0336.3
IOS request: read data                 IOS response: io error
Final status: Rec by retrying
IOS-P: 00-3     Channel: 36/3   Device type: DD301      Retry count: 1
Requested cylinder: 003500        Head: 001     Sector: 0020  (Unicos)
Failing cylinder:   003500        Head: 004     Sector: 0002  (Physical)
Physical Block: 000324902
Request Length (sect): 000206   Spiral Offset: 000000
General Status:  100000         Last ml Status:  000000
```

Figure 12-1. OLHPA Display Example for a DD-301 (Sheet 1 of 2)

```
Error Recovery Trace (last 20 entries, first to final)
---|-------------------------------------------------------------------------
    |Disk  Disk  Rec     Drive SRB     M1      DCA12:  Ending  Mcode   Mcode
##| Req  Resp  Param   Oct1   Oct0   Status  A=0     Status  Line    Seq
---|-------------------------------------------------------------------------
00| 002   010  000006  040    000    000000  000200  100200  000000  dd301rcl
01| 174   000  000006  000    000    000000  000000  000200  000001    ldstat
02| 175   000  000000  362    043    000000  000000  000200  000006    ldstat
03| 175   000  000000  362    043    000000  000000  000200  000002    rdy301
04| 174   000  000000  000    000    000000  000000  000200  000012    rdy301
05| 001   000  000000  000    000    000000  000000  000000  000005  dd301rcl
---|-------------------------------------------------------------------------

DCA2 STATUS PACKET

DCA2 Command: 000020    (Read Data)
    Parameter: 140714

---------- DCA:13 ----------              ---------- DCA:12 ----------
Ending status: 100200                     Adaptor status: 000200
ID Parameter 0 status: 003500             Syndrome status: 000000
ID Parameter 1 status: 000402             Byte count status: 000000
                                          Tag status: 000022

6X Condition Bits:  040                   7X Condition Bits:  002

Stream 0: ecc: 31510307530  Offset: 006156  Defect Add: 00615
Stream 2: ecc: 31510307530  Offset: 006156  Defect Add: 00615
Stream 3: ecc: 31510307530  Offset: 006156  Defect Add: 00615
Stream 5: ecc: 31510307530  Offset: 006156  Defect Add: 00615
Stream 6: ecc: 31510307530  Offset: 006156  Defect Add: 00615
Stream 7: ecc: 31510307530  Offset: 006156  Defect Add: 00615
                 Combined Head Mask: 001     Flawing Defect Address: 00615

DRIVE ERROR PACKET

Status Response Block:
        (0x00-07): 000  000  000  000  000  000  000  000
        (0x08-0f): 000  000  000  000  000  000  000  000
        (0x10-17): 000  000  000  000  000  000  000  000
        (0x18-1f): 000  000  000  000  000  000  000  000

Extended Status Response Block:
        (0x00-07): 043  362  000  000  100  323  040  000
        (0x08-0f): 000  000  000  000  000  000  000  000
        (0x10-17): 000  000  000  000
```

Figure 12-1. OLHPA Display Example for a DD-301 (Sheet 2)

ERRPT Report for DD-301 / DCA-2 errors

Figure 12-2 shows an ERRPT error report for a DD-301 disk drive. Refer to Table 12-1 for a cross-reference to the tables that describe each status.

```
Disk error/Path summary:
        active =        0336.3   major = 00   minor = 210   type = dd301
        primary =       0336.3
        alternate =     0000.0
Resolution:
        recovery code = 000 / Recovered by retrying after 1 retries
IOS request:
        request  code = 002 / read data
        length = 206    cyl = 03500     head = 001      sec = 020
IOS response:
        response code = 010 / io error
        error location  cyl = 03500     head = 004      sec = 002


DCAx status:
        status response block
          000    000    000    000    000    000    000    000
          000    000    000    000    000    000    000    000
          000    000    000    000    000    000    000    000
          000    000    000    000    000    000    000    000

        extended status response block
          043    362    000    000    100    323    040    000
          000    000    000    000    000    000    000    000
          000    000    000    000

        dca2  command   bits   =  000020  command parameter      =  140714

        6x   condition   bits  =  000040  7x   condition   bits  =  000002
        drive  ending  status  =  100200  adaptor  status        =  000200
        id parameter 0 status  =  003500  syndrome status        =  000000
        id parameter 1 status  =  000402  transfer count status  =  000000
                                          IPI  tag  status       =  000022
Compressed ECC status:
        stream          ecc    offset  mask  defect
             0   31510307530    006156  0200  000615
             2   31510307530    006156  0200  000615
             3   31510307530    006156  0200  000615
             5   31510307530    006156  0200  000615
             6   31510307530    006156  0200  000615
             7   31510307530    006156  0200  000615


ERROR RECOVERY TRACE INFO(First to Last, all numbers in octal)

Disk  Disk  Rec  GStat  GStat   DCA12   DCA12   DCA13   Mcode    Mcode
 Req  Resp  Par   Oct1   Oct0     A=1     A=0     A=0    Line  Sequence
 002   010  006    040    000  000000  000200  100200  000000  dd301rcl
 174   000  006    000    000  000000  000000  000200  000001  ldstat
 175   000  000    362    043  000000  000000  000200  000006  ldstat
 175   000  000    362    043  000000  000000  000200  000002  rdy301
 174   000  000    000    000  000000  000000  000200  000012  rdy301
 001   000  000    000    000  000000  000000  000000  000005  dd301rcl
```

Figure 12-2.. ERRPT Display Example for a DD-301

DA-301 (DCA-3) Error Reports

The following subsection provides examples of DA-301 disk array error reports using the OLHPA and ERRPT report generators.

OLHPA Report for DA-301 / DCA-3 Errors

Figure 12-3 shows an OLHPA error report for a DA-301 disk array. Refer to Table 12-1 for a cross-reference to the tables describing each status.

```
HOST ERROR PACKET
Device: A301-05-0-34.1  Major: 032      Minor: 182
          Primary       Alternate       Active
I/O Path: 5034.1        0000.0          5034.1
IOS request: read data                  IOS response: io error
Final status: Rec by retrying
IOS-P: 05-0     Channel: 34/1   Device type: DA301      Retry count: 1
Requested cylinder: 003056        Head: 000     Sector: 0021  (Unicos)
Failing cylinder:   003056        Head: 001     Sector: 0000  (Physical)
Physical Block: 000276875
Request Length (sect): 000025   Spiral Offset: 000000
General Status:  100004         Last m1 Status:  000377
                      DATA ECC error on spindle 2
Error Recovery Trace (last 20 entries, first to final)
--|-----------------------------------------------------------------------
  |Disk  Disk  Rec     Drive SRB     M1      DCA12:  Ending  Mcode   Mcode
##| Req  Resp  Param   Oct1  Oct0    Status  A=0     Status  Line    Seq
--|-----------------------------------------------------------------------
00| 002   010  000000  004   000     000377  001240  100200  000000  da301rcl
01| 174   000  000000  000   000     000377  000040  100200  000001  da301lst
02| 175   000  000000  362   043     000377  000040  100200  000006  da301lst
03| 175   000  000000  362   043     000377  000040  100200  000002  da301sbl
04| 175   000  000000  362   043     000377  000040  100200  000002  da301mst
05| 174   000  000000  000   000     000377  000040  100200  000002  da301sb0
06| 001   000  000000  000   000     000377  000040  100200  000011  da301rcl
--|-----------------------------------------------------------------------

DCA3 STATUS PACKET

Flags for all drives (bit 0 = spindle 0)
  Busy&Done     Busy Flags      Done Flags      DMA Acknowledge
-------------------------------------------------------------------
  000004        000004          000037          000000

DCA3 Command: 000020    (Read Data)
    Parameter: 140714
```

Figure 12-3. OLHPA Display Example for a DA-301 (Sheet 1 of 3)

		Spindle	0	1	2	3	P
		Drive Serial Number	227F	147F	156F	146F	133F
		Random Label	117	117	117	117	117
D	A=0	Interrupt Status	000240	000240	001240	000240	000240
C	A=1	SECDED Status	000377	000377	000377	000377	000377
A:	A=2	Transfer Status	000000	000000	000000	000000	000000
12	A=3	IPI Tag Status	000103	000103	000103	000103	000103
D	A=0	Drive ending Status	100200	100200	100200	100200	100200
C	A=1	ID Parameter 0 Status	003056	003056	003056	003056	003056
A:	A=2	ID Parameter 1 Status	000100	000100	000100	000100	000100
13	A=3	Bus A/B Data	177600	177600	177600	177600	177600

# of parcels remaining in transfer

useless

OK

000100 HD sec.

```
DRIVE ERROR PACKET
 Status Response Block:
  Spindle 0:    (0x00-07): 000  000  000  000  000  000  000  000
                (0x08-0f): 000  000  000  000  000  000  000  000
                (0x10-17): 000  000  000  000  000  000  000  000
                (0x18-1f): 000  000  000  000  000  000  000  000

  Spindle 1:    (0x00-07): 000  000  000  000  000  000  000  000
                (0x08-0f): 000  000  000  000  000  000  000  000
                (0x10-17): 000  000  000  000  000  000  000  000
                (0x18-1f): 000  000  000  000  000  000  000  000

  Spindle 2:    (0x00-07): 000  000  000  000  000  000  000  000
                (0x08-0f): 000  000  000  000  000  000  000  000
                (0x10-17): 000  000  000  000  000  000  000  000
                (0x18-1f): 000  000  000  000  000  000  000  000

  Spindle 3:    (0x00-07): 000  000  000  000  000  000  000  000
                (0x08-0f): 000  000  000  000  000  000  000  000
                (0x10-17): 000  000  000  000  000  000  000  000
                (0x18-1f): 000  000  000  000  000  000  000  000

  Spindle P:    (0x00-07): 000  000  000  000  000  000  000  000
                (0x08-0f): 000  000  000  000  000  000  000  000
                (0x10-17): 000  000  000  000  000  000  000  000
                (0x18-1f): 000  000  000  000  000  000  000  000

Extended Status Response Block:
  Spindle 0:    (0x00-07): 043  362  000  000  126  323  040  000
                (0x08-0f): 000  000  000  000  000  000  000  000
                (0x10-17): 023  362  000  000  122  323  040  000

  Spindle 1:    (0x00-07): 023  362  000  000  122  323  040  000
                (0x08-0f): 000  000  000  000  000  000  000  000
                (0x10-17): 043  362  000  000  122  323  040  000

  Spindle 2:    (0x00-07): 043  362  000  000  122  323  040  000
                (0x08-0f): 000  000  000  000  000  000  000  000
                (0x10-17): 023  362  000  000  122  323  040  000
```

all zero's is good

master

Figure 12-3. OLHPA Display Example for a DA-301 (Sheet 2)

```
Spindle 3:     (0x00–07): 023  362  000  000  122  323  040  000
               (0x08–0f): 000  000  000  000  000  000  000  000
               (0x10–17): 043  362  000  000  122  323  040  000

Spindle P:     (0x00–07): 043  362  000  000  122  323  040  000
               (0x08–0f): 000  000  000  000  000  000  000  000
               (0x10–17): 000  000  000  000

|***************** ECC Status for spindle 0 ******************|

|***************** ECC Status for spindle 1 ******************|

|***************** ECC Status for spindle 2 ******************|
|Stream 2: ecc: 15161701732  Offset: 002606  Defect Add: 00260|
|Stream 3: ecc: 15161701732  Offset: 002606  Defect Add: 00260|
|Combined Head Mask: 001         Flawing Defect Address: 00260|

|***************** ECC Status for spindle 3 ******************|

|***************** ECC Status for spindle P ******************|
```

Figure 12-3. OLHPA Display Example for a DA-301 (Sheet 3)

ERRPT Report for DA-301 / DCA-3 error

Figure 12-4 shows an ERRPT report for a DA-301 disk array. Refer to Table 12-1 for a cross-reference to the tables that describe each status.

```
Disk error/Path summary:
        active =        5034.1   major = 32   minor = 182   type = da301
        primary =       5034.1
        alternate =     0000.0
Resolution:
        recovery code = 000 / Recovered by retrying after 1 retries
IOS request:
        request  code = 002 / read data
        length = 25     cyl = 03056     head = 000      sec = 021
IOS response:
        response code = 010 / io error
        error location  cyl = 03056     head = 001      sec = 000


Unique Identification Area for All Drives:
                Drive S/N       Spindle         Label
                ---------       -------         -----
Spindle_0           227F            0             117
Spindle_1           147F            1             117
Spindle_2           156F            2             117
Spindle_3           146F            3             117
Spindle_4           133F            4             117

DCA3 command(IOB:5/IOB:1) =  000020  command parameter(IOB:16) = 140714

Flags Area for All Drives:
        Bsy&DN          Bsy Flags       DN Flags        DMA Ack
        ------          ---------       --------        -------
        000004             000004         000037         000000

Status Response Block:
Spndle_0  000    000    000    000    000    000    000    000
          000    000    000    000    000    000    000    000
          000    000    000    000    000    000    000    000
          000    000    000    000    000    000    000    000

Spndle_1  000    000    000    000    000    000    000    000
          000    000    000    000    000    000    000    000
          000    000    000    000    000    000    000    000
          000    000    000    000    000    000    000    000

Spndle_2  000    000    000    000    000    000    000    000
          000    000    000    000    000    000    000    000
          000    000    000    000    000    000    000    000
          000    000    000    000    000    000    000    000

Spndle_3  000    000    000    000    000    000    000    000
          000    000    000    000    000    000    000    000
          000    000    000    000    000    000    000    000
          000    000    000    000    000    000    000    000

Spndle_4  000    000    000    000    000    000    000    000
          000    000    000    000    000    000    000    000
          000    000    000    000    000    000    000    000
          000    000    000    000    000    000    000    000
```

Figure 12-4. ERRPT Display Example for a DA-301 Disk Array (Sheet 1 of 2)

```
DCAx status:
 Extended Status Response Block:
Spndle_0  043    362    000    000    126    323    040    000
          000    000    000    000    000    000    000    000
          000    000    000    000
Spndle_1  023    362    000    000    122    323    040    000
          000    000    000    000    000    000    000    000
          000    000    000    000
Spndle_2  043    362    000    000    122    323    040    000
          000    000    000    000    000    000    000    000
          000    000    000    000
Spndle_3  023    362    000    000    122    323    040    000
          000    000    000    000    000    000    000    000
          000    000    000    000
Spndle_4  043    362    000    000    122    323    040    000
          000    000    000    000    000    000    000    000
          000    000    000    000

                Adapter Stat      Secded         Xfer Cnt        IPI Tags
                   DCA12 A=0     DCA12 A=1      DCA12 A=2       DCA12 A=3
                ____________   ____________   ____________   ____________
Spindle_0           000240         000377         000000          000103
Spindle_1           000240         000377         000000          000103
Spindle_2           001240         000377         000000          000103
Spindle_3           000240         000377         000000          000103
Spindle_4           000240         000377         000000          000103

                Ending Stat     ID Param_0     ID Param_1     BusA/B Data
                  DCA13 A=0      DCA13 A=1      DCA13 A=2       DCA13 A=3
                ____________   ____________   ____________   ____________
Spindle_0           100200         003056         000100          177600
Spindle_1           100200         003056         000100          177600
Spindle_2           100200         003056         000100          177600
Spindle_3           100200         003056         000100          177600
Spindle_4           100200         003056         000100          177600

Spindle 2:
Compressed ECC status:
        stream          ecc    offset  mask  defect
             2   15161701732   002606  0200  000260
             3   15161701732   002606  0200  000260

 ERROR RECOVERY TRACE INFO(First to Last, all numbers in octal)

Disk  Disk  Rec    SRB    SRB   DCA12   DCA12   DCA13   Mcode     Mcode
 Req  Resp  Par   Oct1   Oct0     A=1     A=0     A=0    Line  Sequence
____  ____  ___  _____  _____  ______  ______  ______  ______  ________
 002   010  000    004    000  000377  001240  100200  000000  da301rcl
 174   000  000    000    000  000377  000040  100200  000001  da301lst
 175   000  000    362    043  000377  000040  100200  000006  da301lst
 175   000  000    362    043  000377  000040  100200  000002  da301sb1
 175   000  000    362    043  000377  000040  100200  000002  da301mst
 174   000  000    000    000  000377  000040  100200  000002  da301sb0
 001   000  000    000    000  000377  000040  100200  000011  da301rcl
```

Figure 12-4. ERRPT Display Example for a DA-301 (Sheet 2)

Table 12-1. Status Name Cross-reference Chart

Page	Table	Status Name	Obtained By
DCA-2 Channel Adapter Statuses			
12-12	Table 12-2	General status	OLHPA software
12-13	Table 12-3	6X Condition bits	DCA2:12 channel function
12-14	Table 12-4	7X Condition bits	DCA2:12 channel function
12-15	Table 12-5	Adapter status	DCA2:12 channel function
12-16	Table 12-6	SECDED status	DCA2:12 channel function
12-17	Table 12-7	Transfer count status	DCA2:12 channel function
12-17	Table 12-8	Tag status	DCA2:12 channel function
12-18	Table 12-9	Drive ending status	DCA2:13 channel function
12-19	Table 12-10	Disk drive status on Bus B	IPI-2 protocol
12-20	Table 12-11	ID parameter 0 status	DCA2:13 channel function
12-20	Table 12-12	ID parameter 1 status	DCA2:13 channel function
DCA-3 Channel Adapter Statuses			
12-21	Table 12-13	General status	OLHPA software
12-22	Table 12-14	Interrupt status bits	DCA3:12 channel function
12-23	Table 12-15	SECDED status bits	DCA3:12 channel function
12-23	Table 12-16	Transfer count status bits	DCA3:12 channel function
12-24	Table 12-17	IPI tag status bits	DCA3:12 channel function
12-24	Table 12-18	Busy status bits	DCA3:12 channel function
12-25	Table 12-19	Done status bits	DCA3:12 channel function
12-25	Table 12-20	DMA acknowledge-pending status bits	DCA3:12 channel function
12-26	Table 12-21	Drive ending status	DCA3:13 channel function
12-27	Table 12-22	Ending status byte returned on Bus B	IPI-2 protocol
12-28	Table 12-23	ID parameter 0 status	DCA3:13 channel function
12-28	Table 12-24	ID parameter 1 status	DCA3:13 channel function
12-29	Table 12-25	Bus A and B data	DCA3:13 channel function
300 Series Drive Status Response Block			
12-30	Table 12-26	Exception status (Byte 00_{16})	Bus control command (44_{16})
12-31	Table 12-27	Exception status (Byte 01_{16})	Bus control command (44_{16})
12-31	Table 12-28	Unsolicited exception status (Byte 02_{16})	Bus control command (44_{16})
12-31	Table 12-29	Unsolicited exception status (Byte 03_{16})	Bus control command (44_{16})
12-32	Table 12-30	Unsolicited exception status (Byte 04_{16})	Bus control command (44_{16})
12-32	Table 12-31	Unsolicited exception status (Byte 05_{16})	Bus control command (44_{16})
12-32	Table 12-32	Bus control exceptions status (Byte 06_{16})	Bus control command (44_{16})
12-33	Table 12-33	Bus control exceptions status (Byte 07_{16})	Bus control command (44_{16})
12-33	Table 12-34	Slave exception status (Byte 08_{16})	Bus control command (44_{16})

Table 12-1. Status Name Cross-reference Chart (continued)

Page	Table	Status Name	Obtained By
300 Series Drive Status Response Block (continued)			
12-33	Table 12-35	Slave exception status (Byte 09_{16})	Bus control command (44_{16})
12-34	Table 12-36	Slave exception status (Byte $0A_{16}$)	Bus control command (44_{16})
12-34	Table 12-37	Slave exception status (Byte $0B_{16}$)	Bus control command (44_{16})
12-34	Table 12-38	Buffer exception status (Byte $0C_{16}$)	Bus control command (44_{16})
12-34	Table 12-39	Buffer exception status (Byte $0D_{16}$)	Bus control command (44_{16})
12-34	Table 12-40	Buffer exception status (Byte $0E_{16}$)	Bus control command (44_{16})
12-34	Table 12-41	Buffer exception status (Byte $0F_{16}$)	Bus control command (44_{16})
12-35	Table 12-42	IDM detected faults (Byte 10_{16})	Bus control command (44_{16})
12-35	Table 12-43	Drive control module detected faults (Byte 11_{16})	Bus control command (44_{16})
12-36	Table 12-44	Drive control module detected faults (Byte 12_{16})	Bus control command (44_{16})
12-36	Table 12-45	Drive control module detected faults (Byte 13_{16})	Bus control command (44_{16})
12-36	Table 12-46	Drive control module detected faults (Byte 14_{16})	Bus control command (44_{16})
12-37	Table 12-47	IDM / IP detected errors (Byte 15_{16})	Bus control command (44_{16})
12-38	Table 12-48	Servo status (Byte 16_{16})	Bus control command (44_{16})
12-38	Table 12-48	IP error code (Byte 17_{16})	Bus control command (44_{16})
12-41	Table 12-49	Failure detected status (Byte 18_{16})	Bus control command (44_{16})
12-41	Table 12-50	Failure detected status (Byte 19_{16})	Bus control command (44_{16})
12-42	Table 12-51	IDM / IP detected errors (Byte $1A_{16}$)	Bus control command (44_{16})
12-42	Table 12-52	Vendor unique status (Byte $1B_{16}$)	Bus control command (44_{16})
12-42	Table 12-53	Failure pending status (Byte $1C_{16}$)	Bus control command (44_{16})
12-43	Table 12-54	Failure pending status (Byte $1D_{16}$)	Bus control command (44_{16})
12-43	Table 12-55	EEPROM data faults (Byte $1E_{16}$)	Bus control command (44_{16})
12-43	Table 12-56	EEPROM data faults (Byte $1F_{16}$)	Bus control command (44_{16})
300 Series Drive Extended Status Block			
12-44	Table 12-57	Interface flags status (Byte 00_{16})	Bus control command (48_{16})
12-44	Table 12-58	Interface flags status (Byte 01_{16})	Bus control command (48_{16})
12-44	Table 12-59	Data recovery flags status (Byte 02_{16})	Bus control command (48_{16})
12-45	Table 12-60	Data recovery flags status (Byte 03_{16})	Bus control command (48_{16})
12-45	Table 12-61	Slave status flags (Byte 04_{16})	Bus control command (48_{16})
12-45	Table 12-62	Slave status flags (Byte 05_{16})	Bus control command (48_{16})
12-46	Table 12-63	Slave status flags (Byte 06_{16})	Bus control command (48_{16})
12-46	Table 12-65	Slave status flags (Byte 07_{16})	Bus control command (48_{16})
12-46	Table 12-66	Slave alarms (Byte 08_{16})	Bus control command (48_{16})
12-46	Table 12-68	Slave alarms (Byte 09_{16})	Bus control command (48_{16})
12-47	Table 12-69	Slave data recovery level active (Byte $0A_{16}$)	Bus control command (48_{16})

Table 12-1. Status Name Cross-reference Chart (continued)

Page	Table	Status Name	Obtained By
300 Series Drive Extended Status Block (continued)			
12-47	Table 12-69	Slave data recovery level active (Byte $0B_{16}$)	Bus control command (48_{16})
12-47	Table 12-70	Failure pending alarms (Byte $0C_{16}$)	Bus control command (48_{16})
12-47	Table 12-71	Failure pending alarms (Byte $0D_{16}$)	Bus control command (48_{16})
12-47	Table 12-72	Vendor unique extended status (Byte $0E_{16}$)	Bus control command (48_{16})
12-47	Table 12-73	Vendor unique extended status (Byte $0F_{16}$)	Bus control command (48_{16})
12-48	Table 12-74	Thermal Compensation Retry Counts (Byte 10_{16})	Bus control command (48_{16})
12-48	Table 12-75	Thermal Compensation Retry Counts (Byte 11_{16})	Bus control command (48_{16})
12-48	Table 12-76	Thermal Compensation Retry Counts (Byte 12_{16})	Bus control command (48_{16})
12-48	Table 12-77	Thermal Compensation Retry Counts (Byte 13_{16})	Bus control command (48_{16})
Miscellaneous Status Information			
12-49	Table 12-78	OLHPA flaw location information	OLHPA software

DCA-2 Channel Adapter Statuses

General Status

General status is a combination of bits from several of the other statuses. It is combined and displayed by the OLHPA software. Table 12-2 describes each bit of the general status.

Table 12-2. General Status

Bits	Name	Description
0	Bus A parity error	The parity bit of bus A was not set to the expected value. Bus parity checks are performed by the 3DE option on all data transferred from the drive.
1	Byte 1 parity error	Data byte 1 (bus A information) had a parity error. Byte parity checks are performed by the 3DE option only on data destined for the IOS buffer module.
2	Bus B parity error	The parity bit of bus B was not set to the expected value. Bus parity checks are performed by the 3DE option on all data transferred from the drive.
3	Byte 0 parity error	Data byte 0 (bus B information) had a parity error. Byte parity checks are performed by the 3DE option only on data destined for the IOS buffer module.
4	Voltage fault –4.5 V	The –4.5-V is out of range on the channel adapter.
5	Voltage fault +5.0 V	The +5.0-V is out of range on the channel adapter.
6	Single-bit error	A write data bit was wrong, but was corrected by SECDED circuitry in the 3YC option.
7	Double-bit error	Multiple write data bits were wrong and SECDED circuitry in the 3YC option was unable to correct them.
8	Head select fault	The disk drive received an invalid head selection.
9	Off cylinder fault	The heads were not positioned over the correct cylinder during a seek, or the heads moved off cylinder during a data transfer.
10	Seek fault	An error occurred during a seek, read/verify data, or write data bus control operation.
11	Spindle fault	An error occurred during a spin-up, spin-down, or during a read/verify data or write data bus control operation.
12	Execution fault	A disk drive execution fault occurred.
13	ID error correction code (ECC) error	The ID field ECC read from the disk drive did not match the ECC generated by the 3DH options.
14	ID compare error	The ID of the sector read from the disk drive did not compare to the expected ID stored in the 3DG option.
15	Data ECC error	The data field ECC read from the disk drive did not match the ECC generated by the 3DH options.

Condition Bits

When the status select bits are both 0's and the sequencer is given a starting address of 36_8, the DCA2:12 channel function transfers the condition bits to the accumulator. There are two types of condition bits: the 6X condition bits and the 7X condition bits.

6X Condition Bits

The 6X condition bits are assembled by the microcode from information generated by the 3DE option, 3YC option, and voltage sensors on the DCA-2. When this status is read affects the condition of the bus A/B parity error flags because these flags are dynamic. Table 12-3 describes each bit of the 6X condition bits.

Table 12-3. 6X Condition Bits Status

Bit	Name	Description
0	Bus A parity error	The parity bit of bus A was not set to the expected value. Bus parity checks are performed by the 3DE option on all data transferred from the drive.
1	Byte 1 parity error	Byte 1 (bus A information) of the data had a parity error. Byte parity checks are performed by the 3DE option only on data destined for the IOS buffer module.
2	Bus B parity error	The parity bit of bus B was not set to the expected value. Bus parity checks are performed by the 3DE option on all data transferred from the drive.
3	Byte 0 parity error	Byte 0 (bus B information) of the data had a parity error. Byte parity checks are performed by the 3DE option only on data destined for the IOS buffer module.
4	–4.5 voltage bad	The –4.5 voltage setting is out of acceptable range.
5	+5.0 voltage good	When set to 0, this bit indicates that the +5.0 voltage setting is out of acceptable range.
6	Single-bit error	A write data bit was in error, but was corrected by SECDED circuitry in the 3YC option.
7	Double-bit error	Multiple bits were in error and SECDED circuitry in the 3YC options was unable to correct them.

7X Condition Bits

The 7X condition bits are assembled by the microcode from information generated by the 3DH options and 3DG option on the DCA-2. Table 12-4 describes each bit of the 7X condition bits.

Table 12-4. 7X Condition Bits Status

Bit	Name	Description
0	ID compare error	The ID of the sector read from the disk drive did not compare to the expected ID.
1	Data ECC error	The data field ECC read from the disk drive did not match the ECC generated on the read data by the 3DH options.
2	ID ECC error	The ID field ECC read from the disk drive did not match the ECC generated by the 3DH options.
3	Valid flaw	The sector contains a hideable flaw.
4	Unhideable flaw	The sector contains an unhideable flaw.
5	ID field flaw	The sector ID field contains a flaw.
6	Read protect	The read protect bit of the sector ID field is set to 1. (Format default forces this bit to 0)
7	Write protect	The write protect bit of the sector ID field is set to 1. (Format default forces this bit to 0)

Adapter Status

When the status select bits are both 0's, the DCA2:12 channel function transfers the adapter status to the accumulator (refer to Table 12-5). The lower byte of this status should be decoded by first starting at the bottom of the list (200_8 in Table 12-5) and then selecting all status codes that can be ORed into the returned status value. When all set bits of the returned value have been satisfied by the codes selected, decoding is complete. For example, if the returned adapter status is equal to 000363_8, the decode is as follows:

Codes	Applicable
200_8	Yes
100_8	Yes
40_8	Yes
24_8	No
22_8	Yes
21_8	Yes
363_8	(ORed sum of applicable codes equals returned value)

Table 12-5. Adapter Status

Bits	Name	Description
0	DCA-2 status bit 0	Bits Description 000_8– No errors were detected by the sequencer. 001_8– The disk drive did not respond to a request within a set time limit. 002_8– The interface did not return to the IDLE state within a set time limit.
1	DCA-2 status bit 1	003_8– The disk drive did not respond to a select within a set time limit. 004_8– The expected disk drive did not respond to the select sequence. 005_8– The disk drive set the busy flag during a select sequence.
2	DCA-2 status bit 2	006_8– The disk drive is not selected when the sequencer expected it to be. 007_8– The disk drive is selected when the sequencer did not expect it to be.
3	DCA-2 status bit 3	010_8– During a bus control sequence, the disk drive did not set the Sync In signal to 1 within a set time limit. 011_8– During a bus control sequence, the disk drive did not reset the Sync In signal to 0 within a set time limit.
4	DCA-2 status bit 4	012_8– The bus control sequence failed or an information transfer was not required and the disk drive terminated the sequence. 014_8– The sequencer terminated an information transfer.
5	DCA-2 status bit 5	020_8– The read or write operation was terminated due to ID miscompare, disk drive detected error, or disk drive voltage fault. 021_8– A parity error occurred on bus A. 022_8– A parity error occurred on bus B.
6	DCA-2 status bit 6	024_8– A parity error occurred on the ending status byte. 040_8– A parity error occurred on byte 0 of the data.
7	DCA-2 status bit 7	100_8– A parity error occurred on byte 1 of the data. 200_8– An error was detected during the ending status sequence.
8	Single-bit error	SECDED circuitry in the 3YC option corrected 1 bit of write data.
9	Double-bit error	Multiple bits were in error and SECDED circuitry in the 3YC options was unable to correct them.
10	Voltage fault –4.5 V	The –4.5-V is out of range on the channel adapter.
11	Voltage fault +5.0 V	The +5.0-V is out of range on the channel adapter.
12	RAM parity error bit 0	A sequencer parity error occured on bits 0, 4, 8, 12, 16, 20, 24, and 28.
13	RAM parity error bit 1	A sequencer parity error occured on bits 1, 5, 9, 13, 17, 1, 25, and 29.
14	RAM parity error bit 2	A sequencer parity error occured on bits 2, 6, 10, 14, 18, 22, 26, and 30.
15	RAM parity error bit 3	A sequencer parity error occured on bits 3, 7, 11, 15, 19, 23, 27, and 31.

SECDED Status

When status select bit 1 is 0 and bit 0 is 1, the DCA2:12 channel function transfers the SECDED status to the accumulator (refer to Table 12-6).

Table 12-6. SECDED Status

Bit	Name	Description
0	Syndrome bit 0	These bits contain the syndrome bits from the 3YC option SECDED circuitry.
1	Syndrome bit 1	
2	Syndrome bit 2	
3	Syndrome bit 3	
4	Syndrome bit 4	
5	Syndrome bit 5	
6	Syndrome bit 6	
7	Syndrome bit 7	
8	Single-bit count bit 0	These bits contain the number of times the 3YC option detected a single-bit error.
9	Single-bit count bit 1	
10	Single-bit count bit 2	
11	Single-bit count bit 3	
12	Double-bit count bit 0	These bits contain the number of times the 3YC option detected a double-bit error.
13	Double-bit count bit 1	
14	Double-bit count bit 2	
15	Double-bit count bit 3	

Transfer Count Status

When status select bit 1 is 1 and bit 0 is 0, the DCA2:12 channel function transfers the transfer count status to the accumulator (refer to Table 12-7). This value represents the number of parcels remaining to be transferred to the drive when an operation was halted. A non-zero value indicates that an error caused the data transfer sequence to abort.

Table 12-7. Transfer Count Status

Bit	Name	Description
0 through 15	Transfer count bits 0 through 15	These bits contain the current value of the transfer counter in the 3DI option. This value represents the number of parcels remaining to be transferred when an operation sequence was aborted.

Tag Status

When the status select bits are both 1, the DCA2:12 channel function transfers the tag status to the accumulator (refer to Table 12-8). This status represents the state of the IPI interface when the status was requested.

Table 12-8. Tag Status

Bit	Name	Description
0	Attention In signal	State of the Attention In signal from the 3DE option.
1	Slave In signal	State of the slave In signal from the 3DE option.
2	Sync In signal	State of the Sync In signal from the 3DE option.
3	Not used	This bit is not used.
4	Select Out signal	State of the Select Out signal from the 3DF option.
5	Master Out signal	State of the Master Out signal from the 3DF option.
6	Sync Out signal	This bit displays the state of the Sync Out signal from the 3DF option.
7-15	Not used	These bits are not used

Drive Ending Status

When the status select bits are both 0, the DCA2:13 channel function transfers the drive ending status to the accumulator. The drive ending status parcel contains one or two copies of the IPI-2 ending status byte as described in Table 12-9. Refer to Table 12-10 for a description of each bit of the IPI-2 ending status byte.

Table 12-9. Drive Ending Status

Bit	Name	Description
0	Final drive ending status bit 0	These bits contain the final drive ending status byte as defined in Table 12-10.
1	Final drive ending status bit 1	
2	Final drive ending status bit 2	
3	Final drive ending status bit 3	
4	Final drive ending status bit 4	
5	Final drive ending status bit 5	
6	Final drive ending status bit 6	
7	Final drive ending status bit 7	
8	Initial drive ending status bit 0	These bits contain the initial drive ending status byte as defined in Table 12-10.
9	Initial drive ending status bit 1	
10	Initial drive ending status bit 2	
11	Initial drive ending status bit 3	
12	Initial drive ending status bit 4	
13	Initial drive ending status bit 5	
14	Initial drive ending status bit 6	
15	Initial drive ending status bit 7	

Initial Drive Ending Status

The initial drive ending status contains the IPI ending status on bus B after completion of a single, or the first of two, drive function sequences. For example, during a load position routine, the sequencer performs one drive function sequence. The drive ending status from this sequence is stored in the initial drive ending status while the final drive ending status is unused and remains zeros.

Final Drive Ending Status

The final drive ending status contains the second of two drive ending statuses received on bus B after a dual drive function sequence (refer again to Table 12-9). For example, during a write sector of data routine, the sequencer performs two drive function sequences. The initial drive ending status is received after the ID is read and compared. The final drive ending status is received after the data field has been written.

Table 12-10. Disk Drive Status on Bus B

Bit	Name	Description
0	Operation status bit 0	Bits — Description 00_8 – The disk drive executed the bus control command and is available. 01_8 – The disk drive rejected the bus control command and is busy.
1	Operation status bit 1	04_8 – The disk drive did not detect the address mark. 05_8 – The disk drive did not detect the sync byte.
2	Operation status bit 2	06_8 – ECC error (not used by CRI) 07_8 – Verify ID miscompare (not used by CRI)
3	Operation status bit 3	10_8 – An operation exception occurred. The exception status may be read for more information (refer to Table 12-26). 14_8 – An unsolicited exception occurred. The unsolicited exception status must be read before continuing (refer to Table 12-27).
4	Time dependent operation	The last command has not been completed by the disk drive. The disk drive will set the Attention In signal when it completes the command.
5	Odd byte transfer	The last information transfer contained an odd number of bytes. If set, the last byte transferred on bus B is not valid.
6	Bus parity error	The disk drive detected a parity error on a bus control command, information transfer, or controller status.
7	Good transfer	The disk drive did not detect a parity error on a bus control command, information transfer, or controller status.

ID Parameter 0 Status

When status select bit 1 is 0 and bit 0 is 1, the DCA2:13 channel function transfers the ID parameter 0 status to the accumulator. Refer to Table 12-11 for a description of the ID parameter 0 status bits.

Table 12-11. ID Parameter 0 Status

Bits	Name	Description
0 through 15	Cylinder address (ID parameter 0)	These bits contain the current value of the cylinder register in the 3DG option. This represents the expected cylinder address rather than the actual contents of the sector ID field.

ID Parameter 1 Status

When status select bit 1 is 1 and bit 0 is 0, the DCA2:13 channel function transfers the ID parameter 1 status to the accumulator. Refer to Table 12-12 for a description of each bit of the ID parameter 1 status.

Table 12-12. ID Parameter 1 Status

Bit	Name	Description
0	Sector address bit 0	These bits contain the current sector address. This represents the expected sector address rather than the actual contents of the sector ID field.
1	Sector address bit 1	
2	Sector address bit 2	
3	Sector address bit 3	
4	Sector address bit 4	
5	Sector address bit 5	
6	Head address bit 0	These bits contain the current head address. This represents the expected head address rather than the actual contents of the sector ID field.
7	Head address bit 1	
8	Head address bit 2	
9	Head address bit 3	
10	Head address bit 4	
11	Not used	This bit is not used.
12	Read protection	The RP bit was set in the ID field read from the sector. This bit is presently unsupported and should be 0.
13	Write protection	The WP bit was set in the ID field read from the sector. This bit is presently unsupported and should be 0.
14	Not used	This bit is not used.
15	Not used	This bit is not used.

DCA-3 Channel Adapter Statuses

General Status

Table 12-13 describes each bit of general status as assembled by the Online Hardware Performance Analyzer (OLHPA) .

Table 12-13. DA-301 General Status Description

Bit	Name	Description
0	Spindle 0 Busy & Done	An error on spindle 0 or its data path resulted in a Busy/Done condition. (Read from busy/done status bit 0).
1	Spindle 1 Busy & Done	An error on spindle 1 or its data path resulted in a Busy/Done condition. (Read from busy/done status bit 1).
2	Spindle 2 Busy & Done	An error on spindle 2 or its data path resulted in a Busy/Done condition. (Read from busy/done status bit 2).
3	Spindle 3 Busy & Done	An error on spindle 3 or its data path resulted in a Busy/Done condition. (Read from busy/done status bit 3).
4	Spindle 4 Busy & Done	An error on spindle 4 or its data path resulted in a Busy/Done condition. (Read from busy/done status bit 4).
5	Voltage fault	The +5.0V or –4.5V is out of range on the channel adapter. (Read from interrupt status bit 4 ORed with inverted bit 5).
6	Single-bit error	A write data bit was in error and corrected with SECDED circuitry in the 7DL option. (Read from SECDED status single-bit count $\neq 0$).
7	Double-bit error	More than one write data bit was in error and SECDED circuitry in the 7DL option was unable to correct them. (Read from SECDED status double-bit count $\neq 0$).
8	Bus Control / Parameter Fault	The drive rejected a bus control or parameter. (Read from drive Status Response Block byte 3, bit 5).
9	Off Cylinder Fault	A spindle's heads were not positioned over the correct cylinder during a seek, or the heads moved off a cylinder during a data transfer. (Read from drive Status Response Block byte 8, bit 6).
10	Seek Fault	An error occurred during a seek, read data, or write data bus control operation. (Read from drive Status Response Block byte 0, bit 2).
11	Spindle Fault	An error occurred during a spin-up, spin-down, read/verify data, or write data bus control operation. (Read from drive Status Response Block byte 0, bit 1).
12	Completion Fault	The drive detected a fault other than a read, write, seek, or spindle fault while completing a command or data control. (Read from drive Status Response Block byte 0, bit 0).
13	ID ECC error	The ID field ECC read from the disk drive did not match the ECC generated by one or more of the 7DN options. (Read from interrupt status bit 9 AND bit 10).
14	ID compare error	The ID of a sector read from one or more of the spindles did not compare to the expected ID stored in one or more of the 7DN options. (Read from interrupt status bit 8).
15	Data ECC error	The data field (ECC) read from the disk drive did not match the ECC generated by one of the 7DN options. (Read from interrupt status bit 9 ANDed with inverted bit 10).

Interrupt Status

The DCA3:12 function with an accumulator value of 0 returns interrupt status to the channel. Refer to the "DCA-3 Channel Functions" section of this manual for additional information on the interrupt status. Table 12-14 defines the interrupt status bits.

Table 12-14. Interrupt Status Bits

Bit	Name	Description
0	Spindle parity error (Bus byte parity error)	A byte parity error was detected by a 7DN option when data was read out of its deskew buffer.
1	IPI Sequence error	A drive function was attempted from an invalid initial state or a select function timed out.
2	Lost data error	Data transfers between the EIOP buffer and the DCA3 deskew buffer did not occur fast enough. Loss of rotational synchronization by a spindle can cause lost data errors. During chained read/write operations, this error may be the result of a data parity error or an ECC error on the previous sector.
3	Ending status error	A spindle's ending status bits 2^0 through 2^3 are non-zero, bit 2^7 is zero, or the ending status has a parity error.
4	-4.5V voltage fault	The –4.5 V is out of range on the DCA-3.
5	+5.0V voltage good	When set to a 0, this bit indicates that the +5.0 V is out of range on the DCA-3.
6	SECDED error	Corruption of write data was detected by the 7DL option.
7	Data parity error (Striped parity error)	The parity regenerated on the data read from spindles 0 through 3 did not match the parity from spindle 4. This bit can only set if all 5 spindles are enabled during a striped read.
8	ID compare error	The ID of a sector read from a spindle did not compare to the expected ID stored in the appropriate 7DN option. This bit cannot be set on a DCA3:5, function 21 command because the ID compare circuitry on the 7DN option is disabled during ID Verify routines.
9	ECC error	The newly generated ECC did not match the ECC read from a spindle. This error can occur on the ID or data field of a sector. Refer to interrupt status bits 8, 10, 12, and 13 for additional information.
10	ID error	A read or write operation was stopped by an ID error.
11	Hideable flaw	The ID read from a spindle sector was marked as having a hideable flaw. This bit is informational only.
12	Unhidable flaw	The ID read from a spindle sector was marked as having an unhideable flaw.
13	ID field flaw	The ID read from a spindle sector was marked as having an unhideable, ID field flaw.
14	Write protect	The ID read from a spindle sector was marked as write protected.
15	Read protect	The ID read from a spindle sector was marked as read protected. This bit is informational only.

SECDED Status

The DCA3:12 function with an accumulator value of 1 causes the SECDED status to be returned to the channel. Table 12-15 defines the SECDED status bits.

Table 12-15. SECDED Status Bits

Bit	Name	Description
0	Syndrome bit 0	These bits contain the syndrome bits generated by the 7DL option on SECDED errors. (Syndrome only valid for most recent single-bit error)
1	Syndrome bit 1	
2	Syndrome bit 2	
3	Syndrome bit 3	
4	Syndrome bit 4	
5	Syndrome bit 5	
6	Syndrome bit 6	
7	Syndrome bit 7	
8	Single-bit error count 0	These bits contain the number of times the 7DL option detected a single-bit error. All four bits are set if the error count exceeds 17_8.
9	Single-bit error count 1	
10	Single-bit error count 2	
11	Single-bit error count 3	
12	Double-bit error count 0	These bits contain the number of times the 7DL option detected a double-bit error. All four bits are set if the error count exceeds 17_8.
13	Double-bit error count 1	
14	Double-bit error count 2	
15	Double-bit error count 3	

Transfer Count Status

The DCA3:12 function with an accumulator value of 2 causes transfer count status to be returned to the channel. Table 12-16 defines the transfer count status bits.

Table 12-16. Transfer Count Status Bits

Bits	Name	Description
0 through 15	Transfer count bits 0 through 15	These bits contain the current value of the transfer counter on the DCA-3. This value represents the number of parcels remaining to be transferred when an operation sequence was aborted.

IPI Tag Status

The DCA3:12 function with an accumulator value of 3 causes the IPI tag status to be returned to the channel. Table 12-17 defines the control bus status bits.

Table 12-17. IPI Tag Status Bits

Bit	Name	Description
0	Select Out	These bits indicate the state of the intelligent peripheral interface (IPI) when the status was read.
1	Slave In	
2	Master Out	
3	Sync In	
4	Sync Out	
5	Attention In	
6	Gate Bus A out	Data sent out on Bus A.
7	Gate Bus B out	Data sent out on Bus B.
8-15	Not used	These bits are not used.

Busy Status

The DCA-3:12 function with an accumulator value of 4 causes busy status to be returned to the channel. Table 12-18 defines the busy status bits.

Table 12-18. Busy Status Bits

Bit	Name	Description
0	Spindle 0 busy	Spindle 0 is busy
1	Spindle 1 busy	Spindle 1 is busy
2	Spindle 2 busy	Spindle 2 is busy
3	Spindle 3 busy	Spindle 3 is busy
4	Spindle 4 busy	Spindle 4 is busy
5–15	Not used	These bits are not used

Done Status

The DCA3:12 function with an accumulator value of 5 causes the done status to be returned to the channel. Table 12-19 defines the done status bits.

Table 12-19. Done Status Bits

Bit	Name	Description
0	Spindle 0 done	Spindle 0 is done
1	Spindle 1 done	Spindle 1 is done
2	Spindle 2 done	Spindle 2 is done
3	Spindle 3 done	Spindle 3 is done
4	Spindle 4 done	Spindle 4 is done
5–15	Not used	These bits are not used

DMA Acknowledge Pending Status

The DCA3:12 function with an accumulator value of 6 causes the direct memory access (DMA) acknowledge pending status to be returned to the channel. Table 12-20 defines the DMA acknowledge pending status bits.

Table 12-20. DMA Acknowledge-pending Status Bits

Bit	Name	Description
0	Spindle 0 pending	Spindle 0 has a DMA acknowledge pending
1	Spindle 1 pending	Spindle 1 has a DMA acknowledge pending
2	Spindle 2 pending	Spindle 2 has a DMA acknowledge pending
3	Spindle 3 pending	Spindle 3 has a DMA acknowledge pending
4	Spindle 4 pending	Spindle 4 has a DMA acknowledge pending
5–15	Not used	These bits are not used

Drive Ending Status

When the status select bits are both 0, the DCA3:13 channel function transfers the drive ending status to the accumulator. Refer to Table 12-21 for a description of the drive ending status parcel. On single drive functions the drive ending status parcel will contain two copies of the initial drive ending status byte. On dual drive functions this parcel will contain separate initial and final drive ending status bytes. The Ending Status byte is described in Table 12-22.

Table 12-21. Drive Ending Status

Bit	Name	Description
0	Final drive ending status bit 0	These bits contain the final drive ending status byte. Refer to Table 12-22.
1	Final drive ending status bit 1	
2	Final drive ending status bit 2	
3	Final drive ending status bit 3	
4	Final drive ending status bit 4	
5	Final drive ending status bit 5	
6	Final drive ending status bit 6	
7	Final drive ending status bit 7	
8	Initial drive ending status bit 0	These bits contain the initial drive ending status byte. Refer to Table 12-22.
9	Initial drive ending status bit 1	
10	Initial drive ending status bit 2	
11	Initial drive ending status bit 3	
12	Initial drive ending status bit 4	
13	Initial drive ending status bit 5	
14	Initial drive ending status bit 6	
15	Initial drive ending status bit 7	

Initial Drive Ending Status

The initial drive ending status contains the ending status byte returned on bus B after completion of a single, or the first of two, drive function sequences. For example, during a load position routine, the sequencer performs one drive function sequence. The drive ending status from this sequence is stored in the initial drive ending status (upper byte) and copied to the final drive ending status (lower byte).

Final Drive Ending Status

The final drive ending status contains the second of two drive ending statuses returned on bus B after a dual drive function sequence. For example, during a write sector of data routine, the drive performs two function sequences: read ID and write data. The initial drive ending status is received after the ID is read and compared. The final drive ending status is received after the write data has been transferred. On single drive function sequences, the final drive ending status (lower byte) is a copy of the initial drive ending status (upper byte).

Table 12-22. Ending Status Byte Definitions

Bit	Name	Description
0	Operation status bit 0	Decode 00_8 – The disk drive executed the bus control command and is available. 01_8 – The disk drive rejected the bus control command and is busy.
1	Operation status bit 1	04_8 – The disk drive did not detect the address mark. 05_8 – The disk drive did not detect the sync byte. 06_8 – ECC error (not used by CRI) 07_8 – Verify ID miscompare (not used by CRI) 10_8 – An operation exception occurred. The exception status (refer to Table 12-1), may be read for more information. 14_8 – An unsolicited exception occurred. The unsolicited exception status (refer to Table 12-1) must be read before continuing.
2	Operation status bit 2	
3	Operation status bit 3	
4	Time dependent operation	The last command has not been completed by the disk drive. The disk drive will set the Attention In signal when it completes the command.
5	Odd byte transfer	The last information transfer contained an odd number of bytes. If set, the last byte transferred on bus B is not valid.
6	Bus parity error	The disk drive detected a parity error on a bus control command, information transfer, or controller status.
7	Good transfer	The disk drive did not detect a parity error on a bus control command, information transfer, or controller status.

ID Parameter 0 Status

When status select bit 2^1 is 0 and bit 2^0 is 1, the DCA3:13 channel function transfers the ID parameter 0 statuses to the accumulator. Refer to Table 12-23 for a description of the ID parameter 0 status bits.

Table 12-23. ID Parameter 0 Status

Bits	Name	Description
0 through 15	Cylinder address (ID parameter 0)	These bits contain the expected cylinder value as read from the cylinder registers on the DCA-3. This represents the expected cylinder address rather than the actual contents of the sector ID field.

ID Parameter 1 Status

When status select bit 2^1 is 1 and bit 2^0 is 0, the DCA3:13 channel function transfers the ID parameter 1 status to the accumulator. Refer to Table 12-24 for a description of each bit of the ID parameter 1 status.

Table 12-24. ID Parameter 1 Status

Bit	Name	Description
0	Sector address bit 0	These bits contain the expected sector value as read from the sector register on the DCA-3. This represents the expected sector address rather than the actual contents of the sector ID field.
1	Sector address bit 1	
2	Sector address bit 2	
3	Sector address bit 3	
4	Sector address bit 4	
5	Sector address bit 5	
6	Head address bit 0	These bits contain the expected head value as read from the head register on the DCA-3. This represents the expected head address rather than the actual contents of the sector ID field.
7	Head address bit 1	
8	Head address bit 2	
9	Head address bit 3	
10	Head address bit 4	
11	Not used	This bit is not used.
12	Read protection (RP)	This bit is presently unsupported and must be set to 0.
13	Write protection (WP)	This bit is presently unsupported and must be set to 0.
14-15	Not used	These bits are not used.

Bus A and Bus B Data

When status select bit 2^1 is 1 and bit 2^0 is 1, the DCA3:13 channel function transfers the IPI bus A and bus B data bytes to the accumulator. Refer to Table 12-25 for a description of each bit of the bus A and bus B data.

Table 12-25. Bus A and Bus B Data

Bit	Name	Description
0	Bus B data bit 0	These bits indicate the data byte on bus B
1	Bus B data bit 1	
2	Bus B data bit 2	
3	Bus B data bit 3	
4	Bus B data bit 4	
5	Bus B data bit 5	
6	Bus B data bit 0	
7	Bus B data bit 1	
8	Bus A data bit 0	These bits indicate the data byte on bus A
9	Bus A data bit 1	
10	Bus A data bit 2	
11	Bus A data bit 3	
12	Bus A data bit 4	
13	Bus A data bit 5	
14	Bus A data bit 6	
15	Bus A data bit 7	

300 Series Disk Drive Statuses

The following subsection describes the statuses obtained from the 300 series disk drives. These status bytes are divided into two categories or blocks. The first group of status bytes are referred to as the Status Response Block, the second group of status bytes are referred to as the Extended Status Block.

Drive Status Response Block

The status response block is 32 bytes of IPI-2 status information transferred from the disk drive to the DCA-2. The status response block is read when the sequencer sends a bus control code for read status (44_{16}) to the disk drive over bus A. Table 12-26 through Table 12-56 describe each bit in the statuses' response blocks.

Table 12-26. Exception Status (Byte 00_{16})

Bit	Name	Description
0	Completion fault	The drive detected a fault other than a Read, Write, Seek, or Spindle fault while completing a command or data control. At least one bit will be set in bytes 8 through iF describing the fault.
1	Spindle fault	An error occurred during a spin-up, spin-down, read/verify data, or write data bus control operation. At least one bit will be set in bytes 8 through iF describing the fault.
2	Seek fault	An error occurred during a seek, read/verify data, or write data bus control operation. At least one bit will be set in bytes 8 through iF describing the fault.
3	Write fault	An error occurred during a write data bus control operation. At least one bit will be set in bytes 8 through iF describing the fault.
4	Read fault	An error occurred during a read/verify bus control operation. At least one bit will be set in bytes 8 through iF describing the fault.
5	Bus control exception	The disk drive did not accept the last bus control command. At least one bit will be set in bytes 6-7 describing the fault.
6	Unsolicited exception	An exception condition exists at the drive that is not associated with the transfer of a Bus Control. At least one bit in bytes 2-5 will be set to indicate the nature of the exception.
7	Status response	This bit is always set to 0 for a status response.

Table 12-27. Exception Status (Byte 01_{16})

Bit	Name	Description
0 through 5	Reserved	Set to zero.
6	Buffer operation exception	N/A
7	Idle exception	An exception has occurred that was not associated with the transfer of a bus control. At least one bit will be set in bytes 8 through 1F describing the exception.

Table 12-28. Unsolicited Exception Status (Byte 02_{16})

Bits	Name	Description
0	Alternate port semaphore 0	The alternate port received a set alternate port semaphore 0 function code.
1	Alternate port semaphore 1	The alternate port received a set alternate port semaphore 1 function code.
2	Alternate port buffer control changed	N/A
3	Alternate port target modifier changed	The target modifier parameter has changed from the alternate port.
4	Alternate port format complete	The alternate port received a notify alternate port of format completion function code.
5	Alternate port format specification changed	The alternate port accepted a format specification.
6	Alternate port priority select	The alternate port completed a selection sequence with the priority select bit or priority select and priority hold bits set.
7	Slave reset complete	The drive has completed a slave reset or power-on reset.

Table 12-29. Unsolicited Exception Status (Byte 03_{16})

Bit	Name	Description
0	Ready transition	The drive has changed from a not ready to a ready condition.
1	Not ready transition	The drive has changed from a ready to a not ready condition.
2	Failure detected alarm	The drive has detected an internal failure.
3	Failure pending alarm	The drive has detected a pending internal failure. Remove critical data from the drive immediately.
4	Port enabled	N/A
5	Service alarm	N/A

Table 12-29. Unsolicited Exception Status (Byte 03_{16}) (continued)

Bit	Name	Description
6	Spindle sync transition, locked to unlocked	Spindle sync is lost.
7	Spindle sync transition, unlocked to locked	Spindle synchronization is achieved.

Table 12-30. Unsolicited Exception Status (Byte 04_{16})

Bits	Name	Description
0 through 5	Reserved	Set to zero.
6	Alternate port logical reset	A logical reset at the alternate port affected a common resource. This bit is not set if the logical reset does not affect this port.
7	Spindle sync reference signal fault	The spindle sync signal is lost.

Table 12-31. Unsolicited Exception Status (Byte 05_{16})

Bits	Name	Description
0 through 7	Reserved	Set to zero.

Table 12-32. Bus Control/Parameter Exception Status (Byte 06_{16})

Bits	Name	Description
0	Function code context	A valid function code has transferred that is out of context with the state of the drive.
1	Invalid function code	An invalid function code has transferred to the drive.
2	Unsupported function code	A valid function code has transferred that is not supported by the drive.
3	Data control late	A valid data control has transferred but orientation is lost.
4	Bus control context	A valid bus control transferred out of context with the state of the drive.
5	Unsupported bus control	A valid bus control is transferred that has not supported by the drive.
6	Invalid parameter	A valid bus control has transferred to the drive, but one or more of the parameters is invalid, for instance, out of range.
7	Invalid bus control	An invalid bus control has transferred to the drive.

Table 12-33. Bus Control/Parameter Exception Status (Byte 07_{16})

Bit	Name	Description
0 through 5	Reserved	Set to zero.
6	Local spinup context	N/A
7	Write protect context	A write data control has transferred and the write protect switch is on or a write data control was transferred and the thermal compensation process timer had expired for the selected head. In the latter case, Byte 15, Bit 6 in status response will also be set.

Table 12-34. Slave Exception Status (Byte 08_{16})

Bits	Name	Description
0	Actuator temperature fault	N/A
1	Logic temperature fault	N/A
2	Voltage fault	N/A
3	Fan alarm	N/A
4	Spindle sync fault	A fault related to spindle synchronization was detected.
5	Head select fault	N/A
6	Off cylinder fault	The drive did not achieve track-following in the required time during the completion of a seek, or lost track-following during execution of data control.
7	Speed fault	An out-of-speed tolerance condition was detected during execution of a spin up function code or during execution of a data control.

Table 12-35. Slave Exception Status (Byte 09_{16})

Bits	Name	Description
0, 1	Reserved	Set to zero.
2	Data recovery fault	N/A
3	Data Strobe fault	N/A
4	Head offset fault	A write type data control has been received and the data heads were in an offset position.
5	Write Transition fault	N/A
6	Write Current fault	N/A
7	Write Circuit fault	A failure was detected in the write circuit during completion of a write data control.

Table 12-36. Slave Exception Status (Byte $0A_{16}$)

Bits	Name	Description
0 through 7	Reserved	Set to zero.

Table 12-37. Slave Exception Status (Byte $0B_{16}$)

Bits	Name	Description
0 through 7	Reserved	Set to zero.

Table 12-38. Buffer Exception Status (Byte $0C_{16}$)

Bits	Name	Description
0 through 7	Reserved	Set to zero.

Table 12-39. Buffer Exception Status (Byte $0D_{16}$)

Bits	Name	Description
0 through 7	Reserved	Set to zero.

Table 12-40. Buffer Exception Status (Byte $0E_{16}$)

Bits	Name	Description
0 through 7	Reserved	Set to zero.

Table 12-41. Buffer Exception Status (Byte $0F_{16}$)

Bits	Name	Description
0 through 7	Reserved	Set to zero.

Table 12-42. IDM Detected Faults (Byte 10_{16})

Bits	Name	Description
0	Bus control context E	A field data control was issues when Byte 03h Bit 0 of the currently loaded format specification is set to zero.
1	Bus control context D	A sector type data control has been received that operates on the second field when the IDM is programmed for one field per sector.
2	Bus control context C	A sector type data control has been received that operates on the third field when the IDM is programmed for two fields per sector.
3	Bus control context B	An at target type data control is received by RPS is not enabled.
4	Bus control context A	A data control or position type command was received and the device was not ready.
5	Field overrun	The IDM was programmed for a field length greater than the actual field length.
6	Sector overrun	The IDM detected a sector byte count error. This error occurs if the IDM is programmed for a sector length greater than the actual sector length.
7	Track overrun	The IDM detected an invalid track length value. This error can occur if a fake index pulse is received.

Table 12-43. Drive Control Module Detected Faults (Byte 11_{16})

Bit	Name	Description
0	AE error	Read gate and write gate are active at the same time or both AE modules are selected simultaneously.
1	Sector overrun	Read gate or write gate was active at the time an index of sector pulse was seen.
2	Servo processor lost	An error in the SP was detected. The actuator will retract.
3	Three fake SIDs detected	Write gate is active and three SIDs in a row went undetected.
4	Servo write inhibit	Write gate is active while the SP has write inhibit active.
5	Microjog write inhibit	Write gate is active while the head is in the read microjog position.
6	IP retract error	Write gate is active while the actuator is retracted.
7	Write with no sector pulses	Write gate is active but sector enable is inactive.

Table 12-44. Drive Control Module Detected Faults (Byte 12_{16})

Bit	Name	Description
0	IDM write parity error	Write gate is active and the drive control module detects a parity error in the data received from the IDM.
1	PRDF write parity error	Write gate is active and the PRDF detects a parity error in the data received from the drive control module.
2	PRDF register write error	A PRDF register access was attempted while read gate or write gate was active.
3 through 7	Undefined	

Table 12-45. Drive Control Module Detected Faults (Byte 13_{16})

Bits	Name	Description
0	Motor speed error	The SP has detected that the motor is out of speed tolerance.
1	Motor sync error	The SP has detected that the motor is no longer in sync with the reference pulse.
2	Fake and extra index error	A fake index pulse was generated and an extra index pulse was detected in the same Index to index revolution.
3	PRDF read parity error	Read gate is active and the drive control module detects a parity error in the data received from the PRDF.
4	TCR parity error	A parity error in the data supplied by the tangential correction RAM was detected.
5	AE not ready	Read gate or write gate is active and the ARM electronics is not operational.
6, 7	Undefined	

Table 12-46. Drive Control Module Detected Faults (Byte 14_{16})

Bits	Name	Description
0	Servo channel disable	Read gate and SP channel inhibit are active at the same time. The read operation will continue but the data sent is all ones which will prevent the IDM from finding the sync byte. This error is reset at the next activation of read gate.
1	Read/write inhibit	Read gate and SP write inhibit are active at the same time. This error does not stop a read in progress and is reset at the next activation of read gate.
2	High gain during read gate	Read gate and high gain are active at the same time. This error does not stop a read in progress and is reset at the next activation of read gate.
3	Thermal asperity error detected	The PRDF detected a thermal asperity while read gate was active. This error is reset on the next activation of read gate. This error will not stop a read in progress.
4	Fake index	The drive control module did not detect the index SID during a disk revolution.

Table 12-46. Drive Control Module Detected Faults (Byte 14_{16})

Bits	Name	Description
5	Extra index	The drive control module detected more than one index SID during one revolution.
6	IP channel disable	Read gate is active while the read channel is disabled. The read operation will continue but the data sent is all ones which will prevent the IDM from finding the sync byte.
7	Thermal asperity error detected (latched)	The PRDF detected a thermal asperity while read gate was active. Unlike Bit 3, this error is latched. Note that a read in progress will not be interrupted.

Table 12-47. IDM/IP Detected Errors (Byte 15_{16})

Bits	Name	Description
0	Channel sync error	The R/W channel detected read data prior to detecting a valid sync byte.
1	Invalid IDM interrupt	The IDM interrupted the microprocessor but no bits were on in the common interrupts register or the command field in the task control block is invalid.
2	IDM track synchronization attempt failed	The IDM failed in its attempt to synchronize to the track within 2 revolutions of the disk after track synchronization was lost. The IDM loses track synchronization with a track when a new format specification is accepted by the drive, a position calibration is performed or a recalibrate operation is performed.
3	IDM register write/verify failure	This failure was detected during a load format operation. Format information written to an IDM or drive control module register could not be verified by a subsequent read. The format specification is not loaded.
4	SAT miscompare	
5	Reserved	Set to zero.
6	Write data control rejected	Write data control rejected because the thermal calibration process timer for the selected head has expired.
7	IDM detected parity error	The IDM detected a parity error during the previous read operation.

Table 12-48. Servo / IP Error Codes (Bytes 16_{16} and 17_{16})

Bit	Name	Description
Error code (octal)	Error code (hex)	Description Byte 16_{16} contains the error code returned from the Servo processor. Byte 17_{16} contains the error code returned from the Interface processor.
01	01	Spindle speed too fast
02	02	Spindle speed too slow
11	09	Spindle out of sync
12	0A	Master sync pulse lost
13	0B	Slave index lost
14	0C	No sync, motor not started
15	0D	No sync, actuator retracted
21	11	No servo interrupt seen
22	12	Seek settle timeout
23	13	Course Offtrack
24	14	Three fake SIDs
25	15	Unexpected guardband detected
26	16	Seek settle overshoot
27	17	Seek timeout
30	18	Target cylinder out of range
31	19	Invalid command while retracted
32	1A	Update without read bit selected
33	1B	Max seek velocity exceeded
34	1C	Head number out of range
35	1D	Reference track out of range
36	1E	Invalid servo command
37	1F	Velocity high at settle handoff
40	20	Offset out of range
41	21	OD GB not found / ID GB seen
42	22	OD GB not found / data band seen
43	23	OD GB not found / ID and data seen
44	24	OD GB not found
45	25	Six consecutive OD GBs not found
46	26	Six consecutive data bands not seen
47	27	Data band type 0 not found
50	28	Motor start bit not active
51	29	SP lost bit active
52	2A	IP initiated hardware reset
53	2B	SP initiated hardware reset

Table 12-48. Servo / IP Error Codes (Bytes 16_{16} and 17_{16}) (continued)

Bit	Name	Description
54	2C	Path reset
55	2D	Bad coherence
56	2E	Demod conversion too long
57	2F	Demod conversion in progress
60	30	OD GB seen prior to ID GB
61	31	Data band seen prior to ID GB
62	32	Command invalid while NVS not loaded
63	33	Mult Sid offsets error in TC
64	34	NVSRAM checksum error in download
65	35	Drive control module RAM incompatible with SP code
100	40	Motor stuck error
101	41	Spindle motor control error
102	42	Motor spinup timeout error
103	43	Motor spinup failed
104	44	Hallint got invalid interrupt
110	48	Motor sync-up timed out
120	50	Asynchronous servo error
121	51	Drive control module sanity error
122	52	A servo command is already active
123	53	SP did not finish command in time
124	54	IP sanity error
125	55	PATH sanity error
126	56	Servo error
140	60	Degraded mode/motor not running
141	61	Spinup actuator error
142	62	Bringup actuator error
150	68	Divide by zero error
151	69	Invalid program counter
152	6A	Unused op code
160	70	write primitive timeout
161	71	Read primitive timeout
162	72	Track running timeout
170	78	PRDF accumulation measurement failed
200	80	IP general purpose register
201	81	IP stack register
202	82	IP timer control

Table 12-48. Servo / IP Error Codes (Bytes 16_{16} and 17_{16}) (continued)

Bit	Name	Description
203	83	IP register initialization
220	90	Instruction memory checksum
221	91	control store RAM
222	92	Tangential correction RAM
223	93	PRDF palette RAM
224	94	PRDF digital filter RAM
225	95	SP RAM in drive control module
240	A0	IP to IDM communication
241	A1	IDM internal diagnostic
242	A2	IP to drive control module communication
243	A3	IP to PRDF communication
244	A4	IP to SP communication
245	A5	Vital product data not written
246	A6	Select file type servo command
247	A7	Skip bias map error
260	B0	Spindle speed out of tolerance
261	B1	Index pulse not generated by the drive control module
262	B2	Sector pulse not generated by the drive control module
263	B3	Initial recalibration failed
264	B4	Initial thermal update failed
265	B5	Disk write test failed
266	B6	Delta fly height measurement failed
267	B7	Invalid interrupt during BAT
270	B8	Initial retract failed
271	B9	Cannot seek to HSC cylinder
272	BA	Position calibration operation failed
300	C0	Three fake SIDs
301	C1	AE
302	C2	Fake/extra index
303	C3	SP lost
304	C4	Sector overrun
305	C5	Microjog write inhibit
306	C6	SP write inhibit
307	C7	Write with no sector pulses
310	C8	Motor speed
311	C9	PRDF write parity

Table 12-48. Servo / IP Error Codes (Bytes 16_{16} and 17_{16}) (continued)

Bit	Name	Description
312	CA	PRDF read parity
313	CB	IDM write parity
314	CC	TCR parity
315	CD	IP retract
316	CE	SP asynchronous message
317	CF	AE not ready
320	D0	Drive control module fault interrupt bits set
321	D1	Motor sync failure

Table 12-49. Failure Detected Status (Byte 18_{16})

Bits	Name	Description
0	Motor spinup failed	An attempt to start the motor failed.
1	Sector generation fault	A failure was detected in the circuitry that generates the sector pulse.
2	Index generation fault	A failure was detected in the circuitry that generates the index pulse.
3	Initial thermal update failed	The servo update operation, executed as part of the spindle motor start , failed.
4	Initial recalibrate failed	The servo recalibrate operation, executed as part of spindle motor start, failed.
5	Initial retract failed	The servo retract operation, executed as part of spindle motor start, failed.
6	VPD invalid	Vital product data stored on the EEPROM is invalid.
7	MR offset fault	A failure was detected while trying to write the MR offsets loaded flag in SP RAM.

Table 12-50. Failure Detected Status (Byte 19_{16})

Bit	Name	Description
0, 1	Reserved	Set to zero.
2	DRP step failed	The action required by the next DRP step, initiated by the increment slave data recovery level function code, failed.
3	SP RAM write fault	An attempt by the IP to write a word to the servo processor RAM failed.
4	SP RAM read fault	An attempt by the IP to read a word from the servo processor RAM failed.
5	Reference track data length invalid	A length parameter in the reference track data stored in the EEPROM is invalid.

Table 12-50. Failure Detected Status (Byte 19_{16}) (continued)

Bit	Name	Description
6	Read/verify overrun	An index or sector pulse is detected during read or verify operations when read gate is active.
7	Command wrap fault	The read/write channel control lines are in an invalid state during a read or write operation.

Table 12-51. IDM/IP Detected Errors (Byte $1A_{16}$)

Bit	Name	Description
0 through 2	Reserved	Set to zero.
3	Save format specification failed	The format specification, accepted by the drive as a result of a load format specification bus control, was initialized but the attempt to save it in the EEPROM failed.
4	IDM track synchronization attempt failed	The IDM failed to resynchronize to the track within 2 revolutions of the disk after track synchronization was lost. The IDM loses track synchronization with a track when a new format specification is accepted by the drive, a position calibration is performed or a recalibrate operation is performed.
5	Disable secondary update failed	A failure was detected while trying to write the servo RAM location necessary to disable position calibration at the secondary tracks. The controller will see the time needed to perform a position calibration increase.
6	Spindle speed check failed	A BATS-2 failure is detected in the index pulse generation circuitry or the motor is running too slow.
7	SP code load failed	The load of the SP code into the drive control module RAM failed.

Table 12-52. Vendor Unique Status (Byte $1B_{16}$)

Bits	Name	Description
0 through 7	Reserved	Set to zero.

Table 12-53. Failure Pending Status (Byte $1C_{16}$)

Bit	Name	Description
0	Write test failed	The write test, executed as part of spindle motor start, failed.
1	VPD invalid	Vital product data stored in the EEPROM is invalid.
2	Servo degraded	The controller gains or velocity profile data stored in the EEPROM is invalid. Default values are used instead.

Table 12-53. Failure Pending Status (Byte $1C_{16}$)

Bit	Name	Description
3	Read/write degraded	The MR head offset data stored in the EEPROM is invalid. Default values are used instead.
4	Write mode degraded	The write current or write precompensation data stored in the EEPROM is invalid. Default data is used instead.
5	PRDF degraded	Loading of the palette RAM with the EEPROM stored data or the default data failed. This bit is also set if the virtual equalization table and/or the cylinder band stored in the EEPROM is invalid.
6	PRDF RAM check fault	The read/write test of the PRDF palette RAM or digital filter RAM failed.
7	TCR R/W fault	An error was detected while reading data from or writing data to the tangential correction RAM.

Table 12-54. Failure Pending Status (Byte $1D_{16}$)

Bits	Name	Description
0 through 6	Reserved	Set to zero.
7	PFA limit exceeded	A predictive failure limit has been exceeded.

Table 12-55. EEPROM Data Faults (Byte $1E_{16}$)

Bits	Name	Description
0	Checksum failure	Delta fly height data checksum failed
1	Reserved	Set to zero.
2	Checksum failure	Reference track data checksum failed
3	Checksum failure	Write precompensation Array checksum failed
4	Checksum failure	Write current array checksum failed
5	Checksum failure	Cylinder band table checksum failed
6	Checksum failure	Virtual equalization table checksum failed
7	Checksum failure	Palette RAM data checksum failed

Table 12-56. EEPROM Data Faults (Byte $1F_{16}$)

Bits	Name	Description
0 through 5	Reserved	Set to zero.
6	Checksum failure	Format store checksum failed
7	Checksum failure	Vital product data checksum failed

Drive Extended Status Block

The drive extended status block is 20 status bytes transferred from the disk drive in response to a bus control code for Read Extended Status (48_{16}). Table 12-57 through Table 12-77 describe each bit in the drive extended status block.

Table 12-57. Interface Flags Status (Byte 00_{16})

Bits	Name	Description
0	Port 0 enabled	Port 0 on the drive is enabled
1	Port 1 enabled	Port 1 on the drive is enabled
2, 3	Reserved	Set to zero.
4	Port 0 Extended Status	The port over which the read extended status response control received was identified as Port 0 by the drive.
5	Port 1 Extended Status	The port over which the read extended status response control received was identified as Port 1 by the drive.
6, 7	Reserved	Set to zero.

Table 12-58. Interface Flags Status (Byte 01_{16})

Bits	Name	Description
0	Reserve active	A reserve function code has been received over this port (logical explicit allegiance).
1	Target modifier active	The drive has accepted a Load Target Modifier command (08_{16}) on either port.
2, 3	Reserved	Set to zero.
4	No longer busy	"No longer busy" attention enabled at this port.
5	Status pending interrupt	Status pending interrupt attention enabled at this port.
6	RPS interrupt	RPS interrupt attention enabled at this port.
7	Command complete interrupt	Command complete interrupt attention enabled at this port.

Table 12-59. Data Recovery Flags Status (Byte 02_{16})

Bits	Name	Description
0	ECC correction enabled	N/A
1	ECC reporting enabled	N/A
2 through 7	Reserved	Set to zero.

Table 12-60. Data Recovery Flags Status (Byte 03_{16})

Bits	Name	Description
0, 1	Reserved	Set to zero.
2	Strobe Late	Late Data Strobe active
3	Strobe Early	Early Data Strobe active
4	Offset 1	1st level track offset active
5	Offset 2	2nd level track offset active
6	Offset 3	3rd level track offset active
7	Offset Direction	0 = offset out; 1 = offset in

Table 12-61. Slave Status Flags (Byte 04_{16})

Bits	Name	Description
0	Local spindle sync enabled	N/A
1	Sync locked	Spindle sync is enabled and locked within tolerance.
2	Master sync reference source enabled	The spindle is designated as the master sync reference source.
3	Spindle sync offset active	A load index offset command was accepted.
4	Sync enabled	Spindle sync is enabled.
5	Sync transition status enabled	The spindle sync transition status is enabled.
6	Spindle power on	Spindle power is enabled.
7	Write protected	The write protect switch is enabled.

Table 12-62. Slave Status Flags (Byte 05_{16})

Bits	Name	Description
0	Media Present	This bit is always set.
1	HDA ready	The spindle is at speed and the actuator is on cylinder.
2	Carriage locked	N/A
3	Local spinup mode active	The auto start switch is on and the spinup operation has completed successfully.
4	Format specification present	There is an initialized format spec at the drive.
5	Heads loaded	N/A

Table 12-62. Slave Status Flags (Byte 05_{16})

Bits	Name	Description
6	On cylinder	The drive actuator is positioned within tolerance.
7	At speed	The spindle is at operating speed and within tolerance.

Table 12-63. Slave Status Flags (Byte 06_{16})

Bits	Name	Description
0 through 4	Reserved	Set to zero.
5	Calibration enabled	Internal position calibration enabled
6	Period timer expired	The process timer for the selected head has expired.
7	Warm-up interval	The slave is currently in the internal calibration warm-up window.

Table 12-64. Table 12-65. Slave Status Flags (Byte 07_{16})

Bits	Name	Description
0 through 7	Reserved	Set to zero.

Table 12-66. Slave Alarms (Byte 08_{16})

Bits	Name	Description
0	Actuator over temp	N/A
1	Logic over temp	N/A
2	Voltage range error	N/A
3	Reserved	Set to zero.
4	Illegal head selected	N/A
5 through 7	Reserved	Set to zero.

Table 12-67. Table 12-68. Slave Alarms (Byte 09_{16})

Bits	Name	Description
2^0 through 7	Reserved	Set to zero.

Table 12-69. Slave Data Recovery Level Active (Bytes $0A_{16}$ and $0B_{16}$)

Bits	Name	Description
2^0 through 7		This parameter contains the number of the active slave data recovery Procedure Level. Default value = 0.

Table 12-70. Failure Pending Alarms (Byte $0C_{16}$)

Bits	Name	Description
2^0	HDA failure pending	HDA failure pending
1 through 7	Field replacement unit ID	N/A

Table 12-71. Slave Alarms (Byte $0D_{16}$)

Bits	Name	Description
2^0	HDA failure detected	The drive has detected a failure of the HDA.
1 through 7	Field replacement unit ID	N/A

Table 12-72. Vendor Unique Extended Status (Byte $0E_{16}$)

Bits	Name	Description
0 through 7	Reserved	Set to zero.

Table 12-73. Vendor Unique Extended Status (Byte $0F_{16}$)

Bits	Name	Description
0		Torque amplification used on previous motor start.
1	Port 0 disabled via Hardware Switch	Port 0 is disabled via the front panel DIP switches.
2	Port 1 disabled via hardware switch	Port 1 is disabled via the front panel DIP switches.
3	Spindle sync alternate source selected	Spindle sync B is selected as the spindle sync input port.
4 through 7	Reserved	Set to zero.

Table 12-74. Thermal Compensation Retry Counts (Byte 10_{16})

Bits	Name	Description
0 through 3	Head 1 retry count	The retry count required to complete the most recent thermal compensation on logical head 1 (i.e. head group 1)
4 through 7	Head 0 retry count	The retry count required to complete the most recent thermal compensation on logical head 0 (i.e. head group 0)

Table 12-75. Thermal Compensation Retry Counts (Byte 11_{16})

Bits	Name	Description
0 through 3	Head 3 retry count	The retry count required to complete the most recent thermal compensation on logical head 3 (i.e. head group 3)
4 through 7	Head 2 retry count	The retry count required to complete the most recent thermal compensation on logical head 2 (i.e. head group 2)

Table 12-76. Thermal Compensation Retry Counts (Byte 12_{16})

Bits	Name	Description
0 through 3	Head 5 retry count	The retry count required to complete the most recent thermal compensation on logical head 5 (i.e. head group 5)
4 through 7	Head 4 retry count	The retry count required to complete the most recent thermal compensation on logical head 4 (i.e. head group 4)

Table 12-77. Thermal Compensation Retry Counts (Byte 13_{16})

Bits	Name	Description
0 through 3	Unused	Set to zero
4 through 7	Head 6 retry count	The retry count required to complete the most recent thermal compensation on logical head 6 (i.e. head group 6)

Flaw Location Information

The flaw location information contains the physical head under which the flaw was detected, the location of the flaw in the sector, and a calculated defect parameter for hiding the flaw. For disk array applications, this information is displayed separately for each spindle . Table 12-78 describes each entry of the flaw location information.

Table 12-78. OLHPA Flaw Location Information

Information	Description
Stream n	The ECC circuit relative to the spindle. The stream number range is 0 to 7, representing the 8 ECC circuits used for each spindle.
Head mask	This bit mask indicates the physical head under which a flaw or error occurred. Although the head mask contains up to 9 bits, the number of valid bits is determined by the number of heads within a head group for the device type.
Correction offset	The correction offset represents the position of the corrupted data byte within a sector. The returned offset is only valid for correctable errors, uncorrectable errors result in an offset value of all 1s.
Defect address	The defect address contains the calculated value for a defect parameter in a physical sector. The defect parameter is calculated directly from the correction offset.
Combined head mask	This bit mask indicates all the physical heads under which a flaw or error occurred on a sector.
Flawing defect address	The flawing defect address contains the combined value for a defect parameter when multiple streams are in error.

13 MAINTENANCE PROCEDURES AND FIELD REPLACEABLE UNITS (FRUs)

The following section describes the primary maintenance procedures and lists the field-replaceable units (FRUs) associated with the 300 series disk systems.

Maintenance Procedures

The following subsection describes the primary maintenance procedures associated with the 300 series disk systems. Included are repair and replacement procedures for components of the DE-100 enclosure and the DW-300 drawer assembly.

DD-301 (DCA-2) Drive Removal and Replacement Procedure

Perform the following steps to remove and replace a DD-301 within a DW-300 drawer assembly. The design of the DW-300 makes it possible to remove and replace a spindle without affecting the operation of the other spindles within the cabinet, providing proper procedures are followed.

1. If the drive to be removed failed under system operation, record the I/O path and CRI serial number of the drive. This information can be obtained from online error reports such as errpt or olhpa.

2. Ensure that the drive to be removed has been disabled from the operating system.

CAUTION

Always verify the location and CRI serial number of a spindle before attempting to remove it. Removing an active spindle can result in system interrupts and loss of data. (Up to 1.38 GBytes for a DD–301.)

3. Ensure that the spindle to be removed has been spun down. This can be performed online using the spindown action of the ddms utility. Example: **`ddms -aspindown 0230.1`**

   This example spins down unit 1 connected to cluster 0, EIOP 2, channel 30.

4. Power OFF the replacement spindle by setting the corresponding circuit breaker on the front of the DW-300 to the off (0) position.

CAUTION
Ensure the affected spindle slot on a DW-300 drawer assembly is powered OFF before attempting to remove or replace a DD-301. Failure to do so will result in deterioration of the drive-to-drawer interconnect within the slot.

5. Grasp the cam-action handle located on the front left-hand side of the disk drive and pull the handle forward. This will release the drive from the backplane connection.

	CAUTION
	Observe all ESD precautions. Failure to do so could result in damage to the equipment.

6. Remove the drive from the drawer and place in an ESD safe area.

7. Ensure that the front panel switch settings on the replacement drive are set properly.

8. Repeat steps 4 through 6 in reverse order to install the replacement drive.

NOTE: Because device addresses are set via backplane jumpers, setting the unit address on the replacement drive is not necessary.

DA-301 (DCA-3) Spindle Removal and Replacement Procedure

Perform the following steps to remove and replace a spindle within a DA-301 disk array. The design of the DA-301 components make it possible to remove and replace a failing spindle without affecting the other spindles connected to the system, providing proper procedures are followed.

1. Verify that the spindle to be removed has been logically disabled under the operating system. The `pddconf` command can be used to verify the current state of a DA-301 disk array. It will report the array type, I/O path, and which spindles are currently enabled for reads and writes. Refer to Figure 13-5.

```
#pddconf
          disk devices
name type  unit state mode altp flg  wstrm    rstrm
-------------------------------------------------------
0130 DD301  0    up   rw   0132  1  -------  -------
0132 DD301  1    up   rw   0130  1  -------  -------
0134 DD301  0    up   rw   0136  1  -------  -------
0136 DD301  1    up   rw   0134  1  -------  -------
0234 DA301  0    up   rw   1234  1  0100037  0100037
0236 DA301  0    up   rw   1236  1  0100033  0100033
1234 DA301  1    up   rw   0234  1  0100037  0100037
1236 DA301  1    up   rw   0236  1  0100037  0100037
```

0 - not opened yet
1 - primary path
2 - alt path

Figure 13-5. Example of `pddconf` command output

The wstrm and rstrm fields shown in Figure 13-5 represent the array/stream control bits for disk arrays. The upper most bit indicates that parity reconstruction mode is enabled on the DCA-3. The lowest five bits represent the five spindles of an array, with bits 0-3 representing the data spindles and bit 4 representing the parity spindle. A value of 37_8 indicates that all five spindles are enabled. A value of 33_8 indicates that spindle 2 is disabled on the array. A spindle may be automatically disabled by the UNICOS driver, or manually disabled with a command.

Automatic spindle disable – For disk array applications, UNICOS resiliency software will automatically disable a spindle if catastrophic failures are detected. Catastrophic failures include a spindle's inability to acknowledge a select, reset, or request for status information.

Manual spindle disable – In situations when a spindle causes repeated, non-catastrophic errors, the system administrator can manually disable a spindle using the `pddconf` command.

Example: `pddconf -d 0236.0 disable 2`

This example disables spindle 2 of disk array 0 connected to cluster 0, EIOP 2, channel 36.

2. Locate and verify the spindle to be replaced. Read and record the Cray Research serial number of the disabled spindle. This number can be obtained from the online error reports such as errpt or olhpa.

   When a DD-301 is disabled under UNICOS, the spindle's fault (red) LED is illuminated as part of the disable process. The illuminated LED will aid in locating the spindle for replacement. Locate and verify the affected spindle using the CRI serial number before proceeding to the next step.

pddstat -e

CAUTION
Always verify the location and CRI serial number of a disabled spindle. If the wrong spindle in a disk array is disabled or disconnected, all data residing on the array may be lost. (More than 5.5 GBytes for a DA–301.)

3. A remote spin down command can be sent to the affected spindle using the `ddms` utility. The disabled spindle should be spun down before proceeding to the next step.

   Example: **`ddms –aspindown 0236.0–2`**

   This example spins down spindle 2 of disk array 0 connected to cluster 0, EIOP 2, channel 36.

4. Power OFF the disabled spindle by setting the corresponding power switch on the front of the DW-300 to the off (0) position.

CAUTION

Ensure the affected spindle slot on a DW-300 drawer assembly is powered OFF before attempting to remove or replace a DD-301. Failure to do so will result in deterioration of the drive-to-drawer interconnect within the slot.

5. Remove the failing spindle from the DW-300 drawer and replace it with a working spindle. Refer to the "DD-301 Drive Removal and Replacement Procedure" earlier in this section.

6. Power ON the replacement spindle by setting the corresponding power switch on the front of the DW-300 to the on (1) position.

7. The spindle is now ready to be configured into the operating system.

   For disk arrays, the `ddms` utility can be used to spin up a replacement spindle. The format specification is written to the spindle as a subfunction of the spinup action under `ddms`.

   Example: **`ddms –a spinup 0236.0–2`**
   (allow 1-2 minutes for spinup and synchronization)

   This example will spin up, and write format specs to, spindle 2 of array 0 connected to cluster 0, EIOP 2, channel 36.

8. After the spindle is spun up, use the `surf` option of `ddms` to perform a quick write/read test on the scratch area of the new spindle to verify the performance of the hardware.

   Example: **`ddms –a surf –C 0236.0–2`**

   This example performs surface analysis on the scratch area (–C) on spindle 2 of array 0 connected to cluster 0, EIOP 2, channel 36.

9. Use the `reconstruct` option of `ddms` to initialize and reconstruct data to the new spindle.

   Example: **`ddms -a reconstruct 0236.0`**

   The flaw information is read from the new spindle and the UNICOS spares map is updated. Starting at cylinder 0, all data is read from the disk array in a 4-spindle, parity reconstruction mode and written back in 5-spindle mode. Upon completion, the disk array is reconfigured to 5-spindle mode for subsequent use. If unrecovered errors occur during the reconstruction, a ^C can be entered to abort the process and return the disk array to 4-spindle mode. If no unrecovered errors are encountered, `ddms` will automatically complete the process.

   After the last cylinder has been reconstructed, `ddms` will display a summary of unrecovered errors encountered and ask if the process should be completed. If the errors are numnerous and you enter a negative response, the array is returned to 4-spindle mode. If relatively few errors are encountered and you elect to complete the process, owners of the affected files should be notified.

10. Finally, the `pddconf` command can be used to verify the current state of the affected disk array. If the spindle replacement is successful, all five array/stream control bits will be set in the `wstrm` and `rstrm` fields (37_8) to indicate the disk array has returned to a 5-spindle mode. Refer to Figure 13-6.

What DDMS ~~Unicos~~ does when you execute command

1 reset wstrm bits to 37₈
2) Read user flaw table from new spindle
3) reconstructs data and spares cyl. (scratch area never gets rewritten)
4) resets rstrm to 37₈

```
#pddconf
          disk devices
name type  unit state mode altp flg  wstrm   rstrm
-------------------------------------------------------
0130 DD301  0    up   rw   0132  1  -------  -------
0132 DD301  1    up   rw   0130  1  -------  -------
0134 DD301  0    up   rw   0136  1  -------  -------
0136 DD301  1    up   rw   0134  1  -------  -------
0234 DA301  0    up   rw   0236  1  0100037  0100037
0236 DA301  0    up   rw   0234  1  0100037  0100037
```

Figure 13-6. Example of `pddconf` command output

DE-100 Switching Power Supply Removal and Replacement Procedure

Perform the following steps to remove and replace a switching power supply within a DE-100 disk enclosure. The design of the DE-100 makes it possible to remove and replace a failing power supply without affecting the operation of spindles within the cabinet, providing proper procedures are followed.

The power supplies within the DE-100 use an n+1 design. This allows the drives within the cabinet to function normally through the failure, and replacement, of a single switching power supply. This is sometimes referred to as a "hot swap" capability. For this reason, the cabinet and power supplies can remain powered on during this procedure.

1. After locating the faulty power supply, grasp the cam-action handle located at the bottom of the supply with your right hand. Using your thumb, push the end of the handle to the right to release the lock.

2. Pull the cam-action handle towards you to disconnect the supply from the backplane assembly and carefully slide the supply out of the cabinet.

3. Unpack the replacement power supply and carefully slide it into the slot vacated by the faulty supply. The replacement supply should slide in smoothly until there is about 1 inch remaining.

4. Push in on the cam-action handle to lock the replacement power supply into position

5. Read and record the DC voltage on the common output bus by using the WACS display. The output bus should read 36.0 Vdc.

6. Using a DVM, read the DC voltage from the test points located on the front of the newly installed power supply. The test points should indicate 36.7 Vdc. If adjustment is necessary, use the voltage adjustment trim pot located on the front of the supply.

NOTE: The DC voltage level on the common output bus is determined by the switching power supply with the lowest voltage setting. For load balancing between the power supplies, each individual supply should be adjusted to read 36.7 Vdc on it's front panel test points. The voltage drop across the rectifier diodes in each supply (.7v) will result in a 36.0 Vdc level on the common output bus.

WACS Module Removal and Replacement Procedure

Use the following procedure to remove and replace any of the following:

- The WACS Display Module
- The WACS Warning Module
- The WACS Control Module

NOTE: The WACS Display and Warning modules can be removed and replaced without interrupting the disk drives within the DE-100 cabinet. During the time either of these modules is removed, the WACS will be unable to support remote powerup or powerdown actions.

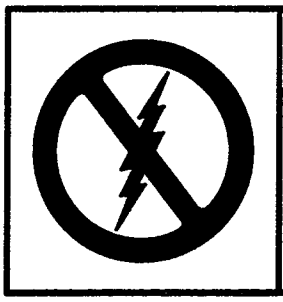
CAUTION

The WACS Control module cannot be removed without causing an immediate powerdown of the DE-100 cabinet. Repair of this module should be limited to preventative or emergency maintenance periods (EM or PM).

1. Using a Philips screwdriver, remove the four bolts securing the top cover of the DE-100 cabinet. These bolts are located in each corner of the top cover and are accessed from the inside of the cabinet.

2. Place a small ladder or step-stool aside the DE-100 to allow access to the top of the cabinet. Remove the top cover and set it aside.

3. Remove the 8 screws (2 per side) securing the top cover of the WACS tray. Remove the tray cover and set it aside.



CAUTION

Observe all ESD precautions. Failure to do so could result in damage to the equipment.

4. Locate the failing WACS module within the tray assembly (refer to Figure 13-7).

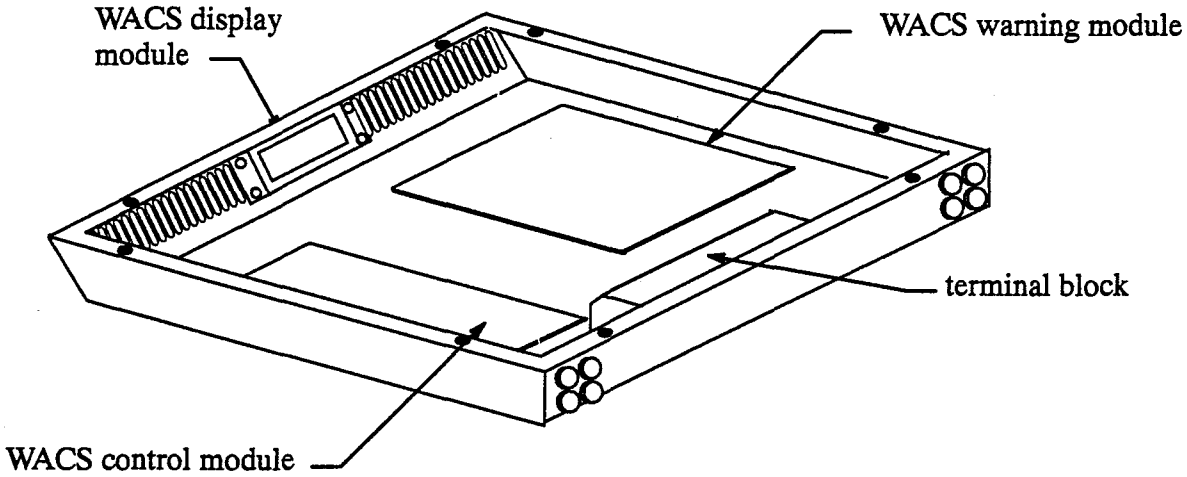


Figure 13-7. WACS Module Locations (top view)

5. Carefully remove and mark all connectors from the WACS module to be removed.

WARNING

240 Vac is present on the terminal block (TB1) of the WACS Control module. Before removing the WACS Control module, ensure cabinet power has been disabled using CB1 on the DE-100 Power Input Box.

6. Carefully remove the screws securing the WACS module to the tray assembly. Retain these screws for installation of the replacement module.

7. Remove the failing module and place in an ESD-safe bag or container.

8. Repeat the above steps in reverse order to install the replacement module.

DW-300 Front Panel Circuit Breaker Removal and Replacement

Use the following procedure to remove and replace a defective front panel circuit breaker on a DW-300 drawer.

1. Open the back door of the DE-100 cabinet and locate the circuit breaker box in the bottom right corner. Turn OFF the circuit breaker for the drawer to be serviced.

WARNING

Ensure that the DC power has been removed from the DW-300 before attempting service. Failure to do so can result in injury or death.

2. On the front of the DW-300 drawer, remove the 4 Philips screws securing the circuit breaker panel to the front of the drawer.

3. Carefully extend the front panel about 4 inches to expose the Power Distribution board behind the panel (refer to Figure 13-8).

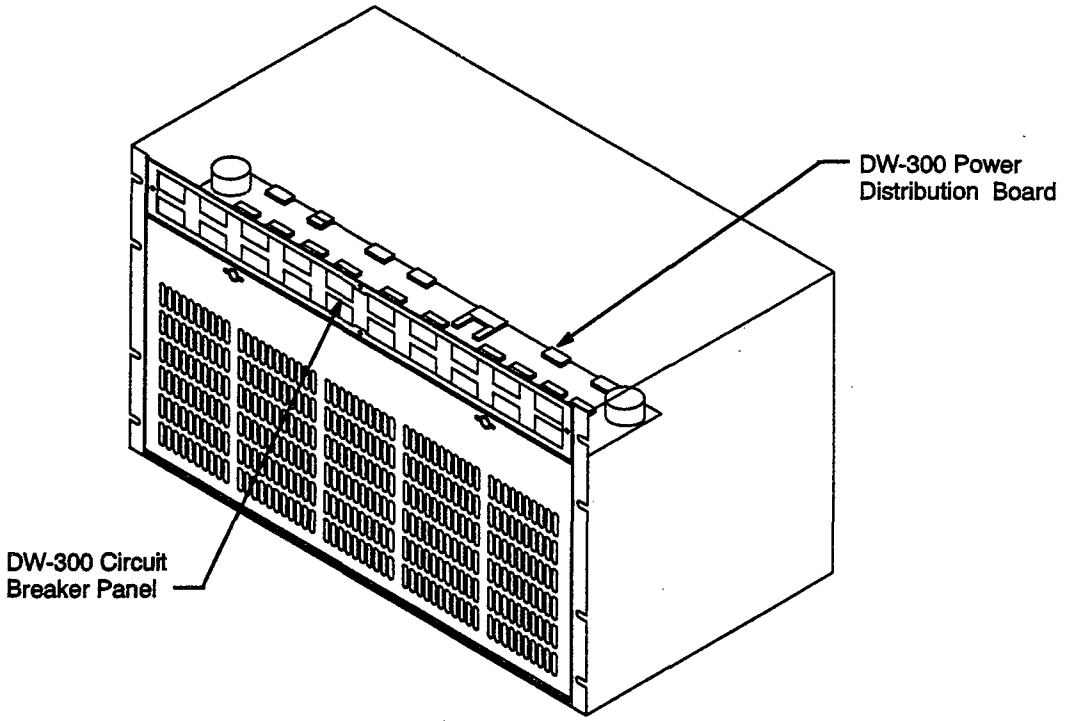


Figure 13-8. DW-300 Drawer Assembly

4. Locate and remove the connector attaching the defective circuit breaker to the Power Distribution board.

NOTE: The circuit breakers located in the bottom row (row 1) of the front panel are connected to the rear connectors on the Power Distribution board. The circuit breakers located in the top row (row 2) of the front panel are connected to the front connectors on the Power Distribution board.

5. Squeeze the sides of the defective circuit breaker while pushing forward to remove the breaker from the front panel.

6. Reverse the previous steps to install the replacement circuit breaker.

DW-300 Power Distribution Board Removal and Replacement

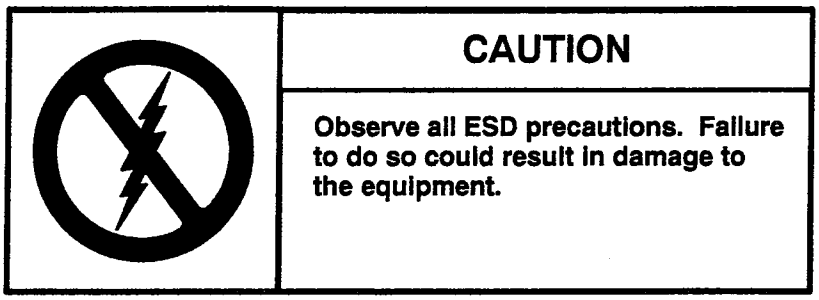
Use the following procedure to remove and replace a defective Power Distribution board in a DW-300 drawer. If the DE-100 WACS indicates a defective thermistor, replacement of this board will be necessary to correct the problem. This procedure can be performed without affecting other drawers within the DE-100 cabinet, but requires a powerdown of the affected DW-300 drawer.

1. Ensure that all drives within the drawer to be serviced are spundown and inaccessible to the operating system.

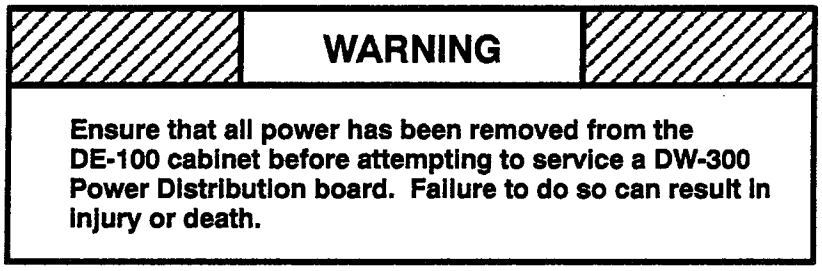
2. Remove power from all spindles within the drawer by setting all circuit breakers on the front of the DW-300 to the OFF (0) position.

CAUTION
Ensure that all spindles in the DW-300 drawer are spundown and powered OFF before attempting to remove them. Failure to do so can result in damage to the spindles.

3. Observing all ESD precautions, remove all spindles from the top row (row 2) of the DW-300 drawer to be serviced and set them aside. Note the exact position of each spindle in the drawer to ensure proper re-installation at the completion of this procedure.



4. Open the rear door of the DE-100 cabinet and locate the drawer circuit breaker bax in the lower right-hand corner. Turn OFF the circuit breaker for the drawer to be serviced. Drawer #1 is the bottom drawer while drawer #4 is at the top.



5. On the front of the DW-300 drawer, remove the 4 Philips screws securing the circuit breaker panel to the front of the drawer.

6. Carefully extend the front panel about 4 inches to expose the Power Distribution board behind the panel (refer again to Figure 13-8).

7. Carefully remove all 20 circuit breaker connectors from the top of the Power Distribution board.

8. Remove the front panel (circuit breakers attached) and set aside

9. Locate the center cooling fan at the rear of the DW-300 drawer being serviced. Remove the AC and sense wire connections from the rear of the cooling fan. Remove the 4 corner screws securing the fan to the back of the drawer chassis and set the fan aside.

10. Reach inside the fan opening and remove the 6 connectors (J21 - 27) attached to the back of the Power Distribution board. Refer to Figure 13-9 for the location of these connections.

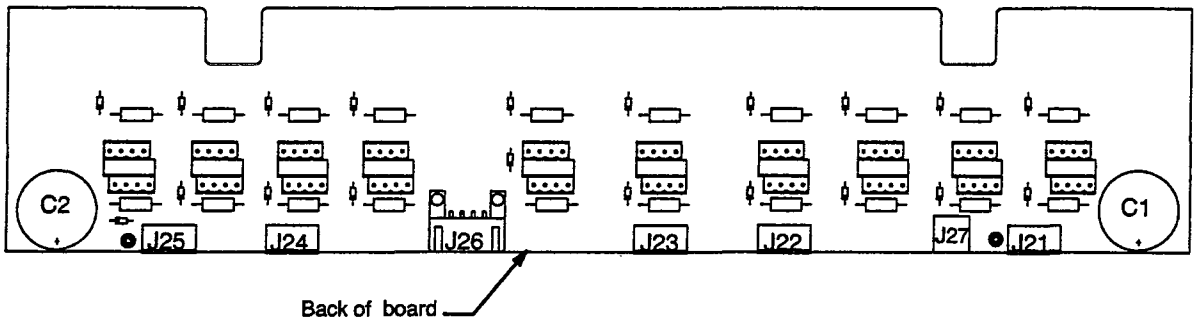


Figure 13-9. DW-300 Power Distribution Board (top view)

11. Using a short screwdriver, reach inside the front of the drawer (top row) and remove the 10 screws securing the Power Distribution board to the chassis. There are 5 screws across both the front and the rear of the Power Distribution board. Set these screws aside for installation of the replacement board.

12. Carefully lift and remove the defective Power Distribution board through the front panel.

13. Remove the mounting standoffs from the defective board and install them onto the replacement board.

14. Reverse the previous steps to install the replacement board.

DW-300 Drawer Removal and Replacement Procedure

This procedure is pending completion of the wire harness and connections to the DW-300 drawer assembly.

Field Replaceable Units (FRUs)

The following subsection describes the field replaceable units (FRUs) associated with the 300 Series disk drive subsystems. This list is subject to change; all part numbers should be confirmed with Logistics at the time of order.

Table 13-1. 300 Series Disk System FRUs

FRU	CRI part number
DD-301 Disk Drive, 3.5"	12291900
DE-100 36Vdc 3000W Switching Power Supply	01819100
DE-100 Power Supply Rack Assembly	01819000
Input Power Cable Assembly **208V** 20A Delta	01819200
Input Power Cable Assembly **400V** 20A Wye	01819300
Fan, Tubeaxial w/alarm	01787001
DW-300 Backplane Module PCB Assy	31434000
DW-300 Power Distribution PCB Assy	31461000
Circuit Breaker, 5A SPST (DW-300 front panel)	01790200
Circuit Breaker, 30A (Power Input Box)	01819601
WACS Display module (DE-100)	31445000
WACS Control module (DE-100)	31446000
WACS Warning module (DE100)	31447000