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Each time this manual is fully revised and reprinted, all change packets to the previous version are incorporated into the new version, and the new version is assigned an alphabetical revision level, which is indicated in the publication number on each page of the manual. A revised manual does not usually contain change bars.

REVISION	DESCRIPTION
	July 1991. Original Printing.
A	November 1992. The manual was reorganized with information on the DD-62, RD-62, and RDE-6 added. Miscellaneous editorial and technical changes were made.
B	February 1993. Information about the disk array product and DCA-3 channel adapter was added. Miscellaneous editorial and technical changes were made.

PREFACE

The *60 Series Disk Systems Guide* is designed as a reference manual for Cray Research, Inc. (CRI) field engineers who have had I/O subsystem model E (IOS-E) and 60 series disk systems training. This manual incorporates diagnostic and hardware information relative to disk drive operations.

The following conventions are used throughout this manual:

- `Courier` font indicates directory pathnames, filenames, commands, utilities, and screen output.

- **`Courier bold`** font indicates commands and options that the user should enter.

- *Italic* font indicates a variable or user-supplied entry.

- Commands must be entered as shown in the command syntax. Spaces must be included or left out as shown; do not use tabs.

- The ↵ symbol indicates pressing the return key.

- Control signals for the IPI-2 interface are in capital letters. For example, BUS CONTROL.

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TABLES

SECTION 1
DISK SYSTEM OVERVIEW

1   DISK SYSTEM OVERVIEW

A disk system consists of DD-60, DD-61, and/or DD-62 spindles, a
DE-60 disk enclosure, and spare spindle(s). The system connects to an
I/O subsystem model E (IOS-E) through a disk channel adapter, either a
DCA-2 (for DD-60, DD-61, or DD-62) or a DCA-3 (for the DA-60 or
DA-62 disk array).

Figure 1-1 is a block diagram of a 60 series disk system connected to a
DCA-2. The DE-60 contains ten disk drives. Three DD-62s (one is a
spare DD-62) are connected to one DCA-2, and seven DD-60s (one is a
spare DD-60) are connected to another DCA-2.
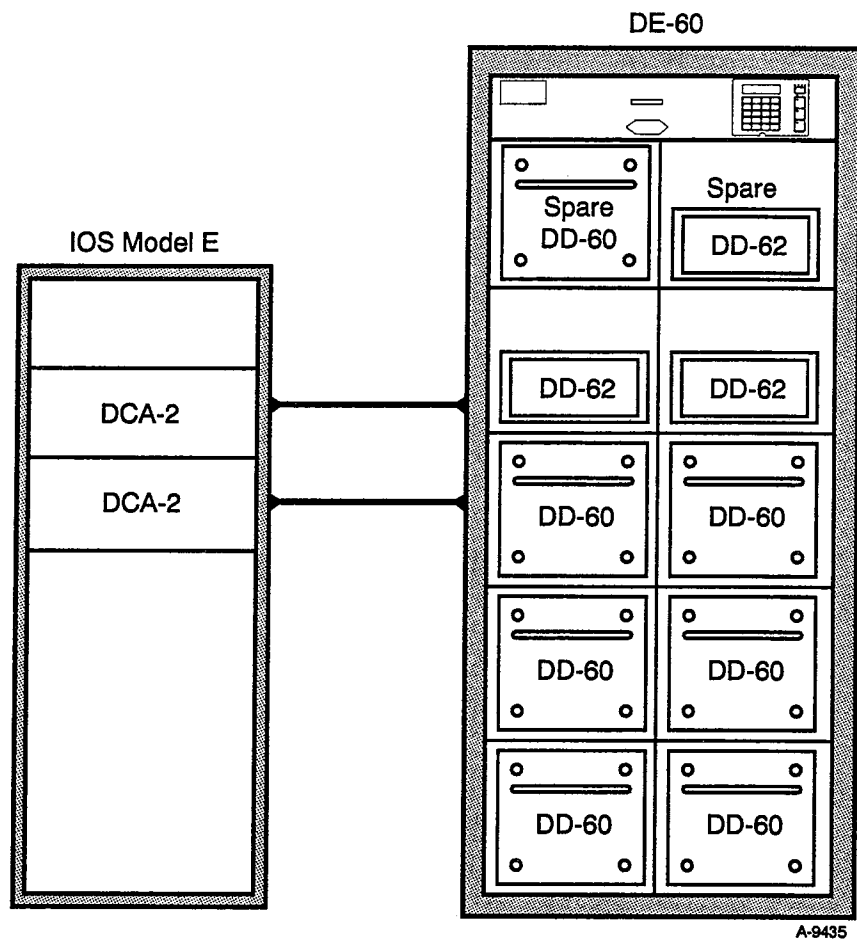
Figure 1-1. Typical 60 Series Disk System Connected to an IOS-E

Disk Drives

DD-60, DD-61, and DD-62 disk drives provide long-term data storage for a Cray Research, Inc. (CRI) computer system. The DD-60 provides a fast data-transfer rate and the DD-61 and DD-62 provide increased data-storage capacity. The RD-62 provides the same performance capabilities as the DD-62; however, the RD-62 can be removed from the removable disk enclosure (RDE-6) cabinet.

DD-60 Disk Drive

The DD-60 is a parallel-head storage unit. Its sustained transfer rate ranges from 16 to 20 Mbytes/s, and it has a storage capacity of 1.96 Gbytes.

One DD-60 contains two groups of nine parallel read/write heads and one servo head. During data transfers to and from the DCA-2, only one group of heads (0 or 1) is used at a time. Eight of the heads transfer data, while the ninth head transfers a parity bit (the parity head is unused when the disk system is connected to a DCA-3). The servo head transfers head position information to the control circuitry in the DD-60.

A sector of data from a DD-60 contains 2,048 64-bit words of system data. The DCA-2 creates the sector from eight physical sectors in the DD-60 (one from each head). Each physical sector contains 256 64-bit words of data.

A logical track is made from eight physical tracks of data in the DD-60. One track contains 23 sectors where data can be stored and retrieved by the operating system.

Two tracks make up one cylinder. The DD-60 has 2,608 data cylinders, 2 maintenance cylinders, and 1 flaw table cylinder.

DD-61 Disk Drive

The DD-61 is a serial-head storage unit. It has a sustained transfer rate of 2.6 Mbytes/s and a storage capacity of 2.23 Gbytes.

One DD-61 contains 19 serial read/write heads and one servo head. During data transfers to and from the DCA-2, only one head (0 through 22_8) is used at a time. The servo head transfers head position information to the control circuitry in the DD-61. DD-61s are not supported by the DCA-3 as a disk array.

A sector of data from a DD-61 contains 512 64-bit words of IOP data. Data is transferred between the DD-61 and DCA-2 in blocks of this fixed size. One track contains 11 sectors where data can be stored and retrieved by the IOS-E.

Nineteen tracks make up one cylinder in the DD-61. DD-61s contain 2,608 data cylinders, 2 maintenance cylinders, and 1 flaw table cylinder.

DD-62 Disk Drive

The DD-62 is a two-head parallel storage unit. It has a sustained transfer rate of 8.14 Mbytes/s and a storage capacity of 2.73 Gbytes.

One DD-62 contains nine read/write head groups and one servo head. During data transfers to and from the DCA-2, two heads are used at a time. The servo head transfers head position information to the servo control circuitry in the DD-62.

A sector of data from a DD-62 contains 512 64-bit words of IOP data. Data is transferred between the DD-62 and DCA-2 in blocks of this fixed size. Each track contains 28 sectors where data can be stored and retrieved by the IOS-E.

The DCA-2 creates a sector from two physical sectors in the DD-62 (one from each head in the head group). Each physical sector contains one half of an IOP data sector.

Nine logical tracks make up one cylinder in the DD-62. DD-62s contain 2,652 data cylinders, 2 maintenance cylinders, and 1 flaw table cylinder.

RD-62 Disk Drive

The RD-62 is a two-head parallel storage unit that is identical to the DD-62 in performance. It has a sustained transfer rate of 8.14 Mbytes/s and a storage capacity of 2.73 Gbytes.

The RD-62 is housed in an RDE-6 enclosure that enables individual drives to be easily removed and replaced by the customer. The RDE-6 enclosure contains up to four RD-62s. Connections to the RD-62s are made through a bulkhead on the RDE-6 cabinet. Because of the limitations of the RDE-6 bulkhead, RD-62s do not support daisy chain or alternate-path cabling configurations like the DD-62s. In all other respects, the RD-62 is equivalent to the DD-62.

DD-60, DD-61, DD-62, and RD-62 Comparison

DD-60s and DD-61s are Sabre VI disk drives; DD-62s and RD-62s are Sabre VII disk drives. All drives are formatted to CRI specifications. Table 1-1 lists the characteristics of the DD-60, DD-61, DD-62, and RD-62.

Table 1-1. DD-60, DD-61, DD-62, and RD-62 Characteristics

Characteristic	DD-60	DD-61	DD-62 and RD-62
Spindle type	Sabre VI 9 head parallel	Sabre VI 19 head serial	Sabre VII 2 head parallel
Sustained transfer rate	16 – 20 Mbytes/s	2.3 – 2.6 Mbytes/s	8.14 Mbytes/s
Burst transfer rate	24 Mbytes/s	3.0 Mbytes/s	9.34 Mbytes/s
Storage capacity (formatted)	1.96 Gbytes	2.23 Gbytes	2.73 Gbytes
Heads per drive	16 data 2 parity 1 servo	19 data 1 servo	18 data 1 servo
Heads active at one time	8 data 1 parity	1 data	2 data
Cylinders per drive	0 – 2,610 (0 – 5062$_8$)	0 – 2,610 (0 – 5062$_8$)	0 – 2,654 (0 – 5136$_8$)
Head groups	0 – 1 (0 – 1$_8$)	0 – 18 (0 – 22$_8$)	0 – 8 (0 – 10$_8$)
Sectors per logical track	0 – 22 (0 – 26$_8$)	0 – 10 (0 – 12$_8$)	0 – 27 (0 – 33$_8$)
Logical sector size in 64-bit words	2,048 CRI words	512 CRI words	512 CRI words
Flaw table cylinder	2,610 (5062$_8$)	2,610 (5062$_8$)	2,654 (5136$_8$)
Maintenance (CE) cylinder	2,608 (5060$_8$)	2,608 (5060$_8$)	2,652 (5134$_8$)
Average single track seek time	3 ms	3 ms	3 ms
Average seek time	13 ms	13 ms	12 ms
Full track seek time	26 ms	26 ms	26 ms
Average latency	8.3 ms	8.3 ms	6.87 ms
Rotational speed (nominal)	3,600 rpm	3,600 rpm	4,365 rpm
Start time (without sequence delay)	1 min, 30 s	1 min, 30 s	1 min, 30 s
Stop time (maximum)	60 s	60 s	60 s
Single disk drive weight (including power supply)	55 lbs 25 kg	41 lbs 18.6 kg	40 lbs 18.1 kg
Actuator type	Balanced rotary	Balanced rotary	Balanced rotary
Data coding to/from media	Nonreturn to zero (NRZ) / 2 – 7 run length limited (RLL)	Nonreturn to zero (NRZ) / 2 – 7 run length limited (RLL)	Nonreturn to zero (NRZ) / 1 – 7 run length limited (RLL)
Type of interface	Intelligent peripheral interface-2 (IPI-2)	Intelligent peripheral interface-2 (IPI-2)	Intelligent peripheral interface-2 (IPI-2)

DE-60 Disk Enclosure

The DE-60 disk enclosure houses combinations of one to ten DD-60, DD-61, and DD-62 disk drives. For example, Figure 1-2 shows a DE-60 with six DD-60s, two DD-62s, one spare DD-62, and one spare DD-60. In addition to the disk drives, the DE-60 contains a terminal block, cooling fan(s), and a maintenance panel.
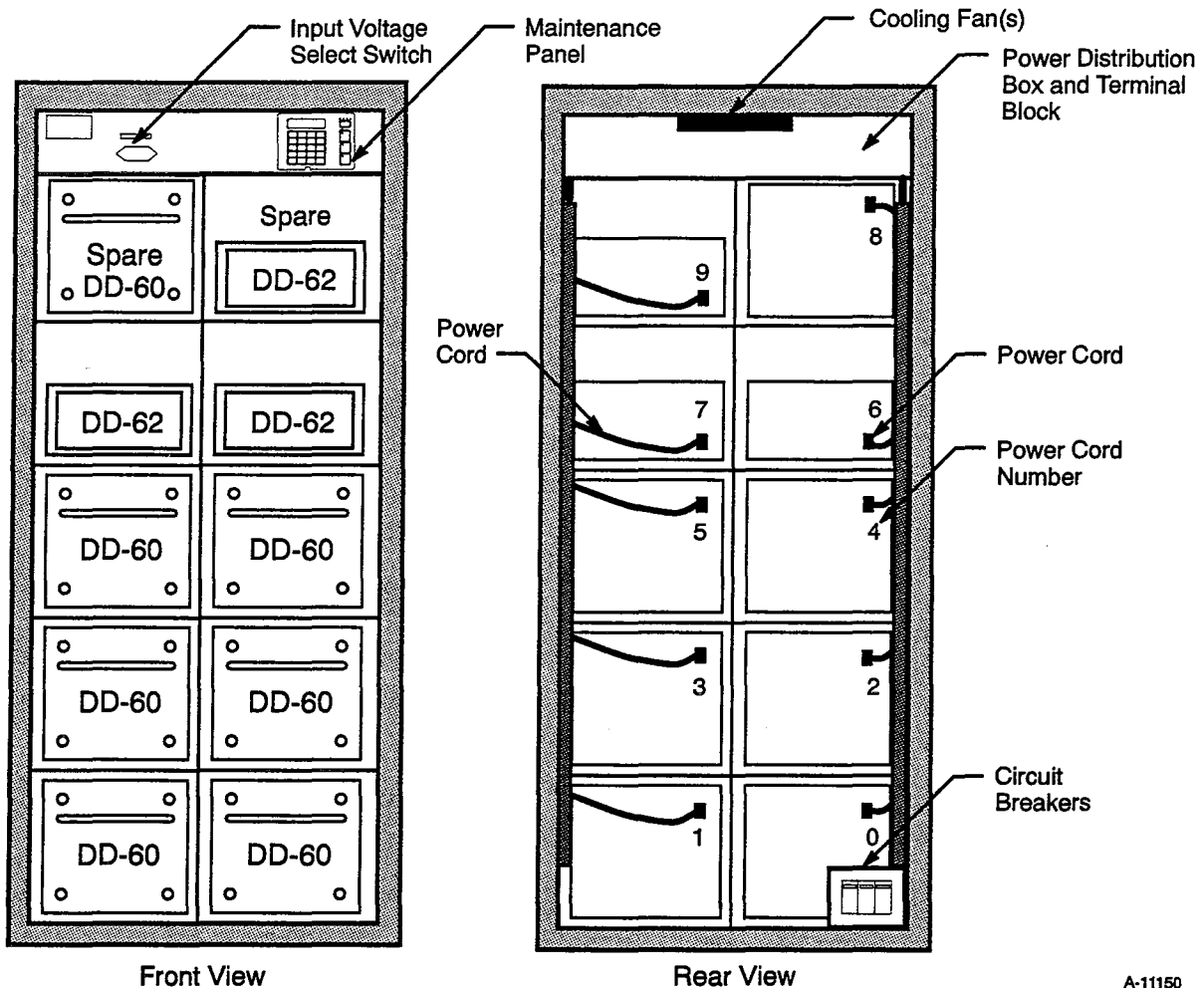
Figure 1-2. Front and Rear Views of the DE-60

The terminal block and voltage switch connect each drive to one of the three-phase loads. A delta output is configured for a 400-Vac input, and a wye output is used for 208-Vac input power. Power cords connect the terminal block to each disk drive and are cut to length for each position in the cabinet. The power cords are numbered as shown in Figure 1-2.

The cooling fan(s) transfer exhaust air from the disk drives to the computer room. The exhaust air exits the rear of the disk drives, moves through the cooling fans, and leaves the DE-60 through a vent in the top of the cabinet.

The maintenance panel is used to run disk drive diagnostics. Refer to the "Maintenance Procedures" section of this manual for more information on the maintenance panel.

The characteristics of a fully loaded DE-60 vary depending on the number of DD-60s, DD-61s, or DD-62s it contains. Table 1-2 compares physical characteristics of a DE-60 with ten DD-60s, DD-61s, or DD-62s installed.

Table 1-2. Characteristics of a Fully Loaded DE-60

Characteristic	Ten DD-60s	Ten DD-61s	Ten DD-62s
Height	61.75 in. (157 cm)	61.75 in. (157 cm)	61.75 in. (157 cm)
Width	24.00 in. (61 cm)	24.00 in. (61 cm)	24.00 in. (61 cm)
Depth	41.50 in. (105 cm)	41.50 in. (105 cm)	41.5 in. (105 cm)
Floor space	6.9 ft^2 (0.6 m^2)	6.9 ft^2 (0.6 m^2)	6.9 ft^2 (0.6 m^2)
Weight	960 lbs (435 kg)	812 lbs (368 kg)	810 lbs (367 kg)
Heat load (8 disk drives)	8,600 Btu/hr (2,520 W)	4,770 Btu/hr (1,400 W)	5,700 Btu/hr (1,670 W)
Cooling	Air-cooled	Air-cooled	Air-cooled
Minimum side clearance	2.00 in. (5 cm)	2.00 in. (5 cm)	2.00 in. (5 cm)
Minimum front clearance	36.00 in. (91 cm)	36.00 in. (91 cm)	36.00 in. (91 cm)
Minimum back clearance	30.00 in. (76 cm)	30.00 in. (76 cm)	30.00 in. (76 cm)
Power cable	6.0 ft (1.8 m)	6.00 ft (1.8 m)	6.00 ft (1.8m)
Maximum data cable length (standard)	65.6 ft (20 m)	65.6 ft (20 m)	65.6 ft (20 m)
Maximum data cable length (optional)	98.4 ft (30 m)	98.4 ft (30 m)	98.4 ft (30 m)
Input Power (selectable) refer to "Input Voltage Select Switch" in Figure 1-2	200-208 Vac, 3 phase, 50/60 Hz, 12 A/phase or 380-416 Vac, 3 phase, 50/60 Hz, 7 A/phase	200-208 Vac, 3 phase, 50/60 Hz, 6.4 A/phase or 380-416 Vac, 3 phase, 50/60 Hz, 3.7 A/phase	200-208 Vac, 3 phase, 50/60 Hz, 6 A/phase or 380-416 Vac, 3 phase, 50/60 Hz, 3 A/phase

Cray Research Proprietary

RDE-6 Disk Enclosure

The RDE-6 disk enclosure is designed to house RD-62 disk drives. The RD-62 disk drive is a removable version of the DD-62 disk drive and is used by customers who require removable disk drives on their site.

Up to four RD-62 disk drives can be housed in one RDE-6 disk drive cabinet (refer to Figure 1-3). The RDE-6 cabinet does not support the daisy chain configuration of RD-62 disk drives.

RDE-6 Front View

A-11100
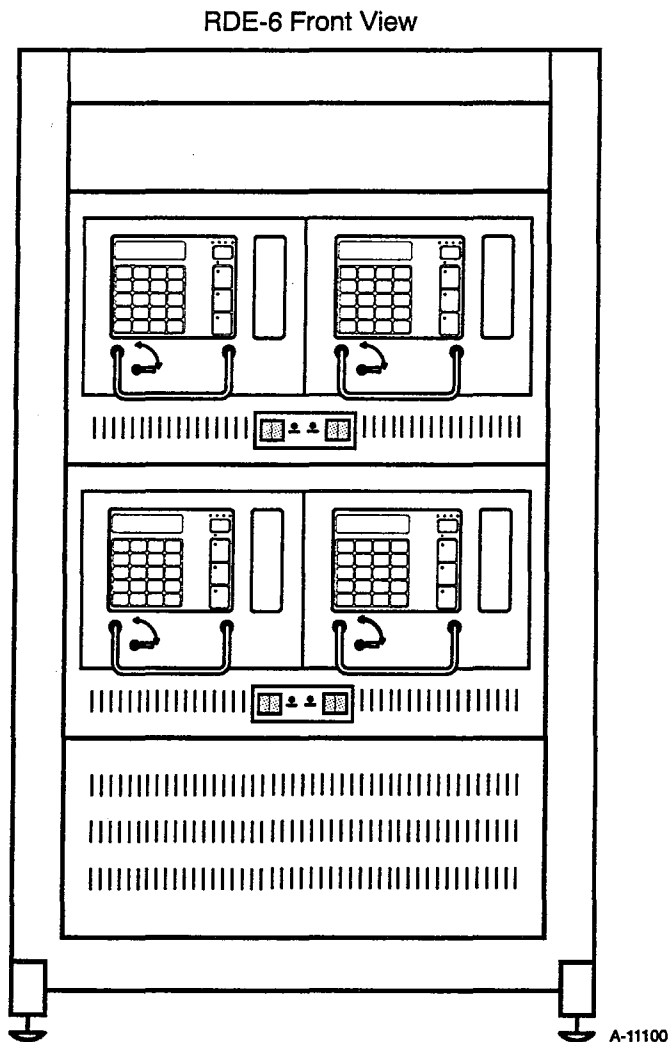
Figure 1-3. RDE-6 with RD-62 Removable Disk Drives

The RD-62 disk drives connect to DCA-2 disk channel adapters, which provide an IPI-2 interface. A separate DCA-2 is required for each RD-62 drive.

Each RD-62 has a maintenance panel that is used to run disk drive diagnostics. Refer to the "Maintenance Procedures" section of this manual for more information on the maintenance panel.

The characteristics of a fully loaded RDE-6 vary depending on the number of RD-62s it contains. Table 1-3 details the physical characteristics of an RDE-6 with four RD-62s installed.

Table 1-3. Characteristics of a Fully Loaded RDE-6

Characteristic	Four RD-62s
Height	42.00 in. (107 cm)
Width	23.00 in. (58 cm)
Depth	36.00 in. (91 cm)
Floor space	5.8 ft^2 (0.5 m^2)
Weight (4 RD-62s)	384 lbs (174 kg)
Maximum heat load	2,543 Btu/hr (745 W)
Cooling	Air-cooled
Side clearance	1.00 in (2.54 cm)
Front clearance	24.00 in. (61 cm)
Back clearance	24.00 in. (61 cm)
Power cable	6-ft (1.8-m) pluggable drop cord
Data cable length (standard)	65.6 ft (20 m)
Data cable length (optional)	98.4 ft (30 m)
Power	208 – 240 Vac, 1 phase, 50/60 Hz, 6 A

Spare Disk Drive

One or more spare DD-60, DD-61, and/or DD-62 disk drives may be cabled into a disk system and configured as a spare device. (RD-62 disk drives are not typically configured with spares.) If a disk drive is failing, the data from the failing drive can be moved to the spare using UNICOS utilities. The spare disk drive can store the data until the failing drive is repaired or replaced.

Only one spare DD-60, DD-61, and/or DD-62 is needed per site, rather than per DE-60. For each drive type, at least one available position on a DCA-2 should be reserved to accommodate connection to a spare device.

DCA-2 Disk Channel Adapter

The DCA-2 provides a communication link between the auxiliary input/output processor (EIOP) in the IOS-E and the DD-60, DD-61, DD-62, and/or RD-62 disk drives (refer to Figure 1-4). The DCA-2 transfers system data from the EIOP buffer board to the disk drive. The DCA-2 also converts control functions from the EIOP into IPI-2 protocol for the disk drives.

The primary functions of the DCA-2 include:

- Communicating with up to eight disk drives
- Passing control functions from the EIOP to the disk drives
- Receiving status from the disk drives
- Generating error-correction codes for write data
- Checking read data error-correction codes and parity

There are several restrictions to the configuration options that are possible with the DCA-2 and the DD-60, DD-61, DD-62, and RD-62 disk drives. These configuration options include the following restrictions:

- Even though the DCA-2 channel adapter supports DD-60, DD-61, DD-62, and RD-62 drives, all drives connected to a single DCA-2 must be of the same type.

- Even though each EIOP supports up to four channel adapters, all channel adapters connected to a single EIOP must be of the same type.
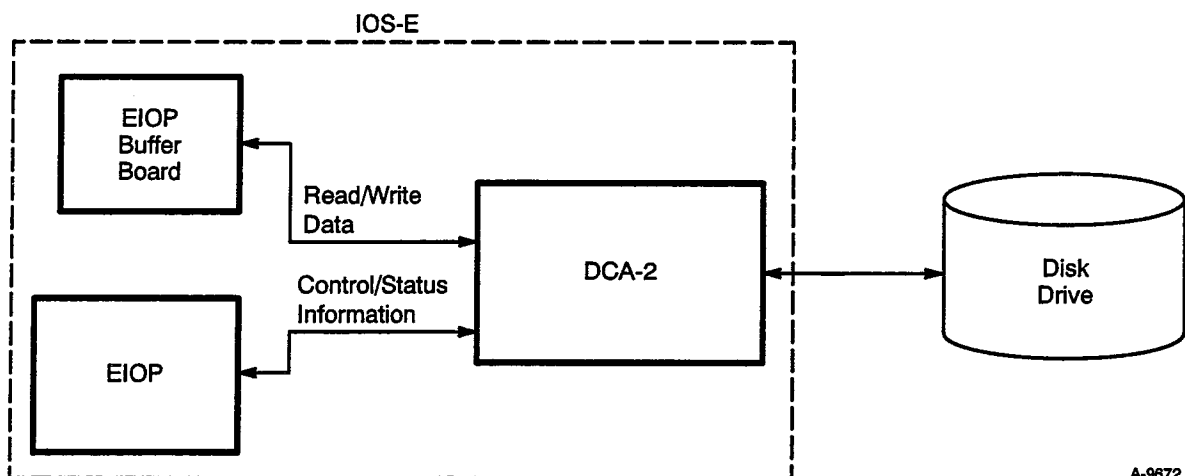
Figure 1-4. Block Diagram of DCA-2 Operations

DCA-3 Disk Channel Adapter

The DCA-3 provides a communication link between the auxiliary input/output processor (EIOP) in the IOS-E and the DA-60 or DA-62 disk arrays (refer to Figure 1-5). The DCA-3 transfers data from the EIOP buffer board to the disk array. The DCA-3 also converts control functions from the EIOP into IPI-2 protocol for the array spindles.

The primary functions of the DCA-3 include:

- Communicating with up to eight disk arrays
- Communicating to each array in 1-, 4-, or 5-spindle mode
- Passing control functions from the EIOP to the disk arrays
- Receiving status from the disk arrays
- Generating error-correction codes for write data
- Checking read data error-correction codes and parity
- Striping write data and parity across the 5-spindle array
- Performing parity reconstruction on read data

A-11355
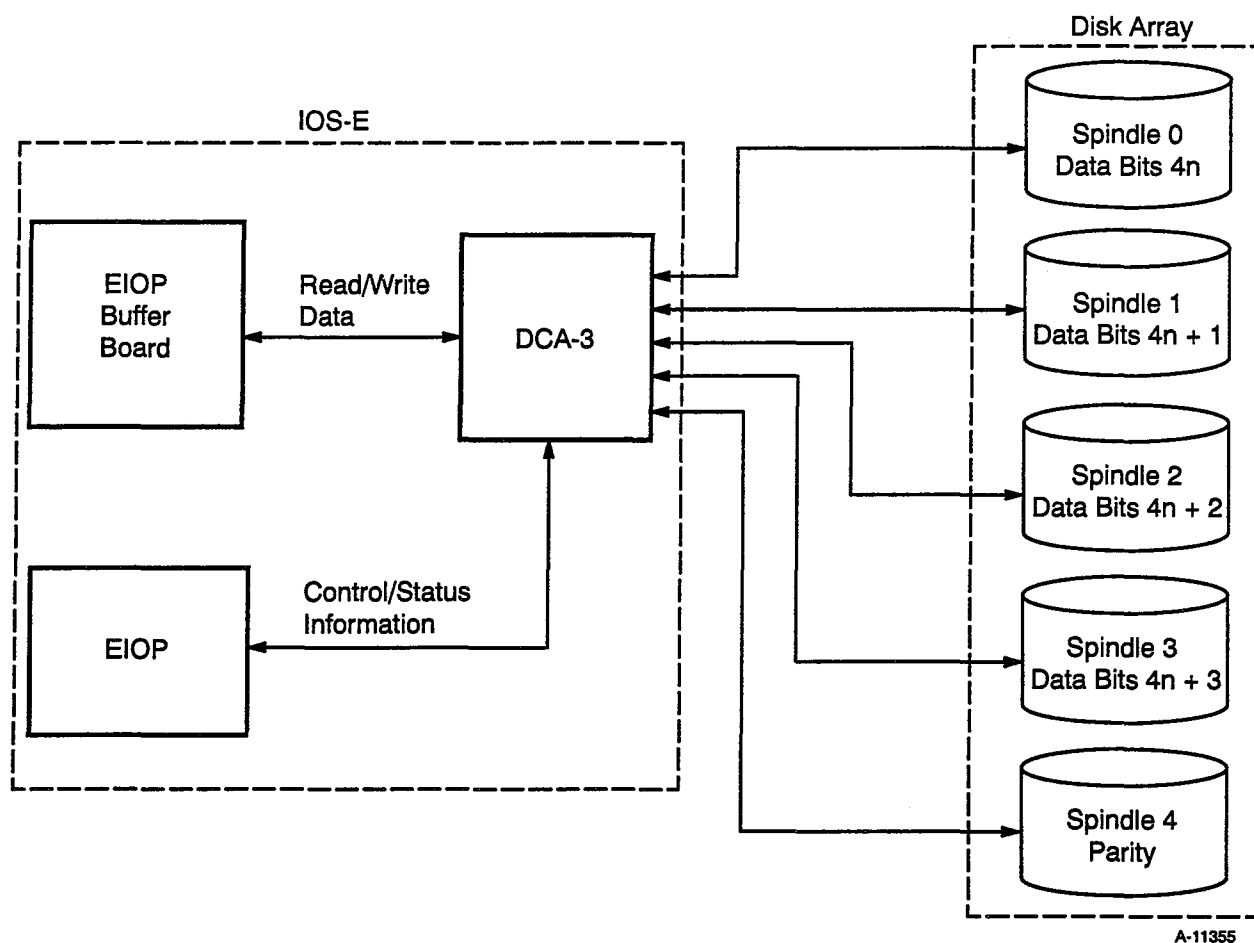
Figure 1-5. Block Diagram of DCA-3 Operations

DCA-2 and DCA-3 Comparison

A DCA-3 can connect to a DA-60 or a DA-62 disk array. The DA-60 comprises five DD-60 spindles; the DA-62 comprises five DD-62 spindles. In each array type, data is striped across four of the spindles while the fifth spindle is used for odd parity.

Use of the terms drive and spindle can be confusing. Whether a device should be referred to as a drive or a spindle is largely determined by the type of channel adapter to which it is connected. If a DD-60 is connected to a DCA-2 channel adapter, it is an individually accessible I/O device and should be referred to as a drive. However, a DD-60 connected to a DCA-3 represents one-fifth of an array and should be referred to as a spindle.

The hardware design and software support of the DCA-3 enable the disk array to sustain full performance and data integrity through a wide variety of problems, up to and including the complete failure of a spindle. Alternate path configurations and cabling options can even provide resiliency against the failure of a DCA-3 or DE-60 disk enclosure. Refer to the "DCA-3 to Disk Array Cabling" section later in this manual.

The spindles used for the disk array are housed in the DE-60 cabinet. Because each cabinet can house up to ten spindles, a single DE-60 can accommodate two complete arrays. The inclusion of an extra spindle as a hot spare device becomes unnecessary due to the resilient nature of the disk array. The number of spindles per cabinet can vary depending on the number and configuration of arrays involved. Cabling configuration details for the disk array are located in the "DCA-3 to Disk Array Cabling" section later in this manual.

The format specification for an individual DD-60 or DD-62 spindle does not change if the spindle is connected to the DCA-3. However, when connected to the DCA-3, each spindle is regarded as one-fifth of the logical device. Data buffering on the DCA-3 allows hideable flaws to be handled on a per-spindle basis. Specific format information is in the "DD-60 and DD-62 Format and Flaw Management" sections later in this manual.

A DD-60 spindle connected to a DCA-2 operates as a 9-head parallel device. When connected to a DCA-3, the DD-60 operates in 8-head parallel mode with the parity head disabled. The hardware switch settings for DD-60 and DD-62 spindles connected to a DCA-2 must be changed for connection to the DCA-3. Details on the switch settings are located in the DD-60 and DD-62 "Hardware Description" sections later in this manual.

Status definitions also differ between the DCA-2 and DCA-3 channel adapters. Refer to the "DCA-3 Systems Status" section in this manual for information specific to the DCA-3.

Disk array performance is basically four times that of the same spindle type connected to a DCA-2. Refer to Table 1-1 for a comparison of the DD-60 and DD-62 drives. Refer to Table 1-4 for a comparison of the DA-60 and DA-62 disk arrays.

Table 1-4. DA-60 and DA-62 Characteristics

Characteristic	DA-60	DA-62
Spindle type	(5) Sabre VI 8 head parallel	(5) Sabre VII 2 head parallel
Sustained transfer rate	Up to 80 Mbytes/s	up to 32.5 Mbytes/s
Storage capacity (formatted)	7.84 Gbytes	10.92 Gbytes
Heads active at one time	32 data 8 parity	8 data 2 parity
Cylinders per array	$0 - 2{,}610$ $(0 - 5062_8)$	$0 - 2{,}654$ $(0 - 5136_8)$
Head groups	$0 - 1$ $(0 - 1_8)$	$0 - 8$ $(0 - 10_8)$
Sectors per logical track	$0 - 22$ $(0 - 26_8)$	$0 - 27$ $(0 - 33_8)$
Logical sector size in 64-bit words	8,192 CRI words	2,048 CRI words
Flaw table cylinder	$2{,}610$ (5062_8)	$2{,}654$ (5136_8)
Maintenance (CE) cylinder	$2{,}608$ (5060_8)	$2{,}652$ (5134_8)
Average single track seek time	3 ms	3 ms
Average seek time	13 ms	12 ms
Full track seek time	26 ms	26 ms
Average latency	8.3 ms	6.87 ms
Rotational speed (nominal)	3,600 rpm	4,365 rpm
Start time (without sequence delay)	1 min, 30 s	1 min, 30 s
Stop time (maximum)	60 s	60 s
Actuator type	Balanced rotary	Balanced rotary
Data coding to/from media	Nonreturn to zero (NRZ) / 2 – 7 run length limited (RLL)	Nonreturn to zero (NRZ) / 1 – 7 run length limited (RLL)
Type of interface	Intelligent peripheral interface-2 (IPI-2)	Intelligent peripheral interface-2 (IPI-2)

SECTION 2
DCA-2 TO DISK DRIVE CABLING
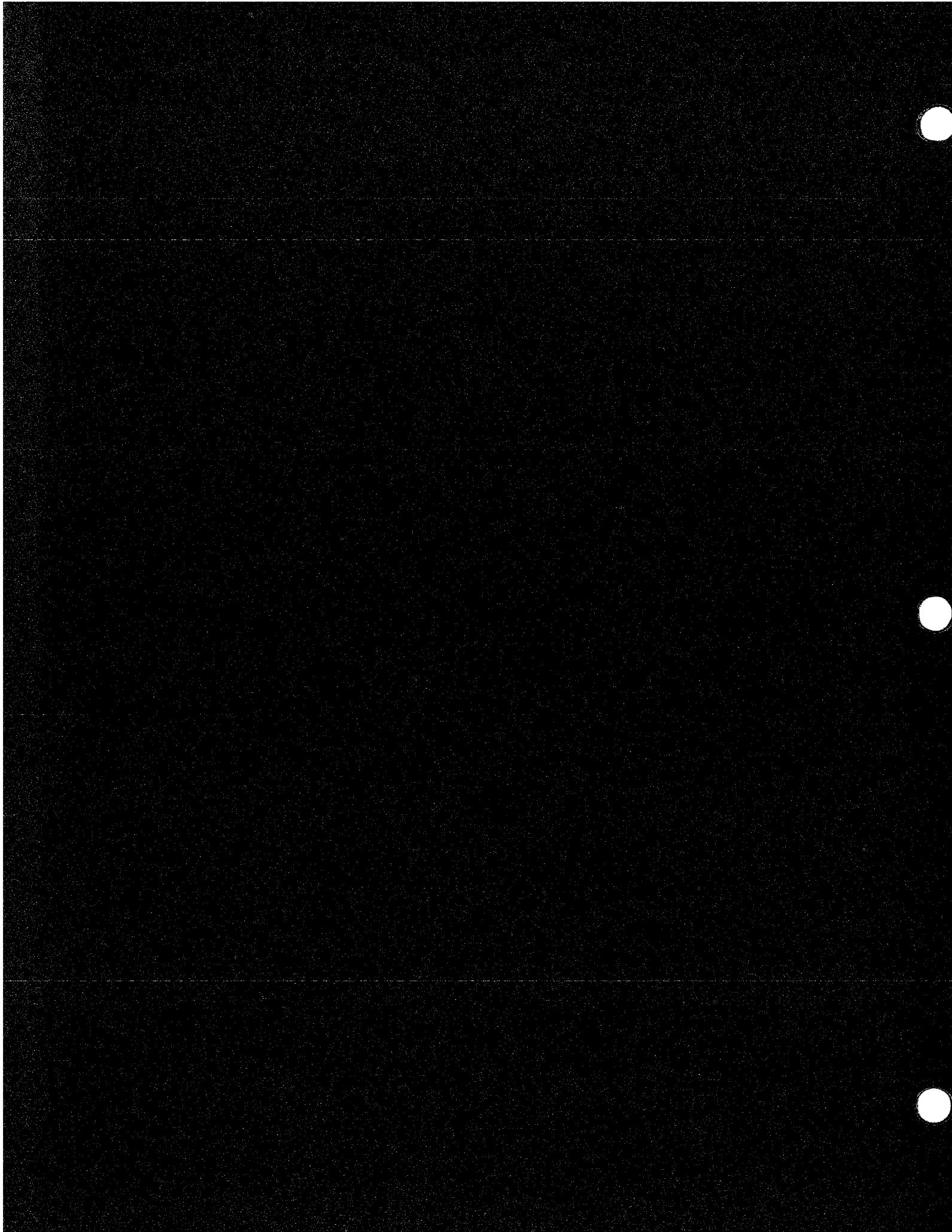
2   DCA-2 TO DISK DRIVE CABLING

This section describes the cabling between the DCA-2 channel adapter in an I/O subsystem model E (IOS-E) and DD-60, DD-61, or DD-62 disk drives. A description of the hardware used to connect the components, a method for labeling the cables, and the possible cabling configurations are included. The cabling for RD-62 drives in an RDE-6 is described in the "RDE-6 Removable Disk Enclosure" section of this manual.

Cabling Hardware

The hardware that connects the DD-60, DD-61, or DD-62 disk drives to the DCA-2 includes the IOS-E bulkhead connectors, a cable to connect the DCA-2 to a disk drive, two different daisy chain cables, and a terminator. Table 2-1 identifies each of these hardware components.

Table 2-1. 60 Series Disk Systems Cable Descriptions

Cable Description	Cable Length	CRI Part Number
DCA-2 to Disk Drive Cable (standard)	20 m (66 ft.)	12127800
DCA-2 to Disk Drive Cable (optional)	30 m (99 ft.)	12127801
Daisy Chain Cable (standard)	61 cm (24 in.)	12135100
Daisy Chain Cable (optional)	137 cm (54 in.)	12135101
2X Daisy Chain Cable †	180 cm (72 in.)	12247600
Terminator	N/A	01686600

† Refer to Figure 15-3 for a complete description of the 2X Daisy Chain cable.

NOTE: Two distinctly different daisy chain cables can be used to connect the 60 series disk drives. The standard daisy chain cables were included with initial shipments of these drives and are described in the next subsection. Later shipments of the 60 series disk drives include the newly designed 2X daisy chain cables, which are detailed in section 15 of this manual.

Daisy Chain Cables

Refer to the following subsections for information about the daisy chain cables used to connect 60 series drives.

Initial Daisy Chain Cable

The initial shipments of 60 series disk drives included the standard daisy chain cables described in this section. These cables connect between the output of the first drive and the input of the second drive. The terminator is connected to the rear of the last drive in a daisy chain. Figure 2-1 demonstrates the use of this initial daisy chain cable.
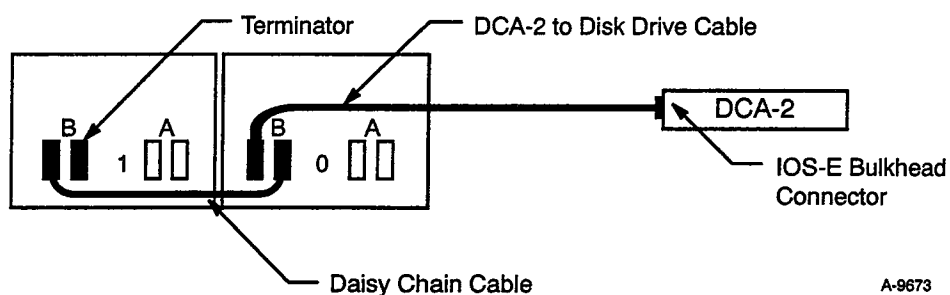
Figure 2-1. Initial Daisy Chain Cabling for 60 Series Disk Systems

2X Daisy Chain Cable

Later shipments of 60 series disk drives include a newly designed 2X daisy chain cable. This cable allows a drive to be removed from a daisy chain without affecting the other units on the chain. The 2X daisy chain cable also requires the terminator be connected to the end of the cable rather than the drive itself. If 3 or more drives are being daisy chained, additional 2X daisy chain cables must be used. Figure 2-2 demonstrates the use of a 2X daisy chain cable.
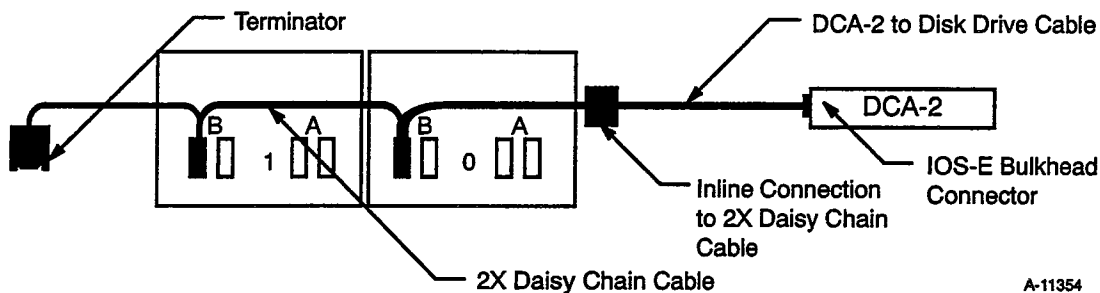
Figure 2-2. 2X Daisy Chain Cabling for 60 Series Disk Systems

IOS-E Bulkhead Connectors

Disk drives are connected to DCA-2 channel adapters through the IOS-E bulkhead. Figure 2-3 shows possible input/output cluster (IOC) 0 connector locations on the Z side of a CRAY Y-MP8I computer system.

Each EIOP has up to four channel adapters. Two channel adapter connectors are located on each side of the chassis. For example, the connectors for channel adapters 0 and 2, which are connected to EIOP 0, are on the Z side of the chassis (refer to Figure 2-3). The connectors for channel adapters 1 and 3, which are also connected to EIOP 0, are on the Y side of the chassis (not shown in Figure 2-3).

DD-60, DD-61, or DD-62 disk drive cables attach to the even-numbered connector (In) of the connector pair for each DCA-2. For example, the cable for a DD-60 connected to the DCA-2 in the number 5 channel adapter position would attach to connector 04 (refer to Figure 2-3).
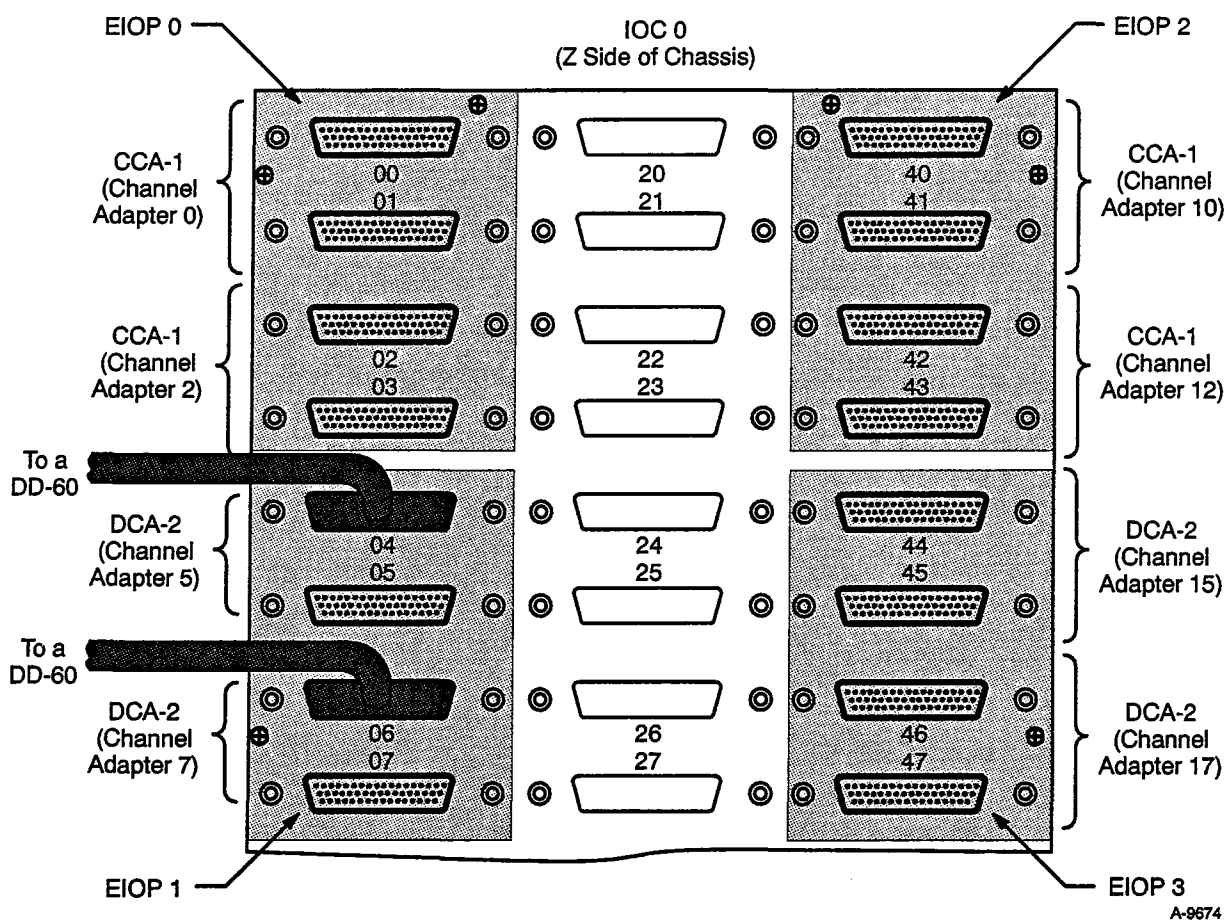
Figure 2-3. Possible IOC 0 Configuration on a CRAY Y-MP8I Computer System

CAUTION

Connect DCA-2 channel adapters to 60 series disk drives only. Connect 60 series disk drives only to DCA-2 channel adapters. Connecting disk drives to the wrong type of channel adapter results in damage to the drives and/or channel adapters.

Identical models of disk drive cables may be swapped to isolate a problem between the DCA-2 and a disk drive. Exchange only cables that are connected to the same type of channel adapter. The easiest way to ensure that the channel adapters are the same type is to exchange the cables at the disk drive end between the same type of disk drives.

For example, if an IOC were configured as shown in Figure 2-3, a problem could exist in the DCA-2 located in the number 5 channel adapter position or in the DD-60 to which it is connected. To isolate the problem, exchange the DD-60 cable at the disk drive end with another DD-60 cable. If the symptoms of the problem move to the other channel, the DD-60 is failing. If the symptoms of the problem remain on the same channel, the DCA-2 is failing and should be replaced with another DCA-2.

DCA-2 to Disk Drive Cables

The cables that connect the DCA-2 to a disk drive come in two lengths:
20 m (66 ft) and 30 meters (99 ft). The 20-m cable is standard, and the
30-m cable is optional. Table 2-2 lists the socket assignments for each
end of a DCA-2 to disk drive cable. Figure 2-4 shows the socket
locations on both ends of the cable.

Table 2-2. DCA-2 to Disk Drive Cable Socket Definitions

Pair No.	Signal Name	CINCH Connector Socket Number (+)	(−)	Disk Drive Connector Socket Number (+)	(−)
1	DC Ground	2	1	1	34
2	Select Out	14	13	43	27
3	Master Out	12	11	45	29
4	Sync Out	6	5	41	25
5	Sync In	10	9	15	48
6	Slave In	8	7	39	23
7	Attention In	4	3	20	4
8	Bus A − Bit 2^0	34	33	13	46
9	Bus A − Bit 2^1	37	36	30	14
10	Bus A − Bit 2^2	39	38	22	6
11	Bus A − Bit 2^3	41	40	26	10
12	Bus A − Bit 2^4	43	42	11	44
13	Bus A − Bit 2^5	45	44	28	12
14	Bus A − Bit 2^6	47	46	37	21
15	Bus A − Bit 2^7	49	48	5	38
16	Bus A − Parity Bit	51	50	47	31
17	Bus B − Bit 2^0	16	15	32	16
18	Bus B − Bit 2^1	18	17	49	33
19	Bus B − Bit 2^2	20	19	3	36
20	Bus B − Bit 2^3	22	21	7	40
21	Bus B − Bit 2^4	24	23	24	8
22	Bus B − Bit 2^5	26	25	9	42
23	Bus B − Bit 2^6	28	27	18	2
24	Bus B − Bit 2^7	30	29	35	19
25	Bus B − Parity Bit	32	31	17	50

Socket 1

EIOP End

Socket 19

Socket 51

Socket 1   Socket 18

Disk Drive
End

Socket 50   A-9675

Figure 2-4. DCA-2 to Disk Drive Cable Sockets

Daisy Chain Cable

The cable used to daisy chain disk drives is 24 in. (61 cm) long or 54 in. (137 cm) long for connecting a spare drive. Table 2-3 lists the pin and socket assignments for each end of the daisy chain cable. Figure 2-5 shows the pin and socket locations on both ends of the cable.

Table 2-3. Daisy Chain Cable Pin and Socket Definitions

Pair No.	Signal Name	Disk Drive Connector Pin Number		Disk Drive Connector Socket Number	
		(+)	(−)	(+)	(−)
1	DC Ground	1	34	1	34
2	Select Out	43	27	43	27
3	Master Out	45	29	45	29
4	Sync Out	41	25	41	25
5	Sync In	15	48	15	48
6	Slave In	39	23	39	23
7	Attention In	20	4	20	4
8	Bus A − Bit 2^0	13	46	13	46
9	Bus A − Bit 2^1	30	14	30	14
10	Bus A − Bit 2^2	22	6	22	6
11	Bus A − Bit 2^3	26	10	26	10
12	Bus A − Bit 2^4	11	44	11	44
13	Bus A − Bit 2^5	28	12	28	12
14	Bus A − Bit 2^6	37	21	37	21
15	Bus A − Bit 2^7	5	38	5	38
16	Bus A − Parity Bit	47	31	47	31
17	Bus B − Bit 2^0	32	16	32	16
18	Bus B − Bit 2^1	49	33	49	33
19	Bus B − Bit 2^2	3	36	3	36
20	Bus B − Bit 2^3	7	40	7	40
21	Bus B − Bit 2^4	24	8	24	8
22	Bus B − Bit 2^5	9	42	9	42
23	Bus B − Bit 2^6	18	2	18	2
24	Bus B − Bit 2^7	35	19	35	19
25	Bus B − Parity Bit	17	50	17	50

Figure 2-5. Daisy Chain (Drive-to-drive) Cable Pins and Sockets

Terminator

The terminator for 60 series disk drives must be used to terminate signals on the last, or only, drive connected to a channel. The CRI part number for the terminator is 01686600. Figure 2-6 shows the terminator.

A-9677
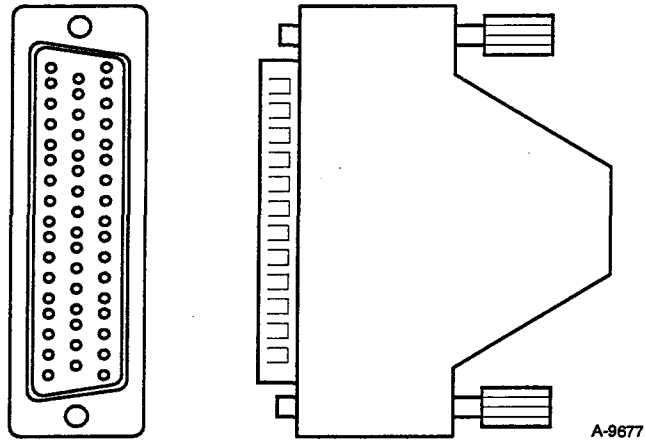
Figure 2-6. Terminator for 60 Series Disk Systems

Cable Labels

To prevent the connection of DD-60, DD-61, DD-62, and RD-62 disk drives to the wrong type of channel adapter, label all 60 series disk drive cables at both ends. Each label should contain the EIOP identification, channel number, device type, and drive unit number(s) to which the cable connects. A range of unit numbers can be specified for daisy chained channels.

The channel adapter type and EIOP channel adapter number provide further information about the channel adapter to which the cable is connected. Figure 2-7 shows these numbers on a sample cable label.
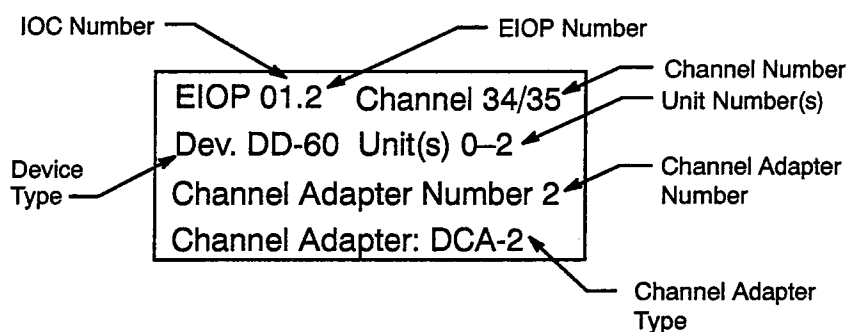
Figure 2-7. 60 Series Disk Drive Cable Label

Configurations

Sixty series disk drives can be cabled in three configurations: single port, daisy chain, or alternate path. Table 2-4 lists the number of components used in each configuration.

Table 2-4. Comparison of 60 Series Disk Drive Configurations

Configuration	DCA-2s	Disk Drives	Advantages
Single port	1	1	Fast data-transfer rate
Daisy chain	1	2 to 8	Large storage capacity per channel
Alternate path	2	2 to 8	Dual-channel access to data on the disk drives

Single-port Configuration

A single-port configuration connects one DCA-2 to one disk drive. In this configuration, the channel accesses information at the maximum data-transfer rate of the disk drive. Because only one disk drive connects to the channel, the storage capacity of the channel is the storage capacity of the disk drive.

Figure 2-8 shows eight disk drives, each connected in a single-port configuration. One DCA-2 connects to the input of port A, and a terminator connects to the output of port A for each disk drive. Port B is not used. Figure 2-9 shows the physical connections on the back of a disk drive.

Label every cable that connects a disk drive to a DCA-2. Doing so ensures that the cable connects a disk drive to a DCA-2 channel adapter. Cabling a 60 series disk drive to the wrong channel adapter damages both the disk drive and the channel adapter.
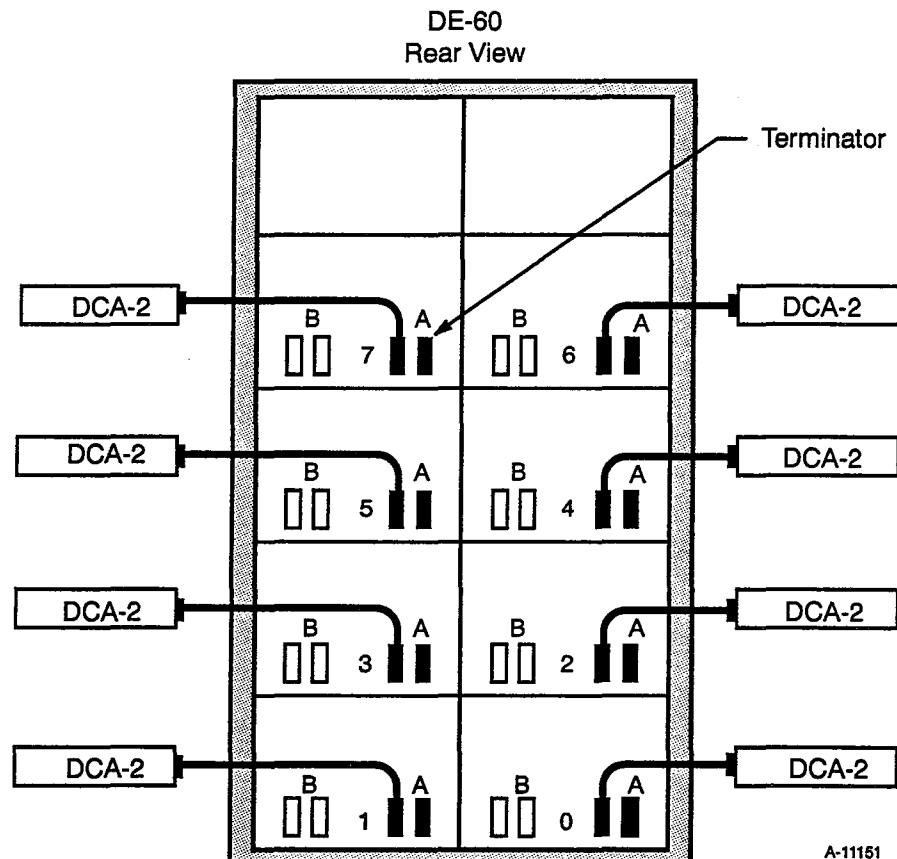
Figure 2-8. Single-port Configurations
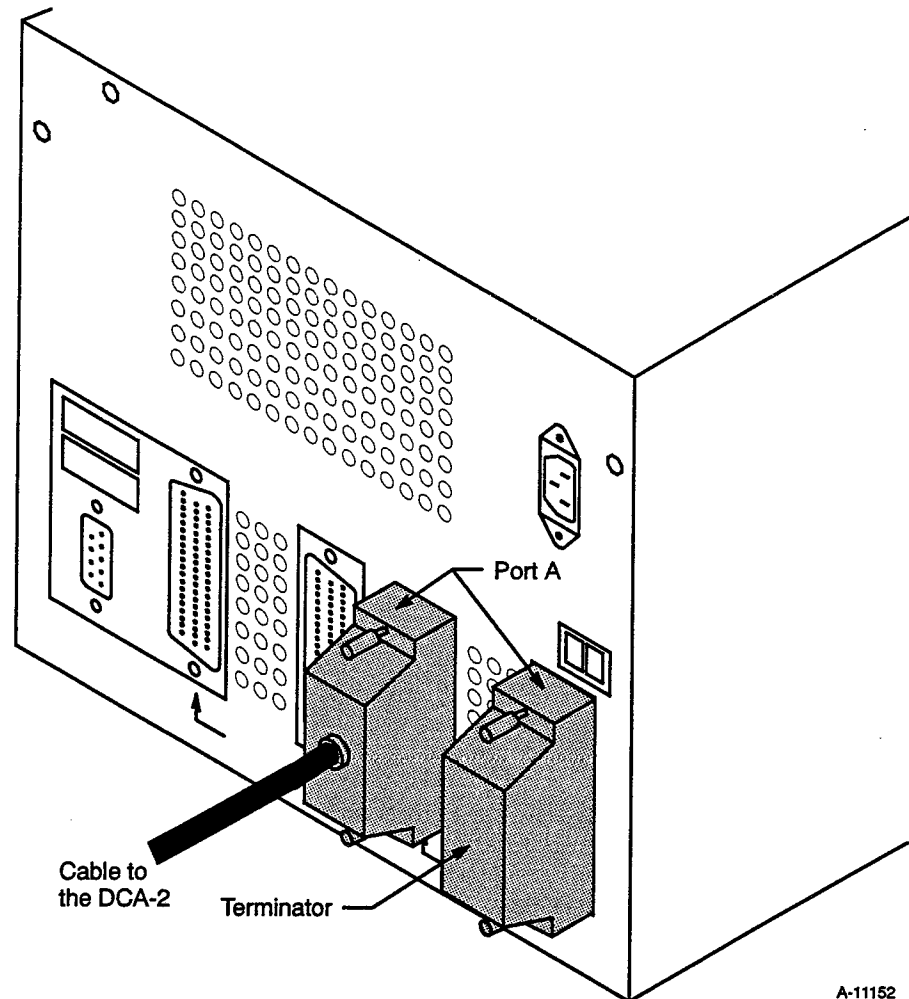
Figure 2-9. Single-port Configuration Cabling

Daisy Chain Configuration

A daisy chain configuration connects one DCA-2 to a maximum of eight disk drives of the same model. The data-storage capacity of the channel is the total storage capacity of all the disk drives in the daisy chain. Because only one disk drive can transfer data to the DCA-2 at a time, the data-transfer rate of the channel is the maximum transfer rate of one disk drive.

Figure 2-10 shows eight disk drives connected in a daisy chain configuration. One DCA-2 connects to the input of port A on the first disk drive in the chain. The output of port A on the first disk drive connects to the input of port A on the next disk drive. The last disk drive in the chain has a terminator connected on the output of port A. Figure 2-11 shows the physical connections on the back of two disk drives.

Label every cable that connects a disk drive to a DCA-2. Doing so ensures that the cable connects a disk drive to a DCA-2 channel adapter. Cabling a 60 series disk drive to the wrong channel adapter damages both the disk drive and the channel adapter.
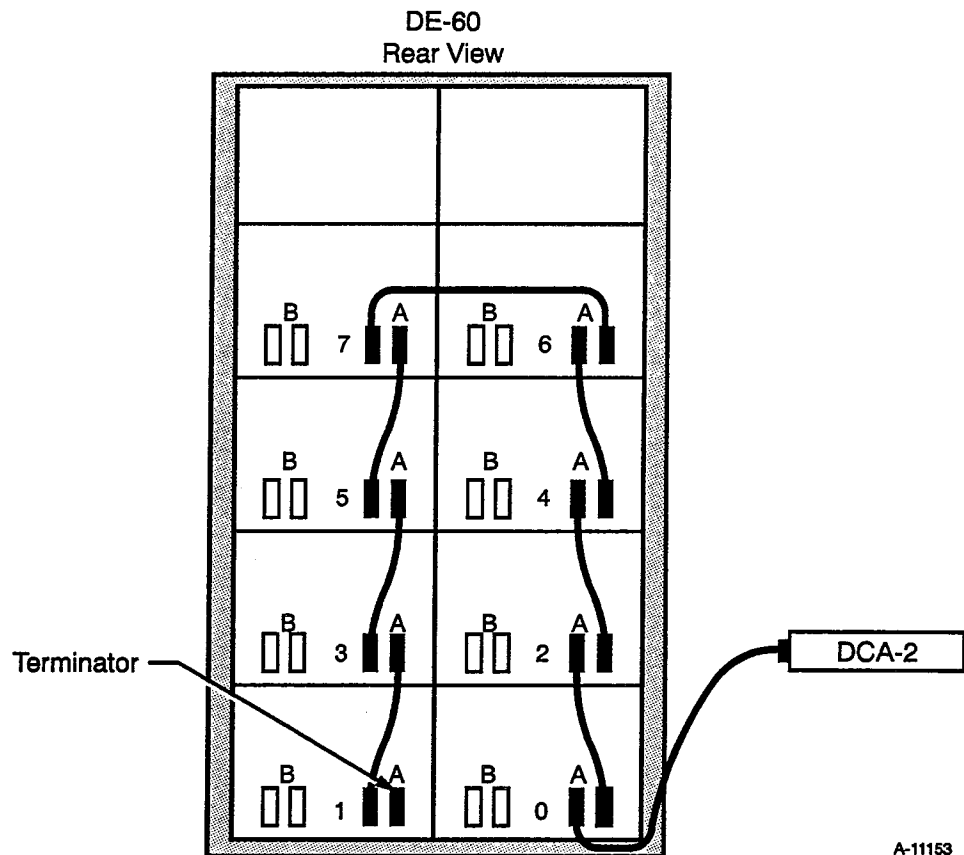
Figure 2-10. Daisy Chain Configuration
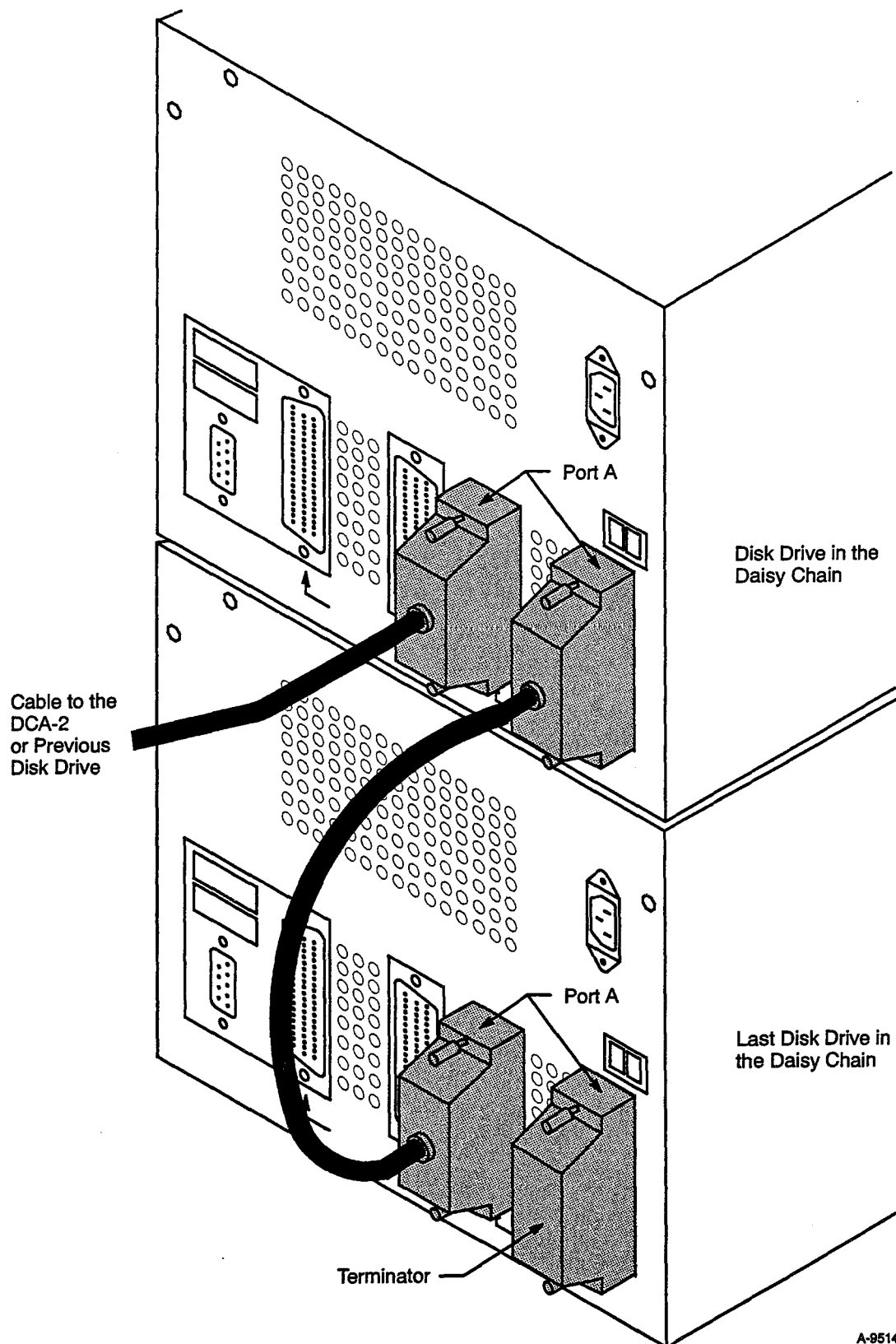
Figure 2-11. Daisy Chain Configuration Cabling

Cray Research Proprietary

Alternate-path Configuration

In an alternate-path configuration each drive is accessible from two DCA-2 channel adapters. Special software enhancements are necessary to use the resiliency advantages of an alternate-path configuration. Alternate-path configurations may connect to two DCA-2s in three combinations: within an EIOP, between two EIOPs, or between two input/output chassis (IOCs). Figure 2-12 shows each of these combinations, and Figure 2-13 is an illustration of the alternate-path configuration cabling.
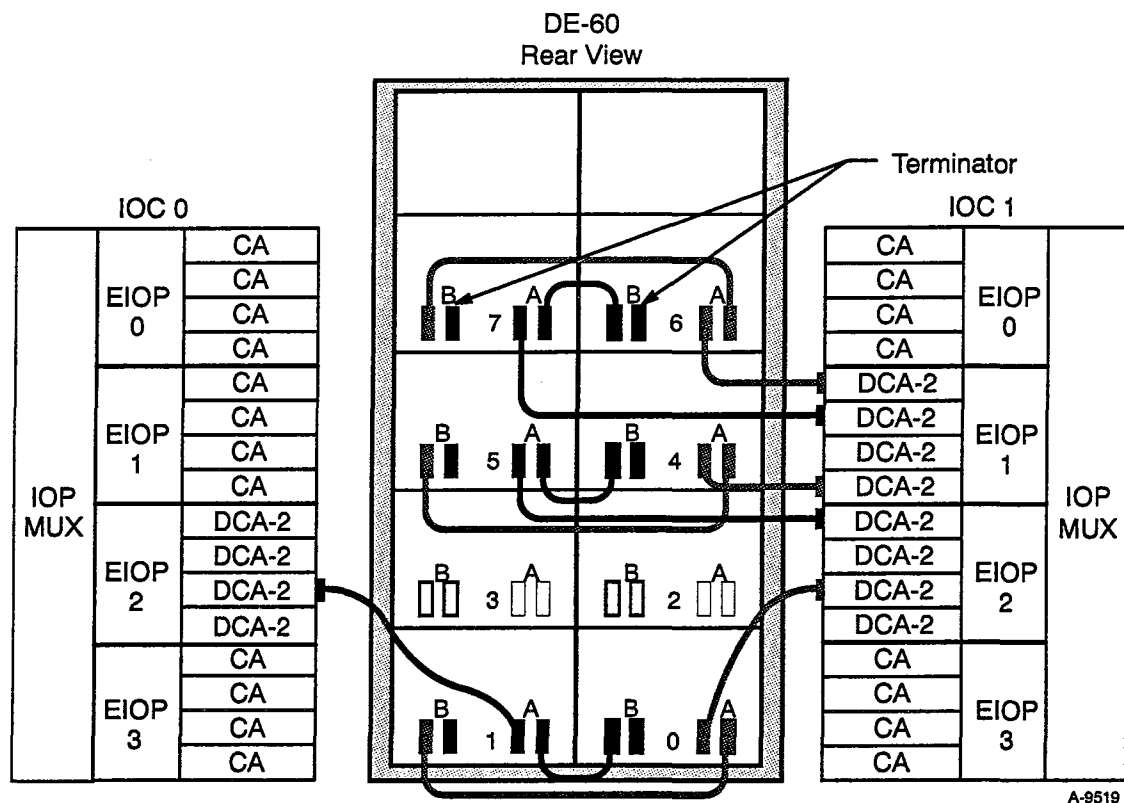
Figure 2-12. Alternate-path Daisy Chain Configuration Combinations

Disk drives 6 and 7 in Figure 2-12 are connected to DCA-2s within an EIOP. If one of the DCA-2s fails to function normally, the other DCA-2 in the EIOP can transfer information to or from the disk drive.

Disk drives 4 and 5 in Figure 2-12 are connected to DCA-2s within two EIOPs in one IOC. If one EIOP fails to function normally, the other EIOP can transfer information to or from the disk drive.

Disk drives 0 and 1 in Figure 2-12 are connected to DCA-2s in two separate IOCs. If one IOC fails to function normally, the other IOC can transfer information to or from the disk drive.
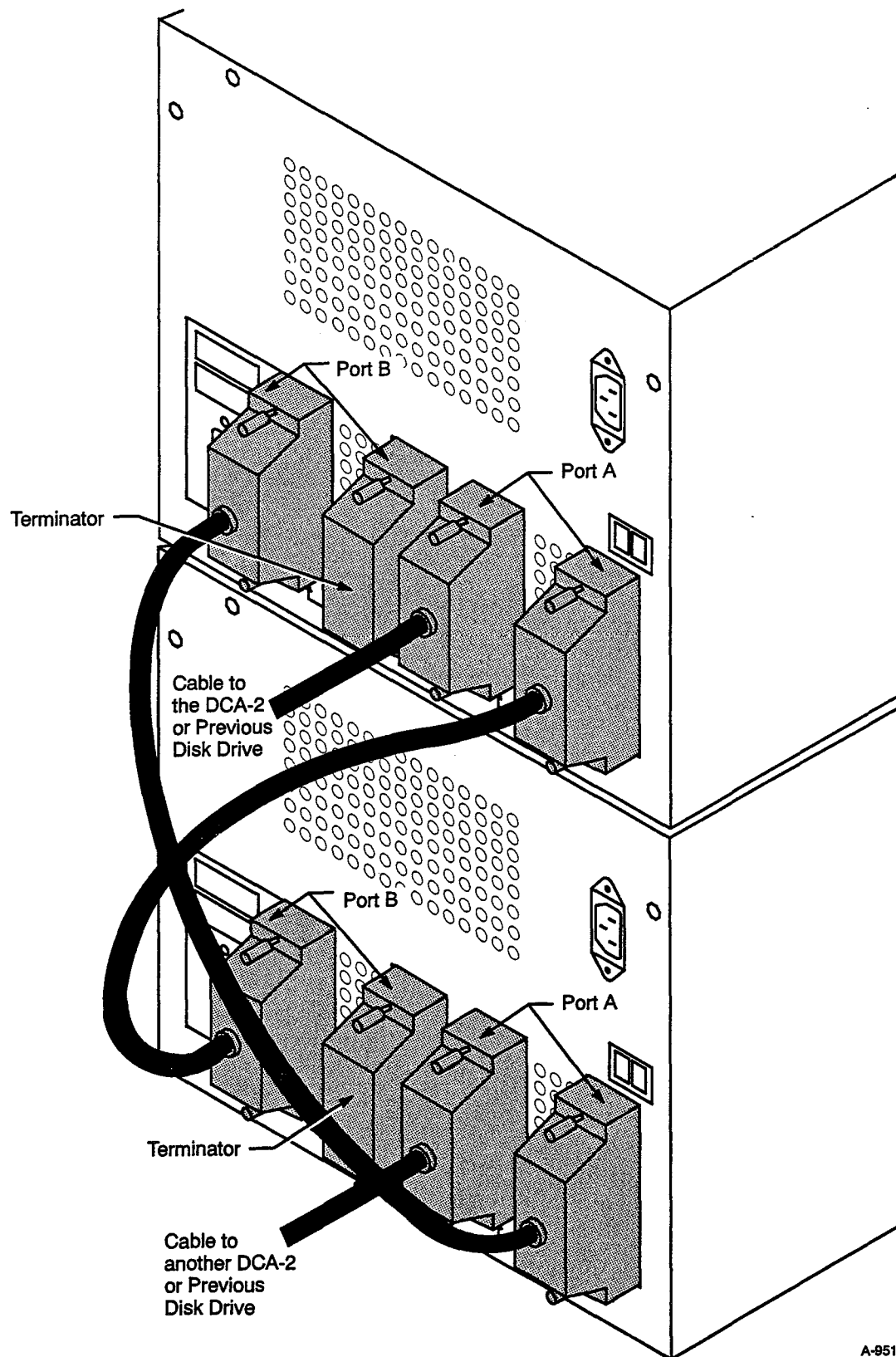
Figure 2-13. Alternate-path Configuration Cabling

SECTION 3
DCA-2 BASIC THEORY OF OPERATIONS
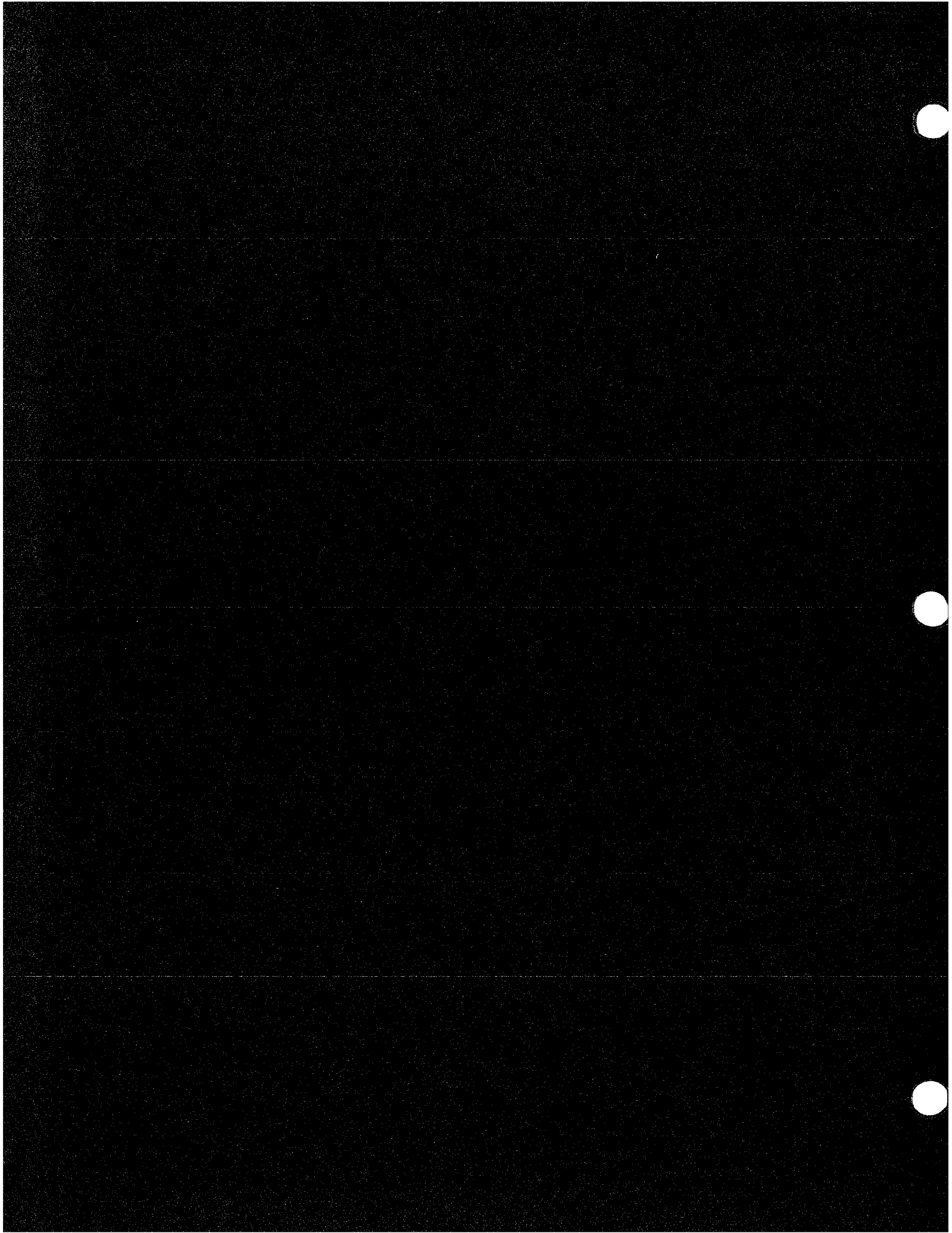
3 DCA-2 BASIC THEORY OF OPERATIONS

This section covers the basic theory of the DCA-2 disk channel adapter, including a description of the options on the DCA-2 and a description of the intelligent peripheral interface-2 (IPI-2) protocol.

DCA-2 Options

The DCA-2 contains 12 options that translate EIOP commands into IPI-2 protocol and transfer data between the EIOP and the disk drives. These options are described below. Figure 3-1 is a block diagram of the options on the DCA-2.

3YA Option

The 3YA option is an interface between the DCA-2 and the EIOP buffer board. It transfers data during write data and read data operations.

During write operations, the EIOP transfers a 72-bit word from the EIOP buffer board to the 3YA option in six 12-bit transfers. A word contains 64 bits of data and 8 single-error correction/double-error detection (SECDED) check bits. For each data word, a check byte (an 8-bit Hamming Code †) is generated. The 3YA option sends the 72-bit word to the 3YC option in five 16-bit transfers.

During read operations, the 3YA option receives each word from the 3YB option in four 16-bit transfers. During the last two transfers, the 3YA also receives check bits from the 3YB in 4-bit transfers. After receiving the data and check bits, the 3YA option sends the 72-bit word to the EIOP buffer board in six 12-bit transfers.

3YC Option

The 3YC option stores data and checks for errors during write data operations. After receiving the data and check bits from the 3YA option, the 3YC generates a new set of check bits for the data. If the new check bits do not match the previous set of check bits, the 3YC checks for a single-bit or double-bit SECDED error.

† Hamming, R. W. "Error Detection and Correcting Codes." *Bell System Technical Journal.* 29.2 (1950): 147-160.

If a single-bit error has occurred, the 3YC option changes the value of the incorrect bit and sends a signal to the 3DD option that a single-bit error occurred. If a double-bit error occurred, the 3YC is incapable of determining the incorrect bits and sends a signal to the 3DD option that a double-bit error occurred.

After performing SECDED, the 3YC generates 2 parity bits for each parcel of data. One parity bit is for bits 2^0 through 2^7 (bus B information) and the other parity bit is for bits 2^8 through 2^{15} (bus A information). The 3YC sends the parcel and parity bits to the 3DH options.

3DH0 Option

The 3DH0 option contains four separate circuits that generate error correction code (ECC) for four of the physical sectors in a DD-60 or half of a sector in a DD-61 or DD-62. For example, one circuit generates ECC for bits 2^0 and 2^8. These bits correspond to the data read from or written to channel 0 of a head group in a DD-60 (refer to the "Read/Write Boards" subsection in Section 5 of this manual.)

During write data operations, the 3DH0 receives 8 bits of data (bits 2^0 through 2^3 and bits 2^8 through 2^{11} of a parcel) from the 3YC option. The 3DH0 calculates a partial ECC for each byte of data and sends the byte of data to the 3DF option. After a sector of data passes through the 3DH0, the 3DH0 sends the complete ECC for four of the channels in a head group to the 3DF option in 8-bit transfers. The 3DH0 option also generates parity bits on the ECC data. The 3DH0 also receives a parity bit for bits 2^0 through 2^7 of a parcel (bus B information) from the 3YC option. The 3DH0 sends this parity bit with each byte of data it transfers to the 3DF option.

During read data operations, the 3DH0 receives 8 bits of data from the 3DE option (bits 2^0 through 2^3 and bits 2^8 through 2^{11} of a parcel). The 3DH0 calculates a partial ECC for each byte of data and stores the information. Immediately after receiving a sector of data, the 3DH0 receives ECC channels 0 through 3 in a head group from the 3DE option. The 3DH0 compares this ECC with the ECC it generated. If the codes do not match, the 3DH0 sends an ECC error to the 3DG option.

3DH1 Option

The 3DH1 option performs the same operations as the 3DH0 option; however, it receives bits 2^4 through 2^7 and 2^{12} through 2^{15} of a parcel. These bits correspond to channels 4 through 7 of a head group in a DD-60. The 3DH1 also transfers the parity bit for bits 2^8 through 2^{15} of a parcel (bus A information) from the 3YC option to the 3DF option.
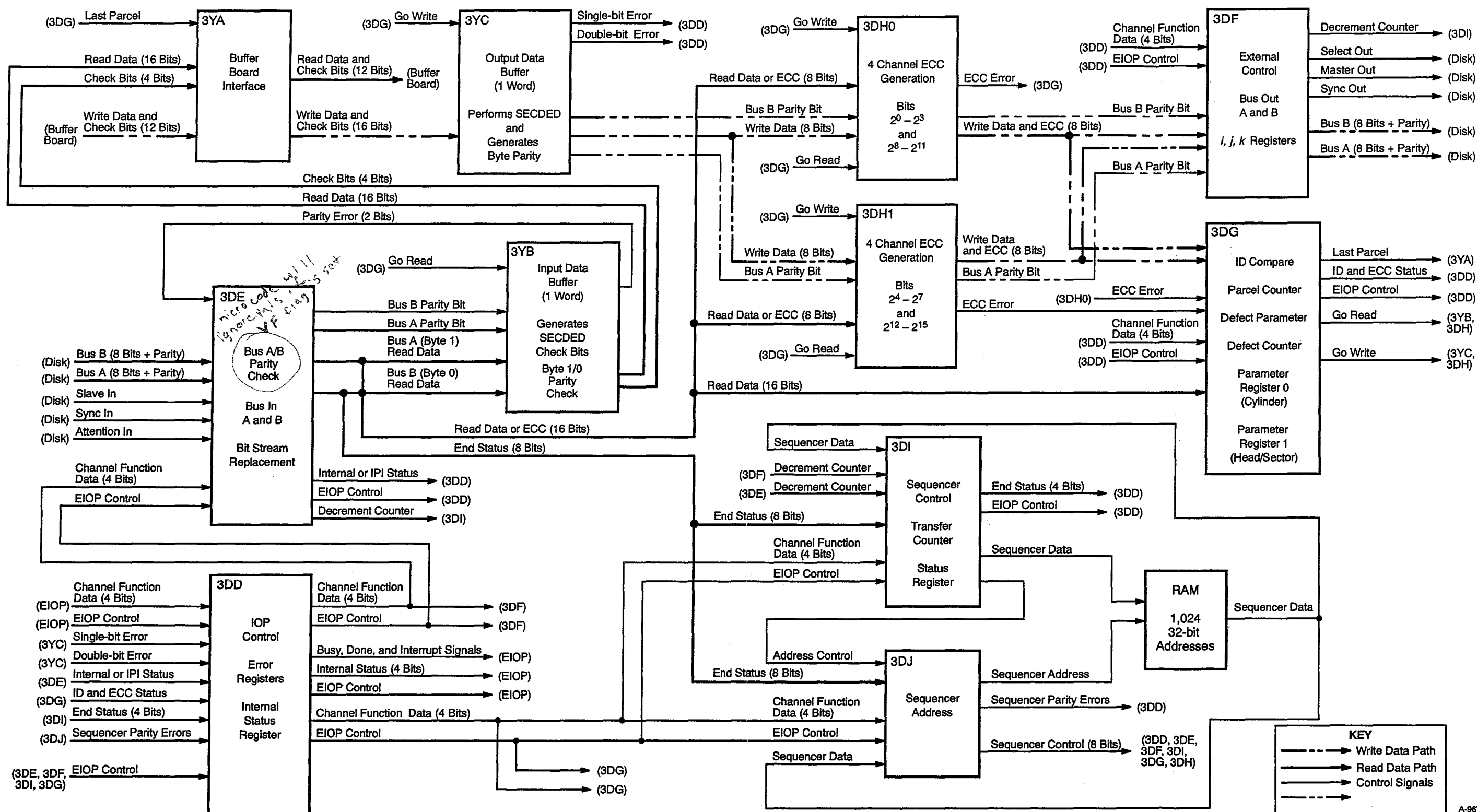
Figure 3-1. DCA-2 Options, Data Paths, and Control Signals

3DF Option

The 3DF option contains signal lines and registers used for IPI-2 information transfers to the disk drive. It also transfers write data from the DCA-2 to the disk drive.

The 3DF option is the IPI-2 communication link for transfers from the DCA-2 to the disk drive. It contains the Select Out, Master Out, Sync Out, Bus A, and Bus B signals used for IPI-2 protocol.

The 3DF option also contains i, j, and k registers, which store IPI commands. Before an information transfer occurs, the i, j, or k registers of the 3DF option are loaded with IPI commands. After receiving a signal from the sequencer (RAM), the 3DF transfers the information stored in the registers to the disk drive over bus A.

During a write data operation, the 3DF receives a parcel of information from the 3DH options. The 3DF option receives bits 2^0 through 2^3 and 2^8 through 2^{11} from 3DH0 and bits 2^4 through 2^7 and 2^{12} through 2^{15} from 3DH1. After receiving the parcel of data, 3DF loads bus B with bits 2^0 through 2^7 and bus A with bits 2^8 through 2^{15}.

The 3DF option also receives two parity bits from the 3DH options. Write data on bus B is protected with the parity bit from 3DH0, and write data on bus A is protected with the parity bit from 3DH1. The 3DF option sends the data and parity bits to the disk drive after it receives them from the 3DH options.

3DE Option

The 3DE option receives IPI-2 control and information transfers from the disk drive. It also receives read data from the disk drive and transfers it to the other options on the DCA-2.

The 3DE option is the IPI-2 communication link for transfers from the disk drive to the DCA-2. It receives the Slave In, Sync In, Bus A, and Bus B signals used for IPI-2 protocol.

During a read data operation, the 3DE receives a byte of data plus a parity bit from both bus A and bus B. After receiving the data and parity bits, the 3DE transfers the information to the 3YB, 3DG, 3DH0, and 3DH1 options. If the read data is ending status or status response information, the 3DE transfers the information from bus B to the 3DJ and 3DI options.

The 3DE option can also perform bit stream replacement, which corrects misread data from a failing head. The 3DE option replaces the data from the failing head with the sum of the data from the other heads and the

parity head. The DCA-2:17 channel function transfers the information needed for bit stream replacement to the 3DE. For more information on channel functions, refer to the "DCA-2 Channel Functions" section of this manual.

3YB Option

The 3YB option stores data and generates SECDED check bits during read data operations. It also checks the parity information.

During read data operations, the 3YB receives a word of data from the 3DE option in four 16-bit transfers. While receiving the word of data, the 3YB generates eight SECDED check bits for the word. It sends the word of data to the 3YA option in four 16-bit transfers. During the last two transfers of data, the 3YB sends the check bits in 4-bit transfers.

The 3YB option also generates a new parity bit for each byte of data it receives from the 3DE. If the new parity bit does not match the previous parity bit, the 3YB signals the 3DD that a byte 0 (bus B) or byte 1 (bus A) parity error occurred.

3DG Option

The 3DG option contains registers for comparing the sector ID field to the expected ID field. It also contains counters for counting parcels of information transferred between the DCA-2 and the disk drive.

The parameter register and cylinder register in the 3DG option store sector ID field parameters. The parameter register stores the head, sector, and option bits (ID parameter 1) of the ID field. The cylinder register stores the cylinder address (ID parameter 0) of the ID field. For more information on the sector ID field, refer to the "Format and Flaw Management" disk drive sections of this manual.

The 3DG option also contains a parcel counter and a defect counter. The parcel counter counts each parcel as it is transferred between the DCA-2 and the disk drive. The defect counter is used to create a defect pad that hides media flaws. For more information on media flaws and the defect pad, refer to the "Format and Flaw Management" disk drive sections of this manual.

3DD Option

The 3DD option receives DCA-2 channel functions and transfers control signals between the EIOP and DCA-2. After receiving a DCA-2 channel function from the EIOP, the 3DD transfers the function information to

the appropriate options on the DCA-2. The 3DD option also contains registers that store errors and internal status generated by the DCA-2. When requested, the 3DD transfers this status information to the EIOP.

3DI Option

The 3DI option counts the number of information transfers between the EIOP and the DCA-2. It also controls the sequencer address (3DJ option) and sends data to the RAM, hereafter referred to as the sequencer.

The transfer counter in the 3DI option counts the transfers between the EIOP local memory or EIOP buffer board and the DCA-2. Before an information transfer occurs, the transfer counter is loaded with the number of parcels to be transferred. The transfer counter decrements once for each parcel transferred.

The 3DI option also controls the sequencer address. The 3DI option signals the 3DJ option when to reset the sequencer address, when to advance the sequencer address, and when the transfer counter reaches zero.

3DJ Option

The 3DJ option transfers the sequencer address to the sequencer. After receiving the signals from the 3DI option, the 3DJ increments the sequencer address or resets the sequencer address to zero. The 3DJ option also monitors conditions of the other options on the DCA-2 that are used for branch control of the sequencer address.

RAM

The RAM is a sequencer that controls the operation of the DCA-2 registers and IPI-2 signal lines. It contains 1,024 addresses that each hold 32 bits of sequencer data.

After receiving the sequencer address from the 3DJ option, the sequencer transfers the sequencer data to the 3DI and the 3DJ options. As the 3DJ option increments through the addresses of the sequencer, the sequencer data controls when the registers on each option are transferred to signal lines and when the IPI-2 signal lines are set or reset.

The information stored in the RAM may be transferred to the EIOP local memory or written over by information from the EIOP local memory. For more information on loading or reading the sequencer data, refer to the "DCA-2 Channel Functions" section of this manual.

IPI-2 Interface Signals

IPI-2 interface signals transfer information between the DCA-2 and the 60 series disk drives. The 24 signals consist of control, attention in, and data signals. Figure 3-2 shows the signals in an IPI-2 interface.
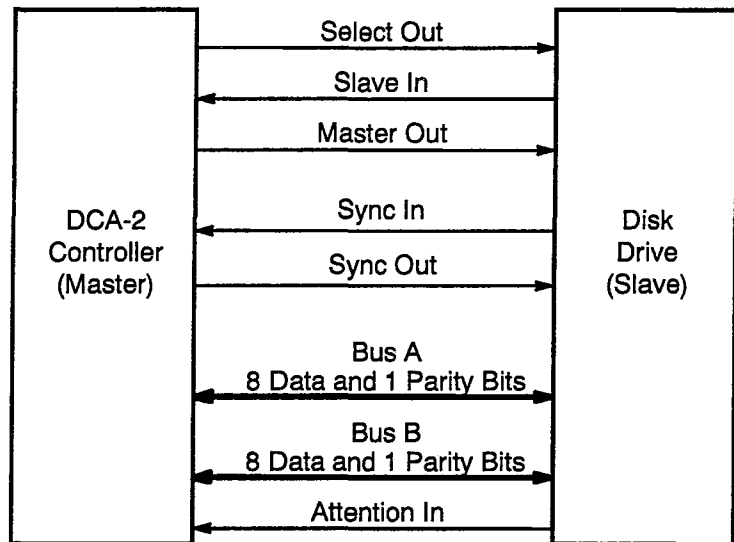
A-9520

Figure 3-2. IPI-2 Interface Signals

Control Signals

Five signals control disk drive operations. These signals are Select Out, Slave in, Master Out, Sync In, and Sync Out.

Select Out

The DCA-2 sends the Select Out signal to select a disk drive for use by the channel. Initially, when the Select Out signal is set, the requested disk drive address is transferred on bus A. The Select Out signal remains set until the controller releases the disk drive from the channel.

Slave In

The disk drive sends the Slave In signal in response to a Select Out signal or a Master Out signal from the DCA-2. During a select operation, the disk drive responds to the Select Out signal with the Slave In signal in order to acknowledge channel reservation. During a reset operation, the disk drive responds to the Master Out signal with the Slave In signal in order to acknowledge the reset operation.

Master Out

The DCA-2 sends the Master Out signal during a data transfer or disk drive reset. To initiate a data transfer, the DCA-2 sets the Master Out signal after loading bus A and bus B with data. To initiate a disk drive reset, the DCA-2 sets the Master Out signal after loading bus A with a reset parameter.

Sync In

The disk drive sends the Sync In signal during a data transfer or bus control operation. During read or write operations, the disk drive sets the Sync In signal to acknowledge the data transfer. For a read operation, the Sync In signal indicates valid data on the bus lines. For a write operation, the Sync In signal indicates that the disk drive is ready to accept data over the bus lines. During a bus control operation, the disk drive sets the Sync In signal to indicate acceptance of the bus control parameter.

Sync Out

The DCA-2 sends the Sync Out signal during a data transfer or bus control operation. During a read or write operation, the DCA-2 sets the Sync Out signal to acknowledge the data transfer. For a read operation, the Sync Out signal indicates the data on the bus lines was received. For a write operation, the Sync Out signal indicates valid data on the bus lines. During a bus control operation, the DCA-2 sets the Sync Out signal after loading bus A with the bus control parameter.

Attention In Signal

The disk drive uses the Attention In signal to inform the DCA-2 that service is required. The disk drive sets the Attention In signal if any of the following interrupts occur:

- Rotational position sensing (RPS) interrupt
- Command completion interrupt
- Status pending interrupt
- No longer busy interrupt

Data Signals

All information transfers between the DCA-2 and disk drive occur over bus A and bus B. Each bus carries nine signals. Eight of the signals are data bits and one signal is an odd parity bit.

Bus A

The DCA-2 uses bus A to transfer command parameters to the disk drive. Refer to the "IPI-2 Interface States" subsection in this section for more information on disk drive operations.

Bus B

The disk drive uses bus B to transfer command responses to the DCA-2. Refer to the "IPI-2 Interface States" subsection in this section for more information on disk drive operations.

Bus A and Bus B

During write operations, the DCA-2 uses bus A and bus B to transfer 18 bits of information to the disk drive. During read operations, the disk drive uses bus A and bus B to transfer 18 bits of information to the DCA-2. Refer to the "IPI-2 Interface States" subsection in this section for more information on disk drive operations.

IPI-2 Interface States

An IPI-2 interface state occurs when all control signals on the IPI-2 interface have a stable logical value. For example, the BUS CONTROL state has the Select Out signal set to 1, the Slave In signal set to 1, the Master Out signal set to 0, the Sync In signal set to 0, and the Sync Out signal set to 1 (refer to Figure 3-3).

Figure 3-3 shows all IPI-2 states. The arrows indicate which states are accessible from the other states. For example, the SLAVE ACKNOWLEDGE state can change into the DESELECT, BUS CONTROL, or TRANSFER READY state.
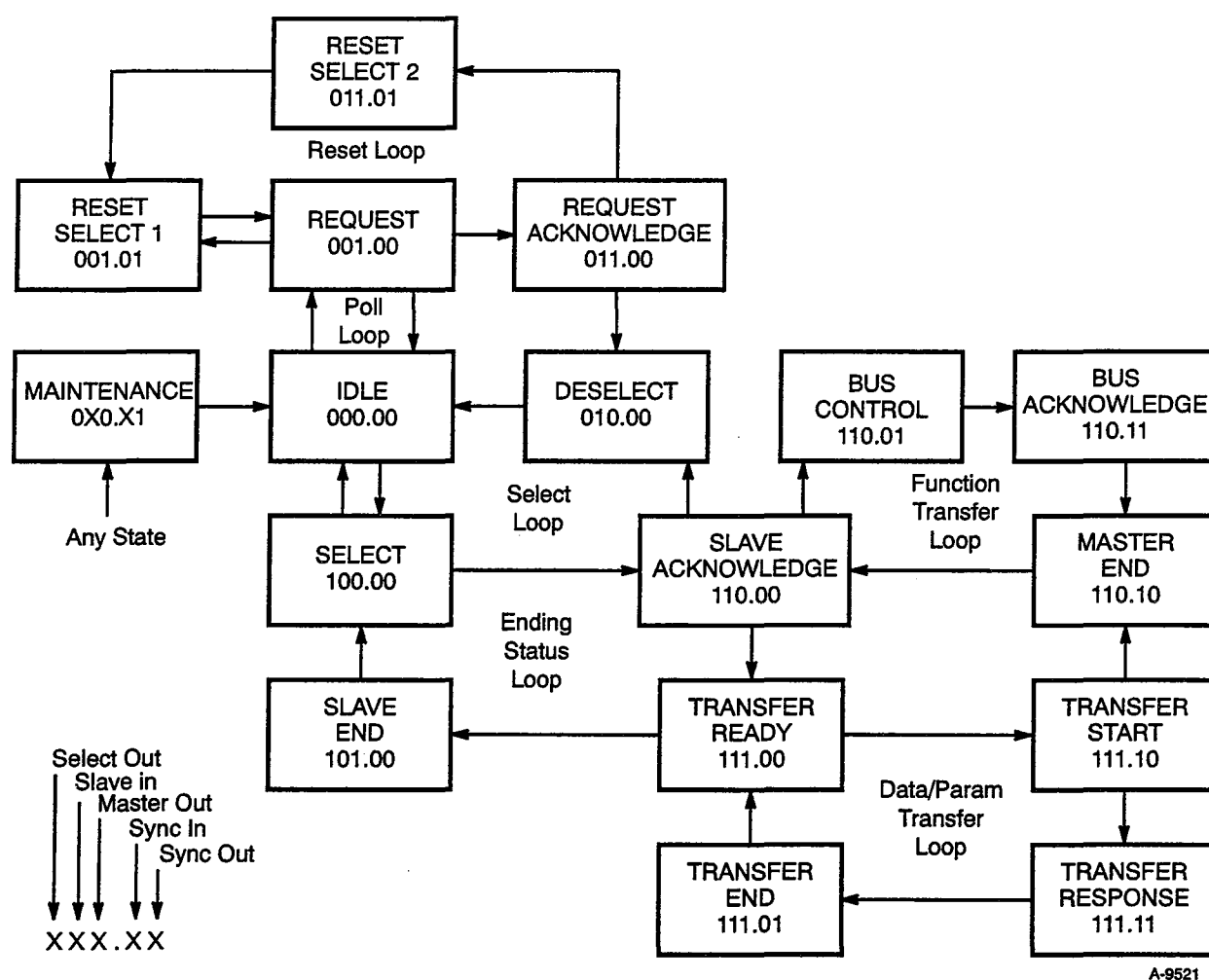
Figure 3-3. IPI-2 Interface States

During normal operation, the IPI-2 interface changes state when one signal changes logical value. For example, to change from the BUS CONTROL state to the BUS ACKNOWLEDGE state, only the Sync In signal changes from 0 to 1 (refer again to Figure 3-3).

All communication between the DCA-2 and disk drive follows a call-and-response sequence through the IPI-2 states. For example, when the interface is in the IDLE state, the DCA-2 sets the Select Out signal to 1, which puts the interface in the SELECT state. In response, the disk drive sets the Slave In signal to 1, which puts the interface into the SLAVE ACKNOWLEDGE state.

Each disk drive operation follows a sequence through the IPI-2 states. The sequencer on the DCA-2 controls the IPI-2 signals, which determine the order of the sequence. At the appropriate time in a sequence, the sequencer loads bus A and bus B with information and transfers it to the disk drive.

IPI-2 Interface State Sequences

An IPI-2 interface state sequence is a set path through the IPI-2 interface states that the sequencer controls. During the sequence, the DCA-2 and disk drive exchange information needed for disk drive operations. The sequences for disk drive operations are:

- Select disk drive
- Bus control
- Interlocked transfer to disk
- Interlocked transfer from disk
- Noninterlocked transfer to disk
- Noninterlocked transfer from disk
- Ending status
- Deselect
- Interrupt request (poll)
- Reset disk drive
- Master reset
- Transfer settings request
- Drive interrupt request

Each sequence determines what information the sequencer or disk drive must place on bus A or bus B. Table 3-1 lists the contents of bus A and bus B for all of the IPI-2 interface state sequences.

The following subsections describe each of the disk drive operation sequences in detail.

Table 3-1. Bus A and Bus B Contents for Each IPI Bus State Sequence

Sequence	Bus A								Bus B							
	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Select disk drive	0	Disk drive address Bit 2^4 is the least significant bit			0	0	0	Priority select	Disk drive 7	Disk drive 6	Disk drive 5	Disk drive 4	Disk drive 3	Disk drive 2	Disk drive 1	Disk drive 0
Bus control	Transfer control or data	Transfer out or in	0	Advance head	Bus control parameter				Bus B is not defined so each bit is set to 0							
Interlocked transfer-to-disk	IPI command parameters from the EIOP local memory to the disk drive								IPI command parameters from the EIOP local memory to the disk drive							
Interlocked transfer-from-disk	IPI status from the disk drive to the DCA2								IPI status from the disk drive to the DCA2							
Noninterlocked transfer-to-disk	Write data from the EIOP buffer board to the disk drive								Write data from the EIOP buffer board to the disk drive							
Noninterlocked transfer-from-disk	Read data from the disk drive to the EIOP buffer board								Read data from the disk drive to the EIOP buffer board							
Ending status	Good transfer	Bus parity error	0	0	0	0	0	0	Good transfer	Bus parity error	Odd byte transfer	Time dependent operation	Final status after operation			
Deselect	Bus A is not defined during a deselect sequence								Bus B is not defined during a deselect sequence							
Interrupt request (Poll)	0	Report busy status	Report ready status	Slave power failure alert	Power on status request	Report status pending interrupt	Report RPS interrupt	Report command complete interrupt	Disk drive 7	Disk drive 6	Disk drive 5	Disk drive 4	Disk drive 3	Disk drive 2	Disk drive 1	Disk drive 0
Reset disk drive	1	Disk drive address Bit 2^4 is the least significant bit			Disable interface drivers	Reset disk drive	Reset logical interface	Reset physical interface	Bus B is not defined during a reset disk drive sequence							
Master reset	Data out 2	Not used	Not used	Data out 1	Not used	Not used	Data out 0	Not used	Bus B is not defined during a master reset sequence							
Transfer settings request	1	Disk drive address Bit 2^4 is the least significant bit			0	0	0	0	0	0	1	0	0	1	1	0
Drive interrupts request	1	Disk drive address Bit 2^4 is the least significant bit			1	0	0	0	0	Busy status	Ready status	0	Priority select status	Status pending interrupt active	RPS interrupt active	Command complete interrupt

Select Disk Drive Sequence

The select disk drive sequence logically connects the DCA-2 to a disk drive. Figure 3-4 shows a select disk drive sequence.
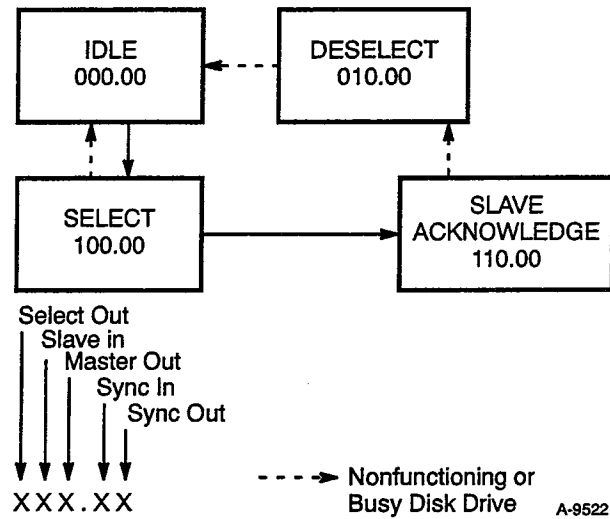
Figure 3-4. Select Disk Drive Sequence

Before a select disk drive sequence begins, the j register in the 3DF option must be loaded with the disk drive address (refer to Table 3-2).

Normal Selection

If no errors occur during the select disk drive sequence, a normal selection sequence occurs. The following sequence describes a normal selection sequence.

1. While the IPI-2 interface is in the IDLE state, the sequencer transfers the disk drive address from the j register in the 3DF option to bus A (refer to Table 3-2).

Table 3-2. Disk Drive Address on Bus A

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
0	Disk drive address Bit 2^4 is the least significant bit			0	0	0	Priority select

2. The sequencer sets the Select Out signal to 1, which puts the IPI-2 interface in the SELECT state.

3. The disk drive loads bus B with the drive select response and sets the Slave In signal equal to 1 (refer to Table 3-3), which puts the interface in the SLAVE ACKNOWLEDGE state and completes the select disk drive sequence.

Table 3-3. Drive Select Response on Bus B

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Disk drive 7	Disk drive 6	Disk drive 5	Disk drive 4	Disk drive 3	Disk drive 2	Disk drive 1	Disk drive 0

Busy Drive Selection

The following sequence describes a busy disk drive selection sequence.

1. While the IPI-2 interface is in the IDLE state, the sequencer transfers the disk drive address (refer to Table 3-2) from the j register in the 3DF option to bus A.

2. The sequencer sets the Select Out signal to 1, which puts the IPI-2 interface in the SELECT state.

3. If the requested disk drive is functioning normally, but cannot perform bus exchanges or information transfers, the disk drive sets the Slave In signal equal to 1 but does not load bus B with the select response. As a result, the interface is put in the SLAVE ACKNOWLEDGE state.

4. The sequencer resets the Select Out signal to 0 to enter the DESELECT state. The disk drive resets the Slave In signal to 0 to return the interface to the IDLE state.

Nonfunctioning Drive Selection

The following sequence describes a nonfunctioning disk drive selection sequence.

1. While the IPI-2 interface is in the IDLE state, the sequencer transfers the disk drive address from the j register in the 3DF option to bus A (refer to Table 3-2).

2. The sequencer sets the Select Out signal to 1, which puts the IPI-2 interface in the SELECT state.

3.   If the requested disk drive does not set the Slave In signal within a
     given time limit, the sequencer resets the Select Out signal to 0 and
     returns the interface to the IDLE state.

Bus Control Sequence

The bus control sequence transfers IPI-2 commands from the DCA-2 to
the disk drive. Figure 3-5 shows a bus control sequence.
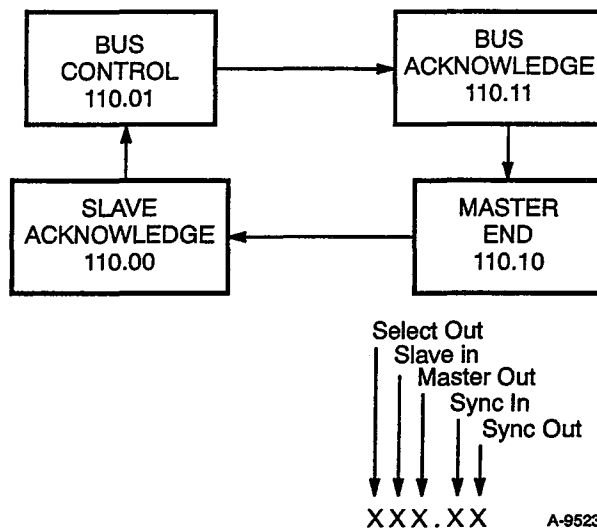
Figure 3-5. Bus Control Sequence

Before a bus control sequence begins, the j and k registers in the 3DF
option (refer to Figure 3-1) must be loaded with bus control commands
(refer to Table 3-4).

1.   While the IPI-2 interface is in the SLAVE ACKNOWLEDGE
     state, the sequencer transfers a bus control command from the j or
     k register in the 3DF option to bus A (refer to Table 3-4).

Table 3-4. Bus Control Command on Bus A

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Transfer control or data	Transfer out or in	0	Advance head	Bus control parameter			

Table 3-5 shows some examples of bus control commands used by Cray Research, Inc. (CRI).

Table 3-5. Sample Bus Control Commands Used by CRI

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Description
0	0	0	0	0	1	0	0	Load cylinder address
0	0	0	0	0	1	0	1	Load head address
0	0	0	0	0	1	1	0	Load rotational positional sensing (RPS) target sector
0	0	0	0	0	1	1	1	Load position
1	1	0	0	1	0	0	0	Read header
1	1	0	0	1	1	0	0	Read header at target
1	1	0	0	0	0	0	1	Read field
1	0	0	0	0	0	0	1	Write field
1	0	0	0	1	1	0	0	Write header at target

2. The sequencer sets the Sync Out signal to 1, which puts the interface into the BUS CONTROL state.

3. The disk drive loads bus B with the bus control response (refer to Table 3-6) and sets the Sync In signal to 1, which puts the interface into the BUS ACKNOWLEDGE state.

Table 3-6. Bus Control Response on Bus B

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Bus B is not defined, so each bit is set to 0							

4. The sequencer resets the Sync Out signal to 0, which puts the interface in the MASTER END state. Bus A is not loaded with any information.

5. The disk drive resets the Sync In signal to 0. This puts the interface in the SLAVE ACKNOWLEDGE state and completes a bus control sequence. Bus B is not loaded with any information.

Interlocked Transfer-to-disk Sequence

The interlocked transfer-to-disk sequence is used to transfer IPI command parameters from the EIOP local memory to the disk drive. Figure 3-6 shows an interlocked transfer-to-disk sequence.
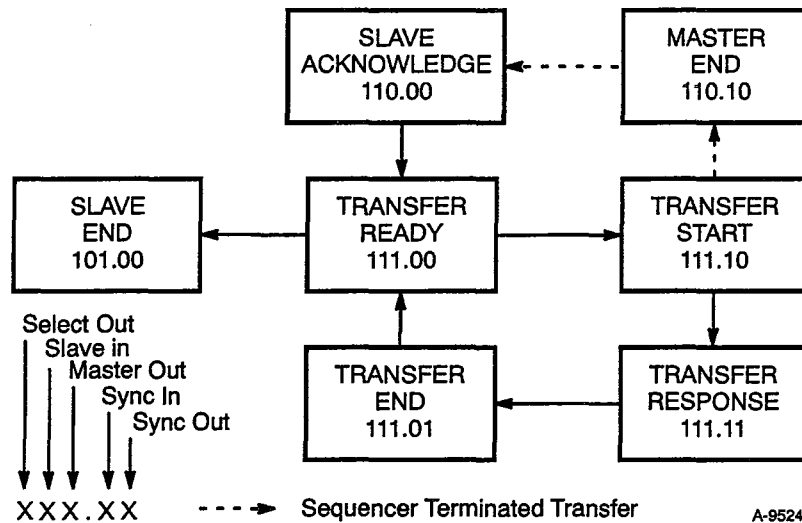
Figure 3-6. Interlocked Transfer-to-disk Sequence

Before starting an interlocked transfer-to-disk sequence, the sequencer must have successfully completed a bus control sequence.

Drive-terminated Transfer

If an interlocked transfer-to-disk sequence completes successfully, the disk drive terminates the transfer as shown in the following sequence.

1.   While the IPI-2 interface is in the SLAVE ACKNOWLEDGE state, the sequencer sets the Master Out signal to 1. Doing so puts the interface in the TRANSFER READY state and signals the disk drive that an information transfer is about to begin.

2.   The disk drive sets the Sync In signal to 1, which puts the interface in the TRANSFER START state and signals the controller that the disk drive is ready to receive information.

3.   The sequencer transfers one parcel of the command parameter from EIOP local memory to bus A and bus B and sets the Sync Out signal to 1, which puts the interface in the TRANSFER RESPONSE state.

4. The disk drive resets the Sync In signal to 0 to acknowledge that it received the parcel of information, which puts the interface in the TRANSFER END state.

5. The sequencer resets the Sync Out signal to 0 to acknowledge the transfer of 1 parcel of information to the disk drive. This puts the interface in the TRANSFER READY state.

    If there is more than 1 parcel of information to be transferred to the disk drive, the sequencer repeats Steps 2 through 5 until all of the parcels are transferred from local memory to the disk drive.

6. The disk drive resets the Slave In signal to 0 to end the interlocked transfer, which puts the interface in the SLAVE END state.

Sequencer-terminated Transfer

If an error occurs during an interlocked transfer to disk sequence, the sequencer terminates the transfer as shown in the following sequence.

1. At some point in the transfer, the disk drive sets the Sync In signal to 1, which puts the interface into the TRANSFER START state and signals the controller that the disk drive is ready to receive information.

2. While the IPI-2 interface is in the TRANSFER START state, the sequencer resets the Master Out signal to 0 to terminate the interlocked transfer, which puts the interface in the MASTER END state.

3. The disk drive resets the Sync In signal to 0 to acknowledge the termination, which puts the interface in the SLAVE ACKNOWLEDGE state.

4. The sequencer sets the Master Out signal to 1 to put the interface in the TRANSFER READY state.

5. The disk drive resets the Slave In signal to 0 to exit the transfer loop, which puts the interface in the SLAVE END state.

Interlocked Transfer-from-disk Sequence

The interlocked transfer-from-disk sequence is used to transfer IPI-2
status information from the disk drive to the EIOP local memory.
Figure 3-7 shows an interlocked transfer-from-disk sequence.
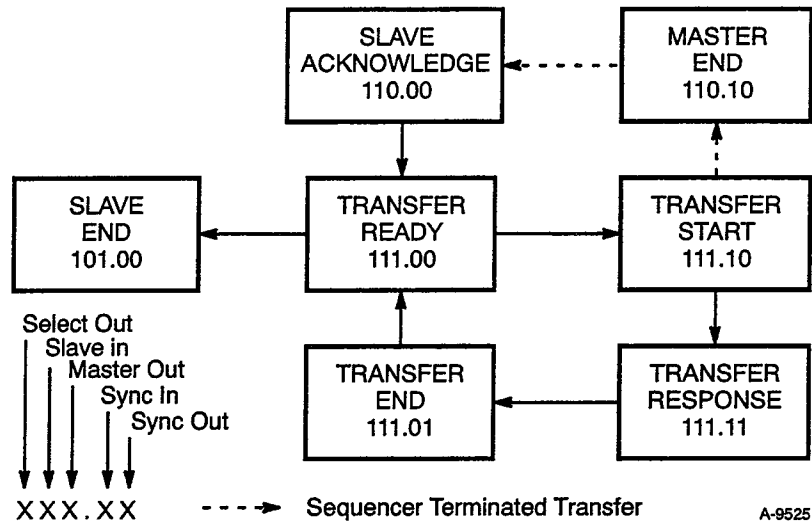
Figure 3-7. Interlocked Transfer-from-disk Sequence

Before starting an interlocked transfer-from-disk sequence, the sequencer
must have successfully completed a bus control sequence.

Drive-terminated Transfer

If an interlocked transfer-from-disk sequence completes successfully, the
disk drive terminates the transfer as shown in the following sequence.

1. While the IPI-2 interface is in the SLAVE ACKNOWLEDGE
    state, the sequencer sets the Master Out signal to 1. Doing so puts
    the interface in the TRANSFER READY state and signals the disk
    drive that an information transfer is about to begin.

2. The disk drive loads bus A and bus B with information and sets the
    Sync In signal to 1. Doing so puts the interface in the TRANSFER
    START state.

3. The sequencer receives the data and sets the Sync Out signal to 1.
    Doing so puts the interface in the TRANSFER RESPONSE state.

4. The disk drive resets the Sync In signal to 0 to acknowledge that
    the DCA-2 received a parcel of data. Doing so puts the interface in
    the TRANSFER END state.

5.   The sequencer resets the Sync Out signal to 0 to acknowledge that the transfer of 1 parcel of information from the disk drive. Doing so puts the interface in the TRANSFER READY state.

If there is more than 1 parcel of information to be transferred from the disk drive, the sequencer repeats Steps 2 through 5 until all of the parcels are transferred from the disk drive.

6.   The disk drive resets the Slave In signal to 0 to terminate the interlocked transfer, which puts the interface in the SLAVE END state.

Sequencer-terminated Transfer

If an error occurs during an interlocked transfer from disk sequence, the sequencer terminates the transfer as shown in the following sequence.

1.   At some point in the transfer, the disk drive sets the Sync In signal to 1, which puts the interface in the TRANSFER START state and signals the controller that the disk drive is ready to receive information.

2.   While in the TRANSFER START state, the sequencer resets the Master Out signal to 0 to terminate the interlocked transfer. Doing so puts the interface in the MASTER END state.

3.   The disk drive resets the Sync In signal to 0 to acknowledge the termination. Doing so puts the interface in the SLAVE ACKNOWLEDGE state.

4.   The sequencer sets the Master Out signal to 1 to put the interface in the TRANSFER READY state.

5.   The disk drive resets the Slave In signal to 0 to exit the transfer loop. Doing so puts the interface in the SLAVE END state.

Noninterlocked Transfer-to-disk Sequence

The noninterlocked transfer-to-disk sequence is used to transfer data from the EIOP buffer board to the disk drive media. Figure 3-8 shows a noninterlocked transfer-to-disk sequence.
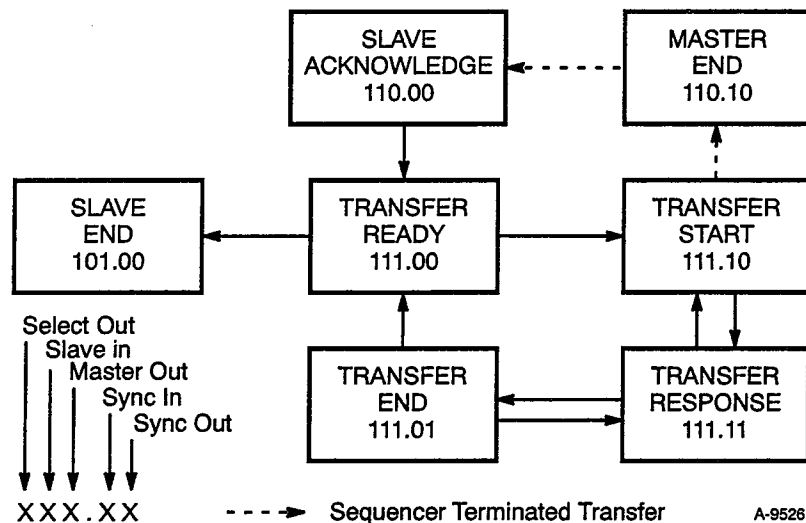
Figure 3-8. Noninterlocked Transfer-to-disk Sequence

Before starting a noninterlocked transfer-to-disk sequence, the sequencer must have successfully completed a bus control sequence.

Drive-terminated Transfer

If a noninterlocked data transfer-to-disk sequence completes successfully, the disk drive terminates the transfer as shown in the following sequence.

1. While the IPI-2 interface is in the SLAVE ACKNOWLEDGE state, the sequencer sets the Master Out signal to 1. Doing so puts the interface in the TRANSFER READY state and signals the disk drive that an information transfer is about to begin.

2. The disk drive and sequencer enter the noninterlocked transfer mode. In the noninterlocked mode, the interface does not follow a set sequence through the IPI bus states. All information transfers between the DCA-2 and disk drive media occur in noninterlocked mode.

The disk drive sets and resets the Sync In signal to create a pulse. After acknowledging the pulse, the sequencer transfers a parcel from the EIOP buffer board to bus A and bus B and sets the Sync Out signal to 1.

Every pulse of the Sync In signal created by the disk drive must be answered with a pulse of the Sync Out signal from the sequencer. Each Sync Out signal pulse sends a parcel of information over bus A and bus B. The pulses continue until all of the information has been transferred to the disk drive.

3.   After the disk drive sends a number of Sync In signal pulses to the sequencer, the disk drive must receive an equal number of Sync Out signals from the sequencer. When this occurs, the disk drive resets the Slave In signal to 0 and terminates the information transfer. Doing so puts the interface in the SLAVE END state.

Sequencer-terminated Transfer

If an error occurs during a noninterlocked data transfer to disk sequence, the sequencer terminates the transfer as shown in the following sequence.

1.   While the IPI-2 interface is in the SLAVE ACKNOWLEDGE state, the sequencer sets the Master Out signal to 1. Doing so puts the interface in the TRANSFER READY state and signals the disk drive that an information transfer is about to begin.

2.   The disk drive and sequencer enter the noninterlocked transfer mode. The disk drive sets and resets the Sync In signal to create a pulse. After acknowledging the pulse, the sequencer transfers a parcel of information from the EIOP buffer board to bus A and bus B and sets the Sync Out signal to 1.

Every Sync In signal pulse created by the disk drive must be answered with a Sync Out signal pulse by the sequencer. Each Sync Out signal pulse sends a parcel of information out on bus A and bus B.

3.   To terminate the data transfer, the sequencer replaces one of the Sync Out signal pulses with a Master Out signal pulse. After sending the Master Out signal pulse, the sequencer stops transferring information to bus A and bus B.

4.   Again, the disk drive must receive the same number of Sync Out signal pulses (including the one Master Out signal pulse) as Sync In signal pulses it sent to the sequencer. When this occurs, the disk drive resets the Slave In signal to 0 and terminates the information transfer. Doing so puts the interface in the SLAVE END state.

Noninterlocked Transfer-from-disk Sequence

The noninterlocked transfer-from-disk sequence is used to transfer data from the disk drive to the EIOP buffer board. Figure 3-9 shows a noninterlocked transfer-from-disk sequence.
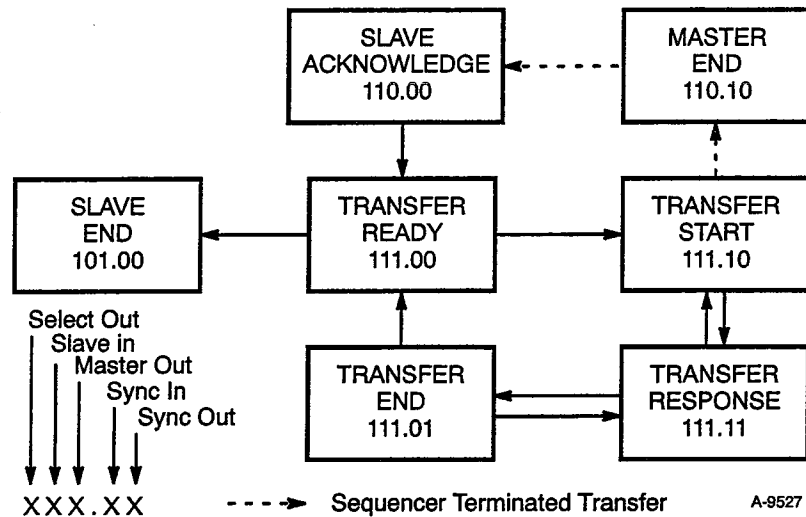
Figure 3-9. Noninterlocked Transfer-from-disk Sequence

Before starting a noninterlocked transfer-from-disk sequence, the sequencer must have successfully completed a bus control sequence.

Drive-terminated Transfer

If an information transfer from disk completes successfully, the disk drive terminates the transfer as shown in the following sequence.

1. While the IPI-2 interface is in the SLAVE ACKNOWLEDGE state, the sequencer sets the Master Out signal to 1. Doing so puts the interface in the TRANSFER READY state and signals the disk drive that an information transfer is about to begin.

2. The disk drive and sequencer enter the noninterlocked transfer mode. The noninterlocked mode is a condition where the interface does not follow a set sequence through the IPI-2 bus states. All information transfers between the DCA-2 and disk drive media occur in noninterlocked mode.

The disk drive loads a parcel of information on bus A and bus B and sets the Sync In signal to 1. The disk drive then resets the Sync In signal to 0 to create a pulse. Each pulse sends a parcel of information on bus A and bus B.

3. After receiving the first parcel of information, the sequencer transfers the parcel to the EIOP buffer board and generates a Sync Out signal pulse. Every Sync In signal pulse created by the disk drive must be answered by a Sync Out signal pulse from the sequencer; however, the disk drive does not have to wait for a Sync Out signal pulse before sending another parcel of information.

4. After sending all parcels of information, the disk drive must receive the same number of Sync Out signal pulses from the sequencer as Sync In signal pulses it sent to the sequencer. When this occurs, the disk drive resets the Slave In signal to 0 and terminates the information transfer. Doing so puts the interface into the SLAVE END state.

Sequencer-terminated Transfer

If an error occurs during an information transfer-from-disk sequence, the sequencer terminates the transfer as shown in the following sequence.

1. While the IPI-2 interface is in the SLAVE ACKNOWLEDGE state, the sequencer sets the Master Out signal to 1. Doing so puts the interface into the TRANSFER READY state and signals the disk drive that an information transfer is about to begin.

2. The disk drive and sequencer enter the noninterlocked transfer mode. The disk drive loads a parcel of information on bus A and bus B and sets the Sync In signal to 1. The disk drive then resets the Sync In signal to 0 to create a pulse. Each pulse sends a parcel of information on bus A and bus B. Every Sync In signal pulse must be answered by a Sync Out signal pulse from the sequencer.

3. To terminate the data transfer, the sequencer replaces one of the Sync Out signal pulses with a Master Out signal. After sending the Master Out signal pulse, the sequencer accepts up to eight Sync In signal pulses while it waits for the disk drive response.

4. Again, the disk drive must receive the same number of Sync Out signal pulses (including the one Master Out signal pulse) as Sync In signal pulses it sent to the sequencer. After receiving the pulses, the disk drive resets the Slave In signal to 0 and terminates the information transfer. Doing so puts the interface in the SLAVE END state.

Ending Status Sequence

The ending status sequence generates controller and disk drive status after an information transfer. Figure 3-10 shows a block diagram of an ending status sequence.
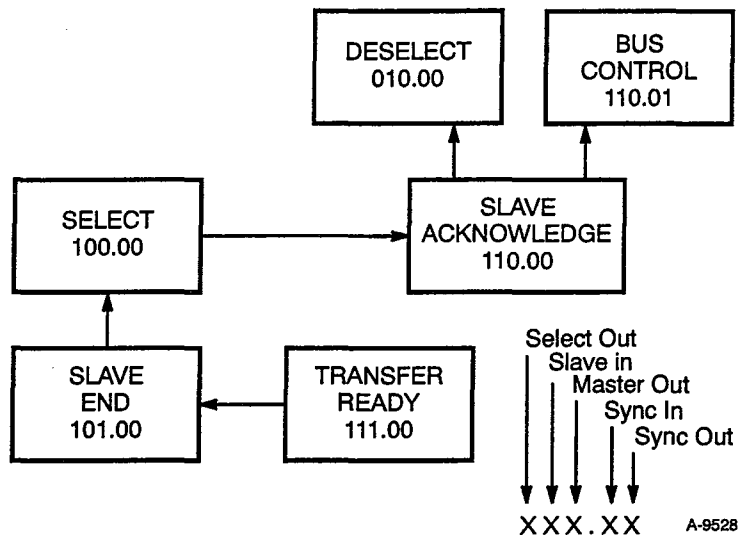
Figure 3-10. Ending Status Sequence

After every information transfer between the DCA-2 and disk drive, the sequencer must perform an ending status sequence.

1. After an information transfer, the disk drive resets the Slave In signal to 0. Doing so puts the interface into the SLAVE END state.

2. The sequencer places the controller status on bus A and resets the Master Out signal to 0 (refer to Table 3-7). Doing so puts the interface into the SELECT state.

Table 3-7. Controller Status on Bus A

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Good transfer	Bus parity error	0	0	0	0	0	0

Table 3-8 shows examples of a successful and an unsuccessful information transfer.

Table 3-8. Sample Controller Statuses

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Description
1	0	0	0	0	0	0	0	The DCA-2 indicates the information transfer was successful.
0	0	0	0	0	0	0	0	The DCA-2 indicates the information transfer was not successful.

3.   The disk drive places the drive ending status on bus B and sets the Slave In signal to 1 (refer to Table 3-9). Doing so puts the interface in the SLAVE ACKNOWLEDGE state.

Table 3-9. Drive Ending Status on Bus B

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Good transfer	Bus parity error	Odd byte transfer	Timed operation	Final status after operation			

Table 3-10 shows examples of drive ending status. For more information on the drive ending statuses on bus B, refer to the "DCA-2 Systems Status" section.

Table 3-10. Sample Drive Ending Statuses

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Description
1	0	0	0	0	0	0	0	The disk drive indicates a successful information transfer.
0	1	0	0	0	0	0	0	The disk drive detected a parity error on a bus control command, information transfer, or controller status.
0	0	0	1	0	0	0	0	The disk drive has not completed the last command.
0	0	0	0	0	0	0	1	The disk drive is busy and did not accept the last bus control command.

If the sequencer is starting another disk drive operation, it loads bus A with a bus control command and starts a bus control sequence.

If the sequencer is deselecting the disk drive, it starts a deselect sequence.

Deselect Sequence

The deselect sequence logically disconnects a disk drive from the DCA-2. Figure 3-11 shows a deselect sequence.
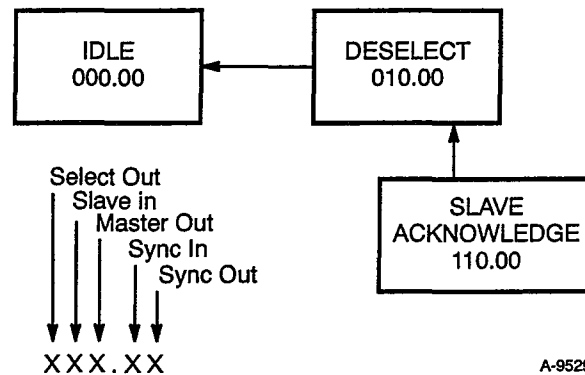
Figure 3-11. Deselect Sequence

The deselect sequence starts from the SLAVE ACKNOWLEDGE state. The sequencer performs a deselect sequence after an ending status or select sequence.

1.   While the IPI-2 interface is in the SLAVE ACKNOWLEDGE state, the sequencer resets the Select Out signal to 0. Doing so puts the interface in the DESELECT state. Bus A and bus B do not contain any information.

2.   The disk drive resets the Slave In signal to 0. Doing so puts the interface in the IDLE state. Bus A and bus B do not contain any information.

During disk drive operations, the sequencer must perform a deselect sequence before performing an interrupt request (poll), disk drive reset, master reset, transfer settings request, or drive interrupt request sequence.

Interrupt Request (Poll) Sequence

The interrupt request (poll) sequence requests all disk drives connected to the channel that have specific interrupts pending to respond on bus B. Figure 3-12 shows an interrupt request sequence.
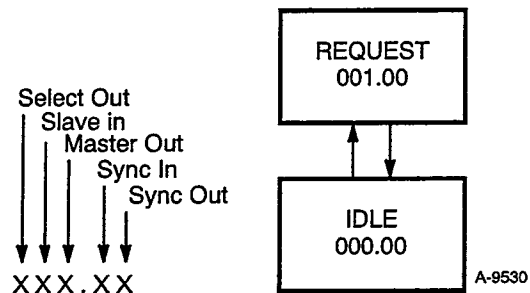
Figure 3-12. Interrupt Request (Poll) Sequence

Before an interrupt request sequence begins, the j and k registers in the 3DF option (refer again to Figure 3-1) must be loaded with the interrupt request (refer to Table 3-11). The i register in the 3DF option must also be loaded with a bit mask set for the requested disk drive.

1. The sequencer transfers the interrupt request from the j register to bus A and sets the Master Out signal to 1 (refer to Table 3-11). Doing so puts the interface in the REQUEST state.

Table 3-11. Interrupt Request on Bus A

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
0	Report busy status	Report ready status	Slave power failure alert	Power on status request	Report status pending interrupt	Report RPS interrupt	Report command complete interrupt

2. Each disk drive that matches the interrupt request loads bus B with the drive select response (refer to Table 3-12) and sets the Attention In signal. As soon as the disk drive that matches the bit mask in the i register responds, the sequencer resets the Master Out signal to 0 to complete the interrupt request sequence.

Table 3-12. Drive Select Response on Bus B

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Disk drive 7	Disk drive 6	Disk drive 5	Disk drive 4	Disk drive 3	Disk drive 2	Disk drive 1	Disk drive 0

Reset Disk Drive Sequence

The reset disk drive sequence resets a selected disk drive. Figure 3-13 shows a reset disk drive sequence.
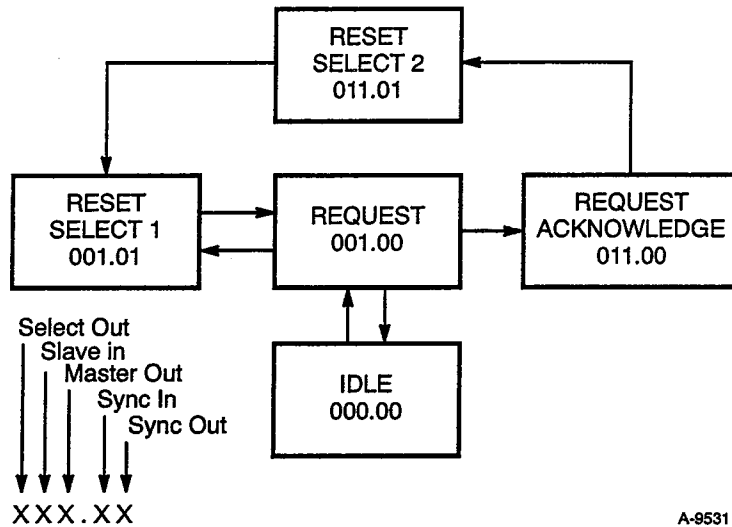
Figure 3-13. Reset Disk Drive Sequence

Before a reset disk drive sequence begins, the *j* register in the 3DF option (refer to Figure 3-1) must be loaded with the selective reset (refer to Table 3-13).

1. The sequencer transfers the selective reset (refer to Table 3-13) from the *j* register in the 3DF option to bus A and sets the Master Out signal to 1. Doing so puts the interface in the REQUEST state.

Table 3-13. Selective Reset on Bus A

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	Disk drive address Bit 2^4 is the least significant bit			Disable interface drivers	Reset disk drive	Reset logical interface	Reset physical interface

2. The disk drive sets the Slave In signal to 1, which puts the interface in the REQUEST ACKNOWLEDGE state. Bus B is not defined during a reset disk drive sequence.

3. The sequencer sets the Sync Out signal to 1 to put the interface in the RESET SELECT 2 state.

4. The disk drive resets the Slave In signal to 0 to enter the RESET SELECT 1 state.

5. The disk drive starts the reset action after the Sync Out signal is set to 1 for at least 2 microseconds.

6. After a set amount of time, the sequencer resets the Sync Out signal to 0 to reenter the REQUEST state.

7. The sequencer terminates the reset disk drive sequence by resetting the Master Out signal to 0.

Master Reset Sequence

The sequencer performs a master reset sequence to enter the MAINTENANCE state. Figure 3-14 shows a master reset sequence.
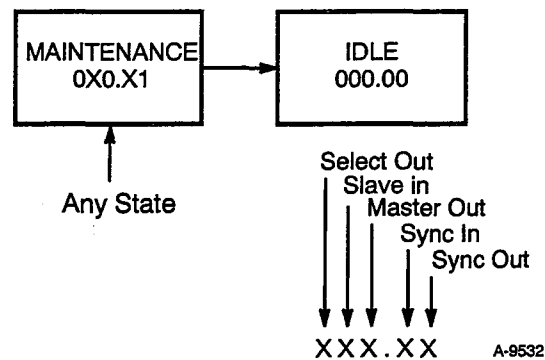
Figure 3-14. Master Reset Sequence

The master reset sequence starts from any state on the IPI-2 interface.

1. The sequencer resets the Select Out and Master Out signals to 0 and sets the Sync Out signal to 1 for at least 10 microseconds. Doing so puts the interface into the MAINTENANCE state.

2. The sequencer loads bus A with a master reset parameter (refer to Table 3-14) and resets the Sync Out signal to 0 to enter the IDLE state. (Only two of the three data out bits, 2^1, 2^4, or 2^7 are set.)

Table 3-14. Master Reset on Bus A

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Data out 2	Not used	Not used	Data out 1	Not used	Not used	Data out 0	Not used

Transfer Settings Request Sequence

The transfer settings request sequence sends the transfer settings for a specific disk drive to the DCA-2. Figure 3-15 shows a transfer settings request sequence.

Select Out
Slave in
Master Out
Sync In
Sync Out

X X X . X X

REQUEST
001.00

REQUEST
ACKNOWLEDGE
011.00

IDLE
000.00

DESELECT
010.00

A-9533
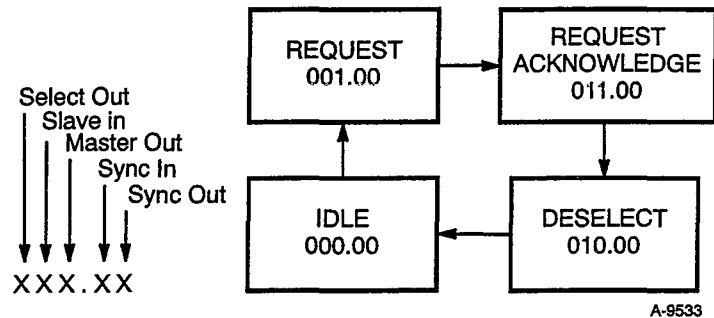
Figure 3-15. Transfer Settings Request and Interrupt Request Sequence

Before a transfer settings request sequence begins, the j and k registers in the 3DF option (refer to Figure 3-1) must be loaded with the transfer settings request (refer to Table 3-15).

1.   The sequencer transfers the transfer settings request (refer to Table 3-15) from the j register in the 3DF option to bus A and sets the Master Out signal to 1. Doing so puts the interface in the REQUEST state.

Table 3-15. Transfer Settings Request on Bus A

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	Disk drive address Bit 2^4 is the least significant bit			0	0	0	0

2.   The disk drive loads bus B with the transfer settings (refer to Table 3-16) and sets the Slave In signal to 1. Doing so puts the interface in the REQUEST ACKNOWLEDGE state.

Table 3-16. Transfer Settings on Bus B

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
0	0	1	0	0	1	1	0

3. The sequencer resets the Master Out signal to 0 to terminate the transfer settings request. Doing so puts the interface into the DESELECT state.

4. The disk drive acknowledges the termination and resets the Slave In signal to 0 to put the interface into the IDLE state.

Drive Interrupt Request Sequence

The drive interrupt request sequence transfers the interrupts for a specific disk drive to the DCA-2. Figure 3-15 shows a drive interrupt request sequence. Before a drive interrupt request sequence begins, the j and k registers in the 3DF option (refer to Figure 3-1) must be loaded with the drive interrupt request (refer to Table 3-17).

1. The sequencer transfers the drive interrupt request (refer to Table 3-17) from the j register in the 3DF option to bus A and sets the Master Out signal to 1. Doing so puts the interface in the REQUEST state.

Table 3-17. Drive Interrupt Request on Bus A

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	Disk drive address Bit 2^4 is the least significant bit			1	0	0	0

2. The disk drive loads bus B with the drive interrupts (refer to Table 3-18) and sets the Slave In signal to 1. Doing so puts the interface into the REQUEST ACKNOWLEDGE state.

Table 3-18. Drive Interrupts on Bus B

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
0	Busy status	Ready status	0	Priority select status	Status pending interrupt active	RPS interrupt active	Command complete interrupt

3. The sequencer resets the Master Out signal to 0 to terminate the drive interrupt request. Doing so puts the interface in the DESELECT state.

4. The disk drive acknowledges the termination and resets the Slave In signal to 0 to enter the IDLE state.

SECTION 4
DCA-2 CHANNEL FUNCTIONS

4 DCA-2 CHANNEL FUNCTIONS

Channel functions for the DCA-2 channel adapter load registers in the DCA-2 and auxiliary input/output processor (EIOP) with information for disk drive operations. The channel functions also transfer a sequencer starting address to initiate an IPI-2 bus state sequence. This section describes each channel function and sample disk drive routines.

Channel Function Descriptions

Table 4-1 briefly describes each DCA-2 channel function; the following subsections describe each function in more detail.

Table 4-1. Channel Functions

Function	EIOP Channel	Description
DCA2:0	Even or odd	Clears the channel busy and channel done flags
DCA2:1	Even	Transfers information from the DCA-2 to local memory
DCA2:1	Odd	Transfers information from local memory to the DCA-2
DCA2:2	Even or odd	Loads the cylinder register with ID parameter 0
DCA2:3	Even or odd	Loads the parameter register with ID parameter 1
DCA2:4	Even or odd	Loads the DCA-2 transfer counter with the transfer count
DCA2:5	Even or odd	Transfers information between the DCA-2 and buffer board
DCA2:6	Even or odd	Disables channel interrupts
DCA2:7	Even or odd	Enables channel interrupts
DCA2:10	Even or odd	Reads the channel local memory address register
DCA2:11	Even or odd	Reads the channel parcel counter
DCA2:12	Even or odd	Reads one of four status parcels
DCA2:13	Even or odd	Reads one of three status parcels
DCA2:14	Even or odd	Loads the channel local memory address register
DCA2:15	Even or odd	Loads the channel local memory parcel counter
DCA2:16	Even or odd	Loads the DCA-2 j and k registers with IPI-2 commands
DCA2:17	Even	Loads the sequencer mode select register
DCA2:17	Odd	Loads the bit stream head select register

DCA2:0 – Clear Channel Busy and Channel Done Flags

The DCA2:0 function resets the EIOP channel busy and channel done flags to 0 or performs a master clear of the channel. The value of the function modifier bits in the d field of the EIOP instruction or in the B register on the EIOP selects the operation to be performed (refer to Figure 4-1).

$$\text{|} \longleftarrow \quad d \text{ Field or B Register} \longrightarrow \text{|}$$

2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
M 2^3	M 2^2	M 2^1	M 2^0	C 2^4	C 2^3	C 2^2	C 2^1	C 2^0
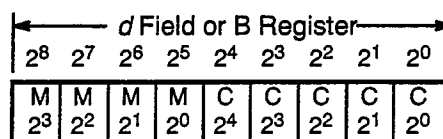
M = Function Modifier Bits
C = Channel Number

Figure 4-1. EIOP Instruction d Field or EIOP B Register

If the function modifier bits are set to 0, the function clears the channel busy and channel done flags. The flags cannot be sampled until 8 clock pulses have passed since the function was issued.

If function modifier bits 1, 2, and 3 are set to 1, this function performs a master clear of the DCA-2.

DCA2:1 – Local Memory Input and Output Transfer

The DCA2:1 function transfers the starting address for the sequencer and a value for the i register from the accumulator to the DCA-2. This function is used for information transfers between the DCA-2 and EIOP local memory.

Figure 4-2 shows the format of the sequencer starting address and i register value in the accumulator. When this function is executed, the DCA-2 loads the i register in the 3DF option with the i register value and loads the sequencer with the sequencer starting address.

$$\text{|} \longleftarrow \quad \text{Accumulator Contents} \longrightarrow \text{|}$$

2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
i 2^7	i 2^6	i 2^5	i 2^4	i 2^3	i 2^2	i 2^1	i 2^0	X x	SQ 2^6	SQ 2^5	SQ 2^4	SQ 2^3	SQ 2^2	SQ 2^1	SQ 2^0
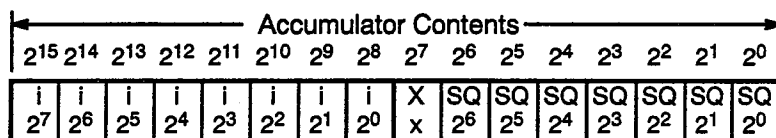
i = *i* Register Value   SQ = Sequencer Starting
X = Not Used   Address

Figure 4-2. DCA2:1 Sequencer Starting Address

After receiving the starting address, the sequencer starts an interlocked information transfer. If the DCA2:1 function is executed on the even EIOP channel, the sequencer transfers information from the DCA-2 to local memory. If the function is executed on the odd EIOP channel, the sequencer transfers information from local memory to the DCA-2. The value of the function modifier bits selects the type of information transferred: IPI-2 protocol, sequencer microcode, or the error-correction code (ECC) register contents (refer to Table 4-2).

Table 4-2. Function Modifier Bits

Modifier Bits				Description
2^3	2^2	2^1	2^0	
0	0	0	0	IPI-2 protocol transfer from local memory to the disk drive
0	0	0	1	IPI-2 status transfer from the disk drive to local memory
0	0	1	0	Sequencer microcode transfer from local memory to the DCA-2
0	0	1	1	Sequencer microcode transfer from the DCA-2 to local memory
0	1	0	1	ECC register transfer from the DCA-2 to local memory

IPI-2 Protocol Transfers

IPI-2 information is transferred from local memory to the disk drive in an interlocked transfer-to-disk sequence. For an example of this operation, refer to the "Seek Routine" subsection in this section.

IPI-2 status information is transferred from the drive to local memory in an interlocked transfer-from-disk sequence (refer to Figure 3-7). The i register value determines what type of status is transferred.

Sequencer Microcode Transfers

All transfers start at the first address of the sequencer and exchange 1,024 32-bit data words. After executing a transfer of sequencer microcode, the DCA2:0 function is executed. This function clears the DCA-2 control logic and direct memory access (DMA) references. The same channel numbering convention is used for the DCA2:0 function as for the DCA2:1 function.

Error-correction Code Register Transfer

During an ECC register transfer, the contents of all eight 4-byte ECC registers are transferred from the 3DH options to local memory.

DCA2:2 – Set ID Parameter 0

The DCA2:2 function transfers the cylinder address (ID parameter 0) from the accumulator to the cylinder register in the 3DG option of the DCA-2. Figure 4-3 shows the format of ID parameter 0 in the accumulator.

							Accumulator Contents								
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
C 2^{15}	C 2^{14}	C 2^{13}	C 2^{12}	C 2^{11}	C 2^{10}	C 2^9	C 2^8	C 2^7	C 2^6	C 2^5	C 2^4	C 2^3	C 2^2	C 2^1	C 2^0
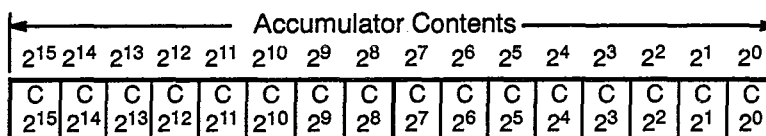
C = Cylinder Address (0 - 5062_8)

Figure 4-3. ID Parameter 0 Format

DCA2:3 – Set ID Parameter 1

The DCA2:3 function transfers the sector address, head address, and option bits (ID parameter 1) from the accumulator to the parameter register in the 3DG option of the DCA-2. Figure 4-4 shows the format of ID parameter 1 in the accumulator. Refer to the "Format and Flaw Management" disk drive sections of this manual for more information on the ID information bit descriptions (which include ID parameter 1).
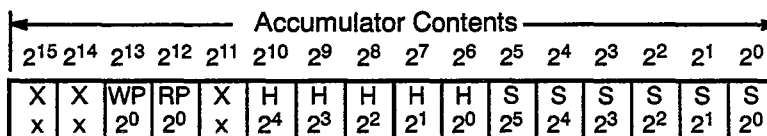
							Accumulator Contents								
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
X x	X x	WP 2^0	RP 2^0	X x	H 2^4	H 2^3	H 2^2	H 2^1	H 2^0	S 2^5	S 2^4	S 2^3	S 2^2	S 2^1	S 2^0

X = Not Used   RP = Read Protected
WP = Write Protected   H = Head Group Address
                              S = Sector Address

Figure 4-4. ID Parameter 1 Format

DCA2:4 – Set Transfer Count

The DCA2:4 function transfers the transfer count from the accumulator to the 3DI option in the DCA-2. The transfer count is the total number of parcels to be transferred between the DCA-2 and the disk drive (in octal). Figure 4-5 shows the format of the transfer count in the accumulator.

◄─────────────── Accumulator Contents ───────────────►															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
T 2^{15}	T 2^{14}	T 2^{13}	T 2^{12}	T 2^{11}	T 2^{10}	T 2^9	T 2^8	T 2^7	T 2^6	T 2^5	T 2^4	T 2^3	T 2^2	T 2^1	T 2^0
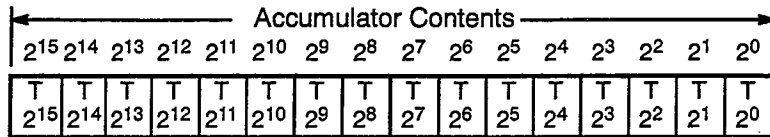
T = Transfer Count

Figure 4-5. Transfer Count Format

DCA2:5 – Starting Sequencer Address and *i* Register Value

The DCA2:5 function transfers the starting address for the sequencer and a value for the *i* register from the accumulator to the DCA-2. This function is used for information transfers between the DCA-2 and the EIOP buffer board.

Figure 4-6 shows the format of the sequencer starting address and *i* register value in the accumulator. When this function is executed, the DCA-2 loads the *i* register in the 3DF option with the *i* register value and loads the sequencer with the sequencer starting address.

◄─────────────── Accumulator Contents ───────────────►															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
i 2^7	i 2^6	i 2^5	i 2^4	i 2^3	i 2^2	i 2^1	i 2^0	X x	SQ 2^6	SQ 2^5	SQ 2^4	SQ 2^3	SQ 2^2	SQ 2^1	SQ 2^0
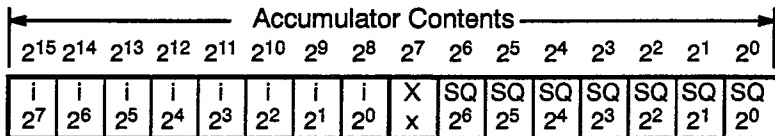
i = *i* Register Value   SQ = Sequencer Starting
X = Not Used   Address

Figure 4-6. DCA2:5 Sequencer Starting Address Format

After receiving the starting address, the sequencer starts an IPI-2 bus state sequence. For an example, refer to the "Write Sector Data Routine" subsection later in this section.

DCA2:6 – Disable Interrupt Enable

The DCA2:6 function sets the EIOP channel enable interrupts flag to 0. When the enable interrupts flag is 0, the channel does not acknowledge any interrupts it receives. This function does not change the states of the channel busy or channel done flags.

DCA2:7 – Enable Interrupt Enable

The DCA2:7 function sets the EIOP channel enable interrupts flag to 1. When the enable interrupts flag is 1, the channel acknowledges any interrupts it receives. This function does not change the states of the channel busy or channel done flags.

DCA2:10 – Read Local Memory Address

The DCA2:10 function transfers the current local memory address from the EIOP channel local memory address register to the accumulator. Figure 4-7 shows the format of the local memory address in the accumulator.

|◄─────────── Accumulator Contents ───────────►|
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
LM 2^{15}	LM 2^{14}	LM 2^{13}	LM 2^{12}	LM 2^{11}	LM 2^{10}	LM 2^9	LM 2^8	LM 2^7	LM 2^6	LM 2^5	LM 2^4	LM 2^3	LM 2^2	LM 2^1	LM 2^0
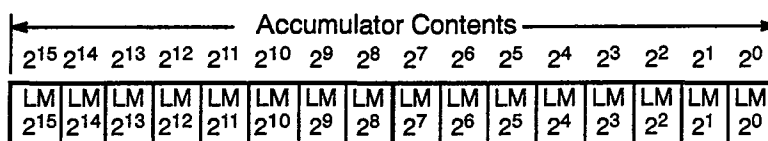
LM = Current Local Memory Address

Figure 4-7. Current Local Memory Address Format

DCA2:11 – Read Local Memory Parcel Count

The DCA2:11 function transfers the inverse of the EIOP channel parcel counter to the accumulator. To obtain the correct parcel count, the accumulator contents must be inverted. Figure 4-8 shows the format of the inverted parcel count in the accumulator.

|◄─────────── Accumulator Contents ───────────►|
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
IP 2^{15}	IP 2^{14}	IP 2^{13}	IP 2^{12}	IP 2^{11}	IP 2^{10}	IP 2^9	IP 2^8	IP 2^7	IP 2^6	IP 2^5	IP 2^4	IP 2^3	IP 2^2	IP 2^1	IP 2^0
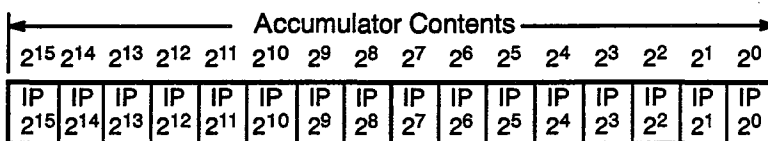
IP = Inverted Parcel Count from the 3DG Option

Figure 4-8. Inverted Parcel Count Format

DCA2:12 – Status Function 0

The DCA2:12 function transfers 1 of 5 status parcels from the DCA-2 to the accumulator. The initial value of the accumulator determines which status parcel is transferred. Figure 4-9 shows the format of the initial accumulator value.

```
|◄──────────────── Accumulator Contents ────────────────►|
 2¹⁵ 2¹⁴ 2¹³ 2¹² 2¹¹ 2¹⁰ 2⁹  2⁸  2⁷  2⁶  2⁵  2⁴  2³  2²  2¹  2⁰
```

X x	X x	X x	X x	X x	X x	X x	X x	X x	X x	X x	X x	X x	X x	ST 2¹	ST 2⁰

X = Not Used　　　　　　　　　　　　　ST = Status Select Bits
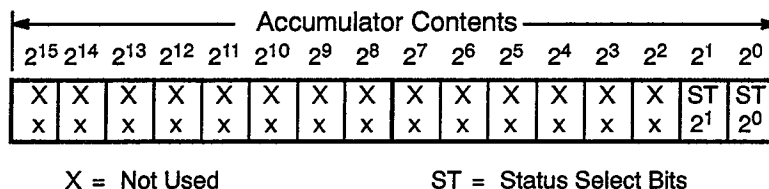
Figure 4-9. Status Select Format

Adapter Status

If the status select bits are both 0, the DCA-2 transfers the adapter status to the accumulator. Figure 4-10 shows the format of the adapter status in the accumulator. For more information on status, refer to the "DCA-2 Systems Status" section of this manual.

```
|◄──────────────── Accumulator Contents ────────────────►|
 2¹⁵ 2¹⁴ 2¹³ 2¹² 2¹¹ 2¹⁰ 2⁹  2⁸  2⁷  2⁶  2⁵  2⁴  2³  2²  2¹  2⁰
```

SP 2³	SP 2²	SP 2¹	SP 2⁰	V5 2⁰	V4 2⁰	DS 2⁰	SS 2⁰	CS 2⁷	CS 2⁶	CS 2⁵	CS 2⁴	CS 2³	CS 2²	CS 2¹	CS 2⁰

SP = Sequencer Parity Error　　　　DS = Double-bit Error
V5 = Voltage Fault +5 V　　　　　　SS = Single-bit Error
V4 = Voltage Fault −4.5 V　　　　　CS = Channel Adapter Status
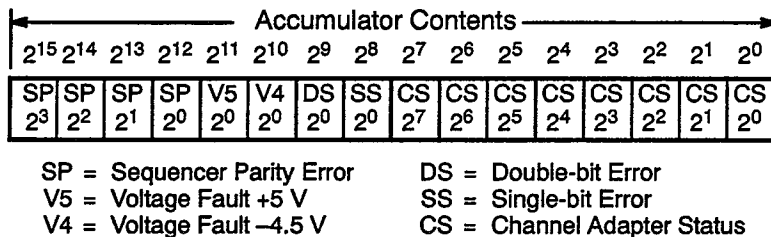
Figure 4-10. Adapter Status Format

6X Condition Bits

If the status select bits are both 0 and the sequencer is first given a starting address of 36₈ (using the DCA2:5 function), the DCA-2 transfers the 6X condition bits to the accumulator. Figure 4-11 shows the format of the 6X condition bits in the accumulator. For more information on status, refer to the "DCA-2 Systems Status" section of this manual.

```
|◄─────────────── Accumulator Contents ────────────────►|
| 2¹⁵ 2¹⁴ 2¹³ 2¹² 2¹¹ 2¹⁰ 2⁹  2⁸  2⁷  2⁶  2⁵  2⁴  2³  2²  2¹  2⁰ |
┌────┬───┬───┬───┬───┬───┬───┬───┬────┬────┬────┬────┬────┬────┬────┬────┐
│ X  │ X │ X │ X │ X │ X │ X │ X │6X  │6X  │6X  │6X  │6X  │6X  │6X  │6X  │
│ x  │ x │ x │ x │ x │ x │ x │ x │2⁷  │2⁶  │2⁵  │2⁴  │2³  │2²  │2¹  │2⁰  │
└────┴───┴───┴───┴───┴───┴───┴───┴────┴────┴────┴────┴────┴────┴────┴────┘
```
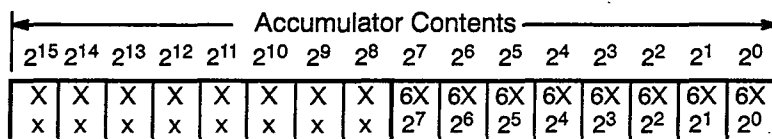
6X = 6X Condition Bits

Figure 4-11. 6X Condition Bits Format

7X Condition Bits

If the status select bits are both 0 and the sequencer is first given a
starting address of 37_8 (using the DCA2:5 function), the DCA-2 transfers
the 7X condition bits to the accumulator. Figure 4-12 shows the format
of the 7X condition bits in the accumulator. For more information on
status, refer to the "DCA-2 Systems Status" section of this manual.

```
|◄─────────────── Accumulator Contents ────────────────►|
| 2¹⁵ 2¹⁴ 2¹³ 2¹² 2¹¹ 2¹⁰ 2⁹  2⁸  2⁷  2⁶  2⁵  2⁴  2³  2²  2¹  2⁰ |
┌────┬───┬───┬───┬───┬───┬───┬───┬────┬────┬────┬────┬────┬────┬────┬────┐
│ X  │ X │ X │ X │ X │ X │ X │ X │7X  │7X  │7X  │7X  │7X  │7X  │7X  │7X  │
│ x  │ x │ x │ x │ x │ x │ x │ x │2⁷  │2⁶  │2⁵  │2⁴  │2³  │2²  │2¹  │2⁰  │
└────┴───┴───┴───┴───┴───┴───┴───┴────┴────┴────┴────┴────┴────┴────┴────┘
```
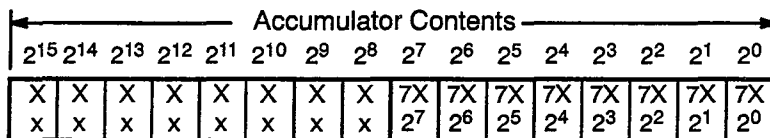
7X = 7X Condition Bits

Figure 4-12. 7X Condition Bits Format

Syndrome Status

If status select bit 2^1 is 0 and bit 2^0 is 1, the DCA-2 transfers the
syndrome status to the accumulator. Figure 4-13 shows the format of the
syndrome status in the accumulator. For more information on status,
refer to the "DCA-2 Systems Status" section of this manual.

```
|◄─────────────── Accumulator Contents ────────────────►|
| 2¹⁵ 2¹⁴ 2¹³ 2¹² 2¹¹ 2¹⁰ 2⁹  2⁸  2⁷  2⁶  2⁵  2⁴  2³  2²  2¹  2⁰ |
┌────┬────┬────┬────┬────┬────┬────┬────┬────┬────┬────┬────┬────┬────┬────┬────┐
│DC  │DC  │DC  │DC  │SC  │SC  │SC  │SC  │SY  │SY  │SY  │SY  │SY  │SY  │SY  │SY  │
│2³  │2²  │2¹  │2⁰  │2³  │2²  │2¹  │2⁰  │2⁷  │2⁶  │2⁵  │2⁴  │2³  │2²  │2¹  │2⁰  │
└────┴────┴────┴────┴────┴────┴────┴────┴────┴────┴────┴────┴────┴────┴────┴────┘
```
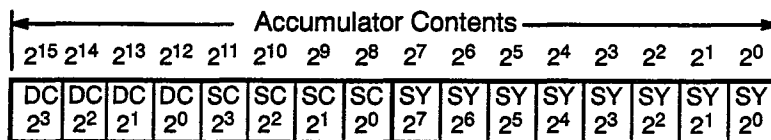
DC = Double-bit Error Count   SY = Syndrome Bits
SC = Single-bit Error Count

Figure 4-13. Syndrome Status Format

Transfer Count Status

If status select bit 2^1 is 1 and bit 2^0 is 0, the DCA-2 sends the transfer count status to the accumulator. The transfer count is the current value of the transfer counter in the 3DI option of the DCA-2. Figure 4-14 shows the format of the byte count status in the accumulator.

	Accumulator Contents														
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
T 2^{15}	T 2^{14}	T 2^{13}	T 2^{12}	T 2^{11}	T 2^{10}	T 2^9	T 2^8	T 2^7	T 2^6	T 2^5	T 2^4	T 2^3	T 2^2	T 2^1	T 2^0
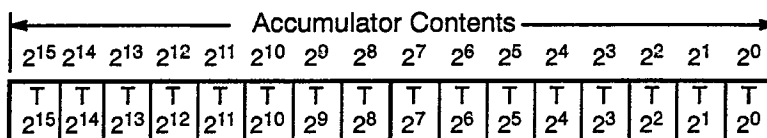
T = Transfer Count

Figure 4-14. Byte Count Status Format

Tag Status

If both status select bits are 1, the DCA-2 transfers the tag status to the accumulator. Figure 4-15 shows the format of the tag status in the accumulator. For more information on status, refer to the "DCA-2 Systems Status" section of this manual.

	Accumulator Contents														
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{11}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^1
X x	X x	X x	X x	X x	X x	X x	X x	X x	SO 2^0	MO 2^0	SL 2^0	X x	SI 2^0	SV 2^0	AI 2^0
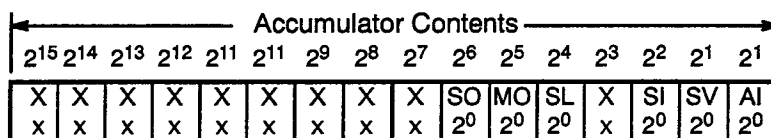
X = Not Used   SI = Sync In Signal
SO = Sync Out Signal   SV = Slave In Signal
MO = Master Out Signal   AI = Attention In Signal
SL = Select Out Signal

Figure 4-15. Tag Status Format

DCA2:13 – Status Function 1

The DCA2:13 function transfers 1 of 3 status parcels to the accumulator. The initial value of the accumulator determines which status parcel is transferred. Figure 4-9 shows the format of the initial accumulator value.

Drive Ending Status

If the status select bits are both 0, the DCA-2 transfers the drive ending status to the accumulator. Figure 4-16 shows the format of the drive ending status in the accumulator. For more information on status, refer to the "DCA-2 Systems Status" section of this manual.

								Accumulator Contents							
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
FS 2^7	FS 2^6	FS 2^5	FS 2^4	FS 2^3	FS 2^2	FS 2^1	FS 2^0	IS 2^7	IS 2^6	IS 2^5	IS 2^4	IS 2^3	IS 2^2	IS 2^1	IS 2^0
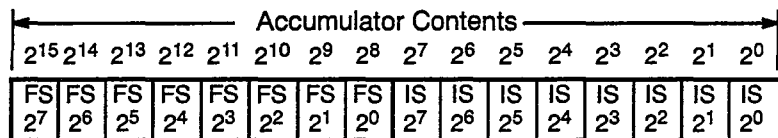
FS = Final Drive Ending Status   IS = Initial Drive Ending Status

Figure 4-16. Drive Ending Status Format

ID Parameter 0 Status

If status select bit 2^1 is 0 and bit 2^0 is 1, the DCA-2 transfers ID parameter 0 status to the accumulator. ID parameter 0 status is the current value stored in the cylinder register (ID parameter 0) of the 3DG option on the DCA-2. Refer again to Figure 4-3 for the format of ID parameter 0 in the accumulator.

ID Parameter 1 Status

If status select bit 2^1 is 1 and bit 2^0 is 0, the DCA-2 transfers ID parameter 1 status to the accumulator. ID parameter 1 status is the current value stored in the parameter register (ID parameter 1) of the 3DG option on the DCA-2. Refer again to Figure 4-4 for the format of ID parameter 1 in the accumulator.

DCA2:14 – Enter Local Memory Starting Address

The DCA2:14 function transfers the local memory starting address from the accumulator to the EIOP channel local memory address register. The local memory starting address is the EIOP local memory address that contains the first parcel of data to be transferred to the DCA-2, or the EIOP local memory address to which the DCA-2 transfers the first parcel of data. Figure 4-17 shows the format of local memory starting address in the accumulator.
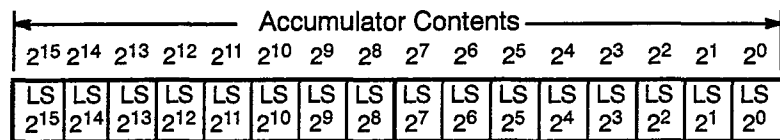
LS = Local Memory Starting Address

Figure 4-17. Local Memory Starting Address Format

During a data transfer, the local memory address register of the channel automatically increments once with each parcel transferred. Execute the DCA2:10 function to transfer the current value of the local memory address register of the channel to the accumulator.

DCA2:15 – Enter Local Memory Parcel Count

The DCA2:15 function transfers the local memory parcel count from the accumulator to the EIOP channel parcel counter. The parcel count is the number of parcels to be transferred between the EIOP local memory and the DCA-2. Figure 4-18 shows the format of the parcel count in the accumulator.
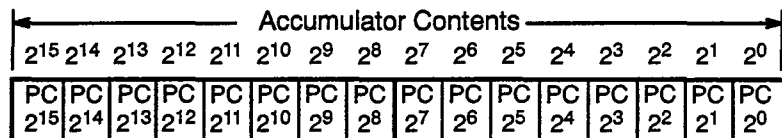
PC = Parcel Count

Figure 4-18. Parcel Count Format

During a data transfer, the channel parcel counter automatically decrements once for each parcel transferred. Execute the DCA2:11 function to transfer the inverted current value of the channel parcel counter to the accumulator.

DCA2:16 – Enter *j* and *k* Control Register Contents

The DCA2:16 function transfers values for the *j* and *k* registers from the accumulator to the 3DF option in the DCA-2. The *j* and *k* registers store bus control codes or IPI-2 command information bytes. Figure 4-19 shows the format of the *j* and *k* register values in the accumulator.

←				Accumulator Contents											→
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
k 2^7	k 2^6	k 2^5	k 2^4	k 2^3	k 2^2	k 2^1	k 2^0	j 2^7	j 2^6	j 2^5	j 2^4	j 2^3	j 2^2	j 2^1	j 2^0
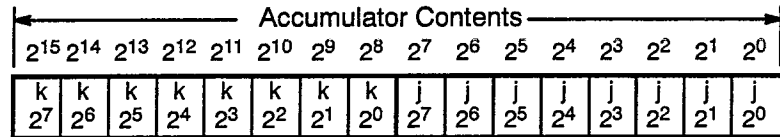
k = *k* Register Value   j = *j* Register Value

Figure 4-19. *j* and *k* Register Values

The sequencer on the DCA-2 controls when the *j* and *k* register contents are sent to the disk drive over bus A or over both bus A and bus B. For an example of this, refer to the "Write Sector Data Routine" subsection later in this section.

DCA2:17 – Enter Mode Select

The DCA2:17 function performs different operations when it is executed on the even channel than when it is executed on the odd channel. The differences are described below.

Even Channel

When executed on the even channel, the DCA2:17 function transfers sequencer mode bits from the accumulator to the sequencer on the DCA-2. The mode bits can be altered for any function sequence. Figure 4-20 shows the format of the sequencer mode bits in the accumulator.

$$\overset{\longleftarrow\qquad\text{Accumulator Contents}\qquad\longrightarrow}{2^{15}\;2^{14}\;2^{13}\;2^{12}\;2^{11}\;2^{10}\;2^{9}\;\;2^{8}\;\;2^{7}\;\;2^{6}\;\;2^{5}\;\;2^{4}\;\;2^{3}\;\;2^{2}\;\;2^{1}\;\;2^{0}}$$

X	X	X	X	X	X	X	X	M	M	M	M	M	M	M	M
x	x	x	x	x	x	x	x	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
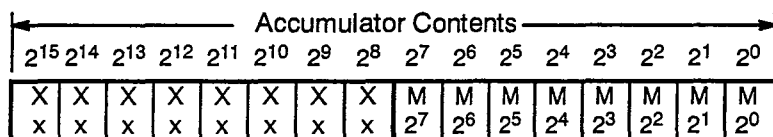
X = Not Used   M = Mode Bits for Sequencer

Figure 4-20. Mode Bits for the Sequencer

The sequencer mode bits abort an executing DCA-2 function, disable
ECC circuitry, disable ID compare circuitry, enable bit stream mode,
toggle the parity bit, or identify the specific disk drive type. Table 4-3
describes each sequencer mode bit.

Table 4-3. Sequencer Mode Bits

Bit	Name	Description
2^0	Abort	When set to 1, this bit signals the sequencer to terminate its operation. The channel Busy, Done, and Active signals are set to 0. (This bit is used only during an interrupt request (poll) sequence.
2^1	No ECC	When set to 1, this bit signals the sequencer to disable the ECC circuits.
2^2	Read ID	When set to 1, this bit signals the sequencer to transfer the first 4 parcels of ID information to the I/O buffer. This mode bit is used by ID verification utilities.
2^3	Read absolute	When set to 1, this bit signals the sequencer to read the data field without comparing the read ID field to the stored ID parameters.
2^4	Bit stream replacement	When set to 1, this bit signals the sequencer to enter the bit stream replacement mode. This mode is used with the DCA2:17 channel function on the odd channel.
2^5	Toggle parity	When set to 1, this bit signals the sequencer to toggle the parity bit on both buses for read or write operations.
2^6	2-head-parallel disk drive mode	When set to 1, this bit signals the sequencer that it is connected to a DD-62 or RD-62 drive.
2^7	Serial disk drive mode	When set to 1, this bit signals the sequencer that it is connected to a DD-61 drive.

Odd Channel

When executed on the odd channel, the DCA2:17 function transfers the lower byte of the accumulator to the bit stream mask register in the sequencer. Figure 4-21 shows the format of the bit stream select bits in the accumulator.

2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
X x	X x	X x	X x	X x	X x	X x	X x	B 2^7	B 2^6	B 2^5	B 2^4	B 2^3	B 2^2	B 2^1	B 2^0

← Accumulator Contents →
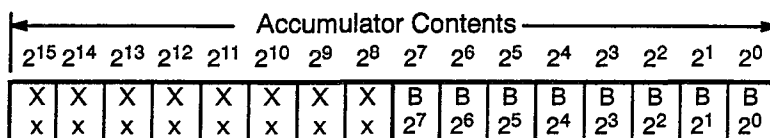
X = Not Used   B = Bit Stream Select Bits

Figure 4-21. Bit Stream Select Bits

NOTE: When not performing bit stream replacement, the bit stream number register contents must be set to 0's or data will be read incorrectly.

When a bit stream select bit is set to 1, the corresponding bits of bus A and bus B are replaced with a bit stream. The bit stream is calculated by summing the parity stream data with the other seven data streams. This enables data recovery to occur whenever a problem exists under a single head of the DD-60.

Sample Disk Drive Function Routines

Unlike previous Cray Research, Inc. channel adapter functions, DCA-2 channel functions do not correspond one-to-one with disk drive functions. For example, executing the DCA2:2 function (Set ID Parameter 0) does not cause the disk drive to seek to the cylinder address loaded in the accumulator.

Disk drive functions such as select, seek, or read operations are done with a function routine that may contain several channel functions. Generally, function routines consist of the following procedures:

1. Clearing the channel busy and channel done flags for both EIOP channels.

2. Loading the EIOP local memory or EIOP buffer board with information for the disk drive operation.

3. Loading the registers in the DCA-2 with the values needed for the disk drive operation.

4. Loading the counter registers in the DCA-2 and EIOP channel with the number of parcels to be transferred.

5. Loading the sequencer with the starting address of the IPI-2 sequence for the disk drive operation.

The following subsections describe sample disk drive function routines. The actual routines and control codes used by the drivers, recovery routines, diagnostics, and utilities may not be the same as the following routines.

Select Unit Routine

The select unit routine logically connects the IOS to a disk drive. The routine consists of the following steps:

1. The DCA2:0 function is executed on both channels to clear the EIOP channel busy and channel done flags.

2. The accumulator is loaded with the disk drive address (refer to Table 3-2). Figure 4-22 shows an example of a disk drive address in the accumulator. This example selects the disk drive with the logical address 5. Refer to the "DD-60 Hardware Description" section of this manual for more information on the logical address.

2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
k	k	k	k	k	k	k	k	j	j	j	j	j	j	j	j
0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0

Accumulator Contents

k = *k* Register Value   j = *j* Register Value
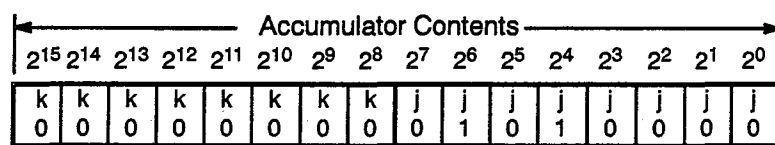
Figure 4-22. Disk Drive Address for Logical Address 5

3. The DCA2:16 function is executed. This function transfers the disk drive address to the *j* register in the 3DF option on the DCA-2.

4. The accumulator is loaded with 13_8, the starting address of the select disk drive sequence (refer to Figure 4-23).

|←─────────── Accumulator Contents ───────────→|
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
i	i	i	i	i	i	i	i	X	SQ	SQ	SQ	SQ	SQ	SQ	SQ
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1
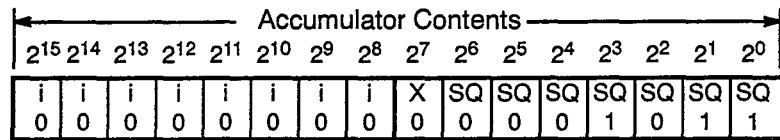
i = *i* Register Value   SQ = Sequencer Starting
X = Not Used   Address

Figure 4-23. Sequencer Starting Address for Select Disk Drive Sequence

5.   The DCA2:5 function is executed. This function transfers the
      starting address to the sequencer. After receiving the address, the
      sequencer performs a select disk drive sequence (refer to
      Figure 3-4). When the sequence is finished, the IPI-2 interface is
      in the SLAVE ACKNOWLEDGE state.

The following optional steps verify that the disk drive was successfully
selected.

6.   The accumulator is loaded with 00_8, the status select bits for status
      01 (refer to Figure 4-24).

|←─────────── Accumulator Contents ───────────→|
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	ST	ST
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
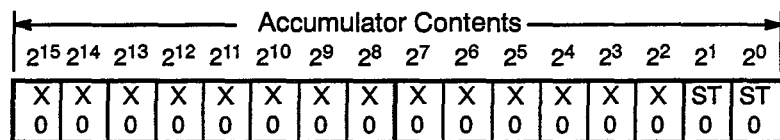
X = Not Used   ST = Status Select Bits

Figure 4-24. Status Select for Status 01

7.   The DCA2:13 function is executed. This function transfers the
      drive ending status to the accumulator. The ending status for a
      select disk drive sequence is the drive select response (refer to
      Table 3-3). Figure 4-25 shows the drive select response for logical
      address 5 in the accumulator.

|←─────────── Accumulator Contents ───────────→|
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
ES	ES	ES	ES	ES	ES	ES	ES	X	X	X	X	X	X	X	X
0	0	1	0	0	0	0	0	x	x	x	x	x	x	x	x
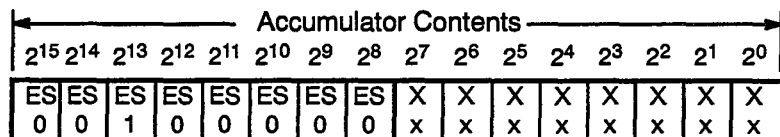
X = Not Used   ES = Ending Status

Figure 4-25. Drive Select Response in the Accumulator

Seek Routine

The seek routine moves the heads to a desired location over the platters. The seek routine consists of the following steps:

1. A select unit routine is performed.

2. Two sequential local memory addresses are loaded with data: the first with 0's and the second with the cylinder address (ID parameter 0). Refer to Figure 4-3 for the format of the cylinder address.

3. The DCA2:0 function is executed on both EIOP channels to clear the channel busy and channel done flags.

4. The accumulator is loaded with 02_8, the transfer count for a seek routine (refer to Figure 4-26).

	Accumulator Contents														
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
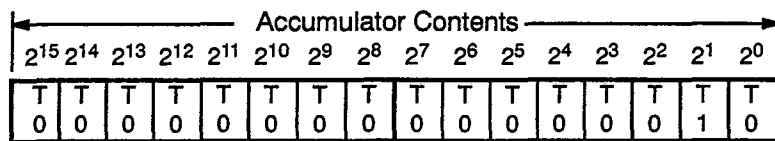
T = Transfer Count

Figure 4-26. Transfer Count for a Seek Routine

5. The DCA2:4 function is executed. This function transfers the transfer count from the accumulator to the transfer counter in the 3DI option.

6. The accumulator is loaded with the local memory starting address. The local memory starting address is the address that contains the cylinder address you entered in Step 2.

7. The DCA2:14 function is executed. This function transfers the local memory starting address to the EIOP channel local memory address register.

8. The accumulator is loaded with 02_8, the local memory parcel count for a seek routine (refer to Figure 4-27).

Accumulator Contents

2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 1	PC 0
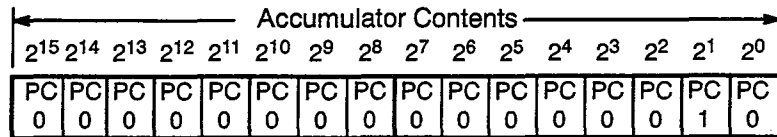
PC = Parcel Count

Figure 4-27. Parcel Count for a Seek Routine

9. The DCA2:15 function is executed. This function transfers the parcel count to the EIOP channel's parcel count register.

10. Bits 2^0 through 2^8 of the accumulator are loaded with the load cylinder bus control code (refer to Figure 4-28).

Accumulator Contents

2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
k 0	k 0	k 0	k 0	k 0	k 0	k 0	k 0	j 0	j 0	j 0	j 0	j 0	j 1	j 0	j 0
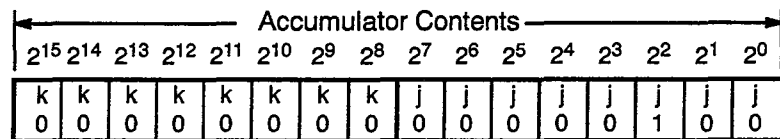
k = *k* Register Value   j = *j* Register Value

Figure 4-28. Load Cylinder Bus Control Code

11. The DCA2:16 function is executed. This function transfers the bus control codes to the *j* and *k* registers in the 3DF option on the DCA-2.

12. The accumulator is loaded with 04_8, the sequencer starting address for a command load (refer to Figure 4-29).

Accumulator Contents

2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
i 0	i 0	i 0	i 0	i 0	i 0	i 0	i 0	X 0	SQ 0	SQ 0	SQ 0	SQ 0	SQ 1	SQ 0	SQ 0
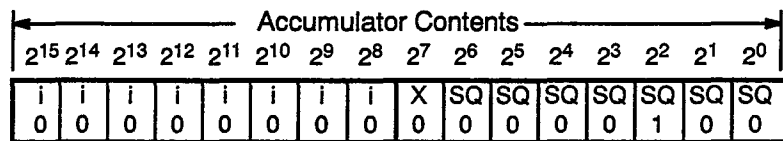
i = *i* Register Value   SQ = Sequencer Starting
X = Not Used   Address

Figure 4-29. Sequencer Starting Address for Command Load

13.   The DCA2:1 function is executed on the odd channel. This signals
       the sequencer to perform a bus control sequence (refer to
       Figure 3-5), an interlocked transfer-to-disk sequence (refer to
       Figure 3-6), and an ending status sequence (refer to Figure 3-10).
       When the sequences are finished, the IPI-2 interface is in the
       SLAVE ACKNOWLEDGE state.

Load Position Routine

The load position routine moves the heads to a desired location over the
platters and selects the desired head. The load position routine consists
of the following steps:

1.   A select unit routine is performed.

2.   Nine (11_8) sequential local memory addresses are loaded with the
      rotational position sensing (RPS) parameter. Refer to Table 4-4 for
      the format of the RPS parameter.

Table 4-4. RPS Parameter Parcel Descriptions

Parcels	Description
0 through 1_8	Cylinder address (ID parameter 0)
2	Head address
3	RPS target sector address
4	RPS pulse width extension
5 through 6_8	RPS pulse width
7 through 10_8	RPS pulse width skew

3.   The DCA2:0 function is executed on both channels to clear the
      channel's busy and done flags.

4.   The accumulator is loaded with 11_8, the transfer count for a load
      position routine (refer to Figure 4-30).

						Accumulator Contents									
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
T 0	T 0	T 0	T 0	T 0	T 0	T 0	T 0	T 0	T 0	T 0	T 0	T 1	T 0	T 0	T 1

T = Transfer Count

Figure 4-30. Transfer Count for a Load Position Routine

5. The DCA2:4 function is executed. This function transfers the transfer count from the accumulator to the transfer counter in the 3DI option.

6. The accumulator is loaded with the local memory starting address. The local memory starting address is the address that contains the parameters entered in Step 2.

7. The DCA2:14 function is executed. This function transfers the local memory starting address to the EIOP channel local memory address register.

8. The accumulator is loaded with 11_8, the local memory parcel count for a load position routine (refer to Figure 4-31).

←						Accumulator Contents								→	
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 0	PC 1	PC 0	PC 0	PC 1
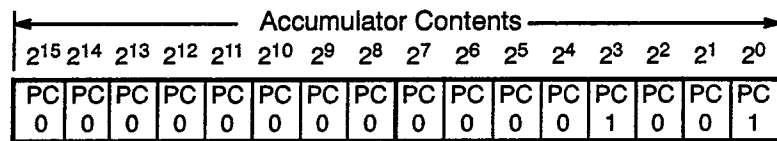
PC = Parcel Count

Figure 4-31. Parcel Count for a Load Position Routine

9. The DCA2:15 function is executed. This function transfers the parcel count to the EIOP channel's parcel count register.

10. Bits 2^0 through 2^8 of the accumulator are loaded with the load position bus control code (refer to Figure 4-32).

←					Accumulator Contents									→	
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
k 0	k 0	k 0	k 0	k 0	k 0	k 0	k 0	j 0	j 0	j 0	j 0	j 0	j 1	j 1	j 1
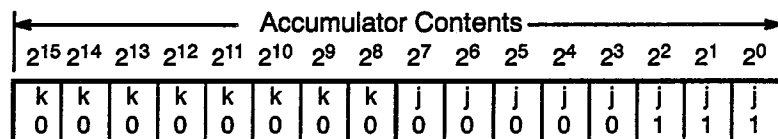
k = k Register Value   j = j Register Value

Figure 4-32. Load Position Bus Control Code

11. The DCA2:16 function is executed. This function transfers the bus control codes to the j and k registers in the 3DF option on the DCA-2.

12. The accumulator is loaded with 04_8, the sequencer starting address for a command load (refer again to Figure 4-29).

13. The DCA2:1 function is executed on the odd channel. This signals the sequencer to perform a bus control sequence (refer to Figure 3-5), an interlocked transfer-to-disk sequence (refer to Figure 3-6), and an ending status sequence (refer to Figure 3-10). When the sequences are finished, the IPI-2 interface is in the SLAVE ACKNOWLEDGE state.

Poll Routine

The poll routine requests all disk drives connected to the channel that have certain interrupts pending to report back to the DCA-2. Before the interrupt request (poll) sequence begins, the IPI-2 interface must be in the IDLE state. The following example is written assuming that the interface is in the SLAVE ACKNOWLEDGE state. The poll routine consists of the following steps:

1. The DCA2:0 function is executed on both channels to clear the channel busy and channel done flags.

2. The accumulator is loaded with 0's.

3. The DCA2:16 function is executed. This function transmits the 0's to the j and k registers of the 3DF option in the DCA-2.

4. The accumulator is loaded with 14_8, the sequencer starting address for a deselect sequence (refer to Figure 4-33).

								Accumulator Contents							
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
i	i	i	i	i	i	i	i	X	SQ	SQ	SQ	SQ	SQ	SQ	SQ
0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

i = *i* Register Value   SQ = Sequencer Starting
X = Not Used   Address
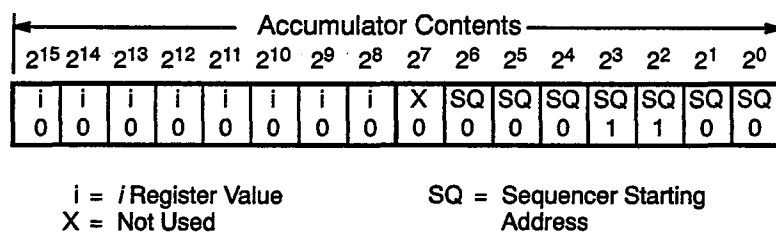
Figure 4-33. Sequencer Starting Address for a Deselect Sequence

5. The DCA2:5 function is executed. This function signals the sequencer to perform a deselect sequence (refer to Figure 3-11). When the sequence is finished, the IPI-2 interface is in the IDLE state.

6. The accumulator is loaded with the interrupt request (refer to Table 3-11). Figure 4-34 shows the interrupt request for an RPS interrupt. This request checks whether a disk drive has completed a load position routine.

							Accumulator Contents								
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
k	k	k	k	k	k	k	k	j	j	j	j	j	j	j	j
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
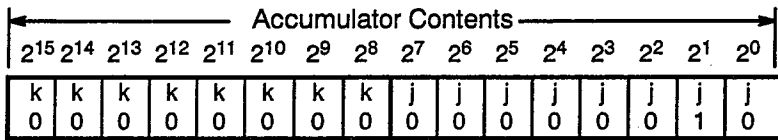
k = *k* Register Value   j = *j* Register Value

Figure 4-34. Interrupt Request in the Accumulator

7. The DCA2:16 function is executed. This function transfers the
    interrupt request to the *j* register in the 3DF option of the DCA-2.

8. The accumulator is loaded with a bit-mapped drive address and the
    sequencer starting address (10_8) of an interrupt request (poll)
    sequence. Figure 4-35 shows the bit-mapped drive address for
    logical address 5 and the starting sequencer address for a poll
    sequence.

							Accumulator Contents								
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
i	i	i	i	i	i	i	i	X	SQ	SQ	SQ	SQ	SQ	SQ	SQ
0	0	1	0	0	0	0	0	x	0	0	0	1	0	0	0
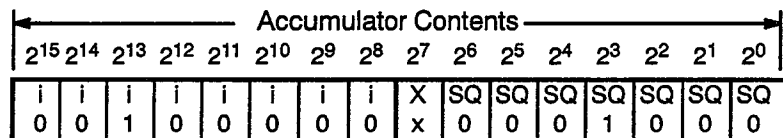
i = *i* Register Value   SQ = Sequencer Starting
X = Not Used   Address

Figure 4-35. Sequencer Starting Address for a Poll Sequence

9. The DCA2:5 function is executed. This function signals the
    sequencer to perform an interrupt request (poll) sequence (refer to
    Figure 3-12). When the disk drive with the logical address
    selected in the *i* register responds, the sequencer returns the IPI-2
    interface to the IDLE state.

Write Sector Data Routine

The write sector data routine writes a sector of data to the disk drive and
consists of the following steps:

1. A select unit routine is performed.

2. A load position routine is performed.

3. The accumulator is loaded with the cylinder address, ID parameter
    0 (refer again to Figure 4-3).

4. The DCA2:2 function is executed. This function transfers the cylinder address to the cylinder register in the 3DG option of the DCA-2.

5. The accumulator is loaded with the head and sector address, ID parameter 1 (refer to Figure 4-4).

6. The DCA2:3 function is executed. This function transfers the head and sector address to the parameter register in the 3DG option of the DCA-2.

7. The accumulator is loaded with the transfer count. The transfer count for a write sector data routine is the total number of parcels in the ID field, ID error-correction code (ECC) field, data field, defect swallow field, and data ECC field. Figure 4-36 shows the transfer count (20154_8) for a DD-60 disk drive.

	Accumulator Contents														
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
T 0	T 0	T 1	T 0	T 0	T 0	T 0	T 0	T 0	T 1	T 1	T 0	T 1	T 1	T 0	T 0

T = Transfer Count in Octal

Figure 4-36. Transfer Count for a DD-60 Disk Drive

8. The DCA2:4 function is executed. This function transfers the transfer count from the accumulator to the transfer counter in the 3DI option.

9. The accumulator is loaded with the read header at target and write field bus control commands. The read header at target bus control command is loaded into the *j* register and the write field bus control command into the *k* register (refer to Figure 4-37).

	Accumulator Contents														
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
k 1	k 0	k 0	k 0	k 0	k 0	k 0	k 1	j 1	j 1	j 0	j 0	j 1	j 1	j 0	j 0

k = *k* Register Value   j = *j* Register Value

Figure 4-37. Read Header at Target and Write Field Bus Control Codes

10.   The DCA2:16 function is executed. This function transfers the bus
       control codes to the j and k registers in the 3DF option of the
       DCA-2.

11.   The accumulator is loaded with 24_8, the sequencer starting address
       for a write data sequence (refer to Figure 4-38).

Figure 4-38. Sequencer Starting Address for a Write Data Sequence

12.   The DCA2:5 function is executed. This function signals the
       sequencer to perform a write data sequence, which contains several
       IPI-2 sequences:

       a.   The sequencer performs a bus control sequence (refer again
             to Figure 3-5). During this sequence, the sequencer transfers
             the contents of the j register (read header at target bus control
             code) to the disk drive.

       b.   The sequencer performs a noninterlocked transfer-from-disk
             sequence (refer again to Figure 3-9). During this sequence,
             the DCA-2 compares the ID field read from the disk drive to
             the ID parameters stored in the 3DG option.

       c.   The sequencer performs an ending status sequence (refer to
             Figure 3-10). During this sequence the DCA-2 and disk
             drive exchange statuses.

       d.   The sequencer performs another bus control sequence (refer
             to Figure 3-5). During this sequence, the sequencer transfers
             the contents of the k register (write data field bus control
             code) to the disk drive.

       e.   The sequencer performs a noninterlocked transfer-to-disk
             sequence (refer to Figure 3-8). During this sequence, the
             DCA-2 receives a sector of data from the EIOP buffer board
             and transfers it to the disk drive.

       f.   The sequencer performs another ending status sequence
             (refer to Figure 3-10). When finished, the IPI-2 interface is
             in the SLAVE ACKNOWLEDGE state.

Read Sector Data Routine

The read sector data routine reads a sector of data from the disk drive and consists of the following steps:

1. A select unit routine is performed.

2. A load position routine is performed.

3. The accumulator is loaded with the cylinder address, ID parameter 0. Refer to Figure 4-3.

4. The DCA2:2 function is executed. This function transfers the cylinder address to the cylinder register in the 3DG option of the DCA-2.

5. The accumulator is loaded with the head and sector address, ID parameter 1. Refer to Figure 4-4.

6. The DCA2:3 function is executed. This function transfers the head and sector address to the parameter register in the 3DG option of the DCA-2.

7. The accumulator is loaded with the transfer count. The transfer count for a read sector data routine is the total number of parcels in the ID field, ID ECC field, data field, defect swallow field, and data ECC field. Figure 4-36 shows the transfer count (20154_8) for a DD-60 disk drive.

8. The DCA2:4 function is executed. This function transfers the transfer count from the accumulator to the transfer counter in the 3DI option.

9. The accumulator is loaded with the read header at target (j register contents) and read field (k register contents) bus control commands. Refer to Figure 4-39.

					Accumulator Contents										
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
k 1	k 1	k 0	k 0	k 0	k 0	k 0	k 1	j 1	j 1	j 0	j 0	j 1	j 1	j 0	j 0

k = *k* Register Value   j = *j* Register Value

Figure 4-39. Read Header at Target and Read Field Bus Control Codes

10. The DCA2:16 function is executed. This function transfers the bus control codes to the j and k registers in the 3DF option of the DCA-2.

11. The accumulator is loaded with the sequencer starting address (20_8) for a read data sequence (refer to Figure 4-40).
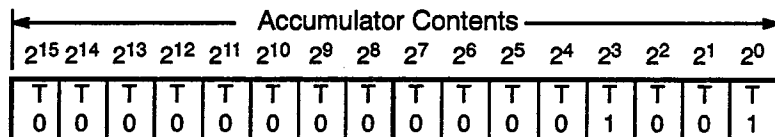
← Accumulator Contents →															
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
i	i	i	i	i	i	i	i	X	SQ	SQ	SQ	SQ	SQ	SQ	SQ
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
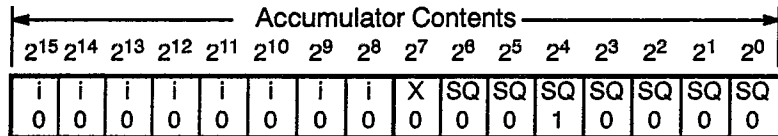
i = i Register Value   SQ = Sequencer Starting
X = Not Used   Address

Figure 4-40. Sequencer Starting Address for a Read Data Sequence

12. The DCA2:5 function is executed. This function signals the sequencer to perform a read data sequence, which contains several IPI-2 sequences.

   a. The sequencer performs a bus control sequence (refer to Figure 3-5). During this sequence, the sequencer transfers the contents of the j register (read header at target bus control code) to the disk drive.

   b. The sequencer performs a noninterlocked transfer-from-disk sequence (refer to Figure 3-9). During this sequence, the DCA-2 compares the ID field read from the disk drive to the ID parameters stored in the 3DG option.

   c. The sequencer performs an ending status sequence (refer to Figure 3-10). During this sequence, the DCA-2 and disk drive exchange statuses.

   d. The sequencer performs another bus control sequence (refer to Figure 3-5). During this sequence, the sequencer transfers the contents of the k register (read data field bus control code) to the disk drive.

   e. The sequencer performs another noninterlocked transfer-from-disk sequence (refer to Figure 3-9). During this sequence, the DCA-2 receives a sector of data from the disk drive and transfers it to the EIOP buffer board.

   f. The sequencer performs another ending status sequence (refer to Figure 3-10). When finished, the IPI-2 interface is in the SLAVE ACKNOWLEDGE state.

SECTION 5
DD-60 HARDWARE DESCRIPTION
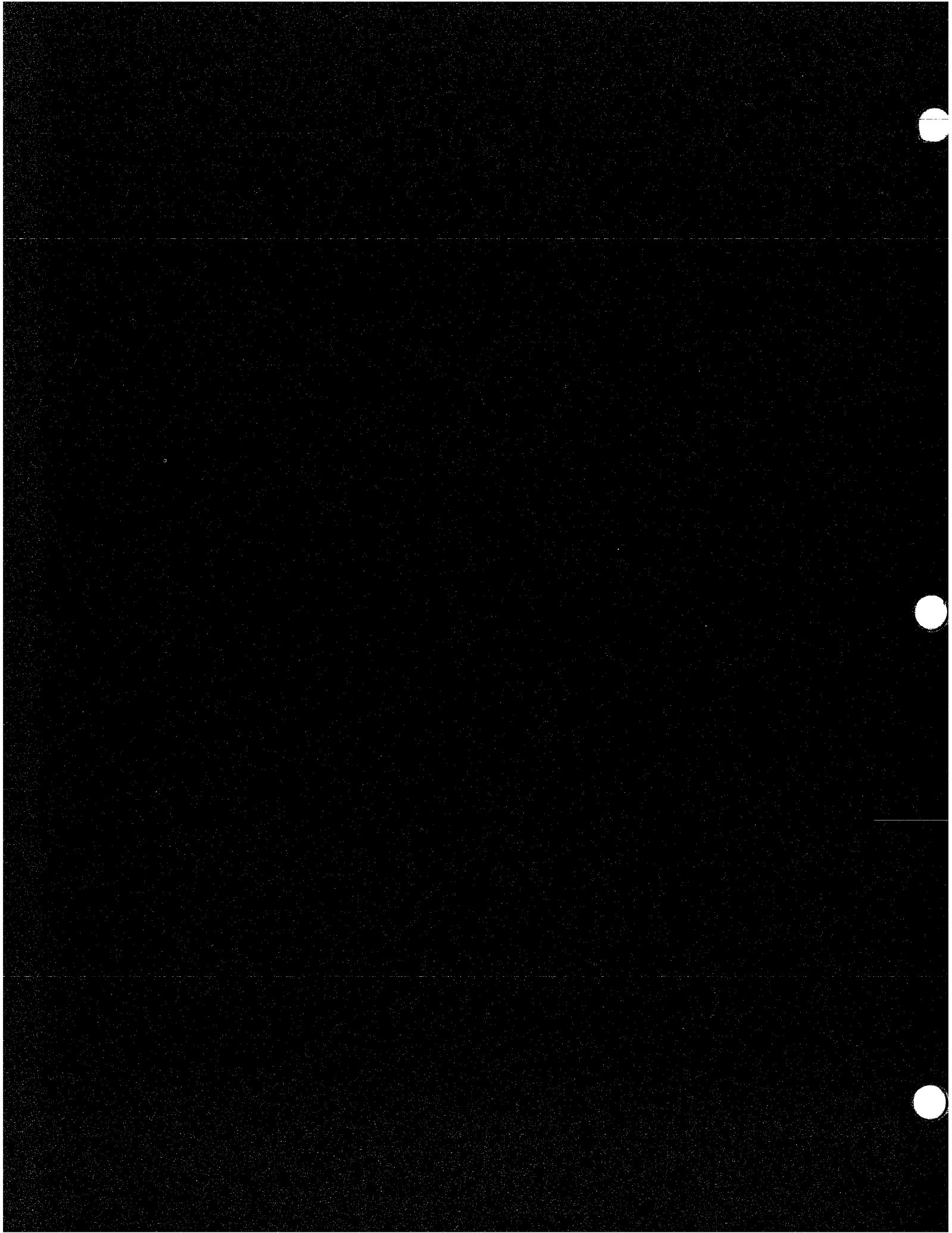
5 DD-60 HARDWARE DESCRIPTION

The DD-60 contains hardware that displays status, changes the disk format, and tests the internal circuitry. The hardware includes the rear panel, power supply, and internal components. DCA-2 applications require the DD-60 to operate in a 9-head parallel mode while DCA-3 applications require an 8-head parallel mode. Hardware differences between the two modes are referred to in this section.

Rear Panel

A set of dual-in-line package (DIP) switches and LED displays is located on the rear panel of the DD-60. The DIP switches set the format of the disk drive, and the displays show I/O status. Figure 5-1 shows the locations of the DIP switches, displays, and synchronization connection.

A-9534
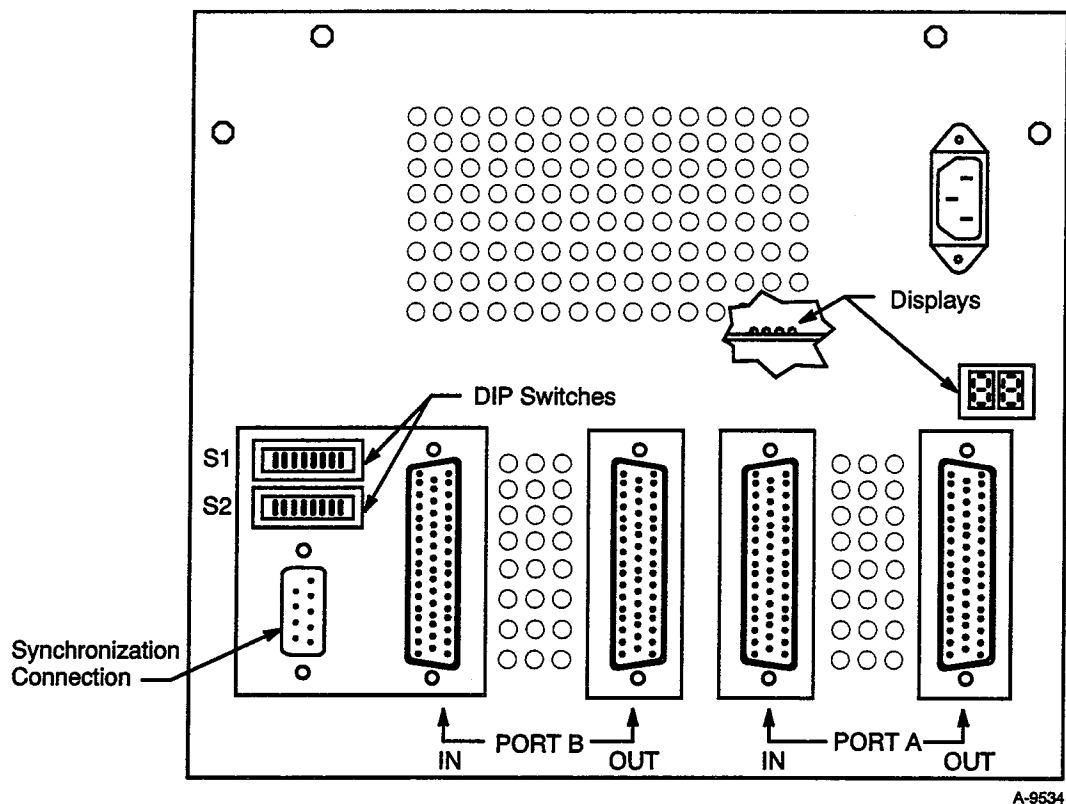
Figure 5-1. Rear Panel of a DD-60 Disk Drive

Upper DIP Switches (S1)

The upper DIP switches set the address and modes of disk drive operation. The S1 switch settings are the same for DCA-2 and DCA-3 applications. These switch settings are shown in Figure 5-2 below.

DCA-2 and DCA-3 Application Settings

A-9535
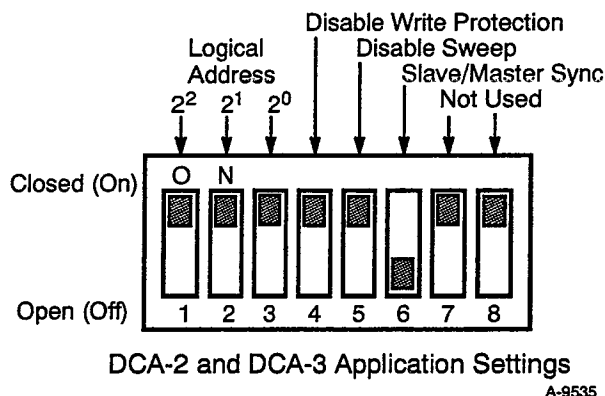
Figure 5-2. Upper DIP Switches (S1) on the DD-60

Disable Write Protection

Set this switch to the closed (On) position to disable write protection mode. If the write protection is enabled, data cannot be written to the disk drive.

Disable Sweep

Set this switch to the closed (On) position to disable the drive's internal sweep cycle activity.

Slave/Master Sync

Set this synchronization switch to the open (Off) position to allow the software to assign the disk drive as a master or slave. If this switch is in the closed (On) position, the disk drive is the master and cannot be reassigned through software commands. Spindle synchronization is used for DCA-3 applications only.

Logical Address

Set these switches to the appropriate logical address of the disk drive (refer to Table 5-1). Each disk drive in a daisy chain or alternate-path configuration must have a unique logical address (refer to Figure 5-3).

If a maintenance panel is not connected, the DD-60 reads the logical
address setting of the S1 DIP switches once during power up. If the
address setting is changed, the DD-60 must be power cycled to recognize
the new address.

Table 5-1. Upper DIP Switch Settings for Logical Address

Logical Address	Switch 1	Switch 2	Switch 3
0	Closed (On)	Closed (On)	Closed (On)
1	Closed (On)	Closed (On)	Open (Off)
2	Closed (On)	Open (Off)	Closed (On)
3	Closed (On)	Open (Off)	Open (Off)
4	Open (Off)	Closed (On)	Closed (On)
5	Open (Off)	Closed (On)	Open (Off)
6	Open (Off)	Open (Off)	Closed (On)
7	Open (Off)	Open (Off)	Open (Off)
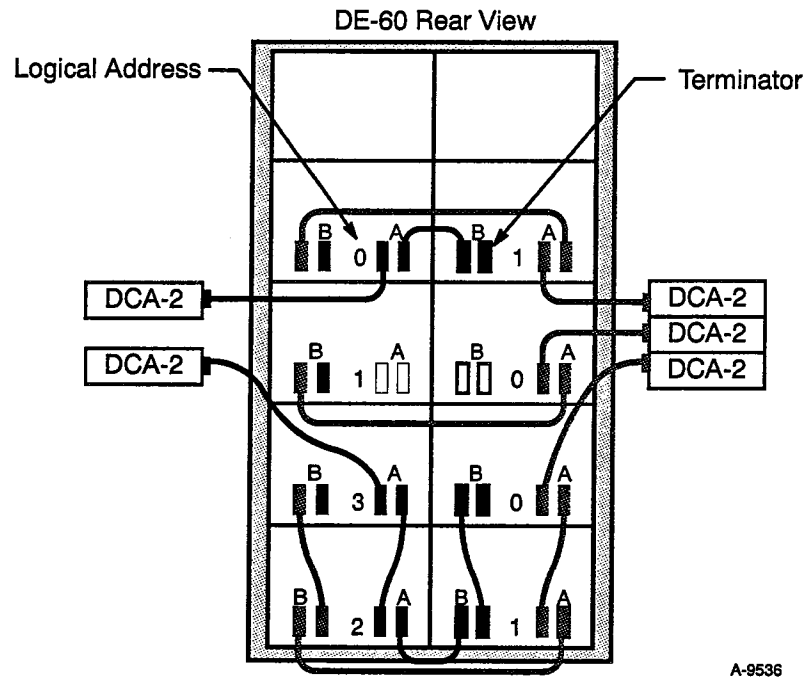
Figure 5-3. Logical Addresses of DCA-2 Drives in a DE-60

If the maintenance panel is connected to the disk drive, the maintenance panel overrides the logical address set on the DIP switches. Refer to the "Maintenance Procedures" section for information on setting the logical address using the maintenance panel.

Lower DIP Switches (S2)

The lower DIP switches change the modes of disk drive operation. The DCA-2 and DCA-3 channel adapters require different switch settings on the DD-60. These switch settings are shown in Figure 5-4 and are described in the following subsections.

CAUTION

The DD-60 S2 DIP switches must be set according to the type of channel adapter being used. Switch settings for DCA-2 applications will not work if the DD-60 is connected to a DCA-3 as an array.
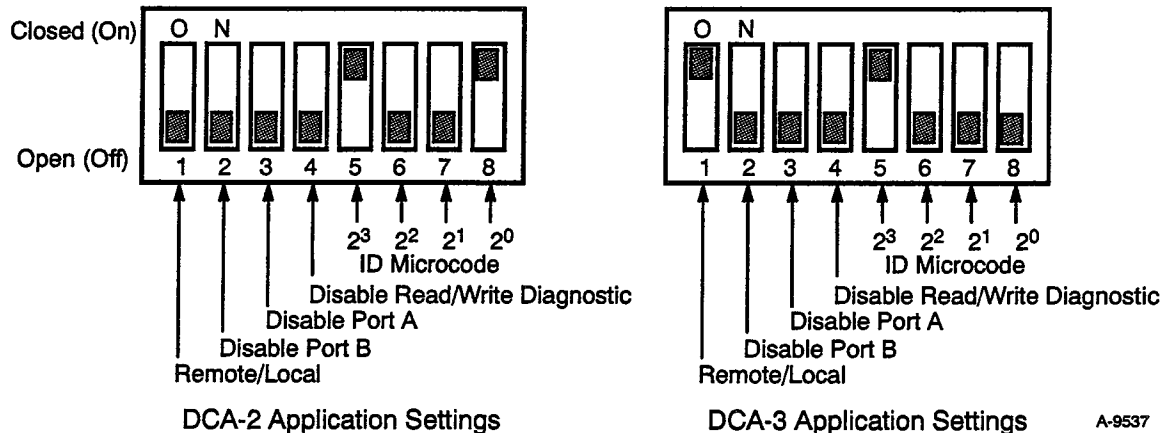
Figure 5-4. Lower DIP Switches (S2) on the DD-60

Remote/Local

Set this switch to the open (Off) position to enable local mode for DCA-2 applications. In local mode, the disk drive spins up when the START/STOP switch is pressed on the maintenance panel. If the disk drive does not have a maintenance panel and it is in local mode, it spins up when DC power is applied.

Set this switch to the closed (On) position, to enable remote mode for DCA-3 applications. In remote mode, the disk drive spins up after it receives a spin-up command from a host controller. Before remote spin-up can occur, you must ensure that the START button is pressed and the DE-60 cabinet breaker and spindle power supply switches are in the ON position. Refer to the spin-up and spin-down procedures in the "Maintenance Procedures" section of this manual.

Disable Port B

Set this switch to the open (Off) position to enable port B.

Disable Port A

Set this switch to the open (Off) position to enable port A.

Disable Read/Write Diagnostic

Set this switch to the open (Off) position to enable the internal diagnostic write/read operation on the IPI diagnostic cylinder (5061_8).

ID Microcode

Make sure the ID microcode switches are properly set before powering on the disk drive. If the ID microcode switch settings are changed, the DD-60 will overwrite the CRI format specification when power is applied to the drive. Reloading the CRI format specification to the drive will be necessary in these cases. The ID microcode switches enable or disable internal disk drive circuitry. This circuitry enables or disables the disk drive internal parity checking and establishes eight-head parallel (DCA-3 applications) or nine-head parallel (DCA-2 applications) information transfers.

CAUTION

Make sure the ID microcode switches are set to the correct positions before powering on the DD-60. If the switches are not correct and power is applied, the format specification in the DD-60 is overwritten.

Rear Panel Displays

The rear panel contains two displays: a two-digit LED display and a four-LED display. Figure 5-5 shows the two displays.
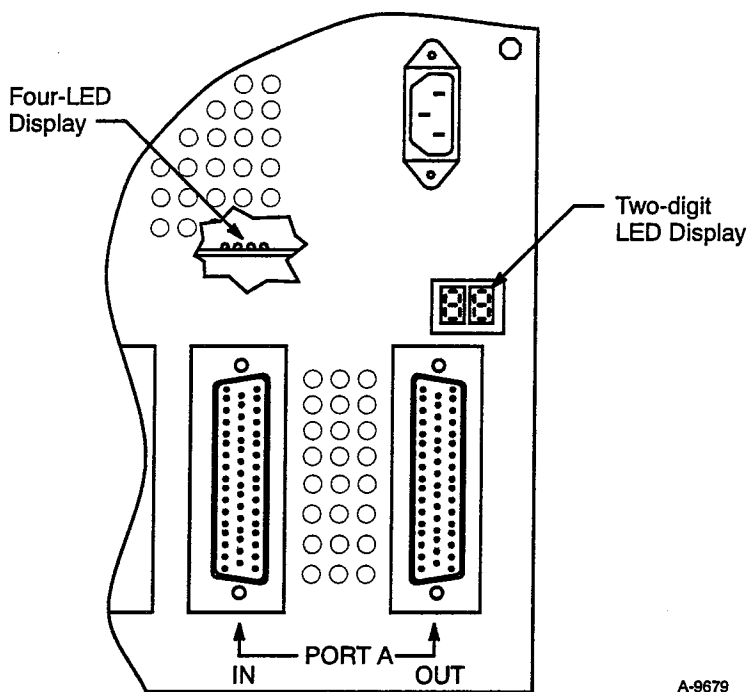
Figure 5-5. DD-60 Rear Panel Displays

Two-digit LED Display

If the maintenance panel is not connected to the disk drive, use the two-digit LED display to view status. During disk drive operations, the two-digit LED display shows the current I/O status.

The I/O status is generated by the I/O microprocessor unit (I/O MPU) in the DD-60. The I/O MPU controls the signal lines that connect the DD-60 to the DCA-2.

Under normal disk drive operating conditions, the rear panel display should show the 01_{16} or 09_{16} I/O status code. For more information on the rear panel display I/O status codes, refer to "DD-60 Rear Panel Display I/O Status" in Section 12 of this manual.

Four-LED Display

The four-LED display, which is connected to the control board in the DD-60, displays the current condition of the power supply and DD-60 (refer to Figure 5-6).
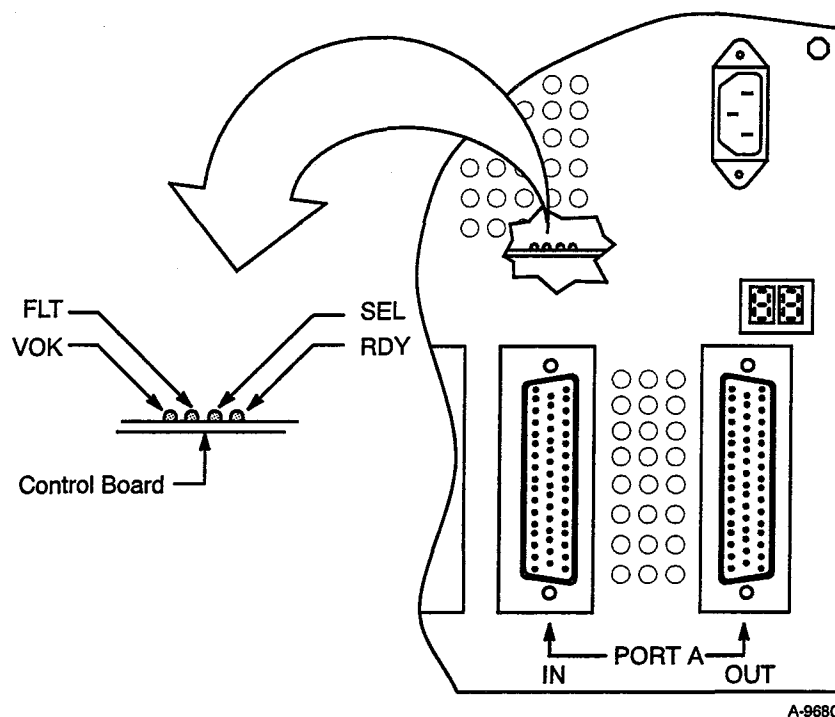
Figure 5-6. Four-LED Display in the DD-60

Table 5-2 describes each of the four LEDs in the display.

Table 5-2. Four-LED Display Description

Name	Description
VOK	The voltage (VOK) LED illuminates if the +5-V power supply is working correctly.
FLT	The drive fault (FLT) LED illuminates if a fault condition is detected by the disk drive.
SEL	The drive selected (SEL) LED illuminates when the DD-60 acknowledges a select command.
RDY	The drive ready (RDY) LED illuminates when the platters are up to speed, the heads are positioned over the first cylinder, and the disk drive is ready for use. The RDY LED also flashes during spin-up and spin-down sequences.

Internal Components

DD-60 disk drives are Sabre VI nine-head parallel (9HP) disk drives. The Sabre VI 9HP disk drive contains three groups of internal components: the circuit boards, head disk assembly (HDA) module, and the power supply.

Circuit Boards

The DD-60 contains up to eight circuit boards of four types: a control board, read/write boards, an IPI logic board, and an I/O transceiver board. A terminator board is substituted for the channel 8 read/write board in DCA-3 applications. Refer to Figure 5-7 for the locations of the DD-60 components.

A-11154
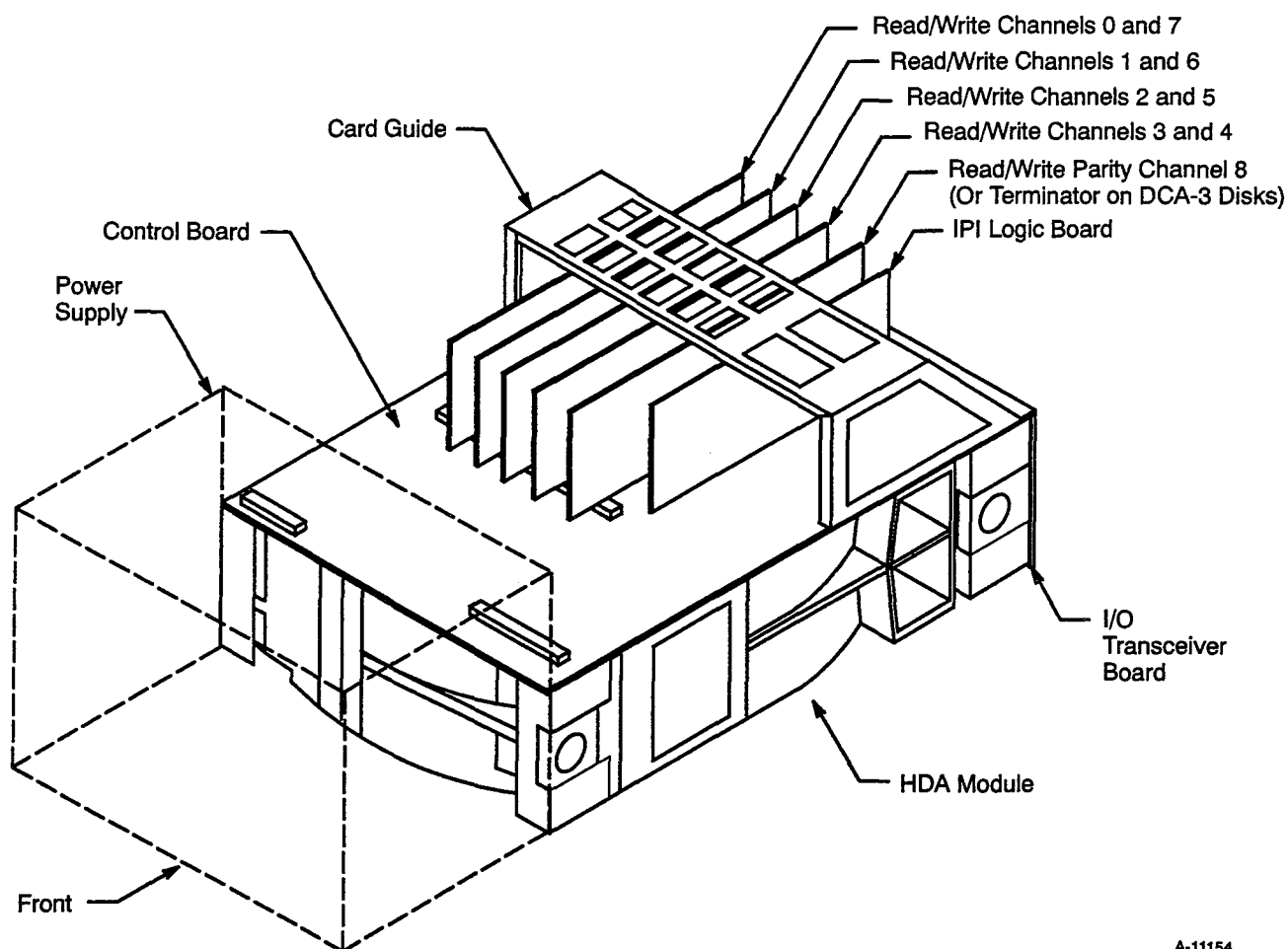
Figure 5-7. DD-60 Component Locations

Read/Write Boards

Four dual-channel read/write boards transfer data from the IPI logic board to the HDA module. They are mounted to the top of the control board as shown in Figure 5-7. A fifth single-channel read/write board (channel 8) is used to transfer parity information in DD–60s connected to a DCA-2 channel adapter. DD-60s connected to a DCA-3 must have a terminator board (CRI part 01785200) installed in place of the channel 8 read/write board. Refer to the Maintenance Procedures section later in this manual for details on converting a DD-60 for DCA-3 use.

Figure 5-8 shows which physical heads are connected to each of the read/write channels. These channel numbers correspond to the bits within each byte of read/write data transferred; channel 8 is the odd parity bit.
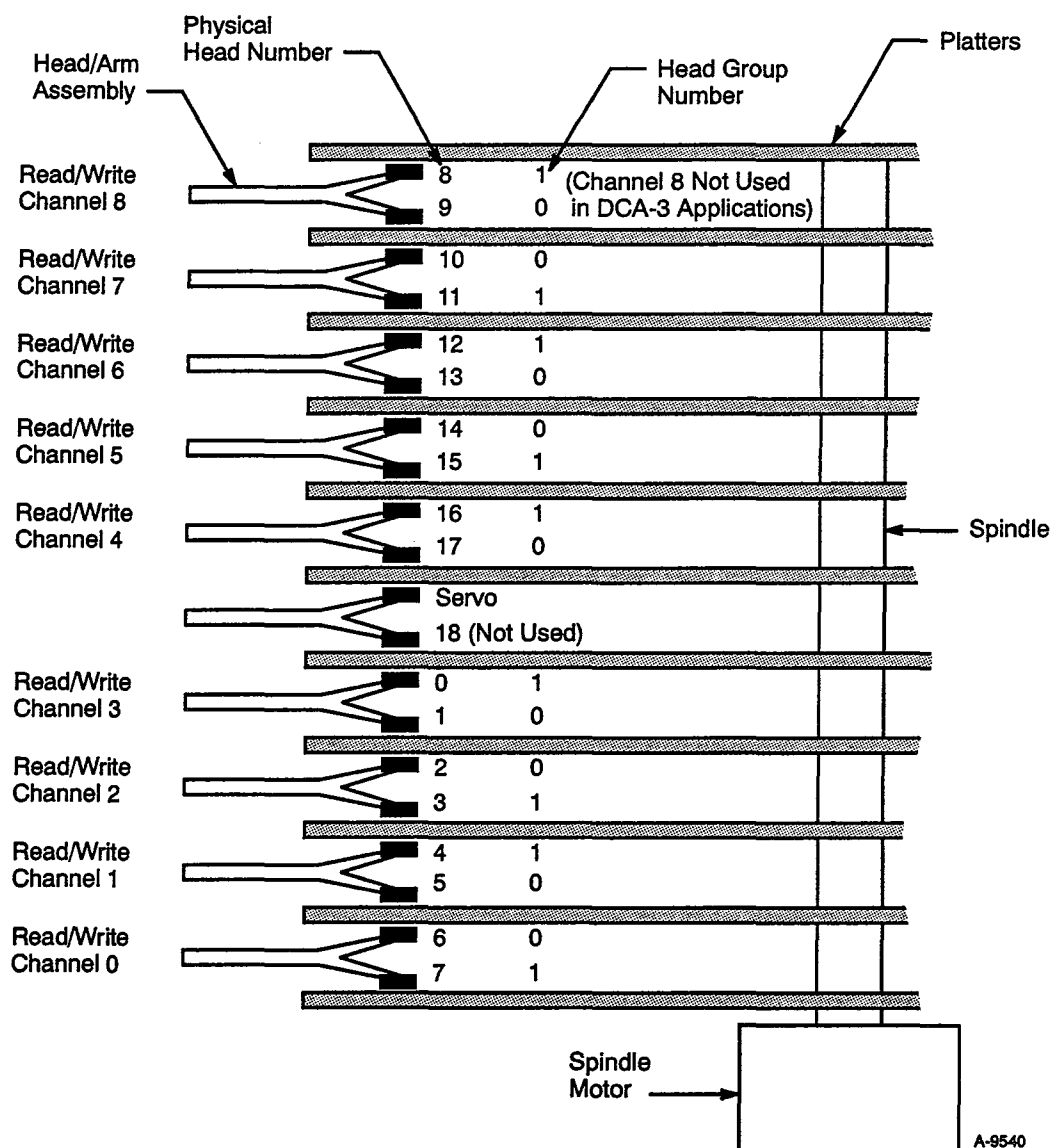
Figure 5-8. DD-60 Physical Head Locations in the HDA

IPI Logic Board

The IPI logic board translates IPI-2 commands from the DCA-2. This board also holds the drive format specification and drive serial number in a nonvolatile RAM. You may need to reload this information if you replace the IPI logic board. Refer again to Figure 5-7 for the location of the IPI logic board in the DD-60.

Control Board

The control board directly controls most disk drive functions. It is mounted to the top of the HDA module and connects to the HDA module through pin connectors under the control board.

I/O Transceiver Board

The I/O transceiver board is mounted to the back of the DD-60. It contains the rear panel DIP switches and LED display. It also contains external cable connectors.

Power Supply

The power supply converts 115 Vac or 230 Vac into DC voltages. All components of the disk drive operate on DC voltage. These voltages are +5 Vdc, –5 Vdc, +12 Vdc, –12 Vdc, and +24 Vdc.

HDA Module

The HDA is a sealed module that contains the circuitry and hardware used to store information, including platters, heads, an actuator, a spindle, and a spindle motor.

Platters

The HDA module contains 11 platters that rotate at 3,600 revolutions per minute. Nine of the platters contain two thin-film media surfaces for reading or writing data. The top and bottom platter contain only one thin-film media data surface (refer again to Figure 5-8).

Heads

The heads transfer information to or from the platter media surface. One head transfers servo information while the other heads transfer data. Physical head 18 is not used (refer again to Figure 5-8).

Actuator

The actuator positions the heads over any of the 2,611 cylinders on the platter surface. The DD-60 has a balanced rotary actuator so the heads move in an arc over the platters.

Spindle

The spindle attaches to the center of all the platters and holds them in place. It is directly connected to the spindle motor (refer again to Figure 5-8).

Spindle Motor

The spindle motor is a 3-phase motor that rotates at 3,600 revolutions per minute. It is directly connected to the spindle and platter assembly (refer again to Figure 5-8). The spindle motor is controlled by a dedicated motor microprocessor unit (MPU) on the control board. This dedicated MPU controls the motor via 3-phases of pulse-width modulated signals.

Maintenance Panel

The maintenance panel can be connected to the front of the power supply and enables the user to set the logical address, examine statuses, view error logs, and run diagnostics. For more information on the maintenance panel, refer to the "Maintenance Procedures" section later in this manual.

SECTION 6
DD-60 FORMAT AND FLAW MANAGEMENT

6 DD-60 FORMAT AND FLAW MANAGEMENT

This section covers format specifications and flaw management properties of the DD-60, including cylinder format, sector format, media flaws, and flaw maps and tables.

Cylinder Format

The DD-60 has 2,611 cylinders, which include data cylinders, diagnostic cylinders, and a flaw table cylinder. Table 6-1 shows the addresses of these cylinders in decimal and octal.

Table 6-1. DD-60 Cylinder Map

Cylinder Type	Addresses
Data cylinders	0 - 2,607 0 - 5057_8
Diagnostic scratch cylinder	2,608 5060_8
IPI diagnostic cylinder	2,609 5061_8
User flaw table cylinder	2,610 (odd sectors) 5062_8 (odd sectors)
Factory flaw table cylinder	2,610 (even sectors) 5062_8 (even sectors)

Data cylinders store system data. Do not write data patterns to these cylinders unless the customer data is offloaded to an alternate location.

The diagnostic scratch cylinder is reserved for DD-60 diagnostics. Use this cylinder to read and write data patterns without destroying system data.

The IPI diagnostic cylinder is reserved for the disk drive. The internal read/write diagnostics use this cylinder during spin-up of the DD-60.

The flaw table cylinder contains both the factory flaw table and the user flaw table. For more information on flaw tables, refer to the "Flaw Maps and Tables" subsection later in this section.

Sector Format

After receiving information from the channel adapter (DCA-2 or DCA-3), the DD-60 stores the information in eight physical sectors (one under each head in a head group). Figure 6-1 shows the format of a physical sector under one head in the head group.
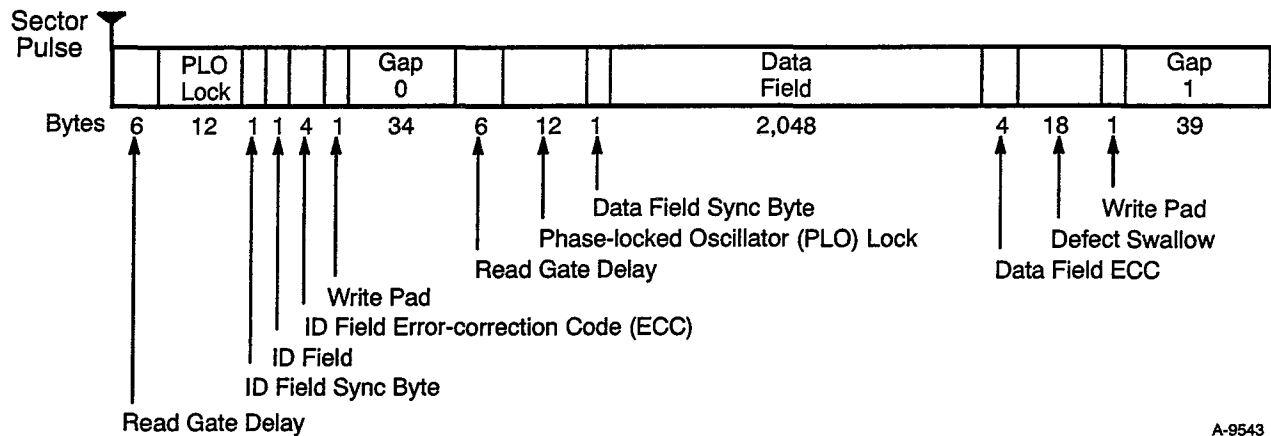
Figure 6-1. DD-60 Physical Sector Format

Each sector contains five field types: timing, data, error correction code (ECC), defect swallow, and ID fields. Table 6-2 shows the relation between the size of a physical field and the logical size of the information from the combined eight heads.

Table 6-2. DD-60 Sector Field Sizes

Sector Field	Physical Size in Bytes	Logical Size in Bytes
Read gate delay	6.0	N/A
PLO lock	12.0	N/A
ID field sync byte	1.0	N/A
ID	1.0	8.0
ID field ECC	4.0	32.0
Write pad	1.0	N/A
Gap 0	34.0	N/A
Data field sync byte	1.0	N/A
Data	2,048.0	16,384.0
Data field ECC	4.0	32.0
Defect swallow	18.0	144.0
Gap 1	39.0	N/A

Timing Fields

Timing fields create time delays for synchronization of the timing circuits during read or write operations. These fields are read gate delay, phased-locked oscillator (PLO) lock, sync bytes, write pad, gap 0, and gap 1.

The following example describes how a timing field is used: gap 0 provides a time delay for the DD-60 to interpret the next command (a read or write data field). Without this delay, the information stored in the data field would be sent to the channel adapter immediately after the ID information.

Data Field

The data field contains 2,048 bytes of system data. The DD-60 distributes 16,384 bytes of data received from the channel adapter into the 8 physical data fields.

ECC Fields

The ECC fields contain ECC generated by the channel adapter during a write data operation. Each physical sector contains 4 bytes of ECC for the ID field in that sector and 4 bytes of ECC for the data field in that sector. The channel adapter uses this information during a read operation.

During a read data operation, the channel adapter reads the data or ID field and generates a new ECC for that field from each physical sector. The channel adapter then compares the new ECCs to the information read from the sector ECC fields.

If the ID or data field ECCs do not match the generated ECCs, the channel adapter signals the EIOP that an error occurred. If the error occurred in the data field, the channel adapter detects the bits that are incorrect and corrects them.

Defect Swallow

The defect swallow enables the data field to expand if a hideable flaw is placed in the sector. For more information on defect swallow and hideable flaws, refer to the "Media Flaws" subsection in this section.

ID Field

The DD-60 stores 8 bytes of logical ID information among the 8 physical ID fields. The ID information contains the logical sector address and media flaw information (refer to Figure 6-2). Table 6-3 describes each bit of the ID information.

	Byte 0								Byte 1						
X x	X x	X x	X x	X x	X x	X x	U 2^8	U 2^7	U 2^6	U 2^5	U 2^4	U 2^3	U 2^2	U 2^1	U 2^0

	Byte 2								Byte 3						
C 2^{15}	C 2^{14}	C 2^{13}	C 2^{12}	C 2^{11}	C 2^{10}	C 2^9	C 2^8	C 2^7	C 2^6	C 2^5	C 2^4	C 2^3	C 2^2	C 2^1	C 2^0

	Byte 4								Byte 5						
X x	X x	WP 0	RP 0	X x	H 2^4	H 2^3	H 2^2	H 2^1	H 2^0	S 2^5	S 2^4	S 2^3	S 2^2	S 2^1	S 2^0

	Byte 6								Byte 7						
VF 2^0	UH 2^0	ID 2^0	D 2^{12}	D 2^{11}	D 2^{10}	D 2^9	D 2^8	D 2^7	D 2^6	D 2^5	D 2^4	D 2^3	D 2^2	D 2^1	D 2^0

A-9542
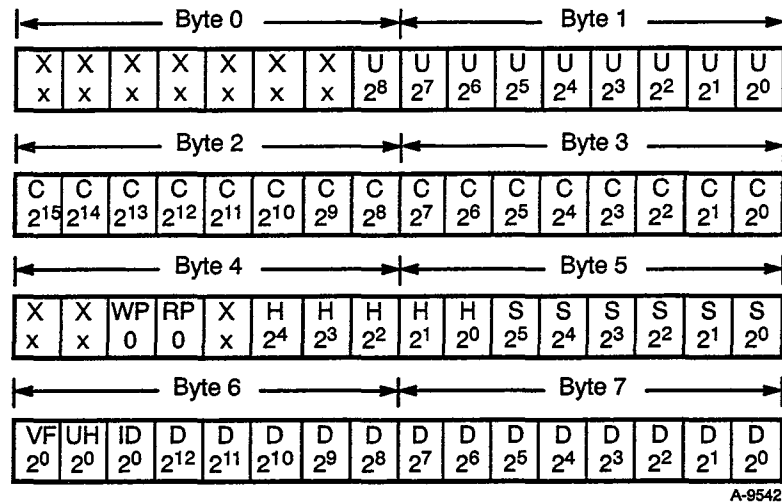
Figure 6-2. DD-60 Logical ID Information

Table 6-3. DD-60 Logical ID Information Description

Bit Symbol	Name	Description
X	Not used	This bit is not used.
U	Defective head	When set to 1, this bit indicates the physical head (head in head group) under which a media flaw exists.
C	Cylinder address	These bits contain the cylinder address of the data (0 – 5062$_8$).
WP	Write protect (must be set to 0)	When set to 1, this bit indicates that data cannot be written to the sector unless this bit is also set in parameter register 1 (currently unused).
RP	Read protect (must be set to 0)	When set to 1, this bit indicates that data cannot be read from the sector unless this bit is also set in parameter register 1 (currently unused).
H	Head address	These bits contain the logical head address (0 – 1).
S	Sector address	These bits contain the sector address of the data (0 – 26$_8$).
VF	Valid flaw	When set to 1, this bit indicates that the flaw in the sector is a known hideable flaw.
UH	Unhideable flaw	When set to 1, this bit indicates that the flaw in the sector is unhideable.
ID	ID field flaw	When set to 1, this bit indicates that the ID field contains an unhideable flaw.
D	Defect parameter	These bits contain the defect parameter. If the sector does not have a media flaw in the data field, the defect parameter is 4004$_8$.

The ID information is transferred between the disk drive and channel adapter in four 16-bit parcels using both bus A and bus B. For example, the first parcel transferred contains byte 0 and byte 1 of the logical ID information.

The entire logical ID information does not exist under an individual head in the head group. Each physical ID field contains 8 bits of the information. Bit 2^0 of each byte transferred is stored under head 0 of the head group. Bit 2^1 of each byte transferred is stored under head 1 of the head group, and so on.

During a write ID field (format) operation, the DD-60 distributes the logical ID information to the 8 ID fields. After the 8 bytes of information are written to the disk drive, each physical ID field contains 8 bits of the information. Figure 6-3 shows the ID fields for the 8 heads in a head group. On DD-60s connected to DCA-2 channel adapters, odd parity information is written under a ninth head.

|← ———— 1 Byte ———— →|

U 2^8	U 2^0	C 2^8	C 2^0	H 2^2	S 2^0	D 2^8	D 2^0	ID Field under Head 0 of Head Group
X x	U 2^1	C 2^9	C 2^1	H 2^3	S 2^1	D 2^9	D 2^1	ID Field under Head 1 of Head Group
X x	U 2^2	C 2^{10}	C 2^2	H 2^4	S 2^2	D 2^{10}	D 2^2	ID Field under Head 2 of Head Group
X x	U 2^3	C 2^{11}	C 2^3	X x	S 2^3	D 2^{11}	D 2^3	ID Field under Head 3 of Head Group
X x	U 2^4	C 2^{12}	C 2^4	RP 0	S 2^4	X 2^x	D 2^4	ID Field under Head 4 of Head Group
X x	U 2^5	C 2^{13}	C 2^5	WP 0	S 2^5	ID 2^0	D 2^5	ID Field under Head 5 of Head Group
X x	U 2^6	C 2^{14}	C 2^6	X x	H 2^0	UH 2^0	D 2^6	ID Field under Head 6 of Head Group
X x	U 2^7	C 2^{15}	C 2^7	X x	H 2^1	VF 2^0	D 2^7	ID Field under Head 7 of Head Group

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Figure 6-3. DD-60 Physical ID Fields

Media Flaws

A media flaw is a defect on the surface of a platter that does not allow the disk drive to read or write information correctly. Flaws are grouped into two categories: hideable flaws and unhideable flaws.

Hideable Flaws

A hideable flaw is a media defect in the data field that can be effectively covered by an 18-byte defect pad. The channel adapter creates this defect pad when it writes data to the disk drive.

Hiding a Media Flaw

When a media defect is found during surface analysis or from an error report, the cylinder, head, and sector address of the flaw is identified along with a defect parameter. The defect parameter for a DD-60 represents the byte boundary in the physical data field where the channel adapter starts to create an 18-byte defect pad.

Values for the defect parameter range from 0_8 to 4004_8 (0 to 2,052). The defect parameter, or location of the first byte of the defect pad, is calculated so that the 18-byte pad is centered over the media flaw. For example, if a media flaw is located at byte 31_8, the defect parameter for this flaw is 21_8 (refer to Figure 6-4).
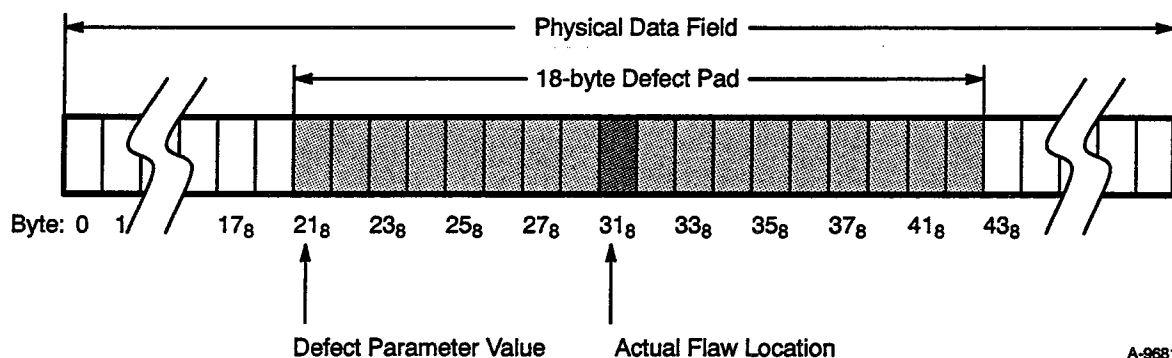
Figure 6-4. Defect Parameter and Actual Flaw Locations in a DD-60 Data Field

Before a write data field operation begins, the defect parameter is read from the sector ID field and transferred to a register in the channel adapter (refer again to Figure 3-1). The data parcel counter in the channel adapter is reset to 0.

The channel adapter uses a parcel counter to count each parcel of data as it is transferred to the disk drive. To count each 64-bit word (or 4 parcels) of data sent to the disk drive, the channel adapter disregards bits 2^0 and 2^1 of the parcel counter. Because the DD-60 uses 8 parallel heads to write data, one 64-bit word of data sent to the disk drive is equivalent to 8 bits (1 byte) of data in a physical data field.

When the value of the word count (from the parcel counter) is equivalent to the defect parameter, the channel adapter halts the parcel counter and starts the defect counter.

While the defect counter is decrementing, the channel adapter stops the transfer of new data to the disk. The channel adapter repeatedly transfers the previous (DCA-2) or next (DCA-3) parcel of data to the disk drive. This continues until 72 repeated parcels (18 bytes under each head) of data are sent to the DD-60.

By sending 72 repeated parcels of data to each DD-60, the channel adapter creates an 18-byte defect pad in the same location under each of the 8 parallel heads. Each byte sent to a physical sector/head corresponds to 1 64-bit word sent to the DD-60 (refer to Figure 6-5).

Physical Sector/Head	Valid Data Parcel	Repeated Logical Parcel	Repeated Logical Parcel	Repeated Logical Parcel	Repeated Logical Parcel	Repeated Logical Parcel	Repeated Logical Parcel	Repeated Logical Parcel	Repeated Logical Parcel	
0	V^0 V^8	R^0 R^8	R^0 R^8	R^0 R^8	R^0 R^8	R^0 R^8	R^0 R^8	R^0 R^8	R^0 R^8	R^0
1	V^1 V^9	R^1 R^9	R^1 R^9	R^1 R^9	R^1 R^9	R^1 R^9	R^1 R^9	R^1 R^9	R^1 R^9	R^1
2	V^2 V^{10}	R^2 R^{10}	R^2 R^{10}	R^2 R^{10}	R^2 R^{10}	R^2 R^{10}	R^2 R^{10}	R^2 R^{10}	R^2 R^{10}	R^2
3	V^3 V^{11}	R^3 R^{11}	R^3 R^{11}	R^3 R^{11}	R^3 R^{11}	R^3 R^{11}	R^3 R^{11}	R^3 R^{11}	R^3 R^{11}	R^3
4	V^4 V^{12}	R^4 R^{12}	R^4 R^{12}	R^4 R^{12}	R^4 R^{12}	R^4 R^{12}	R^4 R^{12}	R^4 R^{12}	R^4 R^{12}	R^4
5	V^5 V^{13}	R^5 R^{13}	R^5 R^{13}	R^5 R^{13}	R^5 R^{13}	R^5 R^{13}	R^5 R^{13}	R^5 R^{13}	R^5 R^{13}	R^5
6	V^6 V^{14}	R^6 R^{14}	R^6 R^{14}	R^6 R^{14}	R^6 R^{14}	R^6 R^{14}	R^6 R^{14}	R^6 R^{14}	R^6 R^{14}	R^6
7	V^7 V^{15}	R^7 R^{15}	R^7 R^{15}	R^7 R^{15}	R^7 R^{15}	R^7 R^{15}	R^7 R^{15}	R^7 R^{15}	R^7 R^{15}	R^7
Parity †	P P	P P	P P	P P	P P	P P	P P	P P	P P	P

18-byte Physical Defect Pad — Byte 0 of Physical Defect Pad — Byte 1 of Physical Defect Pad

† Parity head information does not apply to DCA-3 array applications

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Figure 6-5. Bytes 0 and 1 of the Physical Defect Pads

After creating the defect pads, the channel adapter restarts the parcel counter and signals the EIOP buffer board to resume the transfer of data. This continues until all of the data for the logical sector is sent to the disk drive.

Sector Format with a Hideable Flaw

When a defect pad is inserted into a physical sector, the physical length from the start of the data field to the end of the data field increases from 2,048 bytes to 2,066 bytes. To compensate for the increase in size, the channel adapter overwrites the defect swallow with data. Figure 6-6 shows the format of a physical sector that contains a hideable flaw.
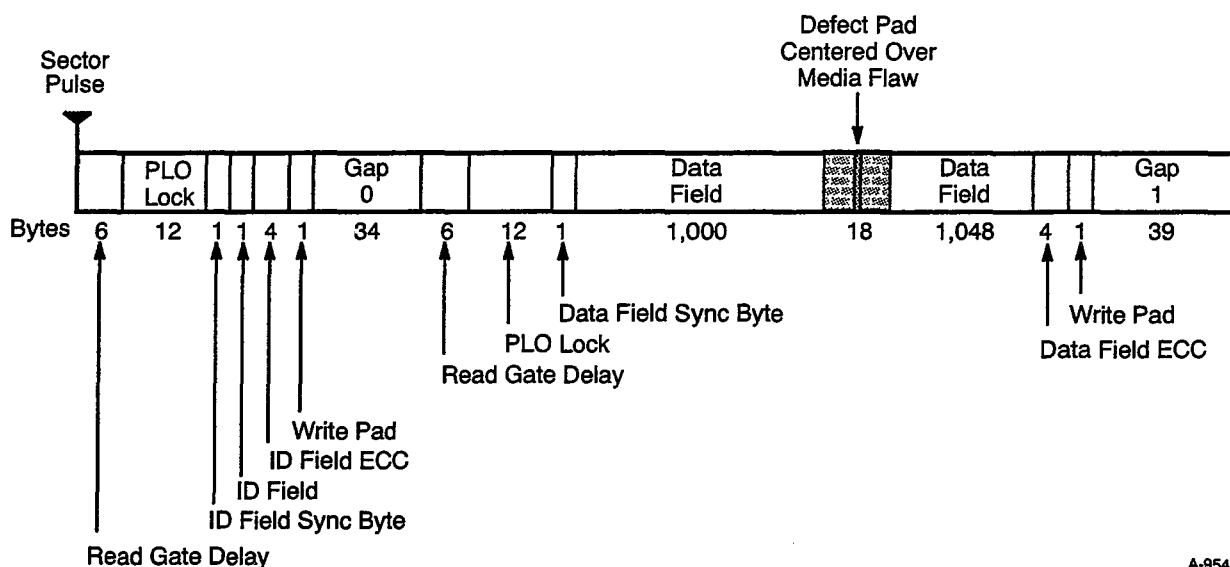
Figure 6-6. DD-60 Physical Sector with a Hideable Flaw

All 8 physical sectors must have a defect pad in the same location as the sector that has a media flaw. Therefore, the logical size of a defect pad is 144 bytes.

Hiding Multiple Media Flaws in One Logical Sector

Two flaws in the same sector under separate physical heads may be covered by one defect pad. If the combined flaws do not have the properties of an unhideable flaw, the channel adapter can create a defect pad to cover the combined flaws. Figure 6-7 shows one defect pad covering two physical sector flaws.
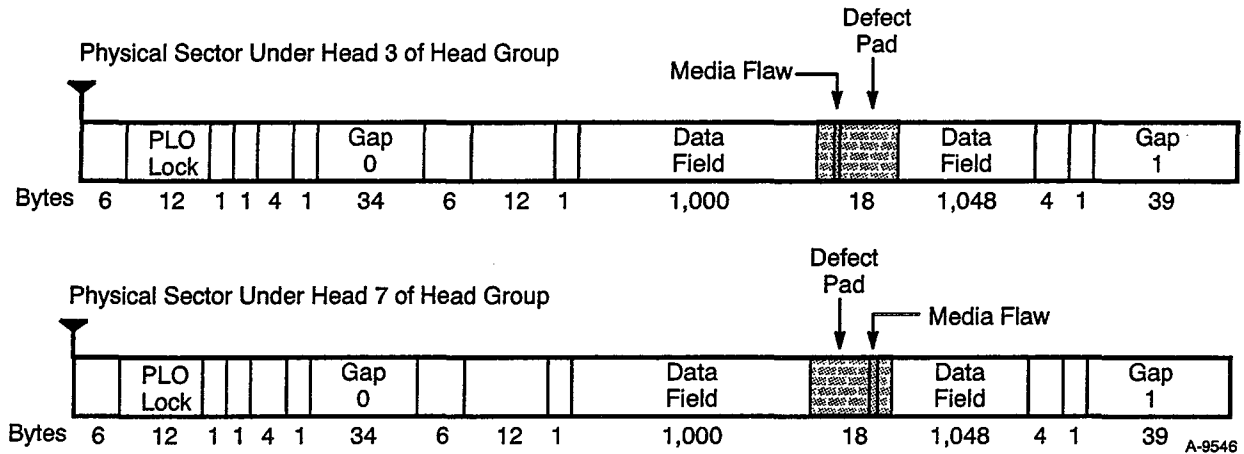
Figure 6-7. Two Physical Sectors with Hideable Flaws Covered by One Defect Pad

Reading a Sector with a Hideable Flaw

Before performing a read data field operation, the channel adapter reads the sector ID field and stores the defect parameter in a register of the channel adapter. The channel adapter then resets the parcel counter (refer again to Figure 3-1).

The channel adapter uses the parcel counter to count each parcel of data as it is transferred to the disk drive. To count each 64-bit word (or 4 parcels) of data sent to the disk drive, the channel adapter disregards bits 2^0 and 2^1 of the parcel counter. Because the DD-60 uses 8 parallel heads to write data, one 64-bit word of data sent from the disk drive is equivalent to 8 bits of data from each head in the head group.

When the value of the word count (from the parcel counter) is equivalent to the defect parameter, the channel adapter halts the parcel counter and starts decrementing the defect counter.

While the defect counter is decrementing, the channel adapter rejects the data parcels coming from the disk. This process continues until the 72 parcels of the defect pad are transferred from the disk drive to the channel adapter.

After all of the repeated data is transferred, the channel adapter resumes the acceptance of data parcels from the disk drive. This process continues until the rest of the data field is transferred to the channel adapter.

Unhideable Flaws

An unhideable flaw is a media flaw that cannot be hidden by a defect pad. If an unhideable flaw occurs, the entire sector cannot be used to store data. Any sectors that contain an unhideable flaw are marked by the operating system as unusable sectors. The following list describes some of the conditions that create an unhideable flaw:

- A flaw exists in the first 8 bytes of the data field.

- A flaw exists outside of the data field of a sector (such as ID or sync byte fields).

- A flaw is longer than 32 bits.

- Two or more flaws exist under separate heads and the combined flaw cannot be covered by one defect pad.

Flaw Maps and Tables

Flaw maps and tables store the locations of media flaws in the DD-60. The maps and tables include a factory flaw map, a user flaw table, and a UNICOS flaw map.

Factory Flaw Table

When Cray Research, Inc. (CRI) purchases a Sabre VI nine-head parallel (9HP) disk drive, it contains a factory flaw table on the even-numbered sectors of cylinder 2,610 (5062_8). The factory flaw table lists the physical locations of all the flaws found during manufacturing checkout. This information is used when the DD-60 is initially formatted.

User Flaw Table

The user flaw table contains a list of all the flaws, hideable and unhideable, including those added since the disk drive was initially formatted. It is located on the odd-numbered sectors of cylinder 2,610 (5062_8). Update the user flaw table every time you add a flaw to a sector in the DD-60. Table 6-4 shows the format of the user flaw table.

Table 6-4. User Flaw Table Format

Word	Parcel	Description
0	0	Cray Research, Inc. serial number in ASCII (bits 2^{63} through 2^{48})
	1	Cray Research, Inc. serial number in ASCII (bits 2^{47} through 2^{32})
	2	Cray Research, Inc. serial number in ASCII (bits 2^{31} through 2^{16})
	3	Cray Research, Inc. serial number in ASCII (bits 2^{15} through 2^{0})
1	0	HDA serial number in hexadecimal (bits 2^{31} through 2^{16})
	1	HDA serial number in hexadecimal (bits 2^{15} through 2^{0})
	2	Not used
	3	Date of recording in hexadecimal (bits 2^{15} through 2^{0})
2 through last entry	0	Flaw ID field parcel 0 (refer again to Figure 6-2)
	1	Flaw ID field parcel 1 (refer again to Figure 6-2)
	2	Flaw ID field parcel 2 (refer again to Figure 6-2)
	3	Flaw ID field parcel 3 (refer again to Figure 6-2)
Terminator	0	All 1's
	1	All 1's
	2	All 1's
	3	All 1's

UNICOS Flaw Map

The UNICOS flaw map is used by the operating system to locate sectors that contain unhideable flaws. If a sector is unusable, the operating system can remap the logical sector to another location in the DD-60. For DCA-3 applications, a sector that is unusable on one spindle will be marked by the operating system as unusable on all 5 spindles in the array.

NOTE: System flaw tables (sometimes referred to as O.S. flaw tables or Engineering flaw tables) do not apply to the 60 series disk drives. Cylinder 0, which was previously used to store the system flaw tables, is a customer cylinder on these drives.

SECTION 7
DD-61 HARDWARE DESCRIPTION
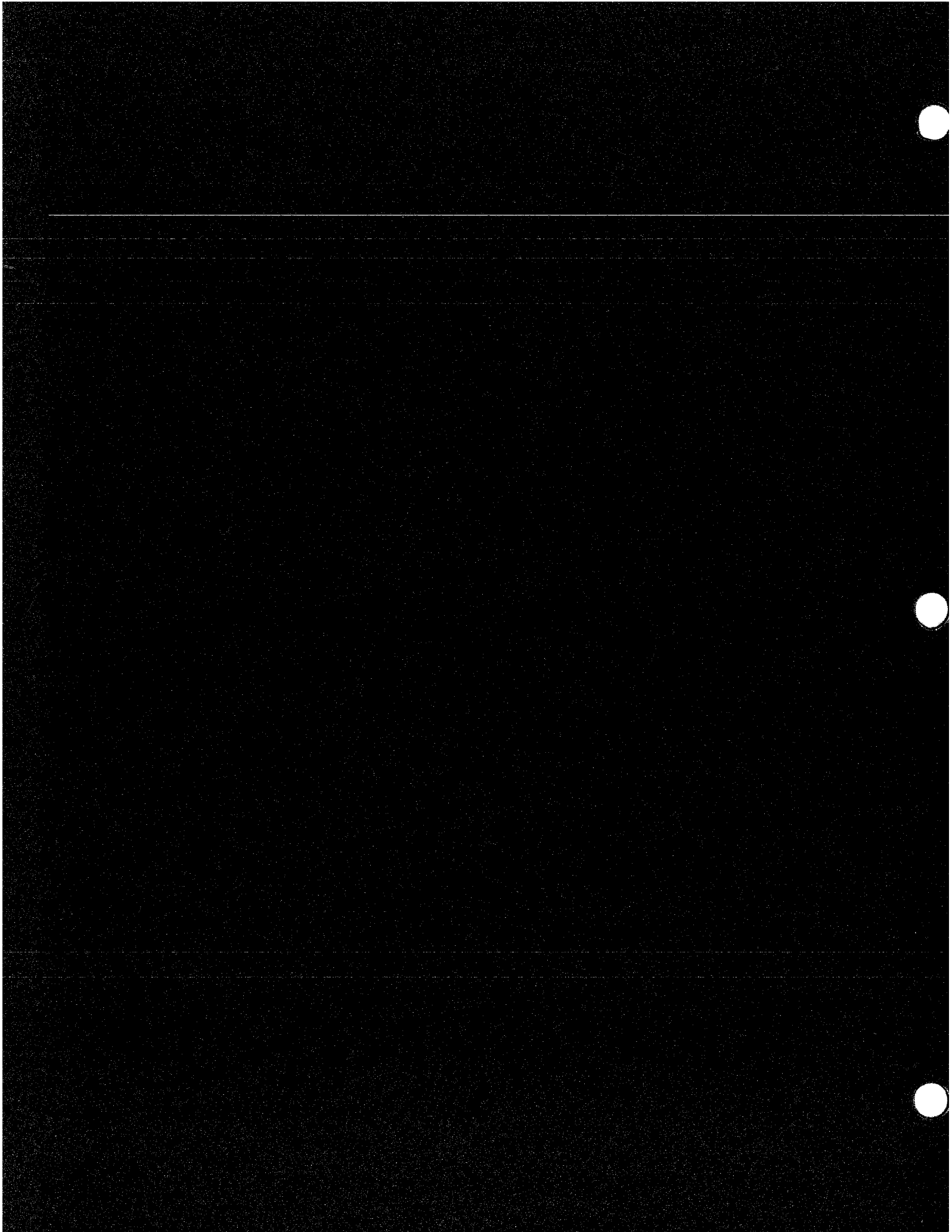
7   DD-61 HARDWARE DESCRIPTION

The DD-61 contains hardware that displays status, defines the disk drive format, and tests the internal circuitry. The hardware includes the rear panel, top panel, maintenance panel, and internal components. The rear panel, top panel, and internal components are described in the following subsections. Refer to the "Maintenance Procedures" section for information on the maintenance panel.

Rear Panel

The rear of the DD-61 contains two sets of dual-in-line package (DIP) switches. The vertical rear panel DIP switches set the format of the disk drive. Figure 7-1 shows the location of the rear panel vertical DIP switch.
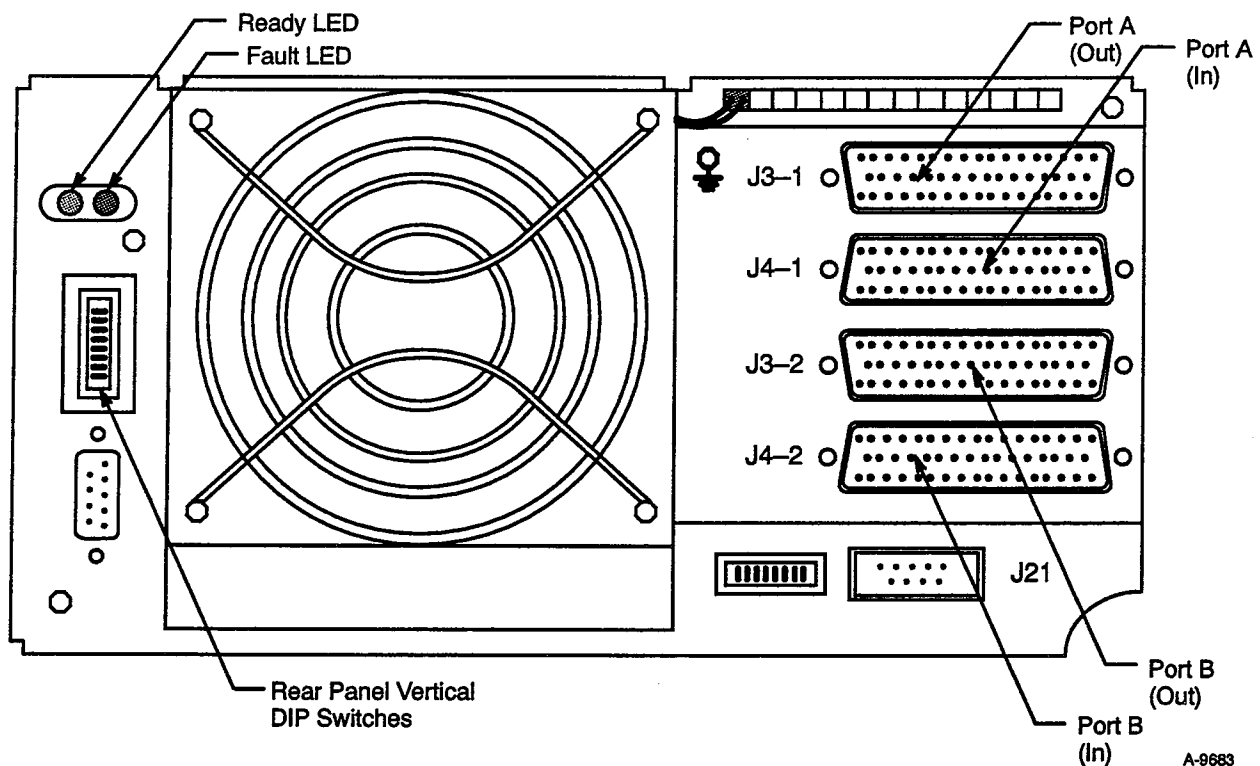
Figure 7-1. Rear Panel of a DD-61 Disk Drive

Rear Panel DIP Switches

The rear panel DIP switches, which are connected to the I/O board in the DD-61, change the modes of input and output operation. The switches are shown in Figure 7-2 below.
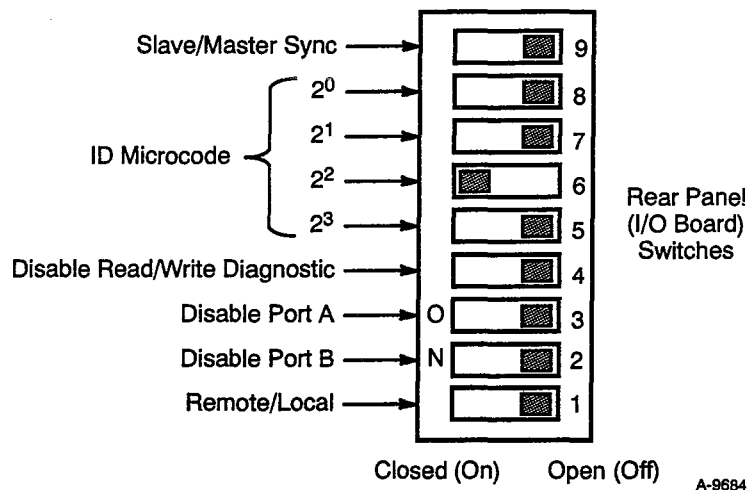
Figure 7-2. Rear Panel (I/O Board) DIP Switches on the DD-61

Slave/Master Sync

Set this switch to the open (Off) position to make the disk drive a slave for synchronization. A slave synchronizes its rotation to the signal from a master.

If this switch is in the closed (On) position, the disk drive is the master for synchronization. This option is currently not used by Cray Research, Inc., so the switch should be set to the off position.

ID Microcode

Make sure the ID microcode switches are set before powering on the disk drive. Do not reset these switches. If these switches change position, the DD-61 may be reformatted and the stored data overwritten.

CAUTION
Make sure the ID microcode switches are set to the correct positions before powering on the DD-61. If the switches are not correct and power is applied, the data stored in the DD-61 may be overwritten with a new format.

The ID microcode switches enable or disable internal disk drive circuitry. This circuitry enables or disables internal parity checking on the disk drive.

Disable Read/Write Diagnostic

Set this switch to the open (Off) position to enable the internal diagnostic read/write operation to the IPI diagnostic cylinder (5061_8).

Disable Port A

Set this switch to the open (Off) position to enable port A. Set this switch to the closed (On) position to disable port A.

Disable Port B

Set this switch to the open (Off) position to enable port B. Set this switch to the closed (On) position to disable port B.

Remote/Local

Set this switch to the open (Off) position to enable local mode. In local mode, the disk drive spins up when the START/STOP switch is pressed on the maintenance panel. If the disk drive does not have a maintenance panel and it is in local mode, it spins up when DC power is applied.

If this switch is set to the closed (On) position, the remote mode is enabled. In remote mode, the disk drive spins up only after it receives a spin-up command from a host controller.

Top Panel

The top panel of the DD-61 contains two sets of DIP switches, four jumpers, and four LEDs. They are mounted on the control circuit board in the DD-61. To access the switches, jumpers, and LEDs, remove the plastic protective cover from the hole in the top panel of the DD-61.

Jumpers

The top panel jumpers, which are connected to the control board in the DD-61, change the modes of the sweep cycle and the runt sector pulse (refer to Figure 7-3 and Table 7-1).
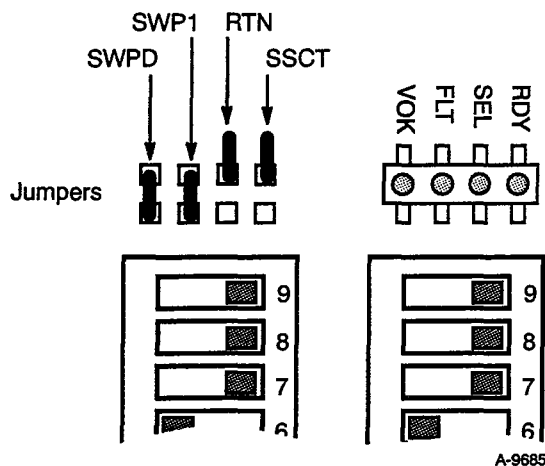
Figure 7-3. Top Panel Jumpers on the DD-61

Table 7-1 describes each of the top panel jumpers.

Table 7-1. Top Panel Jumper Descriptions

Name	Description
SWPD	Connect this jumper to disable the sweep cycle. A sweep cycle moves the heads across the surface of the platter at least once every 12 minutes.
SWP1	Connect this jumper to disable the option for sweep cycle on seeks only.
RTN	Disconnect this jumper to disable the option to return the heads to their original position after a sweep cycle. This is a factory set position. Do not connect this jumper.
SSCT	Disconnect this jumper to enable the detection of runt sector pulses. This jumper is set by the vendor before shipping.

LEDs

Early versions of the DD-61 disk drives were equipped with four top panel LEDs connected to the control board. Later model DD-61 drives do not include these LEDs. These LEDs display the current condition of the power supply and DD-61 disk drives (refer to Figure 7-4).
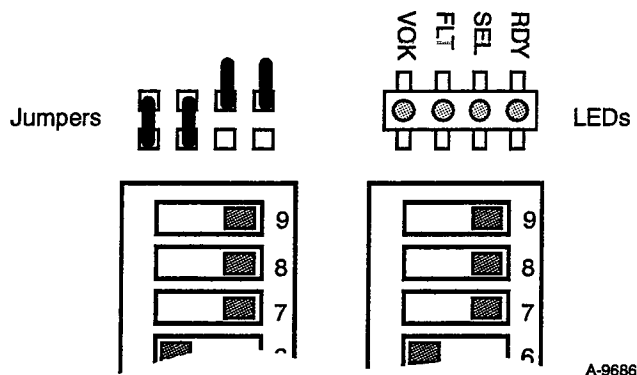
Figure 7-4. Top Panel LEDs on the DD-61

Table 7-2 describes each of the four top panel LEDs.

Table 7-2. Top Panel LED Descriptions

Name	Description
VOK	The voltage (VOK) LED illuminates if the +5-V power supply is working correctly.
FLT	The drive fault (FLT) LED illuminates if a fault condition is detected by the disk drive.
SEL	The drive selected (SEL) LED illuminates when the DD-61 acknowledges a select command.
RDY	The drive ready (RDY) LED illuminates when the platters are up to speed, the heads are positioned over the first cylinder, and the disk drive is ready for use. The RDY LED also flashes during spin-up and spin-down sequences.

Top Panel DIP Switches

The top panel DIP switches, which are connected to the control board, change the modes of disk drive operation. The switches are shown below in Figure 7-5.
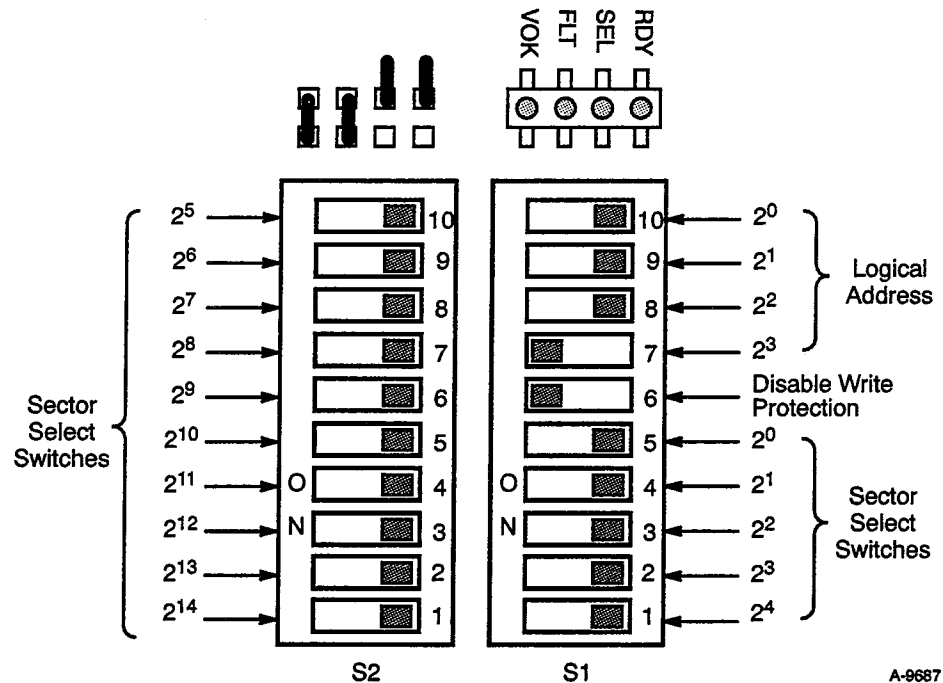
Figure 7-5. Top Panel (Control Board) DIP Switches on the DD-61

Sector Switches

These switches are not used. The settings of these switches have no effect on the DD-61 operation.

Disable Write Protection

Set this switch to the closed (On) position to disable the write protection mode. Set this switch to the open (Off) position to enable the write protection mode. If the write protection mode is enabled, data cannot be written to the disk drive.

Logical Address

Set these switches to the appropriate logical address of the disk drive (refer to Table 7-3). Each disk drive in a daisy chain or alternate-path configuration must have a unique logical address (refer to Figure 7-6).

Table 7-3. Upper DIP Switch Settings for Logical Address

Logical Address	Switch 7	Switch 8	Switch 9	Switch 10
0	Closed (On)	Closed (On)	Closed (On)	Closed (On)
1	Closed (On)	Closed (On)	Closed (On)	Open (Off)
2	Closed (On)	Closed (On)	Open (Off)	Closed (On)
3	Closed (On)	Closed (On)	Open (Off)	Open (Off)
4	Closed (On)	Open (Off)	Closed (On)	Closed (On)
5	Closed (On)	Open (Off)	Closed (On)	Open (Off)
6	Closed (On)	Open (Off)	Open (Off)	Closed (On)
7	Closed (On)	Open (Off)	Open (Off)	Open (Off)
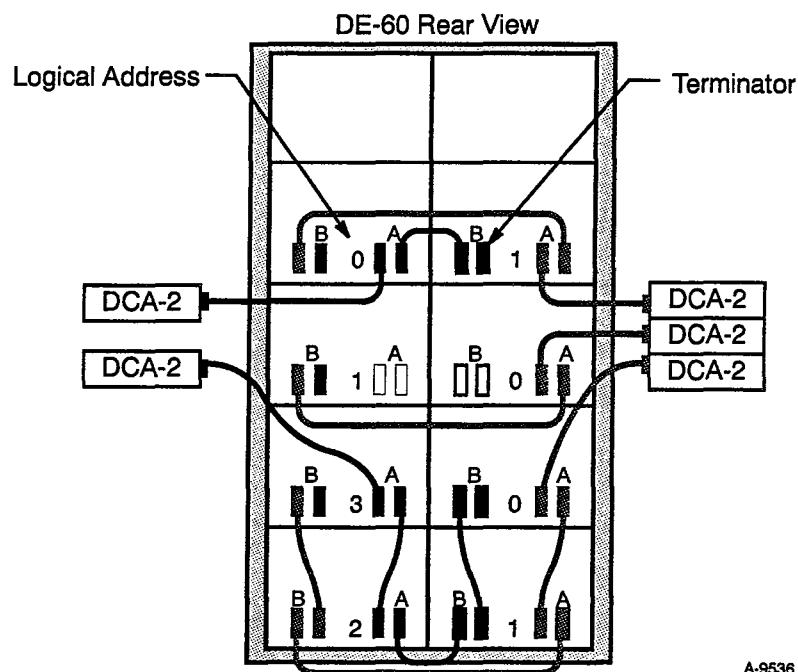
Figure 7-6. Logical Addresses of Disk Drives in a DE-60

If a maintenance panel is connected to the disk drive, the DIP switches do not set the logical address. Refer to the "Maintenance Procedures" section for information on setting the logical address using the maintenance panel.

Internal Components

DD-61 disk drives are Sabre VI 19-head serial disk drives. The Sabre VI 19-head serial disk drive contains three types of internal components: the circuit boards, head disk assembly (HDA) module, and power supply.

Circuit Boards

The DD-61 contains two circuit boards: a control board and an I/O board.

The control board directly controls most disk drive functions, which include read, write, seek, and spindle synchronization. It is mounted to the top of the HDA module and connects to the HDA module through pin connectors under the control board. Figure 7-7 shows the location of the control board relative to the HDA module.

The I/O board controls the disk drive input/output operations, which include selection of the DD-61 and data formatting. Figure 7-7 shows the location of the I/O board relative to the HDA module.
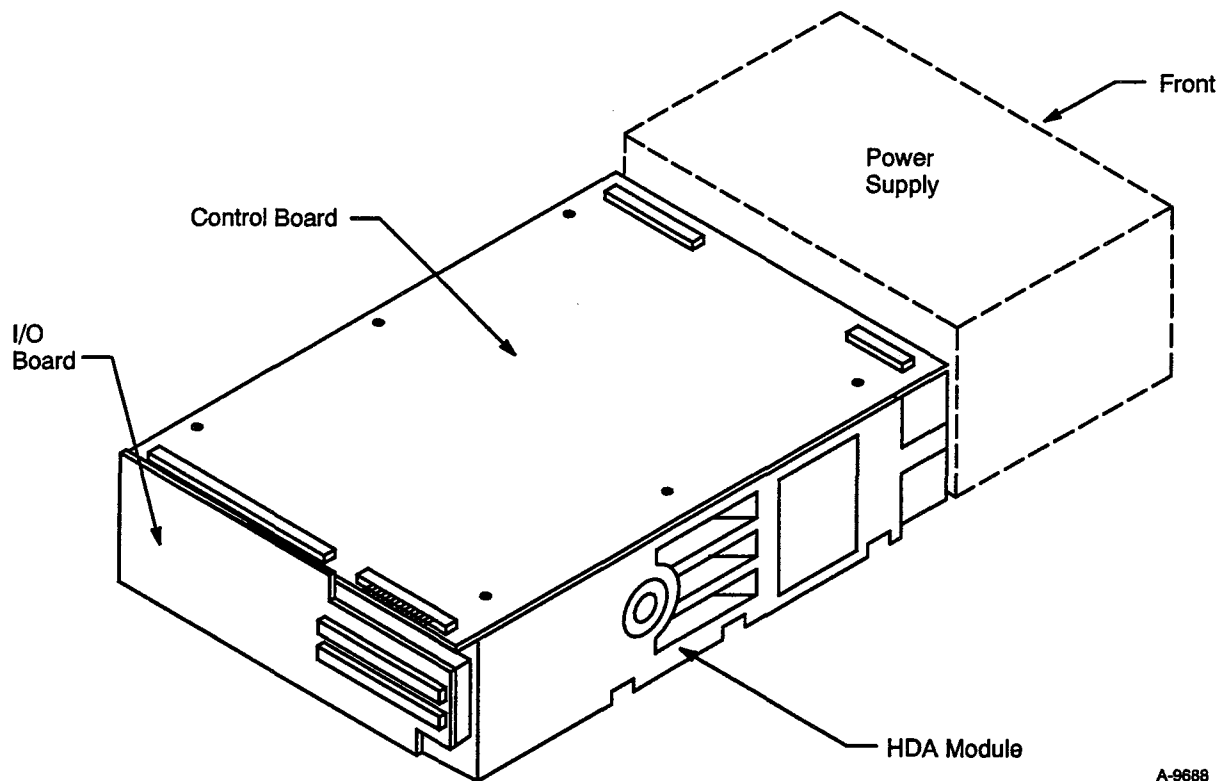
Figure 7-7. DD-61 Circuit Board Locations

HDA Module

The HDA is a sealed module that contains the circuitry and hardware used to store information; this hardware includes platters, heads, an actuator, a spindle, and a spindle motor.

Platters

The HDA module contains 11 platters that rotate at 3,600 revolutions per minute. Nine of the platters contain two thin-film media surfaces for reading or writing data. The top and bottom platter contain only one thin-film media surface (refer to Figure 7-8).
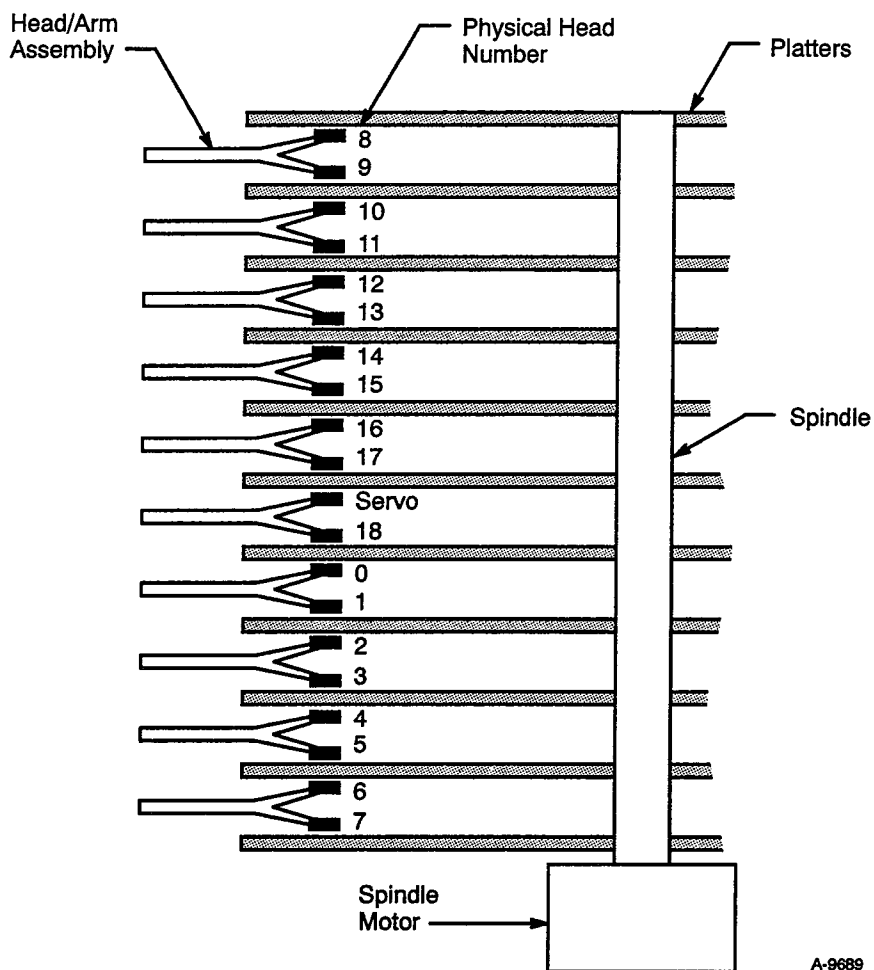
Figure 7-8. DD-61 Physical Head Locations in the HDA

Heads

The heads transfer information to or from the platter media surface. One head transfers servo information, and 19 heads transfer data (refer again to Figure 7-8).

Actuator

The actuator positions the heads over any of the 2,611 tracks on the platter surface. The DD-61 has a balanced rotary actuator so the heads move in an arc over the platters.

Spindle

The spindle attaches to the center of all the platters and holds them in place. It is directly connected to the spindle motor (refer again to Figure 7-8).

Spindle Motor

The spindle motor is a 3-phase motor that rotates at 3,600 revolutions per minute. It is directly connected to the spindle and platter assembly (refer again to Figure 7-8). The spindle motor is controlled by a dedicated motor microprocessor unit on the control board. This dedicated MPU controls the motor via 3-phases of pulse-width modulated signals.

Power Supply

The external power supply converts 115 Vac or 230 Vac into DC voltages. All components of the disk drive operate on DC voltage. These voltages are +5 Vdc, −5 Vdc, +12 Vdc, −12 Vdc, and +24 Vdc.

Maintenance Panel

The maintenance panel is attached to the front of the power supply and allows the user to set the logical address, examine statuses, view error logs, and run diagnostics. For more information on the maintenance panel, refer to the "Maintenance Procedures" section.

If a maintenance panel is connected to the drive, the start button should be used to spin the drive up or down. The main circuit breaker on the DE-60 and the power On/Off switch located on the front of each drive should not be used to power off the drive while it is spinning. When you spin a drive down, you can turn the power On/Off switch to the Off

position only after the drive has been allowed to complete its spin-down sequence. This allows the drive to position its heads over the landing zone before power is lost.

If a maintenance panel is not connected to the drive, it can be powered up and down by using the power On/Off switch located on the front of each drive.

SECTION 8
DD-61 FORMAT AND FLAW MANAGEMENT

8   DD-61 FORMAT AND FLAW MANAGEMENT

This section covers format specifications and flaw management properties of the DD-61 including cylinder format, sector format, media flaws, and flaw maps and tables.

Cylinder Format

The DD-61 has 2,611 cylinders, including data cylinders, diagnostic cylinders, and a flaw table cylinder. Table 8-1 shows the addresses of these cylinders in decimal and octal.

Table 8-1. DD-61 Cylinder Map

Cylinder Type	Addresses
Data cylinders	0 - 2,607 0 - 5057_8
Diagnostic scratch cylinder	2,608 5060_8
IPI diagnostic cylinder	2,609 5061_8
User flaw table cylinder	2,610 (odd sectors) 5062_8 (odd sectors)
Factory flaw table cylinder	2,610 (even sectors) 5062_8 (even sectors)

Data cylinders store system data. Do not write data patterns to these cylinders unless the customer data is offloaded to an alternate location.

The diagnostic scratch cylinder is reserved for DD-61 diagnostics. Use this cylinder to read and write data patterns without destroying system data.

The IPI diagnostic cylinder is reserved for the disk drive. The internal read/write diagnostics use this cylinder during spin-up of the DD-61.

The flaw table cylinder contains both the factory flaw table and the user flaw table. For more information on flaw tables, refer to the "Flaw Maps and Tables" subsection later in this section.

Sector Format

Figure 8-1 shows the format of a DD-61 sector. Each sector contains five field types: timing, ID, data, error-correction code (ECC), and defect swallow. These fields are described in the following subsections.
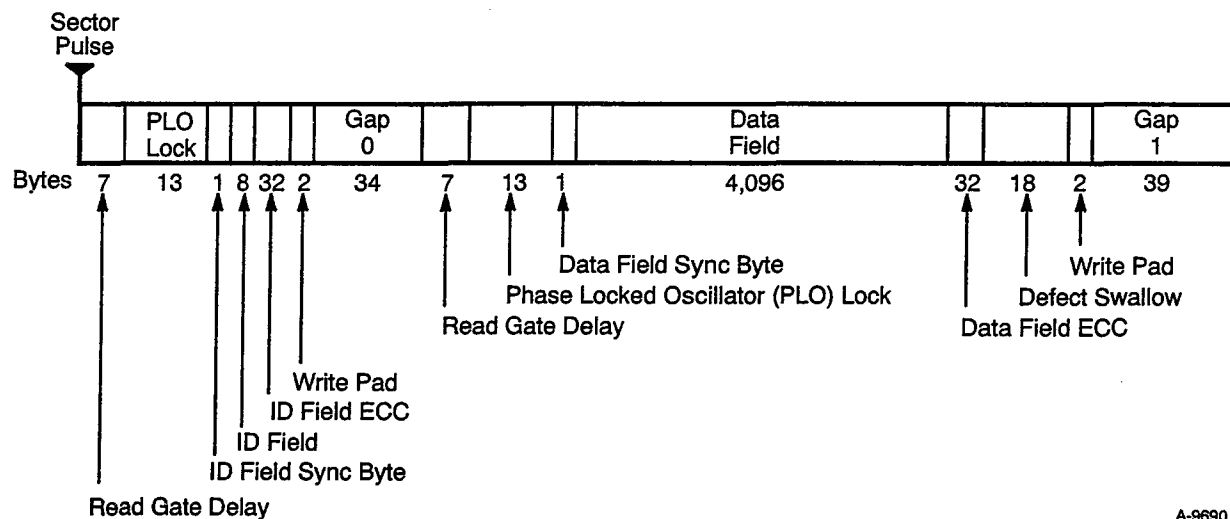
Figure 8-1. DD-61 Sector Format

Timing Fields

Timing fields create time delays for the synchronization of the timing circuits during read or write operations. These fields are read gate delay, PLO lock, sync bytes, write pad, gap 0, and gap 1.

For an example of how a timing field is used: gap 0 provides a time delay for the DD-61 to interpret the next command (a read or write data field). Without this delay, the information stored in the data field would be sent to the DCA-2 immediately after the ID information.

Data Field

The data field contains 4,096 bytes of system data.

ID Field

The ID field contains 8 bytes of information that identify the sector address and whether the sector contains a flaw. Figure 8-2 shows the format of the ID field and Table 8-2 describes each bit in the ID field.

←——— Byte 0 ———→	←——— Byte 1 ———→
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
x	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0

←——— Byte 2 ———→	←——— Byte 3 ———→
C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

←——— Byte 4 ———→	←——— Byte 5 ———→
X	X	WP	RP	X	H	H	H	H	H	S	S	S	S	S	S
x	x	0	0	x	2^4	2^3	2^2	2^1	2^0	2^5	2^4	2^3	2^2	2^1	2^0

←——— Byte 6 ———→	←——— Byte 7 ———→
VF	UH	ID	D	D	D	D	D	D	D	D	D	D	D	D	D
2^0	2^0	2^0	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

A-9542
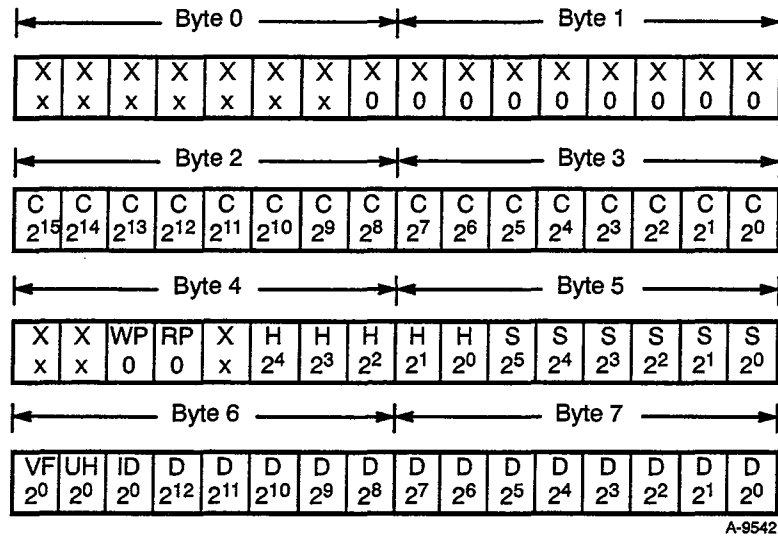
Figure 8-2. DD-61 ID Field Format

Table 8-2. DD-61 Logical ID Information Description

Bit Symbol	Name	Description
X	Not used	This bit is not used.
C	Cylinder address	These bits contain the cylinder address of the data $(0 - 5062_8)$.
WP	Write protect (must be set to 0)	When set to 1, this bit indicates that data cannot be written to the sector unless this bit is also set in parameter register 1 (currently unused).
RP	Read protect (must be set to 0)	When set to 1, this bit indicates that data cannot be read from the sector unless this bit is also set in parameter register 1 (currently unused).
H	Head address	These bits contain the logical head address of the data $(0 - 22_8)$.
S	Sector address	These bits contain the sector address of the data $(0 - 12_8)$.
VF	Valid flaw	When set to 1, this bit indicates that the flaw in the sector is a known hideable flaw.
UH	Unhideable flaw	When set to 1, this bit indicates that the flaw in the sector is unhideable.
ID	ID field flaw	When set to 1, this bit indicates that the ID field contains an unhideable flaw.
D	Defect parameter	These bits contain the defect parameter. If the sector does not have a media flaw in the data field, the defect parameter is 1004_8.

Error-correction Code Fields

The ECC field contains ECC generated by the DCA-2 during a write data operation. The DCA-2 uses this information to correct data errors during a read operation.

During a read data operation, the DCA-2 reads the data or ID field and generates new ECCs. The DCA-2 then compares the new ECCs to the information read from the sector ECC fields.

If the ID or data field ECCs do not match the generated ECCs, the DCA-2 signals the EIOP that an error has occurred. If the error occurs in the data field, the DCA-2 can determine which bits are incorrect and correct them.

Defect Swallow

The defect swallow enables the data field to expand if a hideable flaw is placed in the sector. For more information on the defect swallow and hideable flaws, refer to the "Media Flaws" subsection that follows.

Media Flaws

A media flaw is a defect on the surface of a platter that does not allow the disk drive to read or write information correctly. Flaws are grouped into two categories: hideable flaws and unhideable flaws.

Hideable Flaws

A hideable flaw is a media defect that can be effectively covered by a physical 18-byte defect pad. The DCA-2 creates a defect pad when it writes data to the logical data field.

Hiding a Media Flaw

When a media defect is found during surface analysis or from an error report, the cylinder, head, and sector address of the flaw is identified along with a defect parameter. The defect parameter is the word number in the data field where the DCA-2 starts to create an 18-byte defect pad.

Values for the defect parameter range from 0 to 1004_8 (0 to 4,100). The defect parameter is calculated so that the 18-byte defect pad most effectively covers the media flaw. For example, if a media flaw is located at byte 20_8 (refer to Figure 8-3), the defect pad for this flaw should start at word 1 (byte 10). Although defect pads that start at word 0 and word 2 (bytes 0 and 20_8) would cover the media flaw, the defect pad that starts at word 1 more effectively covers the media flaw.
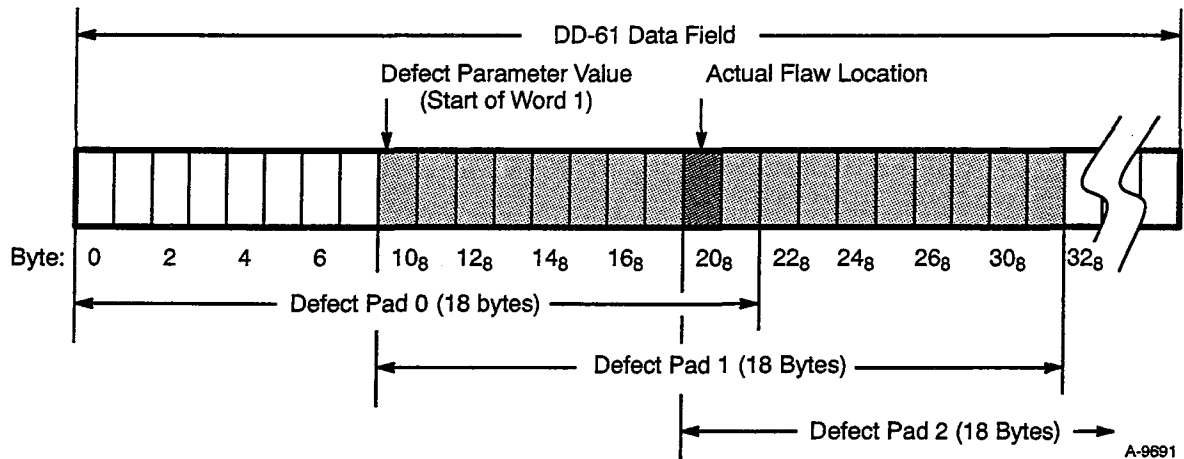
Figure 8-3. Defect Parameter and Actual Flaw Locations in a DD-61 Data Field

Before a write data field operation begins, the defect parameter is read from the sector ID field and transferred to a register in the 3DG option (refer again to Figure 3-1). The data parcel counter in the 3DG is reset to 0. The DCA-2 uses the parcel counter in the 3DG to count each parcel of data as it is transferred to the disk drive.

When the value of the parcel counter is equivalent to the defect parameter, the DCA-2 halts the parcel counter and starts decrementing the defect counter. While the defect counter is decrementing, the sequencer sends a signal to the DCA-2 and EIOP buffer board that halts the transfer of data to the 3DF option.

Because the 3DF option does not receive new data, it sends the previous logical parcel of data to the disk drive until 9 repeated parcels (18 bytes) of data are sent to the disk drive.

After creating the defect pad, the sequencer restarts the parcel counter and signals the DCA-2 and EIOP buffer board to resume the transfer of data to the 3DF option. This transfer continues until all of the data for the data field has been sent to the disk drive.

Sector Format with a Hideable Flaw

When a defect pad is inserted into a sector, the physical length from the start of the data field to the end of the data field increases from 4,096 bytes to 4,114 bytes. To compensate for the increase in size, the DCA-2 overwrites the defect swallow with data. Figure 8-4 shows the format of a sector that contains a hideable flaw.
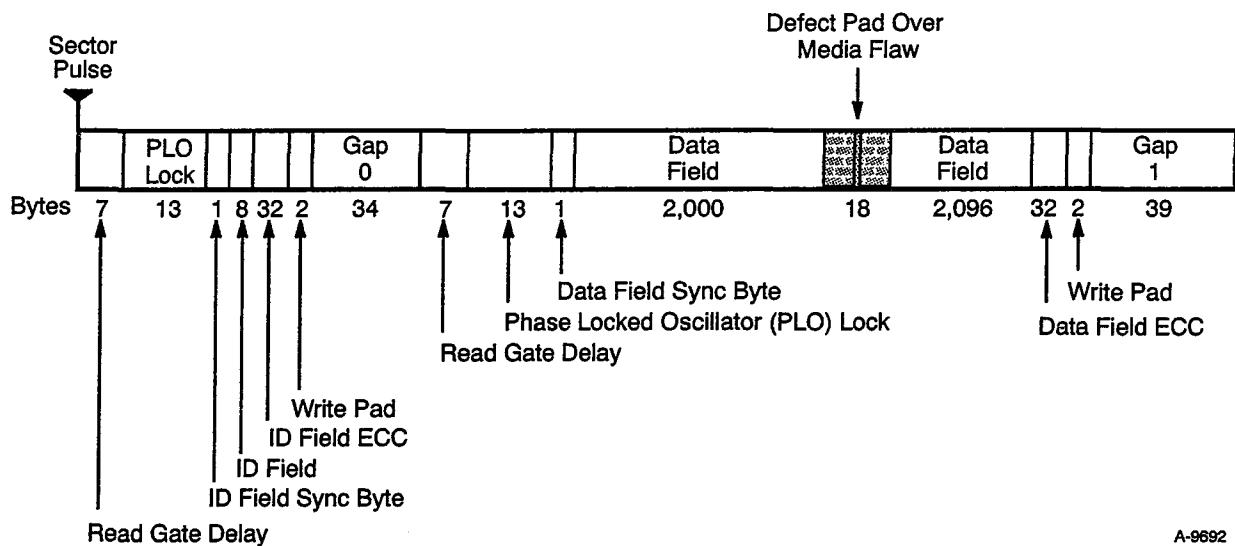
Figure 8-4. DD-61 Sector with a Hideable Flaw

Reading a Sector with a Hideable Flaw

Before performing a read data field operation, the DCA-2 reads the sector ID field and stores the defect parameter in a register of the 3DG option. The DCA-2 then resets the parcel counter in the 3DG option to 0 (refer again to Figure 3-1).

During the read data field operation, the parcel counter counts each parcel of data as it is transferred from the disk drive to the DCA-2. When the value of the parcel counter matches the value of the defect parameter, the sequencer stops the parcel counter and starts decrementing the defect counter.

While the defect counter is decrementing, the sequencer signals the 3YB option not to accept the data parcels coming from the 3DE until after the 9 repeated parcels (18 bytes) have been transferred from the disk drive to the DCA-2.

After all of the repeated data has been transferred, the sequencer restarts the parcel counter and signals the 3YB option to resume accepting data parcels from the disk drive until the rest of the data field is transferred to the DCA-2.

Unhideable Flaws

An unhideable flaw is a media flaw that cannot be hidden by a defect pad. If an unhideable flaw occurs, the entire sector is unable to store data. Any sectors that contain an unhideable flaw are marked by the operating system as unusable sectors. The following list describes some of the conditions that create an unhideable flaw.

- A flaw exists in the first 8 bytes of the data field.

- A flaw exists outside of the data field of a sector (for example, ID or sync byte fields).

- A flaw is longer than 32 bits.

Flaw Maps and Tables

Flaw maps and tables store the locations of media flaws in the DD-61. The maps and tables include a factory flaw map, a user flaw table, and a UNICOS operating system flaw map.

Factory Flaw Table

When Cray Research, Inc. (CRI) purchases a Sabre VI nine-head parallel (9HP) disk drive, it contains a factory flaw table on the even-numbered sectors of cylinder 2,610 (5062_8). The factory flaw table lists the physical locations of all the flaws found during manufacturing checkout. This information is used when the DD-61 is initially formatted.

User Flaw Table

The user flaw table contains a list of all the flaws, hideable and unhideable, including those added since the disk drive was initially formatted. It is located on the odd-numbered sectors of cylinder 2,610 (5062_8). Update the user flaw table each time you add a flaw to a sector in the DD-61. Table 8-3 shows the format of the user flaw table.

Table 8-3. User Flaw Table Format

Word	Parcel	Description
0	0	Cray Research, Inc. serial number in ASCII (bits 2^{63} through 2^{48})
	1	Cray Research, Inc. serial number in ASCII (bits 2^{47} through 2^{32})
	2	Cray Research, Inc. serial number in ASCII (bits 2^{31} through 2^{16})
	3	Cray Research, Inc. serial number in ASCII (bits 2^{15} through 2^{0})
1	0	HDA serial number in hexadecimal (bits 2^{31} through 2^{16})
	1	HDA serial number in hexadecimal (bits 2^{15} through 2^{0})
	2	Not used
	3	Date of recording in hexadecimal (bits 2^{15} through 2^{0})
2 through last entry	0	Flaw ID field parcel 0 (refer to Figure 8-2)
	1	Flaw ID field parcel 1 (refer to Figure 8-2)
	2	Flaw ID field parcel 2 (refer to Figure 8-2)
	3	Flaw ID field parcel 3 (refer to Figure 8-2)
Terminator	0	All 1's
	1	All 1's
	2	All 1's
	3	All 1's

UNICOS Flaw Map

The UNICOS flaw map is used by the operating system to locate sectors that contain unhideable flaws. If a sector is unusable, the operating system can remap the logical sector to another location in the DD-61.

NOTE: System flaw tables (sometimes referred as O.S. flaw tables or Engineering flaw tables) do not apply to the 60 series disk drives. Cylinder 0, which was previously used to store the system flaw tables, is a customer cylinder on these drives.

SECTION 9
DD-62 AND RD-62 HARDWARE DESCRIPTION
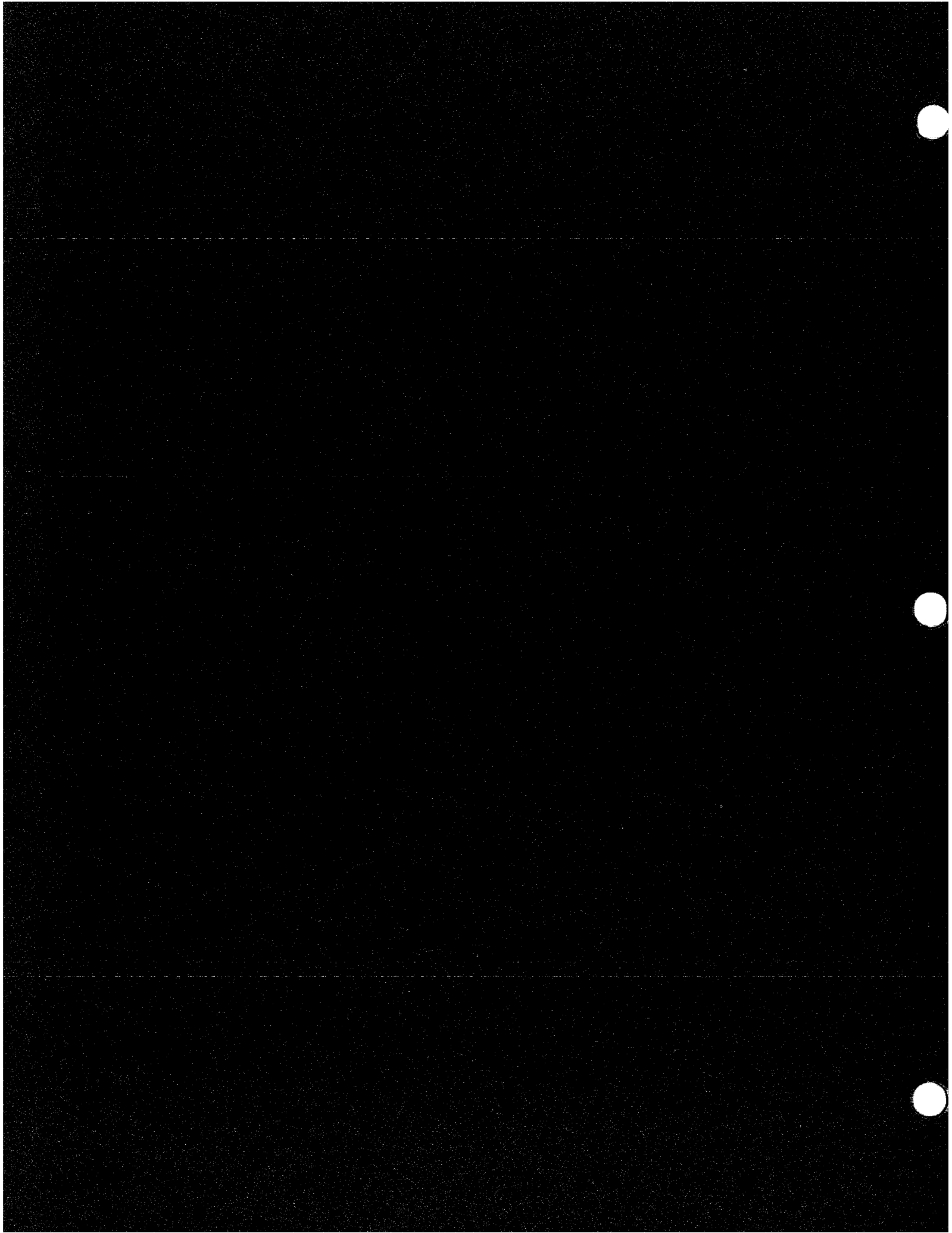
9 DD-62 AND RD-62 HARDWARE DESCRIPTION

The DD-62 and RD-62 disk drives contain hardware that displays status, defines the disk drive format, and tests the internal circuitry. The hardware includes the rear panel, top panel, maintenance panel, and internal components. The rear panel, top panel, and internal components are described in the following subsections. Refer to the "Maintenance Procedures" section for information on the maintenance panel.

Rear Panel

The rear of the DD-62 and RD-62 disk drives contain two sets of dual-in-line package (DIP) switches. The rear panel DIP switch 1 (SW1) sets the format of the disk drive. DIP switch 2 (SW2) sets various hardware options on the DD-62. Both switches require different settings for DCA-2 and DCA-3 applications. Figure 9-1 shows the locations of the DIP switches.
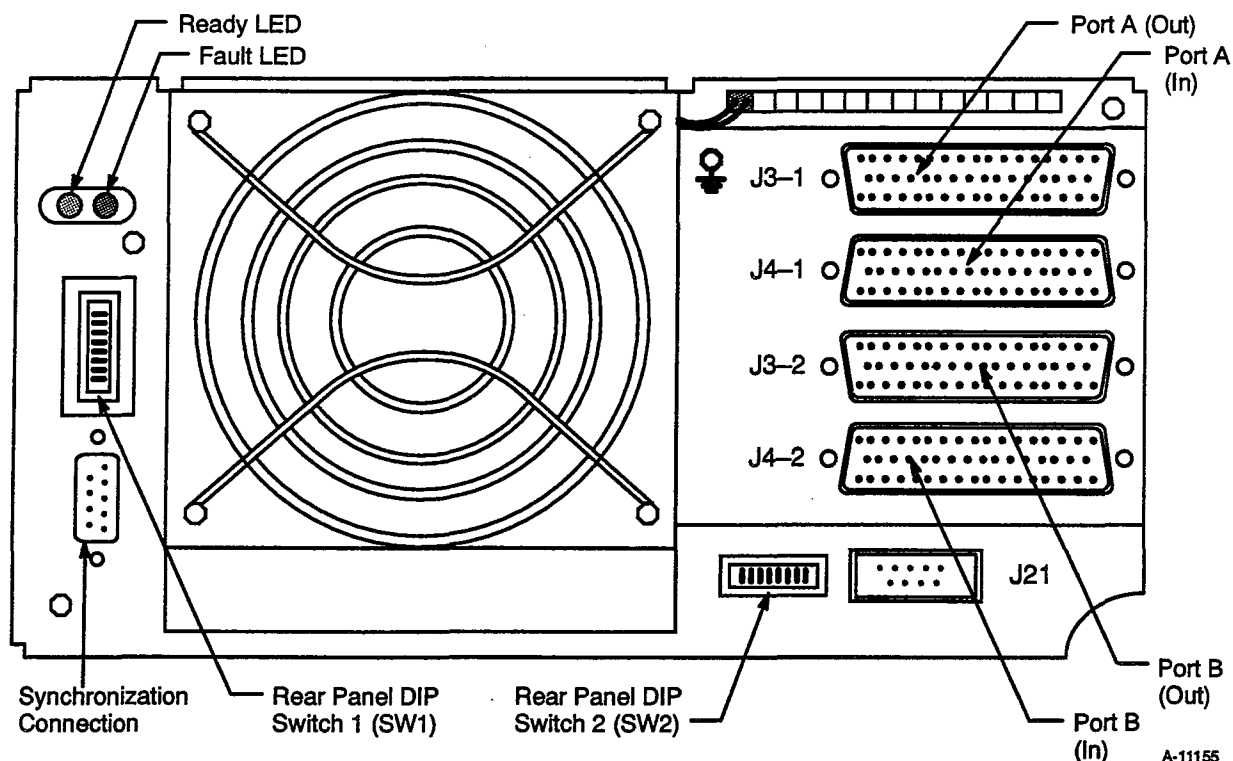
Figure 9-1. Rear Panel of a DD-62 Disk Drive

Rear Panel DIP Switches

The following subsections describe the rear panel DIP switches on the DD-62 and RD-62.

Rear Panel DIP Switch 1

The rear panel DIP switch (SW1) changes the modes of input and output operation. The DCA-2 and DCA-3 channel adapters require different SW1 switch settings. The SW1 switch settings are shown in Figure 9-2.

CAUTION

The DD-62 SW1 DIP switches must be set according to the type of channel adapter being used. Switch settings for DCA-2 applications will not work if the DD-62 is connected to a DCA-3 as an array.
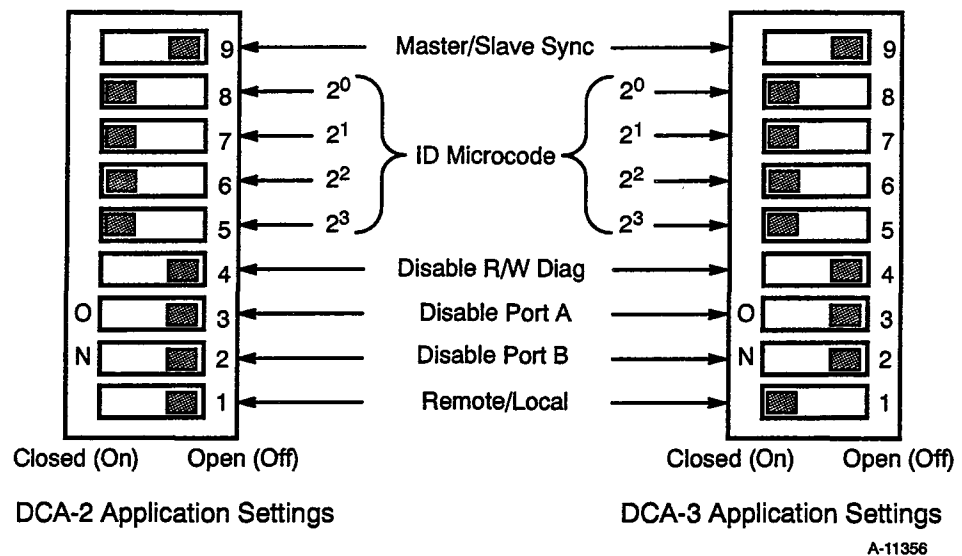
Figure 9-2. Rear Panel DIP Switch 1 (SW1)

Slave/Master Sync

Set this synchronization switch to the open (Off) position to allow software commands to assign the DD-62 as a master or slave. Spindle synchronization is used for DCA-3 applications only.

ID Microcode

Make sure the ID microcode switches are properly set before powering on the disk drive. Do not reset these switches. If these switches change position, the format of the DD-62 will change, and stored data will become inaccessible. The ID microcode switches enable or disable internal disk drive circuitry. This circuitry enables or disables internal parity checking on the disk drive.

```
+-------------------------------------------------------+
|                                                       |
|                    CAUTION                            |
|                                                       |
+-------------------------------------------------------+
|                                                       |
|   Make sure the ID microcode switches are set to the  |
|   correct positions before powering on the DD-62. If  |
|   the switches are not correct and power is applied,   |
|   the data stored in the DD-62 hardware may be        |
|   overwritten with a new format.                      |
|                                                       |
+-------------------------------------------------------+
```

Disable Read/Write Diagnostic

Set this switch to the open (Off) position to enable the internal diagnostic read/write operation to the IPI diagnostic cylinder (5135_8).

Disable Port A and Disable Port B

Set these switches to the open (Off) position to enable ports A and B.

Remote/Local

Set this switch to the open (Off) position to enable local mode for DCA-2 applications. In local mode, the disk drive spins up when the START switch is pressed on the maintenance panel. If the disk drive does not have a maintenance panel and it is in local mode, it spins up when DC power is applied.

Set this switch to the closed (On) position to enable remote mode for DCA-3 applications. In remote mode, the disk drive spins up after it receives a spin-up command from a host controller. Before remote spin-up can occur, you must ensure that the START button is pressed and the DE-60 cabinet breaker and spindle power supply switches are in the ON position. Refer to the spin-up and spin-down procedures in the "Maintenance Procedures" section of this manual.

Rear Panel DIP Switch 2

The rear panel DIP switch 2 (SW2), which is connected to the I/O board in the DD-62, changes the hardware options of the DD-62. The DCA-2 and DCA-3 channel adapters require different SW2 switch settings. The SW2 switch settings for each channel adapter are shown in Figure 9-3.

CAUTION

The DD-62 SW2 DIP switches must be set according to the type of channel adapter being used. Switch settings for DCA-2 applications will not work if the DD-62 is connected to a DCA-3 as an array.

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† Rotation position sensing
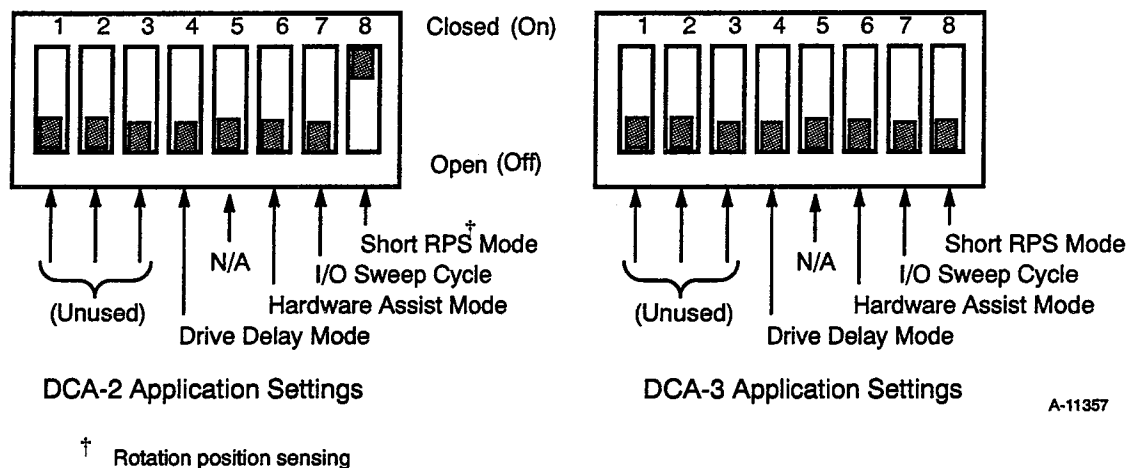
Figure 9-3. Rear Panel DIP Switch 2 (SW2)

Drive Delay Mode

When disabled (Off), the drive will not increase the master turnaround delay received in the load format specification command. This action accounts for its own logic and protocol delays.

Hardware Assist Mode

This feature only applies to the 04, 05, 06, and 07 bus commands. When enabled (Off), ending status is presented much sooner due to enhanced hardware implementation.

I/O Board Initiated Sweep Cycle

When disabled (Off), this switch prevents the I/O board from initiating a seek every fifteen minutes if the DCA-2 has not issued a seek during that time.

Short RPS Mode

When enabled (On) for DCA-2 applications, this switch enables the drive to return the remaining portion of an RPS pulse (sector found) if an RPS-related command (find sector) completes during the defined RPS time (at sector). For DCA-3 applications, this switch should be disabled (Off).

Top Panel

The top panel of the DD-62 contains one set of DIP switches (SW3) and 3 jumpers. They are mounted on the control circuit board in the DD-62. To access the switches and jumpers, remove the plastic protective cover from the hole in the top panel of the DD-62.

Top Panel DIP Switch 3

The top panel DIP switch 3 (SW3), which is accessible through a port on top of the DD-62, changes the address and write mode of disk drive operation. The switch settings shown apply to both DCA-2 and DCA-3 applications. The switch is shown in Figure 9-4.
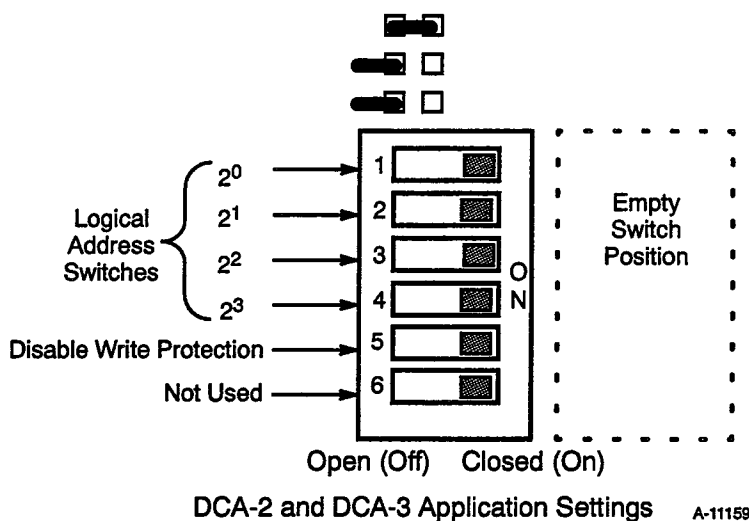
Figure 9-4. Top Panel DIP Switch 3 (SW3)

Logical Address Switches

Set these switches to the appropriate logical address of the disk drive (refer to Table 9-1). Each disk drive in a daisy chain or alternate-path configuration must have a unique logical address (refer to Figure 9-5).

NOTE: Because the RD-62 disk drives cannot be daisy chained, they should always be set to a logical address of 0.

Table 9-1. SW3 DIP Switch Settings for Logical Address

Logical Address	Switch 1	Switch 2	Switch 3	Switch 4
0	Closed (On)	Closed (On)	Closed (On)	Closed (On)
1	Open (Off)	Closed (On)	Closed (On)	Closed (On)
2	Closed (On)	Open (Off)	Closed (On)	Closed (On)
3	Open (Off)	Open (Off)	Closed (On)	Closed (On)
4	Closed (On)	Closed (On)	Open (Off)	Closed (On)
5	Open (Off)	Closed (On)	Open (Off)	Closed (On)
6	Closed (On)	Open (Off)	Open (Off)	Closed (On)
7	Open (Off)	Open (Off)	Open (Off)	Closed (On)
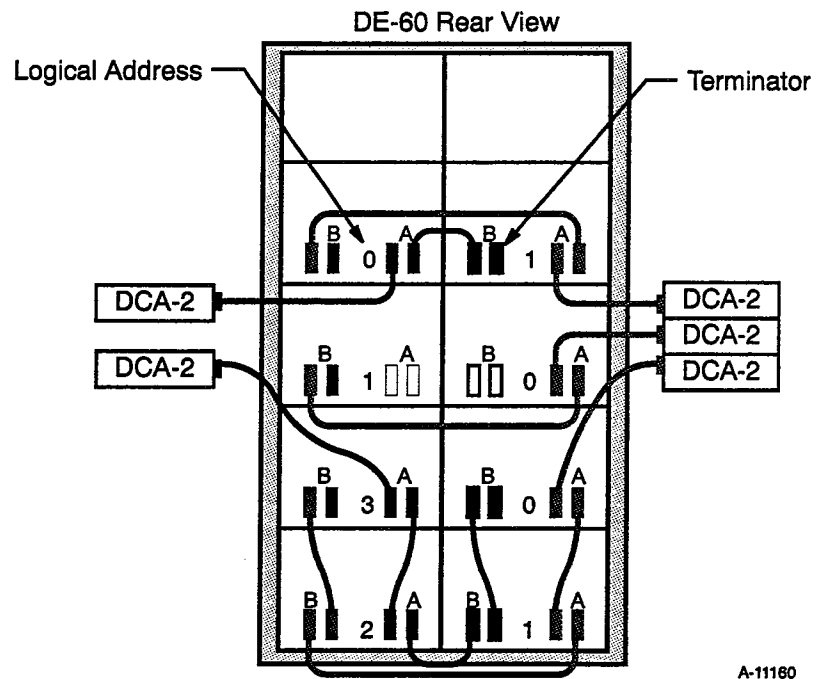
Figure 9-5. Logical Addresses of DCA-2 Drives in a DE-60

When a maintenance panel is connected to the disk drive, the SW3 DIP switches do not set the logical address. Refer to the "Maintenance Procedures" section for information on setting the logical address using the maintenance panel.

Disable Write Protection

Set this switch to the closed (On) position to disable write protection mode. If the write protection mode is enabled, data cannot be written to the disk drive.

Jumpers

The top panel jumpers change the modes of the sweep cycle and the runt sector pulse (refer to Figure 9-6 and Table 9-2).
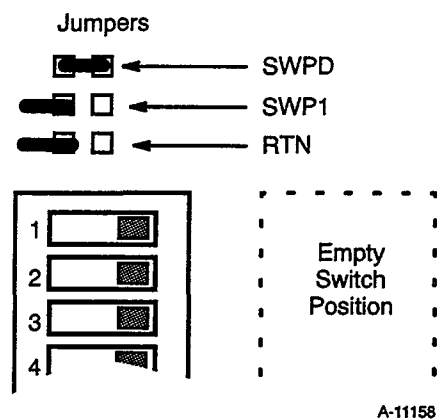
Figure 9-6. Top Panel Jumpers on the DD-62

Table 9-2. Top Panel Jumper Descriptions

Name	Description
SWPD	Connect this jumper to disable the sweep cycle. A sweep cycle moves the heads across the surface of the platter at least once every 12 minutes.
SWP1	Connect this jumper to disable the option for sweep cycles on seeks only.
RTN	Disconnect this jumper to disable the option to return the heads to their original position after a sweep cycle. This is a factory set position. Do not connect this jumper.

Internal Components

DD-62 and RD-62 disk drives are Sabre VII 2-head parallel disk drives. The Sabre VII disk drive contains three types of internal components: the circuit boards, head disk assembly (HDA) module, and power supply.

Circuit Boards

The DD-62 and RD-62 contain two circuit boards: a control board and an I/O board.

The control board directly controls most disk drive functions, which include read, write, seek, and spindle synchronization. It is mounted to the top of the HDA module and connects to the HDA module through pin connectors under the control board. Figure 9-7 shows the location of the control board relative to the HDA module.

The I/O board controls the disk drive input/output operations, which include selection of the DD-62 and RD-62. Figure 9-7 shows the location of the I/O board relative to the HDA module.
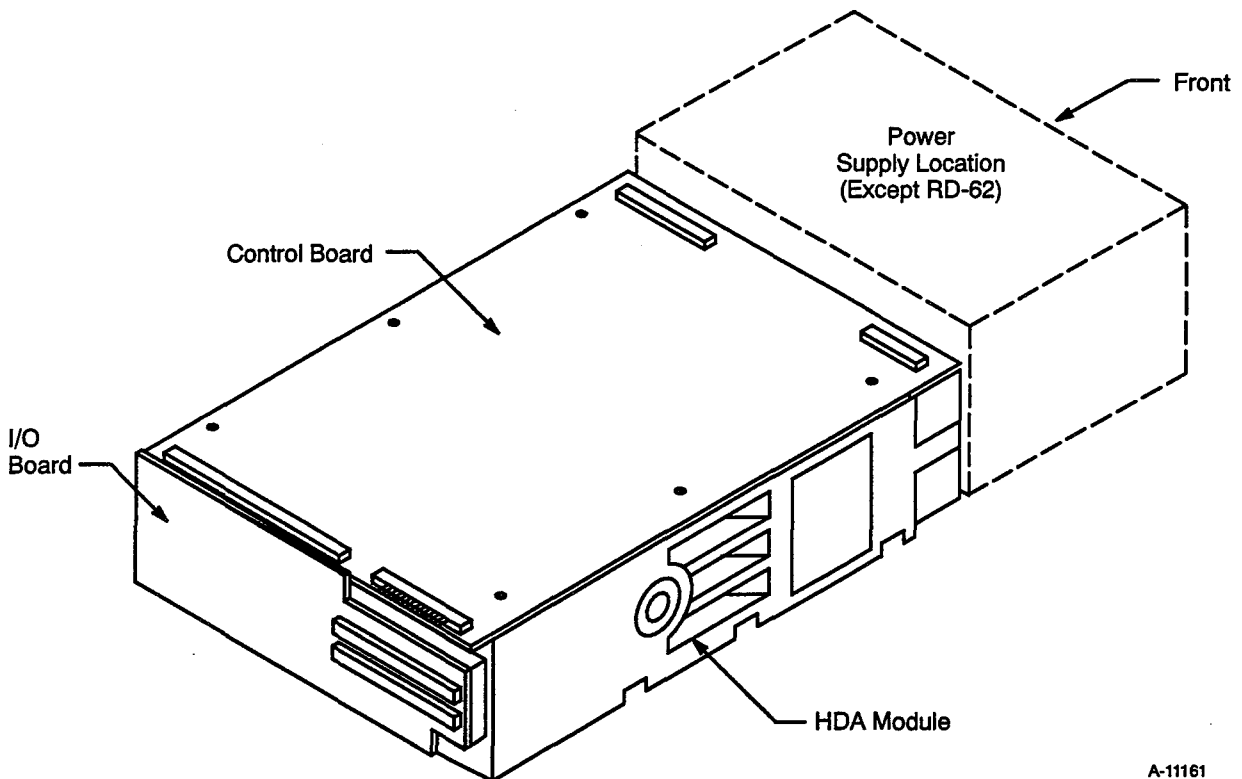
Figure 9-7. DD-62 and RD-62 Circuit Board Locations

Power Supply

The external power supply converts 115 Vac or 230 Vac into DC voltages. All components of the disk drive operate on DC voltage. These voltages are +5 Vdc, –5 Vdc, +12 Vdc, –12 Vdc, and +24 Vdc. Location of the power supply differs between the DD-62 and RD-62.

HDA Module

The HDA is a sealed module that contains the circuitry and hardware used to store information; this hardware includes platters, heads, an actuator, a spindle and spindle motor (refer to Figure 9-8).
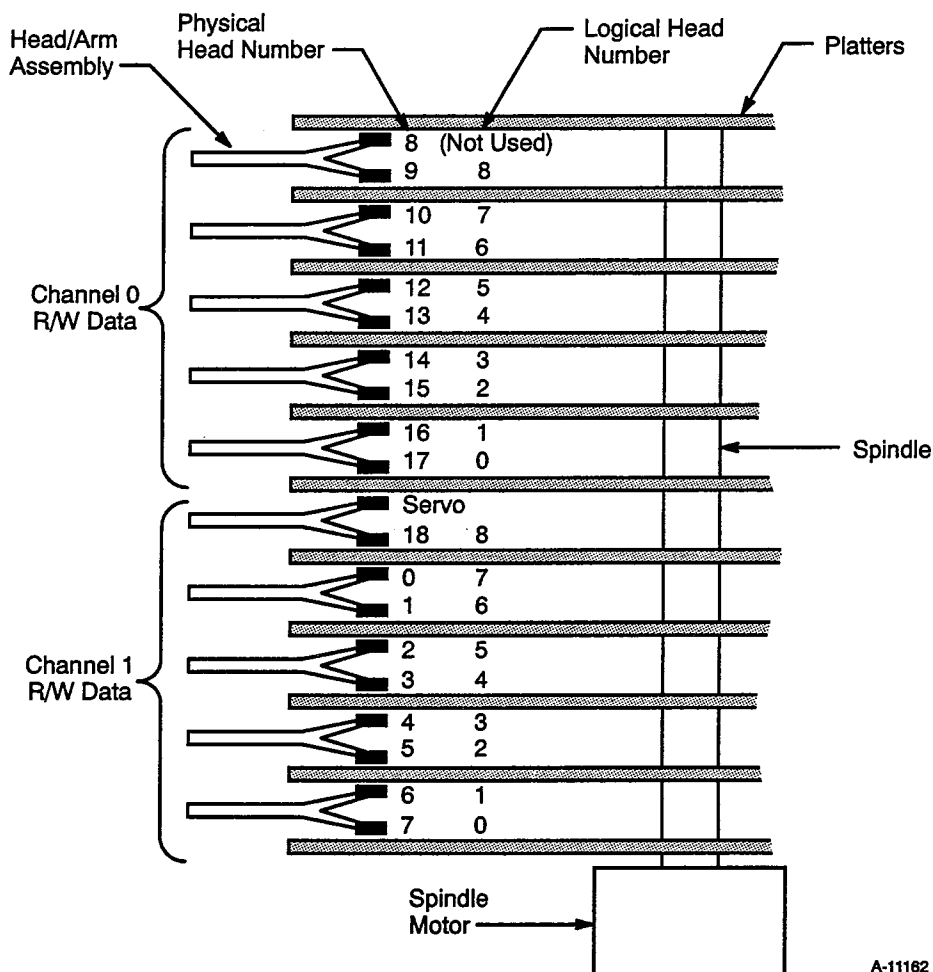
Figure 9-8. DD/RD-62 Physical Head Locations in the HDA

Platters

> The HDA module contains 11 platters that rotate at 4,365 revolutions per minute. Nine of the platters contain two thin-film media surfaces, while the top and bottom platters contain only one thin-film media surface (refer again to Figure 9-8).

Heads

> The heads transfer information to or from the media surface. One head transfers servo information, and nine head pairs transfer data (refer again to Figure 9-8).

Actuator

> The actuator positions the heads over any of the 2,655 tracks on the platter surface. The DD-62 and RD-62 disk drives have a balanced rotary actuator so the heads move in an arc over the platters.

Spindle and Motor

> The spindle attaches to the center of all the platters and holds them in place. It is directly connected to the spindle motor (refer again to Figure 9-8). The spindle motor is a 3-phase motor that rotates at 4,365 revolutions per minute (nominal). It is directly connected to the spindle and platter assembly (refer again to Figure 9-8). The spindle motor is controlled by a dedicated motor microprocessor unit (MPU). This dedicated MPU controls the motor via 3-phases of pulse-width modulated signals.

Maintenance Panel

> The maintenance panel can be connected to the front of the power supply and enables the user to set the logical address, examine statuses, view error logs, and run diagnostics. For more information on the maintenance panel, refer to the "Maintenance Procedures" section .

SECTION 10
DD-62 AND RD-62 FORMAT AND
FLAW MANAGEMENT

10 DD-62 AND RD-62 FORMAT AND FLAW MANAGEMENT

This section covers the format specifications and flaw management properties of the DD-62 and RD-62, including cylinder format, sector format, media flaws, and flaw maps and tables.

Cylinder Format

The DD-62 and RD-62 have 2,655 cylinders, including data cylinders, diagnostic cylinders, and a flaw table cylinder. Table 10-1 shows the addresses of these cylinders in decimal and octal.

Table 10-1. DD-62 and RD-62 Cylinder Map

Cylinder Type	Addresses
Data cylinders	0 - 2,651 0 - 5133_8
Diagnostic scratch cylinder	2,652 5134_8
IPI diagnostic cylinder	2,653 5135_8
User flaw table cylinder	2,654 (odd sectors) 5136_8 (odd sectors)
Factory flaw table cylinder	2,654 (even sectors) 5136_8 (even sectors)

Data cylinders store system data. Do not write data patterns to these cylinders unless the customer data is offloaded to an alternate location.

The diagnostic scratch cylinder is reserved for DD-62 and RD-62 diagnostics. Use this cylinder to read and write data patterns without destroying system data.

The IPI diagnostic cylinder is reserved for the disk drive. The internal read/write diagnostics use this cylinder during spin-up of the DD-62 and RD-62.

The flaw table cylinder contains both the factory flaw table and the user flaw table. For more information on flaw tables, refer to the "Flaw Maps and Tables" subsection later in this section.

Sector Format

After receiving information from a DCA-2 or DCA-3, the DD-62 (or RD-62 in DCA-2 applications only) stores the information in two physical sectors (one under each head in a head group). Figure 10-1 shows the format of a physical sector under one head in the head group.
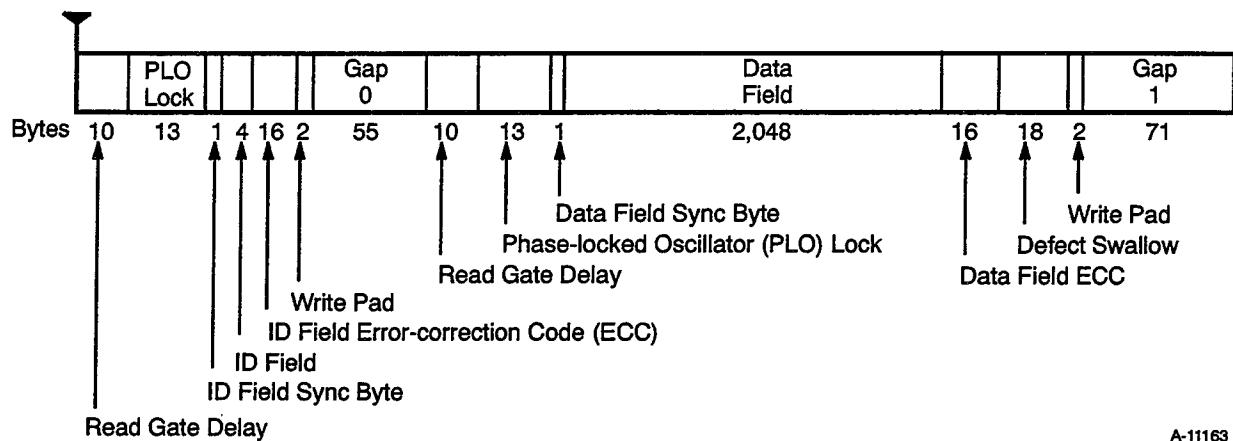
Figure 10-1. DD-62 and RD-62 Physical Sector Format

Each sector contains five field types: timing, data, ECC, defect swallow, and ID. Table 10-2 shows the relation between the size of a physical field and the logical size of the information from the two combined heads.

Table 10-2. DD-62 and RD-62 Sector Field Sizes

Sector Field	Physical Size in Bytes	Logical Size in Bytes
Read gate delay	10.0	N/A
PLO lock	13.0	N/A
ID field sync byte	1.0	N/A
ID	4.0	8.0
ID field ECC	16.0	32.0
Write pad	2.0	N/A
Gap 0	55.0	N/A
Data field sync byte	1.0	N/A

Table 10-2. DD-62 and RD-62 Sector Field Sizes (continued)

Sector Field	Physical Size in Bytes	Logical Size in Bytes
Data	2,048	4,096
Data field ECC	16.0	32.0
Defect swallow	18.0	36.0
Gap 1	71.0	N/A

Timing Fields

Timing fields create time delays for synchronization of the timing circuits during read or write operations. These fields are read gate delay, phase-locked oscillator (PLO) lock, sync bytes, write pad, gap 0, and gap 1.

For example, gap 0 provides a time delay for the DD-62 and RD-62 to interpret the next command (a read or write data field). Without this delay, the information stored in the data field would transfer to the channel adapter immediately after the ID information.

Data Field

The data field contains 2,048 bytes of system data. The DD-62 and RD-62 distributes 4,096 bytes of data received from the channel adapter into the 2 physical data fields.

ECC Fields

The ECC fields contain ECC generated by the channel adapter during a write data operation. Each physical sector contains 16 bytes of ECC for the ID field in that sector and 16 bytes of ECC for the data field in that sector. The channel adapter uses this information during a read operation.

During a read data operation, the channel adapter reads the data or ID field and generates a new ECC for that field from each physical sector. The channel adapter then compares the new ECCs to the information read from the sector ECC fields.

If the ID or data field ECCs do not match the generated ECCs, the channel adapter signals the EIOP that an error occurred. If the error occurred in the data field, the channel adapter can detect the bits that are incorrect and correct them.

Defect Swallow

The defect swallow allows the data field to expand if a hideable flaw is placed in the sector. For more information on defect swallow and hideable flaws, refer to the "Media Flaws" subsection in this section.

ID Field

The DD-62 and RD-62 store 8 bytes of logical ID information among the 2 physical ID fields. The ID information contains the logical sector address and media flaw information (refer to Figure 10-2). Table 10-3 describes each bit of the ID information.
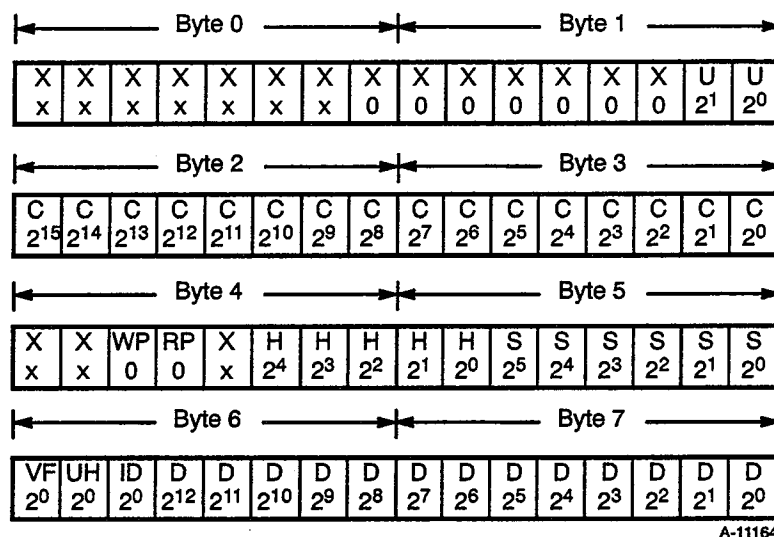
Figure 10-2. DD-62 and RD-62 Logical ID Information

Table 10-3. DD-62 and RD-62 Logical ID Information Description

Bit Symbol	Name	Description
X	Not used	This bit is not used.
U	Defective head	When set to 1, these bits indicate the physical head (head in head group) under which a media flaw exists.
C	Cylinder address	These bits contain the cylinder address of the data $(0 - 5136_8)$.
WP	Write protect (must be set to 0)	When set to 1, this bit indicates that data cannot be written to the sector unless this bit is also set in parameter register 1 (currently unused).
RP	Read protect (must be set to 0)	When set to 1, this bit indicates that data cannot be read from the sector unless this bit is also set in parameter register 1 (currently unused).

Table 10-3. DD-62 and RD-62 Logical ID Information Description (continued)

Bit Symbol	Name	Description
H	Head address	These bits contain the logical head address of the data $(0 - 10_8)$.
S	Sector address	These bits contain the sector address of the data $(0 - 33_8)$.
VF	Valid flaw	When set to 1, this bit indicates that the flaw in the sector is a known hideable flaw.
UH	Unhideable flaw	When set to 1, this bit indicates that the flaw in the sector is unhideable.
ID	ID field flaw	When set to 1, this bit indicates that the ID field contains an unhideable flaw.
D	Defect parameter	These bits contain the defect parameter. If the sector does not have a media flaw in the data field, the defect parameter is 1004_8.

The ID information is transferred between each disk drive and channel adapter in four 16-bit parcels on both bus A and bus B. For example, the first parcel transferred contains byte 0 and byte 1 of the logical ID information.

The entire logical ID information does not reside under an individual head in the head group. Each physical ID field contains 4 bytes of the information. The even-numbered bit of each byte transferred is stored under head 0 of the head group. The odd-numbered bit of each byte transferred is stored under head 1 of the head group.

During a write ID field operation, the DD-62 and RD-62 disk drives distribute the logical ID information to the 2 physical ID fields. After the 8 bytes of information are written to the disk drive, each physical ID field contains 4 bytes of the information. The even-numbered bits are written under head 0 of the head group, and the odd bits are written under head 1 of the head group. Figure 10-3 shows the ID fields for the 2 heads in a head group.

|←――― 1 Byte ―――→|←――― 1 Byte ―――→|←――― 1 Byte ―――→|←――― 1 Byte ―――→|

| X 0 | X x | X x | X x | U 2^0 | X 0 | X 0 | X 0 | C 2^8 | C 2^{10} | C 2^{12} | C 2^{14} | C 2^0 | C 2^2 | C 2^4 | C 2^6 | H 2^2 | H 2^4 | RP 0 | X x | S 2^0 | S 2^2 | S 2^4 | H 2^0 | D 2^8 | D 2^{10} | D 2^{12} | UH 2^0 | D 2^0 | D 2^2 | D 2^4 | D 2^6 |

ID Field under Head 0 of Head Group

|←――― 1 Byte ―――→|←――― 1 Byte ―――→|←――― 1 Byte ―――→|←――― 1 Byte ―――→|

| X x | X x | X x | X x | U 2^1 | X 0 | X 0 | X 0 | C 2^9 | C 2^{11} | C 2^{13} | C 2^{15} | C 2^1 | C 2^3 | C 2^5 | C 2^7 | H 2^3 | X x | WP 0 | X x | S 2^1 | S 2^3 | S 2^5 | H 2^1 | D 2^9 | D 2^{11} | ID 2^0 | VF 2^0 | D 2^1 | D 2^3 | D 2^5 | D 2^7 |

ID Field under Head 1 of Head Group
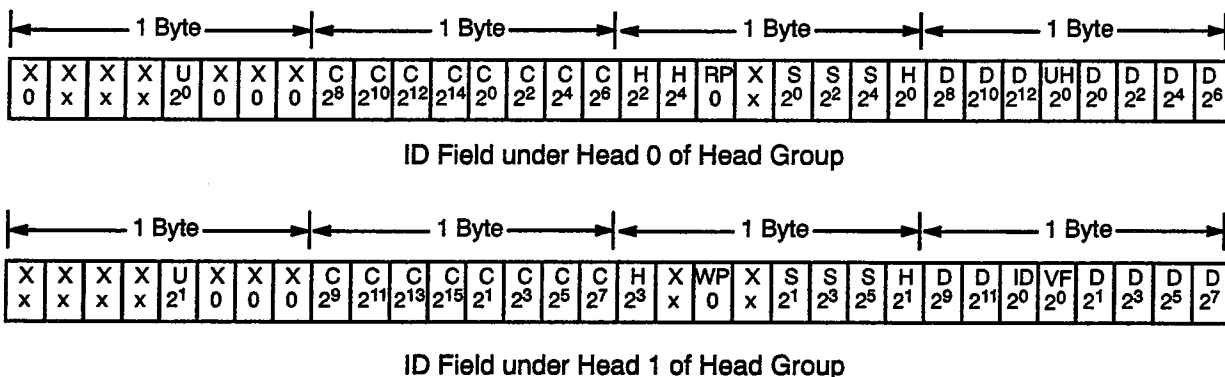
Figure 10-3. DD-62 and RD-62 Physical ID Fields

Media Flaws

A media flaw is a defect on the surface of a platter that does not allow the disk drive to read or write information correctly. Flaws are grouped into two categories: hideable flaws and unhideable flaws.

Hideable Flaws

A hideable flaw is a media defect in the data field that can be effectively covered by an 18-byte defect pad. The channel adapter creates this defect pad when it writes data to the disk drive.

Hiding a Media Flaw

When a media defect is found during surface analysis or from an error report, the cylinder, head, and sector address of the flaw is identified along with a defect parameter. The defect parameter for DD-62s and RD-62s represents the halfword (4-byte) boundary in the physical data field where the channel adapter starts to create an 18-byte defect pad.

Values for the defect parameter range from 0_8 to 1004_8 (0 to 516). The defect parameter, or location of the start of the defect pad, is calculated so that the 18-byte pad most effectively covers over the media flaw. For example, if a media flaw is located at byte 50_8, the defect parameter for this flaw is 10_8 (refer to Figure 10-4).
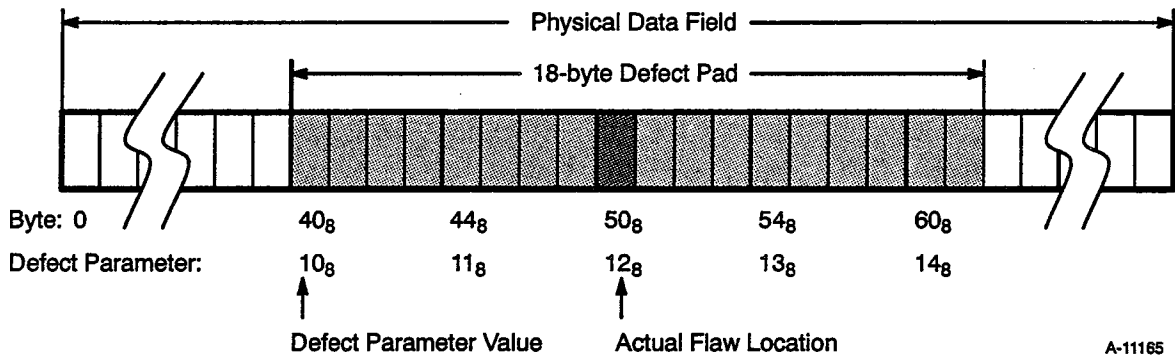
Figure 10-4. Defect Parameter and Actual Flaw Locations in a DD-62 and RD-62 Data Field

Before a write data field operation begins, the defect parameter is read from the sector ID field and transferred to a register in the channel adapter (refer again to Figure 3-1). The data parcel counter in the channel adapter is reset to 0.

The channel adapter uses a parcel counter to count each parcel of data as it is transferred to the disk drive. To count each 64-bit word (or 4 parcels) of data sent to the disk, the channel adapter disregards bits 2^0 and 2^1 of the parcel counter. Because the DD-62 and RD-62 use 2 parallel heads to write data, one 64-bit word of data sent to the disk drive is equivalent to 32 bits (4 bytes) of data under each head of the head group.

When the value of the word count (from the parcel counter) is equivalent to the defect parameter, the channel adapter halts the parcel counter and starts decrementing a defect counter.

While the defect counter is decrementing, the channel adapter signals the EIOP buffer board to halt the transfer of write data. Because the channel adapter does not receive new data, it repeatedly transfers the previous parcel (for DCA-2) or next parcel (for DCA-3) of data to the disk drive. This continues until 18 repeated parcels of data are sent to the disk drive.

By sending 18 repeated parcels of data to each disk drive, the channel adapter creates an 18-byte defect pad in the same location under each of the 2 parallel heads. Each 2 parcels sent to a physical sector/head correspond to one 64-bit word sent to the disk drive (refer to Figure 10-5).

Physical Sector/ Head	18-byte Physical Defect Pad		
	Byte 0 of Physical Defect Pad	Byte 1 of Physical Defect Pad	
0	V^{12} V^{14}	R^0 R^2 R^4 R^6 R^8 R^{10} R^{12} R^{14}	R^0 R^2 R^4 R^6 R^8 R^{10} R^{12} R^{14}	R^0
1	V^{13} V^{15}	R^1 R^3 R^5 R^7 R^9 R^{11} R^{13} R^{15}	R^1 R^3 R^5 R^7 R^9 R^{11} R^{13} R^{15}	R^1

End of Valid Data Parcel   Repeated Logical Parcel   Repeated Logical Parcel

A-11166
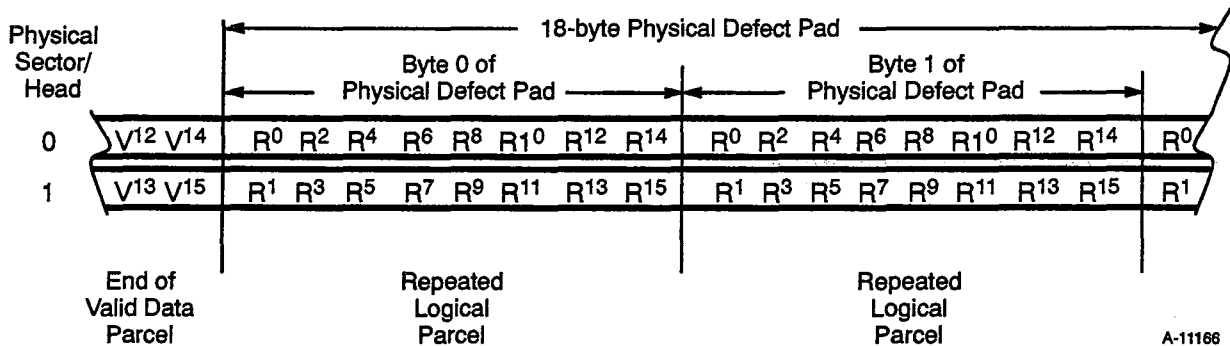
Figure 10-5. Bytes 0 and 1 of the Physical Defect Pad

After creating the defect pads, the channel adapter restarts the parcel counter and signals the EIOP buffer board to resume the transfer of write data. This continues until all of the data for the logical sector is sent to the disk drive.

Sector Format with a Hideable Flaw

When a defect pad is inserted into a physical sector, the physical length from the start of the data field to the end of the data field increases from 2,048 bytes to 2,066 bytes. The defect pad resides over the data field flaw while the channel adapter overwrites the defect swallow with data. Figure 10-6 shows the format of a physical sector with a hideable flaw.
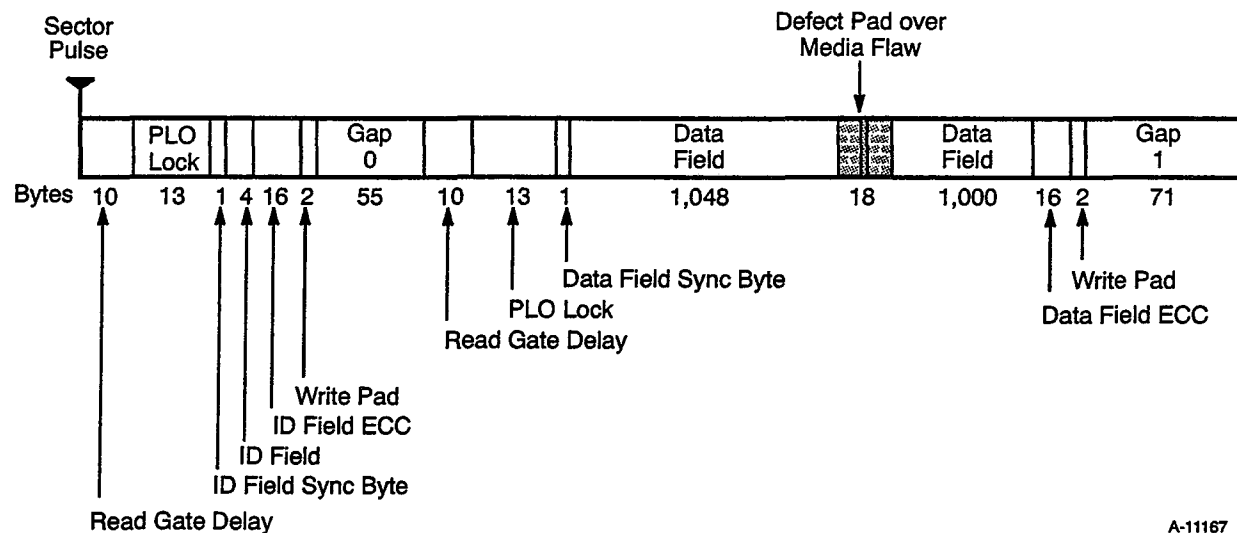
Figure 10-6. DD-62 and RD-62 Physical Sector with a Hideable Flaw

Both physical sectors must have a defect pad in the same location as the sector that has a media flaw. Therefore, the logical size of a defect pad is 36 bytes.

Hiding Multiple Media Flaws in One Logical Sector

Two flaws in the same sector under separate physical heads may be covered by one defect pad. If the combined flaws do not have the properties of an unhideable flaw, the channel adapter can create a defect pad to cover the combined flaws. Figure 10-7 shows one defect pad covering two physical sector flaws.
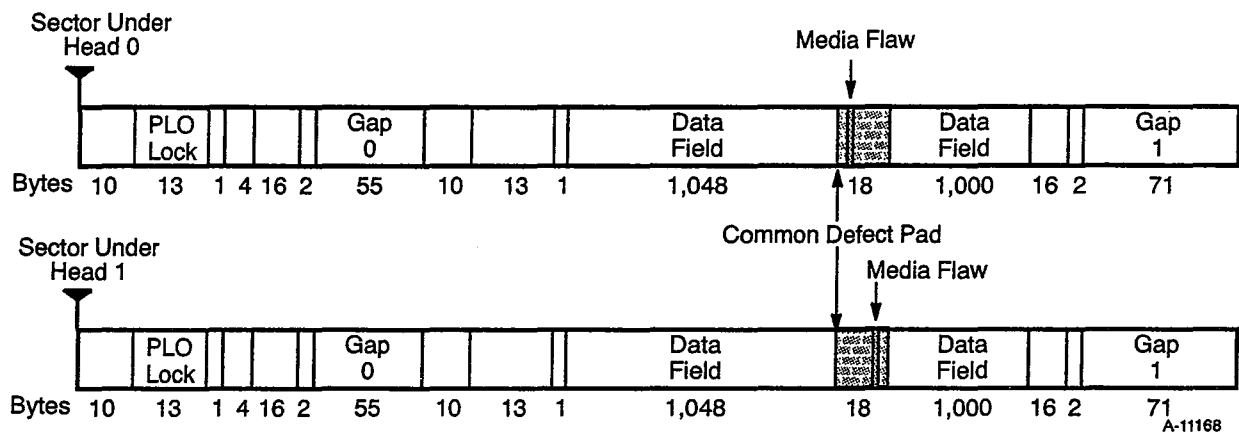
Figure 10-7. Two Physical Sectors with Hideable Flaws Covered by One Defect Pad

Reading a Sector with a Hideable Flaw

Before performing a read data field operation, the channel adapter reads the sector ID field and stores the defect parameter in a register. The channel adapter then resets the parcel counter (refer again to Figure 3-1).

The channel adapter uses the parcel counter to count each parcel of data as it is transferred from the disk drive. To count each 64-bit word (or 4 parcels) of data read from the disk drive, the channel adapter disregards bits 2^0 and 2^1 of the parcel counter. Because the DD-62 and RD-62 use 2 parallel heads to read data, one 64-bit word of data from the disk drive is equivalent to 32 bits of data from each physical data field.

When the value of the word count (from the parcel counter) is equivalent to the defect parameter, the channel adapter halts the parcel counter and starts decrementing a defect counter.

While the defect counter is decrementing, the channel adapter rejects the data parcels read from the defect pad area. This process continues until the 18 parcels of the defect pad are transferred from the disk drive to the channel adapter.

After all of the repeated data is transferred, the channel adapter restarts the parcel counter and resumes the acceptance of data parcels from the disk drive. This process continues until the rest of the data field is transferred to the channel adapter.

Unhideable Flaws

An unhideable flaw is a media flaw that cannot be hidden by a defect pad. If an unhideable flaw occurs, the entire sector is unable to store data. Any sectors that contain an unhideable flaw are marked by the operating system as unusable sectors. The following list describes some of the conditions that create an unhideable flaw.

- A flaw exists in the first 8 bytes of the data field.

- A flaw exists outside of the data field of a sector (such as ID or sync byte fields).

- A flaw is longer than 32 bits.

- Two or more flaws exist under each head of the head group and the combined flaw cannot be covered by one defect pad.

Flaw Maps and Tables

Flaw maps and tables store the locations of media flaws in the DD-62 and RD-62. The maps and tables include a factory flaw map, a user flaw table, and a UNICOS flaw map.

Factory Flaw Table

When Cray Research, Inc. (CRI) purchases a Sabre VII two-head parallel (2HP) disk drive, it contains a factory flaw table on the even-numbered sectors of cylinder 2,654 (5136_8). The factory flaw table lists the physical locations of all the flaws found during manufacturing checkout. This information is used when the DD-62 and RD-62 are initially formatted.

User Flaw Table

The user flaw table contains a list of all the flaws, hideable and unhideable, including those added since the disk drive was initially formatted. It is located on the odd-numbered sectors of cylinder 2,654 (5136_8). Update the user flaw table every time you add a flaw to a sector in the DD-62 and RD-62. Table 10-4 shows the format of the user flaw table.

Table 10-4. User Flaw Table Format

Word	Parcel	Description
0	0	Cray Research, Inc. serial number in ASCII (bits 2^{63} through 2^{48})
	1	Cray Research, Inc. serial number in ASCII (bits 2^{47} through 2^{32})
	2	Cray Research, Inc. serial number in ASCII (bits 2^{31} through 2^{16})
	3	Cray Research, Inc. serial number in ASCII (bits 2^{15} through 2^{0})
1	0	HDA serial number in hexadecimal (bits 2^{31} through 2^{16})
	1	HDA serial number in hexadecimal (bits 2^{15} through 2^{0})
	2	Not used
	3	Date of recording in hexadecimal (bits 2^{15} through 2^{0})
2 through last entry	0	Flaw ID field parcel 0 (refer to Figure 6-2)
	1	Flaw ID field parcel 1 (refer to Figure 6-2)
	2	Flaw ID field parcel 2 (refer to Figure 6-2)
	3	Flaw ID field parcel 3 (refer to Figure 6-2)
Terminator	0	All 1's
	1	All 1's
	2	All 1's
	3	All 1's

UNICOS Flaw Map

The UNICOS flaw map is used by the operating system to locate sectors that contain unhideable flaws. If a sector is unusable, the operating system can remap the logical sector to another location in the DD-62 and RD-62. For DCA-3 applications, a sector which is unusable on one spindle will be marked by the operating system as unusable on all 5 spindles in the array.

NOTE: System flaw tables (sometimes referred as O.S. flaw tables or Engineering flaw tables) do not apply to the 60 series disk drives. Cylinder 0, which was previously used to store the system flaw tables, is a customer cylinder on these drives.

SECTION 11
RDE-6 REMOVABLE DISK ENCLOSURE

11 RDE-6 REMOVABLE DISK ENCLOSURE

This section describes the RDE-6 removable disk enclosure. It provides an overview of the RDE-6, as well as descriptions of component locations, bulkhead connection and cabling, cabinet locking mechanisms, drawer insertion and removal, and service information.

RDE-6 Overview

The RDE-6 cabinet is designed to house up to four RD-62 disk drives. In addition to providing the power and cooling requirements for the RD-62 disk drives, the RDE-6 cabinet also provides for easy insertion and removal of these drives through matched drawer and chassis subassemblies.

The controller accesses each RD-62 disk drive through a single port connection on the back of the RDE-6 cabinet. A separate DCA-2 channel adapter is required for each RD-62 (refer to Figure 11-1).
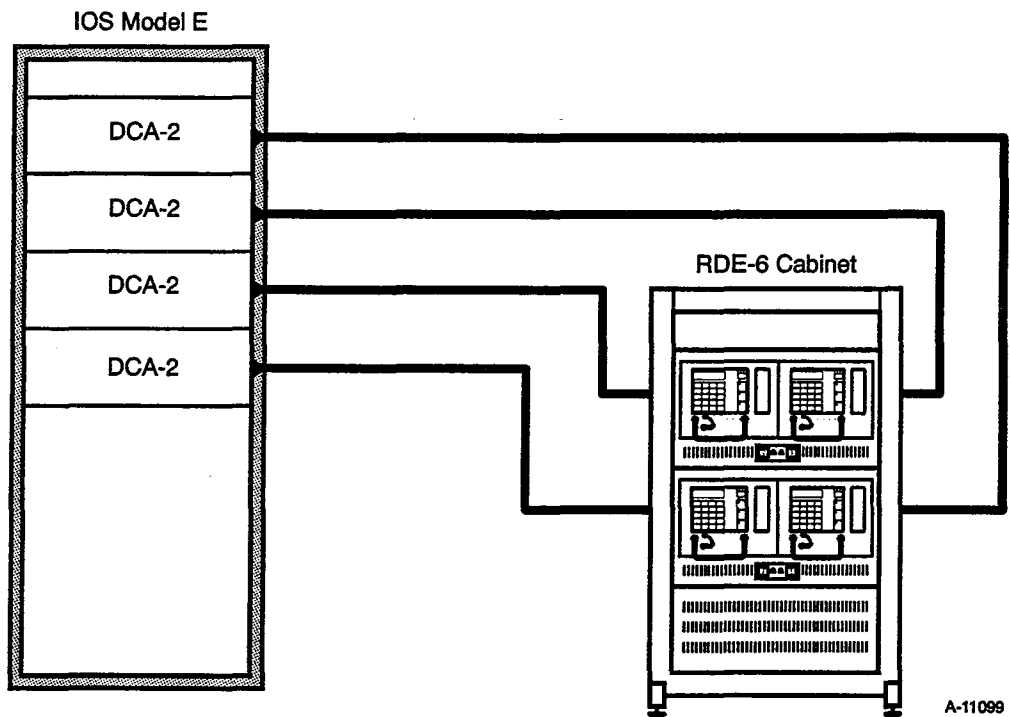
Figure 11-1. RD-62 Cabling Configuration

RDE-6 Component Locations

Figure 11-2 shows the RDE-6 component locations as viewed from the front of the RDE-6 cabinet. Each RDE-6 cabinet contains a total of two chassis; each chassis contains two drawers, and each drawer contains an RD-62 spindle. A drawer assembly containing an RD-62 spindle is referred to as an RD-62 disk drive. Refer to Table 11-1 and Table 11-2 for descriptions of the RDE-6 indicators and switches.
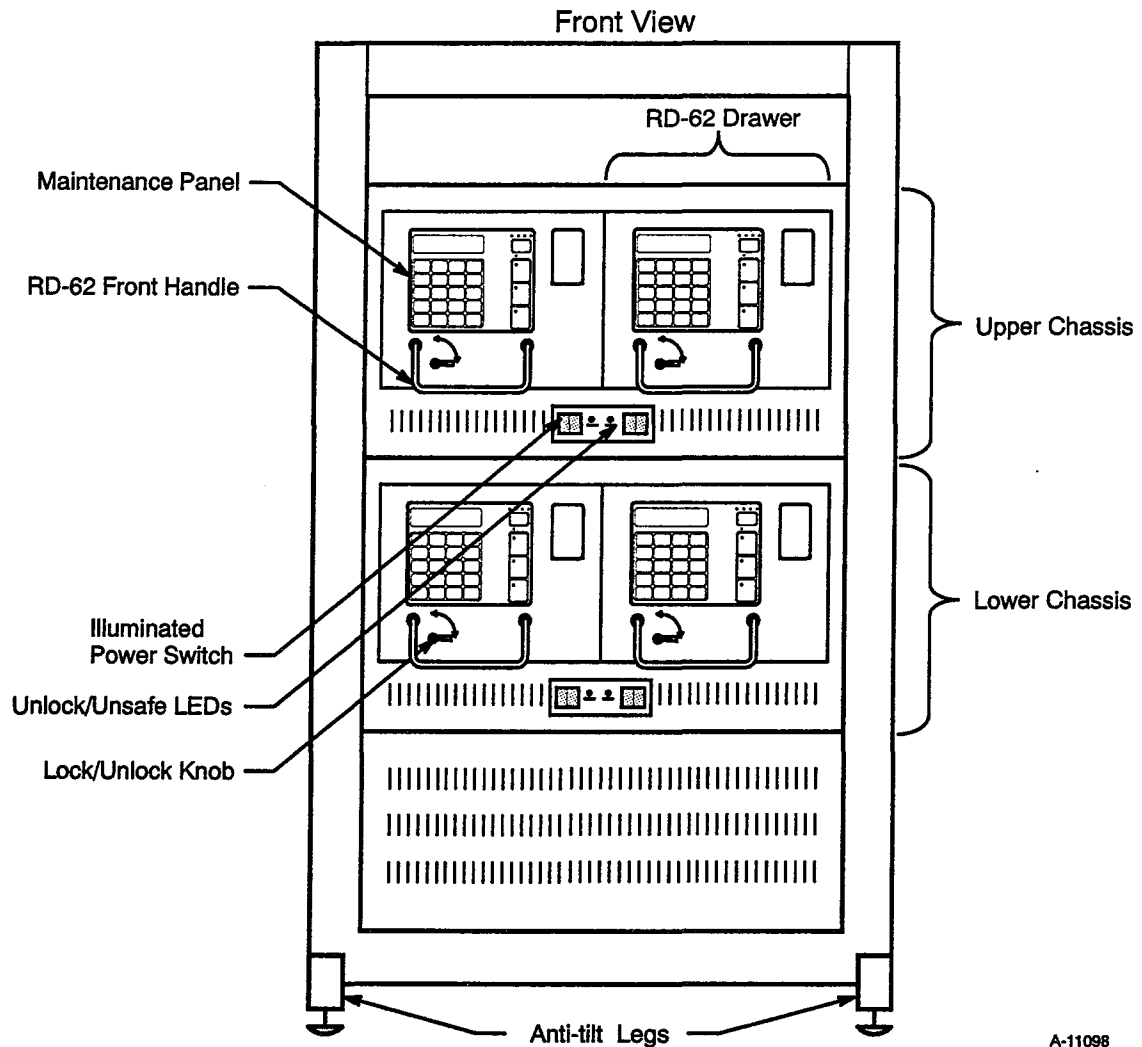
Figure 11-2. RDE-6 Cabinet

Table 11-1 defines the indicators on the front of the RDE-6 cabinet. An RDE-6 can have a maximum of four sets of these indicators, one for each RD-62 drawer in the RDE-6 cabinet. Refer to Figure 11-2 for the locations of these indicators.

Table 11-1 RDE-6 Indicators

Description	Location	Function
Illuminated Power switch	Illuminated rocker switches on front of chassis	The AC power interlock is engaged. AC power is supplied to the RD-62 power supply.
Unlock LED	Between illuminated rocker switches	On – Solenoid is unlocked. Off – Solenoid is locked.
Unsafe LED	Between illuminated rocker switches	Steady light– Power is applied to the drive. It is not safe to remove the drawer. Flashing light – The drive is in a spin-down sequence. It is not safe to remove the drawer. No light – The drive has spun down; power is removed from the drive. It is safe to remove the drawer.
Maintenance panel	Front of drawer	Refer to the "Maintenance Procedures" section

Table 11-2 defines the switches contained within the RDE-6 cabinet. The RDE-6 can contain a maximum of four sets of these switches, one for each RD-62 drawer within the RDE-6 cabinet. Figure 11-3 is a schematic of the interlock switches and indicators.

Table 11-2. RDE-6 Switches

Description	Location	Function
Illuminated Power switch	Illuminated rocker switches on front of chassis	In the ON position, AC power is applied to the RD-62 DC power supply. In the OFF position, AC power is removed from the RD-62 DC power supply.
AC Interlock microswitch (activated by Lock/Unlock knob)	Under solenoid cover in bottom of chassis	This microswitch enables power to be supplied to the front panel power switch if the drawer is properly installed and locked.
RD-62 Power supply switch	Front of RD-62 power supply	This microswitch enables AC into the RD-62 power supply. This switch is always in the ON position.

RDE-6 Cabinet Locking Mechanisms

Several features are designed into the RDE-6 chassis assemblies to prevent damage to the RD-62 and aid in the insertion and removal of the RD-62 drawer. The following paragraphs describe the operational characteristics of these safety features. The exact procedures for inserting and removing the RD-62 are provided later in this section.

As the RD-62 drawer is slid into the chassis receiver, a shutter assembly actuator passes through a hole located in the rear of the drawer and pushes the shutter out of the way of the flag cutout (located on the bottom of the drawer). When this occurs, the Unlock LED illuminates.

When the Lock/Unlock knob located on the drawer front panel is rotated approximately 90 degrees clockwise, the two halves of the zero insertion force (ZIF) connectors lock together. As the ZIF shaft rotates, it passes through the cutout in the bottom of the drawer and into the cutout in the solenoid assembly cover. Near the end of this rotation, the flag comes into contact with an AC interlock switch roller and depresses a micro switch. This enables AC power to pass from the power controller assembly to the Illuminated Power switch located on the front of the chassis (refer to Figure 11-3).

With the ZIF connector locked and the AC Interlock microswitch closed, the front panel Power On switch may be toggled to the ON position. The Power On switch immediately illuminates to indicate that AC power is now applied to the RD-62 DC power supply. After two to three seconds, the locking solenoid engages, moves the solenoid link in front of the ZIF shaft flag, and prevents the Lock/Unlock knob from being rotated to the Unlock position. The Unsafe LED illuminates and the Unlock LED is no longer illuminated.

Before the RD-62 drawer can be removed from the chassis, the illuminated front panel Power On switch must be toggled to the OFF position. The Unsafe LED then flashes to indicate that a transition is occurring. After 50 to 60 seconds, the solenoid disengages, enabling the Lock/Unlock knob to be rotated. The Unsafe LED stops flashing, indicating that the solenoid circuit has attempted to disengage the solenoid link. The Unlock LED monitors the physical position of the solenoid link through a photocell and should illuminate, indicating that the solenoid successfully disengaged. After rotating the Lock/Unlock knob approximately 90 degrees counterclockwise, you can safely removed the RD-62 drawer from the chassis receiver. Refer to the "Drawer Insertion/Removal Procedures" in the following pages.
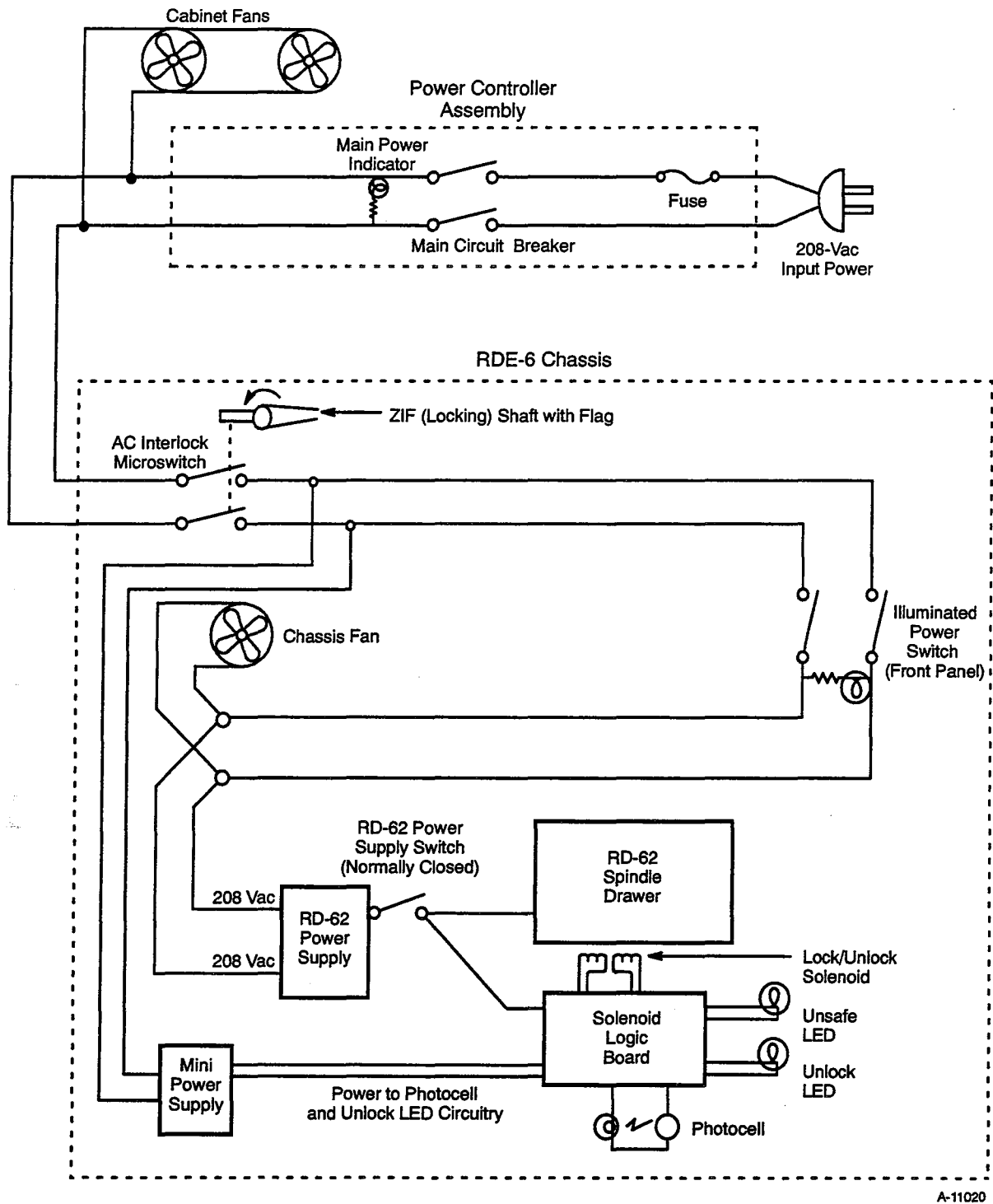
Figure 11-3. RDE-6 Chassis Interlock Switches and Indicators

RDE-6 Bulkhead Connections and Cabling

Figure 11-4 shows component locations as viewed from the rear of the RDE-6 cabinet. Each chassis assembly contains two RD-62 drawers, two sets of I/O connections, and two cooling fans. The main power-distribution assembly is located at the bottom of the cabinet. This assembly distributes the input power to the individual drive power supplies, cooling fans, and solenoid assemblies within the cabinet.
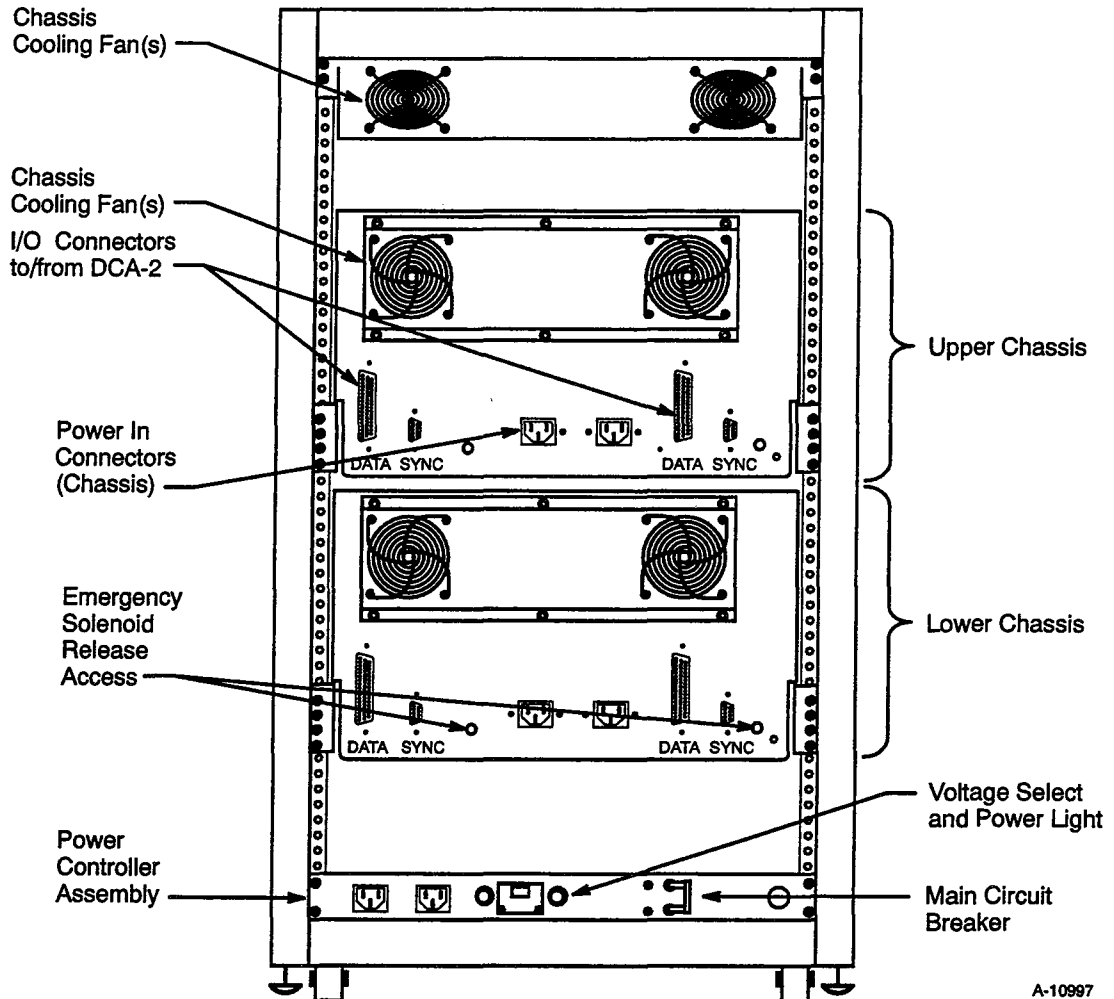
Figure 11-4. RDE-6 Cabinet (Rear)

RDE-6 Drawer Insertion/Removal Procedures

Refer to the following subsections for information on RDE-6 drawer insertion/removal procedures.

CAUTION

Perform RDE-6 drawer insertion and removal procedures exactly as they are described. Failure to do so can result in damage to the RD-62 disk drive.

Drawer Insertion Procedure

Perform the following steps to insert an RD-62 drive into an RDE-6 cabinet.

1. Before attempting to insert an RD-62 drawer into an RDE-6 cabinet, ensure that the following conditions are met for that drawer.

    -   Front panel Power switch is not illuminated
    -   Unsafe LED is not illuminated
    -   Unlock LED is illuminated

CAUTION

The RD-62 spindle/drawer assembly is very heavy. Use caution when handling it to avoid dropping it. Failure to do so could result in damage to the chassis and/or RD-62 disk drive.

---

2. Holding the drawer by the front and top handles, lift and insert the back of the drawer into the cabinet receiver. Ensure that both of the drawer runners rest on the receiver ledges.

3. Slide the drawer in until the assist (upper) handle reaches the bezel.

4. Release the assist handle and rotate it downward until it clears the bezel.

5.   Slide the drawer into the receiver the rest of the way until it stops against the bulkhead.

6.   Rotate the Lock/Unlock knob to the lock position.

7.   Push the Power switch to the ON position to apply AC power.

8.   Listen for the sound of the solenoid engaging 2 to 3 seconds later and verify that the Power switch and Unsafe LED are illuminated. Verify that the Unlock LED is not illuminated.

9.   Press the Start switch on the maintenance panel to spin up the RD-62.

Drawer Removal Procedure

Perform the following steps to remove an RD-62 drive from an RDE-6 cabinet.

1.   Press the Start switch on the maintenance panel to spin down the RD-62.

2.   Push the illuminated Power switch to the Off position to remove AC power from the drawer.

3.   Verify that the Power switch is not illuminated and that the Unsafe LED is flashing.

4.   In approximately 50 to 60 seconds, you will hear a sound as the locking solenoid releases, and the Unsafe LED is no longer illuminated. The Unlock LED must illuminate before the Lock/Unlock knob can be rotated.

5.   Rotate the Lock/Unlock knob to the Unlock position.

     NOTE: If the Unlock LED fails to illuminate, there may be a problem with the solenoid assembly. If the solenoid fails to unlock, insert a small screwdriver into the emergency solenoid release access holes located on the rear of the chassis. This action manually releases the locking solenoid and allows you to remove the drawer. Refer to Figure 11-4 for the location of the emergency solenoid release access holes.

6. Before attempting to remove an RD-62 drawer from an RDE-6 cabinet, ensure that the following conditions are met for that drawer.

- Front panel Power switch is not illuminated
- Unsafe LED is not illuminated
- Unlock LED is illuminated

CAUTION

The RD-62 disk drive weighs approximately 40 pounds. Use care when handling the RD-62 disk drive. Failure to do so could result in damage to the chassis and/or RD-62 disk drive.

---

7. Holding the front handle, slide the drawer out of the receiver until the upper assist handle catch clears the rear of the bezel.

8. Rotate the upper assist handle upward until the catch disengages from the rear of the bezel.

9. With a firm grasp on both handles, slide the drawer the rest of the way out of the receiver.

RDE-6 Servicing Information

The following subsections provide RDE-6 servicing information.

RDE-6 and RD-62 Parts List

Table 11-3 lists the field replaceable spare parts for the RDE-6 enclosure and the RD-62 removable disk drive.

Table 11-3. RDE-6 and RD-62 Parts List

Description of Spare Parts	CRI Part Numbers
RD-62 drawer assembly (not including spindle)	01725300
RD-62 spindle assembly (not including drawer)	01737500
Chassis ZIF connector cable	01757100
Power controller assembly	01757300
Solenoid assembly (logic board)	01757400
Solenoid assembly (mechanical)	01757500
LED and cable	01757600
Cooling fan	01754500
RD-62 DC power supply	01488200
RD-62 I/O board (IPI-2)	01752300
RD-62 control board	01752200

NOTE: The entire RD-62 drawer assembly (CRI part number 01725300) should be considered a field replaceable unit (FRU). Replacement of parts within the drawer is not recommended, due to extremely critical alignment tolerances within the drawer assembly. These replacement parts include the ZIF cable within the drawer, the maintenance (operator) panel, and the maintenance panel cable (refer to Figure 11-5). Correct a failure of any of these parts by removing the RD-62 spindle from the affected drawer assembly and installing the spindle into a replacement drawer assembly.

For additional information on spindle and drawer replacement, refer to the "Spindle and/or Drawer Replacement Procedures" on the following pages.

Spindle and/or Drawer Replacement Procedures

Any failure of a drawer component makes it necessary to replace the entire drawer assembly (refer to Figure 11-5). Failure of the spindle within the drawer assembly also requires removing the spindle from the drawer and replacing it with a new spindle. Perform the following steps to replace a defective drawer or a defective spindle.

CAUTION

Wear an electrostatic discharge (ESD) smock, wrist strap, and ESD shoes during the installation or replacement process. Damage to the disk drive equipment will result if these precautions are not followed.

---

1. Remove the defective RD-62 drawer from the RDE-6 cabinet using the "Drawer Removal Procedure" in the previous subsection. Place it on a static-free work surface. Position the drawer to provide easy access to the back of the assembly.

2. Remove the spindle sync cable from connector J50 located below the fan.

3. Remove the power input cable from the upper edge of the spindle.

4. Remove the IPI terminator from the J3-1 connector on the back of the spindle.

5. Remove the I/O (data) cable from the J4-1 connector on the back of the spindle. Do not pull on the cable wires.

6. Turn the drawer onto one side with the front of the drive facing away from you and the bottom of the drawer facing toward you. Remove the front and rear shock mount screws from the side.

7. Turn the drawer over onto the other side with the top of the drive facing toward you. Remove the front and rear shock mount screws from this side.

8. Slowly rotate the back of the spindle toward you until it is partially removed from the drawer assembly. Remove the allen screw and lock washer located just before the front shock mount on the ground strap. Be sure to keep this screw and lock washer for later use.

9.   Pull the spindle away from the front of the drawer assembly far
     enough to allow access to the cables in front of the spindle.

10. Remove the power test-point cable from the J15A connector on the
     front of the spindle. Remove the maintenance panel cable from the
     J13 connector on the front of the spindle.

11. Now, completely remove the spindle from the drawer assembly.

12. If replacing a defective spindle, unbox the new spindle and inspect
     it for any damage. Check that all DIP switch settings are correct
     (refer to the "DD-62 and RD-62 Hardware Description" earlier in
     this manual). Reverse the previous steps (beginning with Step 11
     and finishing with Step 1) to complete installation of the new
     spindle into the drawer assembly.
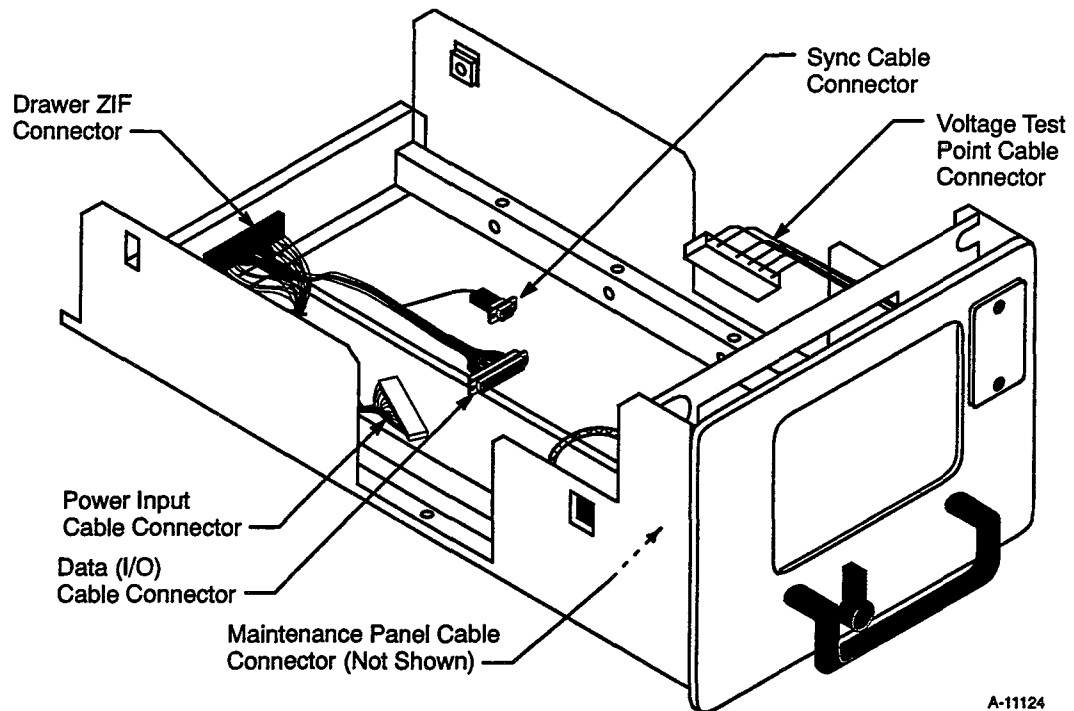
Figure 11-5. RD-62 Drawer Assembly (not including spindle)

13. If replacing a defective drawer assembly, remove the new drawer
     assembly from the shipping box and verify that the following
     accessories are included.

     •   Drive lift plate with handle and mounting screws
     •   Drive mounting screws
     •   Ground strap screw and nut
     •   Interface cable fasteners

> NOTE: Inspect the drawer and verify that the shutter return
> spring did not loosen during shipment.

14.   Reverse the previous steps (beginning with Step 11 and finishing
      with Step 1) to complete installation of the spindle into the
      replacement drawer assembly.

15.   Use the "Drawer Insertion Procedure" in the previous subsection.

RDE-6 Chassis Removal and Access

This subsection provides procedures to allow replacement of components
within the RDE-6 chassis. Always remove the RD-62 drives before
servicing the RDE-6 cabinet. Follow all procedural steps in the order
given unless specifically instructed to do otherwise.

WARNING
Remove all power connections from the RDE-6 cabinet before attempting to service the chassis assembly. Failure to do so could result in serious injury or death because the 208–240 volt connections are exposed.

CAUTION
Wear an electrostatic discharge (ESD) smock, wrist strap, and ESD shoes during the installation or replacement process. Damage to the disk drive equipment will result if these precautions are not followed.

1.   Remove the anti-tilt leg-retaining bolts from the lower front sides
      of the cabinet and extend the legs approximately 18 inches (refer
      again to Figure 11-2). Re-insert the retaining bolts to lock the
      anti-tilt legs in the extended position.

┌───┐
│   **CAUTION**   │
├───┤
│ **Before attempting to access the chassis inside the** │
│ **RDE-6 cabinet, remove all RD-62 drives and ensure** │
│ **that the anti-tilt legs have been properly extended.** │
│ **Failure to do so can cause the RDE-6 to tip forward,** │
│ **resulting in damage to the chassis assemblies** │
│ **and/or cabinet.** │
└───┘

2. Open the rear door of the cabinet by pressing the short portion of the latch and pulling the long portion toward you to expose the internal components located at the rear of the cabinet.

3. Remove the four screws from the chassis restraint bracket on the right rear side of the chassis.

4. From the front of the cabinet, pull the chassis out until the slide locks engage.

5. Remove the four screws that secure the chassis top cover (refer to Figure 11-6).

6. Remove the chassis top cover by lifting up the front of it and pulling it forward after the lip of the top cover has cleared the front bezel as shown in Figure 11-6.

7. Reverse the actions listed above (beginning with Step 6 and finishing with Step 1) to reassemble the chassis.
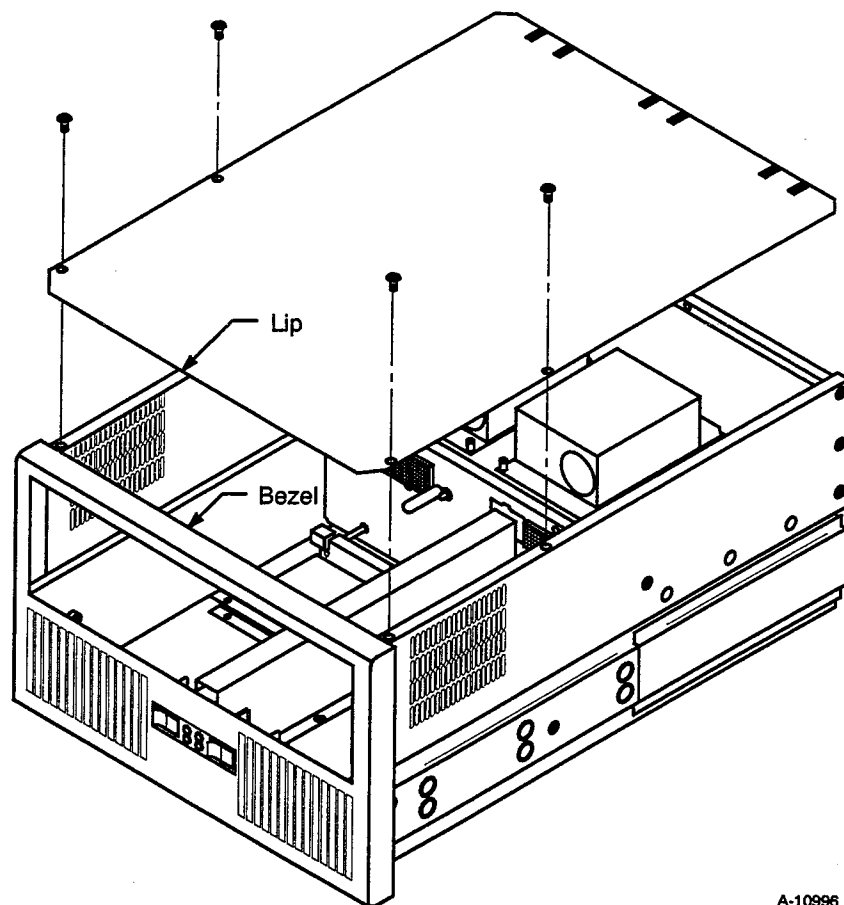
A-10996

Figure 11-6. RDE-6 Chassis Top Cover Removal

RDE-6 Power Controller Assembly Replacement Procedures

Perform the following steps to replace an RDE-6 power controller assembly. Refer to Figure 11-4 for the location of the power controller assembly.

1. Open the rear door of the cabinet by pressing the short portion of the latch and pulling the long portion toward you to expose the internal components.

2. Locate the main circuit breaker switch located in the rear center of the power controller assembly and toggle it to the OFF position.

3. Disconnect the RDE-6 main power input cable from the power source connection.

	WARNING	
Remove all power connections from the RDE-6 cabinet before attempting to service the solenoid assembly. Failure to do so could result in serious injury or death because the 208–240 volt connections are exposed.		

4. Remove the four screws (two on each side) securing the power controller assembly to the RDE-6 cabinet rails.

5. Pull the power controller assembly slowly toward you until the cables on the back are accessible.

6. Disconnect the four drive power cables, the fan power cable, and the main power input cable located on the back of the power controller assembly.

7. Remove the defective power controller assembly from the RDE-6 and position the replacement assembly in the rear of the cabinet.

8. Reverse the previous steps (beginning with Step 6 and finishing with Step 1) to complete installation of the replacement power controller.

RD-62 Power-supply Replacement Procedures

A failed RD-62 power supply can be verified by using the voltage test points located on the front of the drawer assembly. The voltage values and tolerances are shown in Figure 11-7. If the voltage values do not meet specifications, perform the following steps to replace the RD-62 power supply.

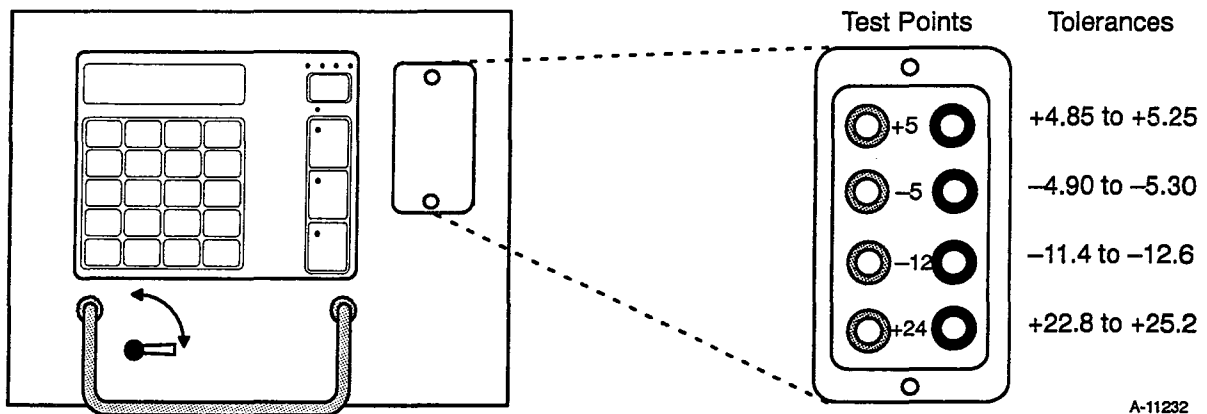| Test Points	Tolerances
+5	+4.85 to +5.25
−5	−4.90 to −5.30
−12	−11.4 to −12.6
+24	+22.8 to +25.2

A-11232

Figure 11-7 RD-62 Voltage Test Points

1. Perform the "RDE-6 Chassis Removal and Access" procedure described earlier in this section.

2. Loosen the captive fasteners located in front of the RD-62 power supply until they pop up (refer to Figure 11-8).

3. Slide the power supply forward and upward to expose the attached power cables.

4. Disconnect the cables and lift the power supply from the chassis.

5. Turn the power supply upside down and remove the four screws that fasten the power-supply plate to the power supply. Retain the mounting plate and screws for installation on the replacement power supply.

6. Ensure that the voltage select switch on the replacement power supply is set to the 208–240-V setting. Verify that the power supply On/Off switch is in the ON or "1" position (refer again to Figure 11-8).

7. Reverse the preceding steps (beginning with Step 5 and finishing with Step 1) to install the replacement power supply.

RD-62 Power
Supply

RD-62 Power-supply
On/Off Switch
(Normally On)

S2 Voltage
Select Switch

RD-62
Power-supply
Mounting Plate

Captive
Fastener

Location of
Solenoid
Assembly

Chassis

A-10995

Figure 11-8. RD-62 Power-supply Positions

Solenoid Logic Control Board Replacement Procedures

Perform the following steps to replace the solenoid logic control board.
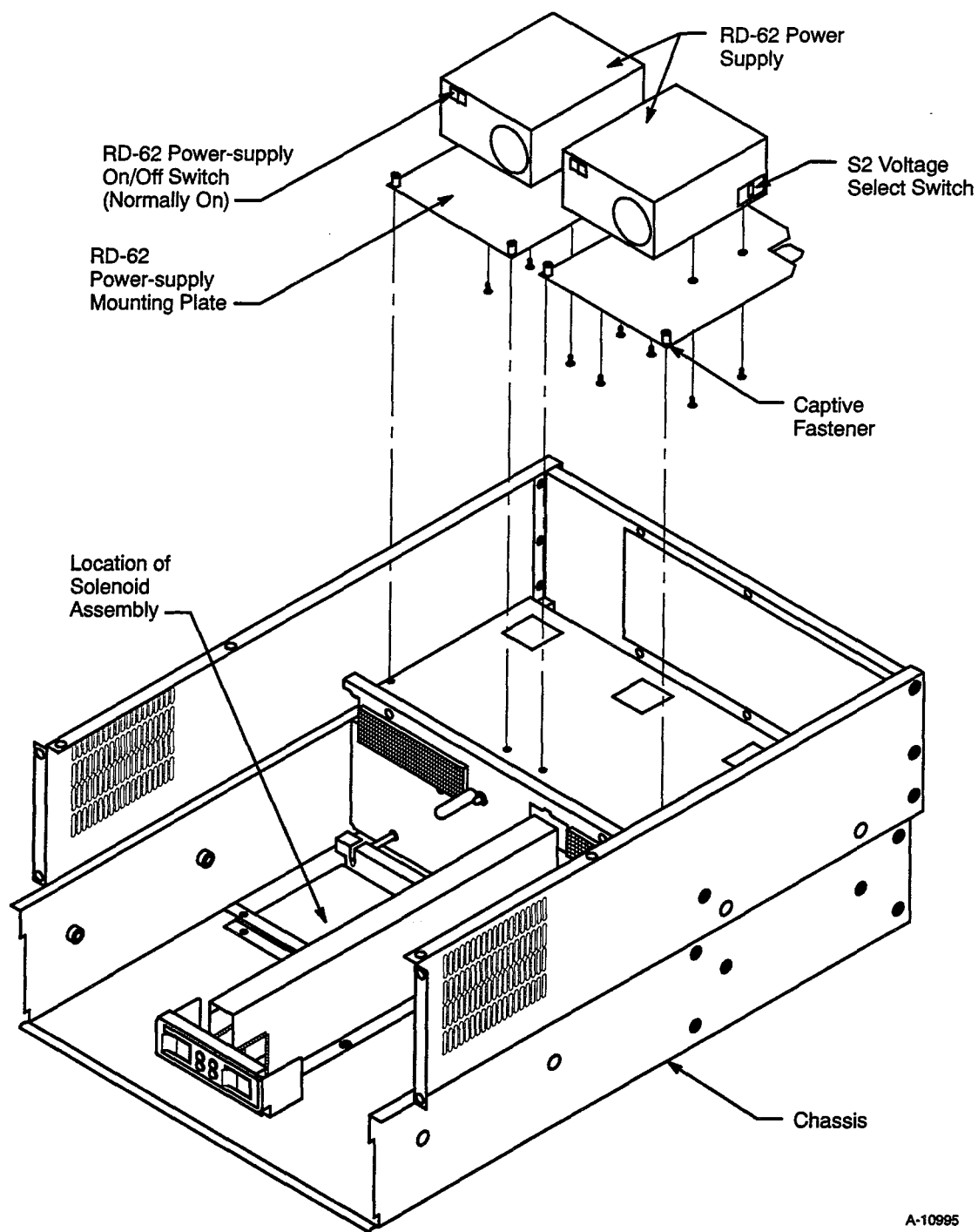
1. Perform the "RDE-6 Chassis Removal and Access" procedure described earlier in this section.

2. Loosen the three fasteners that secure the solenoid assembly cover to the chassis. Refer to Figure 11-9 for the location of the solenoid assembly.
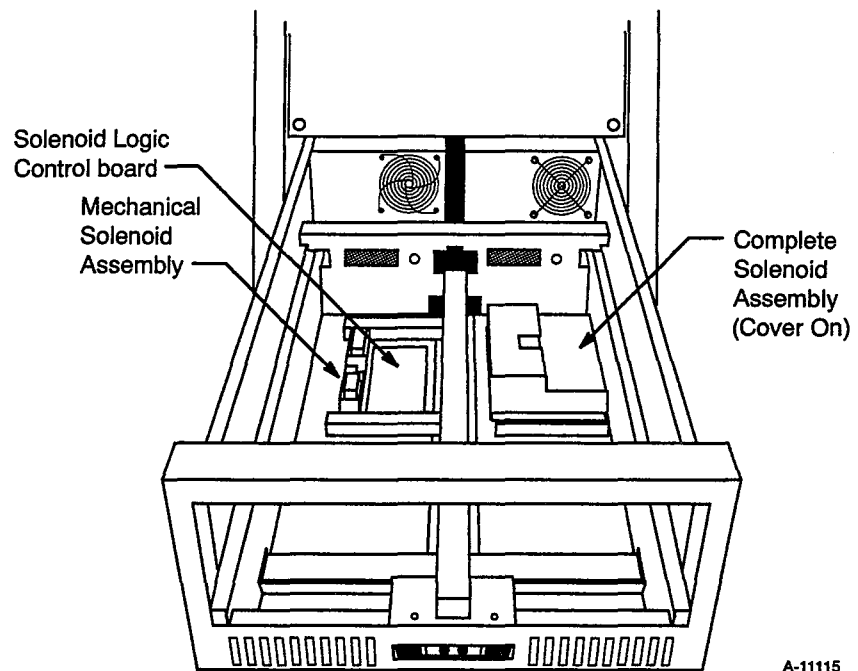
Figure 11-9. RDE-6 Solenoid Assemblies

3. Lift the solenoid cover out of the chassis.

	WARNING	
Remove all power connections from the RDE-6 cabinet before attempting to service the solenoid assembly. Failure to do so could result in serious injury or death because the 208–240 volt connections are exposed.		

CAUTION

Wear an electrostatic discharge (ESD) smock, wrist strap, and ESD shoes during the installation or replacement process. Damage to the solenoid logic will result if these precautions are not followed.

---

4. Unplug the seven connectors attached to the solenoid control board while noting the position and routing of each.

5. Using a Phillips screwdriver, remove the screws located in the corners of the solenoid control board.

6. Remove the logic board from the chassis. Ensure that jumper JP1 is correctly installed on the replacement logic board (refer to Figure 11-10).
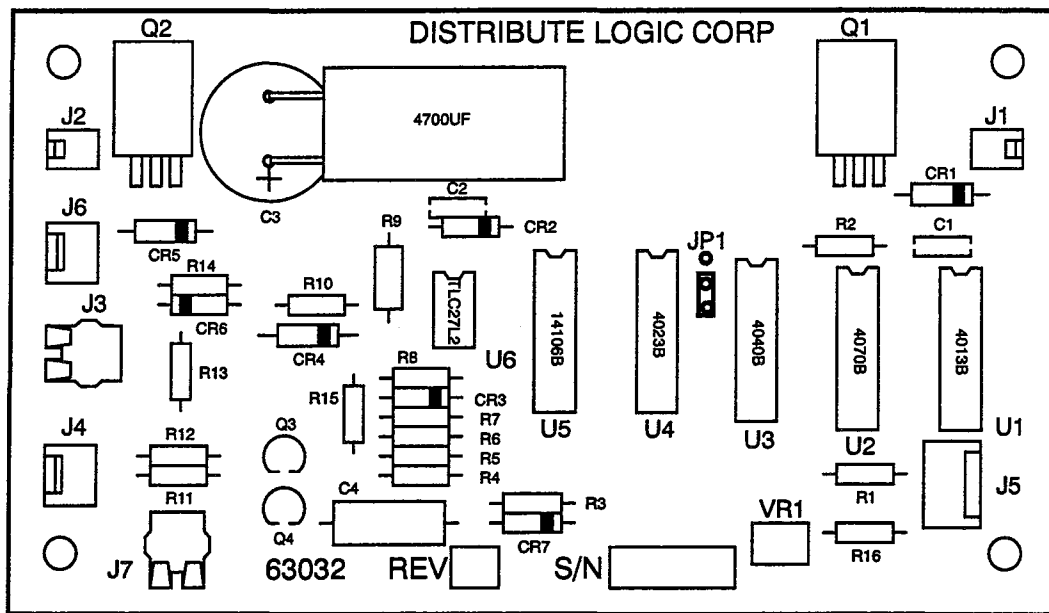
A-10998

Figure 11-10. Solenoid Logic Control Board

7. Reverse the previous steps (beginning with Step 5 and finishing with Step 1) to reinstall the solenoid logic control board. Ensure that the cables are plugged into the correct connectors.

Mechanical Solenoid Assembly Replacement Procedures

Perform the following steps to replace the mechanical solenoid assembly.

1. Perform the "RDE-6 Chassis Removal and Access" procedure described earlier in this section.

2. Loosen the three fasteners that secure the solenoid assembly cover to the chassis until they pop up. Refer to Figure 11-9 for the location of the solenoid assembly.

3. Lift the solenoid cover out of the chassis.

	WARNING	
Remove all power connections from the RDE-6 cabinet before attempting to service the solenoid assembly. Failure to do so could result in serious injury or death because the 208–240 volt connections are exposed.		

4. Unplug the two solenoid connections (J1 and J2) and the position sensor (J5) from the solenoid logic board. Refer to Figure 11-10.

5. Using a Phillips screwdriver, remove the three countersunk screws that secure the mechanical solenoid assembly bracket to the underside of the chassis.

6. Carefully lift and rotate the mechanical solenoid assembly just enough to clear the emergency release rod.

7. While firmly holding the mechanical assembly in one hand, use needle-nose pliers to carefully remove the red and black wires from the top and bottom of the microswitch. Note the position of these wires for correct attachment to the new assembly. Refer to Figure 11-11.

8. Lift the solenoid assembly out of the chassis and reverse the previous steps (beginning with Step 7 and finishing with Step 1) to install the new mechanical solenoid assembly. Ensure that proper cable routing is maintained.

Red Wire
(Pin 1)

Black Wire
(Pin 3)

Top of
Microswitch

Top View

Red Wire
(Pin 1)

Black Wire
(Pin 3)

Microswitch
(Behind Plate)

Red Wire
(Pin 1)

Black Wire
(Pin 3)

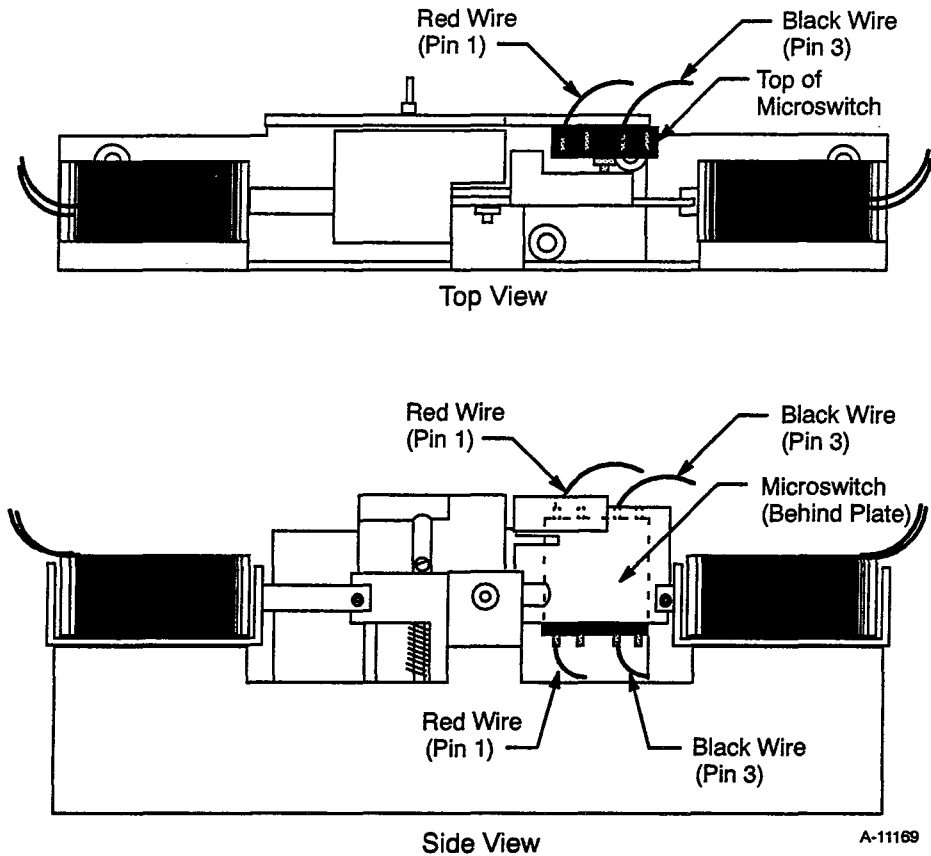Side View   A-11169

Figure 11-11. Mechanical Solenoid Assembly

SECTION 12
DCA-2 SYSTEMS STATUS

12 DCA-2 SYSTEMS STATUS

On DD60 only.
a flaw will cause
parity) errors)

This section provides status information for 60 series disk systems, including DCA-2 channel adapter status and disk drive status information.

OLHPA

Figure 12-1 shows an OLHPA error report for a DD-60. Refer to Table 12-1 for a cross-reference to the tables that describe each status.

```
************************************************************************
HOST ERROR PACKET
Device: 60-0-3-34.0   major = 32        minor = 17    I/O Path: 00334.0
IOS request:  read data                 IOS response:  io error
Final Status: Recovered by CRC regeneration
IOS-P: 00-2     Channel: 34/0     Device type: DD60      Retry Count: 7
Requested cylinder: 00556      Head: 000      Sector: 000 (Unicos)
Failing cylinder:    00556      Head: 000      Sector: 026 (Physical)
Physical Block:   000016859
Request Length (sect):   000026     Spiral Offset:   000006
General status: 100017


DCA2 STATUS PACKET
———————— DCA:13 ————————        ———————— DCA:12 ————————
Ending status:    100100         Adapter status: 000363
ID parameter 0 status: 000556    SECDED status   000000
ID parameter 1 status: 000026    Byte count status: 000000
                                 Tag status   000022


6X Condition Bits:    040        7X Condition Bits:   002


Stream 1:   ecc:  37465325361    Offset: 010146    Defect Add: 1004
Stream 5:   ecc:  46352765123    Offset: 010151    Defect Add: 1005
            Combined head mask: 042        Flawing defect address: 1004


DRIVE ERROR PACKET
Status response block
octet:   0       1       2       3       4       5       6       7
        000     000     000     000     000     000     000     000
Extended status block
octet:   0       1       2       3       4       5       6       7
        257     000     100     303     000     000     000     000


FRU code 1: 80     Fault code 1: 80     Status code 1: 80
  (Hex)   2: 80       (Hex)    2: 80         (Hex)    2: 80

************************************************************************
```

Error
DCA 2
Drive

Figure 12-1. OLHPA Error Report

Table 12-1. Status Name Cross-reference Chart

Table	Status Name	Obtained By
Table 12-2	General status	OLHPA software
Table 12-3	6X Condition bits	DCA2:12 channel function
Table 12-4	7X Condition bits	DCA2:12 channel function
Table 12-5	Adapter status	DCA2:12 channel function
Table 12-6	SECDED status	DCA2:12 channel function
Table 12-7	Transfer count status	DCA2:12 channel function
Table 12-8	Tag status	DCA2:12 channel function
Table 12-9	Drive ending status	DCA2:13 channel function
Table 13-10	Disk drive status on Bus B	IPI-2 protocol
Table 12-11	ID parameter 0 status	DCA2:13 channel function
Table 12-12	ID parameter 1 status	DCA2:13 channel function
Drive Status Response Block		
Table 12-13	Exception status (Byte 0)	Bus control command (44_{16})
Table 12-14	Unsolicited exceptions status (Byte 1)	Bus control command (44_{16})
Table 12-15	Bus Control exceptions status (Byte 2)	Bus control command (44_{16})
Table 12-16	Drive exceptions status (Byte 3)	Bus control command (44_{16})
Table 12-17	Drive exceptions status (Byte 4)	Bus control command (44_{16})
Table 12-18	Drive exceptions status (Byte 5)	Bus control command (44_{16})
Table 12-19	Drive exceptions status (Byte 6)	Bus control command (44_{16})
Table 12-20	Drive exceptions status (Byte 7)	Bus control command (44_{16})
Drive Extended Status Block		
Table 12-21	Interface flags status (Byte 0)	Bus control command (48_{16})
Table 12-22	Data received flags status (Byte 1)	Bus control command (48_{16})
Table 12-23	Data control flags status (Byte 2)	Bus control command (48_{16})
Table 12-24	Disk drive status (Byte 3)	Bus control command (48_{16})
Table 12-25	Disk drive alarms status (Byte 4)	Bus control command (48_{16})
Table 12-26	Vendor defined status (Byte 5)	Bus control command (48_{16})
Table 12-27	Vendor defined status (Byte 6)	Bus control command (48_{16})
Table 12-28	Head skew status (Byte 7)	Bus control command (48_{16})
Miscellaneous Status Information		
Table 12-29	OLHPA flaw location information	OLHPA software
Table 13-30	DD-60 rear panel display I/O status	DD-60 drive firmware
Table 13-31	DME function and error codes	DME software

General Status

General status is a combination of bits from several of the other statuses. It is combined and displayed by the OLHPA software. Table 12-2 describes each bit of the general status.

Table 12-2. General Status

Bit	Name	Description
2^0	Bus A parity error	When set to 1, this bit indicates that the parity bit of bus A was not set to the expected value. This signal is from the 3DE option.
2^1	Byte 1 parity error	When set to 1, this bit indicates that byte 1 (bus A information) of the data had a parity error. This signal is from the 3YB option.
2^2	Bus B parity error	When set to 1, this bit indicates that the parity bit of bus B was not set to the expected value. This signal is from the 3DE option.
2^3	Byte 0 parity error	When set to 1, this bit indicates that byte 0 (bus B information) of the data had a parity error. This signal is from the 3YB option.
2^4	Voltage fault −4.5 V	When set to 1, this bit indicates the −4.5-V supply is out of range.
2^5	Voltage fault +5.0 V	When set to 1, this bit indicates the +5.0-V supply is out of range.
2^6	Single-bit error	When set to 1, this bit indicates that one of the write data bits was wrong, but was corrected with SECDED circuitry in the 3YC option.
2^7	Double-bit error	When set to 1, this bit indicates that multiple write data bits were wrong and that SECDED circuitry in the 3YC option was unable to correct them.
2^8	Head Select Fault	When set to 1, this bit indicates that the disk drive received an invalid head selection.
2^9	Off Cylinder Fault	When set to 1, this bit indicates that the heads were not positioned over the correct cylinder during a seek, or that the heads moved off cylinder during a data transfer.
2^{10}	Seek Fault	When set to 1, this bit indicates that an error occurred during a seek, read/verify data, or write data bus control operation. Refer to the drive exception status bytes 3 through 7, Table 12-16 through Table 12-20, for more information on which conditions can cause the error.
2^{11}	Spindle Fault	When set to 1, this bit indicates that an error occurred during a spin-up, spin-down, or during a read/verify data or write data bus control operation. Refer to the drive exception status bytes 3 through 7, Table 12-16 through Table 12-20, for more information on which conditions can cause the error.
2^{12}	Execution Fault	When set to 1, this bit indicates that a disk drive execution fault occurred. Refer to the drive exception status bytes 3 through 7, Table 12-16 through Table 12-20, for more information on which conditions can cause the error.
2^{13}	ID Error Correction Code (ECC) error	When set to 1, this bit indicates that the ID field ECC read from the disk drive did not match the generated ECC from the 3DH options.
2^{14}	ID compare error	When set to 1, this bit indicates that the ID of the sector read from the disk drive did not compare to the expected ID stored in the 3DG option.
2^{15}	Data ECC error	When set to 1, this bit indicates that the data field error correction code (ECC) read from the disk drive did not match the generated ECC from the 3DH options.

DCA2:12 Statuses

The DCA2:12 statuses are transferred to the accumulator by a DCA2:12 channel function. Refer to Section 2, "DCA-2 Channel Functions," for more information on the DCA2:12 channel function.

Condition Bits

When the status select bits are both 0's and the sequencer is given a starting address of 36_8, the DCA2:12 channel function transfers the condition bits to the accumulator. There are two types of condition bits: the 6X condition bits and the 7X condition bits.

6X Condition Bits

The 6X condition bits are assembled by the microcode from information generated by the 3DE option, 3YC option, and voltage sensors on the DCA-2. When this status is read affects the condition of the bus A/B parity error flags because these flags are dynamic. Table 12-3 describes each bit of the 6X condition bits.

Table 12-3. 6X Condition Bits Status

Bit	Name	Description
2^0	Bus A parity error	When set to 1, this bit indicates that the parity bit of bus A was not set to the expected value. This parity is checked by the 3DE option.
2^1	Byte 1 parity error	When set to 1, this bit indicates that byte 1 (bus A information) of the data had a parity error. This parity is checked by the 3YB option.
2^2	Bus B parity error	When set to 1, this bit indicates that the parity bit of bus B was not set to the expected value. This parity is checked by the 3DE option.
2^3	Byte 0 parity error	When set to 1, this bit indicates that byte 0 (bus B information) of the data had a parity error. This parity is checked by the 3YB option.
2^4	−4.5 voltage bad	When set to 1, this bit indicates that the −4.5 voltage setting is out of acceptable range.
2^5	+5.0 voltage good	When set to 0, this bit indicates that the +5.0 voltage setting is out of acceptable range.
2^6	Single-bit error	When set to 1, this bit indicates that one of the write data bits was in error, but was corrected with SECDED circuitry in the 3YC option.
2^7	Double-bit error	When set to 1, this bit indicates that multiple bits were in error and that SECDED circuitry in the 3YC options was unable to correct them.

7X Condition Bits

The 7X condition bits are assembled by the microcode from information generated by the 3DH options and 3DG option on the DCA-2. Table 12-4 describes each bit of the 7X condition bits.

Table 12-4. 7X Condition Bits Status

Bit	Name	Description
2^0	ID compare error	The ID of the sector read from the disk drive did not compare to the expected ID.
2^1	Data ECC error	When set to 1, this bit indicates that the data field ECC read from the disk drive did not match the generated ECC from the 3DH options.
2^2	ID ECC error	When set to 1, this bit indicates that the ID field ECC read from the disk drive did not match the generated ECC from the 3DH options.
2^3	Valid flaw	When set to 1, this bit indicates that the sector contains a hideable flaw.
2^4	Unhideable flaw	When set to 1, this bit indicates that the sector contains an unhideable flaw.
2^5	ID field flaw	When set to 1, this bit indicates that the sector ID field contains a flaw.
2^6	Read protect	When set to 1, this bit indicates that the read protect bit of the sector ID field is set to 1.
2^7	Write protect	When set to 1, this bit indicates that the write protect bit of the sector ID field is set to 1.

Adapter Status

When the status select bits are both 0's, the DCA2:12 channel function transfers the adapter status to the accumulator (refer to Table 12-5). The lower byte of this status should be decoded by first starting at the bottom of the list (200_8) and then selecting all status codes that can be ORed into the returned status value. When all set bits of the returned value have been satisfied by the codes selected, decoding is complete. For example, if the returned adapter status is equal to 000363_8, the decode is as follows:

Codes	Applicable
200_8	Yes
100_8	Yes
40_8	Yes
24_8	No
22_8	Yes
21_8	Yes
363_8	(ORed sum of applicable codes equals returned value)

Table 12-5. Adapter Status

Bit	Name	Description
2^0	DCA-2 status bit 2^0	**Bits** **Description** 000_8– No errors were detected by the sequencer. 001_8– The disk drive did not respond to a request within a set time limit. 002_8– The interface did not return to the IDLE state within a set time limit.
2^1	DCA-2 status bit 2^1	003_8– The disk drive did not respond to a select within a set time limit. 004_8– The expected disk drive did not respond to the select sequence. 005_8– The disk drive set the busy flag during a select sequence.
2^2	DCA-2 status bit 2^2	006_8– The disk drive is not selected when the sequencer expected it to be. 007_8– The disk drive is selected when the sequencer did not expect it to be.
2^3	DCA-2 status bit 2^3	010_8– During a bus control sequence, the disk drive did not set the Sync In signal to 1 within a set time limit. 011_8– During a bus control sequence, the disk drive did not reset the Sync In signal to 0 within a set time limit.
2^4	DCA-2 status bit 2^4	012_8– The bus control sequence failed or an information transfer was not required and the disk drive terminated the sequence. 014_8– The sequencer terminated an information transfer.
2^5	DCA-2 status bit 2^5	020_8– The read or write operation was terminated due to ID miscompare, disk drive detected error, or disk drive voltage fault. 021_8– A parity error occurred on bus A. 022_8– A parity error occurred on bus B.
2^6	DCA-2 status bit 2^6	024_8– A parity error occurred on the ending status byte. 040_8– A parity error occurred on byte 0 of the data.
2^7	DCA-2 status bit 2^7	100_8– A parity error occurred on byte 1 of the data. 200_8– An error was detected during the ending status sequence.
2^8	Single-bit error	When set to 1, this bit indicates that the SECDED circuitry in the 3YC option corrected 1 bit of write data.
2^9	Double-bit error	When set to 1, this bit indicates that multiple bits were in error and that SECDED circuitry in the 3YC options was unable to correct them.
2^{10}	Voltage fault –4.5 V	When set to 1, this bit indicates that the –4.5-V supply is out of range.
2^{11}	Voltage fault +5.0 V	When set to 1, this bit indicates that the +5.0-V supply is out of range.
2^{12}	RAM parity error bit 2^0	When set to 1, this bit indicates a sequencer parity error on bits 0, 4, 8, 12, 16, 20, 24, and 28.
2^{13}	RAM parity error bit 2^1	When set to 1, this bit indicates a sequencer parity error on bits 1, 5, 9, 13, 17, 21, 25, and 29.
2^{14}	RAM parity error bit 2^2	When set to 1, this bit indicates a sequencer parity error on bits 2, 6, 10, 14, 18, 22, 26, and 30.
2^{15}	RAM parity error bit 2^3	When set to 1, this bit indicates a sequencer parity error on bits 3, 7, 11, 15, 19, 23, 27, and 31.

SECDED Status

When status select bit 2^1 is 0 and bit 2^0 is 1, the DCA2:12 channel function transfers the SECDED status to the accumulator (refer to Table 12-6).

Table 12-6. SECDED Status

Bit	Name	Description
2^0	Syndrome bit 2^0	These bits contain the syndrome bits from the 3YC option SECDED circuitry.
2^1	Syndrome bit 2^1	
2^2	Syndrome bit 2^2	
2^3	Syndrome bit 2^3	
2^4	Syndrome bit 2^4	
2^5	Syndrome bit 2^5	
2^6	Syndrome bit 2^6	
2^7	Syndrome bit 2^7	
2^8	Single-bit count bit 2^0	These bits contain the number of times the 3YC option detected a single-bit error.
2^9	Single-bit count bit 2^1	
2^{10}	Single-bit count bit 2^2	
2^{11}	Single-bit count bit 2^3	
2^{12}	Double-bit count bit 2^0	These bits contain the number of times the 3YC option detected a double-bit error.
2^{13}	Double-bit count bit 2^1	
2^{14}	Double-bit count bit 2^2	
2^{15}	Double-bit count bit 2^3	

Transfer Count Status

When status select bit 2^1 is 1 and bit 2^0 is 0, the DCA2:12 channel function transfers the transfer count status to the accumulator (refer to Table 12-7). This value represents the number of parcels remaining to be transferred to the drive when an operation was halted.

Table 12-7. Transfer Count Status

Bits	Name	Description
2^0 through 2^{15}	Transfer count bits 2^0 through 2^{15}	These bits contain the current value of the transfer counter in the 3DI option.

Tag Status

When the status select bits are both 1, the DCA2:12 channel function transfers the tag status to the accumulator (refer to Table 12-8). This status represents the state of the IPI interface when the status was requested.

Table 12-8. Tag Status

Bit	Name	Description
2^0	Attention In signal	This bit displays the state of the Attention In signal from the 3DE option.
2^1	Slave In signal	This bit displays the state of the Slave In signal from the 3DE option.
2^2	Sync In signal	This bit displays the state of the Sync In signal from the 3DE option.
2^3	Not used	This bit is not used.
2^4	Select Out signal	This bit displays the state of the Select Out signal from the 3DF option.
2^5	Master Out signal	This bit displays the state of the Master Out signal from the 3DF option.
2^6	Sync Out signal	This bit displays the state of the Sync Out signal from the 3DF option.
2^7	Not used	These bits are not used.
2^8	Not used	
2^9	Not used	
2^{10}	Not used	
2^{11}	Not used	
2^{12}	Not used	
2^{13}	Not used	
2^{14}	Not used	
2^{15}	Not used	

DCA2:13 Statuses

The DCA2:13 statuses are transferred to the accumulator by a DCA2:13 channel function. Refer to the "DCA-2 Channel Functions" section for more information on the DCA2:13 channel function.

Drive Ending Status

When the status select bits are both 0, the DCA2:13 channel function transfers the drive ending status to the accumulator. The drive ending status parcel can contain one or two copies of the IPI-2 ending status byte described in Table 12-10. Refer to Table 12-9 for a description of each bit of the drive ending status parcel.

Table 12-9. Drive Ending Status

Bit	Name	Description
2^0	Final drive ending status bit 2^0	
2^1	Final drive ending status bit 2^1	
2^2	Final drive ending status bit 2^2	
2^3	Final drive ending status bit 2^3	These bits contain the final drive ending status byte.
2^4	Final drive ending status bit 2^4	
2^5	Final drive ending status bit 2^5	
2^6	Final drive ending status bit 2^6	
2^7	Final drive ending status bit 2^7	
2^8	Initial drive ending status bit 2^0	
2^9	Initial drive ending status bit 2^1	
2^{10}	Initial drive ending status bit 2^2	
2^{11}	Initial drive ending status bit 2^3	These bits contain the initial drive ending status byte.
2^{12}	Initial drive ending status bit 2^4	
2^{13}	Initial drive ending status bit 2^5	
2^{14}	Initial drive ending status bit 2^6	
2^{15}	Initial drive ending status bit 2^7	

Initial Drive Ending Status

The initial drive ending status contains the IPI ending status on bus B after completion of a single, or the first of two, drive function sequences. For example, during a load position routine, the sequencer performs one drive function sequence. The drive ending status from this sequence is stored in the initial drive ending status while the final drive ending status is unused and remains zeros.

Final Drive Ending Status

The final drive ending status contains the second of two drive ending statuses received on bus B after a dual drive function sequence (refer to Table 12-10). For example, during a write sector of data routine, the sequencer performs two drive function sequences. The initial drive ending status is received after the ID is read and compared. The final drive ending status is received after the data field has been written.

Table 12-10. Disk Drive Status on Bus B

Bit	Name	Description
2^0	Operation status bit 2^0	Bits Description 00_8 – The disk drive executed the bus control command and is available. 01_8 – The disk drive rejected the bus control command and is busy.
2^1	Operation status bit 2^1	04_8 – The disk drive did not detect the address mark. 05_8 – The disk drive did not detect the sync byte.
2^2	Operation status bit 2^2	06_8 – ECC error (not used by CRI) 07_8 – Verify ID miscompare (not used by CRI)
2^3	Operation status bit 2^3	10_8 – An operation exception occurred. The exception status may be read for more information (refer to Table 12-13). 14_8 – An unsolicited exception occurred. The unsolicited exception status must be read before continuing (refer to Table 12-14).
2^4	Time dependent operation	When set to 1, this bit indicates that the last command has not been completed by the disk drive. The disk drive will set the Attention In signal when it completes the command.
2^5	Odd byte transfer	When set to 1, this bit indicates that the last information transfer contained an odd number of bytes. If set, the last byte transferred on bus B is not valid.
2^6	Bus parity error	When set to 1, this bit indicates the disk drive detected a parity error on a bus control command, information transfer, or controller status.
2^7	Good transfer	When set to 1, this bit indicates the disk drive did not detect a parity error on a bus control command, information transfer, or controller status.

ID Parameter 0 Status

When status select bit 2^1 is 0 and bit 2^0 is 1, the DCA2:13 channel function transfers the ID parameter 0 status to the accumulator. Refer to Table 12-11 for a description of the ID parameter 0 status bits.

Table 12-11. ID Parameter 0 Status

Bit	Name	Description
2^0 through 2^{15}	Cylinder address (ID parameter 0)	These bits contain the current value of the cylinder register in the 3DG option.

ID Parameter 1 Status

When status select bit 2^1 is 1 and bit 2^0 is 0, the DCA2:13 channel function transfers the ID parameter 1 status to the accumulator. Refer to Table 12-12 for a description of each bit of the ID parameter 1 status.

Table 12-12. ID Parameter 1 Status

Bit	Name	Description
2^0	Sector address bit 2^0	These bits contain the current sector address.
2^1	Sector address bit 2^1	
2^2	Sector address bit 2^2	
2^3	Sector address bit 2^3	
2^4	Sector address bit 2^4	
2^5	Sector address bit 2^5	
2^6	Head address bit 2^0	These bits contain the current head address.
2^7	Head address bit 2^1	
2^8	Head address bit 2^2	
2^9	Head address bit 2^3	
2^{10}	Head address bit 2^4	
2^{11}	Not used	This bit is not used.
2^{12}	Read protection	When set to 1, this bit indicates that the RP bit was set in the ID field read from the sector. This bit is presently unused.
2^{13}	Write protection	When set to 1, this bit indicates that the WP bit was set in the ID field read from the sector. This bit is presently unused.
2^{14}	Not used	This bit is not used.
2^{15}	Not used	This bit is not used.

Drive Status Response Block

The status response block is 8 bytes of IPI-2 status information transferred from the disk drive to the DCA-2. The status response block is read when the sequencer sends a bus control code for read status (44_{16}) to the disk drive over bus A. Tables 12-13 through 12-20 describe each bit in the statuses' response blocks.

Table 12-13. Exception Status (Byte 0)

Bit	Name	Description
2^0	Execution fault	When set to 1, this bit indicates that a disk drive execution fault occurred. Refer to the drive exception status bytes 3 through 7, Tables 12-16 through 12-20, for more information on conditions that can cause the error.
2^1	Spindle fault	When set to 1, this bit indicates that an error occurred during a spin-up, spin-down, read/verify data, or write data bus control operation. Refer to the drive exception status bytes 3 through 7, Tables 12-16 through 12-20, for more information on conditions that can cause the error.
2^2	Seek fault	When set to 1, this bit indicates that an error occurred during a seek, read/verify data, or write data bus control operation. Refer to the drive exception status bytes 3 through 7, Tables 12-16 through 12-20, for more information on conditions that can cause the error.
2^3	Write fault	When set to 1, this bit indicates that an error occurred during a write data bus control operation. Refer to the drive exception status bytes 3 through 7, Tables 12-16 through 12-20, for more information on conditions that can cause the error.
2^4	Read fault	When set to 1, this bit indicates that an error occurred during a read/verify bus control operation. Refer to the drive exception status bytes 3 through 7, Tables 12-16 through 12-20, for more information on conditions that can cause the error.
2^5	Bus control exception	When set to 1, this bit indicates that the disk drive did not accept the last bus control command. Refer to the bus control exception status (byte 2), Table 12-15, for more information on conditions that can cause the error.
2^6	Unsolicited exception	When set to 1, this bit indicates that the disk drive has an unsolicited exception condition. Refer to the unsolicited exceptions status (byte 1), Table 12-14, for more information on conditions that can cause the error.
2^7	Status response	This bit is always set to 0 for a status response.

Table 12-14. Unsolicited Exceptions Status (Byte 1)

Bit	Name	Description
2^0	Media change	When set to 1, this bit indicates that the head disk assembly (HDA) was removed and replaced with another HDA.
2^1	Ready transition	When set to 1, this bit indicates that the disk drive changed from a not ready condition to a ready condition.
2^2	Not Ready transition	When set to 1, this bit indicates that the disk drive changed from a ready condition to a not ready condition.
2^3	Reserved	This bit is not used.
2^4	Alternate port format complete	When set to 1, this bit indicates that the alternate port received the notify alternate port of format completion bus control command.
2^5	Alternate port format change	When set to 1, this bit indicates that the alternate port accepted a new format specification.
2^6	Alternate port priority select	When set to 1, this bit indicates that the alternate port issued a disk drive address with the priority select bit set to 1.
2^7	Reset complete	When set to 1, this bit indicates that the disk drive completed a reset operation.

Table 12-15. Bus Control Exceptions Status (Byte 2)

Bit	Name	Description
2^0	Reserved	This bit is not used.
2^1	Reserved	This bit is not used.
2^2	Reserved	This bit is not used.
2^3	Data bus control late	When set to 1, this bit indicates that the bus control command was valid but the disk drive did not receive the command within a given time limit.
2^4	Bus control context	When set to 1, this bit indicates that the bus control command was valid but it conflicts with the current disk drive operation.
2^5	Unsupported bus control	When set to 1, this bit indicates that the bus control command was valid but the disk drive does not support the command.
2^6	Invalid parameter	When set to 1, this bit indicates that the bus control parameter was not valid.
2^7	Invalid bus control	When set to 1, this bit indicates that the bus control command issued was not valid.

Table 12-16. Drive Exceptions Status (Byte 3)

Bit	Name	Description
2^0	Reserved	This bit is not used.
2^1	Logic temperature fault	When set to 1, this bit indicates that the disk drive detected an overtemperature condition.
2^2	Voltage fault	When set to 1, this bit indicates that the disk drive detected a voltage that was out of range.
2^3	Reserved	This bit is not used.
2^4	Reserved	This bit is not used.
2^5	Head select fault	When set to 1, this bit indicates that the disk drive received an invalid head selection.
2^6	Off cylinder fault	When set to 1, this bit indicates that the heads were not positioned over the correct cylinder during a seek, or that the heads moved off cylinder during a data transfer.
2^7	Speed fault	When set to 1, this bit indicates that the platters did not reach the required rotation speed during spin-up or lost speed during a data transfer.

Table 12-17. Drive Exceptions Status (Byte 4)

Bit	Name	Description
2^0	Reserved	This bit is not used.
2^1	Reserved	This bit is not used.
2^2	Reserved	This bit is not used.
2^3	Data strobe fault	When set to 1, this bit indicates that the early or late data strobe was in effect when the disk drive received a write data bus control command.
2^4	Head offset fault	When set to 1, this bit indicates that the heads were in an offset position when the disk drive received a write data bus control command.
2^5	Write transmission fault	When set to 1, this bit indicates that the disk drive received a write data bus control command but did not receive write data.
2^6	Reserved	This bit is not used.
2^7	Write protected fault	When set to 1, this bit indicates that the disk drive received a write data bus control command but was in write protected mode.

Table 12-18. Drive Exceptions Status (Byte 5)

Bit	Name	Description
2^0	Reserved	This bit is not used.
2^1	Reserved	This bit is not used.
2^2	Reserved	This bit is not used.
2^3	Reserved	This bit is not used.
2^4	Reserved	This bit is not used.
2^5	Read/write diagnostic disable	When set to 1, this bit indicates that the internal read/write disk drive diagnostics are disabled.
2^6	Diagnostic test incomplete	When set to 1, this bit indicates that the disk drive failed to execute an internal diagnostic test.
2^7	Diagnostic status valid	When set to 1, this bit indicates that an error occurred during internal disk drive diagnostics.

Table 12-19. Drive Exceptions Status (Byte 6)

Bit	Name	Description
2^0	Head 0 error	When set to 1, this bit indicates that head 0 of the logical head group cannot write or read data.
2^1	Head 1 error	When set to 1, this bit indicates that head 1 of the logical head group cannot write or read data.
2^2	Head 2 error	When set to 1, this bit indicates that head 2 of the logical head group cannot write or read data.
2^3	Head 3 error	When set to 1, this bit indicates that head 3 of the logical head group cannot write or read data.
2^4	Head 4 error	When set to 1, this bit indicates that head 4 of the logical head group cannot write or read data.
2^5	Head 5 error	When set to 1, this bit indicates that head 5 of the logical head group cannot write or read data.
2^6	Head 6 error	When set to 1, this bit indicates that head 6 of the logical head group cannot write or read data.
2^7	Heads 7 or 8 error	When set to 1, this bit indicates that head 7 of the logical head group cannot write or read data or that head 8 cannot write or read data.

Table 12-20. Drive Exceptions Status (Byte 7)

Bit	Name	Description
2^0	Reserved	This bit is not used.
2^1	Field overrun	When set to 1, this bit indicates that the heads moved past the end of the ID or data field boundary before a write or read data operation finished.
2^2	Sector overrun	When set to 1, this bit indicates that the heads moved past the end of a sector boundary before a write or read data operation finished.
2^3	Track overrun	When set to 1, this bit indicates that the heads moved past the end of the track before a write or read data operation finished.
2^4	Operation fault	When set to 1, this bit indicates that an error occurred during the last disk drive operation.
2^5	Data control late	When set to 1, this bit indicates that the disk drive did not receive the write or read data bus control command in the specified time limit.
2^6	Data control reject Bit 2^0	00 – Normal status. 01 – The write or read data bus control command was not valid.
2^7	Data control reject Bit 2^1	10 – The write or read data bus control command conflicted with a current disk drive operation. 11 – The disk drive received a write or read data bus control but the rotational position sensing (RPS) was disabled.

Drive Extended Status Block

The drive extended status block is 8 bytes of additional IPI-2 status information transferred from the disk drive to the DCA-2. The drive extended status block is read when the sequencer sends a bus control code for read status (48_{16}) to the disk drive over bus A. Tables 12-21 through 12-28 describe each bit in the drive extended status block.

Table 12-21. Interface Flags Status (Byte 0)

Bit	Name	Description
2^0	Format specification present	When set to 1, this bit indicates that a valid format specification has been loaded to the disk drive.
2^1	Status pending interrupt enables	When set to 1, this bit indicates that the status pending interrupts are enabled so the disk drive can use the Attention In signal on the current port.
2^2	RPS interrupt enabled	When set to 1, this bit indicates that the RPS interrupt is enabled so the disk drive can use the Attention In signal on the current port.
2^3	Command complete interrupt enabled	When set to 1, this bit indicates that the command complete interrupts are enabled so the disk drive can use the Attention In signal on the current port.
2^4	Reserve active	When set to 1, this bit indicates that the disk drive is reserved for use by the current port in use.
2^5	Alternate port enabled	When set to 1, this bit indicates that the alternate port is enabled.
2^6	Port number	When set to 0, this bit indicates that port A is in use. When set to 1, this bit indicates that port B is in use.
2^7	Extended status	This bit is always set to 1.

Table 12-22. Data Received Flags Status (Byte 1)

Bit	Name	Descriptions
2^0	Data ECC enabled	When set to 1, this bit indicates that the disk drive data field ECC circuitry is enabled. This option is not used by Cray Research, Inc. (CRI).
2^1	Header ECC enabled	When set to 1, this bit indicates that the disk drive ID field ECC circuitry is enabled. This option is not used by CRI.
2^2	Reserved	This bit is not used.
2^3	Late data strobe	When set to 1, this bit indicates that the late data strobe is active.
2^4	Early data strobe	When set to 1, this bit indicates that the early data strobe is active.
2^5	Offset magnitude bit 2^0	These bits indicate the magnitude of the head offset operation. If these bits are set to 0, the heads are not offset.
2^6	Offset magnitude bit 2^1	
2^7	Offset direction	When set to 0, this bit indicates that a positive offset of the heads is in effect. When set to 1, this bit indicates that a negative offset of the heads is in effect.

Table 12-23. Data Control Flags Status (Byte 2)

Bit	Name	Description
2^0	Reserved	This bit is not used.
2^1	Reserved	This bit is not used.
2^2	Reserved	This bit is not used.
2^3	Reserved	This bit is not used.
2^4	Reserved	This bit is not used.
2^5	Reserved	This bit is not used.
2^6	Spindle power on	When set to 1, this bit indicates that the disk drive power is on.
2^7	Write protected	When set to 1, this bit indicates that the disk drive is in write protected mode.

Table 12-24. Disk Drive Status (Byte 3)

Bit	Name	Description
2^0	Media present	When set to 1, this bit indicates that the head disk assembly (HDA) is present.
2^1	HDA ready	When set to 1, this bit indicates that the platters are rotating at the correct speed, and that the heads are loaded and positioned on the correct track.
2^2	Reserved	This bit is not used.
2^3	Reserved	This bit is not used.
2^4	Sync locked	When set to 1, this bit indicates that the spindle rotation is synchronized.
2^5	Master sync	When set to 1, this bit indicates that the spindle is currently assigned as the master sync device.
2^6	On cylinder	When set to 1, this bit indicates that the heads are over the correct cylinder.
2^7	Speed	When set to 1, this bit indicates that the platters are rotating at the correct speed.

Table 12-25. Disk Drive Alarms Status (Byte 4)

Bit	Name	Description
2^0	Reserved	This bit is not used.
2^1	Logic over temperature	When set to 1, this bit indicates that the disk drive detected an over temperature condition.
2^2	Voltage range error	When set to 1, this bit indicates that the disk drive detected an out-of-range voltage.
2^3	Reserved	This bit is not used.
2^4	Reserved	This bit is not used.
2^5	Illegal head select	When set to 1, this bit indicates that the disk drive has no heads selected, multiple heads selected, or the wrong head selected.
2^6	Reserved	This bit is not used.
2^7	Reserved	This bit is not used.

Table 12-26. Vendor-defined Status (Byte 5)

Bits	Name	Description
2^0 through 2^1	Reserved	These bits are not used.

Table 12-27. Vendor-defined Status (Byte 6)

Bits	Name	Description
2^0	Spindle type	When set to 0, this bit indicates that the disk drive is set to a 9-head parallel mode (DCA-2 application). When set to 1, this bit indicates that the disk drive is set to an 8-head parallel mode (DCA-3 application).
2^1 through 2^7	Reserved	These bits are not used.

Table 12-28. Head Skew Status (Byte 7)

Bits	Name	Description
2^0 through 2^7	Head skew bits	These bits contain the value of the head skew.

Flaw Location Information

The flaw location information contains the number of the physical head under which the flaw was detected, the location of the flaw in the sector, and the defect parameter of the flaw. It is calculated and displayed by the OLHPA software. Table 12-29 describes each entry of the flaw location information.

Table 12-29. OLHPA Flaw Location Information

Information	Description
Head mask bit	When one of these bits is set to 1, this bit indicates that the sector under the corresponding physical head may have a flaw.
Correction offset	The correction offset contains the position of the detected flaw.
Defect address	The defect address contains the value for the defect parameter in a physical sector.
Combined head mask	When one or more of these bits are set to 1, these bits indicate that the sectors under the corresponding physical heads may have a flaw.
Flawing defect address	The flawing defect address contains the combined value (from multiple heads) for the defect parameter.

DD-60 Rear Panel Display I/O Status

During normal disk drive operations, the DD-60 rear panel display shows the current I/O status for the disk drive. The I/O status contains information on the state of the disk drive hardware and fault information. Table 12-30 describes each I/O status.

Table 12-30. DD-60 Rear Panel Display I/O Status

Status Display (Hex)	Description
00	Initial state after a power-up or slave reset. Successful completion of the power-up or slave reset diagnostics causes the display to change.
01	Initialization state after power-on diagnostics or slave reset. Also indicates that a not-ready transition was detected.
02	Invalid setting of ID microcode switches.
03	Waiting for first ready (first spin-up after powerup or reset). Also indicates that the ready-to-not-ready transition was detected.
04	Timeout waiting for servo test to start.
05	Timeout waiting for servo test to end.

DD-60 Rear Panel Display I/O Status (continued)

Status Display (Hex)	Description
06	Timeout waiting for drive to respond to I/O board.
07	Waiting for ready transition after spin-up command was issued.
08	Undefined.
09	Successful execution of read and write diagnostics.
0A	Undefined.
0B	Undefined.
0C	A test failed, a logic failure occurred, or the heads moved off cylinder during the read and write diagnostics.
0D	Timeout occurred while waiting for the heads to move over the cylinder.
0E	The On-cylinder signal was active after a seek or return-to-zero (RTZ) command was issued during read and write diagnostics.
0F	Expected active On-cylinder signal during read and write diagnostics.
10	Reserved.
11	A read/write fault occurred.
12	Attempted a read or write with a not-on-cylinder fault.
13	Attempted a read or write with a not-on-cylinder fault. Also a read/write fault occurred.
14	A first seek fault occurred.
15	A read/write fault and a first seek fault occurred.
16	Attempted a read/write while the heads were not on cylinder. Also a first seek fault occurred.
17	Attempted a read/write while the heads were not on cylinder, and a first seek fault and read/write fault occurred.
18	A write fault occurred.
19	A read/write fault and a write fault occurred.
1A	Attempted a read/write while the heads were not on cylinder, and a write fault occurred.
1B	Attempted a read/write while the heads were not on cylinder, and a read/write fault and a write fault occurred.
1C	A first seek fault and a write fault occurred.
1D	A read/write fault, a first seek fault, and a write fault occurred.
1E	Attempted a read or write while the heads were not on cylinder. A first seek fault and a write fault also occurred.
1F	Attempted a read or write while the heads were not on cylinder. A read/write fault, a first seek fault, and a write fault also occurred.
20	Reserved.
21	Attempted a write while write protected.
22	A head select fault occurred.
23	Attempted a write while write protected, and a head select fault occurred.

Table 12-30. DD-60 Rear Panel Display I/O Status (continued)

Status Display (Hex)	Description
24	A voltage fault occurred.
25	Attempted a write while write protected, and a voltage fault occurred.
26	A head select fault and a voltage fault occurred.
27	Attempted a write while write protected, and a head select fault and voltage fault occurred.
28	A seek error occurred.
29	Attempted a write while write protected and a seek error occurred.
2A	A head select fault and a seek error occurred.
2B	Attempted a write while write protected, and a head select fault with a seek error occurred.
2C	A voltage fault and seek error occurred.
2D	Attempted a write while write protected. A voltage fault with a seek error also occurred.
2E	A head select fault, voltage fault, and seek error occurred.
2F	Attempted a write while write protected and a head select fault, voltage fault, and seek error occurred.
30	The write/read diagnostic failed. The internal components most likely to have caused the failure: 1. Control circuit board 2. IPI-2 logic circuit board 3. Multiple channel read/write failure or the diagnostic cylinder was not formatted 4. HDA module
31	The write/read diagnostic failed. The internal components most likely to have caused the failure: 1. Read/write channel 8 circuit board 2. Multiple channel read/write failure or the diagnostic cylinder was not formatted 3. Control circuit board 4. IPI-2 logic circuit board
32	The write/read diagnostic failed. The internal components most likely to have caused the failure: 1. Read/write channel 0 and 7 circuit board 2. Read/write channel 8 circuit board 3. Control circuit board 4. IPI-2 logic circuit board
33	The write/read diagnostic failed. The internal components most likely to have caused the failure: 1. Read/write channel 0 and 7 circuit board 2. Control circuit board 3. IPI-2 logic circuit board 4. HDA module

Table 12-30. DD-60 Rear Panel Display I/O Status (continued)

Status Display (Hex)	Description
34	The write/read diagnostic failed. The internal components most likely to have caused the failure: 1. Read/write channel 1 and 6 circuit board 2. Control circuit board 3. IPI-2 logic circuit board 4. HDA module
35	The write/read diagnostic failed. The internal components most likely to have caused the failure: 1. Read/write channel 2 and 5 circuit board 2. Control circuit board 3. IPI-2 logic circuit board 4. HDA module
36	The write/read diagnostic failed. The internal components most likely to have caused the failure: 1. Read/write channel 3 and 4 circuit board 2. Control circuit board 3. IPI-2 logic circuit board 4. HDA module
37	The write/read diagnostic failed. The internal components most likely to have caused the failure: 1. Read/write channel 8 circuit board 2. Control circuit board 3. IPI-2 logic circuit board 4. HDA module
38 through 7F	Undefined.
80 through FF	Reserved.

SECTION 13
DCA-3 BASIC THEORY OF OPERATION

13 DCA-3 BASIC THEORY OF OPERATION

The DCA-3 channel adapter is a half-board controller for an array of five IPI-2 disk storage units. Four spindles (spindles 0 through 3) store data and a fifth spindle (spindle 4) stores parity (refer to Figure 13-1).
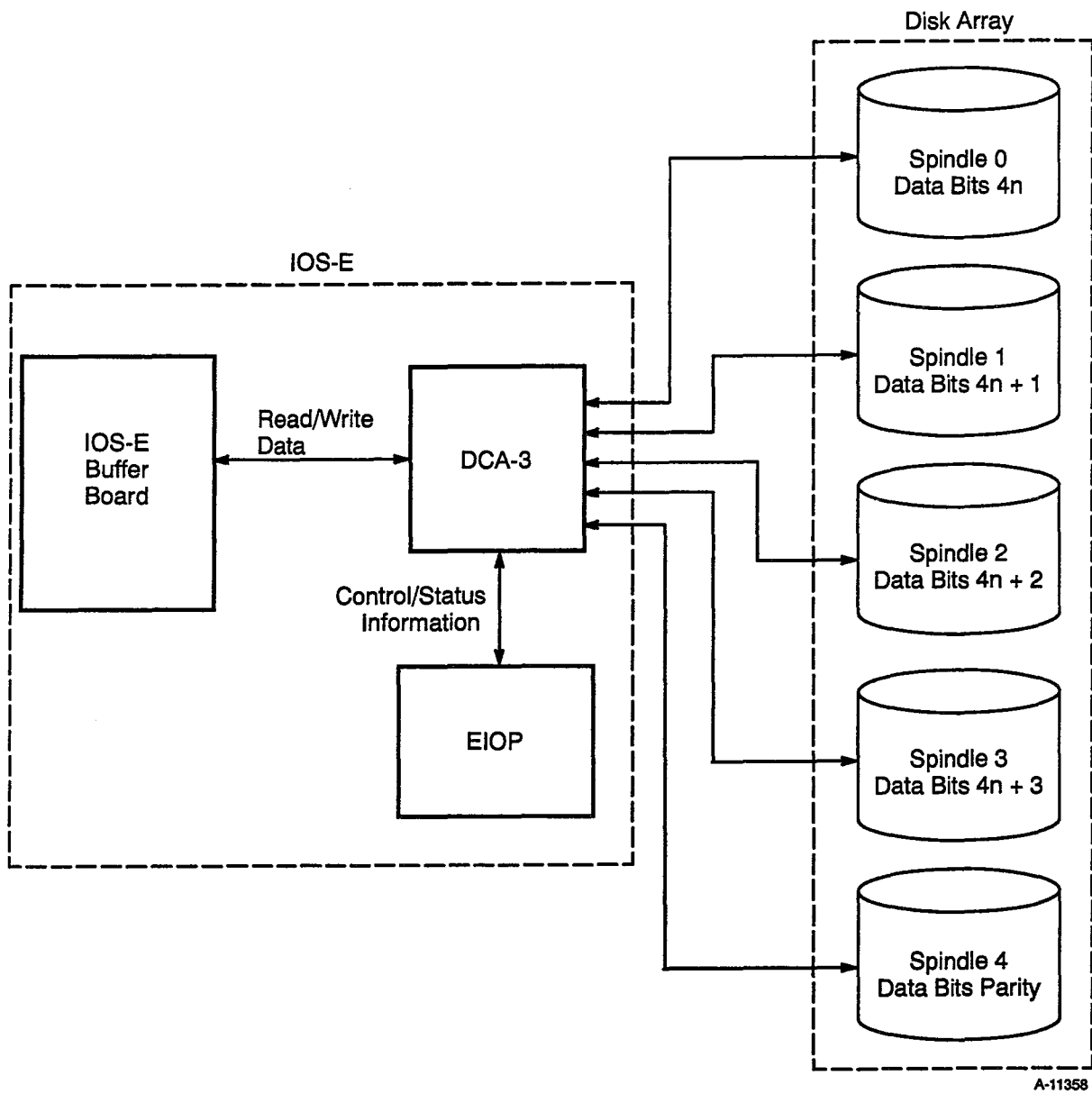
Figure 13-1. Block Diagram of DCA-3 to Disk Array Interface

NOTE: The DCA-3 channel adapter uses data striping as a means of transferring data to the disk array. Data striping is a method by which a Cray word is split into four sections; each section is then sent to a corresponding spindle to be transferred in parallel with the other three sections. This means one striped-data transfer using four spindles completes four times faster than a data transfer using one spindle.

The DCA-3 hardware stripes data from a single I/O buffer path onto the disk array. Spindle 0 stores every fourth bit starting with bit 0, spindle 1 stores every fourth bit starting with bit 1, and so on, for spindles 2 and 3. The parity spindle stores odd parity calculated on each nibble written to the four data spindles. The spindles are synchronized to allow parallel data transfers.

Data buffers on the DCA-3 store 2 Kbytes of data for each spindle of the disk array. The data buffers store at least 75 μsec of data for each spindle, creating a synchronization tolerance of $\pm$ 37.5 μsec.

Programming the DCA-3 disk array is similar to programming the DCA-2 single-drive controller. When the DCA-3 issues drive commands such as cylinder seek commands, the disk array operates as a single logical drive. The disk array also operates as a single unit during normal read and write operations. Drive status functions are more complex than those of the DCA-2 because the status from each individual spindle can be unique.

Under normal operation, functions are fanned out to all spindles in the disk array. However, a spindle mask function (DCA3:17, M0 = 1) can be used to select an individual spindle within the array or to deselect an individual spindle within the array.

A single spindle is most often used by diagnostics and utilities for flaw maintenance and troubleshooting. Deselection of a single spindle (i.e., four-spindle mode) is used to recover from single-spindle failures. Data is read from the four active spindles and parity can be used to reconstruct the data from a failed spindle. Data writes can also be done in four-spindle mode. After a failed spindle is replaced, four-spindle mode is used for parity reconstruction of the data to the replacement spindle.

Data Format

The data format of each individual spindle is identical to the format specification of the drives used with the DCA-2. The same ID field, including a defect parameter, is contained in each sector, including 32 bytes of error-correction code (ECC) that protect the data. The parity data on spindle four is also protected by ECC.

The DCA-3 contains 40 ECC generators, eight for each spindle. This provides one generator for each bit within the read and write data bytes. Each ECC generator creates 32 bits of ECC per sector of data. This 32-bit ECC can detect any data bit(s) in error for its read and write path.

A 32-bit ECC provides a 21-bit correction vector and an 11-bit data correction mask field. The 21-bit correction vector field specifies the starting address of the defect. The 11-bit correction mask indicates which bits are in error.

For a write ECC function, the parity spindle stores parity from the ECC data sent to the data spindles in place of a generated ECC. When data is read from four spindles with data reconstruction enabled, the reconstructed data from the parity spindle and the three good data spindles is substituted for the data on the disabled spindle.

DCA-3 Options

The DCA-3 contains 12 options (four option types) that translate EIOP commands into IPI-2 protocol and transfer data between the EIOP and the disk array. These options are described below. Figure 13-2 is a block diagram of the options on the DCA-3.

7DK Option

The 7DK option provides the communication interface to the EIOP. Channel commands are transmitted from the EIOP to the DCA-3 on a 4-bit path. This path is also used by the DCA-3 to transmit status and response data back to the EIOP.

The 7DK option contains a spindle mask register that allows the DCA-3 to determine which spindles in the array are currently active. This mask is set using the DCA3:17 function. Drive commands issued to the DCA-3 are fanned out to all selected spindles. The DCA-3 monitors the done response for selected spindle(s) only. The DCA-3 supports selection of one, four, or five spindles at a time. Any attempt to select two or three spindles constitutes a command error.

SECDED and voltage statuses are monitored within the 7DK option. If a buffer data error occurs during a write to the array, a syndrome value and error count are sent to the 7DK from the 7DL option. Most other DCA-3 status information is delivered to the 7DK via the 6DM options. The DCA-3 statuses are requested via the DCA3:12 and DCA3:13 functions.

The 7DK option contains a transfer length register to set the number of data transfers between the drive and the EIOP buffer board. EIOP buffer board data transfers are controlled by the 7DK via the 7DL option. Transfer counts vary depending on the specific drive function issued. The transfer count values are set using the DCA3:4 function.

7DL Option

The 7DL option provides a hardware interface to the EIOP buffer board. Single-error correction/double-error detection (SECDED) functions are performed by the 7DL option. Data striping, parity generation, parity checking, and data reconstruction are also performed on the 7DL.

During write operations, the 7DL option receives each 72-bit data word from the EIOP buffer board in six 12-bit transfers. Each word contains 64 data bits and 8 check bits. The 7DL generates new check bits for each data word received from the EIOP buffer board. These check bits are compared to the 8 check bits, which arrived with each word. If the bits do not compare, the 7DL signals the 7DK option that a SECDED error has occurred and transfers the error count and syndrome values. If a single bit is corrupted, the 7DL corrects the data by toggling the bit in error.

After SECDED checking occurs on the write data, the 7DL option stripes the data across four paths; each path is assigned to one of the data spindles. Every fourth bit of data, starting with bit 0, is sent to spindle 0 (4n data). Spindle 1 receives every fourth bit starting with bit 1 (4n+1 data), etc. While striping the data, the 7DL generates an odd parity bit for each nibble sent to the data spindles. This nibble parity bit becomes the write data stream for path 4 (parity spindle).

In addition to generating nibble parity, the 7DL option also generates an odd parity bit for each byte of data transferred to the spindles on bus A and bus B. Table 13-1 shows the bit striping and distribution on the DCA-3.

Table 13-1. DCA-3 Disk Array Data Striping

Spindle		Cray Data Word																	
0	P	60	52	44	36	56	48	40	32	P	28	20	12	4	24	16	8	0
1	P	61	53	45	37	57	49	41	33	P	29	21	13	5	25	17	9	1
2	P	62	54	46	38	58	50	42	34	P	30	22	14	6	26	18	10	2
3	P	63	55	47	39	59	51	43	35	P	31	23	15	7	27	19	11	3
4	P	Nibble Parity								P	Nibble Parity							
IPI Bus	P	Bus A (byte 1)								P	Bus B (byte 0)							

P = Byte Parity protection for transfer on the IPI Bus
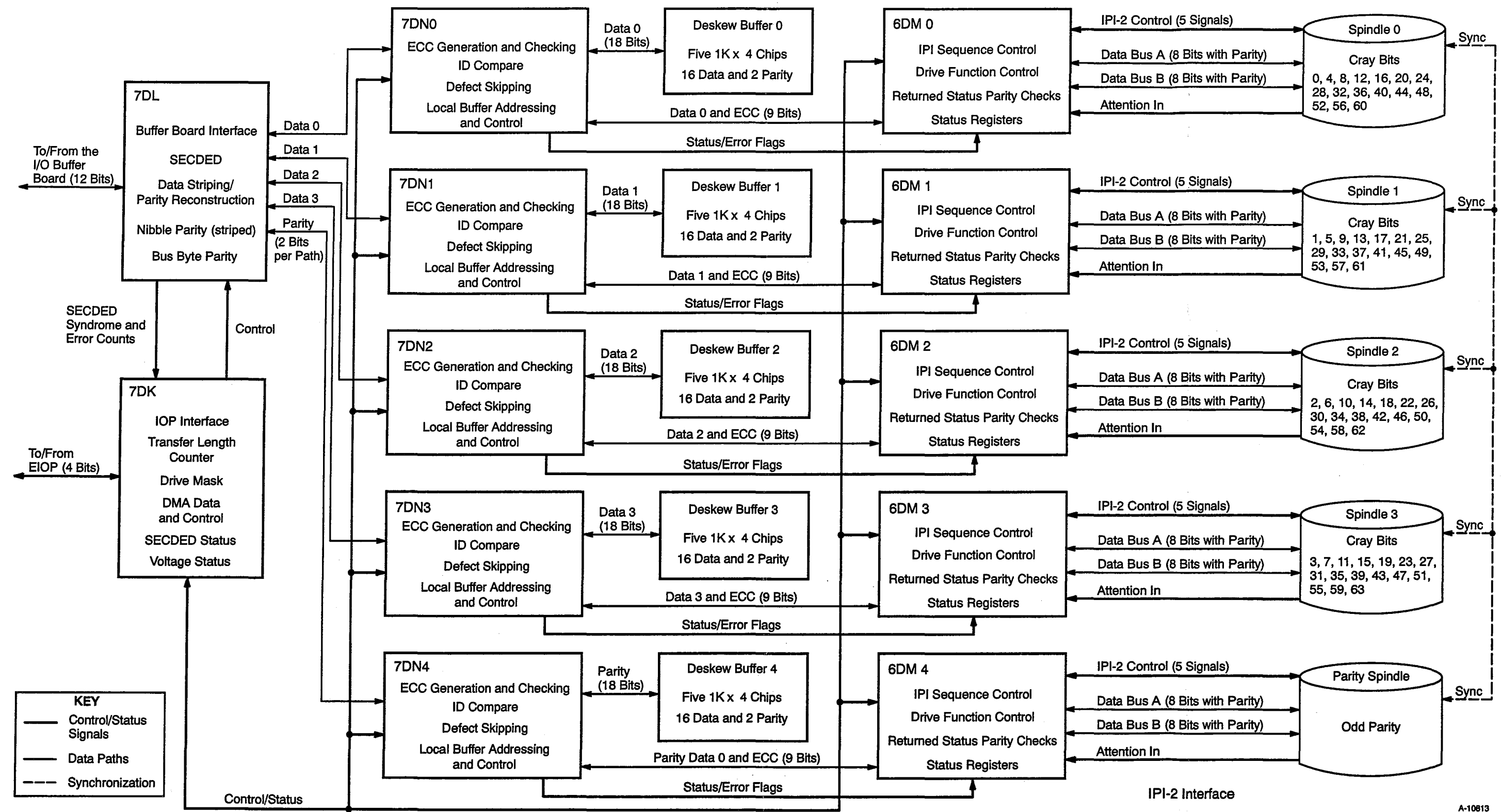
Figure 13-2. DCA-3 Block Diagram

During read operations, the 7DL option receives data from each selected spindle through the appropriate 7DN options. Parity checking is performed on each nibble of striped data using the information read from the parity spindle. Nibble parity errors are flagged by setting bit 7 of the interrupt status parcel (data parity error). In addition, parity checking is performed on each byte of data as it is received from its respective spindle (bus parity). Byte parity errors are flagged by setting bit 0 of the interrupt status parcel (drive parity error).

If a nibble parity error occurs, ECC and status information can be examined to determine which spindle within the array returned the corrupted data. Once the spindle (data stream) is identified, information read from the parity spindle can be used to reconstruct the corrupted data stream. If a spindle within the array is disabled, the 7DL option automatically uses the information from the parity spindle to reconstruct data from the disabled spindle until it is enabled again.

Once parity checking and/or data reconstruction is complete, the 7DL option generates 8 check bits for each 64-bit word to be transmitted to the EIOP buffer board. Each 72-bit word is then sent to the buffer board in six 12-bit transfers.

7DN Options

Five 7DN options reside on the DCA-3, each assigned to handle data for one of the five spindles. Each 7DN option receives write/read data and caches the data in a dedicated deskew buffer. At the appropriate time, the 7DN reads the data from the deskew buffer for transfer to the next option.

Each 7DN option performs most of the functions of an entire DCA-2 channel adapter. The 7DN options handle control of the deskew buffers, ID compare, ECC generation and checking, and defect skipping.

Under normal operations, the read and compare of sector ID field information must precede the transfer of customer data. The ID field data is received by the 7DN options and compared to expected values held in parameter registers 0 and 1. If the actual ID data does not match the expected values, an ID compare error is flagged by setting bit 8 of the interrupt status. In addition, ECC checking is also performed on the ID field data. All ECC errors are flagged by setting bit 9 of the interrupt status. Refer to the "DCA-3 Systems Status" section of this manual for additional status information.

During write operations, each 7DN option receives write data from the 7DL option in 2-bit transfers. The 7DN assembles the data into 2-byte parcels including the parity bit on each byte. The 7DN stores each parcel (16 data bits and 2 parity bits) to a unique location in its associated deskew buffer starting at address location 0. When the spindle is ready

to receive write data, the 7DN reads the data from the deskew buffer for transfer to the disk via the respective 6DM option. As the data is read out of the deskew buffer, each byte is striped across eight ECC circuits in the 7DN option; ECC0 receives bit 0 of each byte, EEC1 receives bit 1 of each byte, and so on. ECC generation is not performed on the byte parity bits read from the deskew buffer; however, the 7DN4 option can generate ECC protection on the nibble parity data for transfer to the parity spindle. Each of the eight ECC circuits generates a 32-bit ECC code.

Defect pad detection and skipping is also performed by the 7DN options. The defect address from a spindle sector is read into the respective 7DN as part of the ID field. When the spindle head is at the beginning of the defect pad, the 7DN stops incrementing the deskew buffer addressing and starts decrementing a defect counter to count the length of the defect pad. The defect length count is different for DD–60 and DD-62 spindles. While the head crosses over the defect pad, the 7DN repeats (stutters) the next valid parcel of data to create the defect pad. When the defect counter has decremented to 0, indicating the end of the defect area, the 7DN resumes reading valid write data from the deskew buffer for transfer to the spindle.

During read operations, each 7DN option receives read data parcels from its associated 6DM option in two 9-bit transfers (8 data bits plus parity). Each data parcel is written to the deskew buffer along with both parity bits. At the proper time, the data parcels are read out of the buffer and split into two bytes. Each byte is striped across the eight ECC circuits for regeneration of the 32-bit protection code. At the completion of the data transfer, the regenerated ECC is compared to the ECC information read from the spindle. If the ECC information does not compare, the error is flagged by bit 9 of the interrupt status (ECC error). The DCA3:1 channel function is used to examine all 40 ECC registers to determine which data stream is in error. After the data ECC is checked, the read data from each of the 7DN options is sent to the 7DL option in 2-bit transfers.

Deskew Buffers

The DCA-3 includes five deskew buffers that provide data buffering for each of the spindle data paths. All control and addressing of the deskew buffers is performed by the respective 7DN options. Each buffer comprises five memory chips. Each chip contains 1024 addresses; each address holds four bits of data. Four of these chips hold read/write data, and the fifth chip stores the two parity bits. Each deskew buffer stores up to 75 µs of data, allowing a total synchronization tolerance of $\pm$ 37.5 µs between spindles. This tolerance also allows the DCA-3 to handle defect skipping individually for each spindle. For example, data transfers can occur on four of the spindles while a defect pad is being skipped on the fifth.

6DM options

The DCA-3 contains five 6DM options, one for each of the spindles of the array. The 6DM options maintain the IPI protocol and sequencing between the DCA-3 and the spindles. Unlike the DCA-2, there is no microcode firmware on the DCA-3; sequencing is performed by the design logic. Most error conditions detected by the 7DN options are reported to status registers in the 6DM options. These statuses are subsequently transferred to the channel via the 7DK option. The 6DM options also perform parity checking on the IPI buses during ending status sequences and other non-data transfers. All read data destined for the EIOP buffer board is passed through the 6DM options without a parity check. Parity checking for read data is performed by the 7DL option.

During write operations, each 6DM option receives write data parcels in two 9-bit transfers (8 data bits plus parity) from the associated 7DN option. The 6DM transfers each parcel of data to the spindle by placing the even byte (0) on bus B and the odd byte (1) on bus A. Each transfer on the buses is accompanied by a Sync Out pulse.

During read operations, each 6DM option receives a parcel of data on each transfer from the spindle; an even byte arrives on bus B while the odd byte arrives on bus A. Each byte transferred on the A and B buses is accompanied by a parity bit. The 6DM transfers the read data parcels to the respective 7DN option in two 9-bit transfers (8 data bits plus parity).

DA-60 and DA-62 Data Striping

Although data striping on the DCA-3 is the same for the DA-60 and DA-62 disk arrays, the data is handled differently on each of the two spindle types. In the following pages, Table 13-2 shows how the data is striped on a DA-60 and Table 13-3 shows data striping on a DA-62.

DCA-3 Handling Precautions

The DCA-3 channel adapter is fragile and must be handled with extreme care. Observe all precautions to ensure that nothing comes in contact with the surface of this half-board. Handle the DCA-3 by the edge connectors only and observe all electrostatic discharge (ESD) precautions. Refer to Figure 13-3 for information on the physical layout of the DCA-3 channel adapter.

Table 13-2. DCA-3 to DA-60 Data Bit Distribution

Spindle	Cray Data Word																
0	60	52	44	36	56	48	40	32	28	20	12	4	24	16	8	0	
1	61	53	45	37	57	49	41	33	29	21	13	5	25	17	9	1	
2	62	54	46	38	58	50	42	34	30	22	14	6	26	18	10	2	
3	63	55	47	39	59	51	43	35	31	23	15	7	27	19	11	3	
4	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	
Head in 8-head group	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
IPI bus	BUS A (byte 1)								BUS B (byte 0)								Byte Parity
Memory chip location for spindle 0 data	AAE3				AAE2				AAE1				AAE0				AAE4
Memory chip location for spindle 1 data	ACB3				ACB2				ACB1				ACB0				ACB4
Memory chip location for spindle 2 data	AEB3				AEB2				AEB1				AEB0				AEB4
Memory chip location for spindle 3 data	AFB3				AFB2				AFB1				AFB0				AFB4
Memory chip location for spindle 4 data	AAB3				AAB2				AAB1				AAB0				AAB4

Table 13-3. DCA-3 to DA-62 Data Bit Distribution

Spindle	Cray Data Word																
0	60	52	44	36	56	48	40	32	28	20	12	4	24	16	8	0	
1	61	53	45	37	57	49	41	33	29	21	13	5	25	17	9	1	
2	62	54	46	38	58	50	42	34	30	22	14	6	26	18	10	2	
3	63	55	47	39	59	51	43	35	31	23	15	7	27	19	11	3	
4	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	parity	
Head in 2-head group	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	
IPI bus	BUS A (byte 1)				BUS B (byte 0)												Buffer Parity
Memory chip location for spindle 0 data	AAE3				AAE2				AAE1				AAE0				AAE4
Memory chip location for spindle 1 data	ACB3				ACB2				ACB1				ACB0				ACB4
Memory chip location for spindle 2 data	AEB3				AEB2				AEB1				AEB0				AEB4
Memory chip location for spindle 3 data	AFB3				AFB2				AFB1				AFB0				AFB4
Memory chip location for spindle 4 data	AAB3				AAB2				AAB1				AAB0				AAB4

Figure 13-3. DCA-3 Board Assembly

SECTION 14
DCA-3 CHANNEL FUNCTIONS

14 DCA-3 CHANNEL FUNCTIONS

Channel functions for the DCA-3 channel adapter transfer information for disk array operations to registers in the DCA-3 and input/output processor (EIOP). This section describes each channel function.

Channel Function Descriptions

Table 14-1 lists the DCA-3 channel functions and describes them briefly.

Table 14-1. DCA-3 Channel Functions

Function	Description
DCA3:0	Clear channel flags
DCA3:1	Start Transfer Start input transfer (even channel) M3, M2, M1, M0 = 0001: Read drive response M3, M2, M1, M0 = 0101: Read ECC registers Start output transfer (odd channel) M3, M2, M1, M0 = 0000: Write drive command
DCA3:2	Set ID parameter 0 (cylinder address)
DCA3:3	Set ID parameter 1 (head and sector address)
DCA3:4	Set transfer count
DCA3:5	Start device function
DCA3:6	Clear interrupt enable flag
DCA3:7	Set interrupt enable flag
DCA3:10	Read local memory address
DCA3:11	Read inverted local memory parcel count
DCA3:12	Read status 0
DCA3:13	Read status 1
DCA3:14	Set local memory starting address
DCA3:15	Set local memory parcel count
DCA3:16	Write control bus data
DCA3:17	M0 = 0: Set Array Type M0 = 1: Set Array Mode

Except for DCA3:1, functions of an even channel with M0=0 are functions to the a-pointer and functions to an odd channel with M0=1 are functions to the b-pointer. Figure 14-1 shows the bit assignments for the modifier (M) bits and channel number in the d field or B Register.

$$\longleftarrow \quad d \text{ Field or B Register} \longrightarrow$$

2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
M 2^3	M 2^2	M 2^1	M 2^0	C 2^4	C 2^3	C 2^2	C 2^1	C 2^0
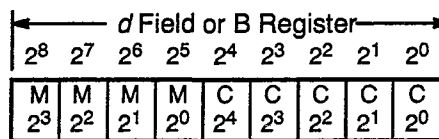
M = Function Modifier Bits
C = Channel Number

Figure 14-1. EIOP Instruction d Field or EIOP B Register

DCA3:0 – Clear Channel Flags

The DCA3:0 function resets the EIOP channel busy and channel done flags to 0 or performs a master clear of the channel.

Channel function DCA3:0 also clears the following status bits:

- Interrupt status bits 2^0 through 2^3 and bits 2^6 through 2^{10}

- SECDED status bits 2^8 through 2^{15}

- All drive busy, drive done, and DMA acknowledge pending bits

DCA3:1 - Start Transfer

The DCA3:1 function starts data transfers between the EIOP local memory and the DCA-3 channel adapter. The condition of function modifier bit 0 determines the direction of the transfer; bits 1 through 3 determine the type of transfer. Refer to Table 14-2 for a list of the modifier bit values used with the DCA3:1 function.

DCA3:1 - Start Input Transfer (even channel)

This function initiates a data transfer from the channel adapter to EIOP local memory. Modifier bit M0 must be set to 1. Bit M2 determines what data is transferred (refer again to Table 14-2).

Table 14-2. DCA3:1 Function Modifier Bits

Modifier Bits 2^3	2^2	2^1	2^0	Description
0	0	0	0	Drive command control function (odd channel)
0	0	0	1	Drive response function (even channel)
0	1	0	1	Read ECC register (even channel)

The even channel operation of this function (for both defined combinations) is as follows:

M3	M2	M1	M0	Operation
0	0	0	1	Drive response function. This function is an interlocked transfer and provides command status information. The lower four bits of the accumulator must be 6_8 (refer to Figure 14-2). The lower byte of the previous DCA3:16 function sent to the odd channel is a response control byte sent to all spindles, which causes them to return information. Parcel 0 from spindles 0 through 4 is stored as parcels 0 through 4 in local memory; parcel 1 is stored as parcels 5 through 9; and so forth.

A done flag for the odd-numbered channel indicates that all spindles have completed their responses. A done flag for the even-numbered channel indicates that the response data has been stored in local memory. The transfer length should be set to the number of parcels expected from one spindle. The local memory parcel count should be set to five times the transfer length. If a spindle is not selected, its locations in local memory are filled with indeterminate data.

←	Accumulator Contents	→

2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
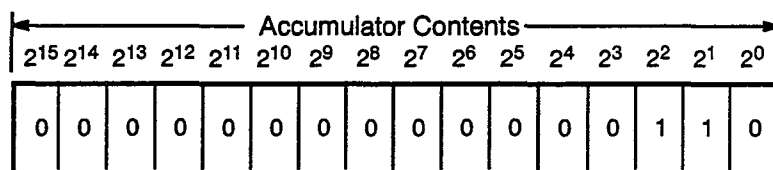
Figure 14-2. DCA3:1 Accumulator Contents for Drive Response

M3	M2	M1	M0	Operation
0	1	0	1	Read ECC register. This function transfers the contents of the ECC registers to local memory. Parcel 0 of the ECC from spindle 0 is transferred first, followed by parcel 0 of the ECC from spindle 1. Parcel 15 of the ECC from spindle 4 is transferred last. The transfer length should be set to 16_{10} (20_8). The local-memory parcel count should be set to 80_{10} (120_8) to receive five 16-parcel ECCs.

DCA3:1 - Start Output Transfer (odd channel)

This function initiates a data transfer from EIOP local memory to the channel adapter. Modifier bit M0 must be cleared to 0. Bits M1 and M3 determine what data is transferred.

The operation of this function for the only defined combination of M0 through M3 is described in the following paragraphs.

M3	M2	M1	M0	Operation
0	0	0	0	Drive command control function. This function transfers information from IOP local memory to all selected spindles. The lower four bits of the accumulator must be set to 04_8 (refer to Figure 14-3). This information transfer follows, and supports, a drive command control byte previously transferred on the even channel with a DCA3:16 function.

A done flag for the odd channel indicates that all data has been sent from local memory. A done flag for the even channel indicates that the drive function has been completed. The transfer length count is not used.
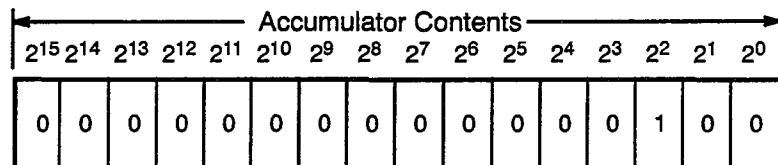
Figure 14-3. DCA3:1 Accumulator Contents for Drive Command

DCA3:2 – Set ID Parameter 0

The DCA3:2 function transfers the requested cylinder address (ID parameter 0) from the accumulator to the cylinder register in the 7DN options of the DCA-3. Figure 14-4 shows the format of ID parameter 0 in the accumulator.
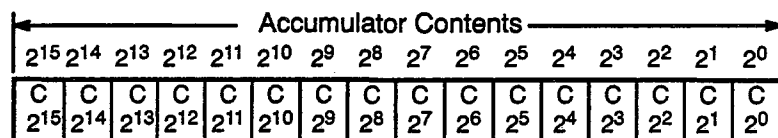
C = Cylinder Address

Figure 14-4. ID Parameter 0 Format

NOTE: Sector ID fields are formatted using the DCA3:5 function with a device function code of 25_8.

DCA3:3 – Set ID Parameter 1

The DCA3:3 function transfers the requested sector address, head address, and option bits (ID parameter 1) from the accumulator to the parameter register in the 7DN options of the DCA-3. Figure 14-5 shows the format of ID parameter 1 in the accumulator. Refer to the "Format and Flaw Management" disk drive sections of this manual for more information on the ID bit descriptions (which include ID parameter 1).

	Accumulator Contents														
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
X	X	WP	RP	X	H	H	H	H	H	S	S	S	S	S	S
x	x	2^0	2^0	x	2^4	2^3	2^2	2^1	2^0	2^5	2^4	2^3	2^2	2^1	2^0

X = Not Used   RP = Read Protected
WP = Write Protected   H = Head Group Address
                                       S = Sector Address
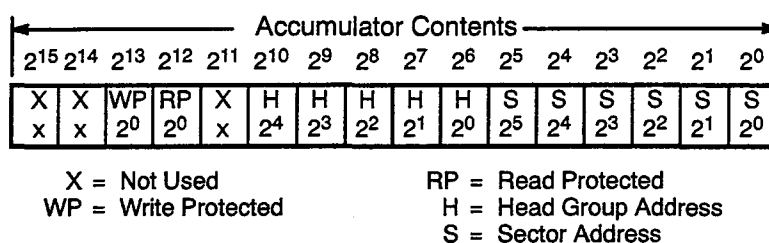
Figure 14-5. ID Parameter 1 Format

NOTE: Sector ID fields are formatted using the DCA3:5 function with a device function code of 25_8.

DCA3:4 – Set Transfer Count

The DCA3:4 function transfers the transfer count from the accumulator to the DCA-3. Figure 14-6 shows the format of the transfer count in the accumulator.

	Accumulator Contents														
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
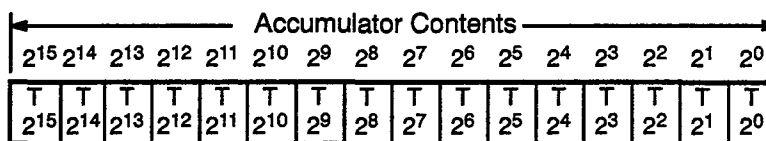
T = Transfer Count

Figure 14-6. Transfer Count Format

Transfer count values can be decoded by the DCA-3 as bytes, parcels, or halfwords depending on the type of transfer initiated. Transfer types are determined by the number of spindles being referenced and the device function issued. Table 14-3 defines the transfer count settings.

Table 14-3. DCA-3 Transfer Counts

Transfer Type	Transfer Count Setting
Data transfer (array mode)	Sector size (halfwords): 040000_8 ($16,384_{10}$) for DA-60 010000_8 ($4,096_{10}$) for DA-62
Data transfer (single spindle mode)	Sector size (bytes): 040000_8 ($16,384_{10}$) for DA-60 010000_8 ($4,096_{10}$) for DA-62
Read or write data to/from buffer board with ECC	Sector size (halfwords) + 32_{10}: 040040_8 ($16,416_{10}$) for DA-60 010040_8 ($4,128_{10}$) for DA-62
Read (verify) sector ID or Write (format) sector ID	Sector ID size (parcels): 000004 for DA-60 and DA-62 a (does not include ID ECC data)

DCA3:5 - Start Device Function

Bits 2^0 through 2^4 of the accumulator contain the device function interpreted by the DCA-3 controller. Figure 14-7 shows the accumulator format. Device functions 5, 7, and 17 through 27 use the lower byte of the DCA3:16 function data as a command control code. The sequence error flag is set if the drive interface is not initially in the SLAVE ACKNOWLEDGE (slaveack) state for all bus control functions. Table 14-4 provides detailed descriptions of the device functions supported by the DCA-3.

← ——————— Accumulator Contents ——————— →
2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^9 2^8 2^7 2^6 2^5	2^4 2^3 2^2 2^1 2^0
Not Used	Device Function Code
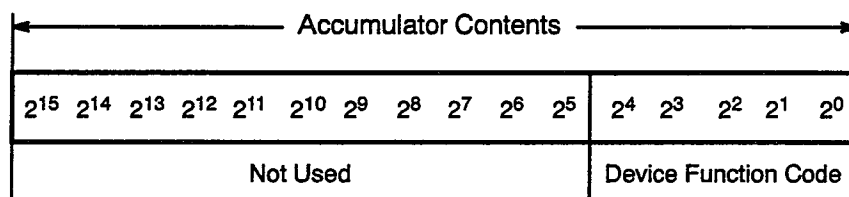
Figure 14-7. DCA3:3 Parameter 1 Control Parcel

Table 14-4. DCA3:5 Device Function Descriptions

Function (Octal)	Device Function Type	Description
00	Write data buffer	Data from the I/O buffer is written into the drive data buffers of the DCA-3 controller. Each word of data is sent to every drive data buffer. The maximum transfer length is 1 Kparcel.
01	Write data buffer striped	This function stores the data from the I/O buffer in the drive data buffers. The transfer length count should be set to 2000 halfwords ($4,096_{10}$ parcels).
02	Read data buffer	Data is transferred from the drive data buffers to the I/O buffer. Word 0 of I/O buffer data is the first word from the drive 0 buffer, word 1 of I/O buffer data is the first word from the drive 1 buffer, and so on. The maximum transfer length is 374_8 parcels.
03	Read data buffer striped	The current contents of the drive data buffers are transferred to the I/O buffer. A parity check from the parity drive buffer is performed if all spindles are selected. Data reconstruction can also be enabled for this reason. This function can be used as part of a diagnostic test of the drive data buffers.
05	Drive command control function	The lower byte of the previous DCA3:16 function is a command control byte. Data from the I/O buffer is sent to all spindles. The transfer length count should be the number of parcels to be sent to the spindles.
07	Drive response control function	The lower byte of the previous DCA3:16 function is a response control byte. Response data from the drives is sent to the I/O buffer. After the transfer completes, word 0 of the I/O buffer contains the first 4 parcels of data received from drive 0. Word 1 contains the first 4 parcels of drive 1. The transfer length count should be set to the number of parcels expected from each spindle.
10	Request interrupts poll	The response from a request interrupt sequence is ANDed with the upper bits of the accumulator. The channel status signals done when the results of the AND functions are nonzero for all selected spindles. A DCA3:0 function terminates this function.
11	Request slave interrupts or transfer settings	This function reports data as defined on the A bus. The drives with the status pending respond by putting the radial address on the B bus.
12	Request interrupt	This function reports interrupt status on the B bus from the spindle designated by the A bus.
13	Select	The ending status error flag sets if the drive response is zero. A sequence error flag sets if the interface is not initially in the idle state or if the drive does not respond in 100µs.
14	Deselect	The sequence error flag sets if the drive interface is not initially in the slave acknowledge (slavack) state.
15	Master reset	This function turns off the drive interface.
16	Selective reset	The sequence error flag sets if the drive is not initially in the idle state. This function then performs a reset function as defined by bits 0–2 on the A bus.

Table 14-4. DCA3:5 Device Function Descriptions (continued)

Function (Octal)	Device Function Type	Description
17	Command with no information transfer	The lower byte of the previous DCA3:16 function is used as a command control in a bus exchange sequence. The bus control sequence is terminated before any information is transferred.
20	Read sector data	This function reads the header data-in bus exchange sequence using bus control in the lower byte of DCA3:16 until ID compare and ECC checking is complete. The field data-in bus exchange sequence uses bus control in the upper byte of DCA3:16 and checks ECC.
21	Read sector ID	This function reads the header using bus control in the lower byte of DCA3:16 and checks ECC. Parcels 0 through 3 of the ID are transferred to the I/O buffer.
22	Read sector absolute	This function reads the header at the target data-in bus exchange sequence using bus control in the lower byte of DCA3:16, without ID compare and without checking ECC. The field data-in exchange sequence uses bus control in the upper byte of DCA3:16 and checks ECC.
23	Read sector data and ECC to the I/O buffer	This function reads the header data-in bus exchange sequence using bus control in the lower byte of DCA3:16 until ID compare and ECC checking is complete. The field data-in bus exchange sequence uses bus control in the upper byte of DCA3:16 without checking ECC. ECC is included in the data passed to the I/O buffer.
24	Write sector data	This function reads the header data-in bus exchange sequence using bus control in the lower byte of DCA3:16 until ID compare and ECC checking is complete. The write field data-out bus exchange sequence uses bus control in the upper byte of DCA3:16 and generates ECC.
25	Write sector ID (format)	This function writes the header at the target data-out bus exchange sequence using bus control in the lower byte of DCA3:16 and generates ECC.
27	Write sector data and ECC from the I/O buffer	This function reads the header data-in bus exchange sequence using bus control in the lower byte of DCA3:16 until ID compare and ECC checking is complete. A write field data-out bus exchange sequence uses bus control in the upper byte of DCA3:16 without generating ECC. (ECC is part of the data from the I/O buffer.)

DCA3:6 – Disable Interrupt Enable Flag

The DCA3:6 function sets the EIOP channel enable interrupt flag to 0. When the enable interrupt flag is 0, the channel does not acknowledge any interrupts it receives. This function does not change the states of the channel busy or channel done flags.

DCA3:7 – Enable Interrupt Enable

The DCA3:7 function sets the EIOP channel enable interrupts flag to 1. When the enable interrupt flag is 1, the channel acknowledges any interrupts it receives. This function does not change the states of the busy and done flags.

DCA3:10 – Read Local Memory Address

The DCA3:10 function transfers the current local memory address from the EIOP channel local-memory address register to the accumulator. Figure 14-8 shows the format of the local memory address in the accumulator.

|←———————— Accumulator Contents ————————→|
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
LM 2^{15}	LM 2^{14}	LM 2^{13}	LM 2^{12}	LM 2^{11}	LM 2^{10}	LM 2^9	LM 2^8	LM 2^7	LM 2^6	LM 2^5	LM 2^4	LM 2^3	LM 2^2	LM 2^1	LM 2^0
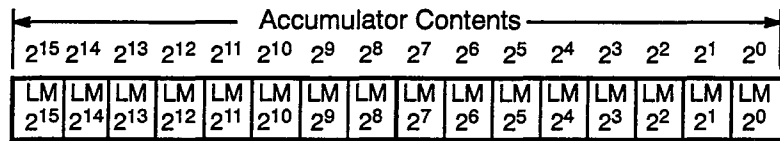
LM = Current Local Memory Address

Figure 14-8. Current Local Memory Address Format

DCA3:11 – Read Inverted Local Memory Parcel Count

The DCA3:11 function transfers the inverse of the EIOP channel parcel counter to the accumulator. To obtain the correct parcel count, the accumulator contents must be subtracted from 177777_8. Figure 14-9 shows the format of the inverted parcel count in the accumulator.

|←———————— Accumulator Contents ————————→|
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
IP 2^{15}	IP 2^{14}	IP 2^{13}	IP 2^{12}	IP 2^{11}	IP 2^{10}	IP 2^9	IP 2^8	IP 2^7	IP 2^6	IP 2^5	IP 2^4	IP 2^3	IP 2^2	IP 2^1	IP 2^0
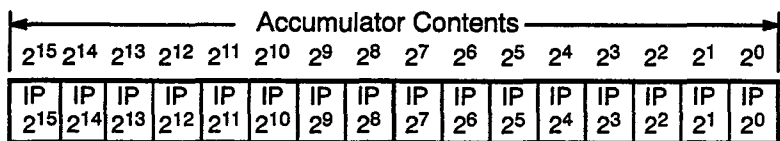
Figure 14-9. Inverted Parcel Count Format

DCA3:12 - Read Status 0

This function transmits one of seven status parcels to the accumulator. The contents of accumulator bits 2^0, 2^1, and 2^2 when the function is issued, determine which status parcel is returned. Table 14-5 shows the seven available status parcels.

Table 14-5. DCA3:12 Status Parcels

Bit	000 Interrupt Status	001 SECDED Status	010 Transfer Count	011 Control Bus Status	100 Busy Status	101 Done Status	110 DMA Ack. Pending Status	111
2^0	Spindle parity error	Syndrome bit 0	Transfer count 2^0	Select out	Spindle 0 busy	Spindle 0 done	Spindle 0 pending	Not Used
2^1	Sequence error	Syndrome bit 1	Transfer count 2^1	Slave-in	Spindle 1 busy	Spindle 1 done	Spindle 1 pending	Not Used
2^2	Lost data error	Syndrome bit 2	Transfer count 2^2	Master-out	Spindle 2 busy	Spindle 2 done	Spindle 2 pending	Not Used
2^3	Ending status error	Syndrome bit 3	Transfer count 2^3	Sync-in	Spindle 3 busy	Spindle 3 done	Spindle 3 pending	Not Used
2^4	−4.5 V voltage fault	Syndrome bit 4	Transfer count 2^4	Sync-out	Spindle 4 busy	Spindle 4 done	Spindle 4 pending	Not Used
2^5	+5.0 V voltage good	Syndrome bit 5	Transfer count 2^5	Attention-in	Not Used	Not Used	Not Used	Not Used
2^6	SECDED error	Syndrome bit 6	Transfer count 2^6	Gate bus A out	Not Used	Not Used	Not Used	Not Used
2^7	Data parity error	Syndrome bit 7	Transfer count 2^7	Gate bus B out	Not Used	Not Used	Not Used	Not Used
2^8	ID compare error	Single-bit error count 2^0	Transfer count 2^8	Not Used	Not Used	Not Used	Not Used	Not Used
2^9	ECC error	Single-bit error count 2^1	Transfer count 2^9	Not Used	Not Used	Not Used	Not Used	Not Used
2^{10}	ID error	Single-bit error count 2^2	Transfer count 2^{10}	Not Used	Not Used	Not Used	Not Used	Not Used
2^{11}	Hidable flaw	Single-bit error count 2^3	Transfer count 2^{11}	Not Used	Not Used	Not Used	Not Used	Not Used
2^{12}	Unhidable flaw	Double-bit error count 2^0	Transfer count 2^{12}	Not Used	Not Used	Not Used	Not Used	Not Used
2^{13}	ID field flaw	Double-bit error count 2^1	Transfer count 2^{13}	Not Used	Not Used	Not Used	Not Used	Not Used
2^{14}	Write protect	Double-bit error count 2^2	Transfer count 2^{14}	Not Used	Not Used	Not Used	Not Used	Not Used
2^{15}	Read protect	Double-bit error count 2^3	Transfer count 2^{15}	Not Used	Not Used	Not Used	Not Used	Not Used

The following information applies to the seven status parcels shown in Table 14-5:

- Issuing a DCA3:0 function clears the following status bits:

    - Interrupt status bits 2^0 through 2^3 and bits 2^6 through 2^{10}

    - SECDED status bits 2^8 through 2^{15}

    - All spindle busy, spindle done, and DMA acknowledge pending status bits.

- The spindle busy and spindle done status parcels are intended to simplify the process of isolating a failure to an individual spindle. When a function is completed with an error, the busy and done flags set. If a failure, such as a spindle parity error, can be attributed to an individual spindle, the busy and done flags for each spindle can be read to determine which spindle had the error. The DMA acknowledge pending status can be used to isolate a hung local memory command or response control to a particular spindle.

- Unlike the DCA-2, stacked functions proceed on the DCA-3 even if the previous function ended in error.

The following information applies to the interrupt status (DCA3:12 accumulator = 0) parcel:

- Bits 2^0 through 2^3 and bits 2^8 through 2^{15} of the interrupt status and all bits of the control bus status are logical ORs of the information from each selected spindle.

- Bits 2^{11} through 2^{15} of the interrupt status are copies from the ID field during the last ID compare operation. If bits $2^{12,}$ 2^{13} or 2^{14} are set, they will result in a busy/done condition. Bits 2^{11} and 2^{15} are informational only.

- Single-bit SECDED errors do not cause the busy flag to remain set after a function has completed.

- If bits 2^0 through 2^3, 2^8, 2^9, and 2^{10} of the interrupt status parcel are set, the individual spindle controller that had the error remains busy after a function has completed.

- Bit 2^0 (spindle parity error) indicates that the spindle response data or that the spindle read data had a parity error.

- Bit 2^1 (sequence error) indicates that a spindle function was attempted from an invalid initial IPI state or that a Select signal timed out.

- Bit 2^2 (a lost data error) is set if the I/O buffer data is not supplied to the spindle data buffer early enough during a write, or if the spindle data buffer is not sent to the I/O buffer quickly enough during a read. Loss of spindle synchronization is one cause of a lost data error. If one spindle has a lost data error, that spindle may be out of sync. If all spindles but one have lost data errors, the one spindle without a lost data error may be out of sync.

- Bit 2^3 (an ending status error) is set after a bus control sequence completes if the spindle ending status bits 2^0 through 2^3 are nonzero, if bit 6 has a parity error, or if bit 2^7 is zero.

- Bits 2^4 and 2^5 (voltage faults) are informational only and do not result in any hardware-initiated action.

- Bit 2^6 indicates a SECDED error. This bit is set if either the single-bit error count or the double-bit error count is not zero.

- Bit 2^7 (data parity error) is set when any nibble parity errors are detected and can occur only during striped reads with all spindles enabled.

- Bit 2^{10} (ID error) is set if a write or a read is stopped by an ID error. Bits 2^8, 2^9, 2^{12}, and 2^{13} provide further information if there is an ID error. If an ID error is detected, a parity error may occur because the data read did not occur. If only bit 2^9 (ECC error) is set, the ECC error occurred after the data field read. Bit 2^9 can be the only bit set if there is an ECC error on a read ID function.

DCA3:13 - Read Status 1

This function transmits one of four status parcels to the accumulator. When the function issues, the contents of accumulator bits 2^0 and 2^1 determine which status parcel is returned. Table 14-6 shows the four status parcels.

Each of the status parcels is a logical OR of the information from each selected spindle. Function DCA3:17 (M0 = 1) determines which spindles are selected.

Table 14-6. DCA3:13 Status Parcels

| Bit | Accumulator Bits 2^1 and 2^0 | | | |
	00 Ending Status	01 ID Parameter 0	10 ID Parameter 1	11 Bus A and Bus B Data
2^0	Ending status 0 bit 0	Cylinder bit 0	Sector bit 0	Bus B data bit 0
2^1	Ending status 0 bit 1	Cylinder bit 1	Sector bit 1	Bus B data bit1
2^2	Ending status 0 bit 2	Cylinder bit 2	Sector bit 2	Bus B data bit 2
2^3	Ending status 0 bit 3	Cylinder bit 3	Sector bit 3	Bus B data bit 3
2^4	Ending status 0 bit 4	Cylinder bit 4	Sector bit 4	Bus B data bit 4
2^5	Ending status 0 bit 5	Cylinder bit 5	Sector bit 5	Bus B data bit 5
2^6	Ending status 0 bit 6	Cylinder bit 6	Head group 0	Bus B data bit 6
2^7	Ending status 0 bit 7	Cylinder bit 7	Head group 1	Bus B data bit 7
2^8	Ending status 1 bit 0	Cylinder bit 8	Head group 2	Bus A data bit 0
2^9	Ending status 1 bit 1	Cylinder bit 9	Head group 3	Bus A data bit 1
2^{10}	Ending status 1 bit 2	Cylinder bit 10	Head group 4	Bus A data bit 2
2^{11}	Ending status 1 bit 3	Cylinder bit 11	Not used	Bus A data bit 3
2^{12}	Ending status 1 bit 4	Cylinder bit 12	Not used	Bus A data bit 4
2^{13}	Ending status 1 bit 5	Cylinder bit 13	Not used	Bus A data bit 5
2^{14}	Ending status 1 bit 6	Cylinder bit 14	Not used	Bus A data bit 6
2^{15}	Ending status 1 bit 7	Cylinder bit 15	Not used	Bus A data bit 7

DCA3:14 - Set Local Memory Starting Address

The DCA3:14 function transfers the local memory starting address from the accumulator to the EIOP channel local-memory address register. The local memory starting address is the EIOP local memory address that contains the first parcel of data to be transferred to the DCA-3, or the

EIOP local memory address to which the DCA-3 transfers the first parcel of data. Figure 14-10 shows the format of the local memory starting address in the accumulator.

|←————————— Accumulator Contents —————————→|
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
LS 2^{15}	LS 2^{14}	LS 2^{13}	LS 2^{12}	LS 2^{11}	LS 2^{10}	LS 2^9	LS 2^8	LS 2^7	LS 2^6	LS 2^5	LS 2^4	LS 2^3	LS 2^2	LS 2^1	LS 2^0
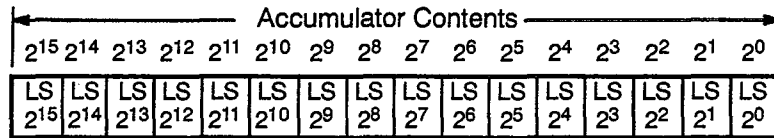
LS = Local Memory Starting Address

Figure 14-10. Local Memory Starting Address Format

During a data transfer, the local memory address register of the channel automatically increments once with each parcel transferred. Execute the DCA3:10 function to transfer the current value of the local memory address register of the channel to the accumulator.

DCA3:15 – Set Local Memory Parcel Count

The DCA3:15 function transfers the local memory parcel count from the accumulator to the EIOP channel parcel counter. The parcel count is the number of parcels to be transferred between the EIOP local memory and the DCA-3. Figure 14-11 shows the format of the parcel count in the accumulator.

|←————————— Accumulator Contents —————————→|
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
PC 2^{15}	PC 2^{14}	PC 2^{13}	PC 2^{12}	PC 2^{11}	PC 2^{10}	PC 2^9	PC 2^8	PC 2^7	PC 2^6	PC 2^5	PC 2^4	PC 2^3	PC 2^2	PC 2^1	PC 2^0
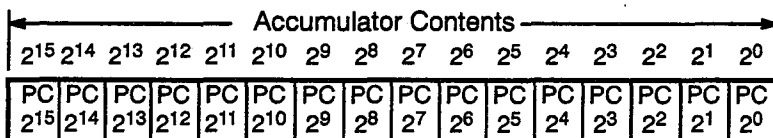
PC = Parcel Count

Figure 14-11. Parcel Count Format

During a data transfer, the channel parcel counter automatically decrements once for each parcel transferred. Execute the DCA3:11 function to transfer the inverted current value of the channel parcel counter to the accumulator.

DCA3:16 – Write Control Bus Data

The DCA3:16 function transfers drive control commands from the accumulator to a register in the DCA-3. This register stores bus control codes or IPI-2 command information bytes. The DCA-3 controls the transfer of the register contents to the selected spindle(s) over bus A or over both bus A and bus B. Figure 14-12 shows the format of the command register values in the accumulator.
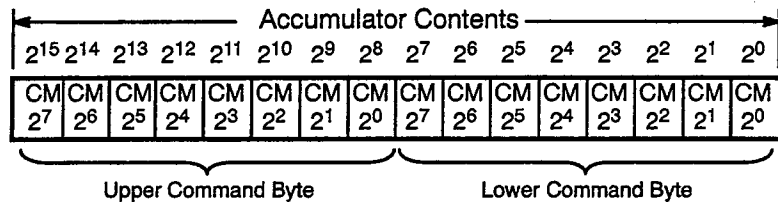
Figure 14-12. Control Register Values

Table 14-7 contains some of the IPI-2 control commands used by CRI.

Table 14-7. Sample Bus Control Commands Used by CRI

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Description
0	0	0	0	0	0	1	0	Load format specification
0	1	0	0	0	0	1	0	Read format specification
0	0	1	0	0	0	1	0	Spin up
0	0	1	0	0	0	0	1	Spin down
0	0	1	0	1	1	1	0	Disable master sync device
0	0	1	0	1	1	1	1	Enable master sync device
0	0	0	0	0	1	0	0	Load cylinder address (seek)
0	0	0	0	0	1	0	1	Load head address (head select)
0	0	0	0	0	1	1	0	Load rotational position sensing (RPS) target sector
0	0	0	0	0	1	1	1	Load position (cylinder, head, sector)
1	1	0	0	1	0	0	0	Read header
1	1	0	0	1	1	0	0	Read header at target
1	1	0	0	0	0	0	1	Read data field
1	0	0	0	0	0	0	1	Write data field
1	0	0	0	1	1	0	0	Write header at target (format)
0	1	0	0	0	1	0	0	Read status
0	1	0	0	1	0	0	0	Read extended status

DCA3:17 - Set Operating Mode

Modifier bit M0 determines which operation is performed by the DCA3:17 function. The following paragraphs explain the different operations.

Set Array Type with M0 = 0

This function uses the accumulator contents to provide the DCA-3 with the number of heads and logical sector size of the disk array type connected (DA-60 or DA-62). This function should be executed immediately following a DCA3:17 set array mode (M0=1) function to properly initialize the array. Figure 14-13 shows the accumulator format.

2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^9	2^8 2^7 2^6 2^5 2^4	2^3 2^2 2^1 2^0
32K 16K 8K 4K 2K 1K 512 Sector Size (32 bit halfwords)	Not Used	8 4 2 1 Number of Heads (per spindle head group)
040010_8 for DA-60 010002_8 for DA-62		

Figure 14-13. DCA3:17 Control Parcel (Even Channel)

Set Array Mode with M0 = 1

This function uses the accumulator contents to enable or disable individual spindles, enable or disable single-spindle mode, and enable or disable data reconstruction during reads. This command must precede all others to ensure proper initialization of the array. Valid spindle enables include selection of 1, 4, or 5 spindles. Two- or three-spindle modes are not supported. Figure 14-14 shows the accumulator format.

2^{15}	2^{14}	2^{13} 2^{12} 2^{11} 2^{10} 2^9 2^8 2^7 2^6 2^5	2^4	2^3	2^2	2^1	2^0
		Not Used (Clear to 0)	Spindle 4	Spindle 3	Spindle 2	Spindle 1	Spindle 0
		Set Single-spindle Mode		Spindle Enables			
Enable data reconstruction during reads (Can Be Set at All Times)							

Figure 14-14. DCA3:17 Control Parcel (Odd Channel)

SECTION 15
DCA-3 TO DISK ARRAY CABLING

15 DCA-3 TO DISK ARRAY CABLING
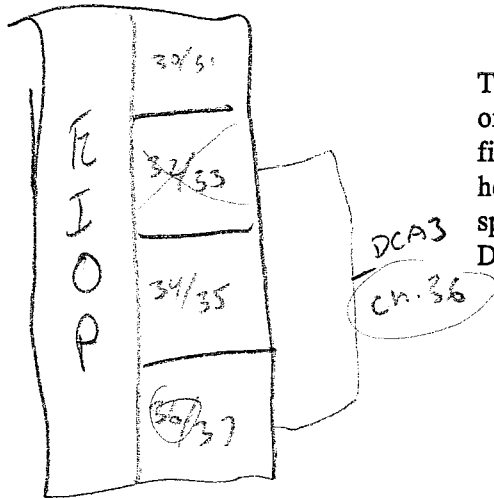
The DCA-3 channel adapter supports a five-spindle disk array composed of DD-60 or DD-62 spindles. Four of the spindles hold data while the fifth spindle contains parity information on the data. The spindles are housed in DE-60 disk enclosure cabinets; each cabinet contains up to ten spindles. As many as eight disk arrays can be daisy chained on a single DCA-3. Figure 15-1 is an overview of a two-array daisy chain.
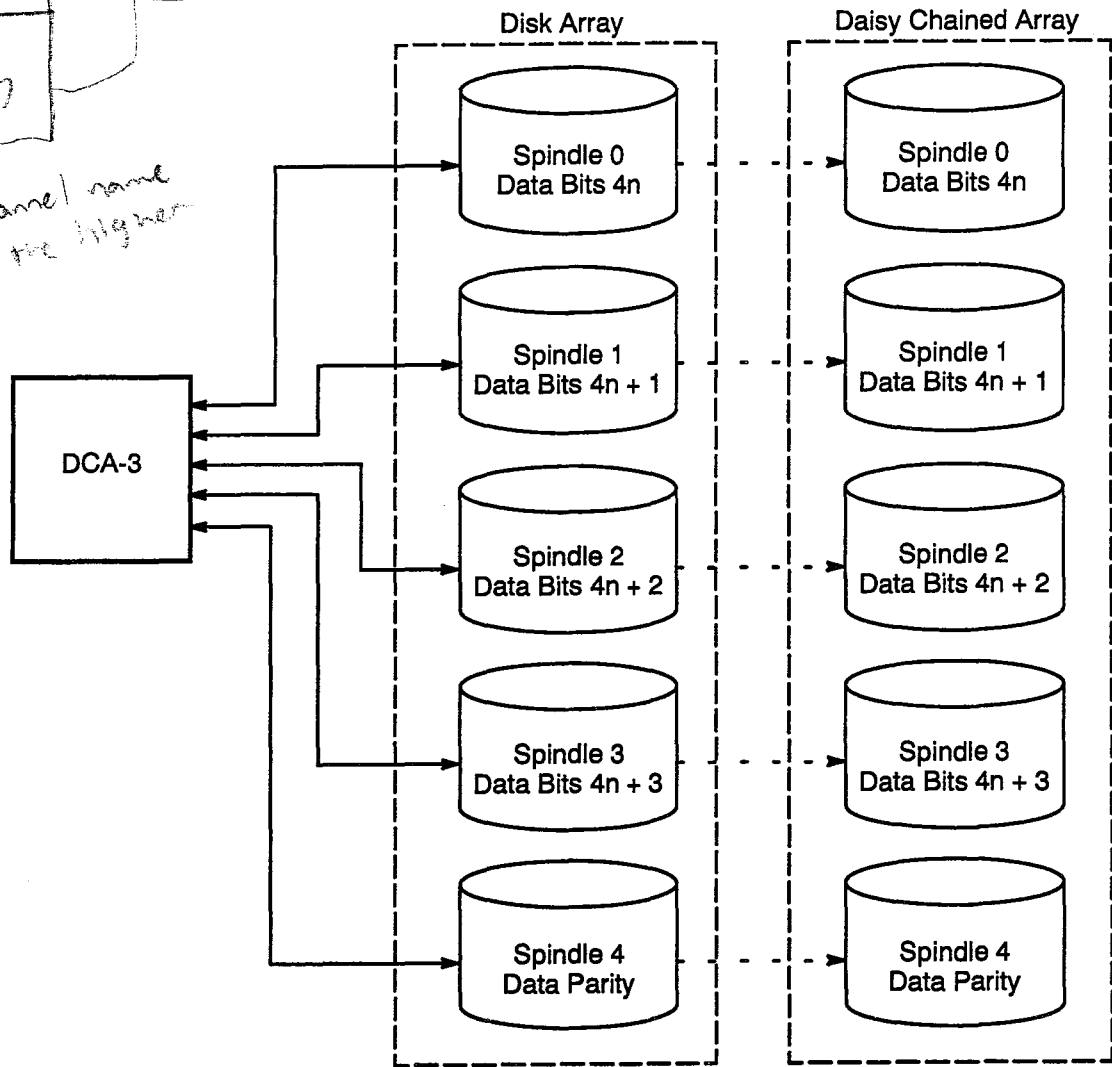
Figure 15-1. Disk Array Overview Block Diagram

Terminology

Because DCA-3 configuration options are numerous and complex, the terminology used to define the components must be accurate and consistent. The following list provides preferred terms and their definitions.

- Channel number – Refers to the logical address assigned to an I/O channel as determined by the location of the channel adapter in the mainframe chassis. The possible channel pairs for a DCA-3 are 34/35 or 36/37(octal).

- Device type – Refers to the type of peripheral device. Device types for a DCA-3 include a Disk Array 60 (DA-60) and a Disk Array 62 (DA-62).

- Unit number – Refers to the logical address of a peripheral device. Unit numbers for a DCA-3 range from 0 to 7, and represent the maximum number of disk arrays that can be daisy chained on a single channel.

- Disk array unit – Refers to a logical peripheral device. A logical device for a DCA-3 is defined as an array of 5 spindles that share a common unit address and are accessed as a single I/O device. Logical disk devices may also be referred to as drives.

- Spindle – Refers to a single disk component within an array or drive. A spindle usually consists of a head disk assembly (HDA), logic circuit boards, power supply, and the necessary containment hardware. Spindles for a DCA-3 include the DD-60 (for a DA-60) or DD-62 (for a DA-62).

Drive vs. Spindle

Use of the terms drive and spindle can be confusing. Whether a device should be referred to as a drive or a spindle is largely determined by the type of channel adapter to which the device is connected. If a DD-60 is connected to a DCA-2 channel adapter, it is an individually accessible I/O device and should be referred to as a drive. However, a DD-60 connected to a DCA-3 represents one-fifth of an array and should be referred to as a spindle.

Cabling Hardware

The cabling hardware requirements for the disk array are determined by the number of disk arrays involved and the configurations chosen. The following subsection describes these hardware components and the requirements for the various cabling options.

Cabling Hardware Components

The cabling hardware for a disk array is divided into 4 basic categories:

- DCA-3-to-spindle data cables (2 lengths)

- Spindle-to-spindle daisy chain data cables (2X)

- Spindle-to-spindle synchronization (sync) cables

- Cable terminators (data and sync cable versions)

Table 15-1 lists all cabling components and their associated CRI part numbers. For illustrations of these cables, refer to Figure 15-2, Figure 15-3, and Figure 15-4.

Table 15-1. Disk Array Cabling Components

Description	Length	CRI Part Number	Reference
DCA-3-to-spindle data cable (standard)	20 meters (66 ft)	12127800	Figure 15-2
DCA-3-to-spindle data cable (optional)	30 meters (99 ft)	12127801	Figure 15-2
2X spindle-to-spindle daisy chain data cable	1.8 meters (6 ft)	12247600	Figure 15-3
Spindle-to-spindle synchronization (sync) cable	4 meters (13.2 ft)	12182701	Figure 15-4
Terminator (data cable)	N/A	01686600	Figure 15-5
Terminator (sync cable)	N/A	01733700	Figure 15-6

DCA-3-to-spindle Data Cables

The DCA-3-to-spindle data cables are available in two lengths: 20 meters (66 ft) and 30 meters (99 ft). Five of these cables are required for each DCA-3 channel adapter: one for each of the four data spindles and one for the parity spindle. One end of the cable connects to the DCA-3 through the IOS-E bulkhead. The spindle end connects directly to the spindles in a single-unit configuration, or to a daisy chain cable if the channel supports more than one disk array. Refer to Figure 15-2 for an illustration of the DCA-3-to-spindle data cable.
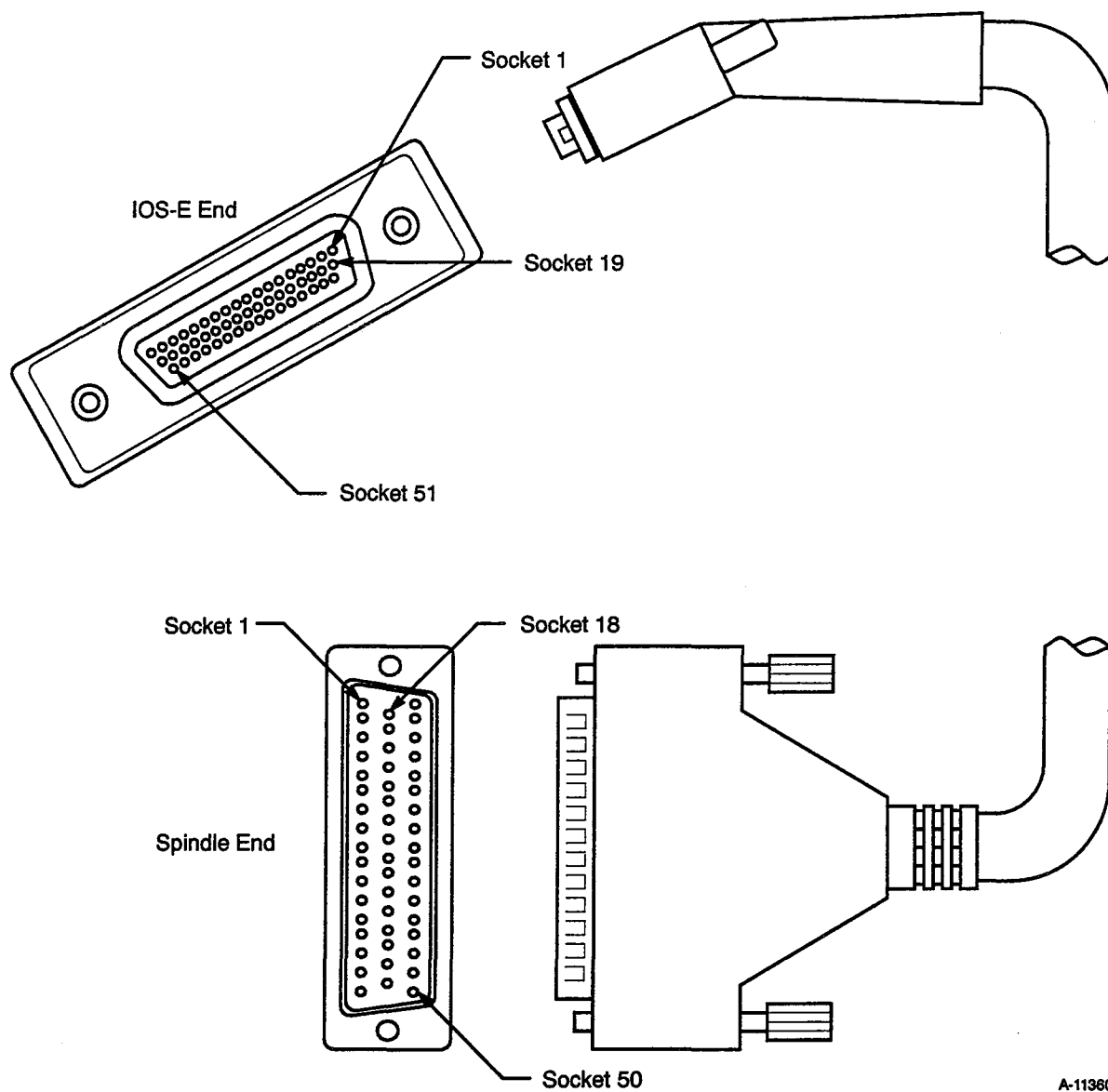
Figure 15-2. DCA-3-to-spindle Data Cable

Table 15-2 defines the pin-out assignments for the wires contained within the DCA-3-to-spindle data cables.

Table 15-2. DCA-3-to-spindle Data Cable Socket Definitions

Pair No.	Signal Name	IOS-E Connector Socket Number		Disk Drive Connector Socket Number	
		(+)	(−)	(+)	(−)
1	DC Ground	2	1	1	34
2	Select Out	14	13	43	27
3	Master Out	12	11	45	29
4	Sync Out	6	5	41	25
5	Sync In	10	9	15	48
6	Slave In	8	7	39	23
7	Attention In	4	3	20	4
8	Bus A − Bit 2^0	34	33	13	46
9	Bus A − Bit 2^1	37	36	30	14
10	Bus A − Bit 2^2	39	38	22	6
11	Bus A − Bit 2^3	41	40	26	10
12	Bus A − Bit 2^4	43	42	11	44
13	Bus A − Bit 2^5	45	44	28	12
14	Bus A − Bit 2^6	47	46	37	21
15	Bus A − Bit 2^7	49	48	5	38
16	Bus A − Parity Bit	51	50	47	31
17	Bus B − Bit 2^0	16	15	32	16
18	Bus B − Bit 2^1	18	17	49	33
19	Bus B − Bit 2^2	20	19	3	36
20	Bus B − Bit 2^3	22	21	7	40
21	Bus B − Bit 2^4	24	23	24	8
22	Bus B − Bit 2^5	26	25	9	42
23	Bus B − Bit 2^6	28	27	18	2
24	Bus B − Bit 2^7	30	29	35	19
25	Bus B − Parity Bit	32	31	17	50

2X Daisy Chain Cable

The 2X daisy chain cable interconnects spindles in a daisy chained configuration. Connector P1 attaches to the DCA-3-to-spindle data cable; connectors P2 and P3 attach to the input port of the spindles.

A terminator must be installed on connector P4 if it is not attached to a second daisy chain cable. (Refer to Figure 15-3 for an illustration of the 2X daisy chain cable.) Proper use of the 2X daisy chain cable permits a single spindle to be removed from a daisy chain without affecting the connections to the remaining spindles in the chain.
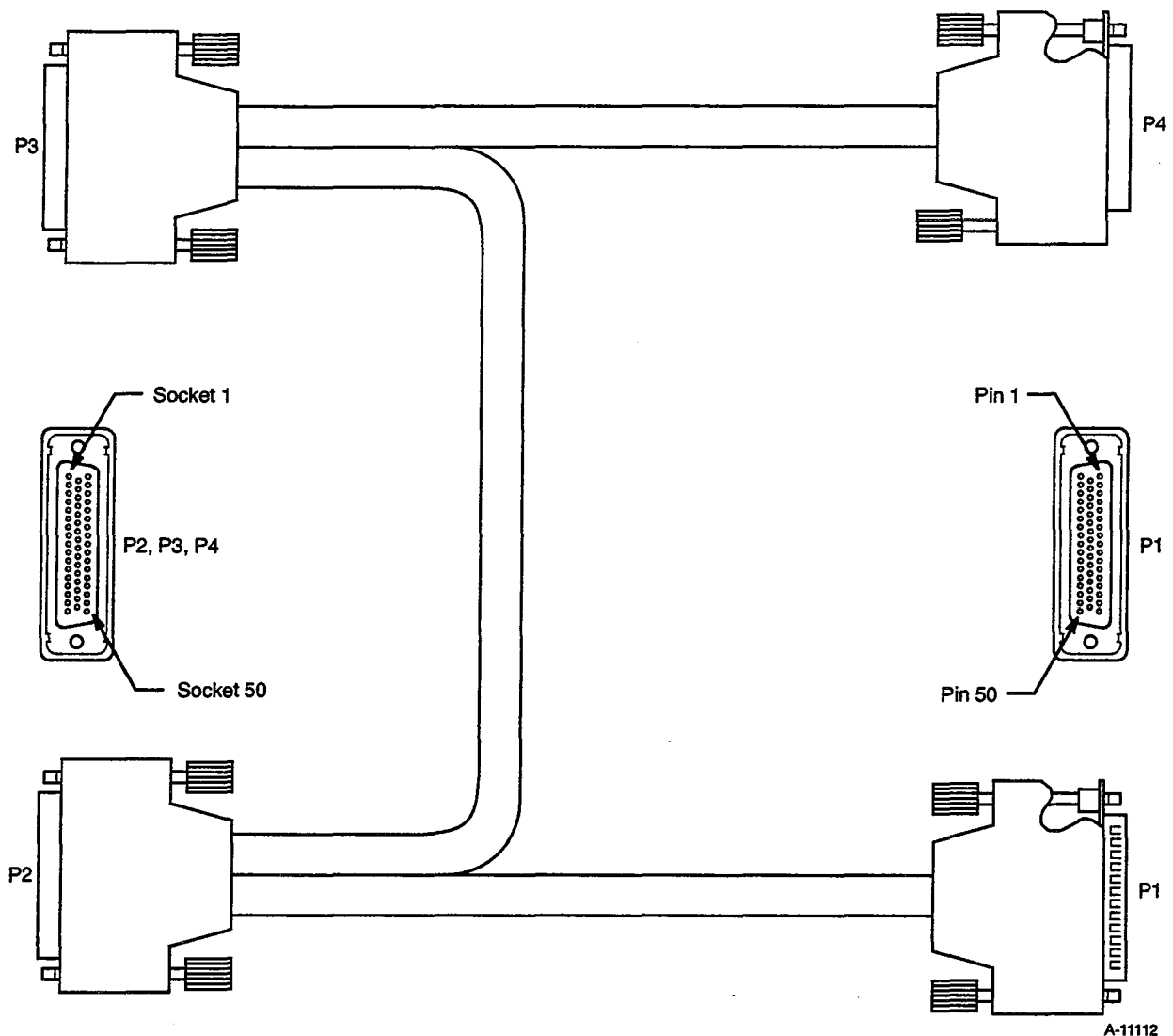
Figure 15-3. 2X Daisy Chain Cable

Table 15-3 defines the pin-out assignments for the wires contained within the 2X daisy chain cables.

Table 15-3. 2X Daisy Chain Cable Pin and Socket Definitions

Pair No.	Signal Name	Disk Drive Connector Pin Number		Disk Drive Connector Socket Number	
		(+)	(−)	(+)	(−)
1	DC Ground	1	34	1	34
2	Select Out	43	27	43	27
3	Master Out	45	29	45	29
4	Sync Out	41	25	41	25
5	Sync In	15	48	15	48
6	Slave In	39	23	39	23
7	Attention In	20	4	20	4
8	Bus A − Bit 2^0	13	46	13	46
9	Bus A − Bit 2^1	30	14	30	14
10	Bus A − Bit 2^2	22	6	22	6
11	Bus A − Bit 2^3	26	10	26	10
12	Bus A − Bit 2^4	11	44	11	44
13	Bus A − Bit 2^5	28	12	28	12
14	Bus A − Bit 2^6	37	21	37	21
15	Bus A − Bit 2^7	5	38	5	38
16	Bus A − Parity Bit	47	31	47	31
17	Bus B − Bit 2^0	32	16	32	16
18	Bus B − Bit 2^1	49	33	49	33
19	Bus B − Bit 2^2	3	36	3	36
20	Bus B − Bit 2^3	7	40	7	40
21	Bus B − Bit 2^4	24	8	24	8
22	Bus B − Bit 2^5	9	42	9	42
23	Bus B − Bit 2^6	18	2	18	2
24	Bus B − Bit 2^7	35	19	35	19
25	Bus B − Parity Bit	17	50	17	50

Spindle-to-spindle Synchronization Cable

The spindle-to-spindle sync cables are connected among the five spindles within an array to accommodate rotational synchronization. A separate sync cable is required for each spindle in a disk array. Connector P1 attaches to the rear of each spindle. Connectors P2 and P3 attach to sync cables on other spindles in the array or are terminated. Refer to Figure 15-4 for an illustration of the sync cable.

NOTE: Synchronization signal is carried on pins 1 and 6. All other pins are unused.

4 Meters (13.2 Feet)
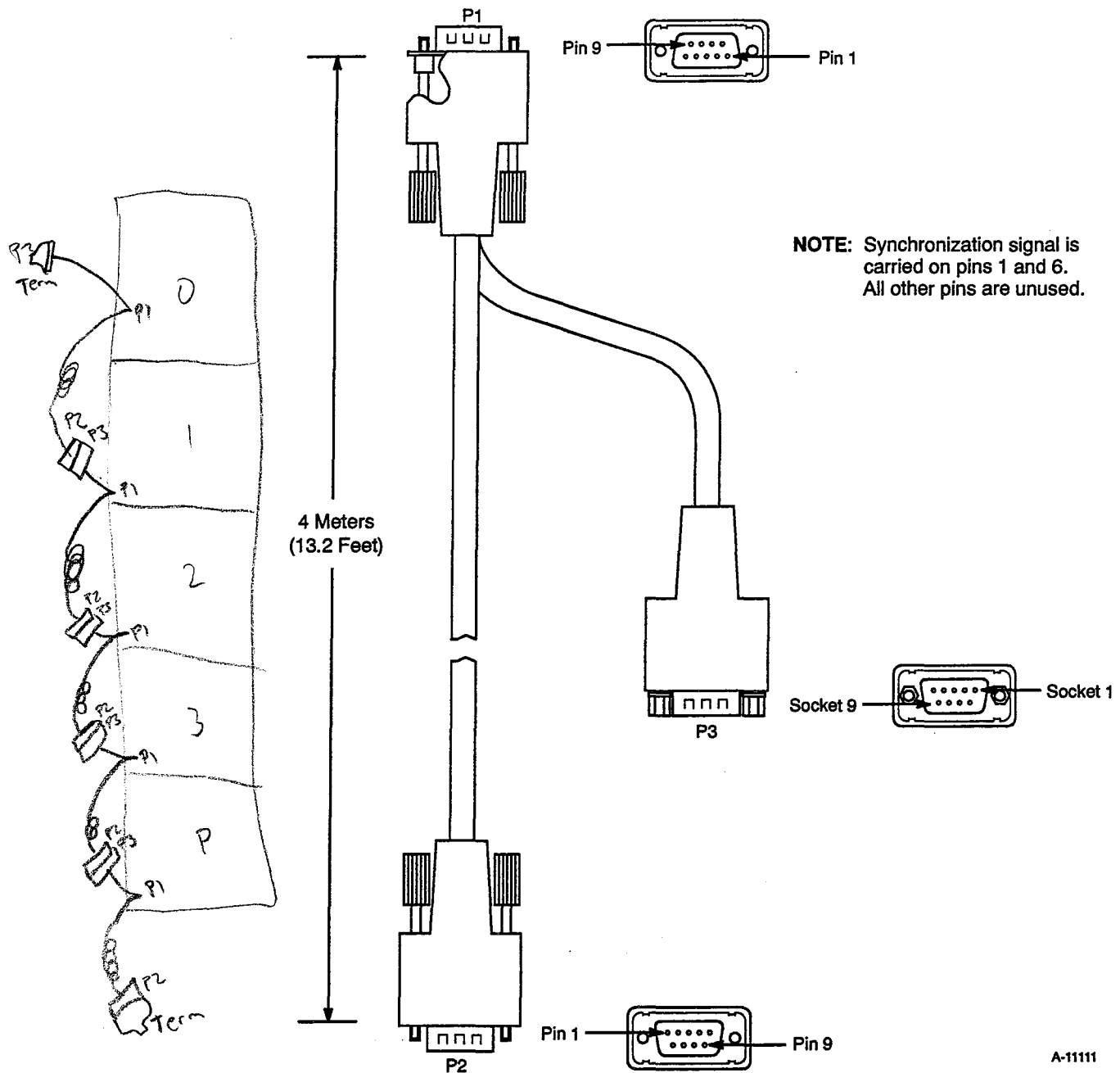
Figure 15-4. Synchronization (Sync) Cable

Data Cable Terminator

The data cable terminator for 60 series disk arrays must be used to terminate signals at the end of a daisy chain cable, or on the rear of the spindle (if daisy chain cables are not used). The CRI part number for the terminator is 01686600. Figure 15-5 shows the data cable terminator.
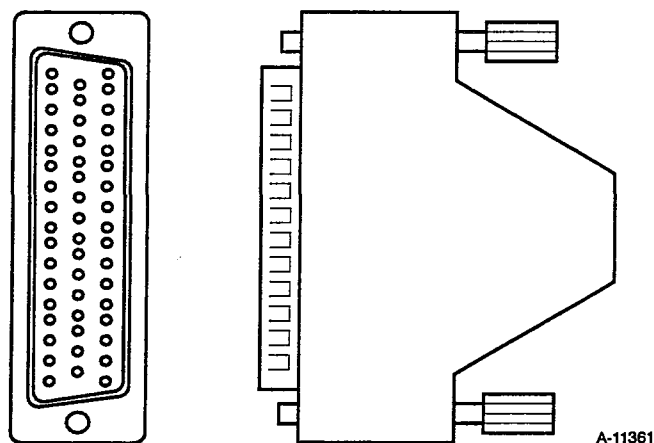
Figure 15-5. Data Cable Terminator for 60 Series Disk Arrays

Synchronization (Sync) Cable Terminator

The synchronization cable terminator must be used to terminate the sync pulse at both ends of the synchronization chain. A separate sync cable is connected to each of the five spindles in an array. The sync cables attached to spindles 1, 2, and 3 connect to the sync cable on the adjacent spindles. Spindles 0 and 4 must have terminators attached to the unused ends. Figure 15-6 shows the synchronization cable terminator.
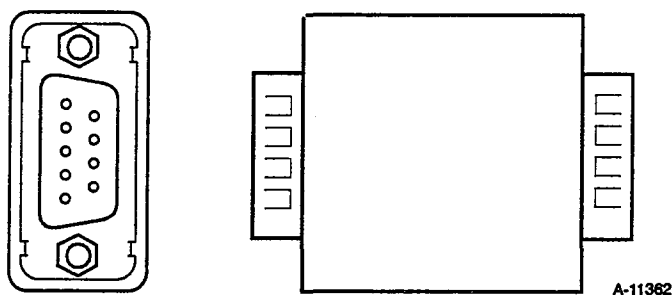
Figure 15-6. Sync Cable Terminator for 60 Series Disk Arrays

IOS-E Bulkhead Connections

Standard bulkhead arrangements on an IOS-E allow for two connections per quarter board position. Because the DCA-3 is a half board channel adapter, it uses each pair of connections normally assigned to the two quarter board positions it occupies. For example, a DCA-3 installed as logical channel pair 34/35 uses the two bulkhead connections for those channels as well as the two connections for channel pair 30/31. A DCA-3 installed as logical channel pair 36/37 also uses the bulkhead connections for channel pair 32/33.

The half board design of the DCA-3 provides four bulkhead connections (one for each of the data spindles), but a fifth connection is needed for the parity spindle. Special wiring in the backplane of the IOS-E accommodates this fifth bulkhead connection. Field change orders (FCOs) and Engineering change orders (ECOs) exist to provide this special wiring. This manual assumes that the necessary wiring has been installed in the IOS-E.

In all DCA-3 applications, the four data spindle cables are connected to one side of the IOS-E/mainframe chassis; the parity spindle cable is connected to the opposite side. Bundling the cables should enable the parity spindle cable to reach the opposite side of the chassis.

The exact layout of an IOS-E bulkhead depends on the chassis type and serial number of a particular machine. The 700, 1600, 1700, 1900, and 2600 series products all represent slight differences in bulkhead design. In addition, differences can exist between machines of different serial numbers within a product group. Not all possible bulkhead layouts are represented in this manual. Table 15-4 lists the DCA-3 bulkhead assignments for cluster 0 of a 700 series IOS-E. Figure 15-7 shows the position of these connections on the bulkhead.

Table 15-4. DCA-3 Bulkhead Connections for 700 Series Chassis (Cluster 0)

Physical Position	Logical I/O Path	Data Spindle (0,1,2,3) Connections	Parity Spindle Connection
CA0 / CA2	00034	ZB 00, 01, 02, 03 (A)†	YB 20 (A)†
CA1 / CA3	00036	YB 00, 01, 02, 03 (B)†	ZB 20 (B)†
CA4 / CA6	00134	YB 04, 05, 06, 07 (C)†	ZB 22 (C)†
CA5 / CA7	00136	ZB 04, 05, 06, 07 (D)†	YB 22 (D)†
CA10 / CA12	00234	ZB 40, 41, 42, 43 (E)†	YB 24 (E)†
CA11 / CA13	00236	YB 40, 41, 42, 43 (F)†	ZB 24 (F)†
CA14 / CA16	00334	YB 44, 45, 46, 47 (G)†	ZB 26 (G)†
CA15 / CA17	00336	ZB 44, 45, 46, 47 (H)†	YB 26 (H)†

† Denotes position indicator used in Figure 15-7

YB Panel (Cluster 0)

Channel 32 CA1 Channel 33	B 00 01 B EIOP 0 / A 20 21 / F 40 41 F EIOP 2

Channel 32
CA11
Channel 33

Channel 36
CA3
Channel 37

Channel 30
CA4
Channel 31

Channel 34
CA6
Channel 35

ZB Panel (Cluster 0)

Channel 30
CA0
Channel 31

Channel 34
CA2
Channel 35

Channel 32
CA5
Channel 33

Channel 36
CA7
Channel 37

A-11363
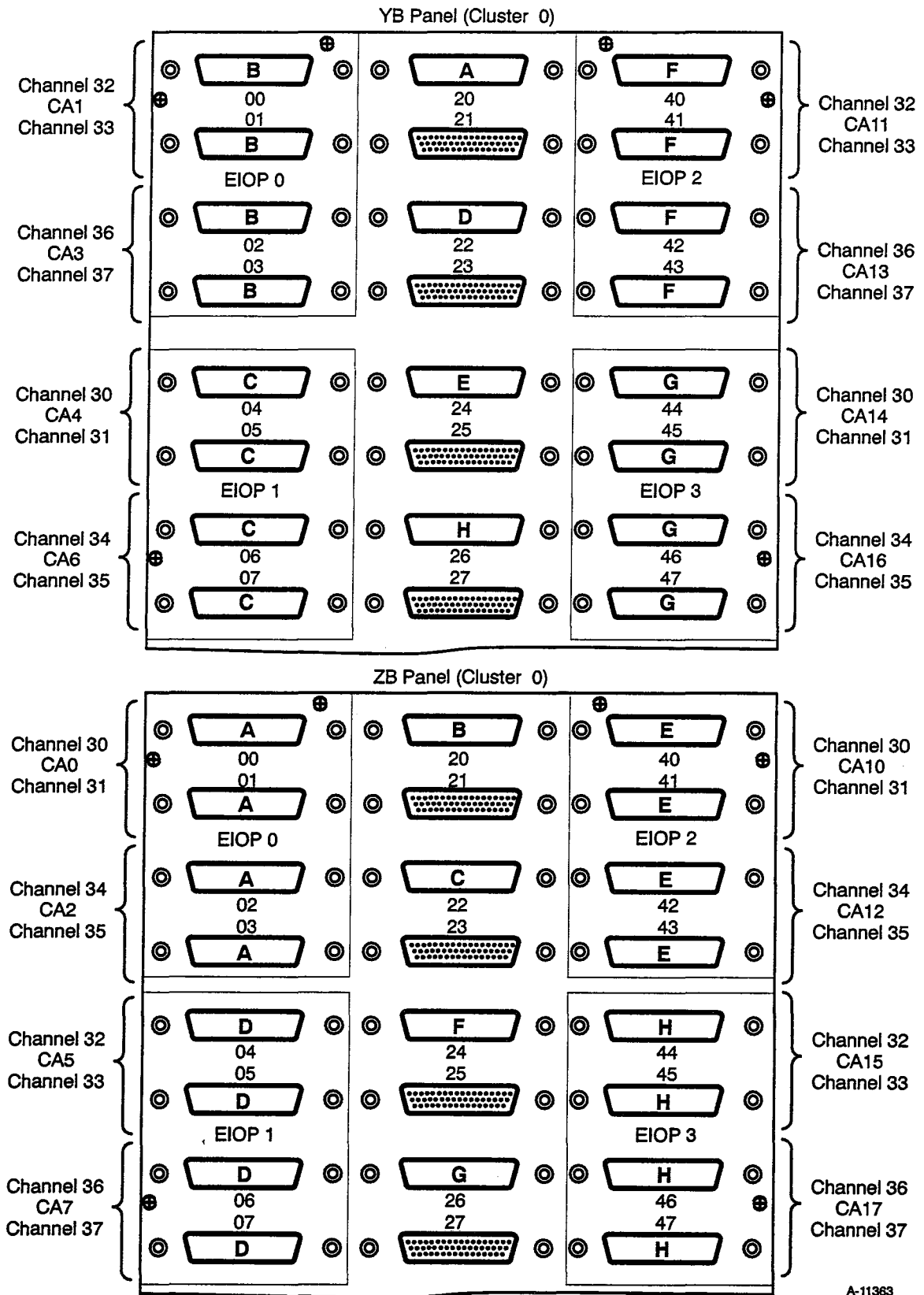
Figure 15-7. DCA-3 Bulkhead Connections for 700 Series IOS-E

Cabling Restrictions

The following cabling restrictions must be followed when connecting cables to the disk array. These include the following:

- Data cables **cannot** be daisy chained between cabinets.

- Data cable terminators must be connected to the **last** connector on a daisy chain cable.

- Synchronization cable terminators must be connected to **both** ends of a sync cable.

Cabling Hardware Requirements

Table 15-5 lists the minimum hardware requirements for various cabling configurations. Note that the number of DE-60 cabinets required cannot be determined from the number of spindles alone; you must also consider how the spindles will be configured.

The minimum numbers provided in Table 15-5 are for connection to a single DCA-3. Alternate-path connections can be accommodated by doubling the number of 2X daisy chain cables listed.

Table 15-5. Disk Array Cabling Hardware Requirements

Configuration	Number of Spindles	Number of DE-60 Cabinets	Number of I/O Cables	Number of 2X Daisy Chain Cables	Number of Data Cable Terminators	Number of Sync Cables	Number of Sync Cable Terminators
Single Array	5	1	5	0	5	5	2
2-array daisy chain	10	1	5	5	5	10	4
3-array daisy chain	15	2	5	10	5	15	6
4-array daisy chain	20	3	5	10	5	20	8
5-array daisy chain	25	3	5	15	5	25	10
6-array daisy chain	30	5	5	15	5	30	12
7-array daisy chain	35	5	5	20	5	35	14
8-array daisy chain	40	5	5	20	5	40	16

Configuration Options

Refer to the following subsections for information about DCA-3 configuration options.

Single-channel to Single-unit Configuration

In a single-channel, single-unit access configuration, each DCA-3 is connected to a single disk array, and each disk array is only accessible through a single DCA-3 channel. Because each DCA-3 is connected to a single array, maximum transfer rates with no conflicts on the channel are possible; however, the single-channel connection to the array means that a failure of the DCA-3 makes the array inaccessible until the hardware problem is corrected.

Single-channel to Daisy Chain Configuration

In this configuration each DCA-3 can be connected to a maximum of eight disk arrays. The advantage of daisy chaining is a cost-effective increase in total storage capacity. The disadvantage is the potential increase in conflicts with each array added to a channel, although effective file system configurations can help to minimize this problem. Again, because each array in the daisy chain is connected to a single DCA-3, a failure of the DCA-3 makes all units on the chain inaccessible.

Alternate-path to Daisy Chain Configuration

In this configuration each array is connected to a primary DCA-3 channel (through port A on each spindle) and an alternate DCA-3 channel (through port B on each spindle), essentially creating a dual-ported daisy chain. Although the alternate path is normally inactive, it provides a secondary access route if the primary path is inaccessible, thus increasing the overall resiliency of the disk system.

Resiliency increases if the primary and secondary DCA-3s reside in separate EIOPs and/or I/O clusters. The primary and alternate paths have an exclusive OR relationship; if the alternate path is activated the primary path must be deactivated.

Disk Enclosure Resilient Configuration

In the disk enclosure resilient configuration, each of the five spindles within an array is installed in a separate DE-60 cabinet; thus, a minimum of five DE-60 cabinets is required. Because a single cabinet contains only one spindle from each of the arrays, if the cabinet fails, all of the affected arrays remain operational through a four-spindle parity-reconstruction mode.

Single-channel to Single-array Configuration

In a single-channel to single array-configuration, each DCA-3 channel adapter is connected to a single array. The logical address setting for each spindle within each array is the same. Individual cables are connected to each of the four data spindles (0-3) and the parity spindle (P). For rotational synchronization, separate sync cables must interconnect the 5 spindles within each array.

Refer to Figure 15-8 for an illustration of single-array cabling. Figure 15-9 is an illustration of the cable connections for spindles 0/P (parity spindle) and 0/3 (data 3 spindle).
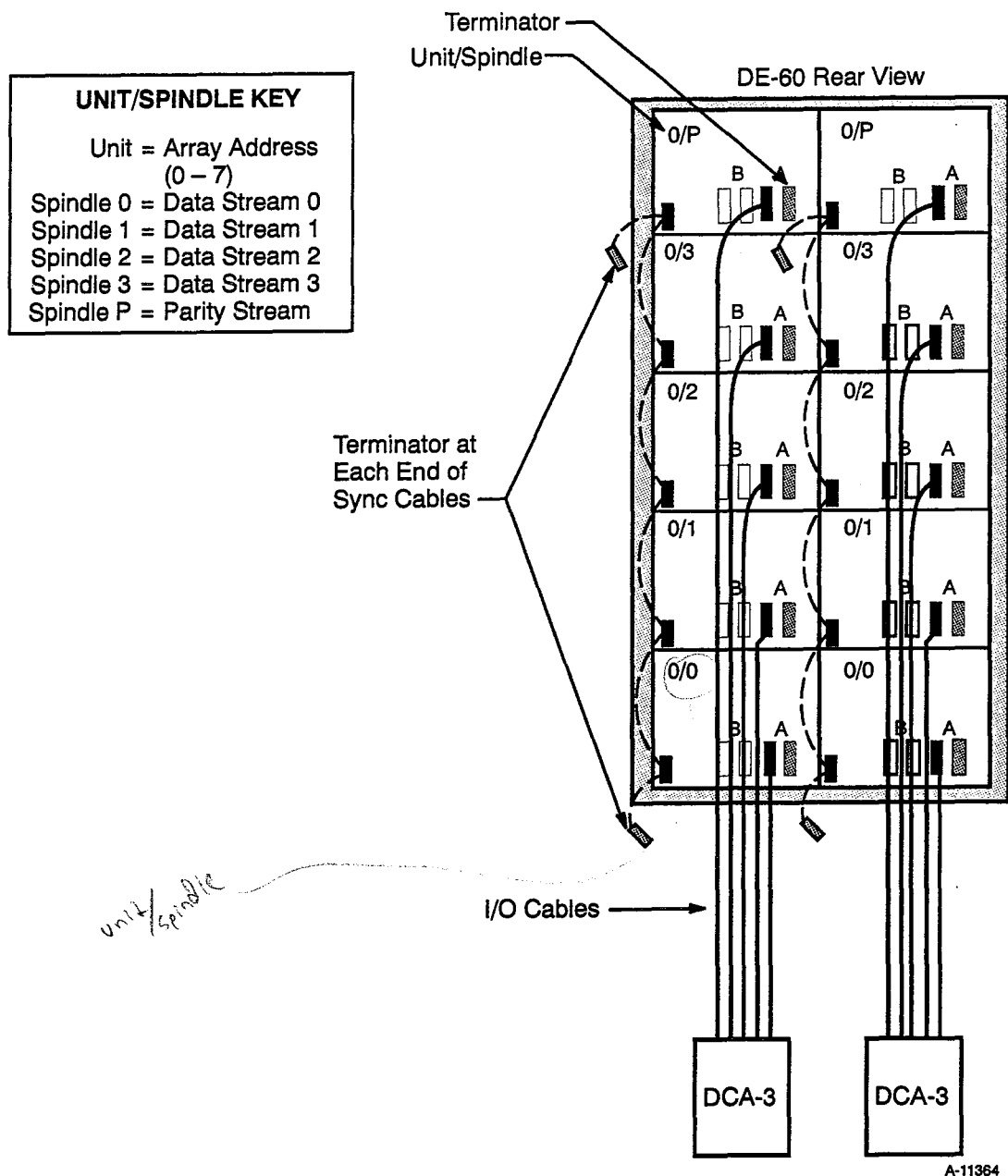
Figure 15-8. Single-array Cabling (2 Channels Shown)

Parity
Spindle

Sync Cable Terminator
Attached to Unused End

Port A

Parity Cable
from DCA-3

Inter-spindle Sync
Cable Connection

Data 3
Spindle

Port A

Data Cable 3
from DCA-3

Inter-spindle Sync
Cable Connection

A-11234
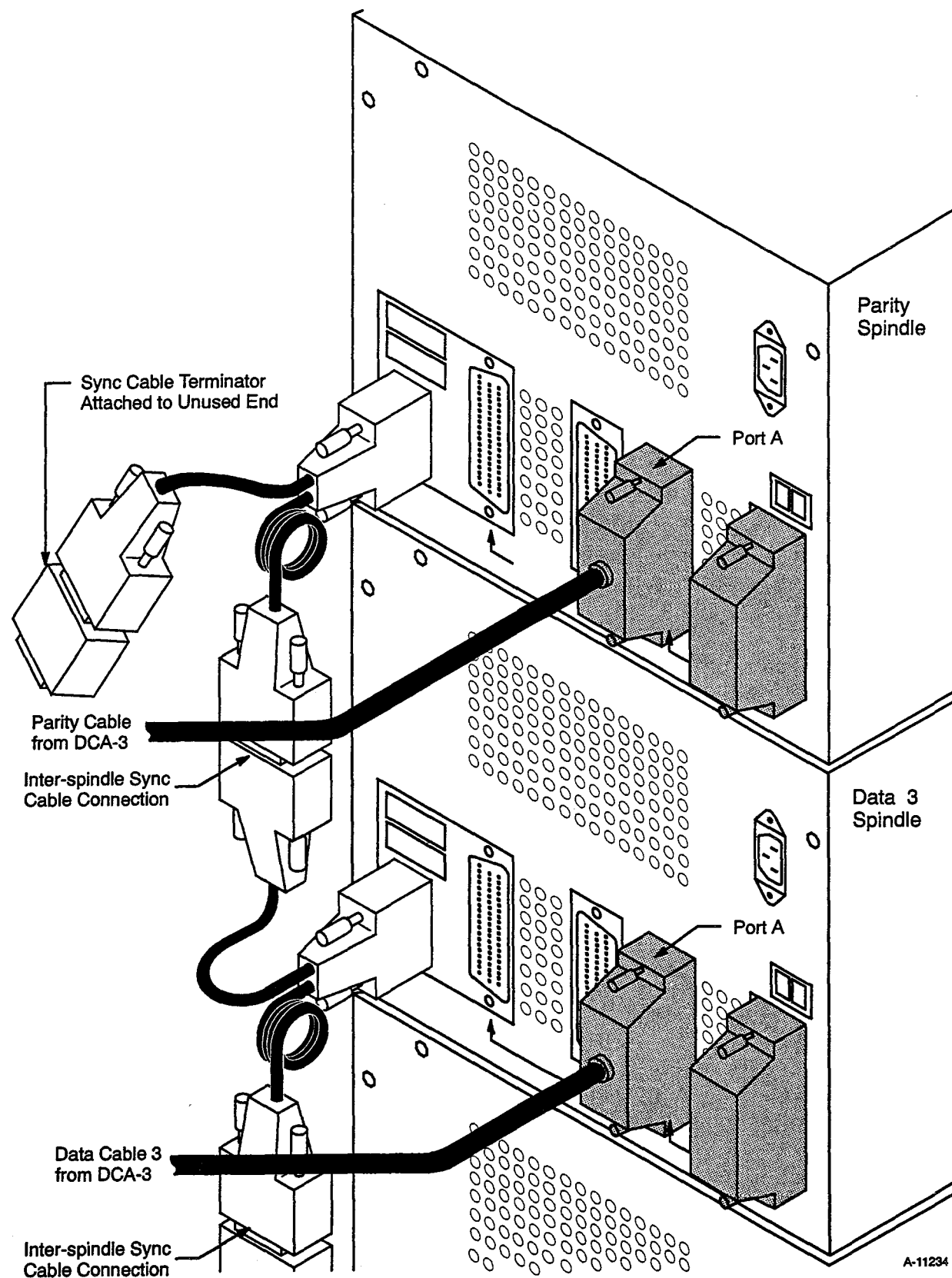
Figure 15-9. Single-array Cable Connections

Figure 15-10 shows the spindle positions for a single array in a partially loaded DE-60 cabinet. Placing the spindles in the positions shown ensures a low center of gravity for the cabinet. If a new array were added to the cabinet, spindles 0/2, 0/3, and 0/P could be relocated above spindles 0/0 and 0/1 in the left-hand column, allowing the new array to be placed in the right-hand column. If each of the two arrays were connected to separate channel adapters, cabling for each column would resemble Figure 15-8.
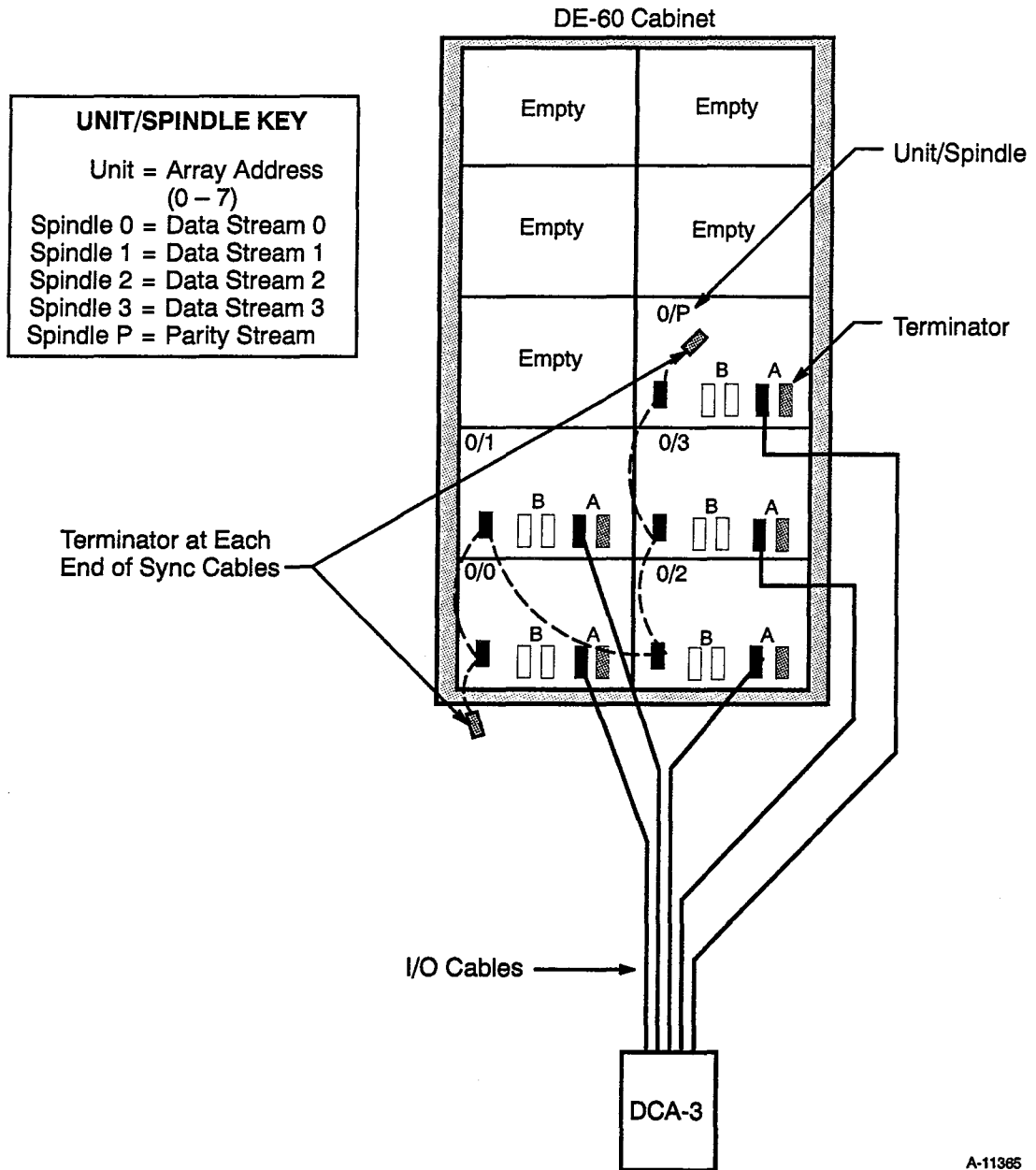
A-11365

Figure 15-10. Single-array Cabling (Partially Populated Cabinet)

Daisy Chained Configurations

The following subsection describes the hardware and interconnects used for daisy chained configurations. Daisy chaining disk arrays presents unique cabling requirements that vary with the hardware limitations and the desired resiliency of the disk subsystem.

Two-array Daisy Chain Configuration

In a two-array, daisy chained configuration, the DCA-3 channel adapter is cabled to the first array. Each disk within the first array is then daisy chained to its counterpart in the second array. The logical address setting on each spindle within each array is the same; however, each array uses a unique address. In many situations, the spindles in the first array are set to logical address 0. The spindles in the second array are set to logical address 1 (refer to Figure 15-11).
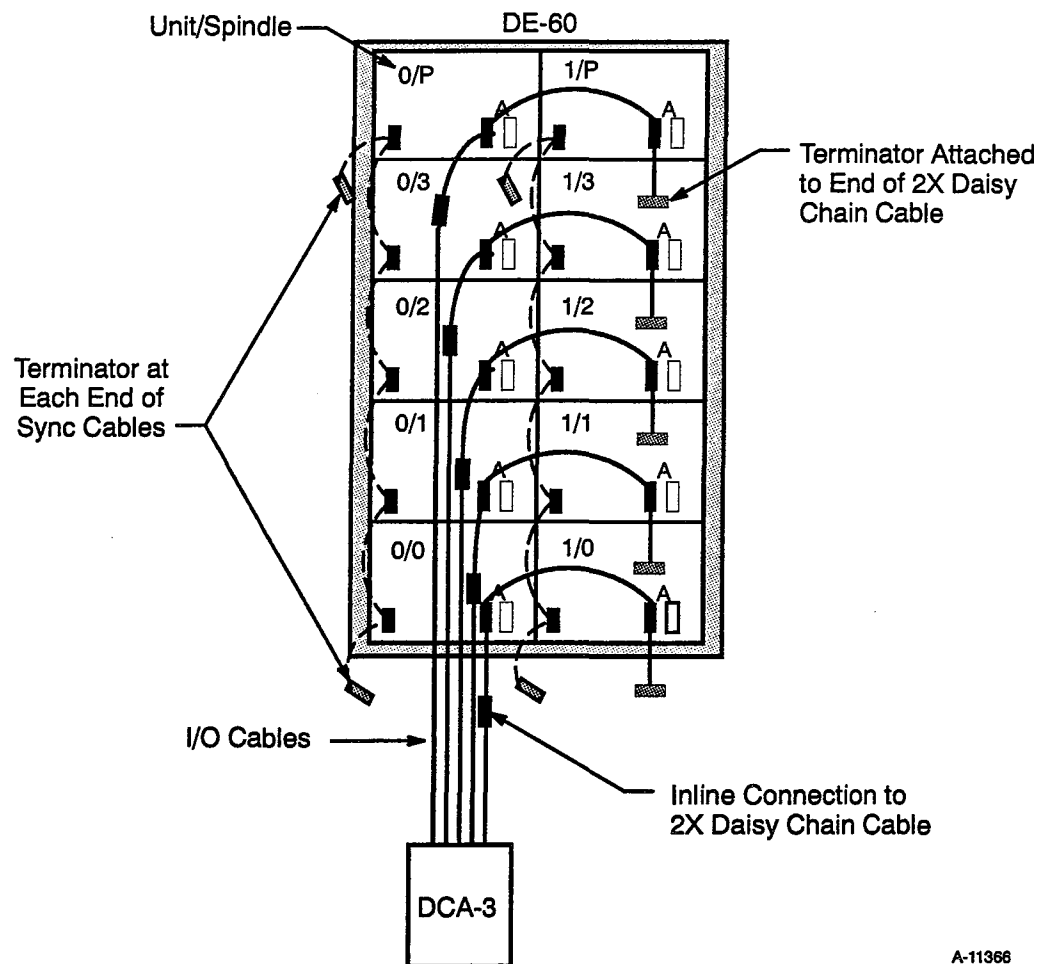
Figure 15-11. Single-channel, Two-array Daisy Chain

Three-array Daisy Chain Configuration

On a channel to which three disk arrays are daisy chained, spindles 0 and 1 of each array are located in cabinet 1, and spindles 2, 3, and P (parity) are located in cabinet 2 (refer to Figure 15-12.) This cabling method allows each data stream to be daisy chained within a single cabinet, ensuring that functional cable lengths do not exceed the specified maximum. The synchronization cables, however, must be run between cabinets to interconnect all 5 spindles within each array. In summary, the sync cables can be run between cabinets, but the data cables cannot.
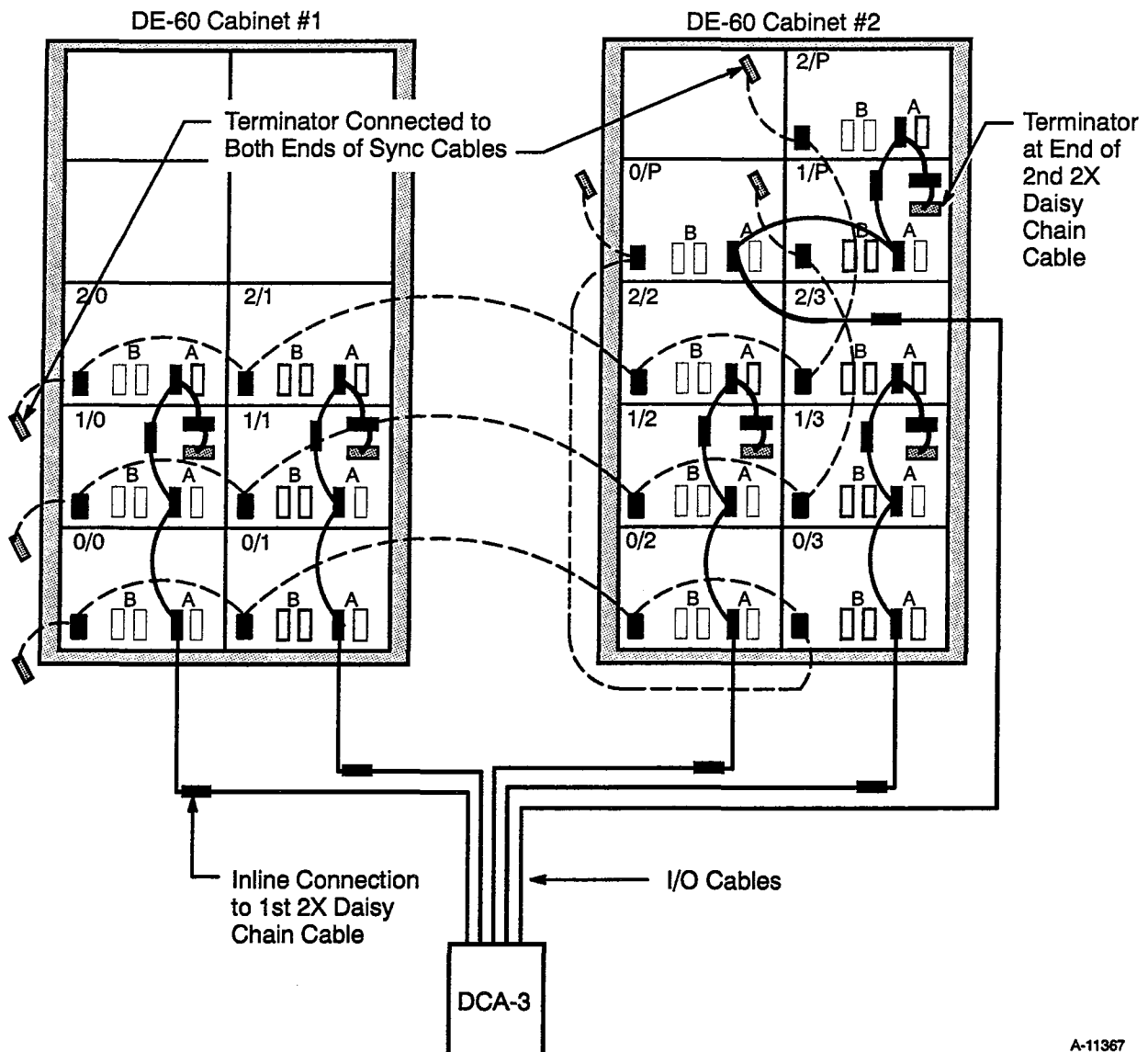
Figure 15-12. Single-channel, Three-array Daisy Chain Configuration

Four-array Daisy Chain Configuration

On a channel to which four disk arrays are daisy chained, spindles 0 and 1 are located in cabinet 1, spindles 2 and 3 are located in cabinet 2, and the parity spindles are located in cabinet 3. Unless additional spindles are housed in cabinet 3, the parity spindles should be located in the bottom of cabinet 3 to maintain a low center of gravity (refer to Figure 15-13).

Although the 20 spindles required for four arrays can be accommodated by two DE-60 cabinets, this arrangement would require running data cables between the cabinets, which is not allowed. Only synchronization cables can connect cabinets.
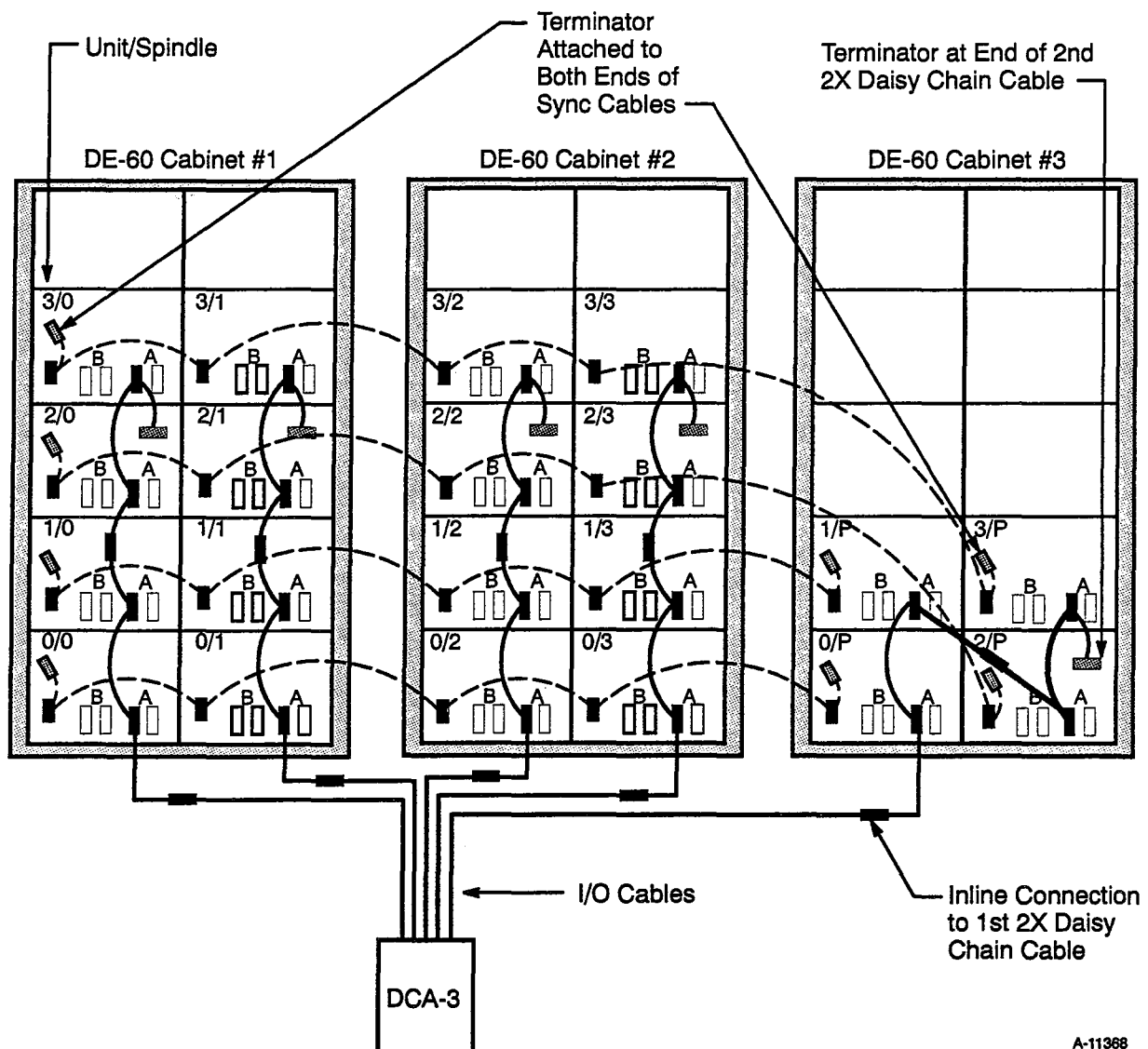
Figure 15-13. Single-channel, Four-array Daisy Chain Configuration

Five-array Daisy Chain Configuration

On a channel to which five disk arrays are daisy chained, data spindles 0 and 1 are located in cabinet 1, data spindles 2 and 3 are located in cabinet 2, and the parity spindles are located in cabinet 3 (refer to Figure 15-14).

Unless additional spindles are housed in cabinet 3, the parity spindles should be located in the bottom of cabinet 3 to maintain a low center of gravity. The spindle positions in the bottom of cabinet 3 should be used whenever a cabinet is half populated.
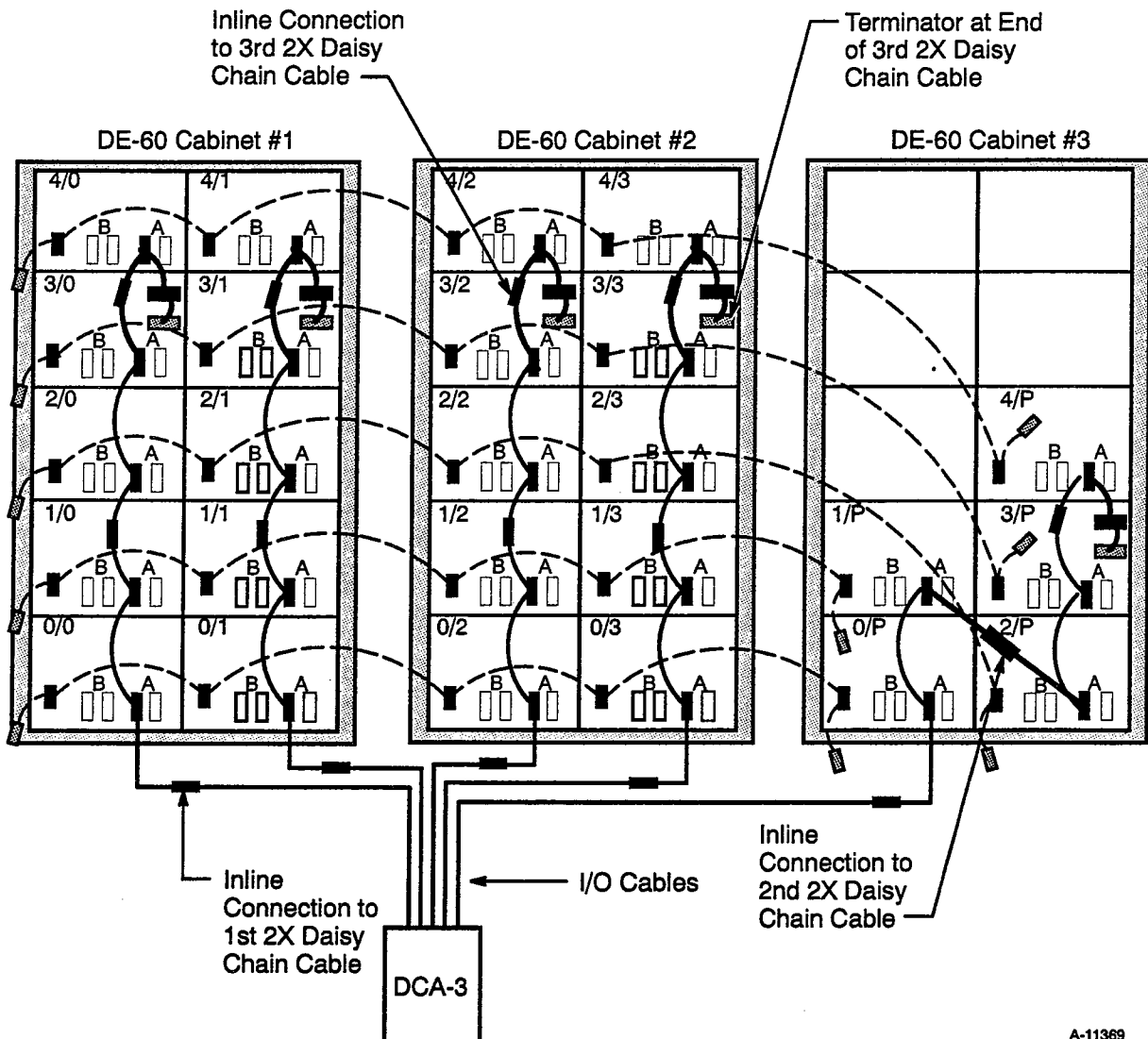
Figure 15-14. Single-channel, Five-array Daisy Chain Configuration

Six-array Daisy Chain Configuration

On a channel to which six or more disk arrays are daisy chained, a minimum of five DE-60 cabinets is required. DE-60 cabinet 1 contains the spindles from each array for stream 0 data, cabinet 2 contains the spindles for stream 1 data, and so on; cabinet 5 holds all of the parity spindles. Figure 15-15 shows a daisy chain of six arrays, which are addressed as units 0 through 5.

In this configuration, each array unit is positioned horizontally across the five cabinets, and the daisy chains are positioned vertically within each cabinet. Although the data cables are daisy chained within each cabinet, the sync cables for each array are interconnected among all five cabinets.

Seven- or Eight-array Daisy Chain Configuration

A daisy chain configuration of seven or eight arrays is similar to the spindle positioning used for six arrays. In these cases, the additional spindles (for units 6 and 7) are placed above the existing spindles shown for each cabinet in Figure 15-15.

Alternate Path and Disk Enclosure Resiliency

Careful attention should be given to the overall resiliency of any disk configuration. Sometimes the configuration possibilities can be limited by the available hardware. Device types, total number of devices, total number of cabinets, and number of channel adapters all affect the configuration options. Documenting all options for every possible hardware configuration is beyond the scope of this manual. Examples are given to demonstrate the basic strategies for achieving resiliency so that the reader can apply these principles to whatever hardware is available.

Minimum Resiliency

In this example, a customer purchases four DCA-3 channel adapters and wants to daisy chain two arrays onto each of the four channels. Because each DE-60 cabinet can accommodate 10 spindles, the customer could accommodate all 40 spindles in four DE-60 cabinets. If only four DE-60 cabinets are used, the cabling scheme for the available hardware is shown in Figure 15-16.

Note that this configuration offers no alternate-path access and no disk enclosure resiliency. If any of the DCA-3 channel adapters is inoperative, the two arrays on that channel are inaccessible until the

channel hardware is repaired or replaced. If power is lost to any of the four DE-60 cabinets, the two arrays housed in that cabinet are inoperative until power is restored to the affected cabinet.

Enhanced Resiliency

For the price of one more DE-60 cabinet and some additional cables, the customer can configure the same disk subsystem for enhanced resiliency. The cable connections and cabinet layout for this resilient configuration are shown in Figure 15-17.

Note that each DCA-3 is connected to a daisy chain of four spindles. Each channel (DCA-3) provides a primary path (Port A) connection to two of the spindles and an alternate path (Port B) connection to the other two spindles. If any of the DCA-3 channel adapters is inoperative, the two primary arrays on that channel are accessible from an alternate-path connection to another DCA-3.

Note that each DE-60 cabinet contains only one spindle from each of the eight array units. If power is lost to any of the four DE-60 cabinets, all eight arrays can still operate in a four-spindle, parity-reconstruction mode. This configuration results in no down time and no data loss to the customer.
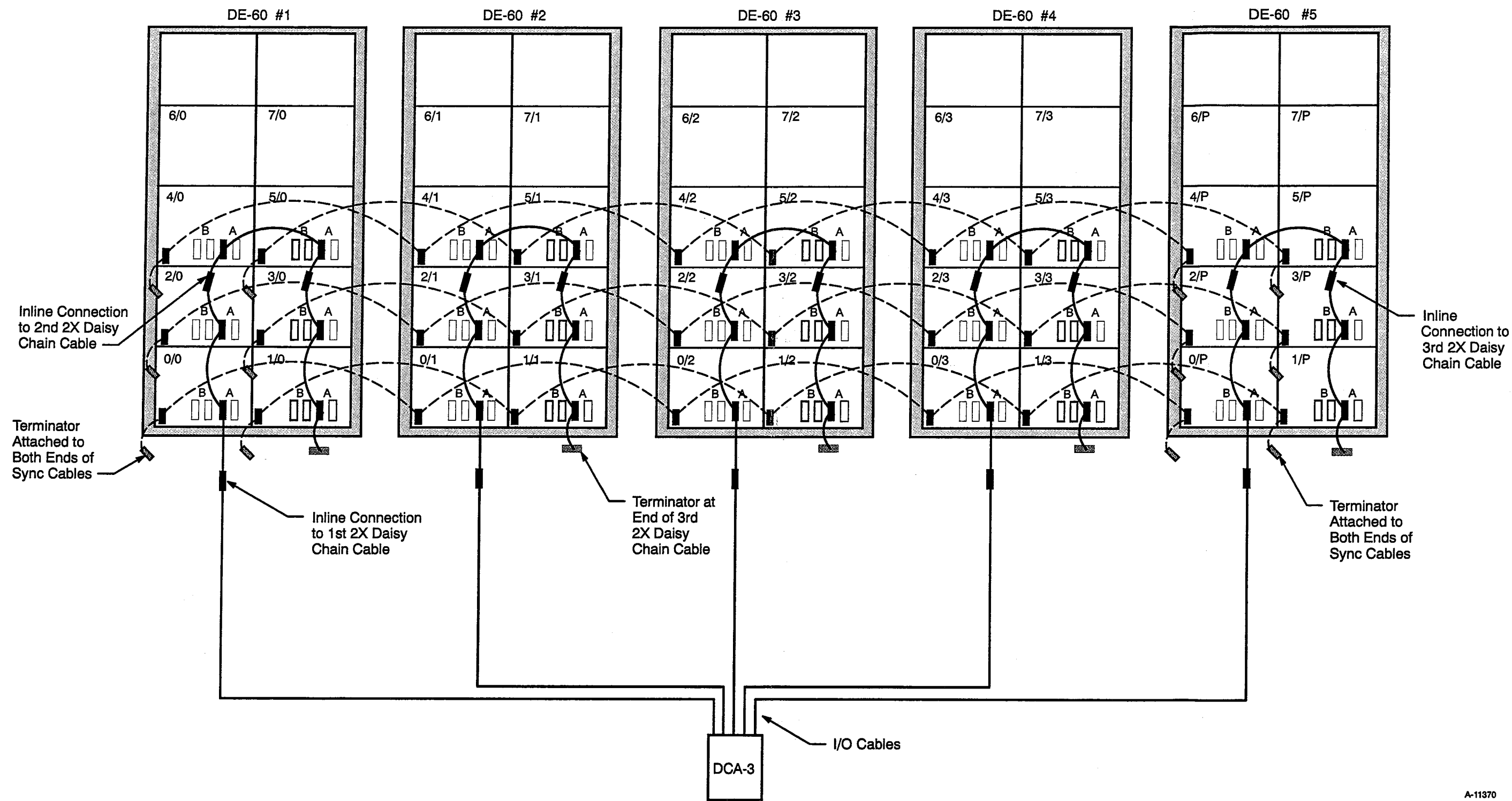
Figure 15-15. Single-channel, Six-array Daisy Chain
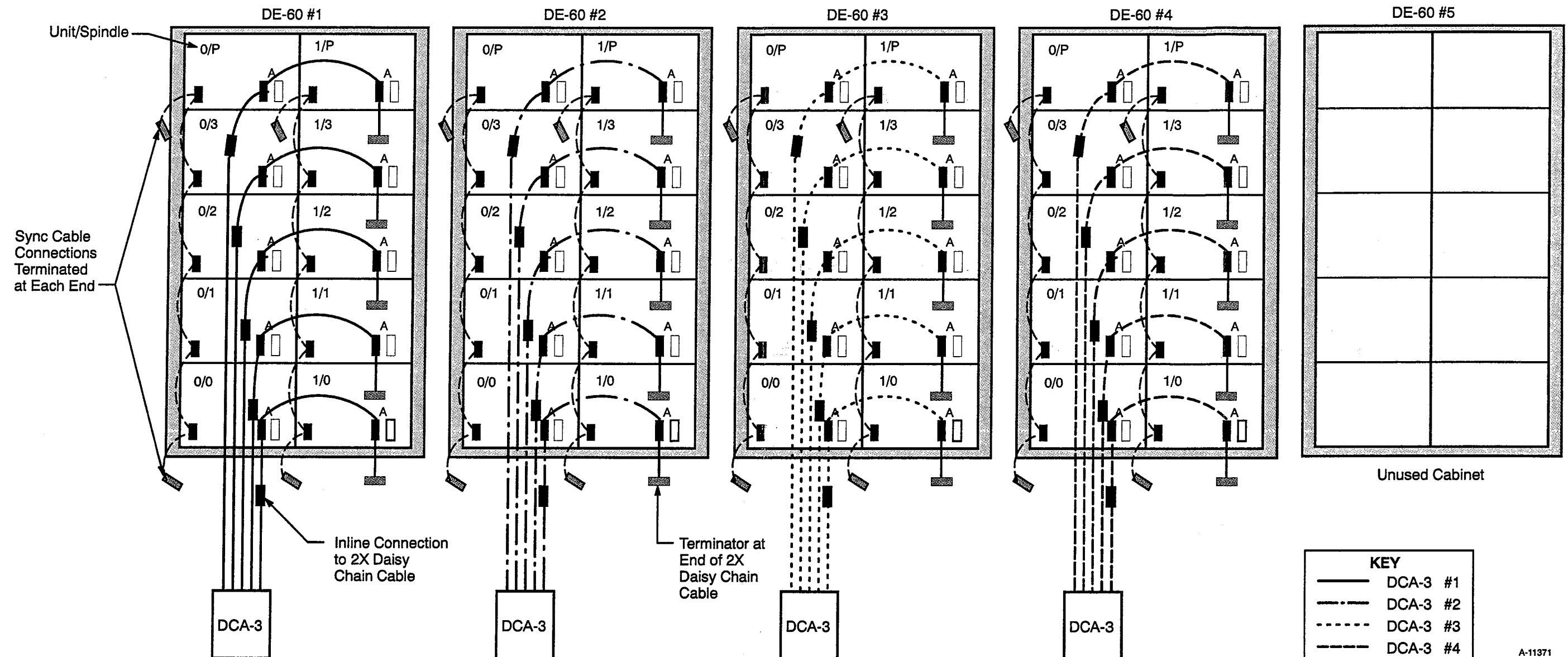
Figure 15-16. Four-channel, Eight-array Configuration with no Alternate Path or Disk Enclosure Resiliency

odd confg -d 0134.0 altpath   } puts Drives in Alternate path mode
odd confg -d 0134.1 altpath   }

   "   "   "   pripath   } puts drives back into primary path mode
              "   pripath   }
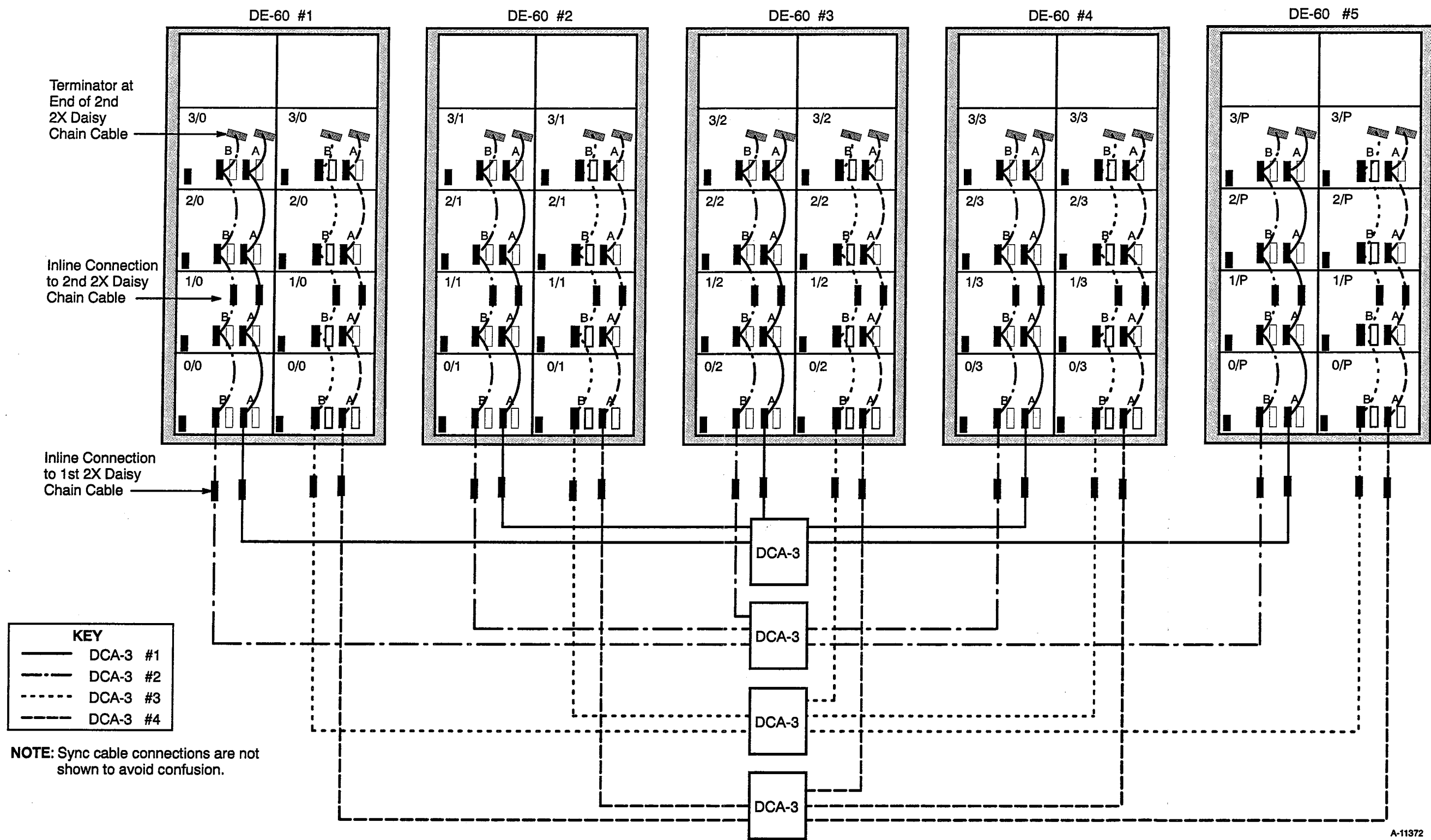
Figure 15-17. Four-channel, Eight-array Configuration with Alternate Path and Disk Enclosure Resiliency

SECTION 16
DCA-3 SYSTEMS STATUS

16 DCA-3 SYSTEMS STATUS

This section provides status information for 60 series disk array systems, including DCA-3 channel adapter status and disk drive status information for the DD-60 and DD-62 spindles.

Status Cross-references

The statuses for 60 series disk arrays can be displayed through the ERRPT and OLHPA report generators.

ERRPT

Figure 16-1 shows an ERRPT error report for a DA-62 disk array. Figure 16-2 shows the same error as reported by OLHPA. Refer to Table 16-1 for a cross-reference to the tables that describe each status.

```
DCA3 ERROR REPORT:

Thu Dec 01 21:03:16 1992

Disk error/Path summary:
          active =    1034.0    major = 32   minor = 214   type = da62
          primary =   1034.0
          alternate =0000.0
Resolution:
          recovery code = 006 / Recovered by disk stream reconstruct after 6
retries
IOS request:
          request code = 002 / read data
          length = 4 cyl = 00375 head = 003 sec = 006
IOS response:
          response code = 010 / io error
          error location       cyl = 00375 head = 003 sec = 015

DCA3 command(IOB:5/IOB:1) =  000020  command parameter(IOB:16) = 140714

Flags Area for All Drives:
          Bsy&DN      Bsy Flags   DN Flags    DMA Ack
          _____      _____   _____    _____

          000001      000001      000037      000000
```

Figure 16-1. ERRPT error display (sheet 1 of 2)

```
Status Response Block:
         Octet0   Octet1   Octet2   Octet3   Octet4   Octet5   Octet6   Octet7

Drive_0   000      000      000      000      000      000      000      000
Drive_1   000      000      000      000      000      000      000      000
Drive_2   000      000      000      000      000      000      000      000
Drive_3   000      000      000      000      000      000      000      000
Drive_4   000      000      000      000      000      000      000      000


Extended Status Response Block:
         Octet0   Octet1   Octet2   Octet3   Octet4   Octet5   Octet6   Octet7

Drive_0   257      000      100      363      000      000      000      004
Drive_1   257      000      100      323      000      000      000      001
Drive_2   257      000      100      323      000      000      000      001
Drive_3   257      000      100      323      000      000      000      000
Drive_4   257      000      100      323      000      000      000      000


         Adapter Stat        SECDED          Xfer Cnt         IPI Tags
         DCA12 A=0          DCA12 A=1        DCA12 A=2        DCA12 A=3

Drive_0    001240             000377           000000           000103
Drive_1    000240             000377           000000           000103
Drive_2    000240             000377           000000           000103
Drive_3    000240             000377           000000           000103
Drive_4    000240             000377           000000           000103


         Ending Stat        ID Param_0       ID Param_1      BusA/B Data
         DCA13 A=0          DCA13 A=1        DCA13 A=2        DCA13 A=3

Drive_0    100200             000375           000315           177600
Drive_1    100200             000375           000315           177600
Drive_2    100200             000375           000315           177600
Drive_3    100200             000375           000315           177600
Drive_4    100200             000375           000315           177600


Spindle 0:
Compressed ECC status:
         stream          ecc      offset   mask   defect
             1      12546003245   000361   0002   000035
             3      12546003245   000361   0002   000035


ERROR RECOVERY TRACE INFO(First to Last, all numbers in octal)

Disk  Disk  Rec   SRB    SRB    DCA12    DCA12    DCA13    Mcode    Mcode
Req   Resp  Par   Oct1   Oct0   A=1      A=0      A=0      Line     Sequence

002   010   004   001    000    000377   001240   100200   000000   da60rdrc
177   000   004   000    000    000377   000040   100200   000001   rdy6a
067   000   004   000    000    000377   000040   000401   000001   seek6a
002   010   004   001    000    000377   001240   100200   000012   da60rdrc
002   000   004   375    000    000377   000040   000401   000055   da60rdrc
002   000   004   375    000    000377   000040   000401   000012   da60rdrc
002   000   004   375    000    000377   000040   000401   000012   da60rdrc
002   000   004   375    000    000377   000040   000401   000012   da60rdrc
001   000   004   000    000    000377   000040   177777   000021   da60rdrc
```

Figure 16-1. ERRPT error display (sheet 2)

OLHPA

Figure 16-2 shows an OLHPA error report for a DA-62 disk array. This report reflects the same error information reported through ERRPT as shown in Figure 16-1. Flawing information for possible media defects is calculated and displayed by OLHPA. Refer to Table 16-1 for a cross-reference to the tables in this section that describe each status.

```
11/12/92 11:19:51 *******************************************************
HOST ERROR PACKET
Device: A62—01—0—34.0  Major: 032 Minor: 214
            Primary      Alternate  Active
I/O Path: 1034.0         0000.0     1034.0
IOS request: read data               IOS response: io error
Final status: Rec strm reconst
IOS—P: 01—0 Channel: 34/0            Device type: DA62     Retry count: 6
Requested cylinder: 000375            Head: 003 Sector: 0006  (Unicos)
Failing cylinder:   000375            Head: 003 Sector: 0015  (Physical)
Physical Block: 000063853
Request Length (sect): 000004    Spiral Offset: 000007
DCA12:A=0 status:  001240
General Status:  100001                     Last ml Status:   000377


Error Recovery Trace (last 20 entries, first to final)
—|———————————————————————————————————————————————————————————————————
  |Disk  Disk  Rec      SRB    SRB    M1       DCA12    Ending  Mcode   Mcode
##| Req  Resp  Param    Oct1   Oct0   Status   :A=0     Status  Line    Seq
—|———————————————————————————————————————————————————————————————————
00| 002  010   000004   001    000    000377   001240   100200  000000  da60rdrc
01| 177  000   000004   000    000    000377   000040   100200  000001  rdy6a
02| 067  000   000004   000    000    000377   000040   000401  000001  seek6a
03| 002  010   000004   001    000    000377   001240   100200  000012  da60rdrc
04| 002  000   000004   375    000    000377   000040   000401  000055  da60rdrc
05| 002  000   000004   375    000    000377   000040   000401  000012  da60rdrc
06| 002  000   000004   375    000    000377   000040   000401  000012  da60rdrc
07| 002  000   000004   375    000    000377   000040   000401  000012  da60rdrc
08| 001  000   000004   000    000    000377   000040   177777  000021  da60rdrc
—|———————————————————————————————————————————————————————————————————



DCA3 STATUS PACKET
Flags for all drives (bit 0 = spindle 0)
   Busy&Done      Busy Flags        Done Flags      DMA Acknowledge
———————————————————————————————————————————————————————————————————
   000001          000001            000037          000000

DCA3 Command: 000020   (Read Data)
      Parameter: 140714
```

Figure 16-2. OLHPA Error Report (Sheet 1 of 2)

		Spindle	0	1	2	3	P
D	A=0	Interrupt Status	001240	000240	000240	000240	000240
C	A=1	SECDED Status	000377	000377	000377	000377	000377
A:	A=2	Transfer Status	000000	000000	000000	000000	000000
12	A=3	IPI Tag Status	000103	000103	000103	000103	000103
D	A=0	Drive ending Status	100200	100200	100200	100200	100200
C	A=1	ID Parameter 0 Status	000375	000375	000375	000375	000375
A:	A=2	ID Parameter 1 Status	000315	000315	000315	000315	000315
13	A=3	Bus A/B Data	177600	177600	177600	177600	177600

DRIVE ERROR PACKET
Status Response Block

octet:	0	1	2	3	4	5	6	7
Spindle 0	000	000	000	000	000	000	000	000
Spindle 1	000	000	000	000	000	000	000	000
Spindle 2	000	000	000	000	000	000	000	000
Spindle 3	000	000	000	000	000	000	000	000
Spindle P	000	000	000	000	000	000	000	000

Extended Status Block

octet:	0	1	2	3	4	5	6	7
Spindle 0	257	000	100	363	000	000	000	004
Spindle 1	257	000	100	323	000	000	000	001
Spindle 2	257	000	100	323	000	000	000	001
Spindle 3	257	000	100	323	000	000	000	000
Spindle P	257	000	100	323	000	000	000	000

```
|****************** ECC Status for spindle 0 ******************|
| Odd Strm: Low Off: 000361 High Off: 000361 Defect Add: 00035|
|Combined Head Mask: 002          Flawing Defect Address: 00035|
```

```
|****************** ECC Status for spindle 1 ******************|
```

```
|****************** ECC Status for spindle 2 ******************|
```

```
|****************** ECC Status for spindle 3 ******************|
```

```
|****************** ECC Status for spindle P ******************|
```

Figure 16-2. OLHPA Error Report (Sheet 2)

Table 16-1. Status Name Cross-reference Chart

Table	Status Name	Obtained By
General Status Response Block		
Table 16-2	General status	OLHPA software
DCA-3:12 Statuses		
Table 16-3	Interrupt status bits	DCA3:12 channel function
Table 16-4	SECDED status bits	DCA3:12 channel function
Table 16-5	Transfer count status bits	DCA3:12 channel function
Table 16-6	IPI tag status bits	DCA3:12 channel function
Table 16-7	Busy status bits	DCA3:12 channel function
Table 16-8	Done status bits	DCA3:12 channel function
Table 16-9	DMA acknowledge-pending status bits	DCA3:12 channel function
DCA-3:13 Statuses		
Table 16-10	Drive ending status	DCA3:13 channel function
Table 16-11	Ending status byte returned on Bus B	IPI-2 protocol
Table 16-12	ID parameter 0 status	DCA3:13 channel function
Table 16-13	ID parameter 1 status	DCA3:13 channel function
Table 16-14	Bus A and B data	DCA3:13 channel function
Drive Status Response Block		
Table 16-15	Exception status (Byte 0)	Bus control command (44_{16})
Table 16-16	Unsolicited exceptions status (Byte 1)	Bus control command (44_{16})
Table 16-17	Bus control exceptions status (Byte 2)	Bus control command (44_{16})
Table 16-18	Drive exceptions status (Byte 3)	Bus control command (44_{16})
Table 16-19	Drive exceptions status (Byte 4)	Bus control command (44_{16})
Table 16-20	Drive exceptions status (Byte 5)	Bus control command (44_{16})
Table 16-21	Drive exceptions status (Byte 6)	Bus control command (44_{16})
Table 16-22	Drive exceptions status (Byte 7)	Bus control command (44_{16})
Drive Extended Status Block		
Table 16-23	Interface flags status (Byte 0)	Bus control command (48_{16})
Table 16-24	Data received flags status (Byte 1)	Bus control command (48_{16})
Table 16-25	Data control flags status (Byte 2)	Bus control command (48_{16})
Table 16-26	Disk drive status (Byte 3)	Bus control command (48_{16})
Table 16-27	Disk drive alarms status (Byte 4)	Bus control command (48_{16})
Table 16-28	Vendor defined status (Byte 5)	Bus control command (48_{16})
Table 16-29	Vendor defined status (Byte 6)	Bus control command (48_{16})
Table 16-30	Head skew status (Byte 7)	Bus control command (48_{16})
Flaw Location Information		
Table 16-31	OLHPA flaw location information	OLHPA software
DD-60 Rear Panel Display I/O Status		
Table 16-32	DD-60 rear panel display I/O status	DD-60 drive firmware

General Status

General status is generated by OLHPA software as a combination of bits from several statuses. Table 16-2 describes each bit of the general status.

Table 16-2. General Status

Bit	Name	Description
2^0	Spindle 0 Busy & Done	When set to 1, this bit indicates that an error on spindle 0 resulted in a Busy/Done condition. (Read from busy/done status bit 0).
2^1	Spindle 1 Busy & Done	When set to 1, this bit indicates that an error on spindle 1 resulted in a Busy/Done condition. (Read from busy/done status bit 1).
2^2	Spindle 2 Busy & Done	When set to 1, this bit indicates that an error on spindle 2 resulted in a Busy/Done condition. (Read from busy/done status bit 2).
2^3	Spindle 3 Busy & Done	When set to 1, this bit indicates that an error on spindle 3 resulted in a Busy/Done condition. (Read from busy/done status bit 3).
2^4	Spindle 4 Busy & Done	When set to 1, this bit indicates that an error on spindle 4 resulted in a Busy/Done condition. (Read from busy/done status bit 4).
2^5	Voltage fault	When set to 1, this bit indicates the +5.0V or −4.5V supply is out of range. (Read from interrupt status bit 4 ORed with bit 5 inverted).
2^6	Single-bit error	When set to 1, this bit indicates that a write data bit was in error, but was corrected with SECDED circuitry in the 7DL option. (Read from SECDED status single-bit count $\neq$0).
2^7	Double-bit error	When set to 1, this bit indicates that more than one write data bit was in error and that SECDED circuitry in the 7DL option was unable to correct them. (Read from SECDED status double-bit count $\neq$0).
2^8	Head Select Fault	When set to 1, this bit indicates that a spindle in the array received an invalid head selection. (Read from drive status byte 3, bit 5).
2^9	Off Cylinder Fault	When set to 1, this bit indicates that a spindle's heads were not positioned over the correct cylinder during a seek, or that the heads moved off a cylinder during a data transfer. (Read from drive status byte 3, bit 6).
2^{10}	Seek Fault	When set to 1, this bit indicates that an error occurred during a seek, read/verify data, or write data bus control operation. Refer to the drive exceptions status bytes 3 through 7, (Table 16-18 through Table 16-22), for more information. (Read from drive status byte 0, bit 2).
2^{11}	Spindle Fault	When set to 1, this bit indicates that an error occurred during a spin-up, spin-down, read/verify data, or write data bus control operation. Refer to the drive exceptions status bytes 3 through 7, (Table 16-18 through Table 16-22), for more information. (Read from drive status byte 0, bit 1).
2^{12}	Execution Fault	When set to 1, this bit indicates that an execution fault occurred. Refer to the drive exceptions status bytes 3 through 7, (Table 16-18 through Table 16-22), for more information. (Read from drive status byte 0, bit 0).
2^{13}	ID ECC error	When set to 1, this bit indicates that the ID field ECC read from the disk drive did not match the generated ECC from one or more of the 7DN options. (Read from interrupt status bit 9 AND bit 10).
2^{14}	ID compare error	When set to 1, this bit indicates that the ID of a sector read from one or more of the spindles did not compare to the expected ID stored in one or more of the 7DN options. (Read from interrupt status bit 8).
2^{15}	Data ECC error	When set to 1, this bit indicates that the data field error correction code (ECC) read from the disk drive did not match the generated ECC from one of the 7DN options. (Read from interrupt status bit 9 ANDed with bit 10 inverted).

DCA3:12 Statuses

This subsections contains information about the seven statuses returned by the DCA3:12 channel function.

Interrupt Status

The DCA3:12 function with an accumulator value of 0 returns interrupt status to the channel. Refer to the "DCA-3 Channel Functions" section of this manual for additional information on the interrupt status. Table 16-3 defines the interrupt status bits.

Table 16-3. Interrupt Status Bits

Bit	Name	Description
2^0	Spindle parity error (Bus byte parity error)	When set to a 1, this bit indicates that a byte parity error was detected by a 7DN option when data was read out of its deskew buffer.
2^1	IPI Sequence error	When set to a 1, this bit indicates that a drive function was attempted from an invalid initial state or that a select function timed out.
2^2	Lost data error	When set to a 1, this bit indicates that data transfers between the EIOP buffer and the DCA3 deskew buffer did not occur fast enough. Loss of rotational synchronization by a spindle can cause lost data errors. During chained read/write operations, this error may be the result of a data parity error or an ECC error on the previous sector.
2^3	Ending status error	When set to a 1, this bit indicates that a spindle's ending status bits 2^0 through 2^3 are non-zero, bit 2^7 is zero, or the ending status has a parity error.
2^4	-4.5V voltage fault	When set to a 1, this bit indicates that the −4.5 V supply is out of range.
2^5	+5.0V voltage good	When set to a 0, this bit indicates that the +5.0 V supply is out of range.
2^6	SECDED error	When set to a 1, this bit indicates that corruption of write data was detected by the 7DL option.
2^7	Data parity error (Striped parity error)	When set to a 1, this bit indicates that the parity regenerated on the data read from spindles 0 through 3 did not match the parity from spindle 4. This bit can only set if all 5 spindles are enabled during a striped read.
2^8	ID compare error	When set to 1, this bit indicates that the ID of a sector read from a spindle did not compare to the expected ID stored in the appropriate 7DN option. This bit cannot be set on a DCA3:5, function 21 command because the ID compare circuitry on the 7DN option is disabled during ID Verify routines.
2^9	ECC error	When set to a 1, this bit indicates that the newly generated ECC did not match the ECC read from a spindle. This error can occur on the ID or data field of a sector. Refer to interrupt status bits 8, 10, 12, and 13 for additional information.
2^{10}	ID error	When set to a 1, this bit indicates that a read or write operation was stopped by an ID error.
2^{11}	Hideable flaw	When set to a 1, this bit indicates that the ID read from a spindle sector was marked as having a hideable flaw. This bit is informational only.
2^{12}	Unhidable flaw	When set to a 1, this bit indicates that the ID read from a spindle sector was marked as having an unhideable flaw.
2^{13}	ID field flaw	When set to a 1, this bit indicates that the ID read from a spindle sector was marked as having an unhideable, ID field flaw.

Table 16-3. Interrupt Status Bits (continued)

Bit	Name	Description
2^{14}	Write protect	When set to a 1, this bit indicates that the ID read from a spindle sector was marked as being write protected.
2^{15}	Read protect	When set to a 1, this bit indicates that the ID read from a spindle sector was marked as being read protected. This bit is informational only.

SECDED Status

The DCA3:12 function with an accumulator value of 1 causes the SECDED status to be returned to the channel. Table 16-4 defines the SECDED status bits.

Table 16-4. SECDED Status Bits

Bit	Name	Description
2^0	Syndrome bit 2^0	These bits contain the syndrome bits generated by the 7DL option on SECDED errors.
2^1	Syndrome bit 2^1	
2^2	Syndrome bit 2^2	
2^3	Syndrome bit 2^3	
2^4	Syndrome bit 2^4	
2^5	Syndrome bit 2^5	
2^6	Syndrome bit 2^6	
2^7	Syndrome bit 2^7	
2^8	Single-bit error count 2^0	These bits contain the number of times the 7DL option detected a single-bit error. All four bits are set if the error count exceeds 17_8.
2^9	Single-bit error count 2^1	
2^{10}	Single-bit error count 2^2	
2^{11}	Single-bit error count 2^3	
2^{12}	Double-bit error count 2^0	These bits contain the number of times the 7DL option detected a double-bit error. All four bits are set if the error count exceeds 17_8.
2^{13}	Double-bit error count 2^1	
2^{14}	Double-bit error count 2^2	
2^{15}	Double-bit error count 2^3	

Transfer Count Status

The DCA3:12 function with an accumulator value of 2 causes transfer count status to be returned to the channel. This value represents the number of parcels remaining to be transferred to the drive when an operation was halted. Table 16-5 defines the transfer count status bits.

Table 16-5. Transfer Count Status Bits

Bits	Name	Description
2^0 through 2^{15}	Transfer count bits 2^0 through 2^{15}	These bits contain the current value of the transfer counter on the DCA-3.

IPI Tag Status

The DCA3:12 function with an accumulator value of 3 causes the IPI tag status to be returned to the channel. Table 16-6 defines the control bus status bits.

Table 16-6. IPI Tag Status Bits

Bit	Name	Description
2^0	Select Out	These bits indicate the state of the intelligent peripheral interface (IPI) when the status was read.
2^1	Slave In	
2^2	Master Out	
2^3	Sync In	
2^4	Sync Out	
2^5	Attention In	
2^6	Gate Bus A out	This bit indicates data sent out on Bus A.
2^7	Gate Bus B out	This bit indicates data sent out on Bus B.
2^8	Not used	These bits are not used.
2^9	Not used	
2^{10}	Not used	
2^{11}	Not used	
2^{12}	Not used	
2^{13}	Not used	
2^{14}	Not used	
2^{15}	Not used	

Busy Status

The DCA-3:12 function with an accumulator value of 4 causes the busy status to be returned to the channel. Table 16-7 defines the busy status bits.

Table 16-7. Busy Status Bits

Bit	Name	Description
2^0	Spindle 0 busy	When set to a 1, this bit indicates spindle 0 is busy
2^1	Spindle 1 busy	When set to a 1, this bit indicates spindle 1 is busy
2^2	Spindle 2 busy	When set to a 1, this bit indicates spindle 2 is busy
2^3	Spindle 3 busy	When set to a 1, this bit indicates spindle 3 is busy

Table 16-7. Busy Status Bits (continued)

Bit	Name	Description
2^4	Spindle 4 busy	When set to a 1, this bit indicates spindle 4 is busy
$2^5 - 2^{15}$	Not used	These bits are not used

Done Status

The DCA3:12 function with an accumulator value of 5 causes the done status to be returned to the channel. Table 16-8 defines the done status bits.

Table 16-8. Done Status Bits

Bit	Name	Description
2^0	Spindle 0 done	When set to a 1, this bit indicates spindle 0 is done
2^1	Spindle 1 done	When set to a 1, this bit indicates spindle 1 is done
2^2	Spindle 2 done	When set to a 1, this bit indicates spindle 2 is done
2^3	Spindle 3 done	When set to a 1, this bit indicates spindle 3 is done
2^4	Spindle 4 done	When set to a 1, this bit indicates spindle 4 is done
$2^5 - 2^{15}$	Not used	These bits are not used

DMA Acknowledge Pending Status

The DCA3:12 function with an accumulator value of 6 causes the direct memory access (DMA) acknowledge pending status to be returned to the channel. Table 16-9 defines the DMA acknowledge pending status bits.

Table 16-9. DMA Acknowledge-pending Status Bits

Bit	Name	Description
2^0	Spindle 0 pending	When set to a 1, this bit indicates spindle 0 has a DMA acknowledge pending
2^1	Spindle 1 pending	When set to a 1, this bit indicates spindle 1 has a DMA acknowledge pending
2^2	Spindle 2 pending	When set to a 1, this bit indicates spindle 2 has a DMA acknowledge pending
2^3	Spindle 3 pending	When set to a 1, this bit indicates spindle 3 has a DMA acknowledge pending
2^4	Spindle 4 pending	When set to a 1, this bit indicates spindle 4 has a DMA acknowledge pending
$2^5 - 2^{15}$	Not used	These bits are not used

DCA3:13 Statuses

The DCA3:13 statuses are transferred to the accumulator by a DCA-3:13 channel function. Refer to the section "DCA-3 Channel Functions," for more information on the DCA3:13 channel function.

Drive Ending Status

When the status select bits are both 0, the DCA3:13 channel function transfers the drive ending status to the accumulator. Refer to Table 16-10 for a description of the drive ending status parcel. On single drive functions the drive ending status parcel will contain two copies of the initial drive ending status byte. On dual drive functions this parcel will contain separate initial and final drive ending status bytes. The Ending Status byte is described in Table 16-11.

Table 16-10. Drive Ending Status

Bit	Name	Description
2^0	Final drive ending status bit 2^0	
2^1	Final drive ending status bit 2^1	
2^2	Final drive ending status bit 2^2	
2^3	Final drive ending status bit 2^3	These bits contain the final drive ending status byte.
2^4	Final drive ending status bit 2^4	
2^5	Final drive ending status bit 2^5	
2^6	Final drive ending status bit 2^6	
2^7	Final drive ending status bit 2^7	
2^8	Initial drive ending status bit 2^0	
2^9	Initial drive ending status bit 2^1	
2^{10}	Initial drive ending status bit 2^2	
2^{11}	Initial drive ending status bit 2^3	These bits contain the initial drive ending status byte.
2^{12}	Initial drive ending status bit 2^4	
2^{13}	Initial drive ending status bit 2^5	
2^{14}	Initial drive ending status bit 2^6	
2^{15}	Initial drive ending status bit 2^7	

Initial Drive Ending Status

The initial drive ending status contains the ending status byte returned on bus B after completion of a single, or the first of two, drive function sequences. For example, during a load position routine, the sequencer

performs one drive function sequence. The drive ending status from this sequence is stored in the initial drive ending status (upper byte) and copied to the final drive ending status (lower byte).

Final Drive Ending Status

The final drive ending status contains the second of two drive ending statuses returned on bus B after a dual drive function sequence. For example, during a write sector of data routine, the drive performs two function sequences. The initial drive ending status is received after the ID is read and compared. The final drive ending status is received after the write data has been transferred. On single drive function sequences, the final drive ending status (lower byte) is a copy of the initial drive ending status (upper byte).

Table 16-11. Ending Status Byte Definitions

Bit	Name	Description
2^0	Operation status bit 2^0	**Bits** **Description** 00_8 – The disk drive executed the bus control command and is available. 01_8 – The disk drive rejected the bus control command and is busy.
2^1	Operation status bit 2^1	04_8 – The disk drive did not detect the address mark. 05_8 – The disk drive did not detect the sync byte.
2^2	Operation status bit 2^2	06_8 – ECC error (not used by CRI) 07_8 – Verify ID miscompare (not used by CRI)
2^3	Operation status bit 2^3	10_8 – An operation exception occurred. The exception status (refer to Table 16-15), may be read for more information. 14_8 – An unsolicited exception occurred. The unsolicited exception status (refer to Table 16-16) must be read before continuing.
2^4	Time dependent operation	When set to 1, this bit indicates that the last command has not been completed by the disk drive. The disk drive will set the Attention In signal when it completes the command.
2^5	Odd byte transfer	When set to 1, this bit indicates that the last information transfer contained an odd number of bytes. If set, the last byte transferred on bus B is not valid.
2^6	Bus parity error	When set to 1, this bit indicates the disk drive detected a parity error on a bus control command, information transfer, or controller status.
2^7	Good transfer	When set to 1, this bit indicates the disk drive did not detect a parity error on a bus control command, information transfer, or controller status.

ID Parameter 0 Status

When status select bit 2^1 is 0 and bit 2^0 is 1, the DCA3:13 channel function transfers the ID parameter 0 status to the accumulator. Refer to Table 16-12 for a description of the ID parameter 0 status bits.

Table 16-12. ID Parameter 0 Status

Bit	Name	Description
2^0 through 2^{15}	Cylinder address (ID parameter 0)	These bits contain the current value of the cylinder register on the DCA-3.

ID Parameter 1 Status

When status select bit 2^1 is 1 and bit 2^0 is 0, the DCA3:13 channel function transfers the ID parameter 1 status to the accumulator. Refer to Table 16-13 for a description of each bit of the ID parameter 1 status.

Table 16-13. ID Parameter 1 Status

Bit	Name	Description
2^0	Sector address bit 2^0	These bits contain the current sector address.
2^1	Sector address bit 2^1	
2^2	Sector address bit 2^2	
2^3	Sector address bit 2^3	
2^4	Sector address bit 2^4	
2^5	Sector address bit 2^5	
2^6	Head address bit 2^0	These bits contain the current head address.
2^7	Head address bit 2^1	
2^8	Head address bit 2^2	
2^9	Head address bit 2^3	
2^{10}	Head address bit 2^4	
2^{11}	Not used	This bit is not used.
2^{12}	Read protection (RP)	When set to 1, this bit indicates that the RP bit was set in the ID field read from the sector. This bit is presently unused.
2^{13}	Write protection (WP)	When set to 1, this bit indicates that the WP bit was set in the ID field read from the sector. This bit is presently unused.
2^{14}	Not used	This bit is not used.
2^{15}	Not used	This bit is not used.

Bus A and Bus B Data

When status select bit 2^1 is 1 and bit 2^0 is 1, the DCA3:13 channel function transfers the IPI bus A and bus B data bytes to the accumulator. Refer to Table 16-14 for a description of each bit of the bus A and bus B data.

Table 16-14. Bus A and Bus B Data

Bit	Name	Description
2^0	Bus B data bit 2^0	These bits indicate the data byte on bus B
2^1	Bus B data bit 2^1	
2^2	Bus B data bit 2^2	
2^3	Bus B data bit 2^3	
2^4	Bus B data bit 2^4	
2^5	Bus B data bit 2^5	
2^6	Bus B data bit 2^0	
2^7	Bus B data bit 2^1	
2^8	Bus A data bit 2^0	These bits indicate the data byte on bus A
2^9	Bus A data bit 2^1	
2^{10}	Bus A data bit 2^2	
2^{11}	Bus A data bit 2^3	
2^{12}	Bus A data bit 2^4	
2^{13}	Bus A data bit 2^5	
2^{14}	Bus A data bit 2^6	
2^{15}	Bus A data bit 2^7	

Drive Status Response Block

The status response block is 8 bytes of IPI-2 status information transferred from the disk drive to the DCA-3. The status response block is read when a bus control code for read status (44_{16}) is issued to the disk drive over bus A. Tables 16-15 through 16-22 describe each bit in the status response blocks.

Table 16-15. Exception Status (Byte 0)

Bit	Name	Description
2^0	Execution fault	When set to 1, this bit indicates that a disk drive execution fault occurred. Refer to the drive exception status bytes 3 through 7, Tables 16-11 through 16–18, for more information on conditions that can cause the error.
2^1	Spindle fault	When set to 1, this bit indicates that an error occurred during a spin-up, spin-down, read/verify data, or write data bus control operation. Refer to the drive exception status bytes 3 through 7, Tables 16-11 through 16-18, for more information on conditions that can cause the error.
2^2	Seek fault	When set to 1, this bit indicates that an error occurred during a seek, read/verify data, or write data bus control operation. Refer to the drive exception status bytes 3 through 7, Tables 16-11 through 16–18, for more information on conditions that can cause the error.
2^3	Write fault	When set to 1, this bit indicates that an error occurred during a write data bus control operation. Refer to the drive exception status bytes 3 through 7, Tables 16-11 through 16-18, for more information on conditions that can cause the error.
2^4	Read fault	When set to 1, this bit indicates that an error occurred during a read/verify bus control operation. Refer to the drive exception status bytes 3 through 7, Tables 16-11 through 16-18, for more information on conditions that can cause the error.
2^5	Bus control exception	When set to 1, this bit indicates that the disk drive did not accept the last bus control command. Refer to the bus control exception status (byte 2), Table 16-17, for more information on conditions that can cause the error.
2^6	Unsolicited exception	When set to 1, this bit indicates that the disk drive has an unsolicited exception condition. Refer to the unsolicited exceptions status (byte 1), Table 16-16, for more information on conditions that can cause the error.
2^7	Status response	This bit is always set to 0 for a status response.

Table 16-16. Unsolicited Exceptions Status (Byte 1)

Bit	Name	Description
2^0	Media change	When set to 1, this bit indicates that the head disk assembly (HDA) was removed and replaced with another HDA.
2^1	Ready transition	When set to 1, this bit indicates that the disk drive changed from a not ready condition to a ready condition.
2^2	Not Ready transition	When set to 1, this bit indicates that the disk drive changed from a ready condition to a not ready condition.
2^3	Reserved	This bit is not used.
2^4	Alternate port format complete	When set to 1, this bit indicates that the alternate port received the notify alternate port of format completion bus control command.
2^5	Alternate port format change	When set to 1, this bit indicates that the alternate port accepted a new format specification.
2^6	Alternate port priority select	When set to 1, this bit indicates that the alternate port issued a disk drive address with the priority select bit set to 1.
2^7	Reset complete	When set to 1, this bit indicates that the disk drive completed a reset operation.

Table 16-17. Bus Control Exceptions Status (Byte 2)

Bit	Name	Description
2^0	Reserved	This bit is not used.
2^1	Reserved	This bit is not used.
2^2	Reserved	This bit is not used.
2^3	Data bus control late	When set to 1, this bit indicates that the bus control command was valid but the disk drive did not receive the command within a given time limit.
2^4	Bus control context	When set to 1, this bit indicates that the bus control command was valid but it conflicts with the current disk drive operation.
2^5	Unsupported bus control	When set to 1, this bit indicates that the bus control command was valid but the disk drive does not support the command.
2^6	Invalid parameter	When set to 1, this bit indicates that the bus control parameter was not valid.
2^7	Invalid bus control	When set to 1, this bit indicates that the bus control command issued was not valid.

Table 16-18. Drive Exceptions Status (Byte 3)

Bit	Name	Description
2^0	Reserved	This bit is not used.
2^1	Logic temperature fault	When set to 1, this bit indicates that the disk drive detected an overtemperature condition.
2^2	Voltage fault	When set to 1, this bit indicates that the disk drive detected a voltage that was out of range.
2^3	Reserved	This bit is not used.
2^4	Reserved	This bit is not used.
2^5	Head select fault	When set to 1, this bit indicates that the disk drive received an invalid head selection.
2^6	Off cylinder fault	When set to 1, this bit indicates that the heads were not positioned over the correct cylinder during a seek, or that the heads moved off cylinder during a data transfer.
2^7	Speed fault	When set to 1, this bit indicates that the platters did not reach the required rotation speed during spin-up or that they lost speed during a data transfer.

Table 16-19. Drive Exceptions Status (Byte 4)

Bit	Name	Description
2^0	Reserved	This bit is not used.
2^1	Reserved	This bit is not used.
2^2	Reserved	This bit is not used.
2^3	Data strobe fault	When set to 1, this bit indicates that the early or late data strobe was in effect when the disk drive received a write data bus control command.

Table 16-19. Drive Exceptions Status (Byte 4) (continued)

Bit	Name	Description
2^4	Head offset fault	When set to 1, this bit indicates that the heads were in an offset position when the disk drive received a write data bus control command.
2^5	Write transmission fault	When set to 1, this bit indicates that the disk drive received a write data bus control command but did not receive write data.
2^6	Reserved	This bit is not used.
2^7	Write protected fault	When set to 1, this bit indicates that the disk drive received a write data bus control command but was in write-protected mode.

Table 16-20. Drive Exceptions Status (Byte 5)

Bit	Name	Description
2^0	Reserved	This bit is not used.
2^1	Reserved	This bit is not used.
2^2	Reserved	This bit is not used.
2^3	Reserved	This bit is not used.
2^4	Reserved	This bit is not used.
2^5	Read/write diagnostic disable	When set to 1, this bit indicates that the internal read/write disk drive diagnostics are disabled.
2^6	Diagnostic test incomplete	When set to 1, this bit indicates that the disk drive failed to execute an internal diagnostic test.
2^7	Diagnostic status valid	When set to 1, this bit indicates that an error occurred during internal disk drive diagnostics.

Table 16-21. Drive Exceptions Status (Byte 6)

Bit	Name	Description
2^0	Head 0 error	When set to 1, this bit indicates that head 0 of the logical head group cannot write or read data.
2^1	Head 1 error	When set to 1, this bit indicates that head 1 of the logical head group cannot write or read data.
2^2	Head 2 error	When set to 1, this bit indicates that head 2 of the logical head group cannot write or read data.
2^3	Head 3 error	When set to 1, this bit indicates that head 3 of the logical head group cannot write or read data.
2^4	Head 4 error	When set to 1, this bit indicates that head 4 of the logical head group cannot write or read data.
2^5	Head 5 error	When set to 1, this bit indicates that head 5 of the logical head group cannot write or read data.

Table 16-21. Drive Exceptions Status (Byte 6) (continued)

Bit	Name	Description
2^6	Head 6 error	When set to 1, this bit indicates that head 6 of the logical head group cannot write or read data.
2^7	Heads 7 or 8 error	When set to 1, this bit indicates that head 7 of the logical head group cannot write or read data or that head 8 cannot write or read data.

Table 16-22. Drive Exceptions Status (Byte 7)

Bit	Name	Description
2^0	Reserved	This bit is not used.
2^1	Field overrun	When set to 1, this bit indicates that the heads moved past the end of the ID or data field boundary before a write or read data operation finished.
2^2	Sector overrun	When set to 1, this bit indicates that the heads moved past the end of a sector boundary before a write or read data operation finished.
2^3	Track overrun	When set to 1, this bit indicates that the heads moved past the end of the track before a write or read data operation finished.
2^4	Operation fault	When set to 1, this bit indicates that an error occurred during the last disk drive operation.
2^5	Data control late	When set to 1, this bit indicates that the disk drive did not receive the write or read data bus control command in the specified time limit.
2^6	Data control reject Bit 2^0	00 – Normal status. 01 – The write or read data bus control command was not valid.
2^7	Data control reject Bit 2^1	10 – The write or read data bus control command conflicted with a current disk drive operation. 11 – The disk drive received a write or read data bus control but the rotational position sensing (RPS) was disabled.

Drive Extended Status Block

The drive extended status block is 8 bytes of additional IPI-2 status information transferred from the disk drive to the DCA-3. The drive extended status block is read when the sequencer sends a bus control code for read status (48_{16}) to the disk drive over bus A. Tables 16-23 through 16-30 describe each bit in the drive extended status block.

Table 16-23. Interface Flags Status (Byte 0)

Bit	Name	Description
2^0	Format specification present	When set to 1, this bit indicates that a valid format specification was loaded to the disk drive.
2^1	Status pending interrupt enables	When set to 1, this bit indicates that the status pending interrupts are enabled so the disk drive can use the Attention In signal on the current port.

Table 16-23. Interface Flags Status (Byte 0) (continued)

Bit	Name	Description
2^2	RPS interrupt enabled	When set to 1, this bit indicates that the rotational positional sensing (RPS) interrupt is enabled so the disk drive can use the Attention In signal on the current port.
2^3	Command complete interrupt enabled	When set to 1, this bit indicates that the command complete interrupts are enabled so the disk drive can use the Attention In signal on the current port.
2^4	Reserve active	When set to 1, this bit indicates that the disk drive is reserved for use by the current port in use.
2^5	Alternate port enabled	When set to 1, this bit indicates that the alternate port is enabled.
2^6	Port number	When set to 0, this bit indicates that port A is in use. When set to 1, this bit indicates that port B is in use.
2^7	Extended status	This bit is always set to 1.

Table 16-24. Data Received Flags Status (Byte 1)

Bit	Name	Descriptions
2^0	Data ECC enabled	When set to 1, this bit indicates that the disk drive data field error-correction code (ECC) circuitry is enabled. This option is not used by CRI.
2^1	Header ECC enabled	When set to 1, this bit indicates that the disk drive ID field ECC circuitry is enabled. This option is not used by CRI.
2^2	Reserved	This bit is not used.
2^3	Late data strobe	When set to 1, this bit indicates that the late data strobe is active.
2^4	Early data strobe	When set to 1, this bit indicates that the early data strobe is active.
2^5	Offset magnitude bit 2^0	These bits indicate the magnitude of the head offset operation. If these bits are set to 0, the heads are not offset.
2^6	Offset magnitude bit 2^1	
2^7	Offset direction	When set to 0, this bit indicates that a positive offset of the heads is in effect. When set to 1, this bit indicates that a negative offset of the heads is in effect.

Table 16-25. Data Control Flags Status (Byte 2)

Bit	Name	Description
2^0	Reserved	This bit is not used.
2^1	Reserved	This bit is not used.
2^2	Reserved	This bit is not used.
2^3	Reserved	This bit is not used.
2^4	Reserved	This bit is not used.
2^5	Reserved	This bit is not used.
2^6	Spindle power on	When set to 1, this bit indicates that the disk drive power is on.
2^7	Write protected	When set to 1, this bit indicates that the disk drive is in write protected mode.

Table 16-26. Disk Drive Status (Byte 3)

Bit	Name	Description
2^0	Media present	When set to 1, this bit indicates that the head disk assembly (HDA) is present.
2^1	HDA ready	When set to 1, this bit indicates that the platters are rotating at the correct speed, and that the heads are loaded and positioned on the correct track.
2^2	Reserved	This bit is not used.
2^3	Reserved	This bit is not used.
2^4	Sync locked	When set to 1, this bit indicates that the spindle rotation is synchronized.
2^5	Master sync	When set to 1, this bit indicates that the spindle is currently assigned as the master sync device.
2^6	On cylinder	When set to 1, this bit indicates that the heads are over the correct cylinder.
2^7	Speed	When set to 1, this bit indicates that the platters are rotating at the correct speed.

Table 16-27. Disk Drive Alarms Status (Byte 4)

Bit	Name	Description
2^0	Reserved	This bit is not used.
2^1	Logic overtemperature	When set to 1, this bit indicates that the disk drive detected an overtemperature condition.
2^2	Voltage range error	When set to 1, this bit indicates that the disk drive detected an out-of-range voltage.
2^3	Reserved	This bit is not used.
2^4	Reserved	This bit is not used.
2^5	Illegal head select	When set to 1, this bit indicates that the disk drive has no heads selected, multiple heads selected, or the wrong head selected.
2^6	Reserved	This bit is not used.
2^7	Reserved	This bit is not used.

Table 16-28. Vendor-defined Status (Byte 5)

Bits	Name	Description
2^0 through 2^1	Reserved	These bits are not used.

Table 16-29. Vendor-defined Status (Byte 6)

Bits	Name	Description
2^0	Spindle type	When set to 0, this bit indicates that the disk drive is set to a 9-head parallel mode (DCA-2 application). When set to 1, this bit indicates that the disk drive is set to an 8-head parallel mode (DCA-3 application).
2^1 through 2^7	Reserved	These bits are not used.

Table 16-30. Head Skew Status (Byte 7)

Bits	Name	Description
2^0 through 2^7	Head skew bits	These bits contain the value of the head skew.

Flaw Location Information

The flaw location information reports the spindle(s) affected, the number of the physical head under which the flaw was detected, the location of the flaw within the sector, and a calculated defect parameter. It is calculated and displayed by the OLHPA software. Table 16-31 describes each entry of the flaw location information.

Table 16-31. OLHPA Flaw Location Information

Information	Description
Stream (Strm)	Indicates the data stream relative to a head within a head group
Offset (Off)	The correction offset contains the position of the detected data field corruption
Defect address	The defect address contains the defect parameter needed to position a defect pad over a single media defect
Combined head mask	An octal bit mask indicating the head(s) within a head group affected by data corruption
Flawing defect address	The flawing defect address contains the combined defect parameter needed to position a defect pad over one or more media defects within a single sector

DD-60 Rear Panel Display I/O Status

During normal disk drive operations, the DD-60 rear panel display shows the current I/O status for the disk drive. The I/O status contains information on the state of the disk drive hardware and fault information. Table 16-32 describes each I/O status display.

Table 16-32. DD-60 Rear Panel Display I/O Status

Status Display (Hex)	Description
00	Initial state after a powerup or slave reset. Successful completion of the power-up or slave reset diagnostics causes the display to change.
01	Initial state after power-on diagnostics or slave reset. Also indicates that a not-ready transition was detected.
02	Invalid setting of ID microcode switches.
03	Waiting for first ready (first spin-up after powerup or reset). Also indicates that the ready-to-not-ready transition was detected.
04	Timeout waiting for servo test to start.
05	Timeout waiting for servo test to end.
06	Timeout waiting for drive to respond to I/O board.
07	Waiting for ready transition after spin-up command was issued.
08	Undefined.
09	Successful execution of read and write diagnostics.
0A	Undefined.
0B	Undefined.
0C	Test failed, a logic failure occurred, or the heads moved off cylinder during the read and write diagnostics.
0D	Timeout occurred while waiting for the heads to move over the cylinder.
0E	On-cylinder signal was active after a seek or return-to-zero (RTZ) command was issued during read and write diagnostics.
0F	Expected active On-cylinder signal during read and write diagnostics.
10	Reserved.
11	Read/write fault occurred.
12	Attempted a read or write with a not–on-cylinder fault.
13	Attempted a read or write with a not-on-cylinder fault. A read/write fault also occurred.
14	First seek fault occurred.
15	Read/write fault and a first seek fault occurred.
16	Attempted a read/write while the heads were not on cylinder. A first seek fault also occurred.

Table 16-32. DD-60 Rear Panel Display I/O Status (continued)

Status Display (Hex)	Description
17	Attempted a read/write while the heads were not on cylinder, and a first seek fault and read/write fault occurred.
18	A write fault occurred.
19	A read/write fault and a write fault occurred.
1A	Attempted a read/write while the heads were not on cylinder, and a write fault occurred.
1B	Attempted a read/write while the heads were not on cylinder, and a read/write fault and a write fault occurred.
1C	A first seek fault and a write fault occurred.
1D	A read/write fault, a first seek fault, and a write fault occurred.
1E	Attempted a read or write while the heads were not on cylinder. A first seek fault and a write fault also occurred.
1F	Attempted a read or write while the heads were not on cylinder. A read/write fault, a first seek fault, and a write fault also occurred.
20	Reserved.
21	Attempted a write while write protected.
22	A head select fault occurred.
23	Attempted a write while write protected, and a head select fault occurred.
24	A voltage fault occurred.
25	Attempted a write while write protected, and a voltage fault occurred.
26	A head select fault and a voltage fault occurred.
27	Attempted a write while write protected, and a head select fault and voltage fault occurred.
28	A seek error occurred.
29	Attempted a write while write protected and a seek error occurred.
2A	A head select fault and a seek error occurred.
2B	Attempted a write while write protected, and a head select fault with a seek error occurred.
2C	A voltage fault and seek error occurred.
2D	Attempted a write while write protected. A voltage fault with a seek error also occurred.
2E	A head select fault, voltage fault, and seek error occurred.
2F	Attempted a write while write protected and a head select fault, voltage fault, and seek error occurred.
30	The write/read diagnostic failed. The internal components most likely to have caused the failure: • Control circuit board • IPI-2 logic circuit board • Multiple channel read/write failure or the diagnostic cylinder was not formatted • HDA module

Table 16-32. DD-60 Rear Panel Display I/O Status (continued)

Status Display (Hex)	Description
31	The write/read diagnostic failed. The internal components most likely to have caused the failure: • Read/write channel 8 circuit board • Multiple channel read/write failure or the diagnostic cylinder was not formatted • Control circuit board • IPI-2 logic circuit board
32	The write/read diagnostic failed. The internal components most likely to have caused the failure: • Read/write channel 0 and 7 circuit board • Read/write channel 8 circuit board • Control circuit board • IPI-2 logic circuit board
33	The write/read diagnostic failed. The internal components most likely to have caused the failure: • Read/write channel 0 and 7 circuit board • Control circuit board • IPI-2 logic circuit board • HDA module
34	The write/read diagnostic failed. The internal components most likely to have caused the failure: • Read/write channel 1 and 6 circuit board • Control circuit board • IPI-2 logic circuit board • HDA module
35	The write/read diagnostic failed. The internal components most likely to have caused the failure: • Read/write channel 2 and 5 circuit board • Control circuit board • IPI-2 logic circuit board • HDA module
36	The write/read diagnostic failed. The internal components most likely to have caused the failure: • Read/write channel 3 and 4 circuit board • Control circuit board • IPI-2 logic circuit board • HDA module
37	The write/read diagnostic failed. The internal components most likely to have caused the failure: • Read/write channel 8 circuit board • Control circuit board • IPI-2 logic circuit board • HDA module
38 through 7F	Undefined.
80 through FF	Reserved.

SECTION 17
MAINTENANCE PROCEDURES

17 MAINTENANCE PROCEDURES

The following subsection briefly describes the available diagnostics and covers several maintenance procedures to follow for servicing the 60 series disk drives. These procedures include installation and removal of the maintenance panel, spin-up and spin-down of the drives, spindle removal and replacement on an active channel, and conversion of a DD-60 from 9-head (DCA-2) to 8-head (DCA-3) mode.

Diagnostics and Utilities

Diagnostics used to test the 60 series disk drives include the maintenance panel diagnostics (refer to the next major subsection) and the offline device maintenance system 2 (DMS2). The utilities used to perform flaw management on the 60 series disk drives include the offline device flaw management (DFM) package and the online disk device maintenance system (DDMS).

Device Maintenance System 2

The DMS2 diagnostic package runs on a maintenance workstation model E (MWS-E) connected to Cray Research, Inc. (CRI) computer systems that have an IOS-E. The DMS2 program performs the following functions:

- Tests any of the 60 series disk drive products

- Communicates with DCA-2 and DCA-3 channel adapters through the DDCA3 diagnostic driver

- Performs basic testing of DCA-2, DCA-3, DD-60, DD-61, and DD-62 through the DCAXB.6X macrocode-based diagnostic

- Performs comprehensive testing of DCA-2, DCA-3, DD-60, DD-61, and DD-62 through the DCAXC.6X macrocode-based diagnostic

For more information on DMS2, refer to the DMS2 and DFM Reference Guide, CRI part number CDM-1032-PR1.

Disk Flaw Management System (DFM)

The DFM utility package runs on a MWS-E connected to CRI computer systems that have an IOS-E. The DFM program performs the following functions:

- Provides communication with DCA-2 and DCA-3 channel adapters through the FID3 (flawing) and FSA3 (surface analysis) drivers

- Performs flaw management for all 60 series disk drives including adding/deleting flaws, reading/writing flaw tables, and formatting for all 60 series disk drives

- Provides utilities for all 60 series disk drives for reading and writing of CRI serial numbers, format specifications, and drive specific information

- Performs surface analysis for all 60 series disk drives

For more information on DFM, refer to the DMS2 and DFM Reference Guide, CRI part number CDM-1032-PR1.

Disk Device Maintenance System (DDMS)

The DDMS program runs on CRI computer systems that have an IOS-E. The DDMS program performs the following functions:

- Performs surface reads, writes, and analysis within a selected range of cylinders, heads, and sectors

- Verifies the sector ID fields according to the contents of the user flaw table stored in the 60 Series disk drives

- Transfers data between a sector and the UNICOS spare map cylinder

- Reformats and rewrites sectors that contain a flaw

- Reads and writes the user flaw table on the 60 Series disk drives

- Performs initialization, spin-up and spin-down, and data reconstruction for spindles within a disk array

For more information on DDMS, refer to the *CRAY Y-MP,
CRAY X-MP EA, and CRAY X-MP Computer Systems UNICOS Online
Diagnostic Maintenance Manual,* CRI part number SPM-1012.

Maintenance Panel

Each DE-60 disk enclosure cabinet contains one maintenance panel. When connected to an individual disk drive, the maintenance panel runs diagnostic tests, requests status, changes the logical address, clears fault latches, and enables or disables write protection. Figure 17-1 shows the switches and displays on the maintenance panel.
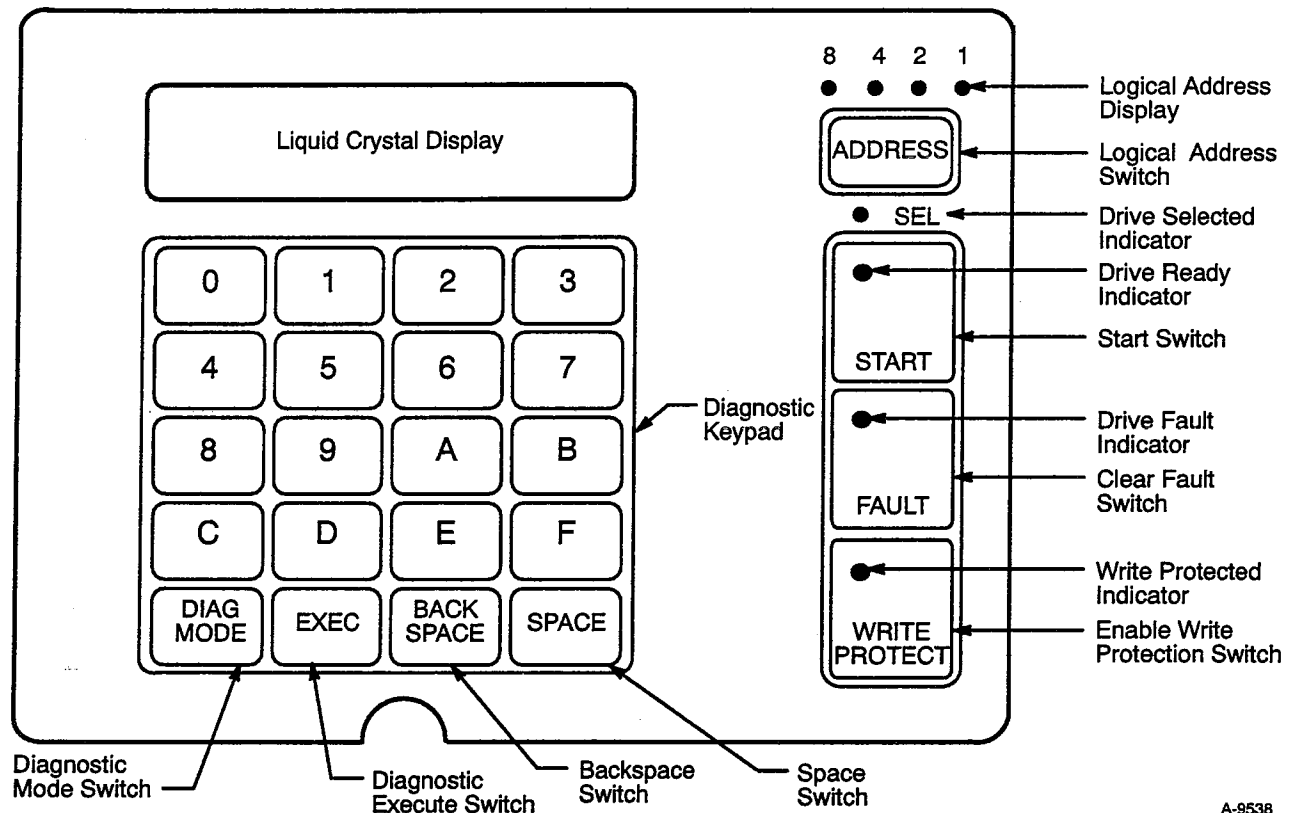
Figure 17-1. Maintenance Panel

Table 17-1 describes each of the switches and displays on the maintenance panel.

Table 17-1. Maintenance Panel Switches and Displays

Switch or Display	Description
Logical Address Display	These LEDs display the logical address of the disk drive. LED number 1 is the least significant bit. LED number 8 is the most significant bit.
Logical Address Switch (see CAUTION below)	Use the ADDRESS switch to enter the logical address. First, press and hold the logical address switch. The display increments through the addresses. When the display shows the correct address, release the logical address switch. When a maintenance panel is installed on a disk drive, the logical address switch overrides the address setting of the hardware DIP switches.
Drive Selected Indicator	The drive selected indicator (SEL) illuminates when the DCA-2 selects the drive for use by the channel.
Start Switch	Use the START switch to start the power-up sequence or power-down sequence for the disk drive.
Drive Ready Indicator	The drive ready indicator illuminates when the platters are up to speed, the heads are positioned over the first cylinder, and the disk drive is ready for use.
Clear Fault Switch	The FAULT switch clears all fault latches in the disk drive. Seek errors must be cleared with a return-to-zero command.
Drive Fault Indicator	The drive fault indicator illuminates if a fault condition exists on the disk drive.
Enable Write Protection Switch	Use the WRITE PROTECT switch to prevent data from being written to the disk drive.
Write Protected Indicator	The write protected indicator illuminates if the disk drive is in write protected mode.
Space Switch	Use the SPACE switch to add a space in diagnostic mode.
Backspace Switch	Use the BACKSPACE switch to remove the last character entered in diagnostic mode.
Diagnostic Mode Switch	Use the DIAG MODE switch to enter and exit diagnostic mode.
Diagnostic Execute Switch	Use the EXEC switch to start a selected test.
Diagnostic Keypad	Use the diagnostic keypad to enter the hexadecimal codes for diagnostic tests.
Liquid Crystal Display	The liquid crystal display displays the diagnostic tests and results.

CAUTION

The 60 series disk drives read the logical address setting on power up only. These drives must be power cycled anytime the logical address setting is changed to ensure the new address is read by the drive's hardware. Failure to do so will result in an inability to properly select the drive.

Installation and Removal

A minimum of one maintenance panel display per DE-60 is provided for DD-60 and DD-61 disk drives. A maintenance panel is included with each DD-62 and RD-62 disk drive. The following procedures describe how to connect the maintenance panel to the disk drives.

CAUTION

Do not remove or install the maintenance panel while the disk drive power supply is on. Severe damage to the maintenance panel may result.

Installation

Use this procedure to connect the maintenance panel to a disk drive:

1. Ensure that the disk drive is powered down and the on/standby switch on the front panel of the drive is in the standby (0) position.

2. Connect the maintenance panel cable to the disk drive.

3. Set the on/standby switch on the drive's power supply to the on (1) position.

4. Enter the correct logical address using the logical address switch on the maintenance panel (refer to Table 17-1). Power cycle the drive using the on/standby switch on the front of the drive. This will ensure that the address setting is read by the drive.

5. Press the START switch on the maintenance panel. The disk drive spins up and the ready indicator flashes for approximately one minute.

6. After the disk drive is ready, enter the diagnostic mode and execute tests 00 and 01 to examine the fault and status registers (or) execute tests 06 and 07 to clear the fault and status registers.

Removal

Use this procedure to disconnect the maintenance panel from a disk drive:

1. Press the START switch on the maintenance panel. The disk drive starts to spin down and the ready indicator on the START switch flashes.

2. After the ready indicator stops flashing, set the on/standby switch on the disk drive power supply to the standby (0) position.

3. Disconnect the maintenance panel cable from the disk drive.

Diagnostic Test Execution

The drives have internal diagnostic tests stored in memory. Perform the following steps on the maintenance panel keypad to select and begin a test:

1. Enter the diagnostic mode by pressing the DIAG MODE switch. The LCD display shows the following message:

    `DIAG TEST XX`

2. Enter the desired two-digit test number on the keypad. (Table 17-2 contains a list of maintenance panel tests and their descriptions.)

Table 17-2. 60 Series Disk Maintenance Panel Tests

Test	Name
00	Displays the contents of the status/error log
01	Displays the contents of the fault log or cylinder log
04	Displays the three internal components most likely to have failed
05	Performs a servo test
06	Clears the status/error log
07	Clears the fault log
08	Performs a seek to a specific cylinder from cylinder 0
09	Performs seeks to random cylinders
0C	Displays the erasable programmable read only memory (EPROM) part number
0E	Performs a return-to-zero seek
12	Performs seeks to sequential cylinders

3. Press the EXEC switch to start the test.

4. To end the test, press the EXEC switch again.

5. To run another test, repeat Steps 2 through 4. When finished, press the DIAG MODE switch to exit the diagnostic mode.

Spin Up and Spin Down Procedures

The following subsection describes procedures to properly spin the 60 series disk drives up and down. Procedural differences exist between DCA-2 and DCA-3 applications, as well as for drives with and without maintenance panels. Procedures are provided for the most common configurations and drive types.

CAUTION

Proper spin-up or spin-down procedures for 60 series disk drives depend on the drive type and whether a maintenance panel is connected. Failure to use the proper procedure can result in damage to the disk drive and/or the data it contains.

Spin Up/Down Procedures for DCA-2 Applications

The following subsection describes spin-up and spin-down procedure for 60 series disk drives connected to a DCA-2 channel adapter. Separate procedures are given for DD-60 and DD-62 disk drives.

DD-60 Disk Drive

Because DD-60 drives do not include a maintenance panel as standard equipment, the following procedures are written assuming this panel is not connected.

Spin-up Procedure

Use the following steps to spin up a DD-60 connected to a DCA-2.

1. Ensure that the main circuit breaker on the DE-60 cabinet is set to the on (up) position to supply power to the drive power supplies.

2. Set the power supply switch located on the front of the drive's power supply to the on (1) position; the DD-60 will perform a spin-up sequence automatically. The I/O status LEDs on the rear of the drive displays a 03 for approximately one minute while the drive is spinning up. The I/O status displays a 09 when the spin-up sequence is complete.

Spin-down Procedure

Use the following steps to spin down a DD-60 disk drive.

1. If an individual drive is to be powered off, set the drive's power supply switch, located on the front of the drive's power supply, to the off (0) position. The drive will automatically perform a spin-down sequence. The cabinet's main circuit breaker should only be set to the off (down) position after each drive has been powered off.

DD-61 Disk Drive

Because DD-61 drives do not include a maintenance panel as standard equipment, the following procedures are written assuming this panel is not connected.

Spin-up Procedure

Use the following steps to spin up a DD-61 connected to a DCA-2.

1. Ensure that the main circuit breaker on the DE-60 cabinet is set to the on (up) position to supply power to the drive power supplies.

2. Set the power supply switch located on the front of the drive's power supply to the on (1) position; the DD-61 will perform a spin-up sequence automatically. The green LED located on the rear of the drive illuminates when the spin-up sequence is complete.

Spin-down Procedure

Use the following steps to spin down a DD-61 disk drive.

1. If an individual drive is to be powered off, set the drive's power supply switch, located on the front of the drive's power supply, to the off (0) position. The drive will automatically perform a spin-down sequence. The cabinet's main circuit breaker should only be set to the off (down) position after each drive has been powered off.

DD-62 Disk Drives

Because the DD-62 drives include a maintenance panel as standard equipment, the following procedures are written assuming this panel is connected.

Spin-up Procedure

Use the following steps to spin up a DD-62 connected to a DCA-2.

1. Ensure that the main circuit breaker on the DE-60 cabinet is set to the on (up) position to supply power to the drive power supplies.

2. Set the power supply switch located behind the upper left corner of the drive's maintenance panel to the on (1) position.

3. Spin up the drive by pressing the START button on the front of the maintenance panel. The LED on the START button will blink for approximately 1 minute while the drive spins up. When spin-up is complete, the LED on the START button remains illuminated.

Spin-down Procedure

Use the following steps to spin down a DD-62 disk drive.

1. Spin down the drive by pressing the START button on the front of the maintenance panel. The LED on the START button blinks for approximately 1 minute while the drive spins down. When spin-down is complete, the LED on the START button is no longer illuminated.

2. If an individual drive is to be powered off, set the drive's power supply switch, located behind the upper left corner of the maintenance panel, to the off (0) position. Power to a drive should not be removed until the spin-down sequence is complete (refer to Step 1). The cabinet's main circuit breaker should only be set to the off (down) position after each drive has been powered off.

Spin Up/Down Procedures for DCA-3 Applications

The following subsection describes spin-up and spin-down procedures for 60 series spindles connected as a disk array to a DCA-3 channel adapter. Spindles connected to a DCA-3 are set to operate in remote mode to enable remote spin-up and spin-down commands via software. Separate procedures are given for DA-60 and DA-62 spindles.

DA-60 Spindles

Because DA-60 spindles do not include a maintenance panel as standard equipment, the following procedures are written assuming this panel is not connected.

Spin-up Procedure

Use the following steps to spin up a DA-60 spindle connected to a DCA-3 channel adapter.

1. Ensure that the main circuit breaker on the DE-60 cabinet is set to the on (up) position to supply power to the spindle power supplies.

2. Set the power supply switch located on the front of the drive's power supply to the on (1) position. The I/O status LEDs on the rear of the drive will display 03 to indicate the spindle is ready to execute a spin-up.

3. Issue a spin-up command to the spindle using system software or appropriate diagnostics.

Spin-down Procedure

Use the following steps to spin down a DA-60 spindle.

1. Execute a spin-down command using system software or appropriate diagnostics and allow 90 seconds for the spin-down to complete. This ensures that the spindle's heads are in the landing zone and not over customer data cylinders.

2. If an individual spindle is to be powered off, set the spindle's power supply switch, located on the front of the drive's power supply, to the off (0) position. Power to a drive should not be removed until the spin-down sequence is complete (refer to Step 1). The cabinet's main circuit breaker should only be set to the off (down) position after each drive has been powered off.

DA-62 Spindles

Because the DA-62 spindles include a maintenance panel as standard equipment, the following procedures are written assuming this panel is connected.

Spin-up Procedure

Use the following steps to spin up a DA-62 spindle connected to a DCA-3 channel adapter.

1. Ensure that the main circuit breaker on the DE-60 cabinet is set to the on (up) position to supply power to the spindle power supplies.

2. Set the power supply switch located behind the upper left corner of the drive's maintenance panel to the on (1) position.

3. Ensure that the START button on the front of the spindle's maintenance panel is in the correct position to allow remote spin-up. You can determine if the button is in the correct position by examining the Drive Status Code displayed on the maintenance panel LCD display. A status of 06 indicates that the spindle is ready and waiting for a remote spin-up command. If the status shows a 03, the spindle is not in the correct state to perform a spin-up sequence. Press the START button on the maintenance panel. A status of 06 will appear on the LCD display to indicate the spindle is ready to receive a remote spin-up command.

4. Issue a spin-up command to the spindle using system software or appropriate diagnostics.

Spin-down Procedure

Use the following steps to spin down a DD-62 spindle.

1. Execute a spin-down command using system software or appropriate diagnostics and allow 90 seconds for the spin-down to complete. This ensures that the spindle's heads are in the landing zone and not over customer data cylinders.

2. If an individual spindle is to be powered off, set the spindle's power supply switch, located behind the upper left corner of the maintenance panel, to the off (0) position. Power to a drive should not be removed until the spin-down sequence is complete (refer to Step 1). The cabinet's main circuit breaker should only be set to the off (down) position after each drive has been powered off.

Converting a DD-60 for DCA-3 Applications

A DD-60 connected to a DCA-2 operates as a 9-head parallel disk drive; a DD-60 spindle connected to a DCA-3 operates as an 8-head parallel device. If a DD-60 is being moved from a DCA-2 to a DCA-3, it must be converted from a 9-head to an 8-head mode of operation. Refer to the *Sabre Drive Maintenance Manual* (CZM-0971) for more detailed information on spindle assembly and disassembly procedures.

CAUTION
Wear an electrostatic discharge (ESD) smock, wrist strap, and ESD shoes during the installation or replacement process. Damage to the disk drive equipment will result if these precautions are not followed.

Perform the following steps to convert a DD-60 from a 9-head parallel disk drive to an 8-head parallel array spindle.

> **NOTE:** The need to convert a DD-60 from DCA-3 applications (8-head mode) to DCA-2 applications (9-head mode) should seldom occur. If this need arises, the necessary procedure can be deduced from following steps.

1. Remove the spindle from the DE-60 cabinet and place it on an approved working surface.

2. Remove the six (three on each side) T-8 torx screws used to secure the top cover to the spindle.

3. Remove the seven (three on the front, four on the rear) T-15 torx screws used to secure the top cover to the spindle.

4. Remove the top cover from the spindle.

5. Remove the four T-15 torx screws that secure the card guide to the vertical mounting brackets and remove the card guide.

6. Carefully remove the channel 8 read/write card and place it in an ESD-safe package. Refer to Figure 17-2 for the location of the channel 8 read/write card.

7. Install a terminator card (CRI part 01785200) into the connector that was vacated by removal of the read/write card in the previous step.

8. Replace the card guide over the remaining cards and ensure that the cards are properly seated in the guide slots. Secure the guide with the T-15 torx screws.

Read/Write Channels 0 and 7
Read/Write Channels 1 and 6
Read/Write Channels 2 and 5
Read/Write Channels 3 and 4
Read/Write Parity Channel 8 (Or Terminator on DCA-3 Disks)
IPI Logic Board

Card Guide

Control Board

Power Supply

I/O Transceiver Board

HDA Module

Front
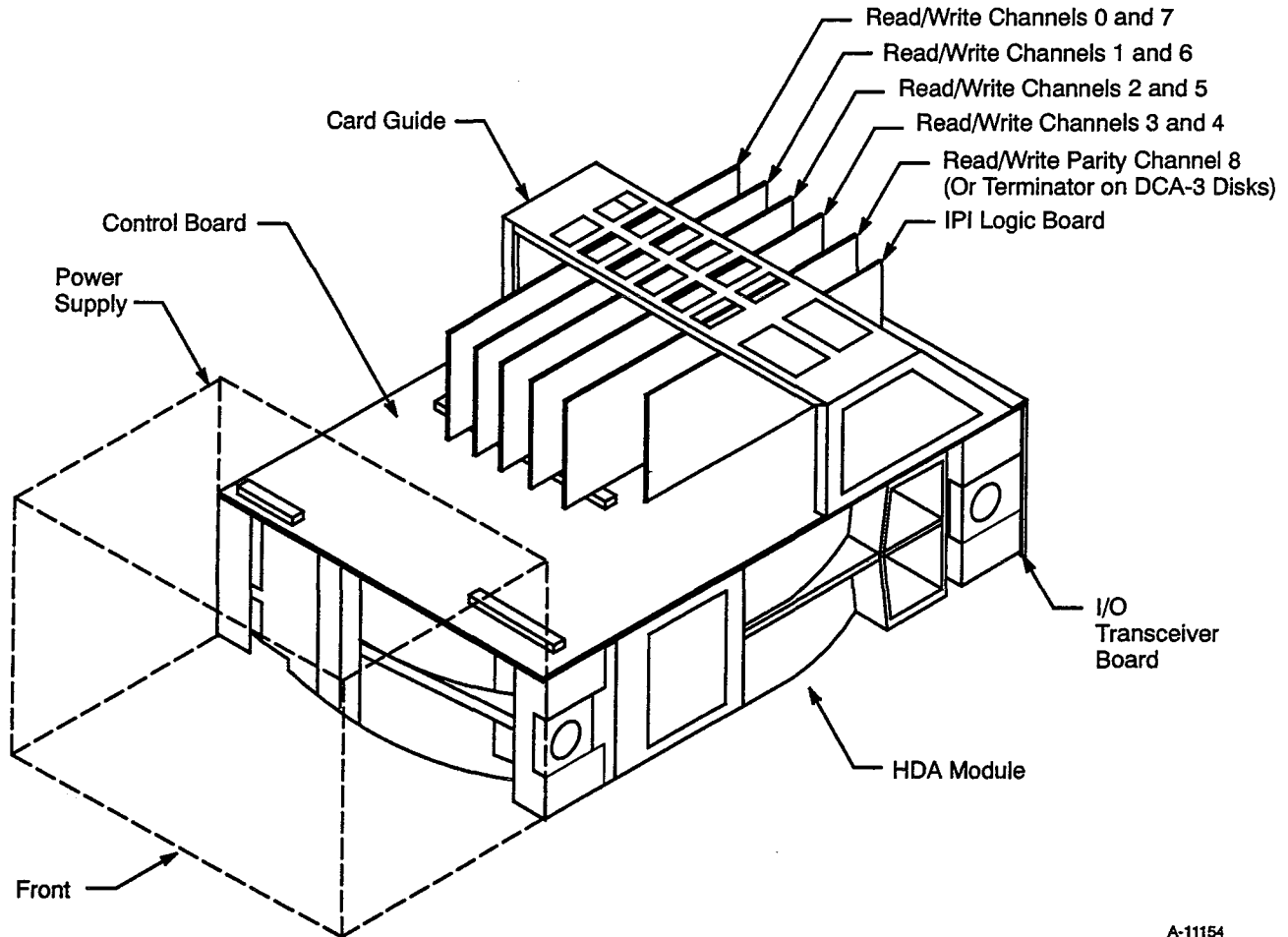
A-11154

Figure 17-2. DD-60 Read/Write Circuit Board Locations

9. Ensure that the internal power cord is properly routed, then replace the spindle top cover and secure it to the spindle using the T-15 and T-8 torx screws.

10. Locate DIP switch S2 on the back of the spindle. On S2, set switch 1 to the ON position and switch 8 to the OFF position (Refer to Figure 17-3 for switch settings).

11. Install the spindle into the DE-60 cabinet.

12. Ensure that the main circuit breaker on the DE-60 cabinet is set to the ON position to supply power to the spindle's power supply.

13. Set the power supply switch located on the front of the drive's power supply to the on (1) position. The I/O status LEDs on the rear of the drive displays 03 to indicate the spindle is ready to execute a spin-up.
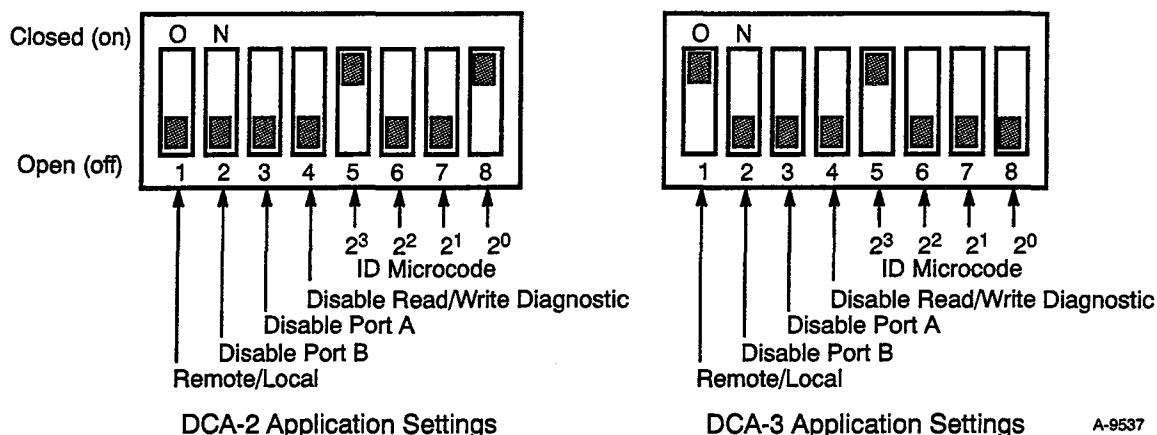
Figure 17-3. Lower DIP Switch (S2) Settings on the DD-60

14. Attach the data and synchronization cables to the spindle.

15. Issue a spin-up command to the spindle using the ddms online utility or an appropriate offline diagnostic.

16. Download the format specification to the spindle using the appropriate diagnostic. If the previous spin up (refer to step 15) is performed with the ddms utility, the format specification is automatically downloaded to the spindle as a subfunction of the spin up sequence.

CAUTION

Ensure the format specification is rewritten to 60 series drives whenever the ID microcode switch settings have been changed. Failure to do so will result in errors and possible data corruption.

---

17. The DD-60 is now ready for DCA-3 (8-head parallel) operation and can be configured as a spindle in a disk array.

Spindle Removal and Replacement Procedures

Perform the following steps to remove a 60 series spindle from a daisy chain of spindles that are cabled using the 2X daisy chain cable. The 2X daisy chain cable makes it possible to remove a failing spindle without affecting the other spindles connected to the same channel, providing proper procedures are followed.

1. Verify that the spindle to be removed has been logically disabled under the operating system. The pddconf command can be used to verify the current state of a disk array. It will report the array type, I/O path, and which spindles are currently enabled for reads and writes. Refer to Figure 17-4.

```
#pddconf
          disk devices
name  type  unit  state  mode  altp  flg  wstrm     rstrm

0130  DD60  0     up     rw    0132  1    ———————   ———————
0132  DD60  1     up     rw    0130  1    ———————   ———————
0134  DD62  0     up     rw    0136  1    ———————   ———————
0136  DD62  1     up     rw    0134  1    ———————   ———————
0234  DA60  0     up     rw    0236  1    0100037   0100037
0236  DA60  0     up     rw    0234  1    0100033   0100033
```

Figure 17-4. Example of pddconf command output

The wstrm and rstrm fields shown in Figure 17-4 represent the array/stream control bits for disk arrays. The upper most bit indicates that parity reconstruction mode is enabled on the DCA-3. The lowest five bits represent the five spindles of an array. A value of 37_8 indicates that all five spindles are enabled. A value of 33_8 indicates that spindle 2 is disabled on the array.

For disk array applications, UNICOS resiliency software will automatically disable a spindle if catastrophic failures are detected. Catastrophic failures include a spindle's inability to acknowledge a select, reset, or request for status information. In situations when a spindle causes repeated, non-catastrophic errors, the system administrator can manually disable a spindle using the pddconf command.

Example: **pddconf 0236.0 disable 2**

This example disables spindle 2 of disk array 0 connected to cluster 0, EIOP 2, channel 36. Subsequent system I/O references to this array are handled in a 4-spindle, parity reconstruction mode.

2.   Verify the physical location of the disabled spindle by matching the Cray Research serial number on the spindle with the Cray Research serial number contained in the spindle's flaw table header. This can be obtained through error report information or by using ddms to read and display the spindle's user flaw table.

     Example: **ddms —areadft 0236.0—2**

     This example reads and displays the flaw table for spindle 2 of disk array 0 connected to cluster 0, EIOP 2, channel 36. This step will not be possible if the failing spindle is incapable of performing reads.

┌───┐
│   **CAUTION**   │
├───┤
│ **Always ensure proper identification of a failing** │
│ **spindle. If the wrong spindle in a disk array is** │
│ **disabled, all data residing on the array may be lost.** │
│ **(As much as 7.84 GBytes for DA—60, or 10.95**   │
│ **GBytes for DA—62.)**   │
└───┘

3.   If the failing spindle is part of a disk array, execute a remote spin down command to the spindle from the operating system using the ddms utility. Do not power off the spindle.

     Example: **ddms —aspindown 0236.0—2**

     This example remotely spins down spindle 2 of disk array 0 connected to cluster 0, EIOP 2, channel 36.

┌───┐
│   **CAUTION**   │
├───┤
│ **Do not power cycle spindles connected to an**   │
│ **active channel. Always remove data and**   │
│ **sync cables from a failing spindle BEFORE**   │
│ **powering off the device. Power cycles cause**   │
│ **interference on a daisy chain, which can**   │
│ **affect other devices on the channel.**   │
└───┘

To verify that a spindle is spun down, check the I/O status display on the back of DD-60s (refer to Table 17-3), or check the maintenance panel LCD display on the front of DD-62s (refer to Table 17-4).

Table 17-3. DD-60 Rear Panel I/O Status Definitions

Status Code	Description
03	Power applied to spindle but HDA is **spun down.**
09	Power applied to spindle, HDA is **spun up**, internal write/read test completed, and ready for select.
01	Power applied to spindle, HDA is **spun up**, and device is ready for select.

Table 17-4. DD-62 Maintenance Panel Status Definitions

Status Code	Description
03	Power applied to spindle, HDA is **spun down**, START switch not pressed, not ready for remote spin up.
06	Power applied to spindle, HDA is **spun down**, START switch pressed, waiting for remote spin-up command.
10	Power applied to spindle, HDA is **spun up** and in sync.

4.   Remove the data cables (and sync cables if the spindle is part of a disk array) from the failing spindle **before** disabling power.

CAUTION

Do not power cycle spindles connected to an active channel. Always remove data and sync cables from a failing spindle BEFORE powering off the device. Power cycles cause interference on a daisy chain, which can affect other devices on the channel.

---

5.   Power off the failing spindle using the power switch on the front of the spindle's power supply.

6.   Remove the failing spindle from the cabinet and replace it with a
      working spindle. Handle the spindles carefully and observe all
      electrostatic discharge (ESD) precautions. Do not reconnect the
      data and sync cables until the new spindle has been powered on.

7.   Power on the replacement spindle by setting the power switch on
      the front of the spindle's power supply to the on (1) position.

      NOTE: If a maintenance panel is connected to the replacement
               spindle in an array, ensure that the START button on the
               front of the maintenance panel is in the correct position to
               allow remote spin-up.

               You can determine whether the button is in the correct
               position by examining the Drive Status Code displayed
               on the maintenance panel LCD display. A status of 06
               indicates that the spindle is ready and waiting for a
               remote spin-up command. If the status shows a 03, the
               spindle is not in the correct state to perform a spin-up
               sequence. Press the START button on the maintenance
               panel. A status of 06 will appear on the LCD display to
               indicate the spindle is ready to receive a remote spin-up
               command.

8.   After power is applied, reconnect the spindle's data and sync
      cables. The spindle is now ready to be configured into the
      operating system.

      For disk arrays, the ddms utility can be used to spin up a
      replacement spindle.

      Example: **ddms —a spinup 0236.0—2**
                    (allow 3 minutes for spinup and synchronization)

      This example will spin up spindle 2 of array 0 connected to cluster
      0, EIOP 2, channel 36.

9.   After the spindle is spun up, use the surf option of ddms to
      perform a quick write/read test on the scratch area of the new
      spindle to verify the performance of the hardware.

      Example: **ddms —a surf —C 0236.0—2**

      This example performs surface analysis on the scratch area (—C) on
      spindle 2 of array 0 connected to cluster 0, EIOP 2, channel 36.

10. Use the `reconstruct` option of ddms to initialize and reconstruct data to the new spindle.

Example: **ddms —a reconstruct 0236.0**

The flaw information is read from the new spindle and the UNICOS spares map is updated. Data is then read from the disk array in a 4-spindle, parity reconstruction mode and written back in 5-spindle mode. Upon completion, the disk array is reconfigured to 5-spindle mode for subsequent use.

If errors occur during the reconstruction, a ^C can be entered to abort the process and return the disk array to 4-spindle mode. If errors are encountered and the process is allowed to complete, a decision must be made regarding the nature of the errors. If the errors are critical, the disk array can be returned to a 4-spindle mode until the cause is resolved. If relatively few errors are encountered, owners of the affected files can be notified.

11. Finally, the `pddconf` command can be used to verify the current state of the affected disk array. If the spindle replacement is successful, all five array/stream control bits will be set in the `wstrm` and `rstrm` fields (37_8) to indicate the disk array has returned to a 5-spindle mode. Refer to Figure 17-5.

```
#pddconf
          disk devices
name  type  unit  state  mode  altp  flg  wstrm     rstrm

0130  DD60   0     up     rw    0132   1   ————————  ————————
0132  DD60   1     up     rw    0130   1   ————————  ————————
0134  DD62   0     up     rw    0136   1   ————————  ————————
0136  DD62   1     up     rw    0134   1   ————————  ————————
0234  DA60   0     up     rw    0236   1   0100037   0100037
0236  DA60   0     up     rw    0234   1   0100037   0100037
```

Figure 17-5. Example of `pddconf` command output

INDEX

Boldface numbers refer to illustrations and charts. Channel functions are listed numerically in the table of contents.

E

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