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# **CRAY®** COMPUTER SYSTEMS

PRE- DC/DD-40 MAINTENANCE MANUAL

CMM1103000

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Revision Description

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PREFACE

Section 1

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A. 1. A. 1.

This manual is intended to help Cray Research, Inc. (CRI) field engineers (FEs) maintain the DC-40 disk controller and the DD-40<sup>3</sup> disk storage device. The DC-40 has been designed and manufactured by CRI to control the DD-40, which consists of XMD spinoles. This is as CRI company private nanan na makana document and should not leave the site. H dision

This manual consists of seven sections. The following is a description North The Property and of each section:

Section	Description
1	Overview - introduces the DC-40 and DD-40,
2	DD-40 Drives - describes the XMD-III drives of the DD-40
3	Cabling - describes the cabling for the DC-40 and DD-40
4	Theory of Operations - describes the DC-40 modules
5	DC-40 Cooling System - describes the cooling system of the DC-40
6	DC-40 Maintenance - describes how to maintain the DC-40
7	Trouble shooting - provides trouble shooting procedures for the DC-40 and the DD-40

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The following publications are relevant to this manual:

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• HR - 0077 Disk Systems Hardware Reference Manual

• 'HR - 0080 Cray Peripheral Equipment Site Planning Reference Manual

Complete details of the DD-40 are contained in the following vendor manuals:

- "CDC Publication Volume 1 83325090 (CRI Publication Number xxxxxxxxx) ſ
- \* CDC Publication Volume 2 83325100 (CRI Publication Number XXXXXXXXXX)
- CDC Publication Volume 3 83325110 (CRI Publication Number xxxxxxxxx)

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The following devices are components of the I/O Subsystem (IOS) of a Cray computer system:

- I/O Processor (IOP)
- Disk Controller Unit-5 (DCU-5)
- DC-40 disk controller (DC-40)
- DD-40 disk storage device (DD-40)

The DD-40 stores information from a Cray computer system. The DC-40 is the interface between the DCU-5 and the DD-40. The DCU-5 is the interface between the IOP and the DC-40.

When the IOP executes a write request, the DC-40 receives the data from the channel, buffers it, and passes it to the DD-40. On a read request, the DC-40 retrieves the data requested from the DD-40, buffers it, and passes it to the channel. The DC-40 does error checking on the data that is read or written and relays status messages to the IOP.

#### WARNING

This device operates in accordance with FCC Part 15, Subpart J Rules.

#### 1.1 COMPONENTS OF THE DC-40

The DC-40 is designed and manufactured by CRI. It occupies a separate cabinet and consists of the following components:

- Four controllers
- Four power supplies
- One cooling system

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Each controller is functionally independent and can control up to two DD-40's. When there are two DD-40's on a controller, one is called the primary DD-40 and the other the shadow DD-40. Each DD-40 consists of four XMD spindles. Because a controller in the DC-40 can control two DD-40's, it can control eight spindles. A DC-40, consisting of four controllers, can control 32 spindles.

Each controller in the DC-40 consists of the following five types of modules:

- 2EI channel interface module
- 2EM disk multiplexer module
- 2EB full-track buffer module
- 2EK disk-data and error-correction module
- 2EJ disk controller module (four per controller)

There are four 2EJ disk controller modules and one of each of the other modules in each controller in the DC-40. Each 2EJ module controls read and write exchanges for a single spindle in the DD-40. The 2EJ module has a single cold plate; all the other modules have a double cold plate.

Figure 1-1 shows the interrelationship of the modules of the DC-40. This figure shows the modules of a single controller of the DC-40.

The DC-40 is cooled by a vapor compression type of cooling system. This system consists of a compressor, a condenser, two evaporators, an accumulator, valves, filters, piping, guages, and controls. The refrigerant used in the cooling system is R-22. Heat is absorbed by the liquid refrigerant from the modules and passed from the refrigerant to a water supply.

#### 1.2 IOS CONFIGURATION

Figure 1-2 shows an IOS with a single DC-40 and a primary and a shadow DD-40 connected to DC-40 controller 0. There are four controllers in the DC-40 and each of these can control a primary and a shadow DD-40. Each DD-40 has four spindles (A, B, C, and D).

One IOP can control up to four DCU-5's. Each DCU-5 can control up to four controllers in the DC-40. Thus one IOP can control up to 16 controllers (that is, up to four DC-40's). A full IOS configuration is as shown in figure 1-3. A single controller in the DC-40 can control up to 8 spindles, a DC-40 can control up to 32 spindles, and an IOP can control up to 128 spindles.

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2EK-ECC



Figure 1-2. IOS Configuration

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SHADOW DRIVES



Figure 1-3. Maximum IOS Configuration

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#### 1.3 DC-40/DD-40 SPECIFICATIONS

This section discusses the following specifications of the DC-40 and DD-40:

- Floor loading
- Heat rejection
- Power requirements
- DD-40 XMD spindle specifications

#### 1.3.1 FLOOR LOADING

The DC-40 cabinet weighs 1100 lbs (500 Kg) and takes up 7.3 sq ft (.68 sq m) of floor space. The DC-40 average floor loading is 150 lbs per sq ft (735 Kg per sq m). Figure 1-4 shows the DC-40 cabinet.



Figure 1-4. Dimensions of the DC-40 Cabinet

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The DD-40 cabinet weighs 800 lbs (364 Kg) and takes up 8.7 sq ft (.81 sq m) of floor space. The DD-40 average floor loading is 92 lbs per sq ft (449 Kg per sq m). Figure 1-5 shows the DD-40 cabinet.



Figure 1-5. Dimensions of the DD-40 Cabinet

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#### 1.3.2 HEAT REJECTION

The DC-40 generates approximately 28,000 BTUs per hour. It is freon-cooled by a self-contained refrigeration unit. The refrigeration condenser unit is cooled by an external water supply.

The DD-40 generates approximately 8,000 BTUs per hour. The heat generated by the DD-40 must be handled by the equipment room air conditioning.

1.3.3 DC-40/DD-40 POWER REQUIREMENTS

The following are the electrical power requirements for the DC-40 and the DD-40:

DC-40:

40A/phase, 120/208, 3 phase Y, 5-pin power plug: IEC 309

DD-40:

208 VAC, 3 phase, 5-pin power plug: NEMA L21 through 20P

The nominal operating current for the DD-40 is:

Phase A-B 2.8A Phase B-C 2.8A Phase C-A 5.6A

The nominal startup current for the DD-40 is:

21.4 A/phase for 3.5 seconds

Spindles A, B, and C start simultaneously, presenting a balanced load to the 3-phase line. Spindle D is started after spindles A, B, and C are up to speed.

1.3.4 DD-40 XMD SPINDLE SPECIFICATIONS

Table 1-1 lists the specifications for the XMD spindles of the DD-40.

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#### Table 1-1. Specifications for the XMD Spindles

Characteristic	Specification
Number of spindles per DD-40	4
Cylinders per spindle	1418 + 2 maintenance
Cylinders per DD-40	1418 + 2 maintenance
Data heads per spindle	19
Buffer capacity	48 sectors
Sectors per track	48
Sectors per cylinder	912
Data bytes per sector	4096
Bytes per spindle, formatted	1,324 Mbytes
Bytes per DD-40, formatted	5,297 Mbytes
Transfer rate	86 Mbits/s
Ports per DD-40	1
Drives active at one time	4
Minimum number of operational drives required per cabinet	4

#### 1.4 DC-40 CONTROLS AND INDICATORS

This section describes the controls and indicators for the DC-40.

Figure 1-6 identifies the controls and indicators of the power supply and refrigeration system control panel. Table 1-2 describes the function of the controls and indicators.

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Figure 1-6. Power Supplies and Refrigeration System Control Panel

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## Table 1-2. Power Supplies and Refrigeration System Control Panel Functions

Name	Function
POWER SUPPLY FAULT A,M indicator	Indicate out-of-range fault in power supplies A and M. A is the lower power supply. M is the upper power supply.
TEMPERATURE FAULT, HI, LO indicator	Indicate out-of-range temperatures within the DC-40.
VOLTAGE SELECT switch	Selects one of four power supply outputs to be displayed at the VOLTAGE READOUT METER.
VOLTAGE READOUT meter	Indicates the value of the selected power supply on the digital voltmeter.
POWER ON switch	Enables power supplies to provide power to the modules and opens the cooling system solenoid.
POWER OFF switch	Disconnects the power supplies from modules and puts the refrigeration system into the pump-down cycle. After about three seconds of pump- down, the compressor is automatically shut off.
ESD GROUND receptacle	Provides ground connection for draining off electrostatic dis- charge (ESD).

Figure 1-7 identifies the controls and indicators of the control panel for a single DC-40 controller. Table 1-3 describes the function of the controls and indicators. The controls and indicators shown for controller 0 are the same for controllers 1, 2, and 3.

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Figure 1-7. DC-40 Control Panel

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Name	Function
Port A Enable/ Disable switch	Allows port A to use the DC-40 when in the ENABLE position. Prevents port A from using the DC-40 when in the DISABLE position.
Port B Enable/ Disable switch	Allows port B to use the DC-40 when when in the ENABLE position. Prevents port B from using the DC-40 when in the DISABLE position. Both port A and port B may be enabled at the same time.
Clock 1,0 switch	Selects the logic clock speed.
Margin -5.2V -2.0V switch	Selects the voltage levels of the logic power supply outputs.
SECDED Enable/ Disable switch	Activates single error correction double error detection (SECDED) when in the ENABLE position. Inactivates SECDED when in the DISABLE position.
SECDED Test/ Norm switch	Allows testing of SECDED by forcing O's to be written into check bits.

Figure 1-8 identifies the controls of the DC-40 power panel. Table 1-4 describes the function of the controls. (This panel is located inside the rear of the DC-40 cabinet.)

CMM1103000



#### Figure 1-8. DC-40 Power Panel

Table 1-4. DC-40 Power Panel Functions

Name	Function
COMPRESSOR circuit breaker	Applies primary power to the compressor and control circuitry.
POWER SUPPLIES circuit breaker	Applies primary power to the power supplies. Observe the warning below.

#### 

#### WARNING

When powering off the DC-40, before turning off the COMPRESSOR and POWER SUPPLY circuit breakers on the DC-40 power panel, you must first press the POWER OFF switch on the power supply and refrigeration system control panel. The refrigeration system must be allowed to power down (about 3 seconds) before removing all power in order to prevent damage to the compressor at start up.

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DD-40 DISK DRIVE

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# DD-40 DISK DRIVE Hardware Training Aid

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# HTA-0859

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# **RECORD OF REVISION**



# PUBLICATION NUMBER HTA-0859

Each time this manual is revised and reprinted, all changes issued against the previous version are incorporated into the new version.

Comments about Cray Research, Inc. Training Volumes should be directed to:

Hardware Training Department Cray Research, Inc. 890 Industrial Boulevard Chippewa Falls, WI 54729 (715) 723-2206

# Revision Description

Α

August 1988 - Original printing.

September 1988. Page 7 added.

This device is exempt from the technical requirements of the FCC's Part 15 Subpart J Rules pursuant to Section 15.801(c).

HTA-0859

# **OBJECTIVES** - Overview

Upon completion of this section, the student will be able to:

- Describe each disk channel with respect to DCU-5 modules, DC-40 modules, and DD-40 drives
- Give specifications on the DC/DD-40 configuration
- Briefly describe each of the DC/DD-40 commands and functions

DC4004W102M

# **OBJECTIVES - DD-40**

Upon completion of this section, the student will be able to:

- Describe the functions of the DD-40, (seek, load, RTZ, write and read)
- Follow the flow charts and diagrams and know which part of the drive is involved with each step
- Explain errors that can occur with each of the drive functions
- Interpret the drive's selected status. (Refer to troubleshooting section)
- Explain the purpose of each part of the Sector Format
- Demonstrate the switch settings for the sector count and I/O Board switch settings

# **OBJECTIVES** - Cabling

Upon completion of this section, the student will be able to:

- Correctly cable the DCU-5, DC-40 and DD-40 together
- Identify and describe each signal on the A and B cables between the DC-40 and DD-40
- Locate the part numbers that identify different cables for the DC-40 and DD-40
- Re-cable DD-40 spindles for fault isolation

DC4004W104M

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# **OBJECTIVES - DC-40**

Upon completion of this section, the student will be able to:

- With the aid of the Boolean and diagrams, describe the major functions of the modules
- Follow the read and write paths through the DC-40 and give a description of what each module does during a read and write
- Determine the bad buffer chip, given the syndrome bits
- Interpret the error bits that are in General Status and Buffer Status and know the module where the bits originate
- Explain the function of each of the fields in the PROM sequencer
- Follow a sequence through the PROM Micro Code
- Explain how defect detection works

DC4004W105M
## **OBJECTIVES** - Lab

Upon completion of this section, the student will be able to:

- Load and run the DC-40 diagnostics and give an explanation of what each test section does
- Set up diagnostics to check out a given number of cylinders and heads
- Execute diagnostic tests from the Fault Display panel
- Use the micro tester to write test and execute diagnostics to the DC-40 and DD-40
- Take refrigeration readings and know how to make adjustments
- Demonstrate adding a flaw to the user flaw table with a defect and moving a defect pad
- Demonstrate writing and reading the O.S. flaw table

DC4004W106M

# DS-40 Commands

	D3-40	Commu	ius	2	8 1 30 m 1		
V	A RI	EGISTER	B R	EGISTER JAND	DESCRIPTION		
Crew 2	1DD000 1DD001 1DD010 1DD020 1DD021 1DD030 1DD040 1DD050 1DD070 1DD100 1DD101	Int. Addr. Int. Addr.	000000 000000 000000 000000 000000 00000	00000U 00000U 00000U 000000 000000 000000	Release Release Opposite and Select Reserve Clear Faults Reset Return to Zerot Select Status General Status Diagnostic Select Select Cylinder Select Head		
	REA	AD					
	1DD200	Int. Addr.	000000	RRRRR	Read disk data (with Read Ahead		
	1DD201 1DD202 1DD203 1DD204 1DD205 1DD206 1DD210 1DD212	Int. Addr. Int. Addr. Int. Addr. Int. Addr. Int. Addr. Int. Addr. Int. Addr. Int. Addr.	000000 000000 000000 000000 000000 00000	RRRRRR RRRRRR RRRRRR RRRRRR RRRRRR RRRRR	Enabled) Read ID Read Absolute Give must ended Read Buffer (16 parcels) Read Syndrome Block Compute Correction Vector Track Header Read disk data (with Read Ahead Enabled Read Buffer (2048 parcels)   Sector		
	WR	ITE					
	1DD300	Int. Addr.	000000	wwwwww	Write disk data (Write Behind Enabled)		
	1DD301 1DD302 1DD303 1DD304 1DD310 1DD314 1DD370	Int. Addr. Int. Addr. Int. Addr. Int. Addr. Int. Addr. Int. Addr. Int. Addr.	000000 000000 000000 000000 000000 00000	WWWWWW WWWWWW WWWWWW WWWWWW WWWWWW PPPPPP	Write ID Write Defective ID Write Buffer (16 parcels) Write Zero ECC -diag to Charge the Write disk data (Write Behind Disabled) Write Buffer (2048 parcels) 1 Sector Echo Parameter		

Jon 1

DEACH PARAM.

DC4004/117

## ACCUMULATOR BITS

## **FUNCTION**

*	DIA:1	Drive Control Functions	
		01000U	Unit select
		010007	Port select
		04hh00	Head select
		078888	Status select (5 status words available)
		10000	General status
		110000	Diagnostic select (2 options available to
		110004	perform Rus-In Parity errors and Status
			Parity errors)
		130000	Reset drive
		140000	Clear faults on drive
		150000	Return to zero
		160001	Release opposite and select
		170001	Release
		170000	Refease
*	DIA:2	Read	
		00xxxx	Read data record with read ahead
		01xxxx	Read ID
		02xxxx	Read absolute
		03xxxx	Read track buffer (16 parcels)
		04xxxx	Read ECC parameter block
		05xxxx	Compute and transfer correction vectors
		06xxxx	Read track header
· .		10xxxx	Read data record with no read ahead
		12xxxx	Read track buffer (1 sector)
*		N L-ite	
-	DIA:5		Write data record with write behind
			Write ID
		$01 \times \times$	Write defective D
		02xxxx	Write track buffer (16 parcels)
		038888	Write data with zero ECC
		07AAAA 10vvvv	Write data record with no write behind
		1/2222	Write track buffer (1 sector)
		170000	WITTE HACK DUITER (1 SECIOI)
*	DIA:4	Diagnostic Echo/Enter Defect Parameter	
		XXXXXX	Echoes xxxxxx out to the 2EI and back,
			and enters Defect Parameter into latches
			on the 2EK

\* DIA:5 Select Cylinder (Seek)

\* Accumulator value accompanies these commands and must be set up before issuing the command.

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- Bit
- $2^0 2^3$  Sector #
- 2<sup>4</sup> 2<sup>5</sup> Drive #
- 26 **Command Error** Command Error will set if a new FNX is received with a FNX in progress. Also if a FNX 12 is decoded, since a FNX 12 is not used in the DC40.
- 27 Channel Diagnostic Mode This bit is set when only the port is selected. The port is selected without selecting a drive when a Unit Select FNX is issued with the lower three bits set. This condition is held until a Unit Select is sent to select the drive, a Reset or a Release Opposite and Select will also clear the bit.
- 28 **Unit Ready** Unit Ready indicates that the drive is up to speed, that the first seek was successful, and that no fault condition exists.
- 2<sup>9</sup> On Cylinder This signal indicates that the servo head is positioned at a track. This line goes inactive if the positioner drifts off cylinder.
- 2<sup>10</sup> Seek Error This signal indicates that the drive took too long to complete a seek, that the positioner has moved outside the recording field, or that the drive was commanded to seek beyond cylinder 1063. The seek error can be cleared by an RTZ command.
- Fault When this line is active, it indicates that one or more of the following faults exists:
  - Read and Write Fault
  - Write or Read attempted while Off Cylinder
  - First Seek Fault
  - Write Fault
  - Write and Write Protected Fault
  - Head Select Fault
  - Voltage Fault
- 2<sup>12</sup> Write Protect This signal indicates that the drive write circuits are disabled. The write protect mode is enabled by a jumper plug on the control board, by a switch on the operator panel, by a fault condition, or by a loss of motor speed. Attempting to write while the write protect mode is active results in a fault condition.
- 2<sup>13</sup> Address Mark When an address mark has been found during an address mark search operation, this line goes high (refer to Tag 3 description).
- 2<sup>14</sup> Index Mark This signal is derived from the servo tracks. It occurs once per revolution of the disk, and its leading edge is the leading edge of sector zero. Note: This signal may be disabled by a switch selection on the I/O board.
- 2<sup>15</sup> Sector Mark This signal is derived from the servo tracks. The number of sector signals that occur for each revolution of the disk is selected by switches on the control board. Note: This signal may be disabled by a switch selection on the I/O board.

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**DD40 - WRITE TRANSFER** 

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## **DD40 - READ TRANSFER**

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DD40 SERVO CIRCUIT



Jibit Pattern

## CALCULATING DEFECT PARAMETER FROM CORRECTION VECTOR

The offset and mask obtained from the CRAYLOG after an ECC error on a DD-40 can be used to calculate a defect pad. The drive can then be reformatted to hide this defect. This should be done only for errors which are corrected in error recovery and repeat after being rewritten. The following algorithm should be used:

 $DEFPAD + R = \frac{100040_8 - OFFSET}{200_8}$ 

if  $R \ge 170_8$ , the defect is unhideable

Example:

$$OFFSET = 75366
 MASK = 003400
  $\frac{100040_8 - 75366_8}{200_8} = \frac{2452_8}{200_8} = 12 + R 52$$$

The defect pad entered in the diagnostic flaw table would be 12. The flaw should be added using format mode 2.

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#### DD-40 EXTRACT ERROR REPORT 1

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Final Status: Corrected 17:46:06.3159 Disk error packet Error type: Read Reason recovery invoked: DN and BZ both set IOP/Chan: 1/27 Device type: DD-40 Unit: 00 Retry count: 3 Expected cylinder: 000567 Expected head group: 000004 Expected sector: 000006 Controller status: 003211 Drive general status: 011406 Function: Read Buffer status: 011406 Final buffer status: 001406 Final drive status: 001406 Drive status: 001406 Offset: Disabled Correction mask: 003400 Previous offset: 051312 Offset: 051312 Previous correction mask: 003400

17:46:06.3467

*	Corrected data error	Read IOP device: 40-1-27A	Local dataset: DD-40	JSQ/Jo
	Cylinder: 0567	Head: 0004	Sector: 0000	-

SQ/Job name: 8/40127

 $\frac{(\#\text{Data bits}_8 + \text{ECC bits}_8) - \text{Offset}_8}{\text{bits in a defect pad}}$ 

 $\frac{100040_8 - 51312_8}{200_8} = \frac{26526_8}{200_8} = 132 \quad \text{R}126_8 = 86_{10}$ 

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## DD-40 EXTRACT ERROR REPORT 2

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17:59:21.1634	Disk error packet	Error type: Read	Final S	tatus: Corrected	
	Reason recovery invoked:	DN and BZ both set			
	IOP/Chan: 1/25	Device type: DD-40	Unit: 00	Retry count:	: 3
	Expected cylinder: 000004	Expected head	l group: 000013	Expected secto	vr: 000024
	Controller status: 114211	Drive general	status: 011430	Function: Rea	d
	Buffer status: 011430	Drive status: 001430	Final buffer status:	001430 F	inal drive status: 001430
	Offset: Disabled				
	Correction mask: 001400	Offset: 074674 Pre	evious correction mask:	001400 Pre	vious offset: 074674

17:59:21.1898

\* Corrected data error Cylinder: 0004 Read IOP device: 40-1-25A Head: 0013 Local dataset: ZZZ25A Sector: 0000

JSQ/Job name: 6/DD125A

(#Data bits + ECC bits) - Offset bits in a defect pad

$$\frac{100040_8 - 74674}{200} = \frac{3144}{200} = 14 \quad \text{R} = 144_8 \text{ or } 100_{10}$$

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DATA PATH WRITE MODE 0

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DATA PATH READ MODE 0

CRAY PROPRIETARY

17

# COMMAND LIST

## COMMAND

## **DESCRIPTION**

DS EX	(Diagnostic start ; Run the selected diagnostics) (Exit ; Prepare spindles for power down)			
MC RC RD RG X	<ul> <li>(Master clear ; Software reset)</li> <li>(Reset all selected disk controllers)</li> <li>(Reset all selected disk cabinets)</li> <li>(Display the contents of an operand registing X = Register number to display</li> </ul>	ster)		
D XXXX DL XXX DR XXX DF DE DC	<ul> <li>(Display memory)</li> <li>(Display memory left)</li> <li>(Display memory right)</li> <li>(Display Forward)</li> <li>(Display the error table)</li> <li>(Display counts for flaw tables) (First left)</li> </ul>	XXXX = Memory Address XXXX = Memory Address XXXX = Memory Address oad the tables)		
S XXXX YYYY S+XXXX YYYY	(Store a value to memory) (Store consecutive memory locations) XXXX = Memory Address YYYY = Value to be stored			
ST ZZ Y X RT ZZ Y X VF ZZ Y X LF ZZ Y X CF ZZ Y X	(Save a flaw table on the expander disk) (Restore a flaw table from the expander (Display a active flaw table) (Load an active flaw table from a DC40 (Clear an active flaw table) ZZ = Channel number of DD40 cabinet Y = Unit number X = Spindle number	disk) disk)		
CFA	(Clear all active flaw tables)			
AF ZZ Y X WWW RF ZZ Y X WWWW	V VV UU TTT S R (Add a flaw to the a V VV UU TTT S R (Remove a flaw to to ZZ = Channel number of the DD40 cabin Y = Unit number X = Spindle number WWWW = Cylinder VV = Head number UU = Sector number TTT = Defect position S = CRI added R = Unhidable defect	active flaw table) the active flaw table) net		

DC4003C26M

PARCEL 1



PARCEL 2

LOWER 4 BITS OF CYLINDER SECTO	PR # UNIT #	CHANNEL #
-----------------------------------	-------------	-----------

PARCEL 3



## FOURTH PARCEL \*

The fourth parcel will be either the logical difference if a data error or Status register 1 if the error was other than a data error.

\* This information is only available in Local Memory.

Hardware Trng. DC4004/113A S.J.M.

#### DC40 - DC40/DD40 DIAGNOSTIC

#### **ENGINEERING - CHIPPEWA FALLS - 11/04/86**

#### **PARAMETERS**

220 =	= Section selects (Lower)			
	1 -	Section 0	2EI data echo through save bus out	
	2 -	Section 1	Force a parity error	
	4 -	Section 2	Full track buffer data bus	
	10 -	Section 3	Full track buffer drive secded	
	20 -	Section 4	Full track buffer spindle addressing	
	30 -	Section 5	Full track buffer sector addressing	
	100 -	Section 6	Track buffer memory	
	200 -	Section 7	Header Reads - Seek Timing - Head Address	
	400 -	Section 10	Correction vector analysis	
	1000 -	Section 11	Disk data bus - scratch cylinder	
	2000 -	Section 12	Disk spindle addressing - scratch cylinder	
	4000 -	Section 13	Disk sector addressing - scratch cylinder	
	10000 -	Section 14	Defect pad writeability	
	20000 -	Section 15	Chaining - write ahead / read ahead	
	40000 -	Section 16	Disk system exerciser	
1	- 00000	Section 17	Seek distance / data verification	

221 = Section selects (Upper)

- 1 Section  $2\overline{1}$  Flaw table generation from factory headers
- 2 Section 22 Disk formatting
- 4 Section 23 Write the O.S. flaw table on O.S. cylinder
- 10 Section 24 Surface analysis
- 222 = Number of passes to run 177777 means infinite
- 223 = Type of disk to test
  - 0 = DD40
    - 1 = DD10
- 226 = Flaw table reference enable
  - 0 = Disable
  - 1 = Enable (default)
- 230 = Spindle number to test (starting)
- 231 = Spindle number to test (ending)
- 232 = Head number to test (starting)
- 233 = Head number to test (ending)
- 234 = Cylinder number to test (starting)
- 235 = Cylinder number to test (ending)
- 240 = IOP channel number for the display
- 241 = IOP channel number for the keyboard
- 242 = Timeout delay used in wait for done (lower)
- 243 = Timeout delay used in wait for done (upper)
- 244 = Number of sectors in each track buffer drive (148 normally)
- 245 = Number of cylinders in one spindle
- 246 = Number of heads in one spindle

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- 250 = Retry count (used in formatting)
- 251 = Scratch cylinder address
- 252 = Flaw table cylinder address
- 253 = Flaw table head number
- 254 = 0.S. flaw table sector number
- 255 = 0.S. flaw table drive number
- 256 = 0.S. flaw table head number
- 257 = O.S. flaw table track number
- 260 = Channel number and unit number for the drive under test. Example:

LOC.	ENTRY	MEANING
260 261 262 263 264 265 266 266 267	000025 100026 177777 177777 177777 177777 177777 177777	Chan 25, unit 0 Chan 26, unit 1 No more

NOTE: These entries must be in ascending order by channel number.

#### ERROR INFORMATION

- 12 = Current test section
- 13 = Current test condition
- 14 =Error code
  - 1 Timeout channel never got done (done = 0 after delay)
  - 2 Channel error (busy = 1, done = 1)
  - 3 Channel took longer to finish than expected
  - 4 Hardware error check status registers
  - 5 Unexpected interrupt
  - 6 Channel not busy too soon
  - 7 Channel done too soon
  - 10 Status registers error
  - 11 Data compare error
  - 12 Software error contact Engineering
  - 13 Exit stack under run
  - 14 Track header defect position past end of track
  - 15 Could'nt find any UD's
  - 16 Unexpected interrupt on DC40 channel
  - 17 Chaining broken
  - 20 Hardware error during chaining check status registers
  - 21 Did'nt get an expected ECC error
  - 22 Timeout on waiting for a DC40 interrupt
  - 23 Did'nt get an expected sync time out
  - 24 Got an ECC error but data compare did'nt fail
  - 25 No writeable sectors, found only defective sectors
  - 26 O.S. flaw table buffer overflow
  - 27 Out of memory for the active flaw table buffer
  - 30 Could'nt find the end of the flaw table
  - 31 Incorrect flaw table on the current spindle

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32 - Could'nt find the flaw table in active memory

33 - Out of temporary buffer space34 - Could'nt find the flaw table entry

35 - Flaw table is too big; it won't fit in buffer memory image

36 - Incomplete flaw table (missing hideables or unhideables)

37 - Empty disk flaw table

40 - The real-time clock is defective

41 - Not enough space on the current spindle trace42 - Could'nt find a clean track on the selected cylinder

43 - Seek distance exceeded the last entry of the seek time chart

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- 20 = Logical difference 21 = Actual data
- 22 = Expected data 23 = Error count
- 24 = Pass count
- 25 = Location in listing where error occurred (E)
- 26 =
- Stop on error flag 0 continue after error and update error count
  - 1 stop on error

## **STATUS INFORMATION**

320 =	STAT0 Bit 0 Bit 1 Bit 2 Bit 3 Bit 4 Bit 5 Bit 6 Bit 7	<pre>(Status register 0) = Drive ready = Drive Status available = Drive Busy/invalid drive command = Drive error = Status parity error = Bus-in parity error = Read data parity error = Frror flag</pre>
321 =	Bit 8-15 STAT1 Bit 0-3 Bit 4-5 Bit 6 Bit 7	= Parameter register (General status) = Sector number of last error = Drive number of last error = Channel error = Ruffor error
	Bit 7 Bit 8 Bit 9 Bit 10 Bit 11 Bit 12	<ul> <li>= Buffer error</li> <li>= Unit ready (all four spindles)</li> <li>= On cylinder (all four spindles)</li> <li>= Seek error (on any of the four spindles)</li> <li>= Drive fault (on any of the four spindles)</li> <li>= ECC error (sector status of last error)</li> </ul>
322 =	Bit 13 Bit 14 Bit 15 STAT2 Bit 0-3 Bit 4-5 Bit 6 Bit 7 Bit 8 Bit 9	<ul> <li>= ID not found (sector status of last error)</li> <li>= Sync time out (sector status of last error)</li> <li>= Defect parity error (sector status of last error)</li> <li>(Track buffer status)</li> <li>= Sector number</li> <li>= Drive number</li> <li>= Uncorrectable buffer error</li> <li>= Buffer error</li> <li>= Unit ready (on specified drive)</li> <li>= On cylinder (on specified drive)</li> </ul>
323 =	Bit 10 Bit 11 Bit 12 Bit 13 Bit 14 Bit 15 STAT3 Bit 0-3 Bit 4-5 Bit 4-5 Bit 6 Bit 7 Bit 8-15	<ul> <li>Seek error (on specified drive)</li> <li>Drive fault (on specified drive)</li> <li>ECC error (on specified sector)</li> <li>ID not found (on specified sector)</li> <li>Sync time out (on specified sector)</li> <li>Defect field parity error (on specified sector)</li> <li>(Drive status)</li> <li>Sector number</li> <li>Drive number</li> <li>Command error</li> <li>Drive in channel diagnostic mode</li> <li>SMD disk bus in bits specified by tags 4 and 5 and SMD disk bus bits 0-2</li> </ul>

## **DEFINE SPECIAL ERROR LOCATIONS**

300 301	177777 000000	ERRPRC CHERCT	177777 0	<ul> <li>Sector address the error occurred in</li> <li>Channel error count</li> </ul>
302 303 304 305 306 307	000000 000000 000000 000000 000000 00000	ERROR1 ERROR2 ERROR3 ERROR4	0 0 0 0 0 0	<ul> <li>General purpose error location</li> <li>General purpose error location</li> <li>General purpose error location</li> <li>General purpose error location</li> </ul>
310 311 312 313 314 315 316 317	000000 000000 000000 000000 000000 00000	ERRCH ERRCI ERRHN ERRSP ERRSN LSTCI ERLNXT ERLNX2	0 0 0 0 0 0 0 0	<ul> <li>Current channel number after error</li> <li>Current cylinder number after error</li> <li>Current head number after error</li> <li>Current spindle number after error</li> <li>Current sector number after error</li> <li>Last cylinder number</li> <li>Next previous error location (E - 1)</li> <li>Next previous error location (E - 2)</li> </ul>
320 321 322 323 324 325 326 327	000000 000000 000000 000000 000000 00000	STAT0 STAT1 STAT2 STAT3 ADREG0 ADREG1	0 0 0 0 0 0 0 0	<ul> <li>Status register 0</li> <li>Status register 1 (general - reg. 1)</li> <li>Status register 2 (track buffer - reg. 1)</li> <li>Status register 3 (spindle - reg. 1)</li> <li>Local Memory Address register 0</li> <li>Local Memory Address register 1</li> </ul>

# USER TEST MODES UNIQUE TO TEST SECTIONS (See the individual test sections for more detail)

330 331	125252 052525	* ****** BFPT1 BFPT2	SECTION 6 125252 52525	<ul><li>(Track Buffer Memory)</li><li>Test data pattern</li><li>Test data pattern</li></ul>
332 333	000044 000001	* ****** CDSL7 FACCRA	SECTION 7 44 1	<ul> <li>(Header reads - seek timing - head address)</li> <li>Condition selector starting / ending</li> <li>Factory track headers or Cray formatted sector IDS</li> </ul>
334 335 336	000400 002000 000000	BSCIST RDCT7 DSPTRA	400 2000 0	<ul> <li>0 - Factory track headers</li> <li>1 - Cray formatted sector IDS (default)</li> <li>2 - Seek timing only (no reads)</li> <li>Base cylinder number step</li> <li>Number of random seeks in condition 4</li> <li>Display cylinder number</li> </ul>
337 340	000044 000001	* ****** CDSL10 WLKINT	SECTION 10 44 1	<ul> <li>(Connection vector analysis)</li> <li>Condition selector starting / ending</li> <li>Walking one interval (1/16)</li> </ul>

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341 342	000777 002000	UCDTPT RDCVP	777 2000	<ul> <li>Uncorrectable data pattern (default = 777)</li> <li>Random correction vector pass count (177777=infinity)</li> </ul>
343 344 345	046000 041000 000023	* ***** WTSCTM RDSCTM RDFSTM	SECTION 15 46000 41000 23	<ul> <li>(Chaining - write ahead / read ahead)</li> <li>Write sector time in RTC count (220 US)</li> <li>Read sector time in RTC count (200 US)</li> <li>First sector read time (19 MS)</li> </ul>
346 347	000015 000035	WTFLTM RDFLTM	15 35	<ul> <li>Full 48 sector write time in milliseconds (10560 US)</li> <li>Full 48 sector read time in milliseconds (9600 US)</li> </ul>
350 351	000550 000570	WTCYTM RDCYTM	550 570	<ul><li>Full cylinder write time in milliseconds</li><li>Full cylinder read time in milliseconds</li></ul>
352 353	000000 000000	* ***** DSEMD RLOUT	SECTION 16 0 0	<ul> <li>(Disk system exerciser)</li> <li>Disk sys. exer. mode (0=I.D. labels , 1=random data)</li> <li>Code rollout - see section 16 for details</li> </ul>
354 355 356 357 360 361	000013 000000 000040 000000 125252 000001	* ****** CDSL17 ACCSEL CYLSKP DATSEL OPDAPT PSS17	SECTION 17 13 0 40 0 125252 1	<ul> <li>(Seek distance / data verification)</li> <li>Condition selector starting / ending</li> <li>Cylinder access selector scratch / both</li> <li>Number of cylinders to skip within the selected range</li> <li>Data selector random / user specified</li> <li>User specified data pattern</li> <li>Number of passes to run this test section</li> </ul>
362	000000	* ***** FLAMOD	SECTION 20 0	(Flaw table generation) • Flaw table generation mode (factory / Cray)
363,	000004	* ***** FMTMDE	SECTION 21 4	<ul> <li>(Disk formatting)</li> <li>Format mode (see the formatter section for more detail)</li> <li>0 = All IDS are written - replaces flaw table</li> <li>2 = Only Cray added IDS are written, merges new flaws</li> <li>4 = ID verify only - no writes to the disk</li> </ul>
364	000001	VERIFY	1	• Format mode 0 verify Enable; 0 = disable, 1 = Enable
365 366	000001 000002	* ***** OSFLMD SECNUM	SECTION 22 1 2	<ul> <li>(O.S. flaw table generation)</li> <li>Mode of operation (seperate / combined)</li> <li>Number of sectors allowed for O.S. table</li> </ul>
367 370	000001 000001	* ***** SFAMOD PASMOD	SECTION 23 1 1	<ul> <li>(Surface analysis)</li> <li>Surface analysis mode (whole / incremental)</li> <li>Passmode 0 = multiple pass shift counts on all sectors</li> <li>1 = multiple pass shift counts on error only</li> </ul>
371	000000	HCPRND	0	• Test patterns (test patterns / random numbers)
372 373 374	000100 000040 000100	RNDPAS PASSHF SHFCNT	100 40 100	<ul> <li>Number of passes in random number mode</li> <li>Number of shifts to cinsitute one pass</li> <li>Multiple pass shift count (2 passes - 40 shifts per pass)</li> </ul>
375 376	000002 021225	PATNUM	2 21225	<ul> <li>Number of data pat. par. (to change, double or halve)</li> <li>Data Pattern</li> </ul>

.

377	014714	14714	Data pattern
400	000000	0	Spare data pattern location
401	000000	0	• Spare data pattern location
402	000000	0	• Spare data pattern location
403	000000	0	• Spare data pattern location
404	00000	0	• Spare data pattern location
405	000000	0	• Spare data pattern location

DCUS101/82



DC-40 MAINTENANCE PANEL



## DC-40 CABLE CONTROL PANEL



DC-40 CONTROL SYSTEM (SERIAL NO. 1-9)

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# DC-40 CONTROL CIRCUIT OPERATION (SERIAL NO. 1 - 9)

## Start Sequence

Start switch (S2) latches K11 which then allows 12 volt power to flow to the control circuit. S2 and K11 pull K4.

K4 pulls K6, opens the alarm circuit and opens the condensing unit fault circuit.

K6 pulls K2, K3, and K9 (K2 primary thermostat relay) (K3 back-up thermostat relay) (K9 power lost relay).

K2, K3, and K4 pull K8.

K8 pulls K15 and energizes the refrigeration solenoid and hour meter. Activation of the refrigeration solenoid causes a pressure differential in the refrigeration system which causes the condensing unit to turn on, thus pulling K14.

K14 pulls K13 (condensing unit fault relay).

K15 enables the power supplies which pull K5 and K10.

K5 and K10 pull K7.

K7 activates power on light, latches K12 (power supply fault relay) and K7 and K8 pull TD1.

TD1 holds K6 and K8 and also provides a .5 second ride through for line voltage variations.

After the system starts operation S2 can be released and K4 dropped. K4 then enables the condensing unit fault circuit and the alarm circuit.

## Fault Sequence

### Power Lost Fault

In the event of a power line sag TD1 provides a .5 second ride through to ensure system stability and prevent nuisance faults.

In the event the power loss lasts longer than .5 seconds TD1 will time out. When power is restored K6, K8, and K9 will be unable to pull, the system will remain shutdown and the power lost lamp will be lit and the alarm will sound.

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#### Condensing Unit Fault

If the current through K14 (condensing unit current sense relay) drops below the holding threshold this will cause K13 (condensing unit fault relay) to drop. K13 will pull TD2 and light the condensing unit fault lamp. After TD2 times out (one minute) K8 drops causing the system to power down and the alarm to sound.

#### *Power Supply Fault*

Failure of a power supply will drop K7. K7 then drops TD1, K12 and the power on light. K12 then lights the power supply fault lamp and sounds the alarm. After a .5 second wait K6 and K8 drop causing the system to shut down, but the alarm remains.

#### Thermostat Fault

A primary thernostat fault drops K2 which will cause TD2 to time out, the temperature fault lamp to illuminate and the alarm to sound. After one minute TD2 drops K8, the system powers down and the alarm remains.

A back-up thermostat fault will drop K3 which lights the back-up temperature light, sounds the alarm, and drops K8 which causes system power down.

#### Stop Sequence

ine,

When stop switch (S1) is pushed K11 unlatches and all 12 volt power is removed from the control circuit.

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#### REFRIGERATION SYSTEM DC40 WEEKLY CHECKOFF SHEET

Site Name	
Site S/N	
DC40 S/N	·

Return completed copy monthly to Hardware Tech Support, Chippewa Falls.

Properties of Saturated Refrigerant, R-22

Press.

		-	
Temp.	Press.		Temp.
10	33		34
17	40		41
20	43		48
23	46		57
26	50		65

	<u>,</u>		DISCH	IARGE				SUC <sup>-</sup>	TION				MISCEL	LANEO	US	
	Date Checked DD/MM/YY	Pressure	Saturation Temp.	Liquid Line Temp.	Sub- cooling	Hot Gas Temp.	Pressure	Saturation Temp.	Temp.	Super- heat	Water Temp. In	Water Temp. Out	ΔΤ	Oil Level	LL Glass	Initials
	Nominal	170-210	97-110	See Inst.	5-10'	170-215	30-60	See Inst.	50-60*	15-20'				1./2	Green	
32					·											
									)				3			

# TEMPERATURE PRESSURE CHART

Vacuum - Inches of Mercury - Italic Figures				TEN	<b>NPERA</b>	rur	EP	RES	SUI	RE	CHART	P٢	essure – Po Bold Figur	ands Per Sq es	<sub>i</sub> uare Inch G	iage	
TEMPER- ATURE		REFI	RIGER	ANT		TEMPER- ATURE		REF	RIGER	ANT		TEMPER-		REF	RIGEI	RANT	
° F.	12	22	500	502	717	۴ <b>.</b>	12	22	500	502	717	۴F.	12	22	500	502	717
-60	19.0	12.0	17.0	7.2	18.6	12	15.8	34.7	21.2	43.2	25.6	42	38.8	71.4	48.2	83.8	61.6
-55	17.3	9.2	15.0	3.8	16.6	13	16.4	35.7	21.9	44.3	26.5	43	39.8	73.0	49.4	85.4	63,1
-50	15.4	6.2	12.8	0.2	14.3	14	17.1	36.7	22.6	45.4	27.5	44	40.7	74.5	50.5	87.0	64.7
15	13.3	2.7	10.4	1.9	11.7	15	17.7	37.7	23.4	46.5	28.4	45	41.7	76.0	51.6	88.7	66.3
-40	11.0	0.5	7.6	4.1	8.7	16	18.4	38.7	24.1	47.7	29.4	46	42.6	77.6	52.8	90.4	67.9
-35	8.4	2.6	4.6	6.5	5.4	17	19.0	39.8	24.9	48.8	30.4	47	43.6	79.2	54.0	92.1	69.5
-30	5.5	4.9	1.2	9.2	1.6	18	19.7	40.8	25.7	50.0	31.4	48	44.6	80.8	55.1	93.9	71.1
-25	2.3	7.4	1.2	12.1	1.3	19	20.4	41.9	26.5	51.2	32.5	49	45.7	82.4	56.3	95.6	72.8
-20	0.6	10.1	3.2	15.3	3.6	20	21.0	43.0	27.3	52.4	33.5	50	46.7	84.0	57.6	97.4	74.5
-18	1.3	11.3	4.1	16.7	4.6	21	21.7	44.1	28.1	53.7	34.6	55	52.0	92.6	63.9	106. <b>6</b>	83.4
-16	2.0	12.5	5.0	18.1	5.6	22	22.4	45.3	28.9	54.9	35.7	60	57.7	101.6	70.6	116.4	92.9
-14	2.8	13.8	5.9	19.5	6.7	23	23.2	46.4	29.8	56.2	36.8	65	63.8	111.2	77.8	126.7	103.1
-12	3.6	15.1	6.8	21.0	7.9	24	23.9	47.6	30.6	57.5	37.9	70	70.2	121.4	85.4	137.6	114.1
-10	4.5	16.5	7.8	22.6	9.0	25	24.6	48.8	31.5	58.8	39.0	75	77.0	132.2	93.5	149.1	125.8
8	5.4	17.9	8.8	24.2	10.3	26	25.4	49.9	32.4	60.1	40.2	80	84.2	143.6	102.0	161.2	138.3
- 6	6.3	19.3	9.9	25.8	11.6	27	26.1	51.2	33.2	61.5	41.4	85	91.8	155.7	111.0	174.0	151.7
- 4	7.2	20.8	11.0	27.5	12.9	28	26.9	52.4	34.2	62.8	42.6	90	99.8	168.4	120.6	187.4	165.9
- 2	8.2	22.4	12.1	29.3	14.3	29	27.7	53.6	35.1	64.2	43.8	、,95	108.2	181.8	130.6	201.4	181.1
0	9.2	24.0	13.3	31.1	15.7	30	28.4	54.9	36.0	65.6	45.0	100	117.2	195.9	141.2	216.2	197.2
1	9.7	24.8	13.9	32.0	16.5	31	29.2	56.2	36.9	67.Ò	46.3	105	126.6	210.8	152.4	231.7	214.2
$^{2}$	10.2	25.6	14.5	32.9	17.2	32	30.1	57.5	37.9	68.4	47.6	110	136.4	226.4	164.1	247.9	232.3
3	10.7	26.4	15.1	33.9	18.0	33	30.9	58.8	38.9	69.9	48.9	115	146.8	242.7	176.5	264.9	251.5
4	11.2	27.3	15.7	34.9	18.8	34	31.7	60.1	39.9	71.3	50.2	120	157.6	259. <b>9</b>	189.4	282.7	271.7
5	11.8	28.2	16.4	35.8	19.6	35	32.6	61.5	40.9	72.8	51.6	125	169.1	277.9	203.0	301.4	293.1
6	12.3	29.1	17.0	36.8	20.4	36	33.4	62.8	41.9	74.3	52.9	130	181.0	296.8	217.2	320.8	
7	12.9	30.0	17.7	37.9	21.2	37	34.3	64.2	42.9	75.8	54.3	135	193.5	316.6	232.1	341.2	
8	13.5	30.9	18.4	38,9	22.1	38	35.2	65.6	43.9	77.4	55.7	140	206.6	337.2	247.7	362.6	
9	14.0	31.8	19.0	39.9	22.9	39	36.1	67.1	45.0	79.0	57.2	1.45	220.3	358.9	264.0	385.0	·
10	14.6	32.8	19.7	41.0	23.8	40	37.0	68.5	46.1	80.5	58.6	150	234. <b>6</b>	381.5	281.1	408.4	
11	15.2	33.7	20.4	42.1	24.7	41	37.9	70.0	47.1	82.1	60.1	155	249.5	405.1	298.9	432.9	

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NAME:				DATE:		<u></u>			
HOW	СОМРО	NENT REPL	ACEMENT			LEVEL	· · · · ·		
	COMPO C MODUL POWER I/O CAR R/W CA DRIVE DRIVE DRIVE DRIVE DRIVE DRIVE FAL FAL FAULT FAULT FAL FAN MOTOR HDA IN RELAY MOTHE REGUL	E (HDA) SUPPLY D (VJX) RD (VJX) RD (WNX) BELT OL CARD VDX AMP UCX FOR PANEL PB DISPLAY UQX REPLACEMEN TERFACE BOARD R BOARD ATOR BOARD	а <i>семент</i> Х Т						
Circle test	<i>DC-40</i> t sections use	DIAGNOSTI ed during lab.	$\begin{array}{c} C \\ 0 & 1 & 2 & 3 \\ 15 & 16 & 17 \end{array}$	4 5 6 7	10 11 12	13 14			
	FORMA SURFAC	ITER E ANALYSIS O.S. FLAW TAB	15 16 17 2	21 22 23 24	ł	······			
COMMENTS	OTHER ADD/RE READY VOLTAC RUN DIA MAINTE REFRIG CONNEG REPLAC PERFOR SCOPE S XMD VO VOLTAC CHECK WRITE A	MOVE FREON FOR SHIPPING JE MEASUREM AGNOSTICS FE ENANCE PANE ERATION ADJUCT OFFLINE TH E A MODULE I M ADJUSTME DECTOR DLTAGE MEASI JE ADJUSTMEN OUT DRIVE FR A PROGRAM U	FROM THE REF /INSTALLATIO ENT JOM CE PANEL JSTMENTS STER POWER SUPPLY NTS ON POWER UREMENT JT OM OFFLINE T SING MICRO DO	RIG. SYSTEM N SUPPLY ESTER DTS					
KEY:	A	В	С	•					
HOW	Shown or Video	Lecture or Theory	Performed				-		
LEVEL	Excellent - 5 Above Averag	Average - e - 4 Below Av	3 Unsati erage - 2 Not A	sfactory - 1 pply - N/A					
Student's Sign	nature		,,,,,,,_,_			_			
Instructor's Si	gnature					_			
If you sigr	n this sheet	t, you are re	sponsible on	site for this	task.	MF02W09A	~		

# HOW TO INSTALL AND USE THE MIX EDITOR

The following information can be used to set up your version of the MIX editor for your terminal type along with a few steps to get you started using the MIX editor.

The first thing that must be done is to have the file "SETUP.EDT" built for your terminal characteristics. If you happen to have either a Dialog-80, Dialog-150 and/or an Ampex 230 (emulating a D-150) the steps below should work. First, place the MIX diskette into one of the floppy drives and select that drive.

- 1. Type SETEDIT <cr> A menu will be displayed
- 2. Type T < cr> A new menu will be displayed on which will be several terminal types
- 3. Type 7 <cr> This will select terminal type D-80 which is the closest to correct as any others. It will return to the main menu
- 4. Type R <cr> and at the message asking for the filename type MACRO.TXT <cr> This will add the macro file to the terminal characteristics already there
- 5. Type O <cr> The letter, not the number. At the filename request type TEMP.TXT This will write the text file you have just built out to diskette.
- 6. Type E <cr> to exit SETEDIT. A message will ask if you want to create an edit file, type N <cr>

Now comes the tricky part. Go back to drive A: and

- 7. PIP TEMP.TXT to the A drive of the hard disk
- 8. With the use of some other text editor (ED or whatever), the eight line must be modified. As it stands now, it reads "CURSOR COLROW". It must be changed to read "CURSOR ROWCOL"
- 9. Now that the text file has been corrected and resaved, it must be converted to binary and renamed. To do this:
- 10. PIP TEMP.TXT back to the MIX diskette and select the floppy drive
- 11. Type SETEDIT (cr) This will get the main menu
- 12. Type R <cr> and at the filename request type TEMP.TXT It will read in the corrected text file
- 13. Type W <cr> and at the filename request type SETUP.EDT This will save it as a binary file useable by the editor
- 14. Type E < cr > To exit

Hardware Trng. DC4004/118 S.J.M. Now that you have a correct version of the terminal information on the diskette, you can begin to edit. There are three files on the diskette that need to be present on the hard disk as you edit. They are EDIT.COM, EDIT.OVY, and SETUP.EDT. You can start to edit by simply typing:

#### EDIT (filename)

If you are creating a new file there is no need for the filename.

A message will appear saying "Reading setup file...". When it is finished an EOB\* will appear, this is the end of block marker. You are now in the insert mode and ready to start typing. The keyboard is set up to be WordStar compatable; but as you learn more about this you will find it can be modified to be any way you want it.

If you are not familiar with this type of editor, on the following pages is a partial list of the command with a very brief description (kind of a ready reference) to help you get started. It is in no way complete.

To save your file and exit the editor hit the escape key and then an E. The prompt will appear requesting a filename. If the file already has a name simply hit return or else give the file a name. Then a prompt requesting a backup will appear. If you want a backup hit return. If you don't, type N and return. If you want to quit the editor without saving the file type ESCAPE followed by a Q. It will ask for a confirmation.

Again, if you have any questions or problems, contact the Diagnostics Department at (715) 723-2206. (Technical Operations Building, Chippewa Falls, WI)

Hardware Trng. DC4004/119 S.J.M.  $A^{A}$  is the control key, it should be held down while typing the other specified key(s).

A^[ is the escape key. By depressing the escape key you enter the command mode. The cursor will drop to the bottom left corner and display a < >. Command mode's full usage is explained in the book beginning on page 31.

COMMAND	DESCRIPTION	
^ <u>S</u>	Moves the cursor left one position	
^A	Moves the cursor left one word	
^QS	Moves the cursor to the beginning of the line	
^D	Moves the cursor right one position	
^F	Moves the cursor right one word	
^QD	Moves the cursor to the end of the line	
^E	Moves the cursor up one position	
^QE	Moves the cursor to the top of the page	
^R	Moves the cursor up one page	
^X	Moves the cursor down one position	
^QX	Moves the cursor to the bottom of the page	
^Č	Moves the cursor down one page	
۸W	Scrolls the screen up one line (does not move the cursor)	
^Z	Scrolls the screen down one line (does not move the cursor)	
^G	Deletes a character under the cursor	
DEL key	Deletes the character to the left of the cursor	
MT.	Deletes word	
^QY	Deletes from the cursor to the end of line	
ΛY	Deletes line	
^U	Undoes the line deleted by ^Y (can be used to move a line)	
^QT	Undoes the word deleted by ^T	
^QL	Undo whatever changes were made to this line	
^QJ	Joins the following line with this line	
۸V	Toggles insert mode on and off	
^OI	Toggles auto indent on and off	
^N	Insert one new line	
^QN #	Inserts # number of lines	
^KB	Marks the beginning of the block	
VKK KD	Marks the end of the block	
^KV or KM	Moves the block	
	Conjes the block	
^KY	Deletes the block	
^KW	Writes the block to file	
^KR	Reads the block from file	
^KL	Makes all characters in the block lower case	
^KU	Makes all characters in the block upper case	
^KP	Prints block	

Hardware Trng. DC4004/120 S.J.M.

^KO ^KI	Outputs the block to temporary file Inputs the block from temporary file
^[SS	Split screen - it will ask for row to split horizontally, if no # is specified, it will ask for column
^O	Other screen - toggles between the split screens
^I or TAB key ^B ^[DT ^[TS ^[TC ^[TB # ^[TABS = #, #, #	Tabs right four spaces Tabs left four spaces Deletes tabs Sets tab at cursor position Clears tab at cursor position Sets tabs at # intervals Sets tabs at colums #, #, and #
^[LN ^[AL	Toggles line numbers (do not become part of file) Auto line numbers that stay in file (useful for BASIC)
^KX ^KS ^KD ^KQ ^KF ^KJ ^KE	Saves the present file and exits the editor Saves the present file but continues editing it Saves the present file and creates a new file in the editor Quits with no save and stays in the editor Lists the directory specified as directory path Deletes the file specified by filename Writes lines to file filename
^QF ^L ^QA ^QV	Find string - a prompt will ask for the string to find Finds the next occurance of the previously defined string Find and replace - a prompt will ask for the string to find, then the string to replace it. When it finds a match, it will ask Replace? y/n/q. A y will replace, a n will not replace, and the search will continue until a q is typed. Will return the cursor to the position it had prior to any of these instructions

Hardware Trng. DC4004/121 S.J.M. 

# CONTROL RELAY FUNCTIONS (SERIAL NO. 1 - 9)

- K1 -Condensing unit contactor, controlled by high/low pressure switch. K2 -Pulled by K6, self-latching, controlled by primary "T" stats, 4 sets of contacts. A = Self-latch and temperature light B – Alarm circuit C = K8 pull D = TD2 pull K3 -Pulled by K6, self-latching controlled by secondary "T" stats, 4 sets of contacts. A = Self-latchB = Alarm circuitC = K8 pull and latch circuit D = Power lost light circuitMomentary, controlled by start switch and K11, 4 sets of contacts. K4 -A = TD2 pull circuit  $\dot{B} = K6$  pull C = K8 pull D = Alarm powerK5 -Pulled by "A" power supplies, 1 set of contacts in K7 pull. K6 -Pulled by K4, latched by TD1, 4 sets of contacts. A = K9 pull B = K13B pull D = K2 pull C = K3 pull
- K7-Pulled by K5 and K10, 4 sets of contacts.<br/>A = TD1 pullB = K12A pullC = K12B pullD = Power on light
- K8 Pulled by K4, K2, and K3, latched by TD1, TD2, and K3, 4 sets of contacts
   A = Pull K15, energize solenoid and H.M. B = Pull TD1 C = Pull K12B
   D = Alarm circuit
- K9 Pulled by K6, self-latching, 4 sets of contacts. A = Self-latch B = Alarm circuit C = Power lost light D = Power lost light
- K10 Pulled by "M" power supplies, 1 set of contacts in K7 pull.
- K11 Latched by start switch, unlatched by stop switch, 2 sets of contacts. A = K4 pull B = Passes power for all other circuit components
- K12 Latched by K7, unlatched by K7 and K6, 2 sets of contacts. A = Alarm circuit B = Power supply light
- K13 Latched by K14, unlatched by K8 and K14, 2 sets of contacts. A = Pull TD2 B = Condensing unit light
- K14 Latched and unlatched by flow of current to condensing unit. 1 set of contacts. A = Latch K13 B = Unlatch K13
- K15 Pulled by K8, 3 sets of contacts used to supply power to power supplies.
- TDR1 Pulled by K8 and K7, 2 sets of contacts, delay on drop. A = Holds K6 B = Part of hold for K8
- TDR2 Pulled by K2 or K13 and K4, 2 sets of contacts, delay on pull. A = Part of K8 hold B = Not used

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#### 2. DD-40 DRIVES

The DD-40 disk storage unit (sometimes called a drive) contains 4 XMD spindles (sometimes called spindles). This section provides the following information on the XMD spindles:

- A description of the XMD spindles
- The XMD switches and indicators
- XMD power-on and power-off procedures
- Drive address selection
- Drive head selection

#### 2.1 DESCRIPTION

Each XMD spindle controls reading and writing of data to 6 disks. Data is read and written across 19 heads which ride on the surface of the disks. The DD-40 drive has an internal power supply, which receives its input power from the site's main power source.

Figure 2-1 is a block diagram of an XMD spindle.

The DD-40 drives operates under direction of the DC-40 disk controller. The DC-40 communicates with the DD-40 drive by way of an interface consisting of a number of I/O lines. Some of the interface lines (e.g., those that carry commands to the drive) are not enabled if the drive is not selected by the DC-40. Unit selection enables the DC-40, which can be connected to more than one drive, to initiate and direct an operation on a specific drive.

All operations performed by the drive are related to reading and writing data. Writing and reading data is performed by heads, which are positioned over the recording surfaces of the rotating disks. There are 2 heads for each disk surface. The heads are positioned in such a way that data is written in concentric tracks around the disk surfaces. Before any read or write operation can be performed, the DC-40 must instruct the drive to position the heads over the desired tracks (called seeking) and use the head located over the surface where the operation

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### 2-1. XMD Block Diagram

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Figure 2-2. XMD Drive Head/Disk Relationship

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will be performed (called head selection). An XMD spindle has 19 data heads and one servo head. Figure 2-2 shows the relationship of the heads to the disks for an XMD spindle.

After selecting a head and arriving at the correct data track, the portion of the track where the data will be written or read must be located. This is called track orientation and is done by using the Index and Sector signals generated by the spindle. The Index signal indicates the logical beginning of each track. The Sector signal indicates the position of the head on the track with respect to the index.

When the desired location is reached, the DC-40 commands the spindle to read or write data. During a read operation, the spindle recovers data from the disks and transmits it to the controller. During a write operation, the spindle receives data from the controller, processes it, and writes it on the disks.

The spindle is capable of recognizing fault conditions that may occur during its operation. When a fault condition is detected, it is indicated by a fault signal to the DC-40 and by a maintenance indicator on the XMD spindle itself.

Table 2-1 lists the specifications of the XMD spindles.

Characteristic	Specification		
Size Height Width Length Weight Interface SMD-O/SMD-E	26.4 cm (10.3 in) 48.0 cm (18.9 in) 76.5 cm (30.1 in) 80.1 kg (176 lbs)		
Recording Total Capacity (unformatted) PA1A4/1A5 ⊀№9 & PA1A6/1A7 ¥№9 & Bytes per track	858 Mbytes 1359 Mbytes 50,400 bytes		

Table 2-1. XMD Spindle Specifications.

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Characteristic	Specification		
Number of disks: 850 Mbytes Xm9 L 1350 Mbytes Xm0 3	5 6		
Movable data heads: 850 Mbytes xm0 2 1350 Mbytes xm03	16 19		
Servo heads	1		
Tracks per inch: 850 Mbytes こ 1350 Mbytes ろ	960 1280		
Physical heads per surface	2		
Logical cylinders per head/disk assembly: 850 Mbytes 2- 1350 Mbytes 3	1064 (0 through 1063) 1420 (0 through 1419)		
Transfer rate			
Disk speed at 3600 rpm	24.2 MHz (3,025,000 bytes/s)		
Latency			
Average	8.33 ms (disk rotation speed at 3600 rpm)		
Maximum	17.3 ms (disk rotation speed at 3474 rpm)		
Recording			
Mode	2 through 7 code		
Density	15,400 bpi (inner track)		
Seek Time			
Full	30 ms		
	8		

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CRAY PROPRIETARY THIS IS A PRELIMINARY DRAFT COPY Table 2-1. XMD Spindle Specifications (continued)

Characteristic	Specification			
Average	16 ms			
Single track	5 ms maximum			
Start Time	3 minutes 30 seconds maximum (not including power sequence delay determined by unit address in string)			
Stop time				
Start switch OFF	30 seconds maximum			
Power loss	30 seconds maximum			

#### 2.2 XMD SPINDLE SWITCHES AND INDICATORS

Table 2-2 lists the XMD spindle switches and indicators. Figure 2-3 shows where the switches and indicators are located on an XMD spindle.

Table 2-2. XMD Spindle Switches and Indicators Functions

Switch/Indicator	Function
CB1 (ON/OFF) circuit breaker	POWER SUPPLY REAR PANEL Applies site AC power to the fan and the internal power supply, which supplies the DC operating voltages to the spindle electronics.

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2-б

Function
The $\pm 5$ V supplies are protected by current limiting circuitry in the power supply.
Protects the voice coil in the module from overheating caused by failure of the power amplifier board.
FRONT PANEL
The logic plug activates switches that establish the logical address of the device. A logic plug, numbered 0, is included with each unit, and logic plugs, numbered 1 through 15, are available as options. The unit selected indicator is lit if the spindle is selected.
The START switch has alternate action, in for start and out for stop, and it contains the ready indicator. Pressing the START switch to the start position activates the power-up sequence, and the ready indicator flashes until the disks are up to speed, the heads are loaded, a stabilization period has elapsed, and there are no fault conditions. The ready indicator is on steady with power up complete. Pressing the START switch to release it from the start position causes the ready indicator to flash for 30 seconds.
The FAULT indicator is inside the fault clear switch, and it lights if a fault exists within the spindle. It is turned off by any of the following (provided that the error condition or conditions no longer exist):

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Table 2-2. XMD Spindle Switches and Indicators Functions (continued).

Switch/Indicator	Function
WRITE PROTECT switch/ indicator	<ul> <li>Pressing the fault clear switch</li> <li>Fault clear command from the controller</li> <li>Reapplying ac power to the spindle</li> <li>The operation of the WRITE PROTECT switch, or installing the write protect plug on the control board, places the spindle in the write protected mode (preventing write operations) and lights the WRITE PROTECT indicator.</li> <li>CONTROL BOARD</li> </ul>
Sector select switches	Allows the disk to be divided into segments or sectors. The switch settings determine the number of sectors per track.
FAU	ILT/STATUS DISPLAY BOARD
First seek indicator	Indicates that the spindle failed the first seek/load attempt.
R/W●OC indicator	Indicates a read or write condition occurred during a seek operation (an off-cylinder condition).
WRT indicator	Indicates that a write fault occurred.
RD•WRT indicator	Indicates that a read and a write command existed simultaneously.
VOLT indicator	Indicates a below normal voltage existed.
HD SEL indicator	Indicates a multiple head selected fault has occurred.
Diagnostic mode indicator	Indicates that the spindle is in diagnostic mode (green LED).

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Switch/Indicator	Function
Diagnostic mode switch	Places the spindle in diagnostic mode and disables the I/O.
Diagnostic execute switch	Starts and stops diagnostic tests.
Diagnostic step switch	Selects individual diagnostic tests.
Diagnostic/servo fault display	When a spindle is in diagnostic mode, the display indicates which diagnostic test is being initiated. If a failure occurs, the status code display indicates which major assembly or assemblies are the most likely cause of the problem. When a spindle is not in diagnostic mode, the display indicates error status code generated by the microprocessor. I/O BOARD
DEVICE ID switches	Provide a device type status code. Switch settings determine a device ID code that conforms to individual customer requirements.
I/O OPTIONS switches	Allow selection of specific I/O options. Switch settings determine which options are enabled.

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2 PROTECTS VOICE COIL IN MODULE.

Figure 2-3. XMD Spindle Switches and Indicators (Sheet 1 of 2)

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Figure 2-3. XMD Spindle Switches and Indicators (Sheet 2 of 2)

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#### I/O BOARD SWITCH SETTINGS

On the NO board, there are two sets of switches. The set of switches at location E103 is for setting a device I.D. but is unused for drives in the DD40. The other set of switches located at C503 is used to select the I/O options. The following table gives the switch numbers (1-10) along with the switch I.D., the position of each switch and a description of the option used in the DD40. All switches are in the "OFF" position except switch number 8 which is "ON" to select the extended cylinder addressing.

Switch Number	Switch I.D.	Description of I/O Options used in the DD40		
1	1A	OFF - Index & Sector in Channel 1,		
2	1B	OFF - Index & Sector in Channel 1,		
3	2A	OFF - Index & Sector in Channel 2,		
4	2B	OFF - Index & Sector in Channel 2,		
5	1D	OFF - Channel 1 Enabled		
6	2D	OFF - Channel 2 Enabled		
. 7	SO	OFF - Extended SMD Mode		
8	XA	ON - Extended Cylinder Addressing		
9	AR	OFF - Absolute Reserve Mode		
10	RL	OFF - Remote Power Up		

# SWITCH SETTINGS FOR I/O OPTIONS



2-11A

### SECTOR SWITCHES

The sector switches are located on the control board and are set to predetermined value to provide 12 sectors per revolution. The following table shows the location of the two switch packages on the control board, F556 and F563. It also gives the desired number of sectors in the left most column followed by the setting for each of the individual switches. Each switch is represented by either a C for closed or an O for open.

The switches preset a byte counter. The counter is incremented by each servo byte until it reaches a value of 4095 when it is preset again. Each servo byte is equal to 2.25 data bytes. The switches are shown in the following figure. Bit  $2^0$  is the left most switch and bit  $2^{11}$  is the right most switch.

Number of Sectors		· L Sv	ocati witch	on Fi 1 Nun	556 nber				Loc Swit	atior ch N	F56. Iumbe	3 er	
	1	2	3	4	5	6		1	2	3	4	5	6
6	0	0	С	0	С	0		0	С	0	С	С	С
7	С	С	С	С	С	С		С	0	0	0	С	C
8	С	С	С	С	0	С		С	С	0	С	0	С
9	С	С	С	0	С	С		0	С	С	0	0	С
10	С	С	С	С	С	С		0	С	0	0	0	С
11	С	С	0	0	С	С		С	С	С	С	С	0
12	С	0	0	С	0	0		С	0	С	С	С	0
13	0	С	0	С	С	С	ĺ	0	С	0	С	С	0
14	С	С	С	С	С	С		0	0	0	С	С	0
15	0	0	С	0	С	0		С	С	C	0	С	0

### SECTOR SELECT SWITCH SETTINGS



SECTOR SWITCHES

#### POWER ON INITIALIZATION

The power on initialization is the process the drive goes through from the time power is applied until the drive is waiting for start conditions.

For power on initialization to occur, both CB1 and CB2 must be on to provide AC and DC power to the drive. Until the +5V reaches 4.9V, the drive Master clear signal is active which resets the sector count and disables the Interface Card.

When drive power reaches its desired level there is a 3 ms. delay, after which the MPU starts three self tests. These tests are:

-A check of the MPU firmware instructions.

-Writing to and reading from the RAM.

-The MPU sends data to the peripheral interface adapters (PIA) and reads it back to initialize them.

If one of the first two tests fail, the MPU stops and turns on all fault LEDs on Fault panel. If the third test fails, the MPU attempts to turn on the First Seek LED. Any fault on the power on initialization must be cleared by a power cycle.

After the self tests have been successfully completed, the Master Clear becomes inactive and the MPU clears the cylinder address register, head address register, on-cylinder FF, and the fault latches. The MPU now waits for the start conditions before starting the load operation.

Figure 2-5 shows the power on circuitry and Figure 2-6 shows the power on initialization flowchart. Both figures can be used as an aid in troubleshooting problems that occur during a power on initialization.

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2-11C



Power On Initialization Flowchart

.2-11D



Power On Circuitry

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2-11E

#### 2.3 XMD POWER-ON AND POWER-OFF PROCEDURES

The power supply circuit breaker (CB1) on the power supply rear panel is usually left on, so that dc power is available to the drive.

The following procedure describes how to power-up the DD-40.

- 1. Press the START switch. If the LOCAL/REMOTE switch was set in the REMOTE position during drive installation, the power up sequence continues when power sequence ground is available from the controller. If the LOCAL/REMOTE switch was set in the LOCAL position, the power-up sequence begins immediately. When set to the REMOTE position, the power-up sequence of each spindle (except spindle 0) is delayed. The length of the delay is determined by the number of the unit logic plug used in increments of  $\frac{1}{2}$  seconds. Devy  $= 10 \text{ Sec} \times 0^{-11} e^{100}$
- 2. Observe that the ready indicator (located in the START switch) flashes, indicating that power-up is in progress.
- 3. Observe that the ready indicator lights steadily within 3 minutes and 30 seconds, indicating that the disks are up to speed, the heads are loaded, and a stabilization period has elapsed.
- 4. Ensure that the FAULT indicator is off.

The power-up sequence is now complete, and the drive is ready to write data.

The following procedure describes how to power-down the DD-40.

- 1. Press the START switch to release it from the start position.
- 2. Observe that the ready indicator (located in the START switch) flashes, indicating that power-up is in progress.
- Observe that the READY indicator goes off after approximately 30 seconds.

When power-down is complete, the heads are positioned in the landing zone and the disks are not rotating. Normally, the power supply circuit breaker (CB1) is left on to continue supplying power to the drive.

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#### LOAD OPERATION

When the power on initialization is complete, the MPU checks the Over Temperature on the Power Amp board to make sure it is inactive and waits for the start conditions. The MPU will wait for the start switch to be depressed. When this happens, provided the remote/local switch is in the remote position and that the DD40 has its A cables connected to the DC40 to provide the correct signal on the sequence Pick and Hold lines, the MPU will start the load operation. Once these conditions are met, a delay is started. This delay is:

Unit Address X 10 sec = Delay (in Seconds)

When the delay ends the MPU unlocks the actuator, pulls the heads against the carriage stop, and the motor starts to spin. The Ready light on the operator's panel will start to flash. The MPU checks for the signal Speed OK within three to seven seconds. If Speed OK is not detected in three attempts, the MPU will stop trying and wait for CB1 to be turned off and back on again to allow another three attempts.

When Speed OK is detected by the MPU, it checks and rechecks the speed until the drive is spinning at the rated speed. This is done by counting Speed pulses.

The MPU enables the Power Amplifier, checks for any faults, and starts a 200 ms. timer. The MPU starts pulsing the voice coil to move the actuator inward. This continues until a servo signal is detected. The actuator is now moving inward. After 40 ms. the MPU checks for 32 cylinder crossing pulses. When the 32 pulses are detected, the MPU checks that the 200 ms. timer has not timed out. At this point, heads are over the data area. The actuator direction is reversed and starts moving outward under coarse control. The actuator moves in the outward direction until the outer guardband is detected. Once the outer guardband is detected the MPU checks for two cylinder pulses. The actuator is turned around and moves toward Cylinder 0. The MPU must detect at least one cyclinder pulse for the outer guardband. There is one additional cylinder pulse detected before the heads reach Cylinder 0. With one third track to go, fine control is enabled and coarse control is disabled.

The MPU checks that on-cylinder stays active for 2.1 ms. If it does not, the MPU will wait for up to 11 ms. for on-cylinder to go active and check it again. When on-cylinder stays active for 2.1 ms. and the servo signal is still present and three or more cylinder crossing pulses were not detected after on-cylinder, the MPU starts the scan cycle.

The scan cycle consists of two cycles of single track seeks from Cylinder 0 to 1419 and back to 0. (See Figure 2-7). The scan cycle is followed by the velocity calibration cycle which executes a series of 128 track seeks to calibrate the velocity measurement circuit.

At the end of the load operation, the heads are positioned to Cylinder 0. A successful load operation will take 3 minutes and 30 seconds. A successful load operation is indicated by a steady unit ready light and unit ready and seek end being sent to the controller. The DD40 is ready to receive commands from the DC40.

During the load operation, the MPU periodically checks the fault line to make sure there is no fault present. It also checks for other conditions that must be present to allow the load operation to continue. The following is a list that will cause a first seek fault.

-A fault is detected during the load operation.

-The servo signal is present before the actuator starts to move forward.

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-It takes longer that 200 ms. to detect 32 cylinder pulses.

-The servo signal is lost during the reverse motion of the actuator.

-At least one cylinder pulse of the outer guardband was not detected before Cylinder 0 was found.

-Three or more cylinder pulses are detected after Cylinder 0 has been detected.

-When Cylinder 0 has been detected and on-cylinder is active, if on-cylinder goes inactive before 2.1 ms. and does not return to the active state in 11ms.

Any of the above occurances will cause the MPU to set fault first seek fault, retract and lock the actuator, and send servo status to the fault display board. When the fault is cleared, the MPU will attempt another load operation.

The Load Operation Flowchart gives a step by step flow of this operation. The Load Trajectory shows the movement of the actuator during the load operation.



Load Operation Flowchart (Sheet 1 of 4)

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2-12C



Load Operation Flowchart (Sheet 2)

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Load Operation Flowchart (Sheet 3)



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Load Operation Flowchart (Sheet 4)

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The Load Seek Trajectory summarizes what happens during the load operation. It also shows the movement of the heads with respect to the guardbands and the data zones.



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#### I/O SIGNALS

The I/O signals for the A cable are shown on page 2-10N, I/O Signal Processing (Sheet 1 of 2). The signals on the A cable are listed in the table on page 2-10O and a brief discription is given on the page 2-10P. The I/O signals for the B cable are shown on page 2-10Q. Sheet 2 of I/O Signal Processing figure. The signals for the B cable are listed on page 2-10R. A brief description of the B cable signals is given on page 2-10S.

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2-12H



I/O Signal Processing (Sheet 1 of 2)

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# I/O BOARD - VJX

# A CABLE - J03/J04

SIGNAL

# DC40 - I/O

## XMD - LO/HI

Unit Salast Tag	DU JEI	22/52
Unit Select Tag		22/52
Unit Select bit 1		23/33
Unit Select bit 1		24/34
	R3 - 2EJ	20/30
	K4 - ZEJ	1/31
lag 2	K5 - ZEJ	2/32
lag 3	R6 - ZEJ	3/33
Tag 4	R7 - 2EJ	30/60
Tag 5	R8 - 2EJ	27/57
Bus 0	R9 - 2EJ	4/34
Bus 1	R10 - 2EJ	5/35
Bus 2	R11 - 2EJ	6/36
Bus 3	R12 - 2EJ	7/37
Bus 4	R13 - 2EJ	8/38
Bus 5	R14 - 2EJ	9/39
Bus 6	R15 - 2EJ	10/40
Bus 7	R16 - 2EJ	11/41
Bus 8	R17 - 2EJ	12/42
Bus 9	R18 - 2EJ	13/43
Status 0	118, 126, 134, 142 - 2EM	19/49
Status 1	119, 127, 135, 143 - 2EM	17/47
Status 2	120, 128, 136, 144 - 2EM	16/46
Status 3	I21, I29, I37, I45 - 2EM	15/45
Status 4	122, 130, 138, 146 - 2EM	28/58
Status 5	I23, I31, I39, I47 - 2EM	20/50
Status 6	124, 132, 140, 148 - 2EM	18/48
Status 7	125, 133, 141, 149 - 2EM	25/45
Open Cable Detect	R34 - 2EJ	14/44
Busy	N/U	21/51
Spindle Sequence Pick	Controller GND	29
Spindle Sequence Hold	Controller GND	59

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2-12J

XMD A Cable Signals	
<u>Signal</u>	Description
Unit Select Tag	This signal is sent to the drive along with the Unit Select Bits 0-2 to select the desired unit.
Unit Select Bits 0-2	These signals must be active at least 200 ns before the Unit Select Tag becomes active. Only Unit Select bit 0 is used by the DC40 to select either the Primary $(2^0 = 0)$ or Shadow $(2^0 = 1)$ DD40. (Unit Select Bit 3 is used on Tag 5.)
Tag 1	Lower cylinder select, bits $2^{0}-2^{9}$ . (When doing a cylinder select the higher bits must be sent first.)
Tag 2	Head Select/Higher Cylinder Bits. Head select bits are represented in Bus Out Bits 2 <sup>0</sup> -2 <sup>4</sup> . The upper cylinder bits (2 <sup>10</sup> and 2 <sup>11</sup> ) are represented by Bus Out Bits 2 <sup>7</sup> and 2 <sup>8</sup> . (The upper cylinder bits must be sent before the lower cylinder bits.)
Tag 3	Enable the Control bits to be sent out on the bus. When the Bus Out Bit is active it controls the following in the XMD. $2^0$ - Write Gate $2^1$ - Read Gate $2^2$ - Offset + Offsets positioner toward the spindle for 2.75 ns. $2^3$ - Offset - Offsets positioner away from the spindle for 2.75 ns. $2^4$ - Clear Fault $2^5$ - Not used $2^6$ - RTZ $2^7$ - Data Strobe Early $2^8$ - Data Strobes Late $2^9$ - Not Used
Tag 4 and 5	Selected Status
(See individual status words for bit by bit discription in Troubleshooting section of this manual.)	Tag 4 - Sector Status Tag 5 - Extended Status BOBO=0 BOB1=0 Tag 5 - Operating Status B0B0=1 BOB1=0 Tag 5 - Diagnostic Status B0B0=0 BOB1-1 Tag 5 - Diagnostic Execute Status B0B0=1 BOB1=1
Open Call Detect	Detects loss of power in DC40
Pich	DC40 Ground
Hold	DC40 Ground
Bus In Bits 0-7	Drive Status or Selected Status
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I/O Signal Processing (Sheet 2)

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# I/O BOARD - VJX

# B CABLE - J02

SIGNAL	PRIMARY DC40 - I/O	XMD - LO/HI
Write Data Ground	R4, R12, R20, R28 - 2EK	8/20 7
Write Clock Ground	R5, R13, R21, R29 - 2EK	6/19 18
Servo Clock Ground	16, 122, 132, 142 - 2EK	2/14 1
Read Data Ground	I5 - 2EJ	3/16 15
Read Clock Ground	16 - 2EJ	5/17 4
Seek End Ground	I10 - 2EJ	10/23 11
Unit Selected Ground	I9 - 2EJ	22/9 21
Index Ground	I7 - 2EJ	12/24 25
Sector	I8 - 2EJ	13/26

## SIGNAL

## SHADOW DC40 - I/O

Write Data	R4, R12, R20, R28 - 2EK	8/20
Write Clock	R5, R13, R21, R29 - 2EK	6/19
Servo Clock	17, 123, 133, 143 - 2EK	2/14
Read Data	I11 - 2EJ	3/16
Read Clock	I12 - 2EJ	5/17
Seek End	I16 - 2EJ	10/23
Unit Selected	I15 - 2EJ	22/9
Index	113 - 2EJ	12/24
Sector	I14 - 2EJ	13/26

2-12M ·

XMD B Cable Signals

The B cable signal for spindle A and B share one 55 pin cable between the DC40 and DD40. The B cable signals for spindle C and D are shared by another cable.

Signal	Description
Write Data	NRZ Data to XMD
Write Clock	24 MHz/41.3ns
Servo Clock	24.192 MHz/41.3ns
Read Data	NRZ Data from XMD
Read Clock	24 MHz/41.3ns
Seek End	Seek End with On cylinder indicates the seek was completed as expected. Seek End without On cylinder indicates a Seek Error. When a Diagnostic Execute Status is performed, Seek End indicates test execution is complete.
Unit Selected	This is the response to a Unit Select Tag and a match between the Unit Select Bits and Drive Address.
Index	Decoded from servo tracks once per resolution.
Sector	12 Sector pulses per revolution. This is determined by the setting on the sector switches.

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2-12N

#### 2.4 DD-40 ADDRESS SELECTION

The XMD spindles within the DD-40 cabinet are not individually addressable from the IOP. A spindle is selected with 3 bits of the unit select bus. The logic plug supplied with the DD-40 is inserted in the top of the operator panel. When inserted, it activates switches that establish the logical address of the DD-40. The logic plug also determines the delay before startup.

In each DD-40 cabinet, three of the four spindles are given the same number. The bottom spindle is one number higher than the other three if the DD-40 is the primary DD-40 and one number lower if it is the shadow DD-40. The top three spindles in the shadow DD-40 are one number higher than the same three spindles in the primary DD-40. Figure 2-4 shows how the addresses of the XMD spindles are specified.

The DD-40's connected to DC-40 disk controller unit 0 use numbers 0 and 1 and the DD-40's connected to disk controller unit 1 use numbers 2 and 3, and so on.

When the primary DD-40 is selected, the unit select command is issued with the lower 3 bits of the accumulator equal to 0's. The unit select tag and the lower 3 bits of the accumulator are sent to the DD-40 from the disk controller unit. Some of the bits are inverted in the drop cables to make the 3 unit select bits match the unit number when they reach the DD-40. When the shadow unit is selected,  $2^0$  is set in the accumulator. When the logical address of the DD-40 matches the address that is sent by the disk controller, the select compare signal is enabled if open cable detect signal is active. The select compare signal enables the transmitter and receivers. Select compare is also the unit selected signal returned to the DC-40.

When the DD-40 cabinet circuit breaker is turned on, the top three spindles of the primary DD-40 start to spin up first and the bottom spindle starts spinning 10 seconds later. For the shadow DD-40, the bottom spindle starts spinning first and the top three spindles 10 seconds later. The startup delay is the unit number times 10 seconds.

#### 2.5 XMD SPINDLE HEAD SELECTION

The XMD spindle has 19 data heads and 1 servo head. There are 2 heads on a disk surface and 4 heads on a head/arm assembly. The heads must be positioned at the cylinder from which the data is to be read or written before a head can be selected. Only one data head can be selected at a time. Figure 2-5 shows the head select circuits of the XMD-III spindle.

The cylinder address and head address are held in registers in the bus out decode gate array. The spindle's Micro Processor Unit (MPU) uses a series of pulses on I/O control lines 1 and 2 to transfer the cylinder address to the MPU. The MPU sends another series of pulses on I/O control lines 1 and 2 that cause the bus-out gate array to output the head address. Until the spindle is commanded to do another seek, the head address is held on the head/cylinder address lines. The head/cylinder lines go to the read/write board when they address a ROM, which outputs the correct signals on arm select lines 1 through 5.

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From DCU-5/DC





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Figure 2-5. XMD Head Select Circuits

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If a head address greater than 18 is received, no head is selected. If a write is attempted with no head selected, a write fault occurs.

Table 2-3 lists the head select addressing for the XMD spindles.

Head (decimal)	Head (hex)	Arm	He O	ad/Cyli 1	nder Ad 2	ldress I 3	Lines 4
· · · · ·					· · · ·		
0	0	1	0	0	0	0	0
1	1	1	1	0	0	0	0
2	2	1	0	1	0	0	0
. 3	3	1	1	1	0	0	0
4	4	2	0	0	1	0	0
5	5	2	1	0	1	0	0
6	6	2	0	1	1	0	0
7	7	2	1	1	1	0	0
8	8	3	0	0	0	1	0
9	9	3	1	0	0	1	0
10	A	3	0	1	0	1	0
11	В	3	1	1	0	1	0
12	С	4	0	0	1	1	0
13	D	4	1	0	1	1	0
14	Е	4	0	1	1	1	0
15	F	4	1	1	1	1	0
16	10	5	0	0	0	0	1
17	11	5	1	0	0	0	1
18	12	5	0	1	0	0	1

# Table 2-3. XMD Spindle Head Select Addressing

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# NORMAL SEEK

When the DD40 is ready and selected the controller can send it a command to do a seek. The controller sends the cylinder address to the DD40 in two parts. First, the drive receives the upper two cylinder address bits as bus out bits  $2^7 \& 2^8$  along with the head address and Tag 2. The lower ten cylinder address bits are sent next, along with Tag 1. The maximum cylinder address is 1419. On-cylinder goes low and the MPU is interrupted via PIA-1.

The MPU pulses the Bus Out Decode array and it transfers the cylinder address 4 bits at a time to the MPU RAM where it is stored. After the cylinder address is stored, the head address is ready from the Bus Out Decode array. (See Head Selection). The MPU compares the new cylinder address to the present cylinder address to determine two things, the direction of the seek, and the distance of the seek in tracks.

Before the MPU starts the seek it checks that there is no fault, the servo signal is being detected and the speed is O.K. If no errors are detected, the MPU starts a 60 ms. timer and starts the seek.

If it is a one track seek, the MPU sets T=1 and  $T\leq 8$  and starts to move the actuator. The actuator accelerates until it reaches the maximum speed for a one track seek. The actuator will coast for a period then decelerate and eventually settle on the cylinder under fine control.

If it is a seek of two or more tracks, the actuator starts moving and the MPU loads the tracks to go into a counter. The actuator continues to accelerate. Each time the servo head crosses a cylinder, a pulse is generated which decrements the counter. The actual speed of the actuator is compared to the expected speed, which is held in a table in the ROM to see if the actuator has reached the desired speed. This will be repeated until the actual speed exceeds the expected speed. When this happens, the counter for tracks to go is checked to see if it is less than 256 tracks to go. If the counter is less than 256 tracks, the actuator begins to decelerate. If the counter is at 256 or more tracks the actuator continues at a constant velocity until the tracks to go is less than 256.

When the tracks to go is less than 256, the actuator begins to decelerate. The MPU starts to compare the actual speed to the next lower desired speed in the ROM table. When the tracks to go are less than or equal to 40, the actuator decelerates again. The MPU begins to compare to the next lower desired speed until the tracks to go are less than or equal to 8. When the last cylinder pulse is detected, the MPU sets T=1 and with 1/3 track to, go the MPU enables the fine control.

After a delay, the servo enters track follow mode. On-cylinder will become active and the MPU will check on-cylinder until it remains active for 2.1 ms. If on-cylinder does not stay active for 2.1 ms., it must return to the active state within 11 ms. so the MPU can check it again. This cycle will repeat until either the on-cylinder signal stays active for 2.1 ms. or the 11 ms. timer expires before on-cylinder returns to the active state.

If the seek was successful, the drive will send seek end to the controller.

At the beginning of the seek, the MPU checks the fault signal, the servo signal, and the speed O.K. signal to make sure that it is safe to proceed with the seek operation. At the end of the seek, the MPU checks the servo signal, that no guardband is being detected and that the seek was completed within 60 ms. The 11 ms. timer cannot expire before on-cylinder returns to the active state. If the MPU detects an error in any of the above conditions, it drops all servo commands, stops the actuator, sends seek error to the controller, and waits for a return to zero command from the controller.

When the actuator reaches the maximum speed for any given seek, the MPU will check the deceleration time and adjust the velocity gain if necessary.



Normal Seek Flowchart (Sheet 1 of 5)

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Normal Seek Flowchart (Sheet 2)

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Normal Seek Flowchart (Sheet 3)

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Normal Seek Flowchart (Sheet 4)

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Normal Seek Flowchart (Sheet 5)

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# **RETURN TO ZERO SEEK**

During a normal seek operation, if a seek error occurs the only method of clearing it is to issue a return to zero command from the controller. (A seek error does not set the fault signal and therefore cannot be cleared by depressing the fault switch.) To do this the controller sets bit six true on the bus out and sends Tag 3 to the interface board.

When the bus out decode gate array on the interface board decode the return to zero it clears the cylinder register, the head register, on-cylinder FF and the seek error FF, all contained in the bus out gate array. The MPU receives a return to zero interrupt from the bus out gate array.

The return to zero interrupt will cause the MPU to stop the actuator motion and start moving it in an outward direction under coarse control. The acutator continues to move outward until the outer guardband is detected. Once the outer guardband is detected, the MPU checks for two cylinder pulses before reversing the direction of the actuator. The actuator begins to move toward Cylinder 0. The MPU must see at least one cylinder pulse for the outer guardband. There is one additional cylinder pulse detected before the heads reach Cylinder 0. With one third track to go fine control is enabled and course control is disabled.

The MPU checks that on-cylinder stays active for 2.1 ms. If it does not, the MPU will wait for up to 11 ms. for on-cylinder to go active and check it again. When on-cylinder stays active for 2.1 ms., the MPU checks other conditions that would indicate an error occurred before proceeding. These conditions are that there were not three or more cylinder pulses detected after on-cylinder was detected, that the servo signal is present and that no guardband is being detected. The MPU will continue if no error condition is found.

If the return to zero seek was completed in less than 60 ms. the MPU performs a velocity gain calibration. The ready light will be on steady and seek end and drive ready will be sent to the controller. The DD40 is now ready to receive commands from the DC40.

During the return to zero seek the MPU periodically checks condition that will determine if the operation should be continued. The following list shows the conditions that will cause the return to zero operation to be stopped.

-A fault is detected at the beginning of the return to zero.

-The servo signal is not present at the beginning of the return to zero.

- -The servo signal is lost after the outer guardband is detected.
- -One or more cylinder pulses from the outer guardband was not detected before Cylinder 0 was found.
- -Three or more cylinder pulses are detected after Cylinder 0 has been detected.
- -When Cylinder 0 has been detected and on-cylinder is active, if on-cylinder goes inactive before 2.1 ms. and does not return to the active status in 11 ms.

Any of the above occurances will cause the MPU to set the fault light, flash the ready light, send servo status code to the fault display board and send seek error to the controller. The operating status select can be used by the controller to read the servo status code.

The return to zero flowchart gives a step by step flow of this operation.

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Return to Zero (RTZ) Seek (Sheet 1 of 2)

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Return to Zero (RTZ) Seek (Sheet 2)

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#### 2.6 WRITE CIRCUIT

Figure 2-6 is a block diagram of the write circuit. This circuit has four main parts: the write PLO, the 2 through 7 encoder, write compensation, and arm preamp. The write operation begins when the DC-40 controller sends tag 3 and bus-out bit 0 is true. The NRZ data starts coming from the controller at this time, synchronized by the 24.2 MHz clock. The servo clock is sent to the DC-40 controller and returned to the spindle as the write clock.

The write PLO generates the following:

- 24.2 MHz servo clock, which is sent to the controller by way of the I/O board.
- 12.096 MHz clock used in the read comparator
- 48.8 MHz 2F clock used in the 2 through 7 data encoder. The 2F clock is also used as an input to the frequency dividing circuit.

The 4.032 output from the divider is used for comparison with the 4.032 MHz reference frequency 4.032 MHz). This comparison keeps the 48.4 MHz 2F clock stable.

The encoder gate array changes NRZ data to 2 through 7 data. Table 2-4 shows the relationship between NRZ and 2 through 7 code words.

NRZ Code Words	2 Through 7 Code Words
00	1000
01	0100
100	001000
101	100100
111	000100
1100	00001000
1101	00100100

Table 2-4. Relationship Between NRZ and 2 Through 7 Codes

The NRZ data is broken down into seven NRZ code words. For each NRZ code word, there is a there is a corresponding 2 through 7 code word. The 2 through 7 encoder receives from the I/O board the following signals: write clock, write gate and write data. The encoder chip looks for one of the seven NRZ words. When a word is recognized, the 2 through 7 equivalent word is sent to the write compensate circuit. In the write compensate circuit, 2 through 7 data goes through a pulse shaping circuit, a shift register, and a patten decode. The purpose of this circuit is to compensate for peak shift in the data on the drive. The part of the circuit that compensates for peak shift is divided into two parts. One part is for tracks less than 768 (outer zone tracks) and one part is for tracks greater than 768 (inner zone tracks). The data is sent out on one of the four data lines early, late, normal, or block

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R/W CARD



# Figure 2-6. Write Circuit Block Diagram

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shift. The write enable signal is used as an enable for the write toggle flip-flop (F/F). As a bit arrives on a data input line, the write toggle F/F toggles. If the F/F starts at 0, the first 1 bit sets it, the next clears it, and so on. From the write toggle F/F the data goes to the selected preamp inside the module and to the selected head.

The write enable allows the operation to continue as long as 1) write protect is off, 2) there are no faults, 3) the drive is at the correct speed, 4) the power amp is enables, and 5) the write gate is on.

#### 2.7 READ CIRCUIT

Figure 2-7 is a block diagram of the read circuit. Data is read by the selected head and sent to the read buffer amplifier by way of the preamp. The data is split into low resolution data and high resolution data. Each kind of data is sent through a waveshaping network. When the data is changed from analog to digital data, it enters the data latch chip, which reduces the high frequency noise. From the data latch, the 2 through 7 data is sent to the read comparator and the PLO circuit, where the data is synchronized to the 48.4 MHz clock.

The data is sent to the 2 through 7 decode gate array, which looks for one of the 2 through 7 data words and sends out the corresponding NRZ data word. The NRZ data is synchronized to the 24.2 MHz read clock and sent to the controller by way of the I/O board.

#### 2.8 FAULT AND ERROR CIRCUITS

Figure 2-8 shows the fault and error detection circuitry. There are two kinds of errors: those erros that are indicated by a fault and those that are not. When a fault is indicated, the XMD spindle sends the DC-40 controller fault and write protected. The MPU drops the ready signal and tries to identify the fault. The MPU reads the seven fault latches from the bus-out decode gate array and lights the corresponding LED on the fault display board.

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Figure 2-7. Read Circuit Block Diagram

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Figure 2-8. Fault and Error Detection Circuitry (page 1 of 2)

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Figure 2-8. Fault and Error Detection Circuitry (page 2 of 2)

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The fault light indicates the following faults:

- Voltage fault
- Read or write and off cylinder
- Write fault
- Head select fault
- Read and write fault
- Write and write protected fault\*
- First seek fault
  - \* This signal does not have a corresponding LED on the fault display board.

There are two error conditions that do not cause a fault: motor speed error (less than 2100 RPM) and seek error (cleared by RTZ).

For more information on the fault signals and errors, see pages 1-142 through 1-150 in Control Data manual 83325100.

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# DD40 SECTOR FORMAT

Each track in the 3340 is divided into 48 sectors, twelve sectors on each of the four spindles. The following figure shows the format of one sector. The length of one sector is 4198 bytes or 1866 servo bytes. The sector I.D. is six bytes in length. The first three bytes contain the actual I.D. of head, cylinder and sector. These three bytes are used on the 2EJ to detect when the correct sector is under the heads. The fourth byte is all zeros. The last two bytes contain the defect parameter which is protected by three bits of parity. The defect parameter is used on the 2EK to point to where within the data field the defect appears. When the head reaches the defect in the data field, the defect parameter is used to disable the read or write logic until the 17 byte defect pad has passed under the data head.

The bottom half of the diagram shows a data field without a defect and one with a defect. Notice that the last gap (Gap 3) is 17 bytes shorter when there is a defect than when there is no defect. The same amount of data is written in the data field and the sector has the same number of total bytes whether or not there is a defect. The data field is followed by four bytes of Error Correction Code (ECC) which is generated by the 2EK on the data field. Gap 3 is normally 21 bytes if there is no defect present in the data field or 4 bytes if a defect exists in the data field. There are two sync bytes in each sector, one prior to the I.D. and the other prior to the data field.



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Figure 3-1 shows the cable connections between a DCU-5 in the IOS and a DC-40. Each controller in the DC-40 is connected to a DCU-5 by a bus-in and bus-out cable. Two DCU-5's can be connected to each controller (one through the A port and one through the B port). One DCU-5 can access a controller at a time.

The cable between the DCU-5 and the DC-40 is normally 50 ft long, but it can be up to 80 ft long.

Figure 3-2 shows the DD-40 drive configuration and bulkhead cable ports. Figure 3-3 shows the cable connections of a DC-40 controller to primary and shadow DD-40's.

Each controller can be cabled to a primary and a shadow DD-40. A controller has eight cables, four A cables and four B cables. The four A cables are connected to four IN ports, one for each drive, in the primary DD-40. If there is a shadow DD-40 on the controller, A cables are connected from OUT ports on the primary DD-40 to IN ports on the shadow DD-40.

Two B cables are connected from the controller to the primary DD-40 and two to the shadow DD-40. Each B cable contains identical sets of signals. One B cable contains the signals for spindles A and B and the other contains the signals for spindles C and D. Each B cable separates into two cables, one for each spindle, when it goes from the bulkhead to the back of the DD-40. Unlike the A cables, the B cables are not daisychained from the primary to the shadow DD-40. Separate B cables carry the B cable signals from the DC-40 to the shadow DD-40.

The A and B cables are connected from the bulkhead to the back of the spindles. The cables that make this connection are 10 in. longer for a given spindle than for the spindle below it. If a shadow DD-40 is not connected to the controller, a terminator on the primary DD-40 terminates the A cable signals. If a shadow DD-40 is connected, A cables take the signals from the spindles to the OUT ports on the bulkhead, from which they can be linked to the shadow DD-40. The A cables are terminated on the shadow DD-40.

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# Figure 3-1. DC-40 to IOS Communication

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	Drive A
	Drive B
	Drive C
	Drive D
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Figure 3-2. DD-40 Drive Configuration and Bulkhead

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Figure 3-3. DC-40/DD-40 Cabling Diagram

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Table 3-1 lists the pin assignments for the A cable that connects the DC-40 controllers to the primary and shadow DD-40s. Table 3-2 describes the A cable signals.

Si	ignal Name	Inverted Pin	Normal Pin
Si Ur Ur Ur Ur Ta Ta Ta Ta Bu Bu Bu Bu Bu Bu Bu Bu Bu Bu Bu Bu Bu	ignal Name nit select Tag nit select 1 (Bit 0) nit select 2 (Bit 1) nit select 3 (Bit 2) ag 1 - Cyl select cover 106-55 ag 2 - Hedd Addr., upper 2 cyl ddd ag 3 - control bits ag 4 2 select status ag 5 2 select status as 0 as 1 as 2 as 3 as 4 as 5 as 6 as 7 as 8 as 9 catus 0 catus 1 catus 2 catus 3 catus 4 catus 5	Inverted Pin	Normal Pin 52 53 54 56 31 32 33 60 57 34 35 36 37 34 35 36 37 38 39 40 41 42 43 39 40 41 42 43 49 47 46 45 58 50
St St Op Bu Sp	catus 6 catus 7 pen cable detect asy pindle sequence pick	18 25 14 21	48 55 44 51 29 2 c . N
SE	pindle sequence hold		59 \$ 9* <sup>1</sup> %

# Table 3-1. A Cable Pin Assignments

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Signal	Description	
Unit select tag	This signal is sent to the drive along with unit select bits 0 through 2 to select the desired unit.	
Unit select bits O through 2	These signals must be active at least 200 ns before the unit select tag becomes active. Only unit select bit 0 is used by the DC-40 to select either the primary $(2^0 = 0)$ or shadow $(2^0 = 1)$ DD-40. (Unit select bit 3 is used on tag 5.)	
Tag 1	Lower cylinder select, bits 2 <sup>0</sup> through 2 <sup>9</sup> . (When doing a cylinder select, the higher bits must be sent first.)	
Tag 2	Head select/higher cylinder bits. Head select bits are represented in bus-out bits $2^0$ through $2^4$ . The upper cylinder bits $(2^{10})$ and $2^{11}$ are represented by bus-out bits $2^7$ and $2^8$ . (The upper cylinder bits must be sent before the lower cylinder bits.)	
Tag 3	Enable the control bits to be sent out on the bus. When the bus-out bit is active, it controls the following in the XMD:	
	<ul> <li>2<sup>0</sup> - Write gate</li> <li>2<sup>1</sup> - Read gate</li> <li>2<sup>2</sup> - Offset - offsets positioner toward the spindle.</li> <li>2<sup>3</sup> - Offset - offsets positioner away from the spindle.</li> <li>2<sup>4</sup> - Clear fault</li> <li>2<sup>5</sup> - Not used</li> <li>2<sup>6</sup> - RTZ</li> <li>2<sup>7</sup> - Data strobe early</li> <li>2<sup>8</sup> - Data strobe late</li> <li>2<sup>9</sup> - Not used</li> </ul>	
Tags 4 and 5	Selected status	

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Table 3-2. XMD A Cable Signals (continued)

Signal	Description
(See the trouble shooting section for a description of the individual status words.)	Tag 4 - Sector status Tag 5 - Extended status BOBO = 0 BOB1 = 0 Tag 5 - Operating status BOBO = 1 BOB1 = 0
Tags 4 and 5	Selected status
	Tag 5 - Diagnostic status BOBO = 0 BOB1 = 1 Tag 5 - Diagnostic execute status BOBO = 1 BOB1 = 1
Open cable detect	Disables the DD-40 when a loss of power in the DC-40 occurs.
Pick	DC-40 ground
Hold	DC-40 ground
Bus-in bits 0-7	Drive status or selected status

Table 3-3 lists the pin assignments for the B cable that connects the DC-40 controllers to the primary and shadow DD-40s. Table 3-4 describes the B cable signals.

Signal Name	Inverted Pin	Normal Pin
Ground	A	B
Servo Clock 24.2 mHz	b	C
Read Data	a	V
Ground	D	E
Read Clock 24.2 mHz	d	e

Table 3-3. B Cable Pin Assignments

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Table	3-3.	в	Cable	Pin	Assignments	(continued)
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Signal Name	Inverted Pin	Normal Pin
Signal Name Write Clock 24.2 MHt Ground Write Data Unit Selected Seek End On Cyl Ground Index Sector Ground Ground Ground Servo Clock Read Data Ground Read Clock Write Clock Ground Write Data Unit Selected Seek End	Inverted Pin w F f J h y JJ GG NN AA MM DD FF j K m N P S r	Normal Pin x G g H i z KK HH PP BB LL CC EE k L CC EE k L n P q R S
Ground	T T	S U
Sector Ground	v C	W X
Ground	Y	Z

The B cable signal for spindles A and B share one 55-pin cable between the DC-40 and the DD-40. The B cable signals for spindles C and D are shared by another cable.

# Table 3-4. XMD B Cable Signals

Signal	Description
Write data	NRZ data to XMĐ

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# Table 3-4. XMD B Cable Signals (continued)

Signal	Description
Write clock	Clocks write data into the drive (24 MHz/41.3 ns)
Servo clock	Used by the DC-40 to synchronize the transfer of write data to the servo clock (24.192 MHz/41.3 ns)
Read data	NRZ data from XMD
Read clock	24 MHz/41.3 ns
Seek end	Seek end with on-cylinder indicates the seek was completed as expected. Seek end without on-cylinder indicates a seek error. When a diagnostic execute status is performed, seek end indicates test execution is complete.
Unit selected	This is the response to a unit select tag and a match between the unit select bits and drive address.
Index	Decoded from servo tracks once per revolution.
Sector	Twelve sector pulses per revolution. This is determined by the setting on the sector switches.

Table 3-5 gives the part numbers of the drop and interconnect cables for the DCU-5, DC-40, and DD-40. The reference numbers correspond to the numbers on Figure 3-3.

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Cable	Number
DC-40 to DCU-5 Interconnect Cables	1 Cable PN 10559201 Socket PN 01106500 Plug PN 01106600
DC-40 Drop Cables (to DCU-5)	2 Bus In Cable PN 02203500 Bus Out Cable PN 02203501 55 Pin Socket PN 01106500 55 Pin Plug PN 01106600
DC-40 Drop Cables (to DD-40)	3 A and B Cables PN 12021000 61 Pin Plug PN 01110400
DD-40 to DC-40 and DD-40 to DD-40 Interconnect Cables	A and B Cables PN 01110500
DD-40 Bulkhead to Disk Drive Cables	<ul> <li>(3) A Cable - 70" - PN 12019700</li> <li>(7) - 80" - PN 12019701</li> <li>(6) - 90" - PN 12019702</li> <li>(5) -100" - PN 12019703</li> </ul>
	9 B Cable - 70/80" - PN 12019800 -90/100" - PN 12019801
A and B Cable 61-Pin Bulkhead Connector	PN 01234600
A Cable 60-Pin Flat-Cable- Type Connector	PN 01311300
B Cable 26-Pin Flat-Cable- Type Connector	PN 01311200

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This section is a theory of operations for the modules of the DC-40. The DC-40 has the following modules:

- 2EI channel interface module receives data from the DCU-5 on a write and passes data to the DCU-5 on a read.
- 2EB full-track buffer module buffers read and write data.
- 2EM disk multiplexer module provides control for reads and writes.
- 2EJ disk controller module controls an XMD spindle in the DD-40.
- 2EK disk-data and error-correction module performs error correction and defect detection on data read from the disk.

A DC-40 has four controllers. Each controller has four 2EJ modules and one of each of the other modules. A controller can control one primary and one shadow DD-40, each of which has four XMD spindles.

The DC-40 adapts the signals and protocol of the DCU-5 to the spindles in the DD-40. The DC-40 performs the following functions:

- Controls up to 32 DD-40s.
- Buffers read and write data transfers between the DCU-5 and the DD-40s.
- Passes control functions to the selected spindles.
- Generates error-correction codes for write data.
- Checks read-correction codes and and computes a correction vector for correcting read data.
- Controls the distribution of read/write data over 48 sectors per cylinder using 12 sectors from each of the four spindles.
- Passes status from the spindles to the DCU-5.

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Figure 4-1 is a chassis map of the DC-40. Figure 4-2 is a block diagram of the DC-40.

## 4.1 2EI MODULE

The 2EI module (see figure 4-3) receives write data from the DCU-5 and sends it to the 2EB module's full-track buffer. The 2EI module also receives read data from the full track buffer and sends it to the DCU-5. There are two ports on the 2EI module, so that data can be received from or sent to different locations on each port. Port A or B must be selected before data can be sent through the port. The port is selected with either a select the port function (010007) or a select the DD-40 drive function. A 010001 select code specifies the shadow DD-40 and a 010000 select code specifies the primary DD-40.

## 4.1.1 2EI MODULE - FUNCTION DECODE

When the DC-40/DD-40 receives a function code from the DCU-5, a 4-bit function code is latched into the F terms and a corresponding 16-bit function parameter is latched into the A terms. (Port A or B must be selected.) The same clock is used to clock in the function code, the function parameter, and data when doing a write. Once the function code and function parameter are latched, the function code is sent to the function decode. At the same time, the function code and function parameter go to the parity checking circuit.

The following three conditions block the go function (term QO) from going to the 2EM module: command error (term B12), parity error (term F41), and diagnostic mode (term F30). Two clock periods (CPs) pass after the function is latched before go function (term R48) and the function code (terms R49 through R52) are sent to the 2EM module. They are followed by the function parameter in the next 4 CPs, 4 bits each CP.

## 4.1.2 2EI MODULE - WRITE

When data is received from the DCU-5, it passes through the U terms and is latched in terms A20 through A36 for port A or terms A40 through A56 for port B (terms A36 and A56 are parity bits.) The data and the parity bit are sent to the parity checking circuit. If a parity error is detected on a data transfer, it is flagged in the general status. From the A terms, the data enters terms A0 through A15 and is latched in the M terms. Terms M0 through M15 receive the even parcels and terms M20 through M35 receive the odd parcels. The odd parcels go to bank A and the even parcels go to bank B on the 2EB module.

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Figure 4-1. DC-40 Chassis Map

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