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ENGINEERING NOTE

CRAY-1/CDC 7600/CYBER 76 PPU CHANNEL INTERFACE

Start Date: Jul 31, 1978
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This Engineering Note defines the hardware and operational characteristics of a CRAY-1 Interface that allows I/O communications between a CRAY-1 normal speed asynchronous I/O channel and an I/O channel of a Control Data 7600 or CYBER 76 Peripheral Processor Unit (PPU) channel.

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-	Jul 31, 1978	Start Date.
A	Aug 14, 1978	Original Release. This document is intended to replace two other Engineering Notes previously issued for the CRAY-1 / CDC 7600 PPU Interface. These two Engineering Notes were originated 2 July 1976, and 1 March 1977 and are now obsolete.

Each time this Engineering Note is revised, all changes issued against the previous version are incorporated into the new version and the new version is assigned an alphabetic level. Each page changed by revised information has the revision level applied in the lower right-hand corner. Requests for copies of Cray Research, Inc. Engineering Notes may be directed to:

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CDC 7600/CYBER 76 PPU CHANNEL INTERFACE

1.0 SCOPE

This document defines the hardware and operational characteristics of a CRAY-1 Interface that allows I/O communications between a CRAY-1 normal speed asynchronous I/O channel and an I/O channel of a Control Data 7600 or CYBER 76 Peripheral Processor (PPU) channel.

2.0 APPLICABLE DOCUMENTS

The following Cray Research publications are applicable:

2240001 CRAY-1 Site Planning Manual
2240012 CRAY-OS Version 1 System Programmers Handbook
2240638 CRAY-1 I/O Channel Engineering Specification
2240966 CRAY-1 Channel Adapter Engineering Note

The following Control Data publications are applicable:

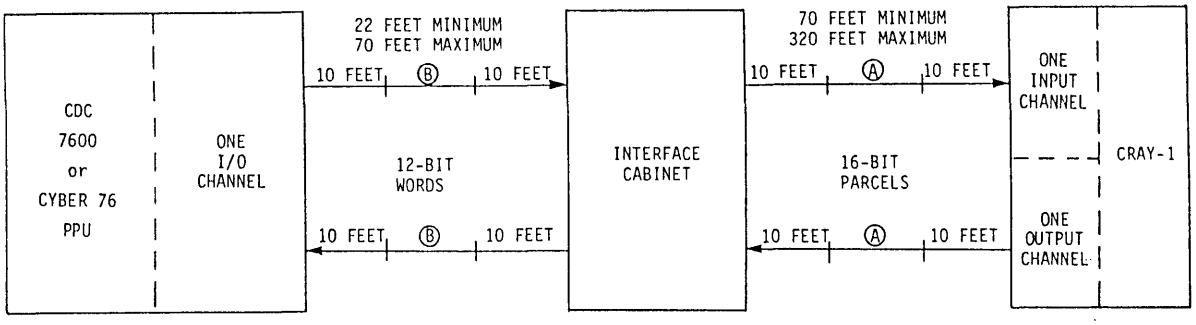
60367200 CYBER 76 Hardware Reference Manual
60408700 CYBER 76 I/O Specifications
60274900 AB101-A PPU Theory Of Operation

Operations not covered by this engineering note will meet the requirements set forth in the above documents.

3.0 REQUIREMENTS

3.1 GENERAL DESCRIPTION

The Interface allows asynchronous I/O communications between a CRAY-1 and a Control Data 7600 or CYBER 76 PPU in a full duplex mode of operation. The hardware interface is passive; it performs no operation other than passing data between the CRAY-1 and the PPU. No capability exists to accept function words or to return status words. The software is responsible for synchronizing the two processors. Figure 1 illustrates the connections between the devices. In the normal configuration, the Interface would be placed as close to the 7600 as possible.



NOTE:

1. THE INTERCONNECTING LOGIC CABLES, Ⓐ , ARE AVAILABLE IN PRECUT LENGTHS IN 50 FOOT INCREMENTS RANGING FROM 50 FEET UP TO 300 FEET.
2. THE INTERCONNECTING LOGIC CABLES, Ⓑ , ARE AVAILABLE IN PRECUT LENGTHS OF 2 FEET, 30 FEET, AND 50 FEET.
3. THE 10 FOOT PPU CHANNEL DROP CABLES CONNECTED TO THE PPU BACKPANEL MUST BE SUPPLIED BY THE CUSTOMER.

Figure 1. Interface Connections

3.2 FUNCTIONAL DESCRIPTION

3.2.1 MODE SELECTION

The Interface is capable of operating in either of two manually selectable modes -- normal speed mode or high speed mode. A switch mounted inside the interface cabinet is used to select the desired mode. In high speed mode, once the first word of a block is transferred, the Interface anticipates the word flag/ resume handshake to gain the additional speed. For this reason only block transfer instructions should be executed by the PPU when in this mode. All I/O instructions are allowed in the normal speed mode.

3.2.2 TRANSFER RATES

The slowest device in the communications link determines the maximum transfer rate. The CRAY-1 side of the Interface is capable of transferring data at 64 megabits/second regardless of the cable length between the CRAY-1 and the Interface. The maximum transfer rate of the 7600 side of the Interface is a function of the mode of operation and the cable length between the 7600 and the Interface. Table 1 summarizes the possible transfer rates on the 7600 side of the Interface.

Table 1. 7600 Transfer Rates (Megabits/Sec)

Cable Length	Normal Speed		High Speed	
	Input	Output	Input	Output
22 Feet	36.4	36.4	80.0	72.7
50 Feet	31.2	31.2	80.0	62.3
70 Feet	29.1	29.1	80.0	54.5

3.2.3 DATA HANDLING

The Interface accepts 16-bit parcels of data from a CRAY-1 output channel, disassembles them into 12-bit PPU words, and passes them to a PPU input channel. Alternately, it accepts 12-bit words of data from a PPU output channel, assembles them into 16-bit parcels, and passes them to a CRAY-1 input channel; an output record flag must be transmitted at the end of the data block to complete the data transfer. Parcels are assembled/disassembled from left to right as shown in figure 2.

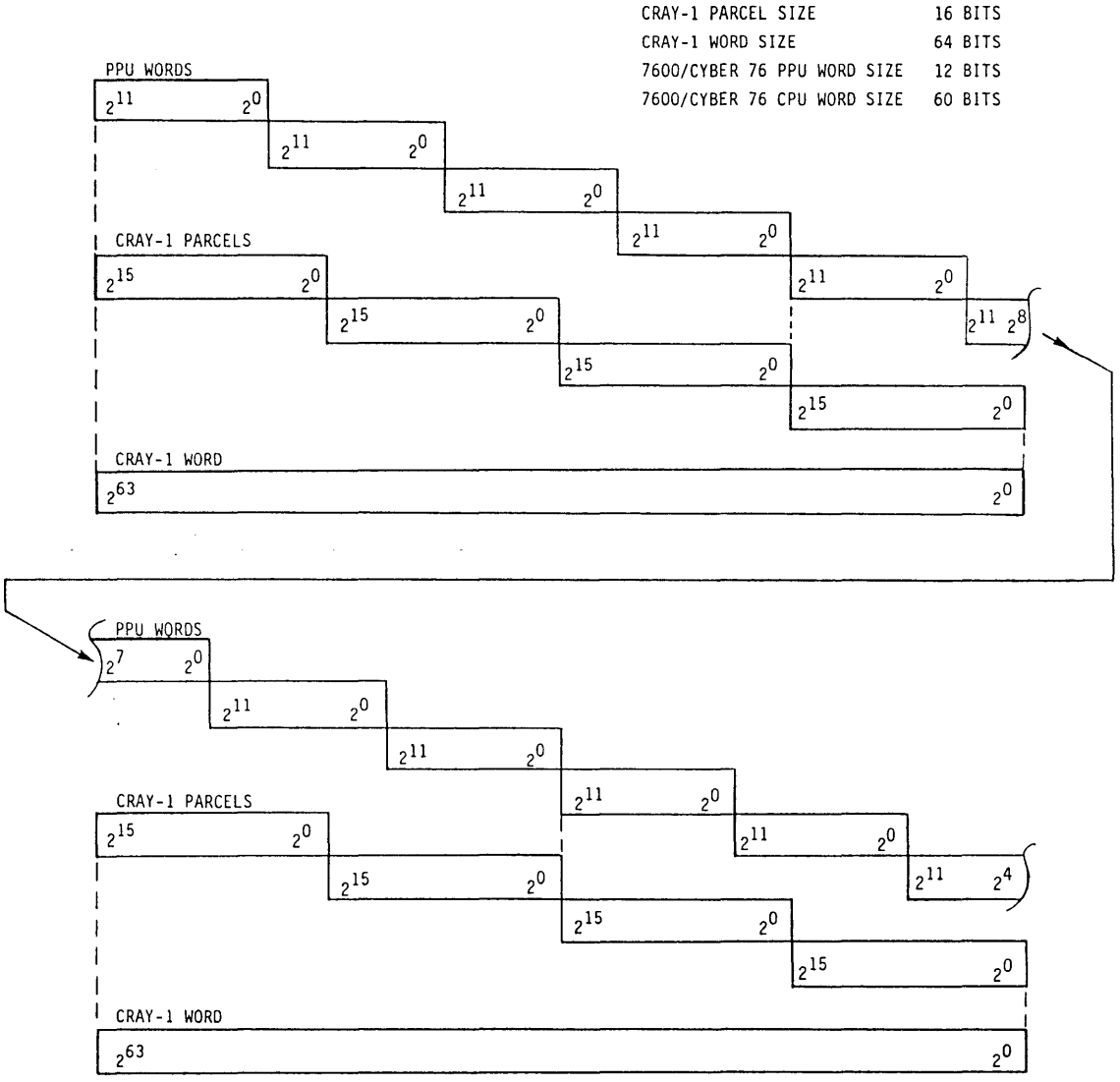


Figure 2. Parcel Assembly/Disassembly

If the number of 16-bit parcels transferred is not a multiple of three, or if the number of 12-bit PPU words transferred is not a multiple of four, the last parcel of the data block does not fall on a parcel boundary. In this case, the low order bits of the last parcel or last PPU word are zero-filled.

3.2.4 RECORD SIZE

Data records from the CRAY-1 may be any non-zero integer number of parcels in length. The minimum length of records from the PPU is two 12-bit words.

3.2.5 PARITY

Each 16-bit parcel of data to/from the CRAY-1 has a six-bit single error correction/double error detection (SECDED) code appended to it. Corrective action for a multiple-bit error is a software function. No parity bits are used for data to/from the PPU channel.

3.2.5.1 CRAY-1 OUTPUT DATA ERROR

An uncorrectable data error occurring in the data from the CRAY-1 to the Interface is reported to the 7600 by means of a short transmission. That is, the last 12-bit word of the data block is not transmitted to the PPU. The input record flag is not inhibited. The CRAY-1 is not notified by the hardware of the error condition.

3.2.5.2 CRAY-1 INPUT DATA ERROR

If an uncorrectable data error occurs in a transmission from the Interface to the CRAY-1, the CRAY-1 input channel's error flag will go set. The data transfer will continue, as if no error had occurred. When the input disconnect signal is received at the end of the data block, the channel generates an

I/O interrupt request. The routine which services the interrupt will then check the state of the channel error flag. At this point, any corrective action is a function of the software.

3.2.6 INTERFACE LOGIC SIGNALS

Figure 3 illustrates the logic signals interconnecting the Interface logic with a CRAY-1 I/O channel and a PPU channel. The characteristics of all signals connected to the CRAY-1 meet the requirements of CRI specifications for the CRAY-1 long-line channel adapter. The characteristics of all signals connected to the PPU meet the requirements of specifications for the 7600/CYBER 76 PPU channel as described in CDC publication 60408700. The timing relationships for these signals are illustrated in figures 4 through 7.

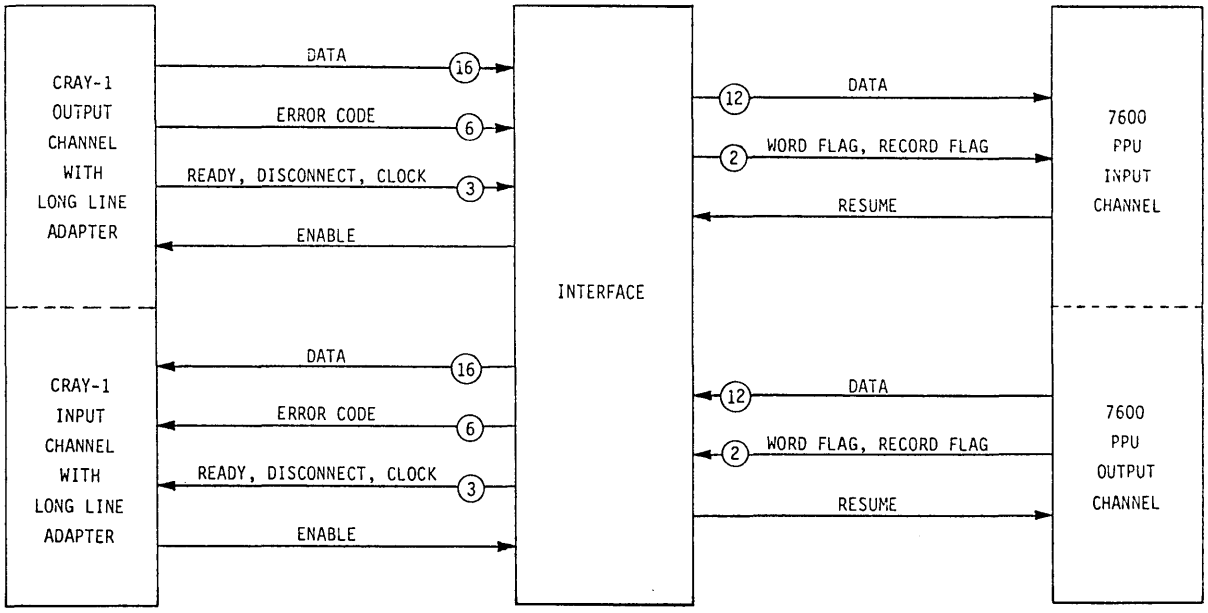


Figure 3. Interface Logic Signals

PULSE TIMES

t_1 45 ± 5 nsec.

t_2 145 ± 5 nsec.

t_3 6 to 7 PPU clock periods plus cable delay both ways.

t_4 20 ± 2 nsec if CRAY-1 output data is available in Interface buffer register, otherwise 18 ± 2 nsec after CRAY-1 output ready arrives.

t_5 20 ± 2 nsec after last input word resume.

TIMING NOTES

① All signal times are those seen at the Interface end of the logic cables.

② Assumes PPU is executing an input instruction. If not, t_3 becomes 8 or 13 PPU clock periods plus cable delay one way after IAM is loaded into PPU's Fd register or 3 PPU clock periods plus cable delay one way after IAN is loaded.

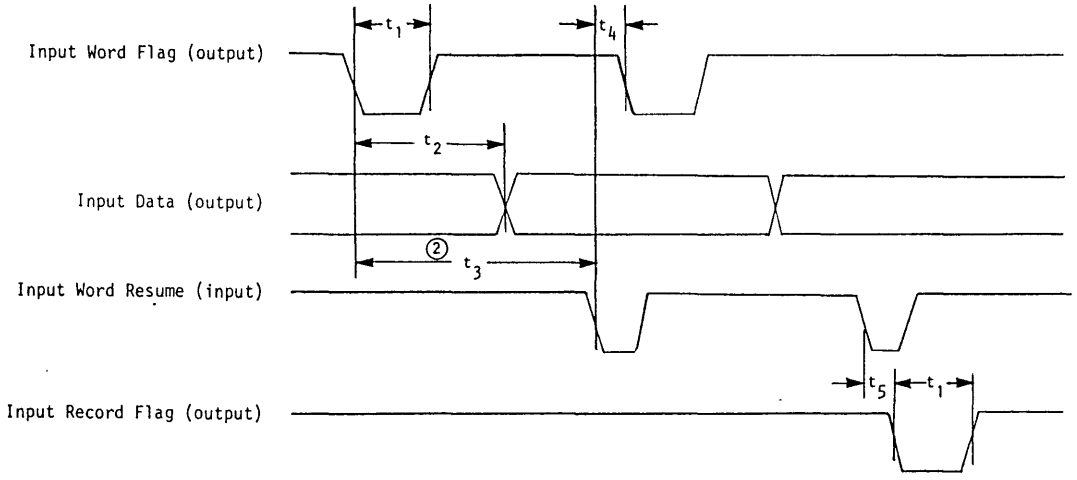


Figure 4. PPU Signal Timing, Normal Speed Input

PULSE TIMES

t_1	45 ± 5 nsec.
t_2	145 ± 5 nsec.
t_3	First word only - 6 to 7 PPU clock periods plus cable delay both ways.
t_4	Second word only - 20 ± 2 nsec.
t_5	145 ± 5 nsec after last input word flag is transmitted.
t_6	See note ④: Word 0 to word 1, 210 ± 5 nsec. Word 1 to word 2, 250 ± 5 nsec. Word 2 to word 3, 145 ± 5 nsec. Word 3 to word 0, 145 ± 5 nsec.

TIMING NOTES

① All signal times are those seen at the Interface end of the logic cables.

② The input word resume only has significance when it is the response to the first input word flag of a block.

③ Assumes PPU is executing an input instruction. If not, t_3 becomes 8 or 13 clock periods plus cable delay one way after IAM is loaded into the PPU's Fd register.

④ PPU words are defined as follows:

CRAY-1 PARCELS →

WORD 0	WORD 1	WORD 2	WORD 3

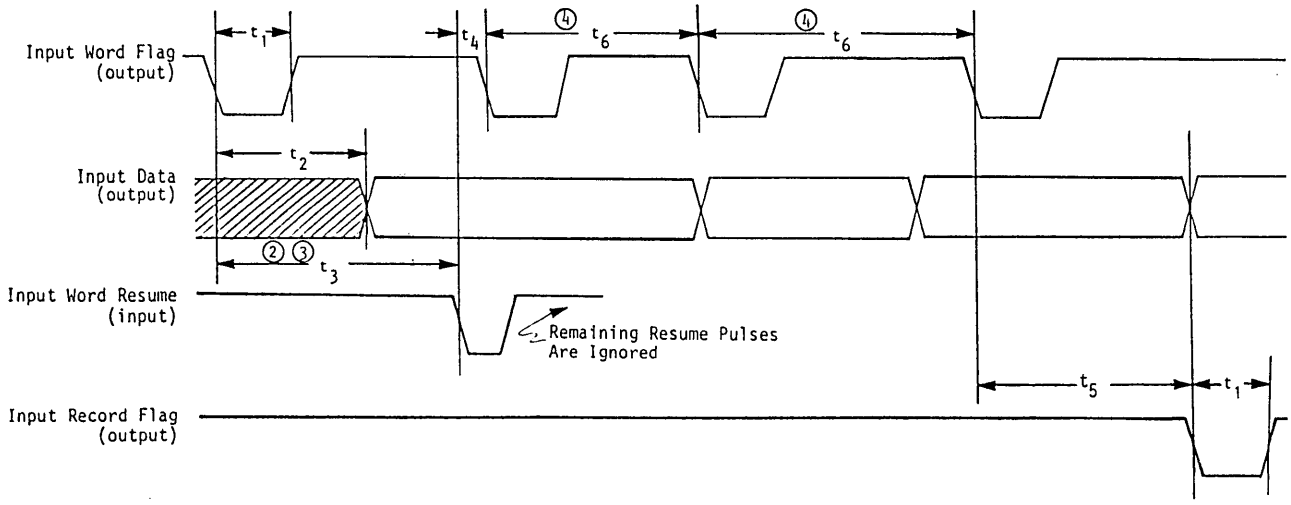


Figure 5. PPU Signal Timing, High Speed Input

PULSE TIMES

t_1 20 nsec minimum.

t_2 5 nsec maximum.

t_3 16 ± 2 nsec if Interface input buffer is empty, otherwise 35 ± 5 nsec after CRAY-1 input resume is received.

t_4 45 ± 5 nsec.

t_5 0 nsec minimum.

t_6 0 nsec minimum after last output word flag.

TIMING NOTES

① All signal times are those seen at the Interface and of the logic cables.

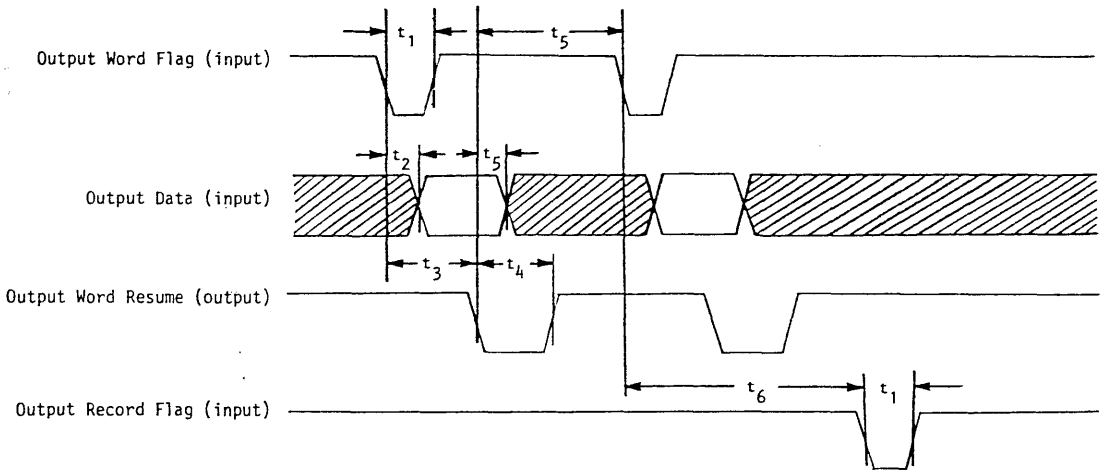


Figure 6. PPU Signal Timing, Normal Speed Output

PULSE TIMES

t_1 20 nsec minimum.

t_2 5 nsec maximum.

t_3 16 ± 2 nsec if Interface input buffer is empty, otherwise 35 ± 5 nsec after CRAY-1 input resume is received.

t_4 45 ± 5 nsec.

t_5 0 nsec minimum.

t_6 0 nsec minimum after last output word flag.

t_7 160 ± 5 nsec, after first output word resume only.

TIMING NOTES

(1) All signal times are those seen at the Interface end of the logic cables.

(2) If the Interface input buffer register is full, causing t_3 to be extended, the second output word flag after the current one will be received 6-7 PPU clock periods plus cable delay both ways after the output word resume is transmitted.

PARAMETER	TIME IN PPU CLOCK PERIODS		
	22 FEET	50 FEET	70 FEET
t_8, on 1st OWF only	10	14	16
t_9, every other word	5	5	5
t_9, alternate words	7	9	11

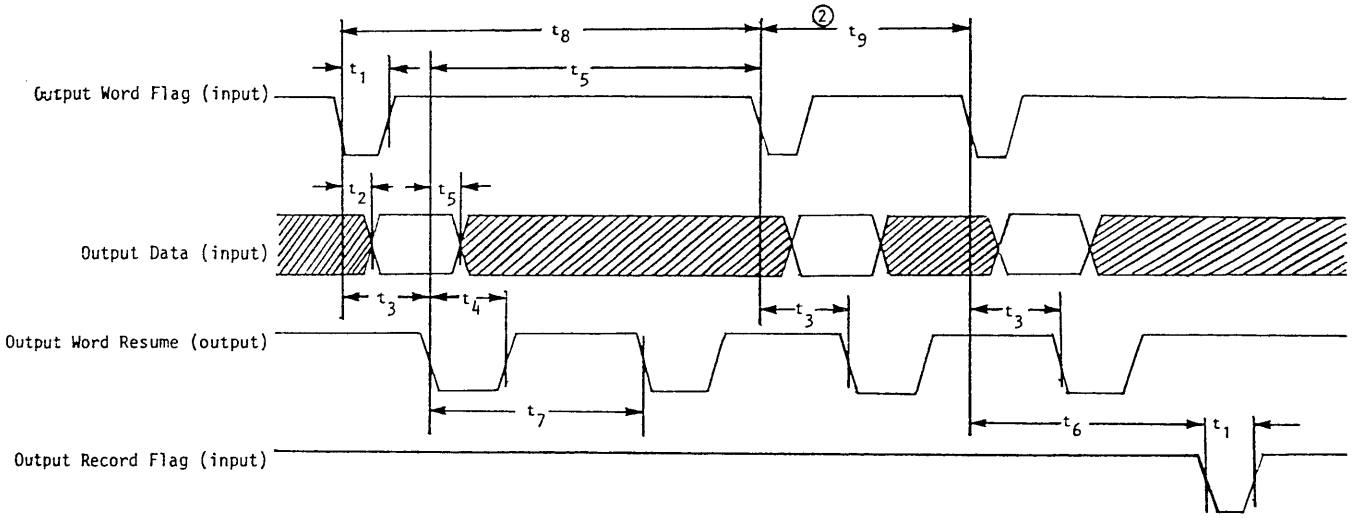


Figure 7. PPU Signal Timing, High Speed Output

4.0 PROGRAMMING CONSIDERATIONS

4.1 SOFTWARE PROTOCOL

A strict protocol must be followed to assure that each transmission is completed prior to the next transmission. Either processor (CRAY-1 or 7600) may be designated as the master processor, however, the CRAY-1 is typically the slave processor. Refer to the CRAY-OS System Programmer's Handbook for a description of the CRAY-1 protocol.

Figure 8 illustrates a suggested software protocol. In terms of the CRAY-1 CRAY-OS software protocol, this example illustrates sending one LCP and one subsegment in both directions.

Note that the software maintains the CRAY-1 input channel open at all times to allow the 7600 to start an error recovery at any time.

7600/CYBER 76	CRAY-1
	1. Wait for six-word control package (LCP). a. Activate input channel for LCP b. Wait for interrupt.
2. Send six-word control package (LCP). a. Execute output instruction. b. Send record flag.	
	3. Receive LCP. a. Clear input channel interrupt. b. Clear output channel interrupt. c. Activate input channel for segment using information in LCP. d. Wait for interrupt.
4. Send segment. a. Execute output instruction. b. Send record flag.	
	5. Receive segment. a. Clear input channel interrupt.
	6. Send LCP. a. Activate output channel with LCP. b. Activate input channel for LCP. c. Wait for interrupt.
7. Receive LCP. a. Wait for input word flag. b. Execute input instruction. c. CRAY-1 disconnect generates input record flag which terminates input instruction. d. Check word count for short transmission indicating a data error.	
	8. Send segment. a. Clear output interrupt b. Activate output channel with segment. c. Wait for interrupt.
9. Receive segment. a. Wait for input word flag. b. Execute input instruction. c. CRAY-1 disconnect generates input record flag which terminates input instruction. d. Check word count for short transmission indicating a data error.	
	10. Process output termination. a. Clear output interrupt. b. Wait for interrupt on input channel.
11. Repeat sequence by starting at step 2.	

Figure 8. Suggested Software Protocol

4.2 DATA ERRORS

Reporting of data errors depends on where the error occurred.

1. Uncorrectable data errors occurring on a transmission from the Interface to the CRAY-1 are reported by setting the CRAY-1 channel error flag for the applicable input channel. This, in turn, generates an error interrupt request to the CPU which occurs upon receiving the input disconnect at the end of the data block.

2. Uncorrectable data errors occurring on a transmission from the CRAY-1 to the Interface are indicated by means of an incomplete data block being received by the 7600 PPU. That is, the number of PPU words passed on from the Interface to the PPU is one word less than the number of words in the actual data block. For this reason, the PPU program should always check the number of words received against the expected word count.

3. Since no parity bits are used on the PPU channel, data errors occurring between the PPU and the Interface are not detected by the hardware.

4.3 HIGH SPEED MODE

4.3.1 PPU OUTPUT

If, while in high speed mode, there is a gap in the data stream, all words transferred after the gap are transferred at the normal speed rate. High speed operation will be resumed upon receipt of the output record flag. Such a gap in the data stream will occur if one-word output instructions (OAN) are used or if more than one block output instruction (OAM) is used to transfer the entire block of data.

4.3.2 PPU INPUT

Once the resume for the first word of a PPU input block has been received, the Interface streams data to the PPU at a nearly constant rate without checking for the presence of subsequent resumes. If the PPU uses one-word input instructions (IAN) or a block input instruct (IAM) with a word count less than the actual block size, data will be lost.

4.4 UNEQUAL BLOCK LENGTHS

4.4.1 CRAY-1 OUTPUT

If the number of 16-bit parcels in the CRAY-1 output data block is less than or equal to 3/4 of the number of 12-bit words in the PPU input block length, the CRAY-1 output disconnect signal generates an input record flag to terminate the data transmission.

If the CRAY-1 output block length is greater than 3/4 of the input block length, the outcome depends on the mode of operation selected.

- In normal speed mode, the CRAY-1 output channel hangs waiting for a subsequent PPU input. Since the Interface is fully duplex, no loss of data occurs, even if the PPU performs an output operation before the subsequent input which reads the remaining words in the stacked up data block.

- In high speed mode, all CRAY-1 output data transferred to the PPU after the PPU instruction completes until a subsequent input instruction is executed is lost. If the remainder of the data block is completely transmitted to the PPU before a subsequent PPU input is initiated, the last word in the oversized block will be received by the PPU as the first word of the next block, and the new block will appear to contain one additional 12-bit word which could cause the whole process to be repeated if it causes the new block to become too large.

4.4.2 CRAY-1 INPUT

If the number of 12-bit words in the PPU output data block is less than or equal to 4/3 the number of 16-bit parcels in the CRAY-1 input block length, the output record flag generates a CRAY-1 input disconnect signal to terminate the data transmission. If the output block length is greater than 4/3 of the input block length, all CRAY-1 input ready signals received after CA becomes equal to CL cause the CRAY-1 channel error flag to set, resulting in a series of CPU interrupt requests. Resumes are returned for all parcels received, but those parcels in the data block which are received after CA equals CL are lost. Similarly, data is lost if the PPU initiates an output when the CRAY-1 input channel is not active.

4.5 INITIALIZATION

4.5.1 MASTER CLEAR

The Interface logic may be master cleared by any of the following methods:

- A CRAY-1 channel master clear signal generated by the CRAY-1 MCU during CPU deadstart time.
- A programmable CRAY-1 channel master clear generated by setting the input channel's current address (CA) equal to its limit address (CL).
- Two successive output record flags from the 7600 PPU.

If the master clear is received from the CRAY-1, the Interface will send a stream of output word resumes and input record flags to the 7600 PPU at a 4 MHz rate for as long as the master clear signal is applied. If the master clear is generated by the 7600, a single output word resume is returned to the PPU.

4.5.2 7600 MASTER CLEAR SEQUENCE

It is recommended that the 7600 PPU instruction sequence shown in figure 9 be used when master clearing the Interface from the 7600 to prevent hanging the Interface.

```
1.  RFN  n     Send ORF on interface channel.
2.  SHN  18    Delay
3.  NOM  *+3   Done if output word resume returned.
4.  RFN  n     Send second ORF.
```

Figure 9. PPU Comand Sequence for Master Clear

4.5.3 CRAY-1 CHANNEL CONSIDERATIONS

The following CRAY-1 channel characteristics should be considered whenever initializing the Interface.

1. The CRAY-1 channel pair is not affected by a master clear generated by the 7600 PPU. After a master clear operation by the 7600, communications may be reestablished by the software using short message blocks.

2. A programmed CRAY-1 channel master clear only affects the CRAY-1 input channel. It is suggested that a clear interrupt instruction be executed for the output channel in conjunction with the programmed master clear operation.

3. The CRAY-1 output channel is only master cleared when the CPU is dead-started by the MCU.

4. If a clear interrupt instruction (0012j0) is executed for the output channel while the channel is engaged in transferring data, the channel is deactivated and the data transfer is halted, but no disconnect is sent to indicate end of transmission.

5. If the CRAY-1 output channel is busy transferring data when the interface is master cleared by other than a CRAY-1 dead start, the output channel continues to transmit data but the data transmitted while the master clear signal is present is lost. The amount of data lost depends upon which master clear method was used. Zero to thirteen parcels will be lost as a result of a master clear from the 7600 PPU. The length of the programmed CRAY-1 master clear is determined by software. All parcels transmitted during this time are lost at a rate of one parcel every 250 nsec (20 clock periods). However, rather than wait for the output channel to flush itself in this manner, it is recommended that a clear interrupt instruction be executed for the output channel during the programmed master clear operation. This will halt the flow of data and the missing disconnect will be satisfied by the master clear operation.

4.6 ABNORMAL CONDITIONS

This section describes what will most likely happen as seen from the 7600 PPU if the Interface or the CRAY-1 channel pair catastrophically fails due to a power loss or to a failure in either unit's control logic. (A failure is considered catastrophic if the CPU is unable to service the interrupt).

4.6.1 INTERFACE POWER LOSS

If the Interface loses power or if the cables to the PPU are disconnected, all of the PPU channel's differential line receivers will assume an indeterminate logic level. This problem is a characteristic of the 7600 line receiver.

4.6.2 PPU INPUT

If, during a 7600 input operation, either the CRAY-1 output channel or the Interface fails catastrophically or if the CRAY-1 loses power, the PPU input channel hangs waiting for an input word flag or an input record flag.

4.6.3 PPU OUTPUT

If, during a 7600 output operation, either the CRAY-1 input channel or the Interface fails catastrophically or if the CRAY-1 loses power, the PPU output channel hangs waiting for an output word resume.

5.0 MAINTENANCES FEATURES

5.1 SPECIAL TEST CONFIGURATIONS

If only one processor (either the CRAY-1 or the 7600 PPU) is connected to the Interface, partial testing of the Interface may be performed by using special jumper cables to loop the output data back around to the input on the disconnected side of the Interface.

5.2 SECDED NETWORK

Since no user indication is given of a single bit error occurring on the data paths between the Interface and the CRAY-1, the error correction feature may be disabled during diagnostic testing to isolate individual bit failures.

6.0 PHYSICAL CHARACTERISTICS

6.1 CABINET

The Interface logic is contained in a separate air-cooled cabinet. Refer to the CRAY-1 Site Planning Reference Manual for dimensions and floor cutout locations. The unit weighs approximately 100 pounds.

6.2 CABLE LENGTH RESTRICTIONS

Refer to figure 1 for maximum and minumum cable lengths.